HIGH VOLTAGE, HIGH POWER DENSITY ELECTRONIC POWER CONDITIONERS FOR MICROWAVE POWER MODULES (MPMS)

THESIS

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By

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PREFACE

I, Joel Malcolm Holland, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

All the work described in this thesis was carried out in the Department of Power Electronics, Motors, and Drives at Newcastle University under the supervision of Professor Volker Pickert, Professor Mohammed E. Elgendy, and Gary Henderson of CPI TMD Technologies. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others except as specified in the text and summarised in the Statement of Contributions.

This dissertation is not substantially the same as any that I have submitted, or is being concurrently submitted, for a degree or diploma or other qualification at Newcastle University or any other University or similar institution. It does not exceed 100,000 words, including footnotes, tables, and figures but excluding bibliography, appendices, and any supporting data.

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I would like to thank my best friend within the Power Electronics, Machines and Drives Lab, Mohammed Mahfuz Kamal, with whom I spent most of my time during this doctorate. Our discussions, both serious and light-hearted, made my time at the university much easier. I give thanks to Runo Nielsen who continuously provided me with invaluable assistance regarding the design of series-parallel resonant power converters. Without his detailed knowledge and assistance on this topic it would have remained absolute mystery for years to come.

I would finally like to thank my family. Without their support, completion of this journey would not have been possible. I am eternally grateful to my mother and father who continue to support me in my endeavours in every way possible.

ABSTRACT

Recent advancements in Wide Bandgap (WBG) semiconductor devices have enabled the next generation of power electronics. Applications such as battery electric vehicles and consumer electronic chargers are increasingly incorporating these devices to achieve substantial improvements in achievable power density through increased switching frequencies, enhanced efficiency, and superior thermal performance. High voltage applications such as Electronic Power Conditioners (EPCs) for Microwave Power Modules (MPMs) strive to optimize design for power density to minimize payload weight for Traveling Wave Tube (TWT) based radar transmission systems within airborne applications such as Unmanned Aerial Vehicles (UAVs). There is a significant lack of research regarding the utilization of WBG transistors in such systems with frequencies approaching 1MHz. This thesis begins by giving a brief introduction to the requirements for an EPC within an MPM system, such as the requirement for ultra-low-noise outputs due to the relationship between AC voltage variations and phase-noise performance of the radar transmission process and the required controller bandwidth to ensure adequate voltage regulation under periodic, highly dynamic variations within the output loading depending on the required operating mode. An in-depth literature review is performed to give an overview of current state-of-the-art high voltage converters, transformer design, and advanced control techniques in the scientific literature and commercial products. A novel hybrid fully independently controlled DC/DC converter is proposed for the collector and cathode electrodes of the TWT to allow individual optimization for their specific requirements. A series-parallel resonant converter is proposed for the collector electrode, processing 600W of power at an output voltage of -3kV with a variable switching frequency of between 176kHz-300kHz. The cathode regulator, which is critical for phase-noise performance, consists of a fixed-frequency resonant active-clamped fly-back converter operating at frequencies of at least 600kHz, delivering an output power of 60W at voltages of -6kV. A comprehensive discussion of the effects of excessive transformer parasitic capacitance and how this affects maximum achievable switching frequency is discussed. It is demonstrated within this work that commonly accepted equations for the active clamp fly-back converter are no longer valid as the switching frequency approaches the transformer's Self-Resonant Frequency (SRF) where significant parallel resonant behaviour exists. Simulation results of both converters are presented including steady-state performance and dynamic response against multiple radar transmission regimes. An additional four-element multi-resonant active clamp fly-back converter is simulated which can achieve substantially higher gain and bandwidth through reductions in magnetizing inductance. A set of practical results are presented which illustrate the suitability of the proposed topologies through generation of significantly high voltage potentials at elevated switching frequencies with WBG devices which agree well with proposed design procedures. Due to the high frequency nature of the converter, significant issues such as EMI generation and inductive coupling into sensitive feedback lines have limited the ability to form a closed-loop controller. A comprehensive set of recommendations are provided for further work to mitigate these issues.

TABLE OF CONTENTS

NOMENCLATURE

ACF: Active Clamp Fly-back

ACMC: Average Current Mode Control

ADC: Analogue-to-Digital Converter

AM: Amplitude Modulation

BJT: Bipolar Junction Transistor

CCM: Continuous Conduction Mode

CHMC: Charge Mode Control

CMC: Current Mode Control

CSA: Current Sense Amplifier

CW: Continuous Wave

DCM: Discontinuous Conduction Mode

DSP: Digital Signal Processor

ECM: Electronic Countermeasures

EMC: Electromagnetic Compatibility

EMI: Electromagnetic Interference

EPC: Electronic Power Conditioner

EW: Electronic Warfare

FHA: Fundamental Harmonic Approximation

FRA: Frequency Response Analyzer

GaN: Gallium Nitride

HHC: Hybrid Hysteretic Control

MMIC: Monolithic Microwave Integrated Circuit

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

MPM: Microwave Power Module

PCB: Printed Circuit Board

PM: Phase Modulation

PRC: Parallel Resonant Converter

PRF: Pulse Repetition Frequency

PSFB: Phase Shifted Full Bridge

PWM: Pulse Width Modulation

RADAR: Radio Detection and Ranging

RF: Radio Frequency

RHPZ: Right-Half Plane Zero

RMS: Root Means Squared

SMPS: Switched Mode Power Supply

SRC: Series Resonant Converter

SRF: Self-Resonant Frequency

SSPA: Solid-State Power Amplifier

TWT: Travelling Wave Tube

UAV: Unmanned Aerial Vehicle

VCO: Voltage Controlled Oscillator

VIC: Voltage Injection Control

VMC: Voltage Mode Control

WBG: Wide Bandgap

LIST OF SYMBOLS

A_C: *Collector Regulator Series-to-Parallel Capacitor Ratio*
A_P: *Phase Pushing Factor*
C_{C_e}: *Cathode Output Capacitance*
C_{CL}: *Active Clamp Capacitance*
C_{eq_L}: *Series-Parallel State Equivalent Capacitance*
C_{eq_P}: *Parallel State Equivalent Capacitance*
C_{f1}: *First Second-Stage Filter Output Capacitance*
C_{N_L}: *Equivalent Series Capacitance of Collector Regulator*
C_{P_F}: *Parallel Resonant Fly-Back Capacitance*
C_{P_L}: *Collector Parallel Resonant Capacitance*
C_{R_F}: *Fly-Back Converter Lumped Switched Node Resonant Capacitance*
C_{S_L}: *Physical Series Resonant Capacitor for Collector Regulator*
C_{T_L}: *Total Effective Capacitance of Collector Regulator*
D_F: *Fly-Back Switch Duty Cycle*
D'_F: *Clamp Switch Duty Cycle*
F_{BW}: *Controller Effective Bandwidth*
f_{c_F}: *Fly-Back Cross-Over Frequency*
$F_{C_{Losc}}$: *Sub-Resonance Oscillation Frequency*
F_{RF}: *RF Frequency of TWT in GHz*
F_{R_z}: *Right Half-Plane Zero Frequency*
F_{S_F}: *Fly-Back Switching Frequency*
$F_{S_{R_{TX}}}$: *Fly-Back Transformer Self-Resonant Frequency*
$I_{CL_{pp}}$: *Peak-to-Peak Clamp Capacitor Current*
$\widetilde{I_{in_L}}$: *Collector Converter Peak Tank Input Current*
$\widetilde{I_{in_{rms_L}}}$: *Collector Converter Peak Tank Input Current (RMS Value)*
I_{L_M}: *Magnetizing Current*
$I_{L_{M_L}}$: *Peak Magnetizing Current during Series-Parallel State*
$\ddot{I}_{L_{M_L}}$: *Adjusted Magnetizing Current due to Sub-Resonance*
$I_{L_{M_P}}$: *Peak Magnetizing Current during Parallel State*
$I_{L_{R_L}}$: *Peak Resonant Inductance Current during Parallel State*
$I_{L_{R_P}}$: *Peak Resonant Inductance Current during Parallel State*
I_{O_C}: *Collector Output Current*
I_{O_F}: *Average Fly-Back Output Current*
I_{o_L}: *Series-Parallel State Output Current*
I_{o_P}: *Parallel State Output Current*
$I_{S_{1F(pk)}}$: *Fly-Back Switch Peak Current*
k_l: *AC-Voltage Coefficient of Series-Parallel State*
k_p: *AC-Voltage Coefficient of Parallel State*
k_{v_L}: *Series-Parallel State Voltage Coefficient*
k_{v_P}: *Parallel State Voltage Coefficient*
$L_{M_{F_p}}$: *Fly-Back Converter Primary Magnetizing Inductance*
L_{R_F}: *Fly-Back Converter Series Resonant Inductance*
L_{S_L}: *Collector Converter Series Resonant Inductor*
L_T: *Pin-to-Pin Length of TWT*
M_{i_C}: *Current Input-to-Output Transfer Function*
M_{v_C}: *Voltage Input-to-Output Transfer Function*
N_C: *Collector Transformer Effective Turns Ratio*
N_F: *Fly-Back Converter Transformer Turns Ratio*
P_{O_F}: *Fly-Back Converter Output Power*
Q_d: *Second-Stage Filter Damping Quality Factor*
Q_{S_L}: *Collector Converter Series Loaded Quality Factor*
R_{Coeff}: *Resistive Load Coefficient*
R_{dC_1}: *Damping Resistance of First Filter Capacitor*
R_{dC_2}: *Damping Resistance of Second Filter Capacitor*
$R_{d_{Lf}}$: *Damping Resistance of Filter Inductor*
R_{eq_L}: *Equivalent Load Resistance during Series-Parallel State*
R_{eq_P}: *Equivalent Load Resistance during Parallel State*
$R_{n_{LCC}}$: *Equivalent Series Load Resistance of Collector Load*
R_{O_C}: *Actual Collector Output Resistance*
R_{O_F}: *Fly-Back Actual Output Resistance*
$T_{C_{L_{osc}}}$: *Clamp Oscillation Period*
T_{Dop}: *Optimum Dead-Time Delay*
$T_{F_{off}}$: *Fly-back Switch Off-Time*
T_{S_F}: *Fly-Back Converter Switching Period*
$\widetilde{V_{AC}}$: *Cathode AC Voltage Variation*
V_{CA}: *Cathode Voltage in kV*
V_{CL}: *Active Clamp Voltage*
$V_{CL_{INIT}}$: *Initial Clamp Voltage*
$V_{CL_{PK}}$: *Peak Clamp Voltage*
$\widetilde{V_{CL_r}}$: *Multi-Resonant Fly-Back Clamp Voltage (RMS)*
V_{CO_P}: *First Output Capacitor Voltage of Full-Bridge Voltage Multiplier*
V_{CO_L}: *Second Output Capacitor Voltage of Full-Bridge Voltage Multiplier*
$V_{C_{P_{L_{pk}}}}$: *Peak Parallel Capacitor Voltage during Series-Parallel State*
$V_{C_{P_L}}$: *Collector Parallel Resonant Capacitor Instantaneous Voltage*
$\overline{V_{C_{P_L}}}$: *Collector Parallel Resonant Capacitor Initial Voltage*
$V_{C_{P_P}}$: *Peak Parallel Capacitor Voltage during Parallel State*
V_{DC}: *DC Input Line Voltage*
V_{D_L}: *Series-Parallel State Output Diode Voltage*
V_{D_P}: *Parallel State Diode Voltage*
V_{DS_F}: *Fly-Back Switch Drain-Source Voltage*
V_{eq_L}: *Equivalent Source Resistance of Collector Regulator*
$V_{L_{R_L}}$: *Series Resonant Inductor Voltage during Series-Parallel State*
$V_{L_{R_P}}$: *Series Resonant Inductor Voltage during Parallel State*
V_{O_C}: *Collector Output Voltage*
V_{O_F}: *Fly-Back Converter Output Voltage*
V_{O_L}: *Effective Series-Parallel State Output Voltage*
V_{O_P}: *Effective Parallel State Output Voltage*

$\widehat{V_{T_r}}$: *Multi-Resonant Fly-Back Effective Tank Input Voltage (RMS)*
V_{TXF}: *Fly-Back Converter Transformer Primary Voltage*
$V_{TX_{HPL}}$: *Series-Parallel State Peak Transformer First Harmonic*
V_{TX_L}: *Series-Parallel State Actual Transformer Peak Voltage*
$V_{TX_{HPP}}$: *Parallel State Peak Transformer First Harmonic*
V_{TX_P}: *Parallel State Actual Transformer Peak Voltage*
$X_{C_{CL}}$: *Clamp Capacitor Impedance*
X_{C_L}: *Impedance of Collector Series Resonant Capacitor*
$X_{C_{P_F}}$: *Parallel Capacitor Impedance*
$X_{C_{P_F}//C_{CL}}$: *Effective Parallel Impedance of Series-Parallel State*
X_{L_L}: *Impedance of Collector Series Resonant Inductor*
$X_{L_{R_F}}$: *Series Resonant Inductor Impedance*
Z_{T_L}: *Tank Input Impedance of Collector Regulator*

α: *Fly-Back Efficiency*

β_L: *Series-Parallel State Transformer Phase Angle*
β_P: *Parallel State Transformer Phase Angle*

ϑ_S: *Input-to-Output TWT Phase Shift*

φ_{PH}: *Spurious Phase Modulation*

$\Im_{C/S}$: *Carrier-to-Sideband Ratio in dB*

δ_C: *Collector Output Diode Conduction Period*
δ_L: *Output Diode Conduction during Series-Parallel State*
δ_P: *Output Diode Conduction during Parallel State*

ΔV_{CL}: *Clamp Voltage Deviation*
$\Delta V_{C_{tr}}$: *Transient Voltage Deviation*
$\Delta I_{C_{tr}}$: *Transient Load Current Step*

ω_{e_L}: *Modified Angular Frequency during Series-Parallel State*
ω_{e_P}: *Modified Angular Frequency during Parallel State*

ω_{h_f}: *Upper Frequency of Second-Stage Output Filter*
ω_{n_F}: *Normalised Angular Frequency of Multi-Resonant Fly-Back*
ω_{n_L}: *Normalized Angular Switching Frequency of Collector Regulator*
$\omega_{n_{L_{est}}}$: *Estimated Normalised Angular Frequency*
$\omega_{n_{req_L}}$: *Required Normalised Angular Series Resonant Frequency*
ω_{o_L}: *Collector Converter Series Angular Resonant Frequency*
$\omega_{o_{L_{est}}}$: *Estimated Normalised Angular Series Resonant Frequency*
$\omega_{o_{Lp}}$: *First Angular Parallel Resonant Frequency of Multi-Resonant Fly-Back*
$\omega_{o_{Ls}}$: *Angular Series Resonant Frequency of Multi-Resonant Fly-Back*
$\omega_{o_{Pp}}$: *Second Angular Parallel Resonant Frequency of Multi-Resonant Fly-Back*
ω_{P_L}: *Unloaded Parallel Resonant Angular Frequency of Collector*
ω_{s_L}: *Collector Converter Angular Switching Frequency*
$\omega_{s_{L_{est}}}$: *Estimated Normalised Angular Switching Frequency*

$\aleph$: *Normalised Angular Frequency Adjustment Factor*

ϖ_c: *Frequency Limitation Coefficient*

Π: *Alternative Load Coefficient*
Π_F: *Alternative Load Coefficient for Fly-Back Converter*
Π_L: *Alternative Load Coefficient for Series-Parallel State*
Π_P: *Alternative Load Coefficient for Parallel State*

θ_C: *Collector Rectifier Diode Conduction Angle*
θ_{CA}: *Output Diode Conduction Angle*
θ_L: *Series-Parallel State Conduction Angle*
θ_P: *Parallel State Conduction Angle*

γ: *Dimensionless Load Coefficient*

AIMS AND OBJECTIVES

The main aims of this research are to research, design, and prototype a small, lightweight, and efficient converter that may be utilized to generate the main high voltage power supply for a mini-TWT utilized within an MPM. These devices are typically employed as either radar transmitters or jammers, and therefore the RF noise performance is a critical parameter. Output voltage noise and ripple within the electrodes is directly translated by the TWT directly into RF noise, and the solution must prioritise minimizing these factors particularly during steady state. When used as a radar transmitter, the TWT grid voltage is modulated to switch the beam current on and off. This grid voltage is typically generated by a separate converter and does not need to be considered within this research except for its direct influence on the converter loading. When the beam current is switched off by the grid, the cathode, collector, and helix (earth) currents are effectively zero. When the electron beam is turned on, most electrons will flow from the cathode to the electrode with a small proportion (~5%) reaching the TWT body, held at earth potential. Pulsed radar transmitters operate in many different modes ranging from long, slow pulses for high position fidelity and short, fast pulses for accurate dynamic tracking. As a result, the power converter design must be able to operate with load changes from zero to maximum at rates from 100Hz to 100kHz. The dynamic performance of the cathode is of utmost importance, and dynamic variations within the output voltage must be minimized. This is typically achieved by the insertion of large amounts of output capacitance, which will typically constrain the size of the rectifying network. For an MPM mounted in an airborne application, further factors substantially constrain the size and weight of the solution, such as the isolation transformer and the heat-sinking system. The objectives to address the above are outlined briefly, below:

1. Perform an in-depth analysis of current topological approaches and identify the preferred solution.

2. Operate the converter at a considerably high frequency to explore the relationship between switching frequency, converter miniaturisation, controller bandwidth, and RF transmission performance which are critical to overall system performance.

3. Explore the use of new, wide-band gap semiconductor devices to exploit their enhanced characteristics when compared to traditional silicon device within high frequency modern power conversion applications.

4. Explore the limitations of such techniques and devices when utilized within systems operating under high voltage potential conditions within the multi-kilovolt range.

STATEMENT OF CONTRIBUTIONS

Research regarding the utilization of WBG semiconductor devices in modern power converters is typically focused on the generation of lower voltage output within the range of 12-400V. Although small amounts of research have been performed to investigate their use within higher voltage applications such as for the electrodes of a TWT, this has typically been constrained to voltages substantially less than would be required and furthermore does not investigate the influence of a shared common output. Therefore, this research aims to expand on previous research and provide the following contributions:

- Provides both a detailed discussion regarding the requirements of a power converter for a TWT utilized within an MPM system and an in-depth topological review of standard switching DC/DC converter topologies, discussing strengths and weaknesses of each with respect to the required specifications.

- Provides a detailed discussion of the current body of research and the limitations regarding the implementation of high switching frequencies within high voltage applications utilizing capacitively filtered outputs, such as the transformer parasitic components, rectifier load network, use of resonant switching techniques, and other substantial bottlenecks.

- Proposes a novel DC/DC switching topology that addresses the considerably disparate requirements of the cathode and collector electrodes of a TWT. Consisting of two parallel connected converters sharing the common DC input, the total load power is effectively partitioned to allow individual optimisations within the electrode to be powered. Further novelty is found regarding the exploration of the influence of additional parasitic components within an active-clamped fly-back converter and how this modifies both steady-state and dynamic converter characteristics across differing line and load conditions.

- Provides the first, full-scale experiments regarding the use of new WBG materials within high voltage EPCs within an MPM intended to be used within a multi-mode radar system. Provision of both in-depth simulation and practical results demonstrate the converter's ability to generate multi-kilovolt output voltages within a load system that is highly representative of an actual TWT at switching frequencies more than 600kHz to minimize size and weight, while enhancing both overall system efficiency and theoretical performance of the RF amplification process. A detailed discussion then follows, detailing how physical limitations of high voltage applications and the bottlenecks still present significantly constrain one's ability to fully exploit semiconductor devices, particularly WBG devices, to their full effect.

1 INTRODUCTION

1.1 APPLICATION BACKGROUND

RADAR (Radio Detection and Ranging) is an object-detection system that uses radio waves to collect information regarding the distance, angle, and velocity of certain objects. A typical Radar system consists of a transmitter that emits radio waves toward a target, with a corresponding receiver that "listens" for signals that are reflected off the target. Depending on the application, this receiver may either be static and located within very close proximity to the transmitter or may be mounted within airborne equipment that moves relative to a target. Standard radar theory including an explanation of the Doppler Effect is presented in [1, 2]. For airborne electronic warfare (EW) and electronic countermeasure (ECM) applications specifically, for which this research is concerned, refer to [3].

This introduction will focus on the helical, gridded multi-mode TWT amplification process within pulsed multi-mode radars. Miniature versions of these devices, alongside a Solid-State Power Amplifier (SSPA), high voltage power supply, and associated control circuitry, to form a compact, rugged package designed for applications across land, sea, and air. Combining both solid-state and vacuum tube electronics provides an unbeatable RF amplification solution in applications where volume, weight, and prime power are at a premium. MPM technology has enabled high power transmission within the 2-40GHz range, while demonstrating an order of magnitude increase in RF output power per unit weight compared to standard TWT solutions [4].

1.1.1 *Travelling Wave Tube Amplifiers*

Improvements in radar technology is continuously required such that current state-of-the-art can stay ahead of countermeasures intended to deceive or block them. To have an effective anti-jamming radar would require novel techniques to enhance visibility while being jammed, coupled with the ability to shift frequency over a significantly wide bandwidth at fast speeds to avoid dwelling that would otherwise occur at the jammer source frequency [5]. Wide bandwidth systems allow amplification of wideband noise and may deceptively retransmit a hostile radar pulse to inhibit its ability to track position [6].

The TWT was the answer to the above issues, able to provide wide-frequency bandwidth amplification at sufficient gains, with improved output power and efficiency compared to previous amplification devices [7].

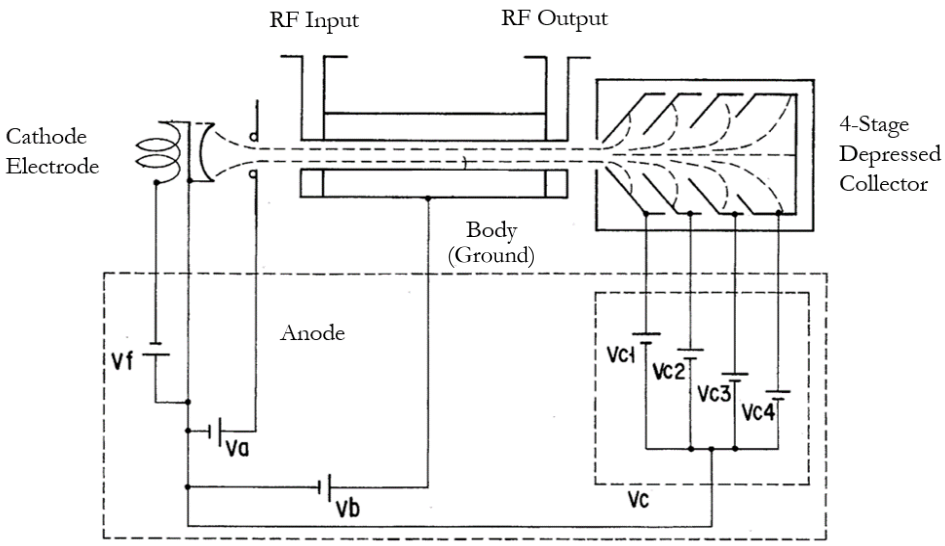

Fig.1: TWT Microwave Amplifier with Four-Stage Depressed Collector Configuration [8].

For complete TWT theory, refer to [9, 10]. In essence, TWTs consist of a cathode, a slow-wave structure, a magnetic focussing system, RF input and output couplers, and at least one depressed collector. The slow-wave structure consists of a helical coil which, in the absence of an electron beam, supports a travelling wave along the axis having a phase velocity substantially less than light. Thermionic emission from the cathode generates a stream of electrons that traverse the helix, causing electron bunching as they are accelerated or decelerated by the field wave components.

The electron beam travels at the initial velocity of electrons which is appreciably different to that of the wave phase velocity. The bunching of electrons within the beam results in a larger portion of electrons being decelerated than those being accelerated over any cross-section of the helix, resulting in transfer of energy from the electron beam to the travelling wave [11]. This produces an alternating space charge force that alters the wave field structure and consequently the phase velocity of the wave. Complete field theory of the amplification process is presented in [12].

This action causes significant amplification of the input RF signal as it travels through the helical structure and towards the collector. Electrons that did not contribute to amplification of the RF signal are intercepted by the collector and returned to the helix through an external supply. Increasing the number of depressed collectors at differing depressed voltage potentials from the cathode voltage allows notable improvements in the number of electrons that are recovered, substantially improving efficiency [13, 14].

1.1.2 Microwave Power Modules (MPMs)

In modern military applications, stringent requirements are imposed upon both the size and weight of the solution without sacrificing power or performance. MPMs combine high power, high efficiency, and wideband amplification properties of vacuum tube-based solutions and the low-noise signal processing capabilities of solid-state technologies to provide a complete microwave amplifier solution. When combined with an EPC to provide the necessary voltage potentials required within the amplifier, a complete, miniaturised device is formed that is particularly suitable for mounting in applications such as UAVs:

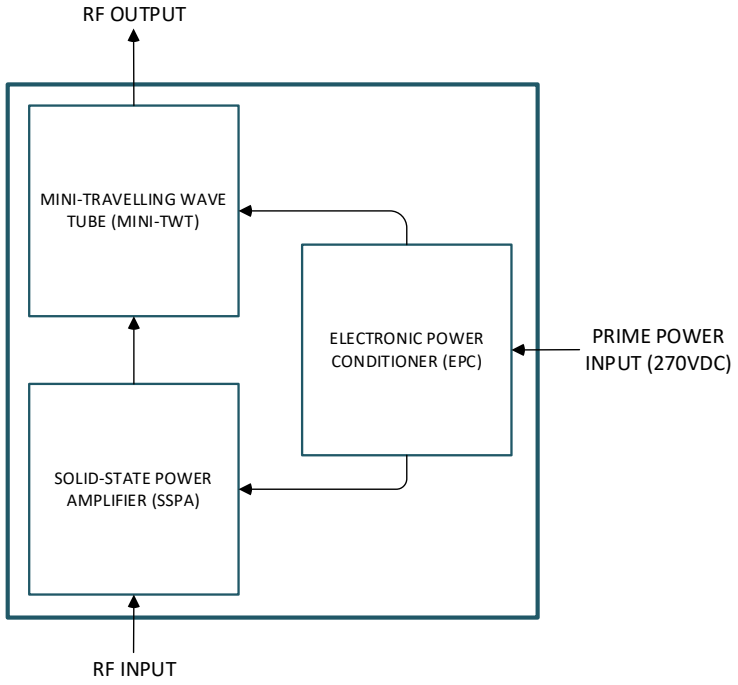

Fig.2: MPM Block Diagram Operating from 270VDC Prime Power DC Input.

Discrete solid-state RF-power devices began to appear at the end of the 1960s with the introduction of silicon bipolar transistors. The proliferation of new solid-state devices in the following century and consequently the utilization of new semiconductor materials began to offer amplification at frequencies up to 100GHz and above [15]. Such amplifiers may be grown as Monolithic Microwave Integrated Circuit (MMIC) structures to substantially improve performance of modular SSPA amplifier modules [16]. The inclusion of solid-state amplifiers in MPM systems serves multiple crucial purposes for enhancing TWT performance by partitioning the gain equally between the power amplifier and the TWT. Operating from a typical prime power of 270VDC +/- 10%, an MPM delivers anywhere from 50-200W of Continuous Wave (CW) RF power with gains >50dB spanning bandwidths exceeding two octaves with extremely low noise figures of <10dB. Although having lower power than standalone TWT systems, power combining of multiple units

is possible [17]. Ultra-compact, state-of-the-art MPM devices can be either narrow-band or wide-band, covering multiple frequency ranges, and can operate in both pulsed and CW mode depending on the application. Inclusion of solid-state electronics significantly enhances the performance of the microwave amplification process through RF input signal conditioning 18]. These enhancements include pre-amplification, equalisation, power enhancements, and linearization. The lattermost is of great importance, since under increasing RF input drive, extraction of energy from the emitted electron beam of a TWT is increased which causes it to slow down significantly. Phase modulation of the transmitted RF signal ensues, resulting in non-linear changes in gain and gain compression well below the RF output power saturation point. Through utilization of a SSPA linearizer, the point at which this compression occurs can be forced to a point much closer to the TWT saturation point, which is beneficial to the carrier performance characteristics of the tube and enables high power transmission [19]. SSPA solutions have also been shown to offer some level of compensation for AM/PM phase distortions that can significantly inhibit phase-noise performance of the amplification process [20].

1.1.3 Gridded Control and Multi-Mode Radar

Pulsed modulation wave amplification is particularly useful in military applications since this enables "multi-mode" operation depending on the frequency and duty cycle of a voltage applied to a grid control electrode. The choice of pulse repetition frequency (PRF) is critical to the performance of pulsed radar systems and has direct consequences on both the presence of range and Doppler ambiguities within the system [21, 22]. For very low PRFs, one can implement precise and resolute range measurements, at the expense of creation of Doppler ambiguities that are often too severe to be resolved. At very high PRFs, good noise-aspect capability exists – allowing high closing-rate targets to appear in the clutter-free region of the spectrum. This often precludes the use of simple, accurate pulse delay ranging techniques and reduces effectiveness regarding detection range against low-closing-rate targets due to sidelobe clutter. A full overview of the effects of implemented low, medium, and high PRFs is provided in [23]. PRFs utilized by airborne radars range from hundreds of hertz to several hundred kilohertz at X-band. This wildly varying dynamic behaviour imposes some difficult requirements on the design of the EPC:

- To minimize output load capacitance and enable high power density, controller bandwidth must be significantly elevated to account for the voltage excursions that occur due to dynamic changes in load current when the electron beam is modulated.

- Frequency and duty cycle of modulation can change at any time depending on the required mode of multi-mode radar; short, high frequency pulses of ~1-3% duty cycle at 100kHz for accurate dynamic tracking and long, slow pulses of ~50% duty cycle at 100Hz for high position fidelity. Load current changes from the full-load value to zero, with typical specifications stating that the maximum voltage excursion from the nominal value for an MPM must not exceed +/-5V for a -6,000VDC cathode voltage and +/-100V for a -3,000VDC depressed collector voltage during any transient event. This discrepancy, which will be explained in further detail in the following section, is to ensure adequate performance over all load transient conditions due to the criticality of phase-noise performance and its dependence on the stability of the cathode voltage imposed on the TWT.

- Steady-State Stability of the cathode voltage is of utmost importance for phase-noise performance. An AC voltage variation of below 0.1V is required for the cathode to ensure phase modulation of the transmitted RF signal does not occur. The cathode must return to the nameplate voltage during no-load before receipt of a new transmission control pulse.

1.1.4 Electronic Power Conditioner Design and Requirements

MPM efficiency is determined by the efficiencies of individual component parts. Increasing the efficiency of any individual component improves overall efficiency and reduces the burden of the heat-sinking system which often constrains achievable power density. Particularly for airborne applications, it is important that corresponding increases in performance throughout the amplifier chain are achieved without increases in size or weight. Utilization of WBG semiconductor devices promises significant efficiency improvements within the EPC, reducing temperature rise despite operating at elevated switching frequencies.

Radar transmitters are required to amplify low-noise coherent RF waveforms, which may be fixed frequency, frequency chirped, or phase modulated during any radar transmission. The transmitter must provide high-power amplification while preserving both RF signal coherence and fidelity. Minimizing transmitter phase-noise is essential for the radar's ability to detect moving-target signals superimposed on clutter signals [24]. EPCs may produce significant residual noise close to the radar carrier signal during amplification, composed of both Amplitude Modulated (AM) and Phase Modulated (PM) contributions. All electrode voltages within the system must be carefully controlled during CW operation and under any dynamic operating mode.

The cathode voltage has the largest influence on the phase-noise performance of the amplification process, where any AC voltage variations produce significant spurious AM and PM sidebands on the RF output as a direct result of phase modulation of the RF signal as it undergoes amplification within the slow-wave structure within the tube body. Near carrier noise and spurious outputs typically occur within 100Hz-500kHz of the carrier signal, with any other noise components being almost wholly caused by the ripple voltages of the electrodes of the tube. The production of AM sidebands within the output of the TWT are often up to 10dB lower than those produced by the PM sidebands, but AM noise must also be carefully controlled since this can cause PM noise through AM-PM conversion [25].

The required "pushing factors" directly dictate the maximum peak-to-peak cathode voltage ripple limits. AM/AM conversion refers to changes in the RF output voltage produced by variations in the input signal level. When increasing RF drive no longer produces corresponding increase in RF output power, the amplification process becomes non-linear, resulting in significant gain compression as the RF input power is further increased [26], causing degradation in tube output power:

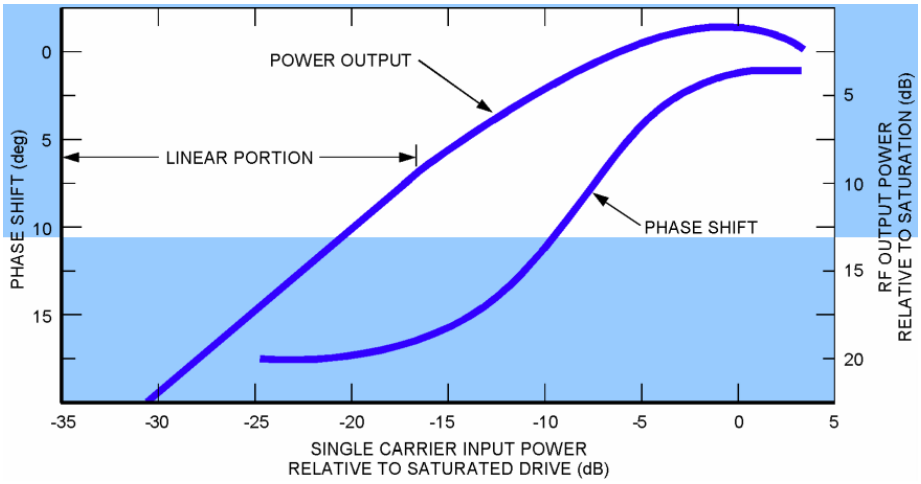

Fig.3: Power Output and Phase Shift as a function of RF Input Power showing the Linear and Saturated Amplification Points [27].

AM/PM distortion effects relate to changes in the phase angle of the RF output with changes in the RF input signal level. Ideally, the phase of the output RF signal is constant and stable with changes in the input signal RF amplitude. However, increases in the signal drive creates sharp rises in the experienced levels of AM/PM conversion of the tube, inducing an increase in the phase-length of the tube as the electron beam is slowed by energy transfer to the RF wave in the non-linear region, causing significant phase-shift in the RF output signal. The RF signal phase is

modulated by multiple time-varying factors that affect the electron beam velocity. Typical phase-pushing factors for variations in each of the TWT power supplies is given below:

- 100 degrees per 1% change in cathode voltage
- 10 degrees per 1% change in grid control voltage
- 0.00005 degrees per 1% change in collector voltage

Interestingly, AC voltage variations within the collector electrode voltage with respect to the tube body have very little effect on RF signal stability. The design of the cathode voltage regulator is, therefore, essential to avoid generation of spurious signal sidebands, and often low-noise operation of the cathode typically demands active filtering methods, with cathode voltage ripple specifications being smaller than one part in a million at steady state. Such techniques require the use of complex circuitry techniques, additional components, and critical PCB real estate. Additional active circuitry at the switching regulator output is often also included to increase the system bandwidth, allowing substantial improvements in accuracy with regards to cathode voltage control. To minimize the solution size within an MPM and enable maximum power density, it is becoming critical to eliminate the use of such circuits. To achieve similar bandwidth performance and ensure adequate attenuation of the significant AC voltage variations naturally exhibited due to fundamental and harmonic components of switching regulators, the MPM switching stages must be operated at switching frequencies considerably higher than their counterparts exploited in typical TWTs. The approximate value of phase-shift between the input and output RF signals can be approximated by:

$$\vartheta_s(°) = \frac{488 L_T F_{RF}}{\sqrt{V_{CA}}} \qquad (1.1)$$

Where ϑ_s is the total phase shift introduced by the TWT in degrees, L_T is the pin-to-pin length of the TWT from RF-input to RF-output in inches, F_{RF} is the RF frequency of operation in GHz, and V_{CA} is the cathode voltage in kilovolts. The phase-pushing factor A_P in degrees per Volt is a measure of the sensitivity of this phase-shift to changes in the electrode voltages:

$$A_P = \frac{d\vartheta_s}{dV_{CA}} = \frac{-0.163 L_T F_{RF}}{V_{CA}^{\frac{3}{2}}} \qquad (1.2)$$

The spurious phase modulation φ_{PH} created by the peak cathode AC voltage variation $\widetilde{V_{AC}}$ can be calculated using the calculated phase-pushing factor, as follows:

$$\varphi_{PH} = A_P \check{V}_{AC} \qquad (1.3)$$

The carrier-to-sideband ratio $\Im_{C/S}$ in decibels produced due to the peak phase shift caused by the AC voltage variations is:

$$\Im_{C/S} = 20 \log(0.5\varphi_{PH}) \qquad (1.4)$$

If several frequency components exist within the AC voltages of the cathode, it is necessary to calculate spurious phase-modulation that occurs due to each individual frequency component and any associated harmonics. This occurs due to variable switching frequency within the EPC, with each frequency generating an "infinite" set of phase-modulated sidebands. By operating the EPC at a fixed frequency, significant reductions in both the number and magnitude of PM sidebands that are present in the spectrum can be achieved. This effect is appreciably more important for the cathode electrode since the phase-pushing factor is substantially higher.

This brings to light an important design choice for the EPC that may substantially improve performance – is there a way to operate the critical cathode regulator at a fixed-frequency while operating the collector regulator at variable frequency, while maintaining exceptional phase-noise performance?

1.1.5 Dynamic Load Characteristics and Controller Bandwidth

Elevated switching frequencies have been continuously shown to enable significant improvements in controller bandwidth [28]. Although fast transient response is desirable, clear limits do exist [29], and extremely high bandwidths may lead to phase margin degradation, resulting in instability and oscillatory behaviour, producing substantial AC variations and thus instability within the cathode voltage. Very high bandwidths are often achieved with hysteretic methods [30, 31], but such systems are inherently unstable and occupy large, uncontrolled frequency spectra and are therefore not desirable for phase-noise performance optimization.

Switched Mode Power Supplies (SMPS) are considered nonlinear, time-varying systems. Up to half of the switching frequency, average small-signal modelling techniques allow approximation as linear systems to allow application of linear control stability analytical techniques [32]. This has been verified for operation in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) [33, 34], and places the first restriction on maximum controller bandwidth. To achieve appropriate phase and gain margins while ensuring flat closed-loop output

impedance, the implemented bandwidth should not exceed one-fifth of the switching frequency, with more conservative designs opting for values as low as one-tenth of this value.

By increasing the inverter switching frequency, additional time to recharge output capacitors following voltage droop caused by periods of RF amplification becomes available. Lower controller bandwidths may be implemented but require higher output capacitances. During a dynamic load current step of magnitude $\Delta I_{C_{tr}}$, a voltage deviation $\Delta V_{c_{tr}}$ occurs, the value of which is a direct function of the implemented controller bandwidth F_{BW} and electrode output capacitance C_{C_e}:

$$\Delta V_{c_{tr}} = \frac{\Delta I_{C_{tr}}}{2\pi F_{BW} C_{C_e}} \qquad (1.5)$$

Fortunately, the substantially reduced current demands within the cathode EPC allows implementation of reduced output capacitance for any given required AC voltage variation and voltage deviation during transient events. By implementing separate voltage regulators for the cathode and collector, differing controller bandwidths may be implemented to provide individual optimization depending on the requirements of the electrode which the controller is intended to operate.

2 LITERATURE REVIEW

2.1 HIGH VOLTAGE ELECTRONIC POWER CONDITIONERS

Due to the constantly changing requirements of TWTs and the environments in which they are employed, the development of suitable accompanying EPC has shown continuous improvements with time. The selection of the appropriate EPC topology is contingent on the method of microwave amplification, the environment within which the amplifier is expected to perform, and the input power supply that is readily available for the application. Although a 270VDC prime power DC bus is standard for aerospace applications following rectification of a 115VAC, three-phase 400Hz source, applications such as space-based or satellite TWTs operate from a 28VDC prime power bus and require significant differences within the EPC. This section will introduce and critically review current state-of-the-art regarding EPC design.

To give a complete overview, the review is not constrained to EPCs operating within MPMs but also discusses the strengths and weaknesses of topologies implemented for higher power amplifiers, as well as those operating from lower voltage buses in space and satellite applications which also require high power density techniques. This review will also be concerned with information regarding high voltage transformer design, complex/fixed-frequency control techniques, and identifies a substantial lack of research regarding the utilization of WBG devices for achieving the high switching frequencies necessary for both low-noise and high bandwidth operation in multi-mode radar supplies.

2.1.1 *Self-Driven Oscillator Regulators*

An oscillator is any circuit that produces continuous, repeated AC waveforms from a DC voltage without external input control signals. In early supplies, Class C Meissner vacuum tube self-driven oscillators with inductively coupled windings generated 6,000V from a primary input source of 300V [35]. It was understood even in 1946 that transformer parasitic capacitance played an important role in converter dynamics, with this oscillator utilizing natural resonances between this capacitance and the magnetizing inductance of a coupled winding. Automatic self-regulation of the output voltage was achieved with a further winding that provides voltage feedback to allow variation in the frequency of oscillation across differing line and loading conditions.

Despite the inherent operating frequency limitations of vacuum tube electronics, their extensive use within earlier power systems allowed remarkable reductions in both the transformer and output filter size while simplifying elaborate and expensive insulation processes when compared to earlier solutions which often operated directly from AC mains supplies.

The generation of sinusoidal AC currents and voltages within any power distribution system has multiple benefits. Non-sinusoidal waveforms, such as square wave, consist of a multitude of additional harmonics beside the fundamental frequency, causing additional losses within the transformer, reduced efficiency, additional heating, and a greater impact on the required heat sinking requirements within the overall system. Generation of both radiated and conducted Electromagnetic Interference (EMI) at a multitude of frequencies may also significantly induce additional concerns regarding Electromagnetic Compatibility (EMC) such as control loop interference and the requirement for complex shielding techniques to comply with stringent military standards.

In applications that require high voltages with low-current biasing, noise levels of less than 100 microvolts in 100MHz noise bandwidths have been achieved through incorporation of switching topologies that focus on minimization of high frequency harmonic content [36]. Since self-oscillating methods achieve regulation through automatic adjustment of the switching frequency, they may be detrimental to phase-noise characteristics of a given TWT.

One example of a typical self-driven oscillator that could be exploited for the generation of low-noise high voltage outputs is shown below in Fig.4:

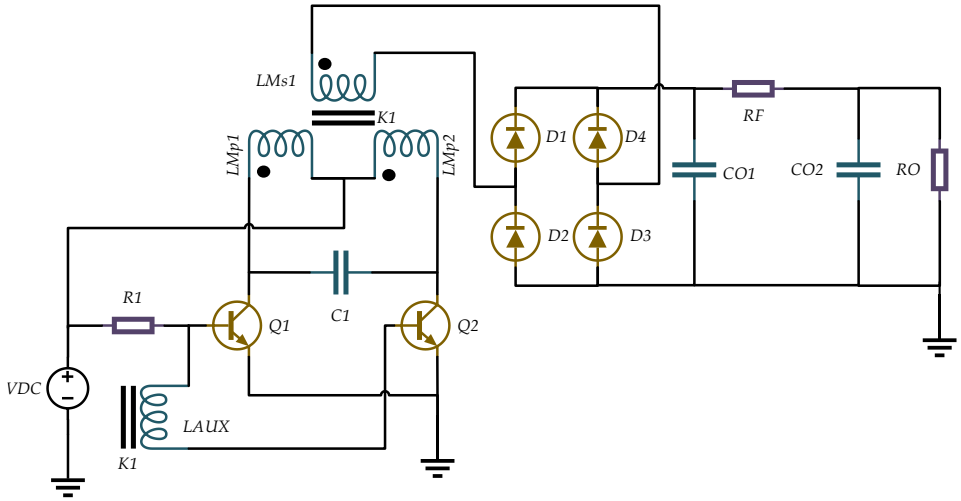

Fig.4: Self-Driven Resonant Oscillator for Ultra-Low Noise, High Voltage Outputs.

2.1.2 *Secondary-Side Regulation*

Linear and shunt regulation techniques are often implemented in very low-power supplies where the differential voltage between the input and output is relatively small to minimize power dissipation. However, they find limited application within high-voltage circuits since they are typically inefficient and do not provide galvanic isolation. Despite this, their impressive ripple, noise, and EMI performance means they have been used extensively alongside switching regulators to form hybrid solutions to allow precise regulation of the cathode electrode of a TWT. An early version of linear regulation for TWTs that enables improvements in achievable amplification output bandwidth can be seen in [37]. Through utilizing both linear and shunt regulating methods, the voltage imposed upon the helix was varied in synchronicity with changes in the anode delay line voltage. This allowed modulation of the beam current to vary the velocity of the electron beam and thus enable tuning over a wider band of frequencies without producing excessive power dissipation than would be achievable with a substantially fixed beam current.

The voltage potential of depressed collectors need only be approximately 50% that of the cathode voltage with respect to the slow wave structure to enable an approximate halving in the overall tube power dissipation without adversely affecting the tube gain or power output characteristic. In early power supplies, the collector voltage potential was typically generated by tapping power from the power supply of the slow wave structure [38, 39], with utilization of linear pass regulators allowing for compensation of changes that exist between the cathode and slow wave voltages [40]. The supply for the filament electrode in high frequency MPMs is typically supplied by a separate, higher current capability SMPS such as a fly-back converter sharing the common DC voltage 270VDC bus in parallel [41].

Secondary-side regulation is particularly useful in charge regulating supplies where dynamically pulsed load currents exist. Implicit detection of the pulse-to-pulse high voltage allows implementation of regulation methods that notably improve phase-noise performance of the amplification process. Techniques to achieve this include the utilization of an additional charge regulation capacitor placed in series with the grounded end of the main output storage capacitor [42]. A current transformer in series with the output capacitor provides bidirectional current sensing, the output of which is time-integrated resulting in precise representations of the high voltage. A similar technique is used in [43], whereby the utilization of a low-voltage, ground referenced sensor allows detection of the desired level of main capacitor charge and controls a low-voltage, solid-state element such as a bipolar junction transistor (BJT) into current cut-off through the injection of voltage step, preventing further charging of the output capacitors. This technique, shown powering a TWT load, is illustrated in Fig.5:

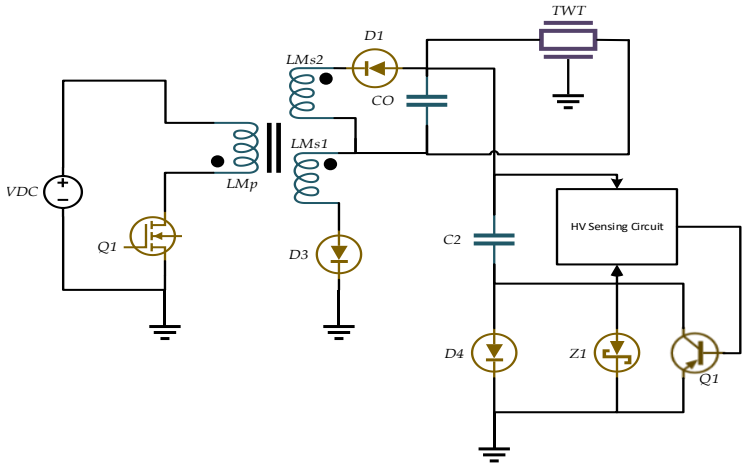

Fig.5: Secondary-Side Precision Linear BJT Regulator for Ultra Low-Noise TWT.

Switched mode regulation of a resonant inverter followed by a voltage stabilization switch driven by a solid-state current mirror was used for the cathode of a TWT operating as high as -60,000V [44, 45]. Operating at 10kHz, resonant energy is shunted into a separate capacitive stage when the load is pulsed off to avoid further charging of the load capacitors. Although these techniques appreciably improve the phase-noise performance of the transmission process, they require additional control electronics which may require full isolation from the high voltage output.

Implementation of these techniques, particularly in older TWT power supplies, allowed compensation for the level of voltage droop that would occur during RF transmission events or substantial voltage excursions across loading conditions due to the implementation of low inverter switching frequencies and thus lower controller bandwidths. MPMs typically operate at lower power levels, with cathode currents being in the range of tens of milliamps, and thus detection of the output filter capacitor current may be difficult to track precisely. Provisions must be made to ensure the signal is amplified and substantially noise free to allow accurate actuations with the developed control signals.

2.1.3 Resonant Power Conversion

The most basic isolated SMPS topology is the fly-back converter, used extensively for generation of high voltage DC potentials [46, 47]. When combined with single-ended diode-capacitor multiplier circuits, they can generate significant voltage potentials but are often limited in the amount of power they can deliver to a load due to their single switch structure. Fly-back converters in their basic form are further limited to low frequency operation due to natural resonances within any circuit, which often cause substantial high-frequency oscillations in drain-source voltages experienced by Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs). If not

controlled adequately, this phenomenon often causes significant device over-voltage conditions, which may be destructive to the switching device [48]. The fly-back converter also exhibits a Right-Half Plane Zero (RHPZ) in the controller feedback response, which is difficult to compensate for and severely restricts the achievable controller bandwidth. Both the single-switch and two-switch variations operate under hard-switching conditions, resulting in significant switching loss and imposing strict limitations on the maximum allowable switching frequency.

The rate at which the output capacitor can be charged is a strong determinant of the power supply accuracy, with elevated switching frequencies allowing a higher number of charging cycles to be performed between pulse-to-pulse transient events. Alternatively, an adaptation of the fly-back converter that recycles transformer magnetizing current back to the input source has been used to form the EPC for the cathode voltage while allowing improvements in the phase stability of the RF transmission process despite low switching frequencies through utilization of information regarding the PRF [49], which enabled replenishment of the capacitor charge within a single switching event and removes step-size dependency. The modified fly-back control circuit implements comparator based hysteretic control to resume switching and recharge the output capacitor once the voltage across it drops by a pre-determined amount, with resultant modulation of the transistors being considerably variable frequency and a function of many variables, making it difficult to optimize the components within the converter.

A key enabler for operation at elevated switching frequencies is the implementation of soft-switching techniques, which utilize inherent and intrinsic resonances between components. Mechanisms that cause switching loss include diode reverse recovery effects, semiconductor output capacitances, and particularly in high voltage transformers, the lumped parasitic capacitance and leakage inductance due to winding turns, technique, and geometry. Through utilization of at least one of these mechanisms, the high level of power dissipation that would occur is instead transferred to the converter source or load [50, 51, 52]. High voltage EPC designs for MPMs have used soft-switching techniques multifariously to combat switching frequency limitations present within previous design iterations [53, 54].

The highest frequency power supply for microwave amplifiers is shown in [55] and consists of a full-bridge series-resonant converter (SRC) employing multiple series connected transformer-rectifier modules. Switching at such elevated frequencies allowed toroidal transformer ferromagnetic cores to be implemented, each having only a single-turn primary and low magnetizing inductance which ensured the transformers did not saturate. Due to the minimal integral number of turns and series connection of the modules, the transformer parasitic capacitance was kept to suitably low values that permitted high frequency operation.

Regulation of the output was performed with a hybrid mode controller, modulating both the inverter frequency and duty cycle to accommodate the relatively high leakage inductance of the toroidal transformers and the strong dependence of the output voltage on the load current level and transients. The method of connecting a plurality of modules is more typically used to generate very high powers and voltages, such as the energization of X-ray tubes [56]. Mixed-mode regulation has been shown to minimize the level of frequency variation required to provide output voltage control with highly dynamic loading conditions, allowing optimization of converter efficiency across a reduced frequency bandwidth [57].

Small-signal modelling has demonstrated that the increased complexity of multi-element resonant converters such as the "LCC" and "LLC" regulators present significant problems when attempting to achieve fast and robust transient responses [58]. Particularly for significant dynamic changes in output load, the large-signal transient behaviour limits the achievable controller bandwidth and results in slow transient response even at elevated switching frequencies. The selection of which resonant structure to use is determined by the input voltage range, required voltage conversion ratio, and required loading levels. The SRC is virtually uncontrollable due to poor frequency selectivity as the converter is unloaded. The use of phase-shifted auxiliary circuits within an SRC can be implemented in high voltage circuits to provide additional reactive energy at no load conditions to allow voltage regulation while maintaining soft switching [59]. The general arrangement of such a circuit utilized within a standard full bridge is illustrated in Fig.6:

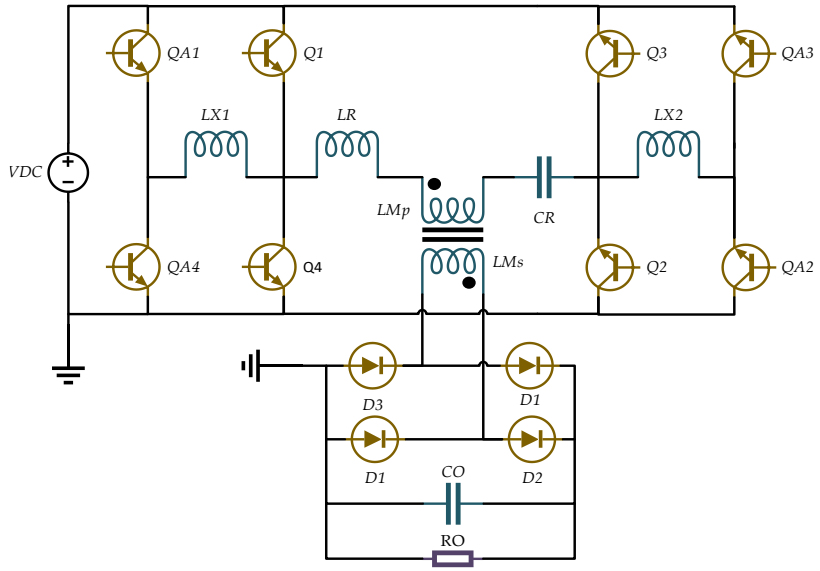

Fig.6: Full Bridge SRC with Phased-Shifted Auxiliary Circuits for No-Load Regulation.

One drawback with utilizing full-bridge converters in applications which require less than 1kW of output power is the additional transistors, control circuitry, and thus complexity.

Half-bridge converters may be employed up to this power level however require large electrolytic or film input capacitors to guarantee low input voltage ripple and stability. Split-capacitor half-bridge converters instead utilize the input capacitors as part of the resonant circuit, allowing notable power density improvements [60]. An adaptation of a series-parallel multi-resonant half-bridge converter operating at fixed-frequency is proposed in [61]. Operating from an input DC voltage of 400VDC, a 1.5kW EPC for a TWT was produced with 97.12% efficiency at 50kHz switching frequency. The inclusion of a bi-directional switch in series with the transformer and the half-bridge input capacitors provides a symmetrical voltage across the transformer winding regardless of implemented duty cycle.

The T-type converter shown in Fig.7 does not implement split-capacitor resonance and instead requires a stable DC voltage to provide transformer clamping. The bi-directional switching mechanism requires two additional switches and corresponding floating gate drivers, as neither are ground-referenced. This substantially increases the controller complexity and is furthermore detrimental to power density. The use of asymmetrical duty cycle operation within fixed-frequency resonant converters has been shown within research to allow minimization of switching losses while also maintaining the lower conduction loss features present within standard Pulse Width Modulation (PWM) regulated converters [62].

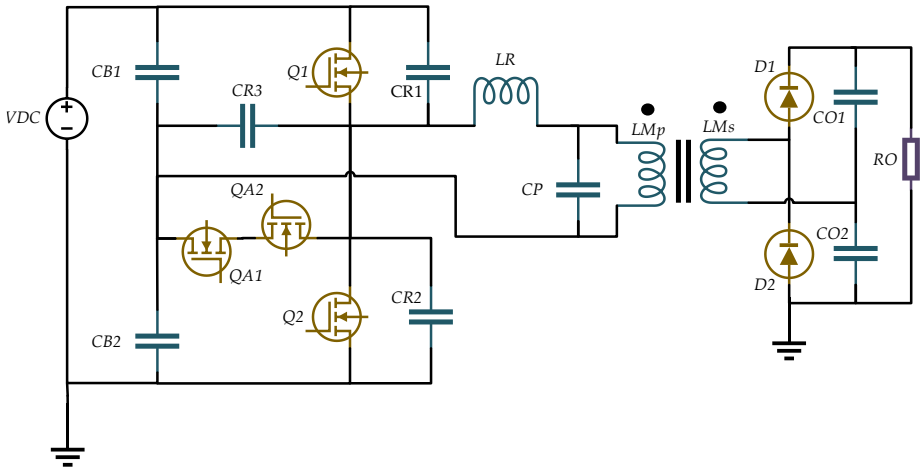

Fig.7: T-Type Converter with Bi-Directional Switching Cell for Asymmetrical Duty Control.

Other techniques of operating resonant converters at fixed frequencies include the manipulation the effective tank resonant frequency through modifying the impedance of the tank components. Methods such as switched capacitors [63, 64] and variable or saturable inductors [65] have been used to some effect but again increase the component count and control complexity. Provisions must be made to ensure the impedance never becomes capacitive to ensure safe operation of the high frequency switches. This requires multiple design choices such as clamping the frequency

range, using precise components, and calculating worst-case impedance variations across all line and load conditions. The method in Fig.8 below utilizes a standard half-bridge resonant converter with an additional switched capacitor cell to achieve modification of the resonant tank impedance:

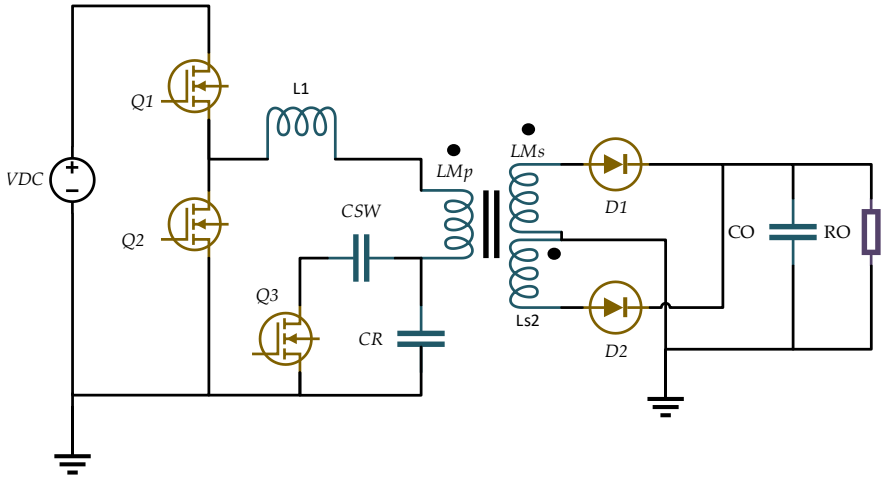

Fig.8: Fixed-Frequency Switched Capacitor Multi-Resonant SRC Converter.

Fixed-frequency modulation of resonant converters can be achieved with phase-shift controllers. The Phase-Shifted Full-Bridge (PSFB) can utilize high levels of transformer leakage to discharge MOSFET output capacitance before a switching instant to significantly reduce switching loss. In [66], a series-resonant tank was combined with a phase-shifted controller to produce a -9,000V cathode voltage for a TWT at switching frequencies of 100kHz. A current-fed, PSFB converter proposed in [67] improves on this by allowing incorporation of the transformer parasitic capacitance while maintaining regulation across the wide load-ranges present within a grid-modulated amplifier. Through the inclusion of an input inductor, shoot-through and half-cycle symmetry cannot cause device failure or transformer core saturation and may also contribute to reductions in EMI.

Phase-shifting parallel connected resonant converter modules has been shown to significantly increase the achievable output power and decrease output ripple in long-pulse applications. Modular, interleaved constructions of N number of identical resonant stages with a fixed phase relation of 360/N between modules was shown to provide significant suppression of AC voltage variations, notable reduction in rise time, stored energy, and total output capacitance in a 50kHz capacitor charger [68]. Each phase-shifted module contained an inverter consisting of diode-clamped energy dosage quasi-resonant capacitors, shown below in Fig.9:

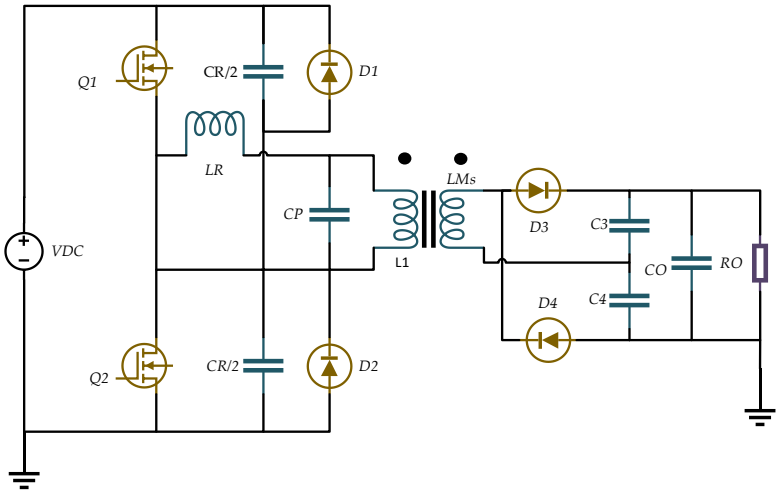

Fig.9: Diode-Clamped Split-Capacitor Resonant Converter for Long-Pulse Applications.

The addition of clamping diodes across the resonant capacitors allows limitation of output current during overloading conditions, which may exist during short-circuit events, or if the frequency of operation is decreased to a point where the circuit becomes net capacitive. This feature is gained at the expense of a substantially reduced voltage gain, due to diode clamping of the resonant capacitors to the maximum input voltage.

2.1.4 *Pre-Regulation of DC Link*

By far the most common method of voltage regulation for TWTs is pre-regulation of the input power source. Typically coupled with high-frequency resonant converters, they enable a multitude of features that are beneficial to the generation of substantially low-noise outputs while allowing simplified control of one or multiple amplifier tubes within a system. For TWTs utilized within space and satellite applications operating from a low-voltage 28VDC bus, the current-fed push-pull converter often forms a part of the EPC due to the low-noise symmetric transformer drive and volt-second regulation through the implementation of current-mode control. An 80kHz active-clamped version of the current-fed push-pull converter was implemented to provide a -3.2kV output voltage for a TWT operating at efficiencies of 93.4% from a 26-44VDC bus [69].

To increase the achievable switching frequency and provide clamping of drain-source voltage and oscillations, buck output current-fed converters may incorporate additional clamping switches. Although clamping of the drain-source voltage is performed, the maximum switch voltage stress remains significantly higher than the prime power voltage, limiting use if operating from a 270VDC source. The issues of converter start-up and TWT arcing have been known to cause appreciable current surges through the EPC switching circuitry, causing device failure and the requirement to

over-rate components for the fault current level. A buck converter pre-regulator utilized alongside a push-pull inverter stage is proposed in [70]. In this arrangement, illustrated in Fig.10, the output inductor of a buck converter acts to regulate and limit current through duty-cycle variations. The push-pull switches, therefore, can operate with both fixed frequency and fixed duty cycle. This has the benefit of significantly reducing the possibility of flux imbalance and potential saturation of the isolating transformer. In the event saturation does begin to occur, the controller can either reduce the input current or force an over-current event, protecting the switching devices. Compared to a typical voltage-fed push-pull converter, the output stage inductor has been eliminated, creating much more favourable conditions for the rectifying diodes.

Depending on the application, the buck converter diode can be replaced with a synchronous MOSFET to enhance efficiency and reduce heat-sinking requirements. In low-voltage, high current outputs the output rectifier may also be replaced with active synchronous rectifying devices to remove the inherent high forward voltage drops of non-synchronous, diode-based rectifiers.

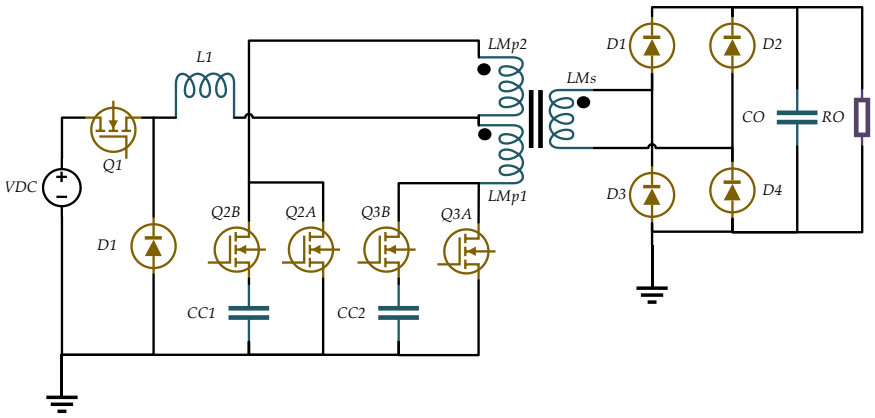

Fig.10: Buck Regulator Current-Fed Active-Clamped Push-Pull Converter.

It is often considered essential for optimum performance that switching regulators within a system be either frequency-synchronised or be substantially frequency separated to avoid generation of frequency harmonics that are not easily filtered. Alternatively, constant variation of the switching frequency of a push-pull stage at an appropriate rate and deviation allows a select band of frequencies to replace the single fundamental frequency and associated harmonics that are present in a fixed-frequency solution [71]. This diffuses the noise created by the switching transistors and that within the RF modulation signal over a wider band of frequencies, decreasing spurious signals for an enhanced phase-noise performance even at sufficiently low transistor switching frequencies. This is only enabled by the inclusion of an additional buck pre-regulator stage. Further examples of non-synchronous buck current and voltage-fed pre-regulators feeding push-pull inverters can be found in [72, 73, 74].

Pre-regulators can also be used to improve voltage regulation through processing only the input voltage variations that are present within the source [75]. Through the inclusion of additional switches and isolating transformers, the voltage across the push-pull output capacitor can be extremely well-regulated. By appropriately proportioning the transformer turns ratios, the buck pre-regulator can process as little as 10% of the total input power flowing from the source to the output load, enhancing processing efficiency. The radar transmitter operating mode is often selected in pseudo-random fashion, such that variations in PRF and pulse-width are predictable. Since the radar processor is knowledgeable of the next transmission pattern in advance, pre-adjustments to the controller loop error voltage may be implemented. Voltage Injection Control (VIC) was first proposed in [76], whereby the radar PRF directly acts upon the PWM generator to change the duty cycle. This reduces settling time following dynamic load changes and thus eliminates false-target identification. The pre-regulator provides peak-current mode control of the inverter input current according to precise samples retrieved from the cathode to compensate for line and loading variations.

One may replace the buck pre-regulator with a boost converter to step-up to a higher intermediate DC-link voltage [77], alleviating the voltage gain contribution required by the isolating transformer or resonant tank. A 300kHz boost-regulator providing a well-regulated 320VDC intermediate voltage from an unregulated 270VDC source has been proposed [78, 79], and is illustrated in its basic form in Fig.11. Losses were minimized by operating a half-bridge resonant inverter from the intermediate regulated source and synchronising the switching frequencies of the two regulators. Precise cathode electrode voltages within +/-0.5% were achieved, exhibiting efficiencies of 90% throughout multiple RF operating mode including CW operation, 200kHz switching, and 5MHz burst operation. The pre-regulator can be adapted for higher switching frequencies by forcing resonant transitions of their switches or by utilizing clamping techniques [80].

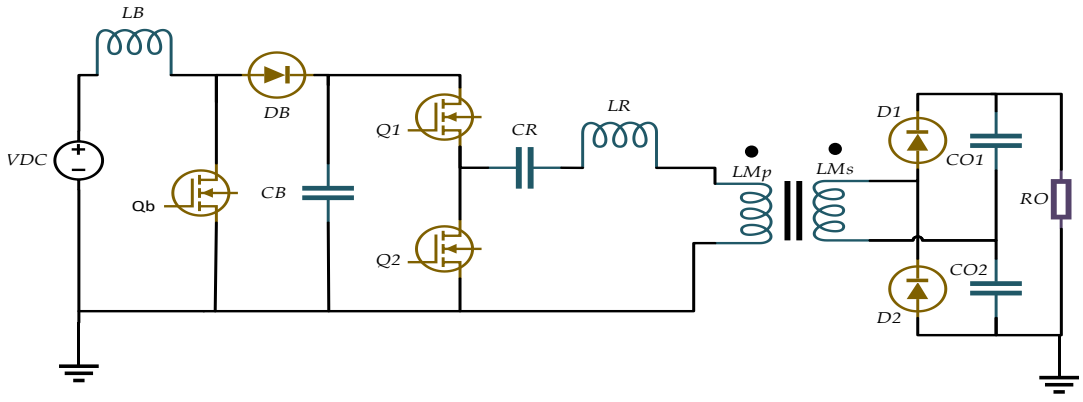

Fig.11: 300kHz Boost Pre-Regulator Stage with SRC Resonant Main Inverter.

Soft-switching, high-gain boost converters may offer substantially more voltage step-up than a standard boost converter [81] but are only particularly interesting for low-voltage bus applications where that would be beneficial. Class E resonant converter topologies in double conversion systems have been used for 28VDC prime power applications to generate intermediate voltages of several hundred volts [82]. In Fig.12 below, an interesting topology is shown which may prove useful for the generation of high-voltage outputs from a low-voltage bus, through the provision of a medium-voltage intermediate bus. It should be noted that, although a simple fly-back is used to illustrate the point, other inverters may prove more beneficial for the main inverter stage for generation of a substantially low-noise high-voltage potential for a TWTA cathode.

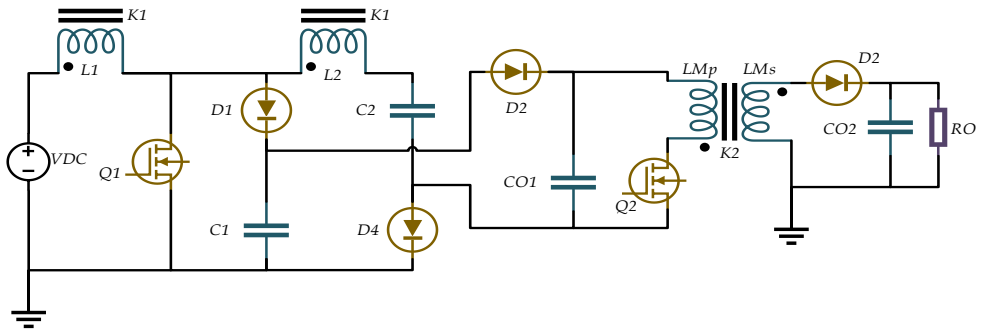

Fig.12: High-Gain Boost Pre-Regulator with a Single-Switch Fly-back Inverter Load.

Such solutions find very limited suitability for higher voltage input buses, and increasing the voltage magnitudes imposed on high frequency transformers can be severely detrimental. Alongside substantially increased transformer volt-seconds requiring a larger core to avoid saturation, the finite rise and fall times of transformer parasitic capacitance may cause output voltage attenuation. A final useful area for the application of pre-regulator stages is for the regulation of multiple TWT cathode and depressed collector electrodes from a single prime power source, which is often seen in spacecraft telecommunications systems [83]. In a similar document, multiple pre-regulators drive push-pull transformers connected in parallel to provide variable, independent control of multiple cathode voltages from a single common bias prime power source, resulting in significant reductions in size, weight, and cost savings in space applications [84].

2.1.5 Transformer Design and Parasitic Reduction

The isolation transformer self-capacitances are pivotal to understanding high-frequency limitations of EPCs. High common-mode noise emissions are dominated by converter displacement currents that result due to high voltage rates of change, with research showing the two critical factors for the generation of significant high frequency noise levels are the distribution of transformer inter-

winding capacitance and the voltage within them [85]. The placement of single, or multiple electrostatic Faraday shields between the primary and secondary windings allows decoupling of high-frequency EMI to the earthed chassis and diversion away from the low-noise outputs to notably reduce capacitive effects [86].

Structural winding techniques have been shown to enable "capacitance cancellation", with the concept of diode-split high voltage transformers mitigating the effects of switching transients by dividing high voltage windings into sections and electrically isolating them [87]. Winding segmentation allows significant reductions in the voltage gradient amplitudes across stray capacitances within the transformer and reduces dissipation caused by current reflection during switching transients while attenuating associated interference. A custom chambered bobbin with symmetrical arrangement of the high voltage windings resulted in identical winding capacitances which induced currents in a conductive coating screen that were the same amplitude but anti-phase, leading to direct cancellation of the induced interference [88].

The SRF of a transformer is typically designed to be an order of magnitude higher than the transistor operating frequency to minimize generation of power oscillations that may cause unacceptable dissipation, temperature rise, and EMI. A full model of the parasitics within a transformer, including more complex common-mode effects, is shown below in Fig.13:

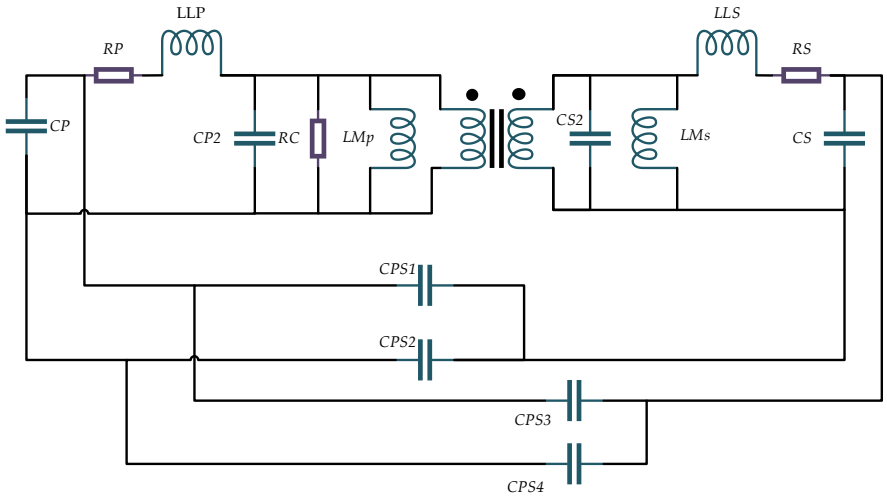

Fig.13: Transformer Model Including Common-Mode Capacitive Effects.

A 4-kV pulse transformer for a TWT was proposed in [89], alongside investigations of winding arrangements and how they affect the achievable transformer SRF. Implementing a segmented winding technique, coupled with "sandwiching" the primary winding between multiple secondary windings within the core window, led to an SRF of 1.4MHz. Due to this topological implementation, the maximum transformer frequency was limited to just 80kHz.

Utilization of resonant switching techniques, however, will often allow the designer to operate closer to the resonant peaks without issue. A further study on winding geometry and techniques for high voltage converters is provided in [90], which further investigated the AC resistance for different geometries and how the mean length of a turn, effective distance between secondary layers, and effective permittivity of insulating dielectric material influence the measured capacitance value.

Common-mode chokes have shown some promise for attenuation of EMI frequencies that far exceed the switching frequency. Additional EMI planes and capacitors, placed very close to the power converter inputs and outputs, may provide low-impedance paths for common-mode return currents [91]. However, this is not suitable for high voltage applications it generates additional capacitance between transformer input and output which will reduce high frequency isolation impedance. The topology illustrated in Fig.14 utilizes an additional transformer coupled through an EMI filter to provide substantial filtering effects. By further winding the secondary of the first transformer and the primary of the second transformer with a single turn, the capacitive coupling between all windings is minimized without affecting the transformer isolation [92].

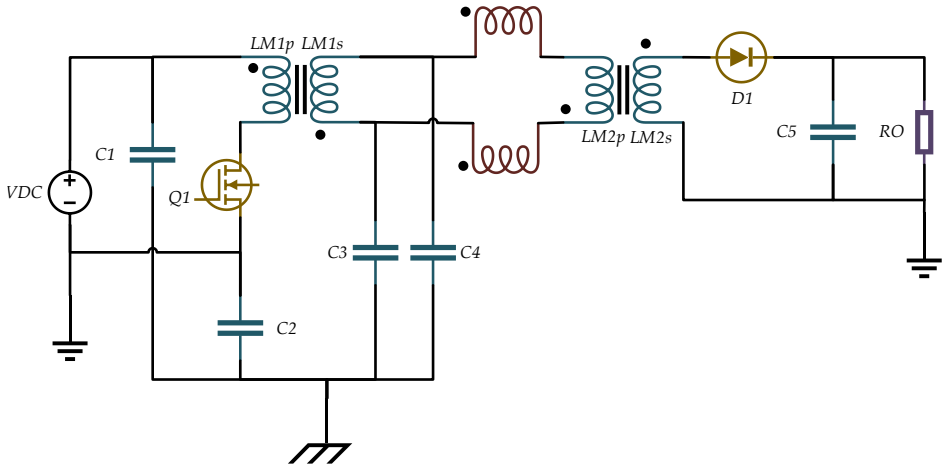

Fig. 14: Additional Isolation Transformer and Common-Mode Choke for Mitigation of Switched-Mode EMI Generation.

Planar transformers consisting of stacked Printed Circuit Board (PCB) arrangements around a ferrite core have been attempted for high power density, high voltage applications [93, 94]. Unfortunately, miniaturization is incredibly difficult in practice, as planar transformers have very close coupling with wide, broadside facing traces which are not optimal for high voltage generation. Such high levels of coupling, and therefore low leakage inductances, will naturally result in higher transformer effective capacitance which will further restrict operation at higher frequencies. As the power density of the solution increases, the transformer core size will ideally reduce, requiring an

increase in the number of turns to prevent core saturation unless a superior ferrite material becomes available. It is particularly difficult in the secondary windings to achieve the required creepage and clearance distances between the individual traces to ensure safe operation. This issue is only exacerbated by the increased likelihood for arcing events as frequency increases.

It has been suggested in literature to remove the isolation transformer from the EPC entirely through capacitive coupling techniques which may be particularly suitable for lower voltage EPCs due to reduced reinforced insulation requirements [95, 96]. Drawbacks of this method include the requirement for multiple series-parallel combinations of isolating capacitors to achieve the necessary isolation voltage. If the isolation capacitors form part of a resonant circuit, to ensure product-to-product consistency, the total overall capacitance must be formed by high-class C0G type ceramic capacitors. Such capacitors, although stable and high performance, prove notoriously difficult to find at higher voltage ratings with sufficient capacity. One such example of capacitive isolation is shown in Fig.15, below:

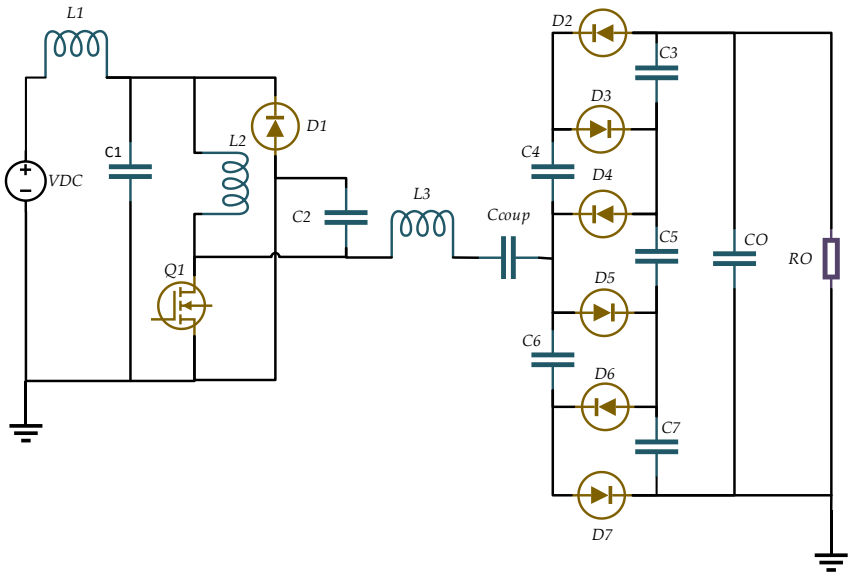

Fig.15: Capacitive Coupled EPC with Diode-Capacitor Chain Multiplier Circuit.

The maximum achievable switching frequency should be viewed as a multi-faceted problem, with the transformer parasitic capacity being the main bottleneck. The maximum power dissipation within the active and passive devices, the transformer windings and core, and any associated temperature rise within the individual components, further dictates maximum switching frequency.

2.1.6 *Control Techniques and Wide Band Gap Devices*

A voltage biasing system for a multi-stage depressed collector proposed that their operating voltages be dynamically adjusted based on the amplifier operating conditions [97]. This is useful since, if the depression voltage is allowed to deviate too far and approaches that of the cathode voltage, a significant increase in the number of electrons that return to the body of the tube occurs, causing both thermal overload and generation of spurious signals. A significant reduction in power consumption of an amplifier operating in saturation could be achieved by manipulating the depressed collector voltages, allowing near-optimal efficiency across multiple different TWT operating conditions regardless of saturation level [98]. The collector electrode, as mentioned previously, is significantly less important for phase-noise performance of the tube, and voltage variations within it need only be considered regarding reductions in amplification efficiency and thus heating created by low collector potentials which hinder the ability to recover the totality of the beam kinetic energy. Loosely regulated or unregulated collector supplies have been proposed to remove the requirement for very high-quality power supplies for both electrodes and allowing precise control and low-noise generation of the phase-noise critical cathode electrode alone at a substantially lower power level [99].

Very little research has been done regarding the utilization of WBG devices in high-voltage EPCs. One study, which operated the inverter at a switching frequency of 830kHz, achieved significant size and weight reductions while maintaining overall efficiencies of 98.25% [100]. The topology is a current-fed, four-element resonant converter and is illustrated in Fig.16 below:

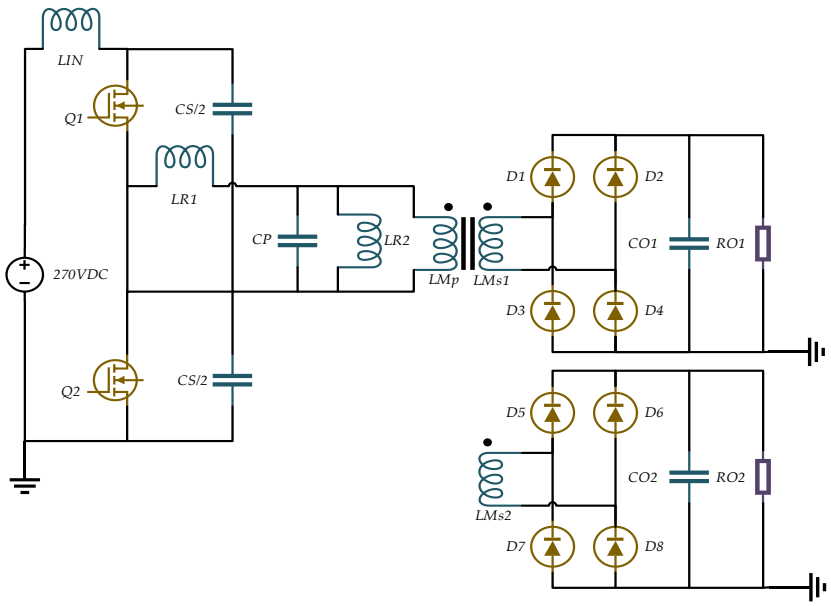

Fig.16: Current-Fed Four-Element Resonant Converter for Generation of a 500V Cathode Voltage with Wide Band-Gap Devices.

Although impressive results, this research has significant limitations that were not addressed:

1. The research concedes that commercial WBG devices did not have blocking voltages beyond 250VDC at the time of writing. This limits the research to satellite-based TWT systems with low-line DC voltage inputs. Commercial Gallium Nitride (GaN) transistors are now becoming more mature with offerings of cascaded devices with voltage ratings of up to 1200VDC. The utilized low voltage GaN devices have substantially less on-state resistance than is achievable in modern day, higher voltage transistors. The device utilized in the above research had $R_{DS_{On}}$ values of $7m\Omega$, whereas current state-of-the-art 650V transistors offer $R_{DS_{On}}$ values between $25m\Omega$ and $450m\Omega$ depending on the device current rating. Utilizing a device with very low on-state drain-source resistance has the potential to minimize conduction losses but tends to increase switching loss due to higher levels of gate charge. The choice of device is therefore entirely application specific, and the device utilized in this research would be wholly unsuitable for use within an MPM transmitter.

2. Generates a maximum cathode voltage of 500VDC. This is substantially lower than the requirements for TWT electrodes. This limits reflected transformer capacitance due to the implementation of a lower transformer turns ratio. The research therefore does not consider additional, substantial bottlenecks that exist within a high voltage generation and typically constrain the switching frequency to levels that are considerably lower than would theoretically be enabled by WBG devices and their superior switching characteristics.

3. Considers two outputs that do not share a common output terminal. It is therefore not truly reflective a TWT load and the interactions that occur between the electrodes.

2.2 SUMMARY

This review has outlined multiple topologies which have been utilized for high voltage generation of the necessary potentials required within a TWT. The achievable switching frequency is clearly limited by several issues which have been shown to limit transistor frequency to around 100kHz or below in most examples despite the use of resonant conversion techniques. The limitations this places on controller bandwidth are often mitigated with complex control techniques to compensate for voltage excursions during load dynamic behaviour. The highest frequency supply that was able to generate appropriate voltages for both the collector and cathode electrodes operated at frequencies of more than 500kHz, but required multiple series-connected toroidal transformers and generated the collector voltages from tapping from the higher voltage cathode supply.

Topological modifications such as splitting the cathode and collector into two separate EPCs may significantly reduce both peak and Root Mean Squared (RMS) currents within the low power cathode supply, theoretically enabling substantially higher frequencies within its regulator. Due to the relationship between controller bandwidth and output current load transient magnitude, this may also enable substantially reduced voltage deviations for a given output load capacitance compared to a single converter solution. Since the cathode and collector can be controlled independently through separate feedback paths, any voltage deviations within the collector are isolated from the cathode. One may additionally utilize simplistic control techniques within the collector electrode such as utilization of the PRF control signal information to optimize the efficiency of the TWT depressed collector without affecting the phase-noise performance of the transmission process since the cathode can remain substantially fixed to the nameplate voltage with minimal AC voltage variation.

The practical work proposed within this thesis aims to provide a novel discussion of how additional bottlenecks within high voltage power supplies restrict the attainable frequency that is currently being enabled with current commercialised WBG devices. The work also provides the first set of results and discussions currently available within research regarding the utilization of WBG semiconductors operating from a 270VDC line voltage. A novel power topology will be proposed that addresses the individual power requirements of the cathode and collector within an MPM which are substantially disparate in a multitude of ways.

3 PROPOSED ELECTRONIC POWER CONDITIONER TOPOLOGY AND DESIGN PROCEDURES

3.1 SPECIFICATION OF SWITCHED MODE POWER SUPPLY

The prime power source is typically a 270VDC+/-10% bus, rectified and smoothed from a 400-Hz, three-phase source. This voltage source is typically unregulated but may be followed by a boost converter to create a regulated intermediate bus of anywhere from 300-400VDC. Another option is the use of a power-factor correction circuit, which has the added benefit of allowing operation close to unity power factor. Coupled with a three-phase input EMI filter, very stringent military standards can be met. However, such devices are often physically large, heavy, and may increase the required heat-sinking capabilities of the system.

The specifications for both the cathode and collector electrodes of the TWT and all other main design considerations are summarised in brief below for clarity:

- Cathode: Output voltage of -6,000VDC with respect to the TWT body, which is held at ground potential. The current magnitude is 10mA +/-5mA and flows wholly from the cathode electrode to an earth chassis to represent pure energy loss to the electron beam transmission process, flowing through the tube body. Variation in this body current is largely determined due to the frequency dependence of the RF input drive of the TWT which causes slight electron beam defocussing.

- Collector: A single depressed collector output voltage of -3,000VDC. The current supplied to this converter flows from the cathode to the collector and is representative of energy recovered from the amplification process. The magnitude is approximately 200mA +/-5mA. The EPC should be adaptable to an amplification tube with up to 4 depressed collectors at different depression ratios to improve tube efficiency.

- Isolation transformer: The design of the transformer is critical to both the size and weight of the power converter and should be minimized. To ensure safe operation at high voltage, the transformer should meet reinforced isolation levels. Therefore,

extremely small leakage current should exist across the isolation when 12kV is applied between the primary windings and all secondary windings together.

- Frequency: To maximize the converter power density, minimize AC voltage variations within the cathode, and ensure exceptional transient response to differing loading conditions present in multi-mode radars, it will be necessary to operate the converter at a substantially high frequency and consider the use of wide bandgap semiconductor devices where appropriate.

- Steady-State Characteristics and Transient Response: To minimize phase variance in the RF signal, the steady-state AC voltage variation on the cathode electrode DC voltage should not exceed 100mV with respect to the tube body. The pulsing regime applied to the cathode can vary anywhere from 100Hz-100kHz depending on the desired operating mode of the transmitter. Under all possible PRF and duty cycle combinations, the maximum variation of the cathode and collector electrodes must be limited to 10V and 200V peak-to-peak, respectively.

- Thermal System: The power density of an MPM solution is typically severely constrained by the need to dissipate significant amounts of heat from the active devices and the transformer. The chosen converter design should optimize the efficiency of power transmission to minimize the impact of the heat removal system.

3.2 HYBRID PARALLEL CONVERTER STRUCTURE

A novel hybrid converter topology consisting of a novel multi-resonant active-clamped resonant flyback and a series-parallel loaded resonant half-bridge converter is proposed, shown below:

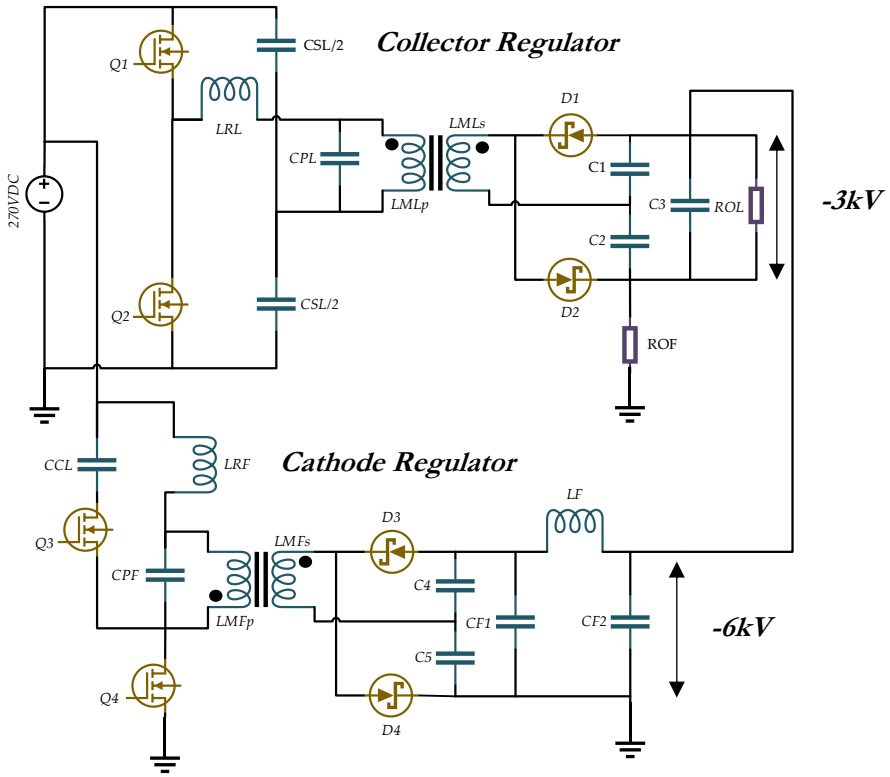

Fig.17: Proposed Novel Hybrid Fully Controllable EPC Topology for an MPM.

The main motivations for such a topology are briefly summarized below:

1. Allows the effective, individual provision of power to the cathode and collector electrodes respectively. Since the two main electrodes are significantly disparate in a multitude of ways, each converter can be individually optimized to efficiently meet their individual requirements.

2. Dedicated control loops can be employed to allow further optimization according to the required steady-state and dynamic characteristics. Resonant converters, particularly close to their high-power peaks, can often display highly non-linear behaviour that is difficult to compensate for and adequately stabilise. Generating the cathode voltage with a low-power resonant converter can enable the use of simple compensation techniques to achieve a

linear response to changes in either frequency or duty cycle across all line and load conditions. This will be discussed in more detail in the following chapter.

3. Different switching frequencies can be used in each converter. By operating the cathode regulator at very high switching frequencies, the peak-to-peak voltage ripple, essential for improved input-to-output phase-noise performance of the RF amplification process, can be achieved. The collector regulator, which processes most of the total load power, can be operated at a lower frequency to enhance overall power conversion efficiency. This minimizes power dissipation, thus alleviating the heat-sinking burden of the system.

4. Enhanced bandwidth is easily implemented at higher switching frequencies, allowing much more accurate control of the cathode voltage during dynamic events. This is particularly important in MPMs with multi-mode TWTs, as both the duty cycle and frequency of load transients can change drastically when in operation. Operating the less critical collector electrode at a lower bandwidth and allowing larger voltage fluctuations during dynamic events is not critical to phase-noise performance, and only decreases TWT efficiency through a reduction in the number of electrons recycled from the transmission process.

5. High-powered load transients in the collector regulator have less influence on the peak dynamic voltage changes in the cathode. In typical systems where the collector and cathode voltage are generated from a single transformer and rectifier network, the full load current transients cause a larger deviation in output voltage. In a hybrid arrangement, only the current flowing through the tube body is processed by the cathode regulator rectifier. This makes meeting the dynamic requirements of the specification easier to achieve, enhancing performance of the RF transmitter.

6. Minimize cathode output capacitance. Spark-over events, common in high-voltage power supplies, can often cause significant damage and even destruction of the TWT device. By processing only the tube body current in the cathode regulator, a minimal level of capacitance can be implemented to achieve an equivalent level of voltage ripple and voltage deviation during transient events. This can reduce the level of charge dissipated in the tube during fault events, making protection easier.

To model the TWT collector electrode, a simple purely resistive, high-power load R_{O_L} is placed in parallel with the collector regulator output capacitance, C_3. This load current circulates within the collector and represents the percentage of electrons that are effectively recovered from the electron

acceleration process. The remaining current is processed by the cathode regulator and flows through load resistance R_{O_F} and into the tube body at earth potential where it is dissipated as heat.

3.3 LCC SERIES-PARALLEL RESONANT COLLECTOR REGULATOR

The most significant portion of the total load power is supplied to single-stage collector via a series-parallel multi-resonant "LCC" converter with split-resonant capacitors. A half-bridge is utilized to reduce the number of switches and corresponding gate drivers. This section will provide insight regarding modelling of the complex three-element resonant circuit, which has been performed in the time-domain [101, 102], and later in the frequency-domain [103, 104]. The LCC resonant converter was also shown to have numerous benefits when compared to both the standalone SRC and Parallel Resonant Converter (PRC) topologies, particularly in high voltage output applications [105].

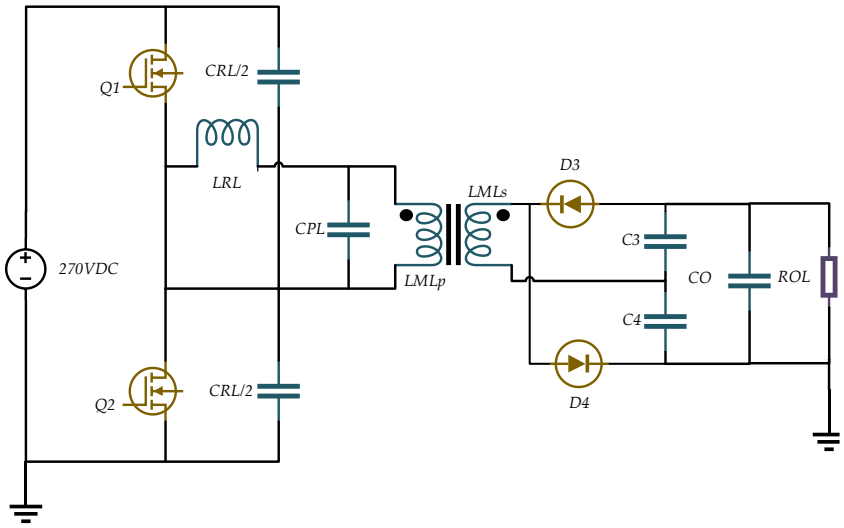

Fig.18: Series-Parallel Resonant LCC Regulator Topology.

3.3.1 *Fundamental Harmonic Approximation with High Voltage Outputs*

Due to their complex behaviour, analysis of resonant converters involves the use of multiple simplifications and approximations to allow the use of classical AC circuit analysis. The input voltage to the resonant tank is a square wave, with a fundamental component which causes a sinusoidal current waveform to flow due to filtering of the higher frequency harmonics. The non-

linear rectifier and filtering network act together to transform the output load resistance into an equivalent impedance as seen by the resonant circuit, dependent on whether the output is a current or voltage source. To optimize the converter for high efficiency, it is preferred to have the transformer perform some level of step-up to minimize the peak and RMS circulating currents present when implementing high gain within the resonant tank components.

The output is split into 4 equivalent series-connected full-wave voltage doubler rectifiers. Standard Fundamental Harmonic Approximation (FHA) techniques, however, cannot predict the highly dynamic load behaviour of an MPM during transient events due to the non-sinusoidal currents that occur as frequency increases to reduce the tank gain and allow effective regulation of the output voltage. Even at full load, there exists significant issues with standard FHA techniques when utilizing capacitive output filters, which requires an entirely different analysis. This issue is particularly exacerbated when considering high voltage and high frequency power conversion where the slew rate of the capacitance may be significantly slowed. The first effect of capacitive output filters is an attenuation in the output voltage for any given input to output resonant converter transfer function due to output diode conduction which clamps the transformer to the output voltage, causing substantial nonlinearities within the converter. R. L. Steigerwald provided additional research regarding the effects of capacitively filtered outputs on the converter transfer function in [106].

3.3.2 *Extended Fundamental Harmonic Approximation*

A simple way to include nonlinearities that reduce the accuracy of the FHA model is to instead calculate the voltage conversion ratio according to the "diode non-conduction angle", which determines the period in which the diodes are conducting current during output clamping. Equations will be taken from [107] and included here to illustrate calculation of the resonant components for the given circuit. Even in the improved FHA methodology, the input current (i_{in_L}) waveform must be assumed sinusoidal:

$$i_{in_L} = \widetilde{I_{in_L}} \sin(\omega_{s_L} t) \qquad (3.01)$$

Where $\widetilde{I_{in_L}}$ is the desired peak resonant tank current. The angular switching frequency, ω_{s_L}, determines the frequency of the sinusoidal current at full load. To allow optimization for high efficiency as the collector processed the most substantial portion of the overall MPM power, and since phase-stability of the RF amplification process is not notably degraded by higher AC voltage ripple of the collector, it may be operated at a frequency much less than that of the cathode.

The equivalent circuit below replaces the parallel resonant capacitance with a combined equivalent series circuit, consisting of a resistance and capacitance:

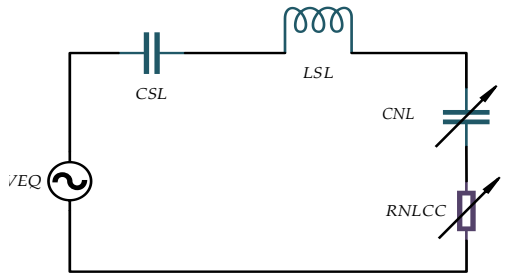

Fig.19: Capacitive Output Series-Parallel Model considering Transformer Non-Linearity.

The series quality factor Q_{S_L} is slightly modified by the new equivalent load capacitance C_{N_L} and an equivalent circuit resistance $R_{n_{LCC}}$ acting in series:

$$Q_{S_L} = \frac{1}{\omega_{o_L} C_{T_L} R_{n_{LCC}}} = \frac{\omega_{o_L} L_{S_L}}{R_{n_{LCC}}} \qquad (3.02)$$

Where ω_{o_L} is the full-load angular frequency of the series-parallel converter, L_{S_L} is the series resonant inductance of the tank, and C_{T_L} is the total equivalent circuit capacitance including the effects of both C_{N_L} and C_{S_L}. The resonant and switching angular frequencies can be normalised to allow analysis of the resonant tank gain with frequency:

$$\omega_{o_L} = \frac{1}{\sqrt{L_{S_L} C_{T_L}}} \qquad (3.03) \qquad\qquad \omega_{n_L} = \frac{\omega_{S_L}}{\omega_{o_L}} \qquad (3.04)$$

The total circuit impedance of the model, Z_{T_L}, can be utilized to calculate the peak resonant tank current $\widetilde{I_{in_L}}$ for a given equivalent source voltage V_{eq_L}:

$$Z_{T_L} = R_{n_{LCC}} + j\left(\omega_{S_L} L_{S_L} - \frac{1}{\omega_{S_L} C_{T_L}}\right) \qquad (3.05) \qquad \therefore \widetilde{I_{in_L}} = \frac{V_{eq_L}}{|Z_{T_L}|} \qquad (3.06)$$

Utilizing the above relations, the input current can be found by calculating the absolute magnitude of the complex tank impedance:

$$\widetilde{I_{in_L}} = \frac{2V_{DC}}{\pi \sqrt{\left\{R_{n_{LCC}}^2 + \left(\omega_{S_L} L_{S_L} - \frac{1}{\omega_{S_L} C_{T_L}}\right)^2\right\}}} \qquad (3.07)$$

Where V_{DC} is the line voltage available to the EPC. The input-to-output current (M_{i_C}) and the input-to-output voltage (M_{v_C}) transfer functions for the converter are related to the collector output rectifier nonconduction angles θ_C, collector transformer turns ratio N_C, the selected passive component values and the AC-related quantities that they create, as follows:

$$M_{i_C} = \frac{\widetilde{I_{in}}_{rms_L}}{I_{O_C}} = \frac{\pi}{\sqrt{2}N_C\{1+\cos(\theta_C)\}} \qquad (3.08)$$

$$M_{v_C} = \frac{N_C V_{O_C}}{V_{DC}} = \frac{1}{\{1+\cos(\theta_C)\}} \frac{1}{\sqrt{\left\{1+Q_{S_L}^2\left(\omega_{n_L}-\frac{1}{\omega_{n_L}}\right)^2\right\}}} \qquad (3.09)$$

Where $\widetilde{I_{in}}_{rms_L}$ is the RMS value of the peak series-parallel tank input current, and V_{O_C} and I_{O_C} are the collector output voltage and current generated, respectively.

3.3.3 *No-Load Regulation*

The voltage imposed upon the parallel resonant capacitor V_{Cp_L} is related to the initial voltage $\overline{V_{C_{P_L}}}$, the parallel capacitance C_{P_L}, the peak tank current, diode conduction time δ_C, and the available angular frequency in which it is allowed to conduct:

$$V_{C_{P_L}} = \overline{V_{C_{P_L}}} + \frac{1}{C_{P_L}}\int_0^{\delta_C} \widetilde{I_{in_L}} \sin(\omega_{s_L} t)\, dt \qquad (3.10)$$

The available time in which the parallel capacitor is allowed to accrue charge is:

$$\delta_C = \frac{1}{\omega_{s_L}} \cos^{-1}\left(1 - \frac{2N_C\omega_{s_L}V_{O_C}C_{P_L}}{\widetilde{I_{in_L}}}\right) = \frac{\theta_C}{\omega_{s_L}} \qquad (3.11)$$

To allow effective regulation during zero-loading conditions, the following output current relation must be equal to zero during the periods in which no RF amplification is to take place:

$$I_{O_C} = \frac{N_C}{2\pi}\left[\int_{\theta_C}^{\pi} \widetilde{I_{in_L}} \sin(\theta_C)\, d\theta_C + \int_{\theta_C+\pi}^{2\pi} -\widetilde{I_{in_L}} \sin(\theta_C)\, d\theta_C\right] \qquad (3.12)$$

Which is made possible through reduction of the diode nonconduction angle to zero degrees. In variable frequency supplies, this is achieved through increases in the switching frequency until the finite charge and discharge times of the parallel capacitance are reduced to a point where the output

diodes no longer conduct current toward the output. The converter frequency bandwidth is the difference between the minimum switching frequency at full load and the maximum frequency required to achieve voltage regulation at zero load. In TWT power supplies that utilize variable frequency control, it is prudent to minimize the bandwidth to reduce the number of operating frequencies that the converter must be guaranteed to be stable across.

The ratio between the parallel and series capacitances has direct influence on the regulation bandwidth and is expressed as $A_C = \frac{C_{P_L}}{C_{S_L}}$. As the load current becomes zero during periods of no RF amplification, the resonant peak shifts to a higher frequency (ω_{P_L}) as the entirety of the input current flows through the parallel resonant capacitor during zero-load:

$$\omega_{P_L} = \frac{1}{\sqrt{\frac{L_{S_L} C_{P_L} C_{S_L}}{C_{P_L} + C_{S_L}}}} \qquad (3.13)$$

High values of both series resonant quality factor (~3-5) and series-to-parallel capacitor ratios (~0.5-1.0) offer improved frequency selectivity and bandwidth, allowing improved control of the tank gain over a given span of switching frequencies. This suggests the use of larger series resonant inductances, and it is quintessential to ensure that the inductive impedance exceeds that of the series-resonant capacitor at all loading levels to enable soft-switching of the MOSFETs. This can be guaranteed by ensuring the load is net inductive at the lowest intended switching frequency, $X_{L_L} > X_{C_L}$. A sub-resonance protection must be incorporated to ensure the controller does not output a lower value to avoid transitioning to capacitive operating mode.

3.3.4 Resonant Converter Control Issues

The output voltage of resonant converters is typically controlled with a single external voltage control loop. An error signal drives a Voltage Controlled Oscillator (VCO) to proportionally change the transistor driving frequency. The amount of power delivery for a given change in control voltage is ideally linear, however significant variations in the open loop steady state gain with output power causes the transfer function to display substantially non-linear characteristics that are difficult to compensate for. This issue is of particularly concern if operating close to the resonant peaks of the transfer characteristic. Efforts to close the feedback loop around the power stage and linearise the response result in either sluggish response or self-oscillation at low and high power, respectively.

Close to the high-power resonant peak of the voltage transfer function, Voltage Mode Control (VMC) will exhibit a second order response to changes in control voltage, such that step changes in control signals require a notable number of cycles to produce resultant changes in the output capacitor average current. This severely limits the achievable converter control bandwidth. Verifying performance of the converter across a wide range of PRFs and duty cycles will be extremely difficult given the level of gain variation and chaotically moving poles and zeroes within the dynamic power transfer function, which change during real-time as the radar operating mode is modified.

An extension of Current Mode Control (CMC), called Charge Mode Control (CHMC), was proposed to tackle this drawback in [108] and was shown to linearize the control-to-output response and produce first-order responses to control signal changes. Other solutions have been proposed to enhance the bandwidth of resonant converters, such as Hybrid Hysteretic Control (HHC) which directly samples the resonant capacitor voltage through a capacitive divider. This sampled resonant capacitor voltage is then connected to two current sources controlled by the gate driver signals, which adds a triangular compensation signal through either sourcing or sinking current at the resonant capacitor node [109]. The use of hybrid duty cycle/frequency control techniques and window comparator based hysteretic control has already been discussed.

3.4 COLLECTOR RESONANT COMPONENTS DESIGN PROCEDURE

Since the collector processes over 90% of the total output power and is not essential to phase-noise performance of the amplification process, it will operate at a moderate, variable frequency and be optimized to achieve high efficiency to minimize heat sinking requirements. A suitable transformer turns ratio must first be calculated to alleviate the level of gain required from the resonant tank. Diode nonconduction values above 90 degrees have been shown to lead to appreciable increases in required input current, which is detrimental to conduction losses and transformer AC winding losses at the desired switching frequencies. A larger turns ratio reduces the peak level of flux excursion within the transformer core as the primary volt-seconds can be kept to a reasonable value, such that core size can be reduced. The larger integral number of turns required is not a notable issue, since the resultant increase in transformer capacitance can be readily included into the series-parallel resonant tank considering a moderate switching frequency and thus longer switching period for parallel capacitor charge and discharge. This should still ideally be minimized to mitigate high frequency AC winding losses and temperature rise. A turns ratio of $N_C = 0.05$ is seen as a reasonable trade-off for efficiency optimization. The required normalised voltage gain from the resonant tank is therefore:

$$M_{v_C} = \frac{N_C V_{O_C}}{V_{DC}} = 0.6173$$

Calculated at low-line DC voltage, at which point requires the largest resonant tank gain, which occurs at the minimum transistor angular switching frequency. A slightly different design methodology is used to optimize the component selection, minimize component current and voltage stresses, prioritize frequency selectivity, bandwidth, and finally to reduce the issues associated with high power control of resonant converters. To decide a suitable nonconduction angle, consider the rearranged version of the input-to-output current equation below:

$$\theta_C = \cos^{-1}\left(\frac{\pi I_{O_C}}{\widetilde{I_{in}}_{rms_L}\sqrt{2}N_C} - 1\right) \qquad (3.14)$$

To optimize efficiency, the maximum diode nonconduction angle is chosen to limit the RMS and peak currents flowing within the converter. Limiting the maximum current to $6.5A_{RMS}$ results in a θ_C of approximately 69°. To ensure inductive switching across the entire load range and controller stability, the normalised switching frequency should be suitably above the resonant frequency. This minimizes issues associated with output voltage control close to the nonlinear resonant peaks during full-loading conditions. An initial estimate of $\omega_{n_{L_{est}}}$ = 1.1 is made. At this stage, an approximate minimum switching frequency should be decided: $\omega_{s_{L_{est}}} = 2\pi\,(180kHz)$. Thus, $\omega_{o_{L_{est}}} = 2\pi(163kHz)$. We may calculate the parallel resonant capacitor C_{P_L} that achieves the required output voltage with this nonconduction angle within the specified current limits and chosen transformer turns ratio at the minimum switching frequency:

$$C_{P_L} = \frac{\widetilde{I_{in_L}}\left(1 - cos(\theta_C)\right)}{2N_C\omega_{s_L}V_{O_C}} \cong 18nF \qquad (3.15)$$

The impedances within the resonant tank that the converter must present to the equivalent complex voltage source can now readily be calculated. Start by defining a dimensionless parameter γ which is a function of the load rectifier characteristics:

$$\gamma = \pi + 2\omega_{s_L}C_{P_L}N_C^2R_{O_C} = 4.67 \qquad (3.16)$$

The series equivalent resistance and capacitance for the extended FHA model may now be calculated:

$$R_{N_{L_{CC}}} = \frac{8N_C^2R_{O_C}}{\gamma^2} = 13.77\Omega \qquad (3.17)$$

$$C_{N_L} = \frac{\pi\gamma^2 C_{P_L}}{2N_C\sqrt{2\pi\omega_{s_L}C_{P_L}R_{O_C}}(\gamma - 2\pi) + \gamma^2\left(\pi - \cos^{-1}\left(\frac{\gamma - 2\pi}{\gamma}\right)\right)} = 63.43nF \qquad (3.18)$$

The total circuit capacitance C_{T_L}, which determines the series angular resonant frequency and quality factor, can be calculated:

$$C_{T_L} = \frac{\omega_{n_L}^2 - 1}{\omega_{s_L}\sqrt{\frac{4}{\pi^2}\left(\frac{V_{DC}}{\widetilde{I_{in}}_L}\right)^2 - R_{n_{LCC}}^2}} = 19.56nF \qquad (3.19)$$

The capacitance is a function of the input power, equivalent series resistance, and the switching/normalised frequencies. One can therefore see how the total effective circuit capacitance can be adjusted to achieve output voltage control. The required physical series capacitor C_{s_L} must now be calculated such that the series-parallel capacitor combination presents the correct impedance to the source:

$$C_{s_L} = \frac{C_{N_L}C_{T_L}}{C_{N_L} - C_{T_L}} \cong 28nF \qquad (3.20)$$

To preserve the resonant frequency used in the above calculations, the series resonant inductance must satisfy the following relation:

$$L_{S_L} = \frac{1}{\omega_{o_L}^2 C_{T_L}} = \cong 49\mu H \qquad (3.21)$$

The following AC quantities result from the chosen passive component quantities:

$$\omega_{o_L} = \frac{1}{\sqrt{L_{S_L}C_{T_L}}} = 1.0215Mrad/s \qquad Q_{S_L} = \frac{\omega_{o_L}L_{S_L}}{R_{N_{L_{CC}}}} = 3.6345 \qquad \omega_{n_L} = \frac{\omega_{s_L}}{\omega_{o_L}} = 1.1043$$

With the above AC quantities and the calculated diode nonconduction angle, we arrive at the voltage conversion ratio for the collector regulator:

$$M_{v_C} = \frac{N_C V_{O_C}}{V_{DC}} = \frac{1}{\{1 + \cos(\theta_C)\}}\frac{1}{\sqrt{\left\{1 + Q_{S_L}^2\left(\omega_{n_L} - \frac{1}{\omega_{n_L}}\right)^2\right\}}} = 0.599 \qquad (3.22)$$

Which gives an output voltage of 2911.14V at low-line voltage and the minimum switching frequency.

The output voltage can be increased in various ways, but to avoid manipulating the calculated passive components, a novel representation of the required normalised frequency to achieve a given required voltage gain is given below:

$$\omega_{n_{req_L}} = \frac{\sqrt{\aleph^2 + 4} + \aleph}{2} \qquad (3.23) \qquad \therefore \aleph = \sqrt{\frac{\left[\left\{\frac{V_{DC}}{N_L V_{O_C}(1 + \cos(\theta_C))}\right\}^2 - 1\right]}{Q_{S_L}^2}} \qquad (3.24)$$

Where $\aleph$ is a normalised, angular frequency "adjustment factor" that assists with the selection of appropriate design parameters and further describes important AC quantities required within the resonant tank. Utilizing this equation, one arrives at a required normalised switching frequency of $\omega_{n_{req_L}}$ = 1.094. The switching frequency is decreased to approximately 176kHz to allow effective regulation at full-load and low-line conditions and to compensate for converter losses. An alternative design technique would be to calculate the required nonconduction angle for a chosen quality factor and desired normalised frequency if desiring to work further away from the nonlinear resonant peaks to ensure stability. However, this typically results in higher rectifier nonconduction angles and thus higher peak and RMS currents within the converter.

3.5 FREQUENCY LIMITATIONS OF HIGH VOLTAGE POWER SUPPLIES

It is likely that the parasitic transformer capacitance will limit the maximum switching frequency that is obtainable for acceptable performance due to finite allowable time for charge and discharge of the parallel capacitance. This increases the duration in which the output load is effectively disconnected during periods of nonconduction, causing attenuation of the output voltage. To compensate, one must operate closer to the nonlinear resonant peaks of the voltage transfer function through either passive component redesign or reductions in switching frequency to enable higher peak discharge currents.

The concept of load coefficient (R_{Coeff}) was first proposed in [110] and is calculated in equation (3.25). Although the paper uses a slightly different model for the converter than was utilized in the previous chapter, the effect of the rectifier conduction angle is still considered for converters with capacitively filtered outputs and finds application to both PRC and series-parallel converters in equal measure, such that this analysis remains consistent.

$$R_{Coeff} = \omega_s C_p R_O N_T^2 \qquad (3.25)$$

The conduction angle of the rectifier θ_{CA} instead describes the angle in which the output rectifier is conducting current, and is calculated through:

$$\theta_{CA}(°) = 2\tan^{-1}\sqrt{\frac{\pi}{2\omega_{s_L}C_{P_L}R_O N_L^2}} = 2\tan^{-1}\sqrt{\frac{\pi}{2R_{Coeff}}} \quad (3.26)$$

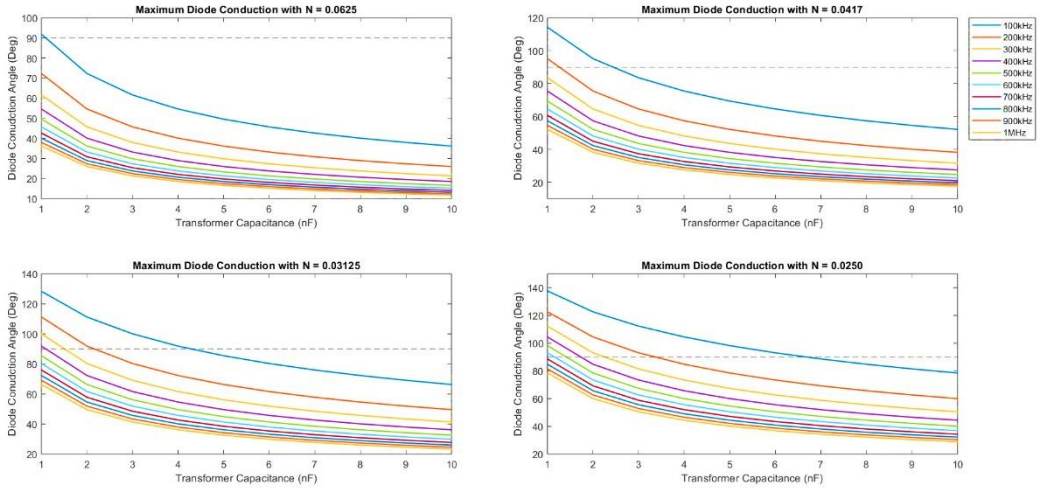

Fig.20: Required Diode Conduction Angles with Different Transformer Turns Ratios and Switching Frequencies for Differing Transformer Parasitic Capacitances with Load Resistance of 600KΩ.

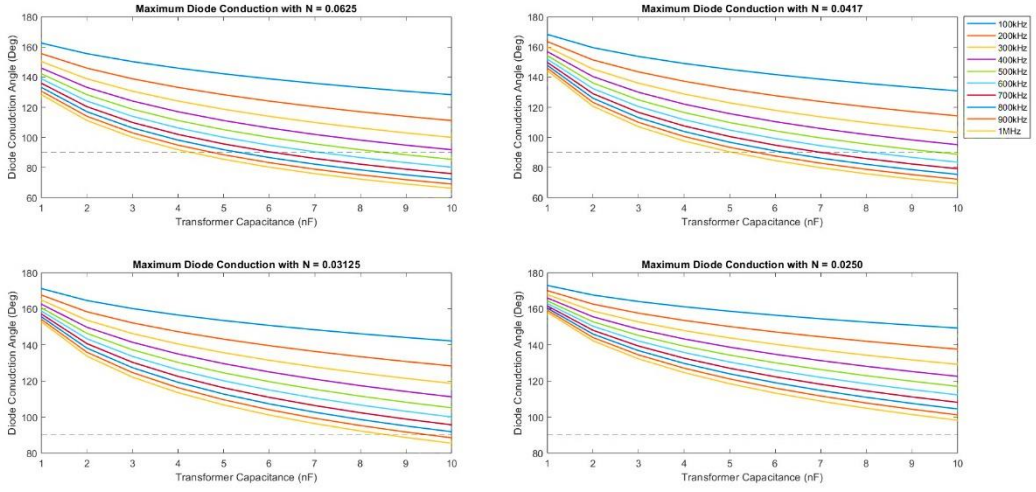

Fig.21: Required Diode Conduction Angles with Different Transformer Turns Ratios and Switching Frequencies for Differing Transformer Parasitic Capacitances with Load Resistance of 15KΩ.

This has multiple implications regarding implementation of high switching frequencies in both high and low power resonant converters. It should be noted that the output voltage can be increased for a constant output rectifier conduction angle through increases of the magnetizing current I_{L_M}:

$$I_{L_M} = \frac{2V_O\omega_s C_p N_T}{(1+cos\theta_{CA})} \quad (3.27) \qquad I_O = \frac{2N_T^2}{\pi} I_{L_M} \sin^2\left(\frac{\theta_{CA}}{2}\right) \quad (3.28) \qquad I_O = \frac{2N_T^2}{\pi} V_O\omega_s C_p \tan^2\left(\frac{\theta_{CA}}{2}\right) \quad (3.29)$$

The figures above demonstrate the maximum switching frequency that is achievable before the output voltage is no longer sufficient without significant increase in tank gain and thus circulating current to assist in charge and discharge of the capacitance. At lower transformer turns ratios, the ability to generate the full cathode output voltage is degraded due to the requirement for charge and discharge to larger voltage magnitudes before output diode clamping occurs. The opposite is true for high transformer turns ratios, which enable significantly higher switching frequencies for a given transformer capacitance. This may, however, lead to a higher level of parasitic capacitance which may negate some of the effects. For the high-power resonant converter, high transformer turns ratios are not conducive to high frequency operation and may cause significant issues. To better understand why this is the case, the figures above indicate a boundary between buck and boost operation modes of resonant converters, which occurs at conduction angles of approximately 90°. Conduction angles below this have been shown to generate significant additional input and peak tank currents, which are detrimental to efforts to optimize efficiency within the high-power converter, but this may be possible in low-power supplies due to the low output current mitigating the maximum circulating currents.

Through observing equation (3.27), one can understand the importance of the $\omega_{s_F} C_{p_F} N_F$ product, referred to now as the frequency limit coefficient ϖ_c, on the achievable output voltage that can be generated without substantial increases in the required magnetizing current. Any corresponding increases in frequency must be met with corresponding decreases in angular switching frequencies, lower transformer parasitic capacitances, or higher transformer turn ratios to minimize slew rate magnitude of the parallel capacitance and the period in which charge and for discharge is allowed without substantially increasing the current stresses within the converter. A novel representation for rapid design of high voltage, high frequency resonant converters is given below to express this dependency:

$$\frac{I_{L_M}(1+cos\theta_{CA})}{2V_O} = \varpi_c \quad (3.27a)$$

The transformer turns ratio is typically decided at an early stage to allow transformer core optimization. For the purposes of this analysis, a moderate turns ratio of 0.0417 is chosen such that the primary voltage in the configuration is limited to approximately 125V, slightly less than was required in the previous collector regulator design. It is also assumed that the transformer magnetizing inductance is sufficiently large, so that it does not contribute to the resonant behaviour of the transformer. The following is produced:

$$\omega_s C_p = \frac{I_{L_M}(1 + cos\theta_{CA})}{2V_O N_T} = 0.02334 \qquad (3.27b)$$

For a switching frequency of 1MHz and a peak current of 9.1A, the transformer must not have a capacitance that exceeds 3.7nF without substantially increasing the magnetizing current within the transformer or increasing the turns ratio. A transformer capacitance of 10nF would limit switching frequency to no more than approximately 372.4kHz without corresponding increases in magnetizing current through operation close to the resonant peaks of the voltage transfer function. The frequency limitation coefficient also substantially limits optimization of passive components. Assuming an appropriate capacitance is achieved, selecting the normalised frequency as $\omega_n = 1.1$ results in a required series resonant frequency point of 909kHz. For the converter characteristics thus far, the equivalent series load is calculated using equations (3.16) and (3.17):

$$\gamma = 4.354 \qquad\qquad R_{N_{LCC}} = 11.01\Omega$$

For the calculated load rectifier value and the intended switching and normalized frequencies, the total circuit capacitance is calculated through equation (3.19):

$$C_{T_L} = 2.58nF$$

For the given resonant frequency, we use equation (3.20) to arrive at a required series capacitance:

$$C_{S_L} = 3.07nF$$

The resonant inductance required and the quality factor this creates, are finally shown below from equations (3.21) and (3.02):

$$L_{S_L} = 11.88uH \qquad Q_{S_L} = 6.163$$

Which results in a net inductive tank impedance and a series-to-parallel capacitor ratio that exceeds 1. There is little work on the steady-state and dynamic performance of series-parallel regulators under such conditions. The above issues place a very strict requirement on the maximum

transformer capacitance and demonstrates the importance the significant bottleneck it imposes upon the converter design if the resonant components are to be optimized.

Importantly, despite the above being a workable solution, these issues become much more severe if a single converter solution is used to generate both electrode voltages. The dependence of ϖ_c is more severe when considering low power resonant converters, such as that utilized within this research. In such cases, however, substantially lower conduction angles required to generate the full output voltage can be accommodated due to the lower output current. Trigonometric power reduction identities applied to equation (3.27) above allow a new expression for the required diode conduction angle:

$$\theta_{CA} = \cos^{-1}\left(\frac{-\Pi + 1}{1 + \Pi}\right) \qquad (3.30)$$

Where Π is an alternative load coefficient, which is a product of the chosen rectifier characteristics, calculated as follows:

$$\Pi = \frac{\pi I_O}{2N_T V_O \varpi_c} \qquad (3.31)$$

To generate -6,000V with a turn ratio of 0.0417 at the same switching frequency and transformer capacitance as in the previous example, would require a diode conduction angle of:

$$\theta_{CA} = 28.55°$$

The peak magnetizing current required to generate this voltage is calculated below with equation (3.28):

$$I_{L_M} = 4.13A$$

The purpose of the hybrid converter solution is to minimize the transformer size and reduce winding loss through processing a minimum amount of required load power. Larger products disallow such benefits through the substantial increase within the magnetizing inductance that is required to generate an equivalent cathode output voltage, which both increases core size if saturation is to be avoided and leads to substantially more winding loss – particularly those attributed to high frequency, AC varying signals. In this case, the dimensionless coefficient is substantially increased, in turn reducing the equivalent series load:

$$\gamma = 51.652 \qquad R_{N_L} = 3.13\Omega$$

The calculated resonant components within the series-parallel converter extended FHA:

$$C_{N_L} = 3.8nF \qquad C_{T_L} = \ 1.328nF \qquad L_{S_L} = 23.08uH$$

The required physical series capacitance to present the correct impedance to the source is calculated as approximately 2nF, which poses similar issues to the high-power converter case. Due to both increased resonant inductance and substantially reduced series equivalent load resistance in the FHA model, the tank quality factor is significantly higher and causes issues regarding controllability. To maintain optimal series-to-parallel capacitor values would require a maximum referred transformer capacitance of just 2nF. It is concluded, therefore, that operation of both low and high-power resonant converters is substantially constrained by the ϖ_c product of the rectifier load network, which should be kept to appropriate levels for an intended switching frequency by carefully selecting an optimal transformer capacitance.

An alternate approach is to increase the transformer turns ratio to minimize the required magnitude of voltage deviation that the parallel capacitor must charge and discharge from. Specifically in low-power converters, a substantially reduced output diode conduction time exists, which means much higher peak magnetizing currents are required to generate the same cathode voltage magnitude. A significant drawback for obtaining elevated switching frequencies within low-power resonant converters is the optimization of the resonant components, which becomes difficult as frequency increases due to restrictions placed upon the circuit quality factor and thus frequency selectivity during unloading. A solution to the problem may lie within the use of advanced voltage multiplier circuits which further alleviate the gain requirement from the resonant tank without substantially increasing the transformer turns ratio. This reduces the required magnitude of the reflected transformer capacitance, such that the time in which diode conduction occurs can be increased. Such solutions have been shown to have higher output impedance, possibly being detrimental to the converters ability to effectively regulate the cathode output voltage during unloading. Additional secondary windings offer similar benefits but reduce power density through mechanisms such as additional winding loss and PCB real estate for corresponding additional rectifier circuits.

This section provided a novel discussion of the frequency limitations of resonant converters depending on the load rectifier network, providing new expressions that allow optimization for high switching frequencies depending on a given load. It will now be shown that the low-quality factor characteristics of the series-parallel converter can be utilized to exceptional effect to allow fixed-frequency, duty cycle control of resonant converters. Through combination with a second resonant network, a multi-resonant converter can be formed that switches between circuits with

substantially differing quality factors to modulate the effective energy stored and energy dissipated within a load, enabling high frequency operation with extremely fast transient response.

3.6 ACTIVE-CLAMP FLY-BACK CONVERTER

An Active Clamp Fly-back (ACF) converter, observed in Fig.22, is commonly used in high frequency, high power density applications for the provision of low-noise outputs through utilization of the transformer leakage and magnetizing inductances to recycle energy that would otherwise be dissipated in passive clamp circuits. The additional circulating resonant energy, if sufficient, causes substantial discharge of switch output capacitances and enables reductions in switching loss to elevate converter efficiency. In literature, this technique has consistently been utilized to obtain switching frequencies in the region of 1MHz in relatively low power designs [111, 112, 113].

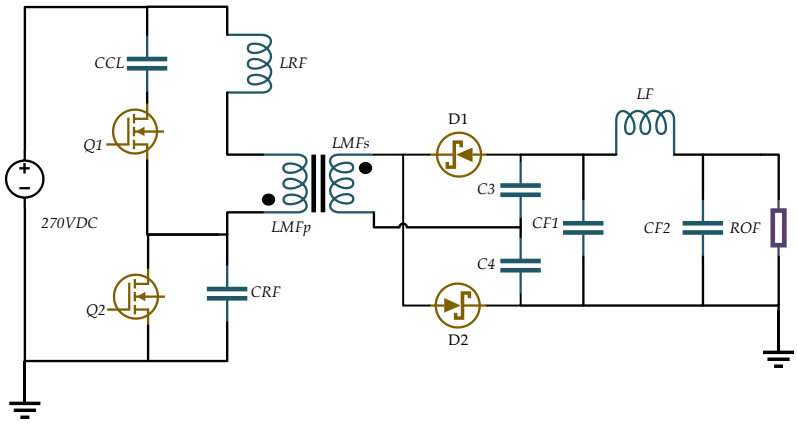

Fig.22: Active Clamp Fly-back Converter with Lumped Resonant Capacitance.

In the most prominent literature, the presence of transformer capacitance is either not considered at all or is modelled as a capacitance that appears effectively in parallel with the MOSFET output capacitance. This would suggest substantial limitations within high voltage applications, where switched node capacitance could be excessive and must be substantially or wholly discharged to enable soft switching of the MOSFETs. Equations will be now taken from [114] to demonstrate strict passive component limitations that are placed on high voltage ACF converters.

3.6.1 Passive Component Limitations

To achieve soft-switching transitions and minimize switching losses, the energy stored within the resonant inductor must exceed or be equivalent to that stored within the equivalent switched node capacitance when the clamp switch turns off: $E_{LR_F} \geq E_{C_{R_F}}$. The above energy balance expression typically enables a calculation of the required resonant inductance to be made, assuming that the resonant inductor voltage is relatively small compared to the input voltage and reflected output voltage:

$$L_{R_F} \geq \frac{C_{R_F}\left(V_{DC} + N_F V_{O_F}\right)^2}{I^2_{S_{1F(pk)}}} \qquad (3.32)$$

Where N_F is the fly-back transformer turns ratio, V_{O_F} is the cathode output voltage, C_{R_F} is the switched-node capacitance, $I_{S_{1F}(pk)}$ is the peak fly-back switch current, and L_{R_F} is the required fly-back resonant inductance. Alternatively, if insufficient energy is stored in the series inductance, the implementation of longer dead times allows additional time for discharge. The "optimum" delay time, T_{Dop} between switch transitions to achieve critical zero-voltage switching is equal to one-quarter of the resonant period formed by the series resonant components:

$$T_{Dop} = \frac{\pi}{2}\sqrt{L_{R_F} C_{R_F}} \qquad (3.33)$$

The insertion of additional, external inductance can assist in full discharge of the switched node capacitance and further improves efficiency and generation of EMI through limiting turn-off di/dt of the output diodes but suggests corresponding increases in required dead time to levels that would cause significant duty cycle loss and limit achievable output voltage without a corresponding decrease in converter switching frequency to accommodate them. Since a voltage divider forms between the magnetizing $L_{M_{F_p}}$ inductance of the transformer and total external resonant inductance, any additional leakage can cause further attenuation of the transformer voltage:

$$V_{TXF} = -\frac{V_{CL} L_{M_{F_p}}}{L_{R_F} + L_{M_{F_p}}} \qquad (3.34)$$

To avoid high frequency oscillations at switch turn-off, it should be assured that one-half of the resonant period formed by L_{R_F} and C_{CL} is much longer than the maximum off-time of the fly-back switch, $T_{F_{off}}$:

$$\pi\sqrt{L_{R_F} C_{CL}} \gg T_{F_{off}} \qquad (3.35)$$

Increases in the clamp capacitor should be avoided, as this significantly affects the converter transient response through provision of transformer reset flux during unloading. The entirety of research on the ACF converter demands that leakage inductance does not exceed 5-10% of the magnetizing inductance before the achievable voltage gain is severely restricted and analysis invalidated.

To preserve this ratio, increases within the leakage inductance must be followed with respective increases in the magnetizing inductance, which is detrimental to the achievable controller bandwidth and may cause core saturation unless core size is increased to reduce peak flux. The achievable controller bandwidth is limited by the RHPZ position of the frequency response, F_{R_z}. To ensure this has minimum impact on the converter dynamics, it is appropriate to ensure that the cross-over frequency f_{c_F} is no higher than one-fifth of the RHPZ frequency:

$$f_{c_F} = \frac{F_{R_z}}{5} = N_F^2 \left(\frac{\frac{V_{O_F}^2}{P_{O_F}} D_F'^2}{10\pi L_{M_{F_p}}} \right) \qquad (3.36)$$

Where N_F is the fly-back transformer turns ratio, D_F' is the clamp switch duty ratio, and V_{O_F}, I_{O_F}, P_{O_F} are the fly-back output voltage, current, and power respectively. By solely processing the 60W required by the cathode in the proposed hybrid solution, one can achieve a substantially higher theoretical cross-over frequency through a more than 10-fold increase in the RHPZ frequency position for a constant transformer turns ratio, maximum duty cycle, and implemented magnetizing inductance. When either the parasitic capacitance or switching frequency are sufficiently low, the impact of the SRF does not interfere with converter performance. A general rule-of-thumb is to ensure the switching frequency does not exceed one-tenth of the transformer SRF $F_{S_{R_{TX}}}$:

$$F_{S_F} < 0.1 F_{S_{R_{TX}}} = \frac{0.1}{2\pi \sqrt{L_{M_{F_p}} C_{R_F}}} \qquad (3.37)$$

This can no longer be assumed in high frequency, high voltage converters which exhibit substantial transformer capacitance.

3.6.2 *Analysis of High Voltage Actively Clamped Fly-Back Converter*

A transformer was designed for the fly-back converter which, after testing with a frequency response analyser (FRA), exhibited a capacitance of 4nF. The transformer consists of 4 secondary windings each of turns ratio 0.2725 feeding voltage doubler rectifiers. Due to the lack of equipment to allow insulation testing for -12kV, the design of the cathode voltage is constrained to a maximum of -4kV. The significance of the lumped node capacitance on the required dead-time and the theoretically achievable switching frequency can be observed by assuming a maximum dead-time of 10% of a 500kHz switching period. The amount of current required to optimally discharge the capacitance can be calculated by combining equations (3.33) and (3.35) and inserting known quantities:

$$I_{S_{1F(pk)}} = 13.62A$$

However, it will be now shown that assumptions made in current literature are not valid when considerable parasitic capacitance exists within the converter. The steady-state and dynamic behaviour will be shown to change drastically as switching frequency approaches or even exceeds that of the SRF. This effect is modelled in Fig.23, and in such cases, additional parallel resonances occur between the components, and a considerable amount of current no longer flows through the transformer magnetizing inductance.

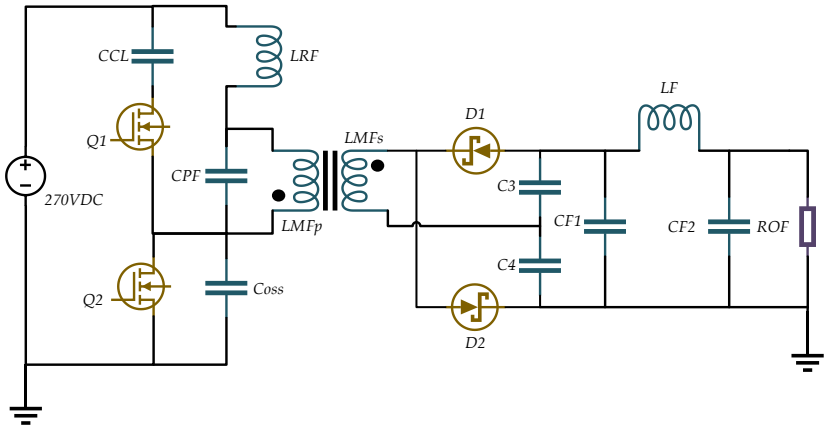

Fig.23: Active Clamp Fly-back Converter with Substantial Parasitic Transformer Capacitance.

In effect, the converter begins to take on characteristics of the parallel resonant and series-parallel resonant half-bridge converters with fixed-frequency asymmetrical duty cycle control, which has been demonstrated in literature [115, 116, 117]. When the fly-back switch is on, the circuit in Fig.24 is created:

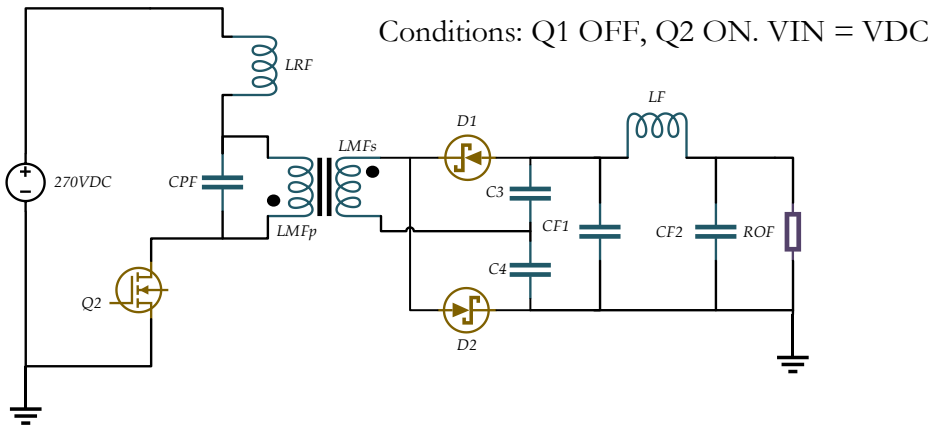

Fig.24: Parallel Resonance Stage of Multi-Resonant Fly-back Converter.

The resonant tank input voltage for this stage is equal to the input line voltage. When the fly-back switch turns off, after a small dead-time, the clamp switch turns on, connecting an additional capacitor in series with the parallel LC circuit – producing (Fig. 25).

The input voltage for this stage is equal to the peak value of the clamping voltage V_{CL} – which is fully controllable and provides substantial attenuation with even small duty cycle changes when required. This creates two distinct controllable resonant states, each with their own input voltages, resonant frequencies, overall circuit gains, and quality factors.

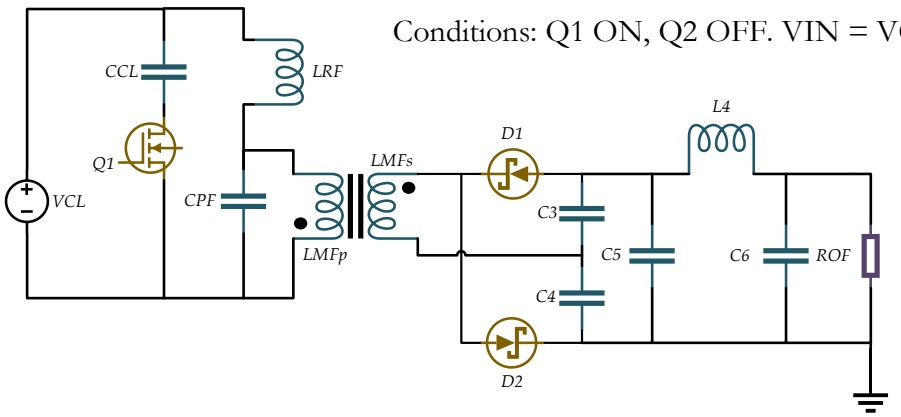

Fig.25: Series-Parallel Resonance Stage of Multi-Resonant Fly-back Converter.

The above circuits can be analysed through extending the methods used in the previous chapters. In fact, it will be seen that any converter exhibiting significant transformer capacitance and capacitive output filters will be subject to attenuation that is directly related to the angular switching frequency and the transformer characteristics such as turns ratio and parasitic capacitances/inductances.

3.6.3 *Design of Duty-Cycle Controlled Multi-Resonant Active Clamp Fly-Back Converter Above Resonance*

After testing with a high-end FRA, the transformer capacitance, measured as 4nF, is used to determine the specific diode conduction angles for an intended switching frequency of 600kHz. The passive components are then calculated to provide the required output voltage with the previously calculated diode conduction angle to provide a simple design process that optimizes the converter for the selected switching frequency to minimize cathode output voltage ripple for enhanced phase-noise performance. Due to the low power nature of the converter, one can utilize small diode conduction angles as the magnetizing current is a function of the output current.

We will start the design by utilizing the novel representation of achievable diode conduction angle presented in equations (3.30) and (3.31). Firstly, note that the cathode output voltage is the average of the voltages generated during the series-parallel (V_{O_L}) and parallel states (V_{O_P}) assuming the output filter imparts negligible voltage ripple on the individual output capacitors of the voltage multiplier at steady-state:

$$V_{O_F} = \frac{V_{O_P} + V_{O_L}}{2} \quad (3.38)$$

We express equation (3.31) as a function of the frequency limitation coefficient and load resistance, which will be constant regardless of the implemented voltages during each state, leaving:

$$\Pi_F = \frac{\pi}{2N_F \varpi_F R_{O_F}} \quad (3.39)$$

Where Π_F and ϖ_c are alternative load and frequency coefficients specific to the fly-back converter. An initial fly-back duty is chosen as 35% and a transformer turns ratio of 0.03406 to limit the maximum drain-source voltage of the fly-back MOSFET and provide some moderate level of step-up to alleviate the tank gain requirement and allow higher switching and normalized frequencies for fixed frequency operation. Very simple modifications to the equations allow a novel expression of the increased and decreased times available to charge and discharge the parallel capacitance. We will define modified effective angular frequencies for the series-parallel ω_{e_L} and parallel ω_{e_P} states, alongside separate load coefficients and diode conduction angles, as follows:

$$\omega_{e_L} = \frac{\pi}{D'_F T_{S_F}} \quad (3.40a) \qquad \omega_{e_P} = \frac{\pi}{D_F T_{S_F}} \quad (3.40b)$$

$$\Pi_{\mathrm{L}} = \frac{\pi}{2N_F^2\omega_{e_L}C_{P_F}R_{O_F}} = 0.194 \qquad \Pi_{\mathrm{P}} = \frac{\pi}{2N_F^2\omega_{e_P}C_{P_F}R_{O_F}} = 0.105$$

$$\theta_L = \cos^{-1}\left(\frac{-\Pi_{\mathrm{L}}+1}{1+\Pi_{\mathrm{L}}}\right) = 47.54° \qquad \theta_P = \cos^{-1}\left(\frac{-\Pi_{\mathrm{P}}+1}{1+\Pi_{\mathrm{P}}}\right) = 35.9°$$

Indicating that the parallel state must deliver more peak current to obtain the same voltage magnitudes. The available conduction angles for the rectifier at varying frequency are shown in Fig.26 for 4nF of total reflected parasitic capacitance and the calculated duty modified rectifier resistance coefficients:

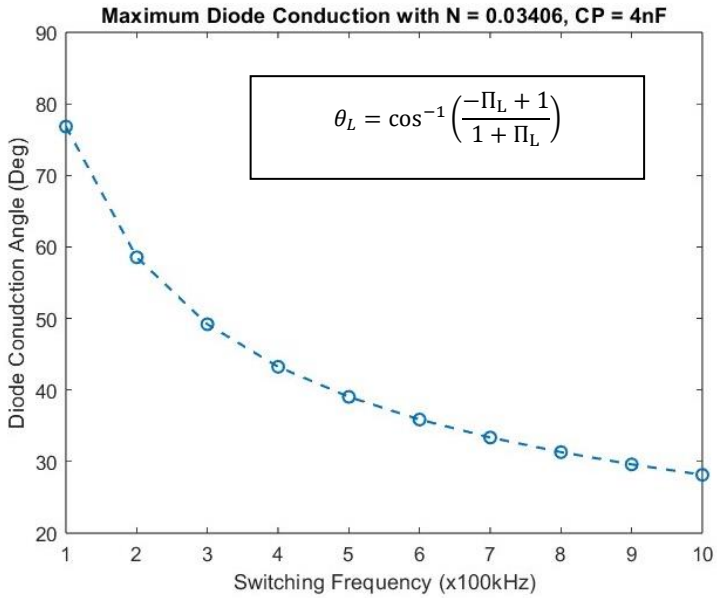

Fig.26: Graphical Representation of Diode Conduction Angle at Designed Transformer Characteristics with Simple Duty Cycle Modifications for Series-Parallel Resonant State.

A higher frequency may be chosen but requires additional gain contribution and peak magnetizing currents from the resonant tank components to generate the same voltage. This often requires navigating closer to the nonlinear resonant peaks of the resonant voltage transfer functions. For completeness, the maximum diode conduction angles for the parallel resonant state for a chosen switching frequency are given below in Fig.27:

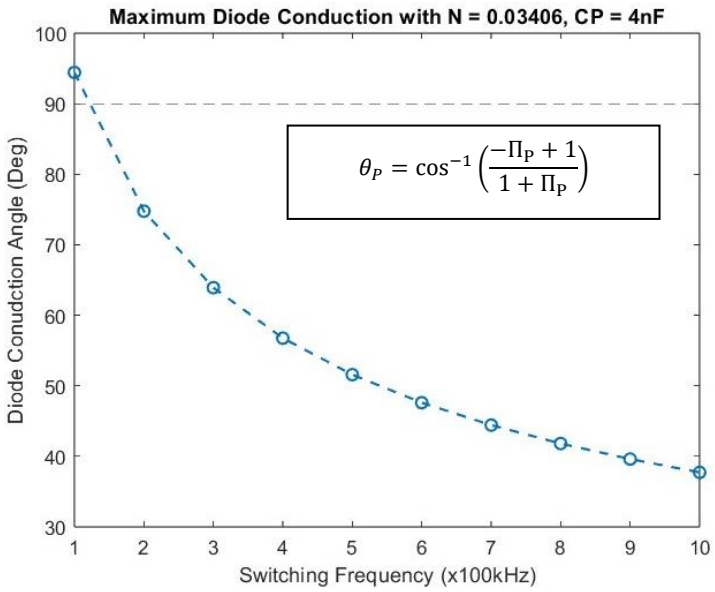

Fig.27: Graphical Representation of Diode Conduction Angle at Designed Transformer Characteristics with Simple Duty Cycle Modifications for Parallel Resonant State.

Equations from [110] will be used within this analysis, alongside modifications to some equations to account for the different resonant stages and the active-clamp nature of the converter from [114] to provide a novel design procedure. Throughout this design, the equations will also be modified to include duty cycle effects on the effective angular frequency. With the diode conduction angles chosen, the corresponding voltage waveform coefficients within each state (k_{v_L}, k_{v_P}) which relate the output voltage and transformer turns ratio to the peak transformer voltages can be calculated:

$$k_{v_L} = 1 + 0.27\sin\left(\frac{\theta_L}{2}\right) = 1.109 \quad (3.41a) \qquad k_{v_P} = 1 + 0.27\sin\left(\frac{\theta_P}{2}\right) = 1.083 \quad (3.41b)$$

Calculation of the equivalent resistance of the modified resonant tank can be calculated utilizing:

$$R_{eq_L} = \frac{R_{O_F} k_{v_L}^2 N_F^2}{2} = 428\Omega \quad (3.42a) \qquad R_{eq_P} = \frac{R_{O_F} k_{v_P}^2 N_F^2}{2} = 408\Omega \quad (3.42b)$$

The peak first harmonics of the transformer voltages can be found through:

$$V_{TX_{HPL}} = V_{O_L} k_{v_L} N_F \quad (3.43a) \qquad V_{TX_{HPP}} = V_{O_P} k_{v_P} N_F \quad (3.43b)$$

With the actual, peak clamped transformer voltages being:

$$V_{TX_L} = \frac{V_{TX_{HPL}}}{k_{v_L}} = V_{O_L} N_F \quad (3.44a) \qquad V_{TX_P} = \frac{V_{TX_{HPP}}}{k_{v_P}} = V_{O_P} N_F \quad (3.44b)$$

To calculate the equivalent capacitances C_{eq_L} and C_{eq_P}, one must define the phase angle between the first harmonics of the transformer voltage and current, which is a function of the diode conduction angle, denoted as β_L and β_P for the series-parallel and parallel resonant states, respectively, below:

$$\beta_L = -25\sin(\theta_L) = -18.44° \quad (3.45a) \qquad \beta_P = -25\sin(\theta_P) = -14.66° \quad (3.45b)$$

$$C_{eq_L} = \frac{2\tan(|\beta_L|)}{N_F^2\omega_{s_F}R_{O_F}k_{v_L}^2} = 206pF \quad (3.46a) \qquad C_{eq_P} = \frac{2\tan(|\beta_P|)}{N_F^2\omega_{s_F}R_{O_F}k_{v_P}^2} = 188pF \quad (3.46b)$$

From this point onward, a novel design procedure will be presented. One significant benefit of the proposed topology is that unlike in standard half-bridge converters, the effective tank input voltages to the resonant converter are substantially higher and can be accurately controlled with duty cycle variation. When the upper half-bridge switch turns off in a standard resonant converter, the source voltage is disconnected.

In an active clamped variation, the peak negative clamp voltage is instead presented to the resonant tank. One can calculate the effective RMS value of the transformer voltage $\widehat{V_{T_r}}$ within any given switching cycle for a bi-polar rectangular voltage assuming some level of voltage ripple $\widehat{V_{CL_r}}$ exists within the clamp capacitor voltage:

$$\widehat{V_{T_r}} = \sqrt{V_{DC}^2(D_F) + \widehat{V_{CL_r}^2}(D_F')} \quad (3.47)$$

The imposed AC voltage variation within the active clamp capacitor is therefore required to allow calculation of the effective RMS voltage presented to the resonant tank circuits. This is particularly true if lower value series resonant capacitors are used to enhance the voltage gain capability of the series-resonant stage. This also allows calculation of the maximum drain-source voltage imposed upon the fly-back MOSFET and will usually dictate maximum duty cycle. The peak clamp voltage $V_{CL_{PK}}$ is related to the effective output voltage during the parallel state and the voltage drop across the series resonant inductor, which is a function of multiple parameters and equal to the drain-source voltage stress of the fly-back switch V_{DS_F}:

$$V_{CL_{PK}} = N_F V_{O_P} + \frac{2L_{R_F}F_{s_F}P_{O_F}}{\alpha V_{DC}D_F(D_F')} = V_{DS_F} \quad (3.48)$$

Where F_{S_F} and D_F are the fly-back switch frequency and duty cycle, respectively. The initial voltage $V_{CL_{INIT}}$ that the clamp charges from is equal to the drain-source voltage stress imposed on the clamp MOSFET, and can be found through:

$$V_{CL_{INIT}} = V_{CL_{PK}} - \frac{\Delta V_{CL}}{2\sqrt{2}} = V_{CL_{PK}} - \frac{I_{CL_{pp}} D'_F(D_F)}{2\sqrt{2} C_{CL} F_{S_F}} \quad (3.49)$$

Where ΔV_{CL} is the clamp voltage ripple voltage, caused by a current $I_{CL_{pp}}$ flowing through the clamp capacitor of value C_{CL}. The effective input voltage during the series-parallel state can therefore be increased through the utilization of larger resonant inductances and smaller clamp capacitors. It is possible to accommodate very small clamp capacitors to theoretically enable rapid transient response and large circuit voltage gains during the series-parallel state. The average RMS voltage imposed on the clamp capacitor, assuming a half-sinusoidal ripple, can be approximated through taking the initial and peak voltage values:

$$\widehat{V_{CL_r}} = V_{CL_{INIT}} + \left(\frac{V_{CL_{PK}} - V_{CL_{INIT}}}{2\sqrt{2}}\right) \quad (3.50)$$

The peak voltages imposed on the parallel capacitor during the parallel $C_{p_{f_P}}$ and series-parallel states $C_{p_{f_L}}$ can be found through the AC voltage coefficients of the passive components, which differ depending on the converter state:

$$N_F V_{O_P} = C_{p_{f_P}} = \frac{k_p \widehat{V_{T_r}}}{k_{v_P}} \quad (3.51a) \qquad N_F V_{O_L} = C_{p_{f_L}} = \frac{k_l \widehat{V_{T_r}}}{k_{v_L}} \quad (3.51b)$$

The difficulty in the design procedure now is that the peak clamp voltage is a function of the output voltage and power generated by the parallel state, the implemented resonant inductances, and the maximum peak-to-peak clamp current magnitude - which are yet undetermined. To operate at fixed frequency, the switching frequency should be substantially above all series ($\omega_{o_{Ls}}$) and parallel resonances ($\omega_{o_{Lp}}$ during the series-parallel state and $\omega_{o_{Pp}}$ during the parallel state) created within the converter. The series combination of the transformer and clamp capacitances in the series-parallel state will always create a frequency higher than that of the parallel resonant state alone. As a result, above resonance, it is likely that the voltage generated by the series-parallel converter will exceed that of the parallel state ($V_{O_L} > V_{O_P}$). The angular frequency relationships of the distinct converter states are:

$$\omega_{o_{Ls}} = \frac{1}{\sqrt{L_{R_F} C_{C_L}}} \quad (3.52a) \qquad \omega_{o_{Lp}} = \frac{1}{\sqrt{L_{R_F}\left(\frac{C_{CL} C_{P_F}}{C_{C_L} + C_{P_F}}\right)}} \quad (3.52b) \qquad \omega_{o_{Pp}} = \frac{1}{\sqrt{L_{R_F} C_{P_F}}} \quad (3.52c)$$

To ensure that the parallel resonant frequencies of the two states are not substantially disparate, one should employ a large series-to-capacitor ratio, but not so large that transient response is degraded. This again demands one to minimize the transformer parasitic capacitance to enable implementation of a smaller A value while maintaining dynamic performance. Choosing a value of A = 0.2 results in a clamp capacitor of approximately 20nF. Making an initial estimate for the normalised angular switching frequency ω_{n_F} of at least 1.3 for now, requires the following:

$$L_{R_F} \geq \frac{1}{\left(\frac{\omega_{S_F}}{\omega_{n_F}}\right)^2 \left(\frac{C_{CL} C_{P_F}}{C_{C_L} + C_{P_F}}\right)} \cong 37uH \quad (3.53)$$

The absolute maximum clamp voltage should be limited to a value somewhat lower than the absolute maximum drain-source voltage ratings of the wide bandgap devices with additional derating applied. The drawback of implementing a small clamp capacitor for enhanced voltage gain and transient response is increased drain-source voltage stress of the fly-back. One novelty of this topology, however, is that higher magnitude output voltages can be generated with reduced drain-source voltage stress for a given turns ratio and duty cycle implementation, assuming the fly-back voltage generated during the charging state is lower than within the series-parallel state (see equation 3.51). If designed properly, the converter can therefore accommodate much higher clamp capacitors with an enhanced transient response while operating at similar drain-source voltages stresses experienced in a standard ACF.

To calculate the peak, initial, and RMS values of the clamp capacitor voltage, first assume that the voltage generated by the parallel state will be somewhat less than the series-parallel state to limit the maximum peak current at full-load such that transformer losses may be optimized:

$$V_{O_F} = \frac{V_{O_L} + V_{O_P}}{2} \qquad V_{O_F} = -4kV \qquad V_{O_P} = -3.7kV \qquad V_{O_L} = -4.3kV$$

The theoretically required magnetizing currents required during the two states, $I_{L_{M_L}}$ and $I_{L_{M_P}}$, can be found with the following expressions:

$$I_{L_{M_L}} = \frac{\pi V_{O_L}}{2N_F \sin^2\left(\frac{\theta_L}{2}\right) R_{O_F}} = 2.034A \quad (3.54a) \qquad I_{L_{M_P}} = \frac{\pi V_{O_P}}{2N_F \sin^2\left(\frac{\theta_P}{2}\right) R_{O_F}} = 2.99A \quad (3.54b)$$

As would be expected, the peak current during the parallel state is higher as it must deliver more peak magnetizing current so develop similar output voltages than the series-parallel state. The absolute minimum peak clamp capacitor voltage can now be found with the calculated parallel state

output values and the minimum series resonant inductance to guarantee a desired minimum normalised switching frequency:

$$V_{CL_{PK}} = -126.02V - 22.7V = -148.72V$$

We can now calculate the initial clamp capacitor voltage utilizing the intended clamp capacitor and maximum peak-to-peak current deviation flowing within it. If we assume the transformer conducts magnetizing current close to the peak quasi-sinusoidal currents, we arrive at:

$$V_{CL_{INIT}} = -148.72V + 31.77V = -116.49V$$

The average RMS value of the clamp capacitor voltage is then found with equation (3.51):

$$\widehat{V_{CL_r}} = -127.86V$$

The effective resonant tank RMS input voltage is found by:

$$\widehat{V_{T_r}} = \sqrt{V_{DC}^2(D) + \widehat{V_{CL_r}}^2(D')} = 176.91V$$

Using equation (3.68) allows determination of the voltage gain or attenuation provided by the series-parallel state k_l:

$$k_l = \frac{1}{\sqrt{\left[1 + \frac{C_{P_F} + C_{eq_l}}{C_{CL}} - \omega_{s_F}^2 L_{R_F}(C_{P_F} + C_{eq_l})\right]^2 + \frac{1}{R_{eq_l}^2}\left(\omega_{s_F} L_{R_F} - \frac{1}{\omega_{s_F} C_{CL}}\right)^2}} \quad (3.55)$$

And for the parallel state, consider the equation for k_P, below:

$$k_p = \frac{1}{\sqrt{\left[1 - \omega_{s_F}^2 L_{R_F}\left(C_{P_F} + C_{eq_p}\right)\right]^2 + \left(\frac{\omega_{s_F} L_{R_F}}{R_{eq_p}}\right)^2}} \quad (3.56)$$

At this point, one must insert the minimum value of resonant inductance that was calculated to determine whether the gain contribution is sufficient or too severe. In this case, a resonant inductance of 40uH was utilized which preserved the required relationships between the two output voltages during each state at the intended duty cycle. Keeping the parallel and clamp capacitor constant and modifying the resonant inductance provides the greatest control as this allows the high frequency parallel relationships of the two states relatively close to each other, which is desirable for fixed frequency operation and reliable operation.

Increasing the resonant inductance to move further away from the resonant tanks as achievable with small duty cycle increases, which increase the effective RMS tank input voltage. This can usually be accommodated as the drain-source voltage stress in this embodiment can be substantially reduced for a given duty cycle and output voltage since the parallel state output diode limits the clamp capacitor voltage to the magnitude generated on the corresponding parallel state output capacitor in the multiplier chain.

To summarize, the following features are obtained with the novel hybrid topology presented above:

1. Changing the fly-back duty cycle modulates the time available for charge of the parallel capacitance through manipulating the diode conduction time. Reducing the duty cycle attenuates the parallel state output voltage, which causes additional attenuation within the effective clamp voltage and thus effective RMS tank input voltage presented to both states to compensate for increased voltage gain during unloading. Small duty cycle changes can cause large attenuation in the total effective cathode voltage. This is indicative of a fully controllable voltage source within the resonant tank.

2. Presents a higher effective tank RMS voltage at steady-state operation when compared to a standard half-bridge resonant converter, such that the required gain from the resonant components is substantially less. This allows higher normalised switching frequencies and thus operation further away from nonlinear resonant peaks at a fixed frequency.

3. With high output resistances, substantial voltage gain is achievable at higher normalised frequencies due to a high resonant tank quality factor. It is essential to fixed frequency operation to ensure the normalised frequency is substantially high to avoid operating at point where the voltage gain during no-load is not too severe to a point where the duty cycle variation required to compensate is too large. Operating far away from the resonant peaking caused by the quality factor also minimizes the slope of the voltage gain transfer function such that component tolerance may have a reduced effect on product-to-product consistencies. This is a similar problem that is observed with fixed-frequency pre-regulation whereby the required voltage deviation within the pre-regulator capacitor is too severe to compensate unloading.

The main drawback of the proposed circuit topology is the difficulty in providing symmetrical transformer voltages, which may cause irregular operation of capacitor-diode voltage multiplier circuits when operating asymmetrically. Gains of the parallel and series-parallel states are dependent on each other due to sharing of the series inductor and parallel capacitor which limits

the achievable symmetry of the transformer voltage. Minimizing the clamp capacitor may allow symmetrical voltage operation and improved transient response but results in higher peak drain-source voltages and lower effective tank RMS input voltages.

Since the output voltage is formed by the average output voltages that would be generated by the series or series-parallel resonant stages alone, any attenuation of the series-parallel resonant state through insertion of additional series resonant capacitance can easily be accounted for through accompanying increases in the parallel circuit output voltage through increases in duty cycle. Through processing a small portion of the EPC power, the duty-cycle to output voltage relationship is significantly more linear than would be achievable in a single converter, high-power variable frequency EPC solution. Sub-resonance protection is not required due to operation at an optimized, fixed frequency.

The limitations of the parallel resonant capacitance can be overcome in the hybrid EPC topology since the additional circulating current due to operation closer to the resonant peak will be less critical due to the reduced processing power of the fly-back and ability to generate the full voltage at low diode conduction angles. Providing additional tank current to charge and discharge the parallel capacitance enables higher conduction angles and increased output voltage for a given load coefficient. Due to the hybrid partitioning of power depending on the electrode to be supplied, one could implement higher gains from within the resonant tank of the fly-back while accommodating any increases in circulating current. The circuit in Fig.28 illustrates the mechanism through which the average cathode voltage is generated through provision of an asymmetric transformer voltage. The graphic also shows the relationship between the output capacitor and diode voltages and how these relate to the voltages generated in each state.

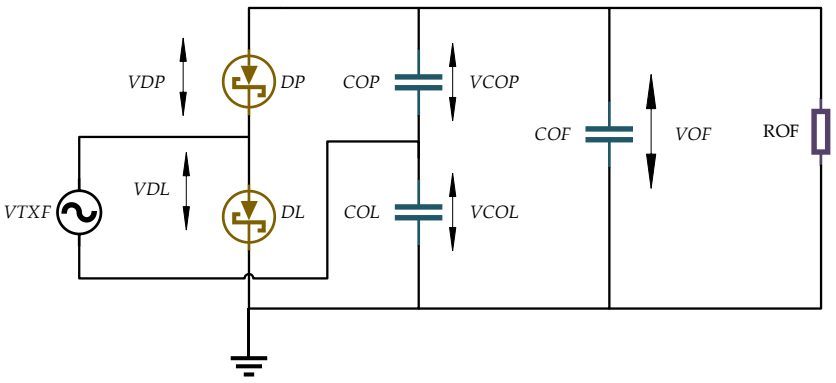

Fig.28: Development of an Average Cathode Voltage through Modulation of Individual State Capacitor Voltage Levels in a Full-Bridge Voltage Doubler Circuit.

The voltage relationships are summarised in the equations below:

$$V_{CO_P} = \frac{V_{O_P}}{2} \quad (3.57a) \quad V_{CO_L} = \frac{V_{O_L}}{2} \quad (3.57b)$$

$$V_{D_P} = V_{D_L} = V_{CO_P} + V_{CO_L} = V_{O_F} \quad (3.58)$$

The rectifier diodes can therefore handle asymmetric excitation without issue as the voltage imposed upon them are equal at steady state. Regulation is achieved by increasing or decreasing the state voltages through modulation of the effective clamp capacitor voltage which, in-turn, modulates the average DC voltage supplied to the cathode electrode from the output rectifying network. This is a simplified analysis that assumes very little or no voltage ripple within the rectifier capacitors.

4 STEADY-STATE AND DYNAMIC EPC SIMULATIONS

4.1 SERIES-PARALLEL COLLECTOR EPC

4.1.1 Steady-State Performance

The implemented components within the collector electrode EPC are summarized below:

Collector Regulator Component Name	Value
Output Voltage	-3,000V
Series Resonant Inductance	49uH
Transformer Magnetizing Inductance	500uH
Series Resonant Capacitance	28nF
Parallel Resonant Capacitance	18nF
Transformer Turns Ratio	0.0500
Output Load Resistance	14.3kΩ

Table 1: Collector EPC Component Selection.

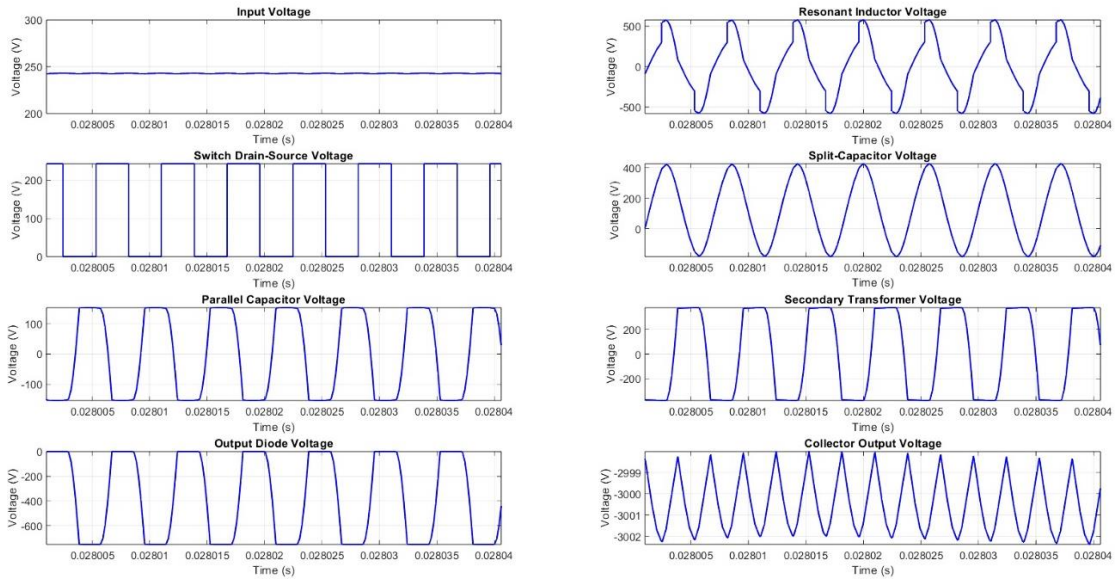

Fig.29: – Full-Load Voltages of the Series-Parallel Resonant Converter at 243V Line Voltage.

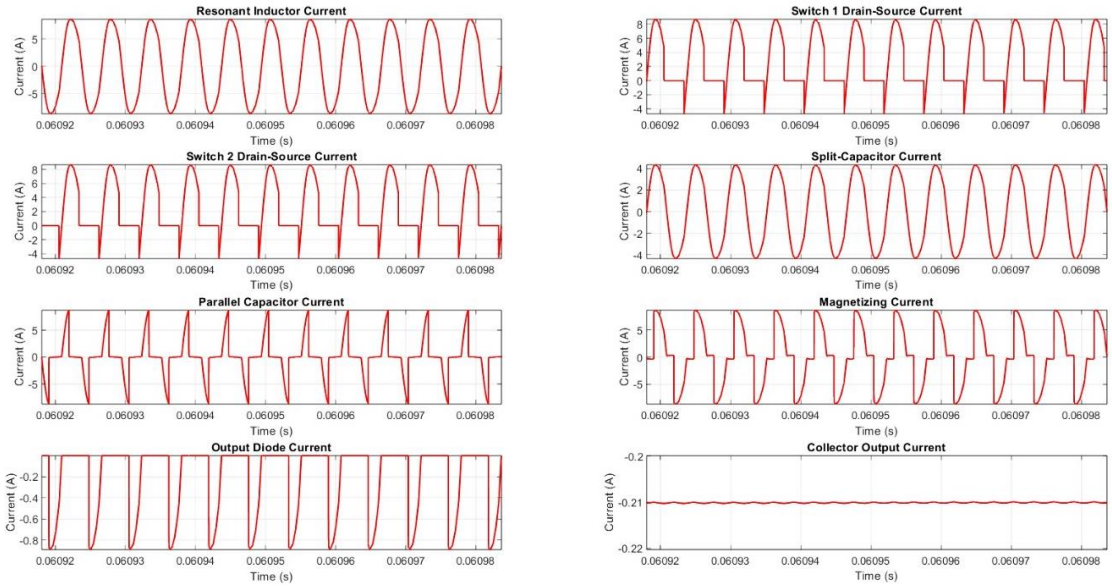

Fig.30: Full-Load Currents of the Series-Parallel Resonant Converter at 243V Line Voltage.

The 600W single depressed collector series-parallel regulator EPC at a variable switching frequency as this has minimal impact on phase-noise performance of the TWT. The minimum switching frequency is 176kHz and occurs at low-line DC input and full-loading. The voltage and current waveforms of the series-parallel converter at full-load switching frequency of 176kHz and low-line DC input voltage of 243V are shown in (Fig. 29) and (Fig. 30). The peak current within the converter is approximately 8.2A, which is slightly less than the calculated maximum value provided in theory. The waveforms are sinusoidal in nature, and the negative excursion within the drain-source current of the MOSFET waveform indicates that soft-switching is achieved with the design.

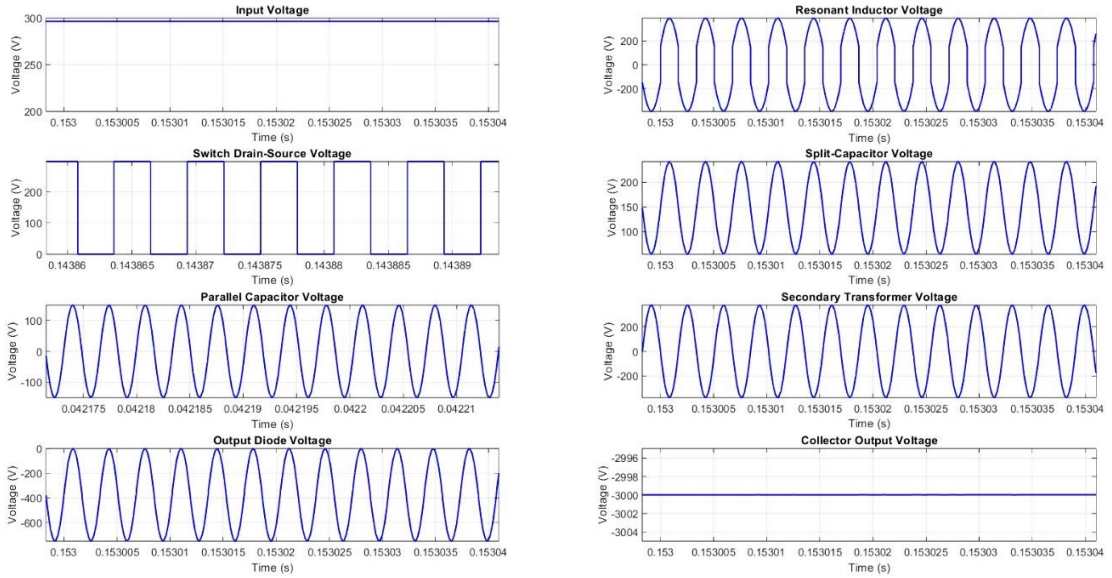

Fig.31: Full-Load Voltages of the Series-Parallel Resonant Converter at 297V Line Voltage.

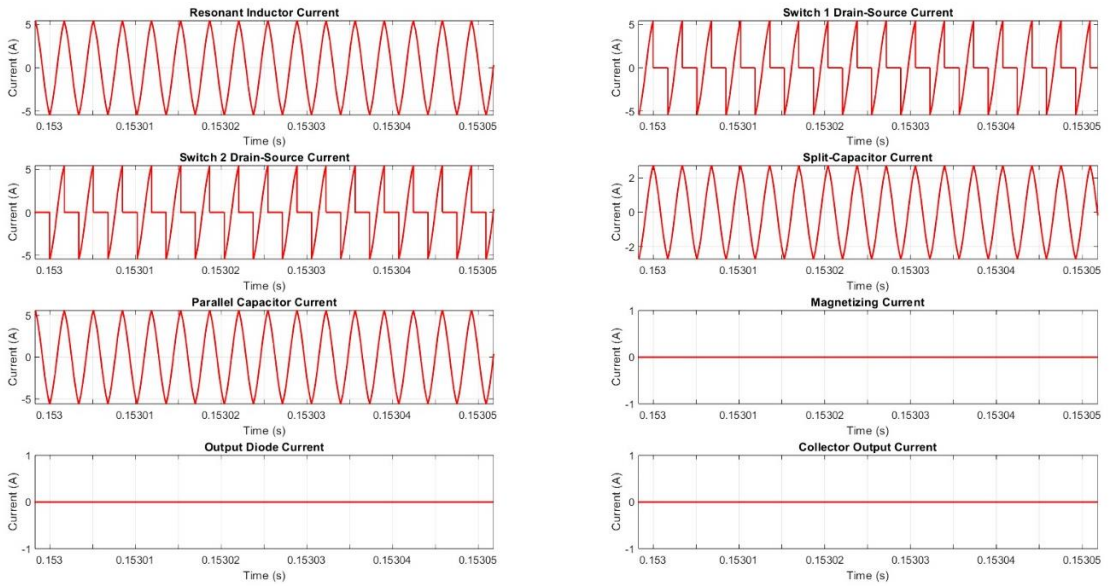

Fig.32: No-Load Currents of the Series-Parallel Resonant Converter at 297V Line Voltage.

During periods of no RF amplification, the transistor switching frequency increases to halt resonant power delivery to the output load. The highest switching frequency required to achieve collector regulation occurs at the highest line voltage and zero-loading level, requiring the largest level of attenuation from the resonant circuit voltage transfer function. With the calculated passive component values, the parallel resonant frequency occurs at a frequency of 236kHz. The regulation frequency will be a value somewhat above this due to the no-load resonant peaking. The results in (Fig.31) and (Fig.32) are taken with a no-load regulation frequency of 295kHz at 297V of DC input voltage. The largest no-load frequency required occurs at high-line input DC voltage of 297V, as this demands the largest level of attenuation with the voltage transfer function.

If standard VMC is implemented, provision of higher maximum frequencies allows sufficient safety margin during RF amplification transient events and minimizes voltage deviation at the expense of increased frequency related losses. At the expense of additional circulating current at both full and zero-loading conditions, the increased parallel capacitor allows measurable reductions in the regulation bandwidth. The resonant waveforms in the no-load case become more triangular, and no current is transferred through the magnetizing inductance. Circulating current is purely reactive and constrained to within the resonant tank, which will cause lower efficiency at no-load, but is not detrimental to phase-noise performance of the tube. A reduced bandwidth is much preferred. For the voltage waveforms, the frequency has been increased to a point whereby the time allowed for charge and discharge of the parallel resonant capacitance creates sinusoidal voltages within the converter, and the output diodes do not conduct output current.

4.1.2 *Transient Performance with Voltage Mode Control*

To demonstrate the issues faced regarding control of high-power resonant converters, a closed-loop digital controller is first implemented to attempt to linearize the converter and provide regulation. It can be clearly observed that characteristics within the controller that were previously outlined such as self-oscillation at full power are present due to the requirement for operation close to the non-linear resonant peaks of the control-to-output transfer function:

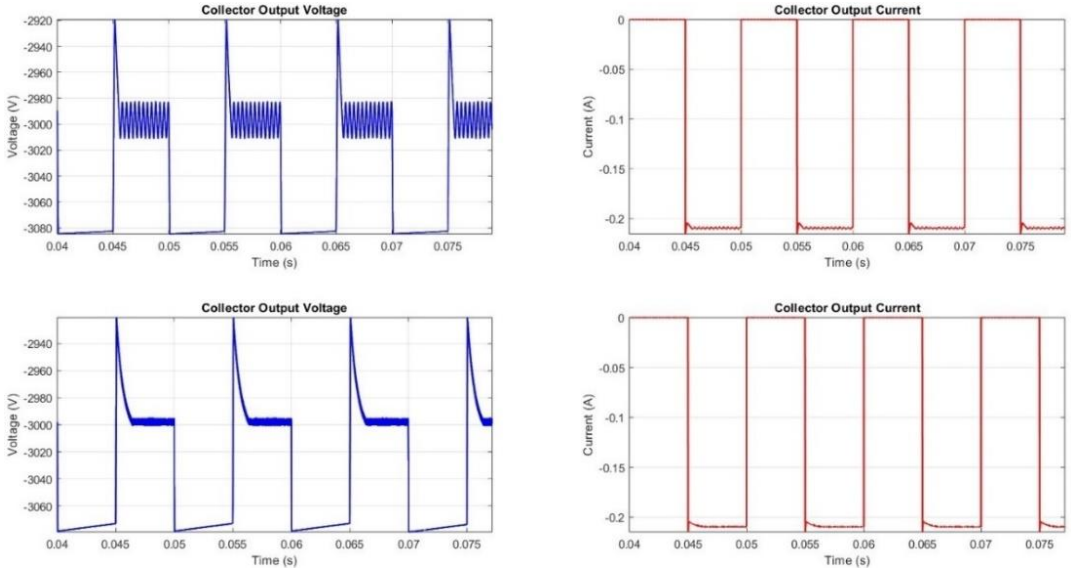

Fig.33: Instability of Collector EPC without (top left, right) and with (bottom left, bottom right) Sub Resonance Protection.

The voltage deviation during no-load is within the required limits for the collector, with undershoot/overshoot of approximately +/-2.7%, or +/-80V, from the nominal specified voltage. As discussed, such an overshoot occurring within the collector electrode does not substantially impact phase-noise performance of the RF amplification process. Deviations in the collector voltage from nominal, however, do impact the overall efficiency of the TWT and therefore, ideally, be minimized during both steady-state and any dynamic operating conditions.

During a transient event with VMC, the second-order response to changes in control voltage within the oscillator can clearly be observed, with many switching cycles being required before the average output current reaches the appropriate value. This is detrimental to the achievable controller bandwidth and thus peak voltage deviation during a given load current transient during pulsed-mode operation of the TWT. The oscillations increase in severity as the PRF increases substantially and can only be stabilised with the insertion of low power density capacitances such as electrolytics. The peak voltage deviation during any transient even can be reduced through increasing the output

capacitance or through utilization of a higher no-load frequency. Alternatively, the PRF information can be utilized to instantly prevent resonant current flow during no-load, as seen in Fig.34 below:

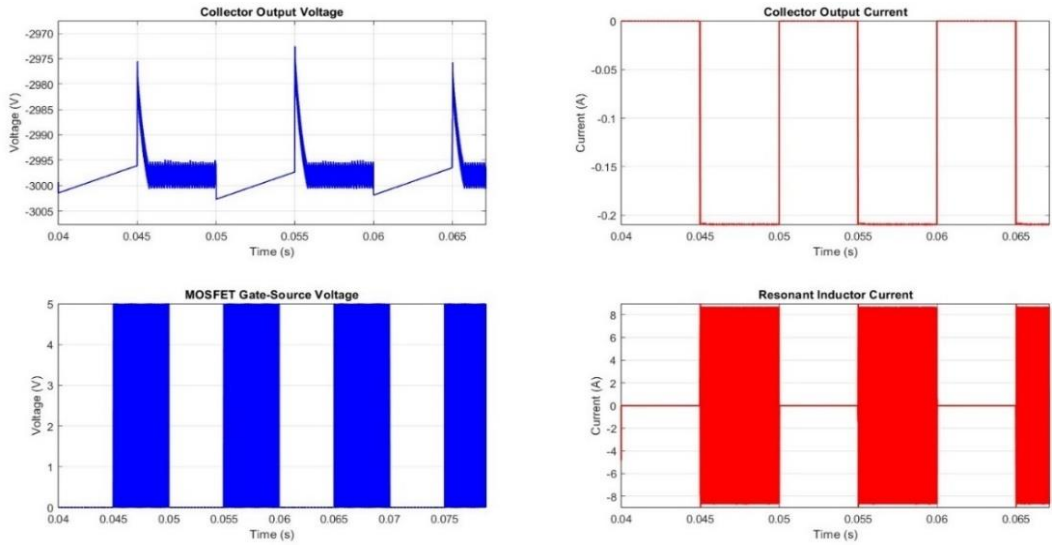

Fig.34: Simple Implementation of PRF Information to Reduce Transient Voltage Deviation within the Collector Electrode.

The undershoot/overshoot has been reduced to approximately +25V/-5V, a substantial improvement over the standard VMC case demonstrated in Fig.33. This technique allows a more constant depression ratio between the cathode and collector to be achieved across operating conditions, leading to improved efficiency. There is also an apparent increase in effective controller bandwidth due to significant improvements within the maximum voltage deviation within the collector during dynamic events. This allows regulation of the collector to be achieved in a reduced time. These factors, combined, have been shown to be optimal for tube efficiencies. The frequency range for regulation is substantially reduced, such that only small frequency variances are required to accommodate input voltage variations during full-load operation. Since no switching occurs at no-load, the converter can be substantially free of noise during periods where RF amplification does not take place. Recovery from a load step is considerably faster, such that steady state can be reached in a reduced time even with low bandwidth controllers.

4.2 MULTI-RESONANT ACTIVE CLAMP FLY-BACK CATHODE EPC

4.2.1 Steady-State Performance

The summary of the chosen component values is given in the table below. The voltages generated by the series-parallel and parallel states are -4.32kVDC and -3.715kVDC respectively. The clamp voltage is increased to approximately 125VDC at low-line and full-loading conditions. The utilized values for the simulation are shown below in Table 2. The most critical converter full-load voltage and current waveforms may be observed in Fig.35 and Fig.36, respectively.

Cathode Regulator Component Name	Value
Output Voltage	-4,000V
Series Resonant Inductance	41uH
Transformer Magnetizing Inductance	500uH
Series Resonant Capacitance	20nF
Parallel Resonant Capacitance	4nF
Transformer Turns Ratio	0.03406
Output Load Resistance	600kΩ

Table 2: Multi-Resonant Fly-back Cathode EPC Component Selection.

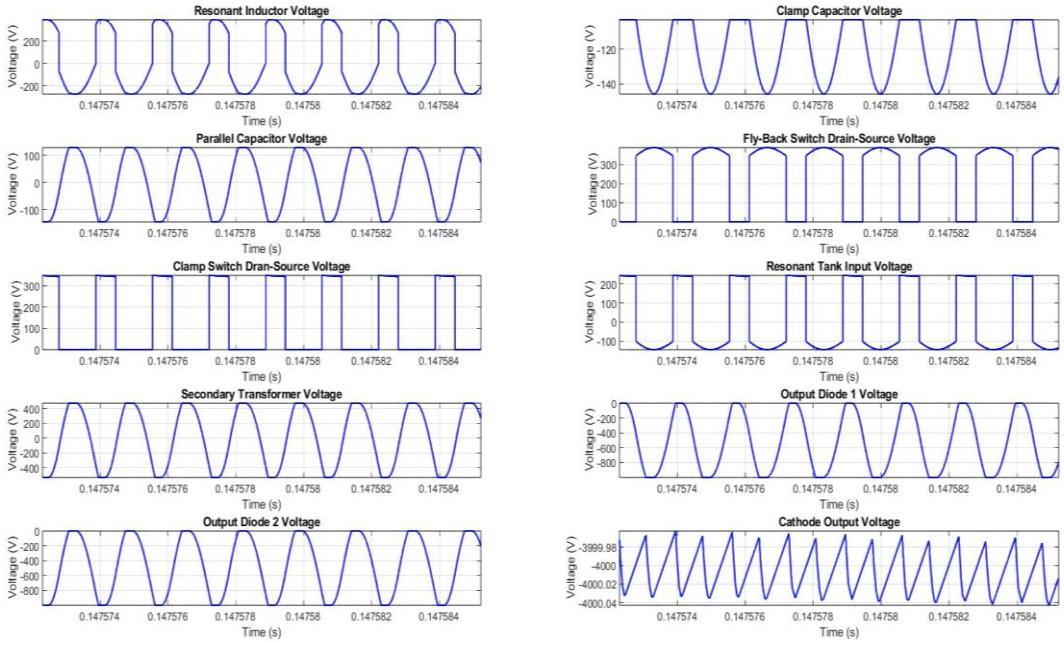

Fig.35: Full-Load Resonant Fly-back Converter Voltage Waveforms with 243VDC Input Voltage at a Switching Frequency of 600kHz and ~35% Duty Cycle.

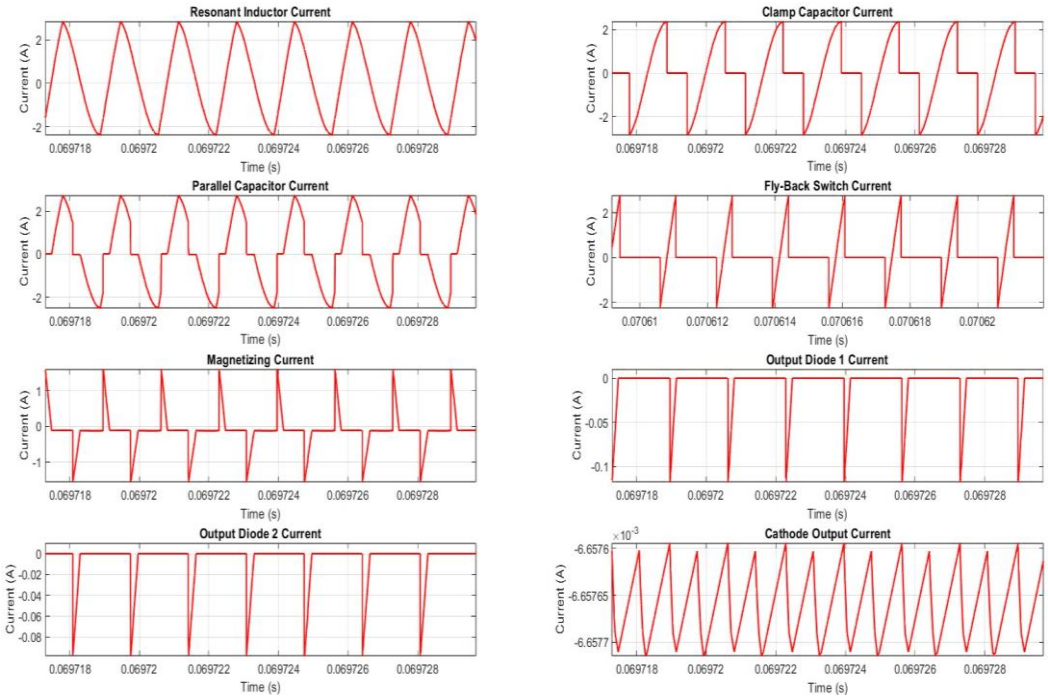

Fig.36: Full-Load Resonant Fly-back Converter Current Waveforms with 243VDC Input Voltage at a Switching Frequency of 600kHz and ~35% Duty Cycle.

The above results show SPICE simulations of the resonant ACF converter at steady-state conditions. The switching frequency is 600kHz. With the implemented tank values calculated, the simulation results agree well with the theoretical design expressions for the fly-back converter at 600kHz switching frequency and the maximum duty cycle under minimum line conditions. The voltage during the parallel state is approximately -3.78kV and is approximately -4.227kV during the series-parallel state. Overall voltage ripple observed within the cathode electrode is just 0.06V.

One observation is that these voltages were generated at magnetizing currents somewhat below the required magnetizing current in the given design procedure. This may be since the circulating current within the resonant inductor, which is available to discharge the parallel capacitor, may substantially exceed the peak magnetizing currents due to resonant behaviour. This is a weakness within the given research, and it is proposed that future work consider both the resonant inductor and magnetizing currents and the impedance relationships to determine the achievable output voltage for a given conduction angle. At low-line, the peak clamp voltage is -148V, with an RMS value of approximately -120V which closely agrees with the calculated values. Due to the low conduction angles required to deliver the minimal current necessary to power the cathode, the voltages within the tank are more sinusoidal than can be seen in the regulator for the collector. The reduced rise and fall-times of the transformer and output diodes may also additionally contribute to reduced noise within the cathode, leading to theoretically superior phase-noise performance due to reduced AC voltage variations. The cathode output voltage can achieve less than 0.1V of AC

voltage variation with just a capacitive output filter, which can be substantially improved with the use of second-stage filtering techniques. Increases in load current can easily be achieved through either increases in duty cycle or reduction in the normalised switching frequency through either increasing the tank resonant frequency or reductions in the switching frequency. Which method is most appropriate will depend on the allowable drain-source voltage stress of the implemented transistor devices, the transformer parasitic capacitance, and the allowable peak currents within the inverter. The typical voltage and current waveforms for the converter under no-load conditions, respectively, are given below in Fig.37 and Fig.38:

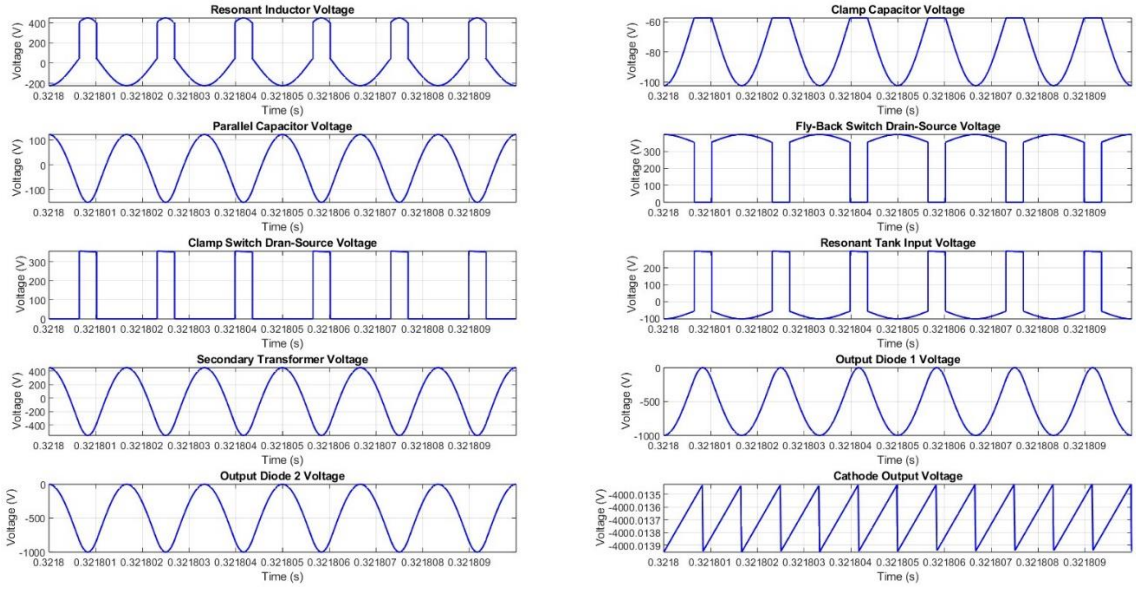

Fig.37: No-Load Resonant Fly-back Converter Voltage Waveforms with 297VDC Input Voltage at a Switching Frequency of 600kHz and ~22.4% Duty Cycle.

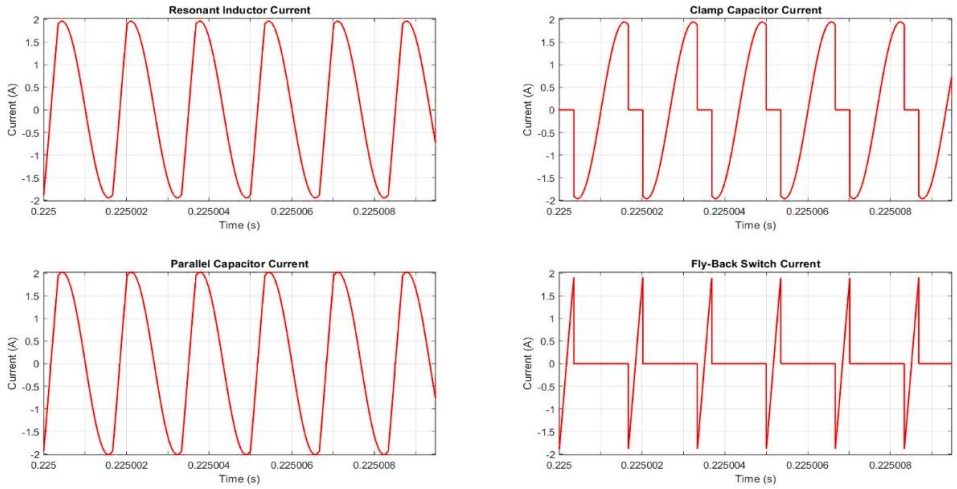

Fig.38: No-Load Resonant Fly-back Converter Current Waveforms with 297VDC Input Voltage at a Switching Frequency of 600kHz and ~22.4% Duty Cycle.

Like the collector regulator, the entirety of the current flows through the parallel transformer capacitance when the load is removed. The resonant waveforms can be seen to be quasi-sinusoidal across all line and loading conditions. The resonant tank input voltage can be seen to be substantially reduced to compensate for the increased gain during converter unloading.

4.2.2 Transient Performance with Voltage Mode Controller

The cathode must be able to maintain tight regulation of the output across any combination of line and loading conditions. The PRF can range anywhere from 100Hz to 100kHz at varying duty cycles depending on the radar operating mode. The converter's ability to effectively regulate the output voltage across high, medium, and low PRF modes at the nominal line voltage are shown in Fig.39, Fig.40, and Fig.41, respectively:

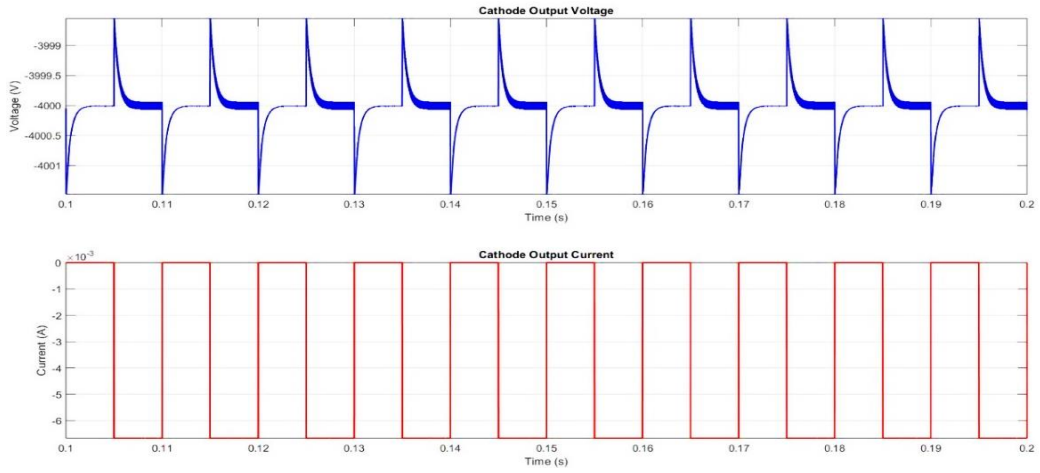

Fig.39: Low PRF Regime of 100Hz with a Duty Ratio of 50% with Voltage Mode Control.

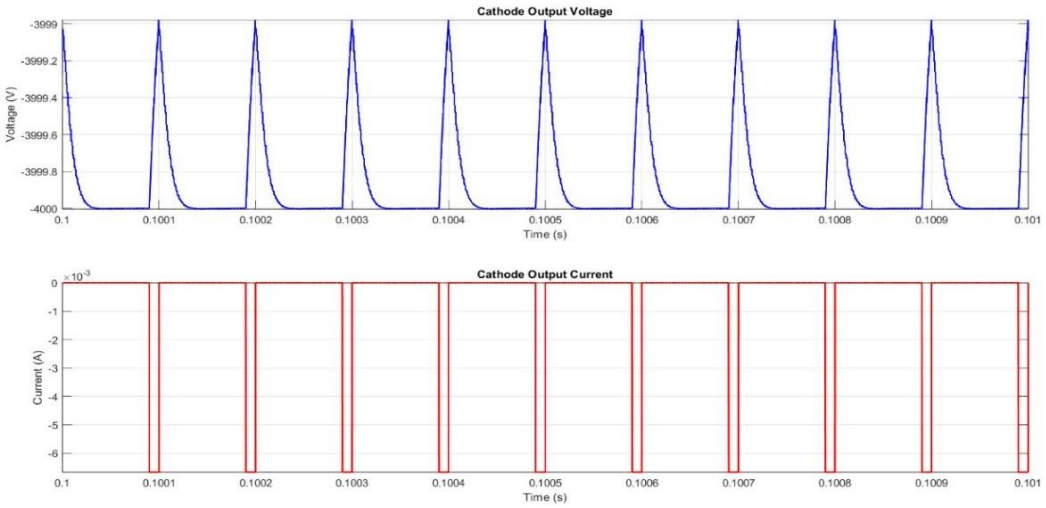

Fig.40: Moderate PRF Regime of 10kHz with a Duty Ratio of 10% with Voltage Mode Control.

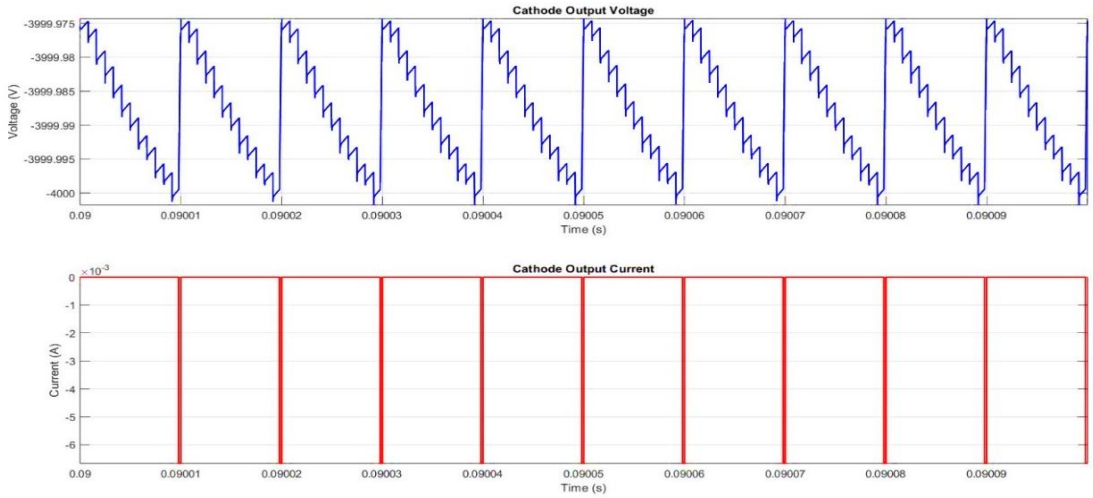

Fig.41: High PRF Regime of 100kHz with a Duty Ratio of 2% with Voltage Mode Controller.

Aggressive transients within the input voltage, like those in Fig.42 below, are also modelled in PLECS to demonstrate the effectiveness of the controller:

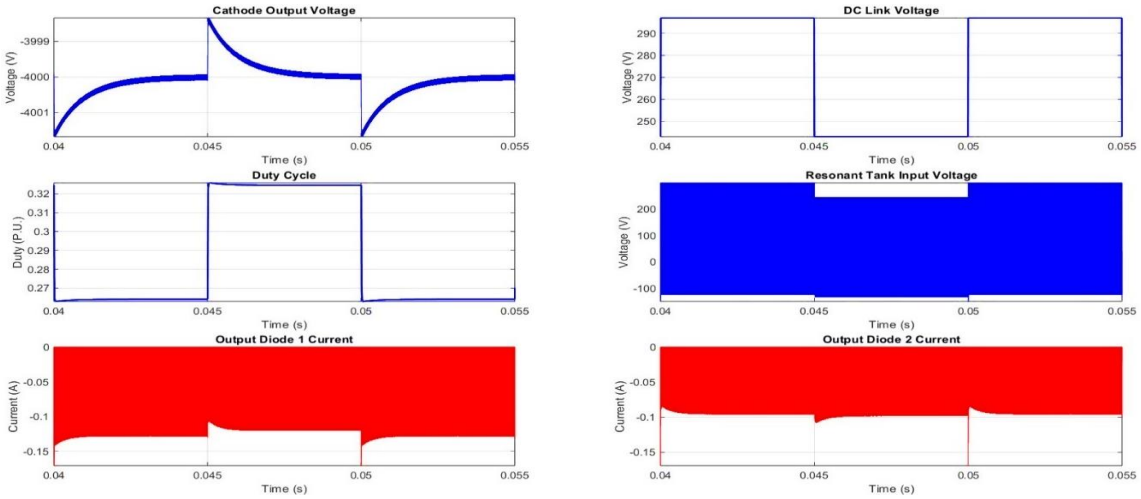

Fig.42: Transient Response during a 243-297V Input 100Hz Transient Event with VMC.

From the above figures, the controller can provide good regulation across all line and loading conditions. The peak deviation within the cathode voltage is less than +/-5V across each implemented PRF and duty cycle combination, and in every case the cathode voltage is returned to steady-state before generation of a new radar transmission pulse occurs. During an input voltage transient, the resonant tank input voltage is either increased or decreased appropriately. When the input voltage reaches the maximum allowable value, the peak clamp voltage presented to the parallel converter stage can be seen to be reduced accordingly to compensate. This also causes the peak currents within the second output diode, which conducts during this stage, to decrease. This ensures that a constant, average current is flowing within the rectifier such that the output voltage

can be maintained effectively during the transient event. Due to the low conduction angle of the rectifier, the change in resonant tank current when the converter is unloaded is small. The second-order response to changes in duty cycle, present in a standard VMC series-parallel converter, is clear. Despite this, the converter maintains stability and linear response to duty cycle changes across all line and loading conditions. The controller bandwidth with VMC is approximately 5.33kHz.

4.2.3 Transient Performance with Average Current Mode Controller

Without specialist control techniques, resonant converters are restricted to voltage mode control to substantial detriment of the controller bandwidth. In the modified resonant fly-back converter, however, one can substantially increase the bandwidth with an additional Current Sense Amplifier (CSA) and Average Current Mode Control (ACMC) of the resonant tank current. A second-stage filter π-filter may be added, to provide substantial attenuation of the switching frequency and resistive damping. For critical damping, the quality factor of the filter, Q_d, should be equal to 1 and is related to the highest cut-off angular frequency of the second-stage filter ω_{h_f}, the first output capacitance C_{f1}, the equivalent series resistances of the two output capacitors (R_{dC_1}, R_{dC_2}), and filter inductor equivalent series resistance $R_{d_{Lf}}$ combined:

$$Q_d = \frac{1}{\omega_{h_f} C_{f1}(R_{d_{Lf}} + R_{dC_1} + R_{dC_2})} \qquad (4.01)$$

The performance of the regulator with ACMC and following the insertion of an additional passive second-stage filter, is demonstrated in Fig 43. This waveform is observed at the output node before the filter, where the cathode feedback voltage would usually be derived, to avoid additional phase-degradation within the control transfer function.

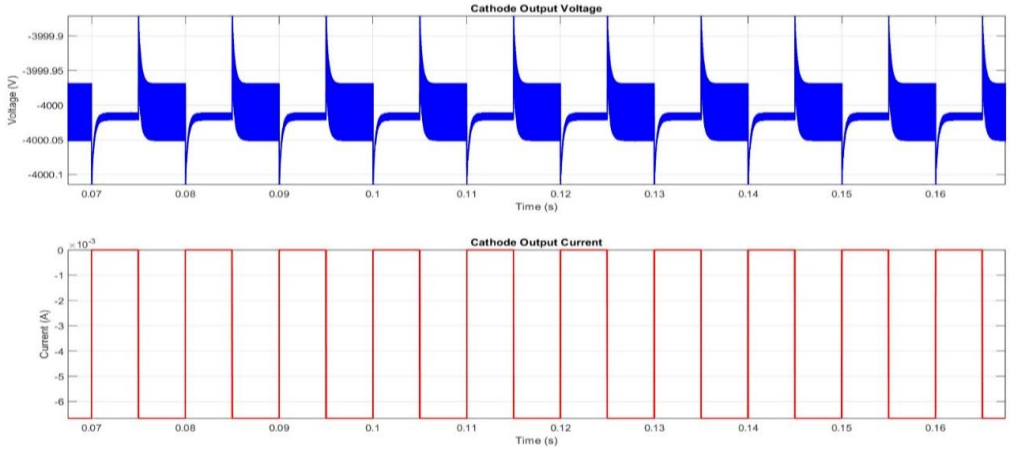

Fig.43: Low PRF Regime of 100Hz with a Duty Ratio of 50% with ACMC and CSA.

For optimum damping and to provide sufficient filtering, a large total resistance is often required. To avoid interfering with the performance of the filter, it is preferred to not insert additional effective ESR into the output capacitors. The voltage feedback resistive network remains at a point before the filter, to ensure any introduced phase-shift does not influence regulation performance. Instead, it is inserted into the series filtering inductor at the expense of introducing voltage drop between the point at which regulation is performed and the actual low-noise collector output. Interestingly, the peak voltage deviation from the cathode nameplate voltage during any dynamic events has been substantially decreased from approximately 2V to approximately 0.2V, resulting in a bandwidth ten times higher than with VMC of ~50kHz. Due to the significant required series damping required to provide significant attenuation without oscillation, a voltage drop occurs at the actual cathode electrode voltage when RF amplification takes place. The simulation result in Fig.44 illustrates this phenomenon, and is taken at the node which supplies the cathode electrode, following the passive filter:

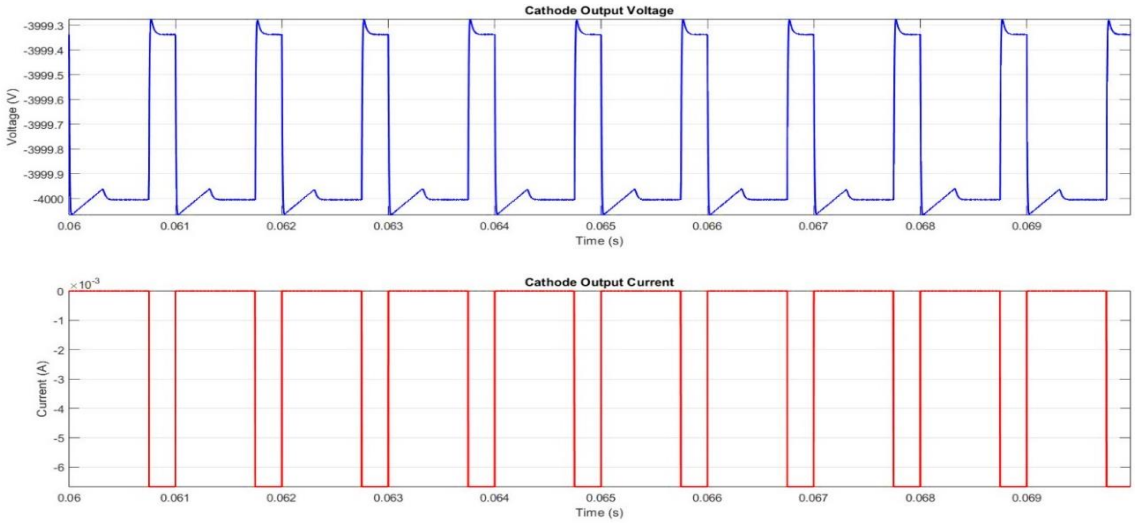

Fig.44: Low/Moderate PRF Regime of 1kHz with a Duty Ratio of 25% with ACMC and Current Sense Amplifier and Series Damped Pi-Filter.

This essentially imparts an artificial ripple frequency with magnitude equal to the voltage drop of the series resistor at the PRF frequency. Alternatively, the damping resistor can be reduced or removed entirely, and insertion of a third-stage RC filter before the cathode load provides substantial attenuation of both switching frequency harmonics and any undamped oscillations from the previous stage. The output filter topology is shown in Fig.45. The respective voltages during the parallel and series-parallel state are denoted C_{O_P} and C_{O_L} respectively, with R_{O_F} representing the purely resistive cathode load.

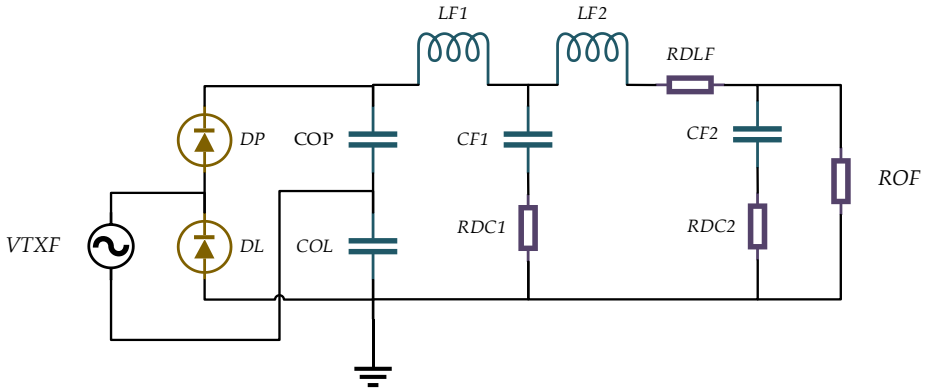

Fig.45: Second-Stage Filter with additional RC Filter Stage for Low-Noise Cathode.

A comparison of filtering performance of the second-stage pi-filter, and the one proposed with an additional R-C filter in Fig.45, are illustrated in Fig.46 below. Both cases utilize ACMC.

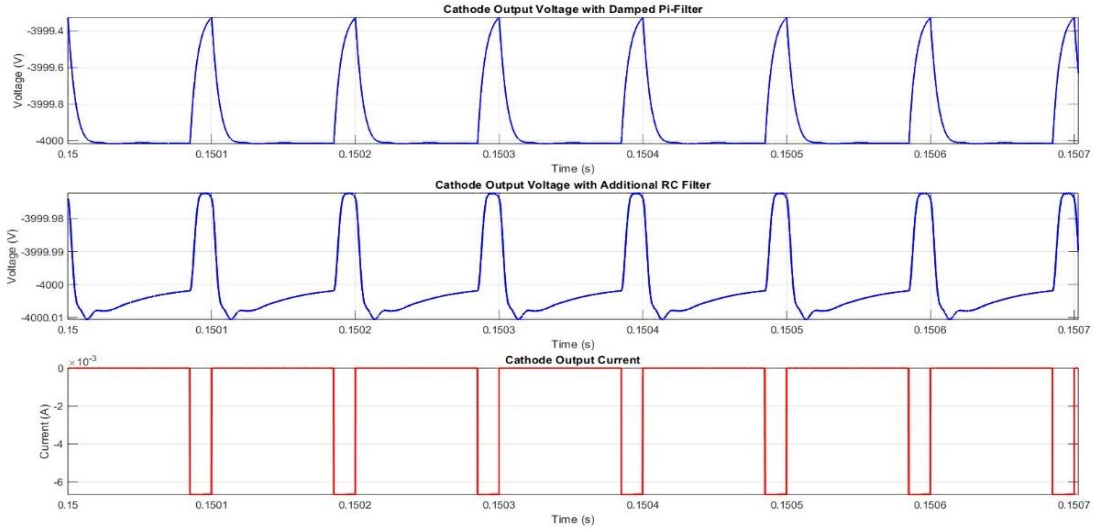

Fig.46: Comparison of Pi-Filter Alone and Additional R-C Filtering Techniques for Achieving Ultra-Low-Noise Cathode Electrode Voltages.

From the above figure, the peak deviation from the cathode electrode voltage during a 10kHz pulse regime is approximately 0.7V in the series damped case and is substantially reduced to less than 0.04V when an additional RC filter is implemented. The cathode steady-state AC voltage variations in the damped filter case are clearly observed in Fig.47, where less than 500 microvolts of AC voltage have been achieved due to the proposed modifications. The drawback of this technique is a slight increase in power dissipation and thus reduced overall efficiency, however this is secondary to the improvements in phase-noise performance due to minimal phase-pushing contributions from the cathode ripple voltage. This technique is only suitable for low-power outputs, whereby a large damping resistor can be used without dissipating significant amounts of power, requiring a physically large damping resistance package size.

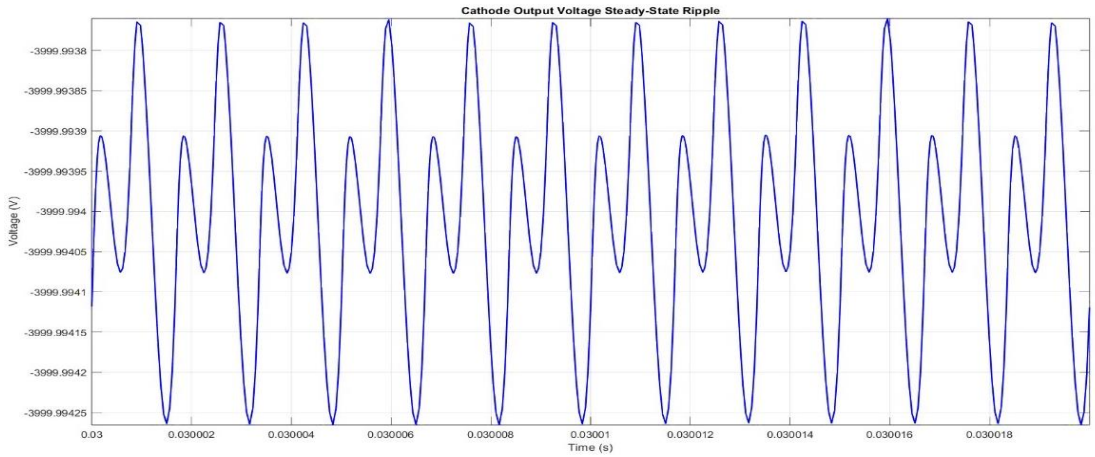

Fig.47: AC-Voltage Cathode Variation at Steady-State of approximately 500uV.

Effective regulation of the cathode has been achieved with minimal voltage drop. Substantial attenuation of the AC-voltage variations and impressive dynamic performance has been achieved across all loading PRF regimes. Due to the very low output current of the cathode, a large resistor can be utilized, minimizing the required additional filter capacitor of the RC filter. For optimal performance of a second-stage filter, the second output capacitor should be substantially higher than the first – ten times is often implemented. This ensures that the second filter resonance is fixed across any operating conditions and will not be affected by any capacitive loading. This becomes difficult at higher frequencies where most of the filtering will be performed at lower voltage potentials such as within the voltage multiplier rectifiers. The third-stage RC filter provides some compensation for this drawback.

A particularly important benefit of this topology can be seen within the waveforms regarding the peak voltage deviations during any transient voltage event. Since the collector regulator does not share the cathode supply, which is frequently seen in literature, the high magnitude current transient events within it have no effect on the voltage magnitude deviation observed within the cathode. This would suggest that a lower peak voltage deviation would be achievable with lower output capacitance and controller bandwidth. This topology is particularly suitable for generation of moderate voltages at low currents at high, fixed switching frequencies such as those within airborne MPM devices. At higher power and output voltages, the requirement for operation close to the resonant peaks which exhibit nonlinear characteristics will remove the possibility for operation at fixed switching frequency across all line and loading conditions due to the required changes in duty cycle magnitude to provide sufficient compensation. This issue is commonly associated with pre-regulation, whereby the required change in regulated input voltage is far too severe to be accomplished within an effective bandwidth. There are also substantial limitations with resonant converter control under high switching frequency due to passive component optimization in series-

parallel converters which will place limitations on both the minimum parallel capacitance and maximum transformer turns ratio to ensure diode conduction angles do not exceed 90 degrees at full-loading operation.

High frequency operation of such converters will often require a substantially low series resonant inductance, such that the improved frequency selectivity of a series-parallel converter substantially deteriorated due to issues regarding quality factor and series-to-resonant capacitor ratios. Such issues can be alleviated through minimizing the transformer parasitic capacitance. In low-power resonant converters, the response to duty cycle is much more linear, such that the benefits of resonant power conversion can be coupled with benefits of PWM duty-cycle fixed frequency control to provide an optimal regulation for the cathode electrode of the MPM with high bandwidth control. Operation of high-power resonant converters is therefore limited to variable frequency control and at lower frequencies, such that optimization within their efficiency is instead achieved. Alternatively, increases in frequency away from the non-linear resonant peaks would provide further linearization of the control-to-output transfer function for improved fixed-frequency control of the cathode voltage. A final issue with the proposed circuit is the presence of DC current within the transformer due to asymmetrical voltage drive. This tends to become more severe as magnetizing inductance decreases. A larger magnetizing inductance reduces the experienced magnitude of DC current but may also reduce the converter's dynamic ability due to the creation of lower RHPZ frequencies.

4.2.4 Steady-State and Dynamic Performance of Novel Four-Element Multi-Resonant Fly-Back

There are multiple ways to increase the output power of the novel proposed converter. The previous converter consists of a series-parallel stage during clamp switch turn-on, and a parallel resonant charging stage during fly-back switch turn-on. The achievable conduction angle for a given choice of parallel capacitor and transformer turns ratio can limit the output power without moving substantially closer to the non-linear resonant peaks of the converter. The maximum output voltage is limited by the resistance coefficient, which is a function of the angular switching frequency, transformer turns ratio, and the selected parallel transformer capacitance. It will now be proposed that, alternatively, reductions in the transformer magnetizing inductance can also enhance the output voltage capability for a constant parallel capacity, switching frequency, and transformer turns ratio by allowing additional magnetizing current to transfer to the load as impedance is reduced. This essentially forms an additional, novel resonant fly-back topology that has enhanced voltage gain capability.

The new circuit topology can be seen in Fig.48 and differs from Fig.22 through the modelling of an additional inductance in parallel with the transformer parallel capacitance. This is typically not realised with a physical inductor but is achieved through the modification of the magnetizing inductance such that it is of a substantially lower value. This modification creates an additional resonance and provides additional benefits which will be further discussed.

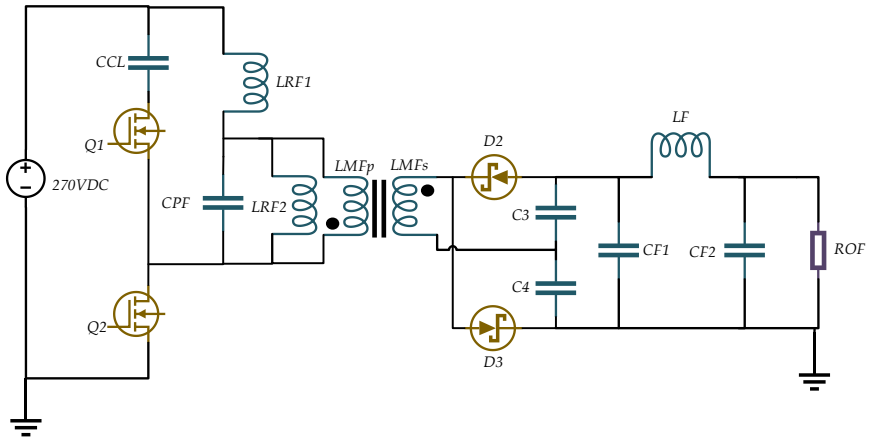

Fig.48: Proposed Four-Element Multi-Resonant Active-Clamped Fly-Back Converter Topology.

The magnetizing inductance has been reduced to 100uH, with the transformer turns ratio, maximum duty cycle, parallel capacity, and load resistance kept constant. Fig.49 and Fig.50 show the converter voltage and current waveforms respectively, when operated under full-loading conditions:

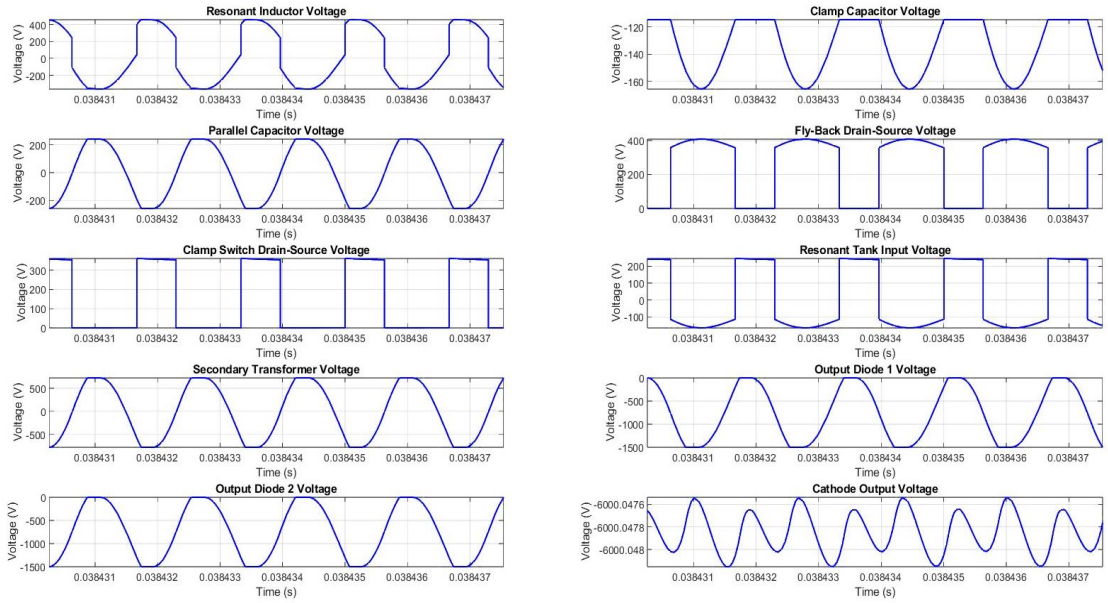

Fig.49: Full-Load LLCC Resonant Fly-back Converter Voltage Waveforms with 243VDC Input Voltage at a Switching Frequency of 600kHz and 35% Duty Cycle.

Which demonstrates that the LLCC modified active clamped fly-back can generate almost 50% more voltage than the standard proposed converter with the same rectifier load network.

This is most likely due to the reduced impedance of the transformer respective to the parallel transformer capacitance and the creation of an additional higher frequency resonance. These, combined, create additional circulating current to increase the diode conduction angle, and additional voltage gain capability that increases the voltage at which diode conduction occurs:

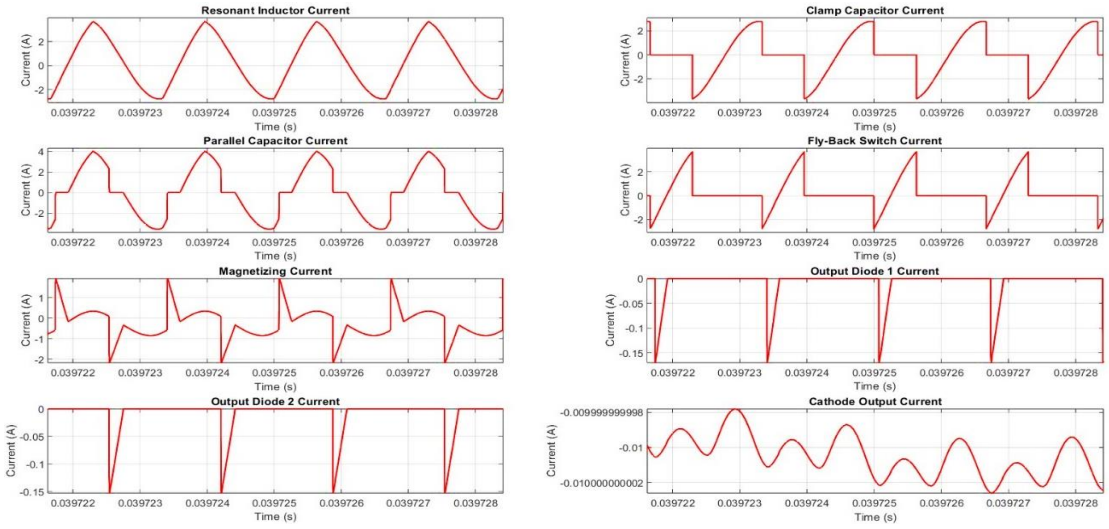

Fig.50: Full-Load Modified LLCC Resonant Fly-back Converter Current Waveforms with 243VDC Input Voltage at a Switching Frequency of 600kHz and 35% Duty Cycle.

The above steady state simulated results give a good indication of the changed converter characteristics at full-loading level. A clear increase in the current, specifically during the series-parallel stage, is evident. Observing the above figure, one can notice one distinct difference between the modified fly-back design and that which has been previously proposed. The magnetizing current and the parallel capacitor have a clear, additional resonance between them that does not involve the resonant inductor nor the clamp capacitor. A sinusoidal current oscillates within this third parallel tank, and thus the peak current within the parallel capacitor increases beyond that of both the resonant inductor and clamp capacitor. The total parallel capacitor current can, therefore, be seen to be equal to the sum of that flowing within the series resonant inductor and the additional sinusoidal variation due to the parallel resonance. This would suggest that this parallel resonance exists in both the series-parallel and PRC stages.

Due to the substantially reduced magnetizing inductance, the converter also displays enhanced transient response through an elevated achievable controller bandwidth. This is most likely due to the frequency of the RHPZ of the fly-back converter shifting to a substantially higher frequency.

If the new resonance created through the reduced magnetizing inductance and the parallel capacitance are still substantially lower than the switching frequency, fixed-frequency duty cycle control can still be maintained. The below figure provides a comparison between asymmetrical duty-cycle control of the two novel resonant fly-back converters at nominal line voltage of 270VDC:

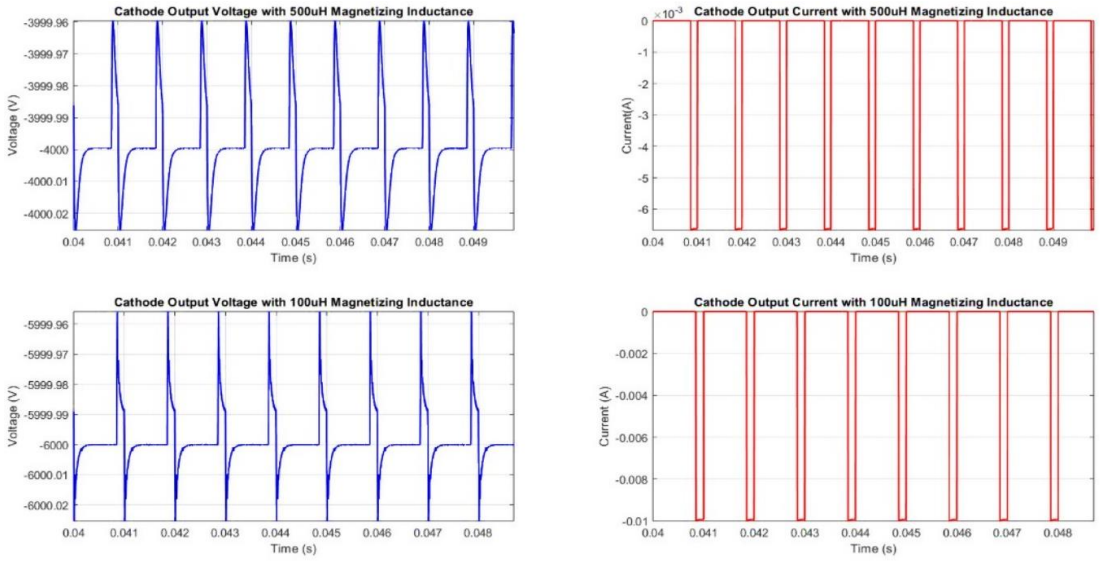

Fig.51: Transient Performance comparison of the Fixed-Frequency Active-Clamp Multi-Resonant Converter with Decreased Magnetizing Inductance.

In the LLCC resonant converter, almost equal voltage deviations during transient events have been achieved for a higher substantially higher output current. The output capacitance was kept constant across both simulations. This is indicative of a superior transient performance in the lower magnetizing inductance case, especially considering the reduced magnetizing inductance also creates a higher first resonant frequency within the output second-stage filter. The increased current during the new LLCC stage does create larger ripple currents and voltages within the clamp capacitor, but since only the peak value is of concern regarding output voltage generation during this stage, it is not of concern. Additional clamp capacitance may be inserted if desired, at the expense of output voltage attenuation due to a larger capacitor ratio. Increases in fly-back duty cycle may compensate, as may slight reductions in normalised switching frequency through the multiple avenues that have been explored here.

Such topological modifications indicate that frequency limitations explored within this work can be overcome despite the significant transformer capacitance which exist in high-voltage designs. Further work needs to be performed on the analysis of this topology and to provide mathematical expressions for the converter characteristics to fully understand the phenomena described above.

4.3 PROPOSED HYBRID CONTROLLER SCHEME

4.4 SUMMARY

The above steady state and transient performance simulations give a good indication of the converter performance across differing line and loading conditions. Within the collector regulator, the simulation results are in good agreement with the proposed design methodology. To minimize collector voltage deviation and minimize the effects of operating close to the full-load resonant peak, the PRF information can be utilized to modulate the switching on and off during transient events, leading to an effective bandwidth that is greater than would be otherwise achievable with standard VMC, which exhibits significant unpredictable and oscillatory behaviour during unloading.

The cathode EPC simulation results also agree very well with the novel proposed design methodology in the previous chapter. Significant gain was achievable at full-load due to an increase in the resonant tank input voltage that is achievable with the active-clamped bride configuration. This enabled high voltages to be achieved while operating substantially above all nonlinear resonant peaks of the two states, such that fixed frequency duty cycle control could be achieved to allow optimization of transmitter phase-noise performance. Due to the low required conduction angle to generate a given output voltage, small variations in fly-back duty cycle enabled rapid response to changing load under all implemented PRFs commonly utilized in airborne ECM/ECW applications. To compensate for increased gain in the series-parallel converter during unloading, substantially attenuation within the effective tank input voltage is achieved through increases in clamp transistor duty cycle. Finally, it was shown that reducing the magnetizing inductance of the two-state resonant fly-back created a second, novel power topology with superior gain due to increased magnetizing current enabling the use of higher conduction angles for a constant load rectifier network. This also enabled enhanced transient response characteristics due to an increased converter bandwidth.

The described technique of utilizing two separate power converters has shown to be effective in the provisioning of power for the two most important electrodes within the MPM during simulation and has benefits regarding thermal system requirements. A substantial reduction in cathode voltage AC voltage variation has been achieved without the requirement for switching the collector regulator, in which most of the current is consumed, at high frequencies. As a result, the impact on the heat-sinking system, which typically constitutes most of the system weight and size, can be minimized. To optimize efficiency of the actual TWT amplifier, specialised regulation techniques within the collector were proposed, which are simple and effective while not influencing the cathode regulator.

The use of wide band-gap devices further enhanced the thermal characteristics of the system, through minimizing switching loss and reducing the required heat-sink requirements for the individual switching devices. Since the collector regulator will switch at lower frequencies and therefore have a more significant contribution in total dissipation due to conduction loss, it may be worthwhile to investigate semiconductor device optimization. For example, the use of SiC MOSFET devices, which exhibit substantially lower on-state drain-source resistance at the expense of higher gate-source capacitance, may allow further thermal enhancements.

5 EXPERIMENTAL SET-UP, RESULTS, AND DISCUSSION

5.1 EXPERIMENTAL SETUP

Due to the high voltage nature of the project, the experimental set-up visible in Fig.52 consists of three mechanically and electrically isolated Perspex boxes. Each contains an important part of the system:

- 300VDC power supply and hybrid switching inverters.
- Isolation transformer, high voltage rectifier, equivalent resistive load, and load switch.
- Low voltage electronics: Low voltage auxiliary power supplies, DSP board, and safety electronics.

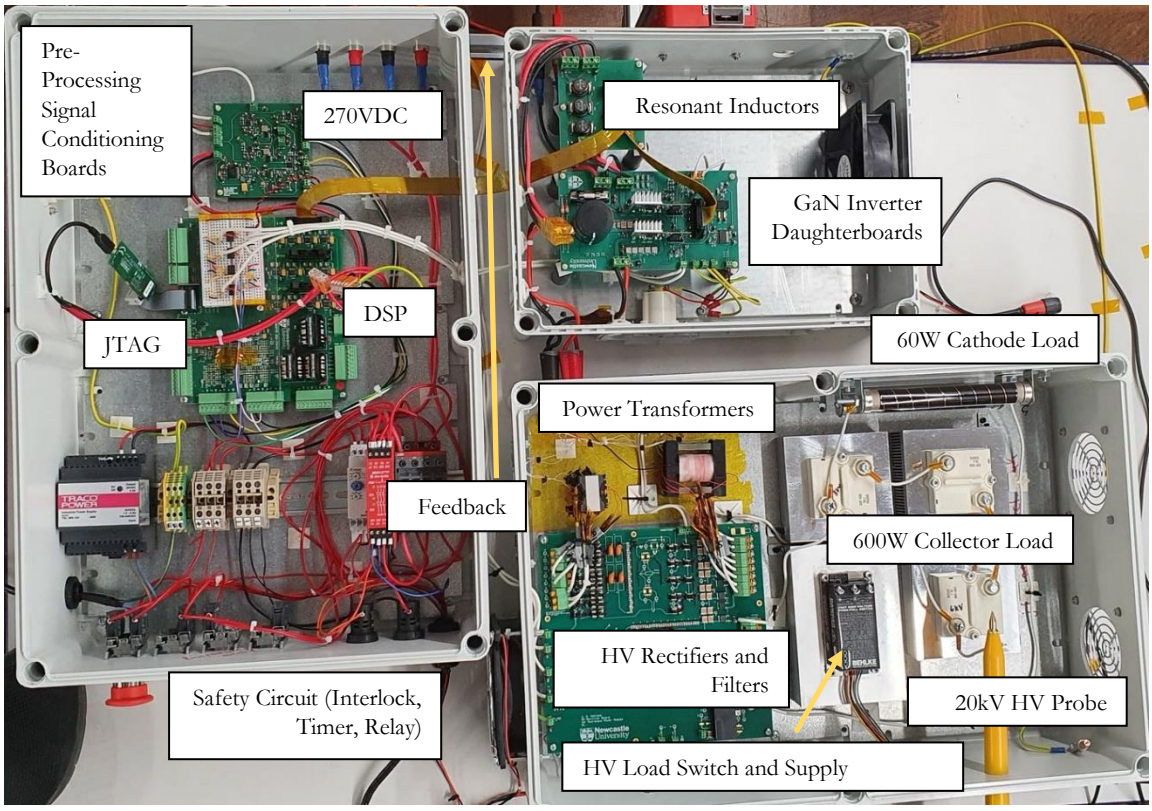

Fig.52: Experimental Test Rig Set-up Including Power Circuit and Digital Control Platform.

All boxes are electrically isolated to reinforced levels, with both transformers tested to have minimum leakage current at voltages of -8kV. The output feedback chain consists of a fail-safe series-parallel combination of resistors and capacitors. The maximum voltage for the cathode has been limited to -4kV such that safety can be guaranteed for the operator. The full equipment list is below:

- Input Power Supply: 300V/10A 3kW by Euro Test.
- Inverter: LMG3410-HB-EVM Evaluation Module, Texas Instruments. Integrated gate driver, 1MHz, 600V/12A, 70mΩ. Fully latching over-current and over-temperature protection. Auxiliary under-voltage lockout. Half-bridge configuration.
- Oscilloscope: Tektronix MSO 4034 Mixed Signal Oscilloscope, 350MHz, 4+16-channels, 2.5GS/s sample rate, 8-bit vertical resolution.
- Auxiliary Supply: EL302RT Triple Power Supply by Aim TT Instruments, 30V/2A.
- Passive Probes: Tektronix P6139B, 500MHz, 300V. Testec TT-HV-151, 200MHz, 1500V.
- High Voltage Differential Probe: Tektronix TMDP0200, 200MHz, +/-750V Common Mode Voltage.
- High Voltage Stacked MOSFET Switch: Behlke HTS 61-01-HB-C, 6000V, 15A, 100kHz maximum switching frequency.

Further power density optimizations may be achieved by replacing the lower current cathode regulator transistors with integrated solutions exhibiting higher drain-source on-state resistance, such as the LMG321xR150, which has substantially less output capacitance. The substantial reduction in output capacitance with the LMG312xR150 can, on the other hand, enable faster discharge of the drain-source voltages in the cathode regulator to meet soft-switching timing conditions more easily at elevated switching frequencies [118, 119]. This would also partially mitigate the effects of output capacitance variation with applied DC voltage, which varies dynamically as the switched node voltage is changed. The collector regulator, which processes more power, should instead be optimized for efficiency and lower switching frequency which would suggest the use of low on-state resistance switches with higher output capacitance levels which can easily be accommodate within the series-parallel switching topology. Both solutions, however, are limited to a maximum switching frequency of 1MHz due to thermal limitations of the integrated package.

5.2 SERIES-PARALLEL RESONANT COLLECTOR REGULATOR RESULTS

The first set of results presented will be concerning the collector regulator, which is intended to be optimized for enhanced efficiency and a lower transistor switching frequency. The actual measured and implemented tank resonant components are shown Table 3 below:

Series-Parallel Resonant Collector Components	Value
External Inductance	37uH
Measured Transformer Leakage Inductance	1uH
Series Resonant Capacitor	28nF
Total Referred Parallel Capacitance	2nF
Magnetizing Inductance	500uH
Transformer Turns Ratio	0.05
Load Resistance	14.3kΩ

Table 3: Practically Implemented Passive Components for Collector EPC.

Fig.53 demonstrates the MOSFET drain-source and split-resonant capacitor voltages with an input voltage of 297VDC, which allowed generation of a collector electrode voltage of approximately -2.5kVDC at a switching frequency of 220kHz:

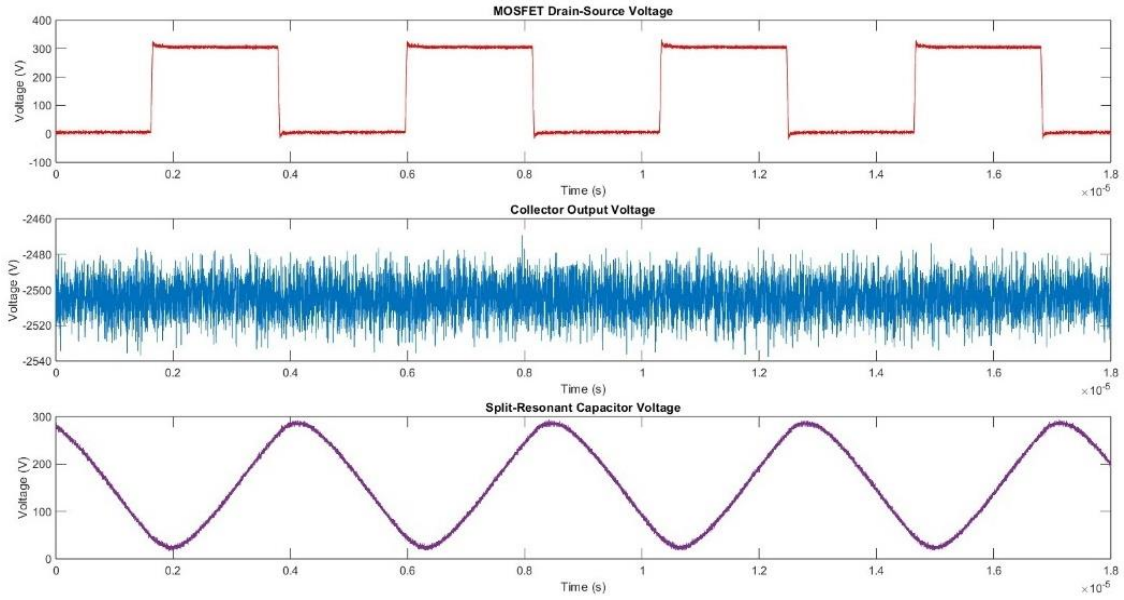

Fig.53: MOSFET Drain-Source and Split-Resonant Capacitor Switching Voltages with 297VDC Line Voltage.

There are two issues that caused discrepancies between the implemented practical resonant components and those intended to be used from the theory:

1. Transformer capacitance: Capacitance was measured to be a value substantially less than the required 18nF given in the design procedure. The total referred capacitance, measured with all transformer secondaries shorted, was only ~2nF. This was due to the use of an oversized core which allowed additional separation between the primary and secondary windings. The voltage potentials present between the primary and secondary windings is also half that of the fly-back transformer, which also results in a lower transformer capacitance. As was detailed previously, a small transformer capacitance causes the series-parallel converter to mimic a series converter more closely, which has reduced gain capability and degraded frequency selectivity. To improve the converter, high-class quality C0G capacitors should be inserted into each secondary winding to increase the referred capacitance and partition the current within them. Refer to Appendix B for an in-depth discussion regarding transformer design, including temperature effects, core loss, winding loss, and how geometry considerably affects the transformer parasitic values.

2. Resonant inductor tolerance: Due to the high inductance value required, external inductors were an essential inclusion in the resonant tank without complicated leakage inductance integration methods such as utilization of a magnetic shunt. The high voltage unshielded inductors displayed tolerances of +/-20% and blocking voltages of 500V. Inserting larger value resonant inductances will reduce the effective tank resonant frequency and allow generation of the necessary voltage at frequencies more suitable for the implemented ferromagnetic core. The level of leakage inductance present within the high-power transformer was also substantially less than was expected and did not substantially change when a core gap was implemented. However, if a higher switching frequency is acceptable, simply inserting the additional ~16nF parallel capacity can bring the converter within specification at low-line voltages and maximum load. This should be incorporated on the secondary side of the transformer and equally distributed across all four secondary windings to minimize power loss.

Despite the incorrect resonant tank values, the split-resonant capacitor voltage is a clean sinusoid, which indicates above resonance operation and good switching characteristics. The MOSFET switch voltage is also a clean switching waveform, with a peak drain-source stress of approximately 310VDC.

The resonant current was measured with a current transformer feeding a full-bridge diode rectifier, an averaging circuit, and a low-pass filter to remove any high frequency noise from the switching circuits for implementation of peak current limiting. The average resonant current is illustrated below in Fig.54:

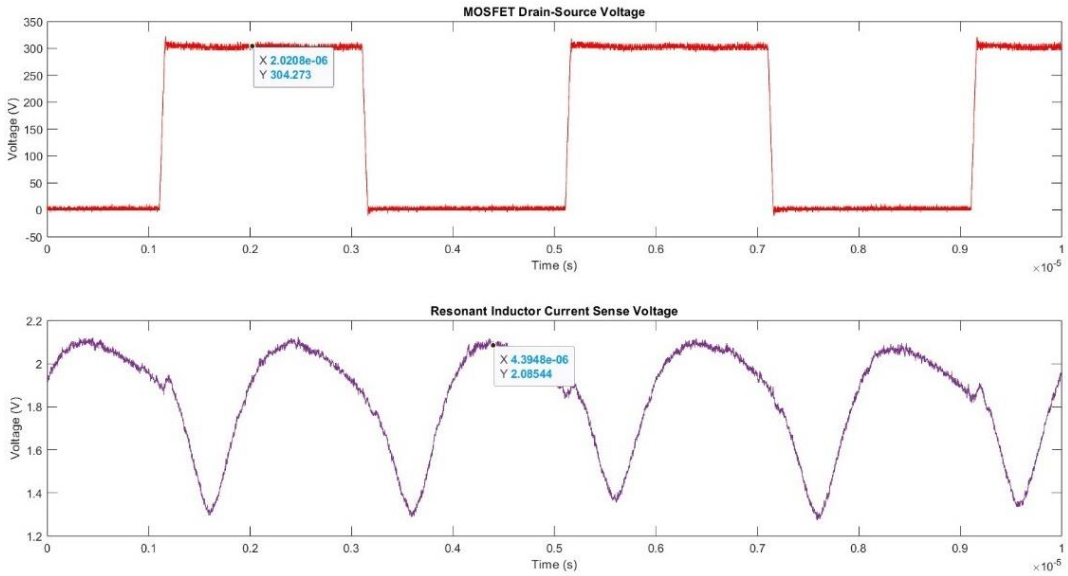

Fig.54: MOSFET Drain-Source Voltage and Series Resonant Inductor Current with 297VDC Line Voltage.

A 1:100 current sense transformer and a voltage sense resistor of 30Ω was incorporated to produce a 3V fault voltage at a peak tank current of 10A. The peak value of the sense voltage is approximately 2.08544V, which corresponds to a primary-side current of approximately 6.95A. The RMS current is approximately 4.92Arms. This is slightly higher than is present in an equivalent simulation of the circuit with the actual measured values incorporated within the EPC (~5.9A peak current).

This may be most likely attributed to converter inefficiencies which are not fully modelled in simulations such as the transformer core and high frequency AC winding losses. Despite the increased circulating current within the primary side, the total converter efficiency is still impressive. The switching frequency of 220kHz allows generation of approximately -2kVDC at low-line and full-loading to preserve a 50% depression ratio between the collector and cathode for optimum tube efficiency. The efficiency of the collector EPC operating in open loop across differing line voltage conditions is summarized in Table 4.

Insertion of additional parallel capacity remains essential to minimize the frequency bandwidth for no-load regulation. The increased gain can be compensated by increasing the series resonant inductance to 49uH through insertion of additional external inductance accounting for large component tolerances. Switching frequency may also be decreased to levels where efficiency would be higher due to reduced transformer losses specifically. It is not desired to raise the switching frequency at full-loading level for the same reasons as described, since the transformer was initially optimized for a frequency of approximately 180kHz.

Line Input Voltage (V)	*Collector Output Voltage (kV)*	*Input Current (A)*	*Output Current (A)*	*Input Power (W)*	*Output Power (W)*	*Efficiency (%)*
243	-2.01	1.21A	0.1392	294.03	279.79	95.16
270	-2.24	1.34A	0.1543	361.80	345.60	95.52
297	-2.490	1.53A	0.1741	454.41	433.51	95.40

Table 4: Collector EPC Efficiency Measurements at Different Line Voltages for Full-Load.

The EPC for the collector regulator achieves a maximum efficiency of 95.16% at minimum line voltage and full-loading level, dissipating only 14.24W during the tests. The efficiency increases in open loop with increase line voltage since the level of output power increase exceeds the additional level of power dissipation at the new operating point.

5.3 MULTI-RESONANT CATHODE REGULATOR RESULTS

The maximum voltage produced by the cathode was limited to -4kVDC. To model the full-load power, high voltage, 45kV resistors of total value 248.1kΩ were used. The cathode regulator was originally designed to be a standard ACF converter without any substantial transformer capacitance such that the SRF was low enough to enable high frequency switching of approximately 1MHz. However, during initial testing, substantial parallel resonant behaviour was observed which produced a large voltage gain at low input voltages and duty cycles. As a direct result, the full output voltage was achieved with a switching frequency of 602kHz and a duty cycle of just 22.4%. The fly-back MOSFET drain-source voltage under these conditions, visible in Fig.55, is approximately 167VDC. The first observation can be made within the rise and fall times of the WBG MOSFET. Full discharge of the drain-source voltage occurs in just 74.4nS with a 6uH inductor – substantially lower than would be expected in standard ACF theory.

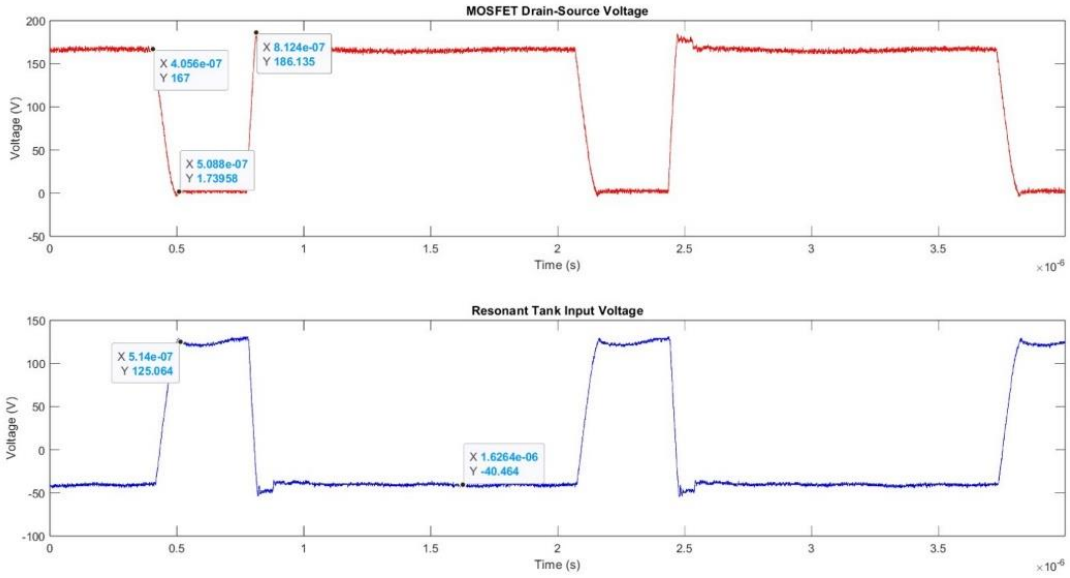

Fig.55: Drain-Source and Resonant Tank Input Voltages of the Multi-Resonant Fly-back.

This supports the argument that the parasitic transformer capacitance should not necessarily be considered lumped with the MOSFET output capacitances, particularly at high frequency where this would typically present the most severe issue when attempting to achieve soft switching. The equations commonly presented in literature, therefore, are not accurate in this case. Despite the above, the design procedure presented in Chapter 3 can still be validated, but some important changes are observed when the converter operates at frequencies below the parallel resonances of the series-parallel and parallel states. The implemented component values utilized within the ACF converter are summarized in Table 5 below:

Standard Active-Clamp Fly-Back Components	Value
External Inductance	3.7uH
Measured Transformer Leakage Inductance	2.2uH
Clamp Capacitance	20nF
Total Referred Parallel Capacitance	4nF
Magnetizing Inductance	500uH
Transformer Turns Ratio	0.03406

Table 5: Implemented Standard Active-Clamp Fly-Back Component Selection.

Given the maximum duty cycle of 22.4%, switching frequency of 602kHz, and output load resistance of 248.1kΩ, the following diode conduction angles are theoretically produced:

$$\Pi_L = 0.560 \qquad \Pi_P = 0.162$$

$$\theta_L = 73.62° \qquad \theta_P = 43.85°$$

This creates the following voltage attenuation coefficients and equivalent load resistances considering finite charge and discharge times and capacitive output filtering effects:

$$k_{v_L} = 1.162 \qquad k_{v_P} = 1.101$$

$$R_{eq_L} = 194\Omega \qquad R_{eq_P} = 174\Omega$$

The phase-angle between the transformer voltages and currents in each state and the equivalent capacitances are then calculated:

$$\beta_L = -23.99° \qquad \beta_P = -17.32°$$

$$C_{eq_L} = 605pF \qquad C_{eq_P} = 473pF$$

From (Fig.55), one can observe that the RMS value of the tank input voltage is approximately -41VDC. With a 125VDC line voltage, this would result in an effective RMS tank input voltage according to the presented theory of:

$$\widehat{V_{T_r}} = \sqrt{V_{DC}^2(D) + \widehat{V_{CL_r}}^2(D')} = 69.31V$$

The AC voltage gain coefficients are calculated for the series-parallel and parallel states, respectively:

$$k_l = 1.196 \qquad k_p = 1.588$$

These voltage gains, theoretically, should produce voltages during each state of approximately:

$$\frac{k_l \widehat{V_{T_r}}}{k_{v_L} N_F} = -2094.5V \qquad \frac{k_p \widehat{V_{T_r}}}{k_{v_P} N_F} = -2935.0V$$

Which results in an average imposed cathode voltage of just -2.549kVDC. However, in practice, the EPC does indeed produce -4kVDC within the cathode electrode of the TWT. The generated output voltage and MOSFET drain-source voltage at the given input voltage is illustrated in Fig.56:

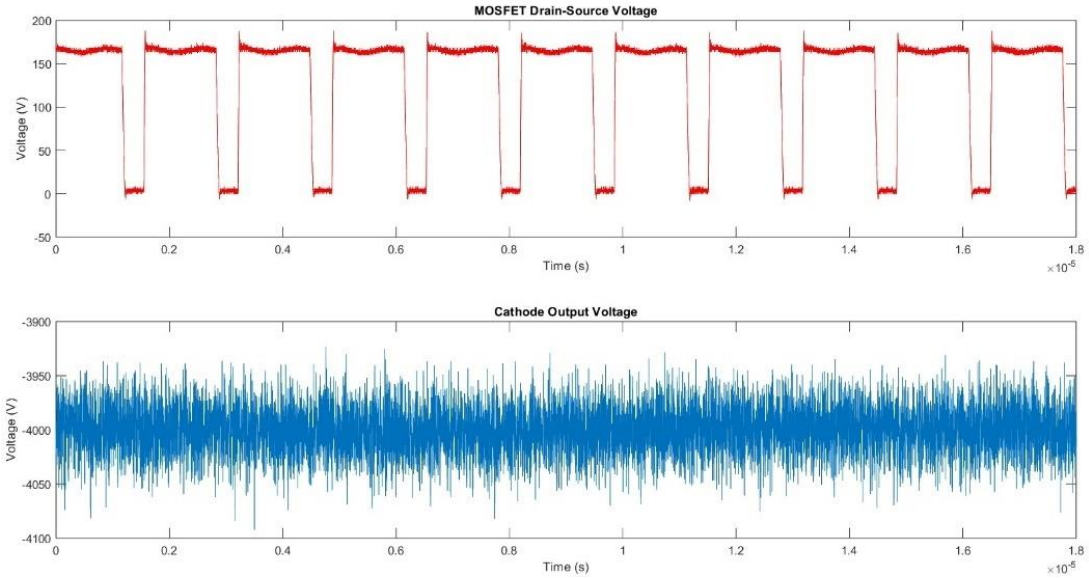

Fig.56: -4kVDC Cathode Output Voltage at 602kHz Switching Frequency at 22.4% Duty.

The discrepancy can be explained due to the behaviour of the resonant inductor which exhibits significant oscillatory behaviour during operation below resonance. The oscillatory behaviour in the resonant inductor, transformer, and output diodes occurs irrespective of whether there is a substantially fixed clamp voltage or whether it also exhibits AC voltage variations. Although most of the equations remain valid, one is of utmost importance, reiterated now for clarity:

$$V_{CL_{PK}} = N_F V_{O_P} + \frac{2L_{R_F} F_{S_F} P_{O_F}}{\alpha V_{DC} D_F (D_F')}$$

The term on the right-hand side of the above equation essentially relates to the voltage imposed on the resonant inductance in a standard ACF converter, which is essential for regulation across differing line and loading conditions. Let us rewrite the above equation as follows, expressed as a function of the voltages developed in each state and the resonant inductor/transformer voltages within them:

$$N_F V_{O_L} = V_{CL_{PK}} - V_{L_{R_L}} \quad (5.01a) \qquad N_F V_{O_P} = V_{DC} - V_{L_{R_P}} \quad (5.01b)$$

As a result, if the voltage imposed on the inductor oscillates along with the output diodes and transformers, the effective tank RMS value may become variable, which invalidates the given design procedure. It is therefore proposed that the provided analysis in Chapter 3 be constrained to fixed-frequency converters operating substantially above the highest parallel resonant peak. Expanding on these equations, consider:

$$N_F V_{O_L} = k_l \frac{\widehat{V_{T_R}}}{k_{v_L}} = V_{CL_{PK}} - V_{L_{R_L}} \quad (5.02a) \qquad N_F V_{O_P} = k_p \frac{\widehat{V_{T_R}}}{k_{v_P}} = V_{DC} - V_{L_{R_P}} \quad (5.02b)$$

The resonant inductor voltage is therefore found:

$$V_{L_{R_L}} = V_{CL_{PK}} - k_l \frac{\widehat{V_{T_R}}}{k_{v_L}} \quad (5.03a) \qquad V_{L_{R_P}} = V_{DC} - k_p \frac{\widehat{V_{T_R}}}{k_{v_P}} \quad (5.03b)$$

Which demonstrates the converter's ability to generate substantial output voltages despite a low effective tank RMS voltage due to an oscillating inductor voltage. Measurement of the inductor voltage in practice is needed to further validate the above without relying on simulation results and presents one drawback of this research. This theory is further validated, however, by the presence of oscillatory in both the transformer and output diode converter waveforms. Fig.57 below illustrates the series-parallel output diode voltage oscillating at the parallel resonant frequency of the parallel converter state:

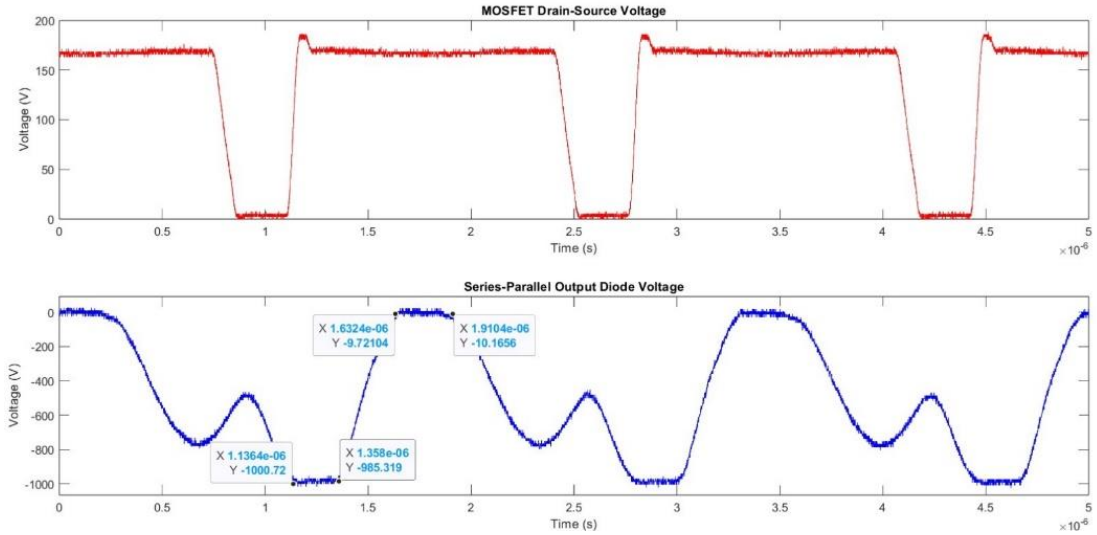

Fig.57: 1MHz Oscillating Series-Parallel Output Diode Voltage at 602kHz with 125VDC Line Voltage Indicating Diode Conduction Times during each state.

To demonstrate that this occurs irrespective of the AC voltage variation that is present on the clamp capacitor, a simulation result in Fig.58 shows the simulation model with a clamp capacitor implementation of 500nF to present a substantially fixed DC source during clamp switch turn-on. The resonant inductance is reduced to compensate for the gain attenuation that occurs during the series-parallel state. This also creates a slight reduction in the clamp voltage to approximately 35V.

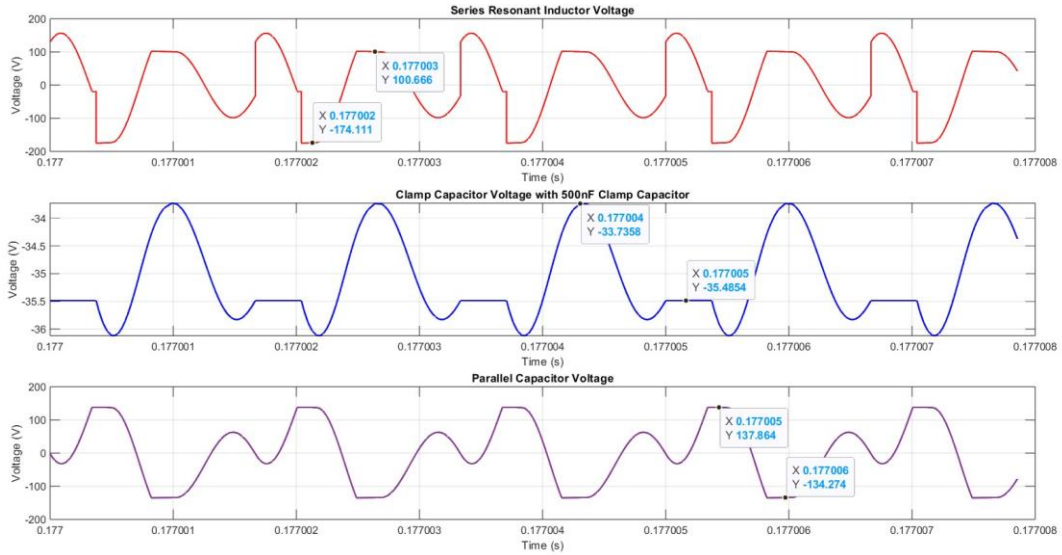

Fig.58: Relationship between Resonant Inductor, Clamp and Parallel Capacitor Voltages during Sub-Resonance Operation.

In this case, one can observe that the peak clamping voltages of the transformers are substantially higher than predicted by the novel design procedure due to an oscillating voltage on the series resonant inductor. The inductor voltage is a function of the peak and RMS tank input voltages, as well as the voltage gain coefficients of the circuit.

The inductor, clamp, and parallel capacitor voltages all oscillate at the same frequency, referred to as the sub-resonance oscillation frequency $F_{C_{L_{osc}}}$, which is related to the parallel resonant frequency of the series-parallel converter state, calculated below:

$$F_{C_{L_{osc}}} = \frac{1}{2\pi\sqrt{\frac{L_{R_F} C_{CL} C_{P_F}}{C_{CL} + C_{P_F}}}} \cong 1.1MHz$$

The transformer voltages in simulations are approximately 137.9V during the parallel state and -134.3V during the series-parallel state. According to the implemented angular switching frequency, these generate:

$$V_{O_L} = 3943.05V \qquad V_{O_P} = 4048.74V \qquad V_{O_F} = 3995.9V$$

Working backwards, we can deduce that:

$$\widehat{V_{T_{r_L}}} = \frac{V_{O_L} k_{v_L} N_F}{k_l} = 130.5V \qquad \widehat{V_{T_{r_P}}} = \frac{V_{O_P} k_{v_P} N_F}{k_p} = 95.6V$$

Which suggests that the oscillating inductor and clamp voltage present an unstable, varying voltage source when operating below resonance despite operating at fixed switching frequencies and duty-cycles; particularly of concern during the parallel converter state where a substantial amount of attenuation exists. It seems that the ACF converter tends to balance the transformer voltages somewhat automatically through modulation of the series resonant inductor voltage. For now, we may instead use the series resonant inductor current to assess the accuracy of the rest of the design procedure. First, observe the series resonant inductor current in Fig.59 below:

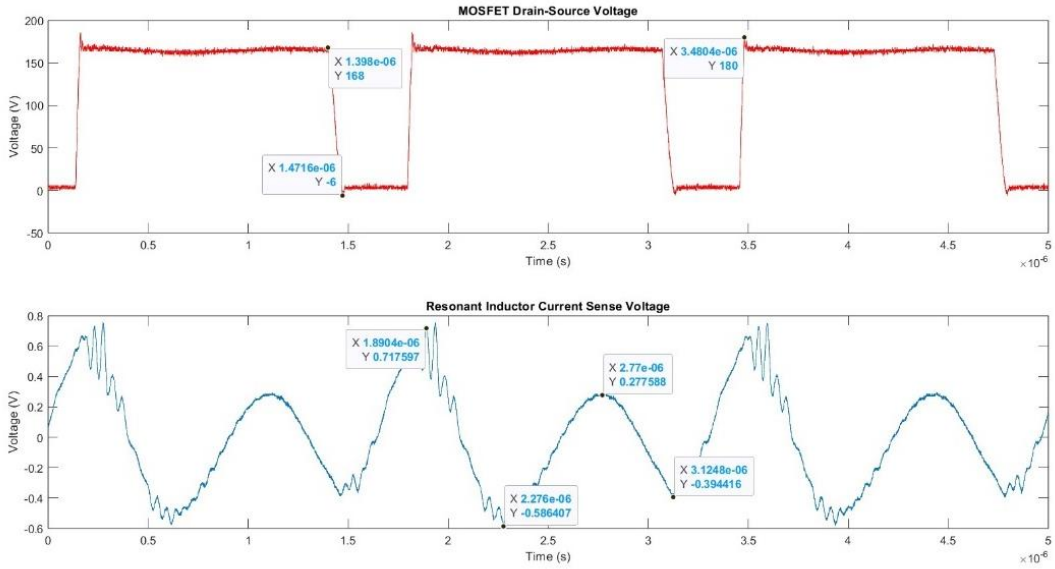

Fig.59: Series Resonant Inductor Current Sense within Multi-Resonant ACF Converter.

The current oscillates at the same frequency as the voltage waveforms (~1.1MHz). First, this leads one to believe that there may be measurement errors within the clamp and drain-source voltages since only very small ripple voltages are produced with a 20nF capacitor despite the magnitude of current flowing through it. The current is measured in practice through utilization of a 1:100 current sense transformer and a 17R resistance to generate a ~1V fault voltage at an intended peak primary current of 6A. A smaller resistance and sense voltage was essential to avoid impedance reflections when sensing lower magnitude high frequency currents, which is incredibly difficult to do accurately – particularly within a high voltage EPC. Although there is switching noise imposed on the sensed voltage waveform, the negative peak current occurs during the series-parallel state and has a magnitude of -0.5864V – corresponding to a peak current of approximately -3.52A.

The peak current during the parallel state is slightly higher, with a voltage sense of 0.7176V corresponding to a peak current of 4.31A. The actual diode conduction times are taken from the series-parallel output diode voltage waveform, through which we can calculate the diode conduction angles utilizing the output diode conduction times during the series-parallel δ_L and parallel δ_P respective to their respective angular switching frequencies, below:

$$\theta_L = \frac{180\delta_L\omega_{S_F}}{\pi} = 60.25° \quad (5.04a) \qquad \theta_P = \frac{180\delta_P\omega_{S_F}}{\pi} = 48.03° \quad (5.04b)$$

Which agree well with the proposed method for calculating duty-cycle effects of diode conduction angles. Due to oscilloscope quantization noise in the produced signals, the actual conduction times may differ slightly from the above. It should also be noted that dead-time was implemented in the digital controller, but only used the clamp gate drive voltage as an input which reduces the effective duty cycle of the series-parallel stage to avoid introducing duty-cycle loss within the ACF. The generated voltages in each state can be readily calculated utilizing the peak series resonant inductor currents and their relationship to the average cathode load current:

$$I_{o_L} = \frac{2N_F}{\pi} I_{L_{R_L}} \sin^2\left(\frac{\theta_L}{2}\right) = 16.79mA \qquad I_{o_P} = \frac{2N_F}{\pi} I_{L_{R_P}} \sin^2\left(\frac{\theta_P}{2}\right) = 15.48mA$$

$$I_{O_F} = \frac{I_{O_L} + I_{O_P}}{2} = 16.13mA \quad (5.05)$$

$$V_{O_F} = R_{O_F} I_{O_F} = 4003.1V \quad V_{O_P} = R_{O_F} I_{O_P} = 3840.6V \quad V_{O_L} = R_{O_F} I_{O_L} = 4165.6V$$

Where $I_{L_{R_L}}$ and $I_{L_{R_P}}$ are the peak currents within the resonant inductor L_{R_P} during the series-parallel and parallel states, respectively. This, however, assumes that the magnitude of the peak current in the resonant inductor during each state is equal to that within the magnetizing inductance. It is possible, particularly when operating sub-resonance, that this will not be the case as high frequency oscillations within the clamp current may oscillate below the peak resonant inductor current before the output diode during the series-parallel state begins to conduct current. This may also occur during the parallel state, but to a much less severe degree. A novel equation is given below to estimate the actual peak magnetizing current when operating sub-resonance, considering the clamp oscillation frequency and peak series resonant inductor current. This is referred to as the adjusted magnetizing current due to sub-resonance, $\ddot{I}_{L_{M_L}}$:

$$\ddot{I}_{L_{M_L}} = I_{L_{R_L}}\left(\frac{\pi D_F'}{T_{C_{L_{osc}}}\omega_{S_F}}\right) \quad (5.06)$$

Where $T_{C_{L_{osc}}}$ is the clamp oscillation period. To enhance the accuracy of the results, it is suggested as further work to enable measurement of the magnetizing and output diode currents within each state to verify the above proposal. A simulation, observed in Fig.60, is performed within SPICE to demonstrate this effect when the clamp current oscillates at above 1.1MHz and shows good agreement with equation (5.06):

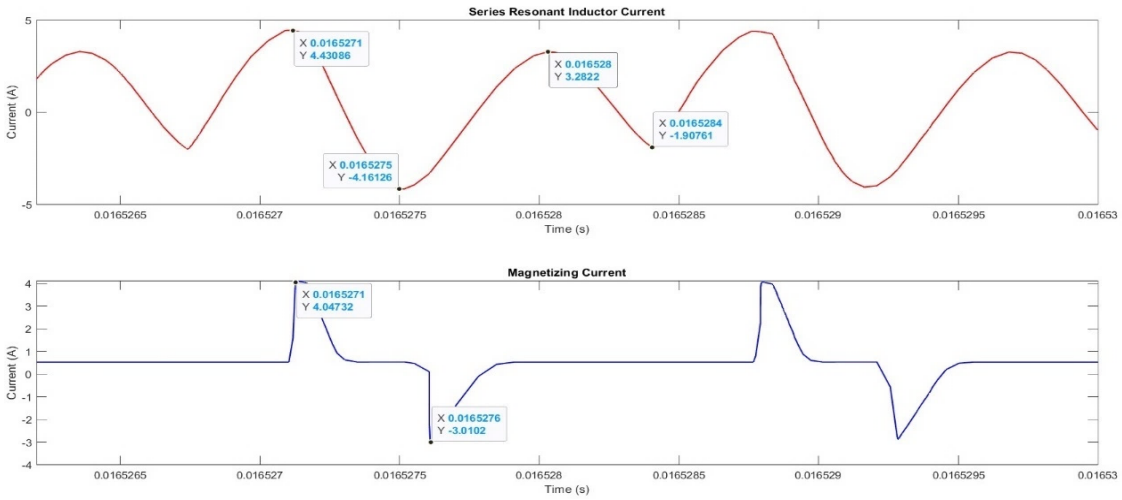

Fig.60: Current-Sharing Relationship between Series Resonant and Magnetizing Inductances.

The analysis presented here does seem to show relatively good agreement with the given theory, however it should be noted that operation below resonance invalidates the design procedure given in Chapter 3 impedes voltage gain capability through two mechanisms:

- High-frequency oscillatory voltage waveforms: the series resonant inductor, clamp voltage, and output diode all exhibit high frequency oscillatory behaviour that reduces the effective RMS tank input voltage, attenuating the achievable peak parallel capacitor voltages within each state.

- High-frequency oscillatory current waveforms: the clamp current oscillates at the series-parallel resonant frequency. This causes the magnetizing current to be substantially lower than the peak magnitude since output diode conduction occurs at the switching frequency. This may further reduce the series-parallel voltage gain that would be achievable according to theory when operating above resonance.

However, this bodes well for high frequency switching within an MPM EPC, since the actual switching frequency must be substantially high to avoid these issues, rather than substantially low in hard-switched fly-back and standard ACF converters.

One can therefore accommodate larger parallel capacities for a selected output voltage while operating at higher normalised frequencies. This is only true within the hybrid EPC where the high load resistance creates a large quality factor.

The drawback of such an approach is component tolerance, where slight variances in passive components values may cause large differences in AC voltage transfer gains. The magnitude of the transformer waveforms will be impacted by the reduced diode conduction times, with new equivalent resistances and capacitances needing to be calculated to fully examine how this behaviour impacts the achievable output voltage. It is recommended that operation of the multi-resonant ACF is strictly limited to operation within the above resonance case such that the simplified design procedure presented in Chapter 3 can be utilized and the converter is presented with a non-oscillatory voltage source. This can be achieved through insertion of higher series resonant inductance, reducing the effective resonant frequency of the tank, and removing all oscillations.

This oscillatory behaviour poses the biggest concern regarding the accuracy of the results. Despite the resonant inductor current clearly having oscillatory behaviour during clamp turn-on, a corresponding voltage ripple is not produced within the 20nF C0G capacitors or on the fly-back switch. It is therefore difficult to fully confirm the proposed theory for operation below resonance, however the values that were measured do seem to show good alignment with the theory and production of an average cathode output voltage of -4kV. Some discrepancies exist within the currents in simulation and those observed in practice, possibly due to the issue with component tolerance. Although all tested with an FRA, it may be difficult to measure the total impedance when in-circuit. There may be a substantially higher parasitic capacitance than was used within the calculations and the simulations due to parasitic capacitance variations with applied voltage that is naturally exhibited within the transformer and output diodes. This feature also affects one's ability to achieve soft switching, since MOSFETs and WBG diodes have output capacitance values that dynamically change with the applied DC voltage, resulting in a capacitance that is effectively variable with time.

Although any increased parasitic capacitance may slightly change the characteristics of the EPC, it is believed that the proposed design process for both sub-resonance and above resonance operation provides a good first-pass estimation of a working design. The actual developed voltage tends to be slightly higher than would be indicated by the diode voltage waveforms, since they do not completely stop conducting current when the capacitor starts to charge back to the output voltage of a given state. Complete accuracy therefore demands measurement of the actual conduction current, rather than the voltage waveforms.

It is believed that the results have shown the effectiveness of the EPCs ability to accurately regulate the output voltage through modulation the average voltage and current imposed on each capacitor within a full-wave voltage doubler circuit through implementation of asymmetrical duty cycle control of a two-state, multi-resonant ACF converter. A further drawback of this technique is the presence of DC current within the transformer. This requires a larger core than would usually be implemented to ensure the core does not saturate. Despite the drawbacks of the converter, the efficiency of the multi-resonant ACF when operating at sub-resonance, reached ~87% at a switching frequency of 602kHz – delivering 64.38W.

The overall converter efficiency is therefore ~93% with a constant depression ratio of 50% when operating with cathode and collector electrode voltages of -4kV and -2kV, respectively.

5.4 NOISE SUSCEPTIBILITY AND CLOSED-LOOP CONTROL ISSUES

The ability to form a closed-loop controller and accurately measure voltage ripple imposed on the cathode and collector electrodes was significantly impeded by the presence of large amounts of high frequency noise. This section will present the original results and methods used to mitigate them, alongside a discussion of how they may affect the characteristics of the loop and achievable bandwidth. For a complete background on noise susceptibility and how this affects high impedance feedback paths and high switching frequency power transmission networks, please refer to Appendix C. The first important consideration is the net impedance of the resonant tank states. At the fixed angular switching frequency, the relationships below are created between the passive components:

$$X_{L_{R_F}} = \omega_{S_F} L_{R_F} = 22.7\Omega \quad X_{C_{CL}} = \frac{1}{\omega_{S_F} C_{CL}} = 13.2\Omega \quad X_{C_{P_F}} = \frac{1}{\omega_{S_F} C_{P_F}} = 66.1\Omega \quad X_{C_{P_F}//C_{CL}} = \frac{1}{\frac{\omega_{S_F} C_{P_F} C_{C_L}}{C_{P_F} + C_{C_L}}} = 79.3\Omega$$

During the parallel switching state specifically, the tank becomes net capacitive. The effect of this is clear within the presented current waveforms in the previous section. Capacitive mode tank operation should be avoided under all circumstances and may cause substantial amounts of high frequency noise to transfer across the transformer and into the sensitive cathode electrode. To mitigate this, a transformer Faraday shield was implemented, but offered little benefit. The issue is especially amplified if not enough dead time is included between switching transitions to allow complete discharge of the MOSFET output capacitances. The first result in this section, given in Fig.61, shows the cathode voltage feedback signal that exist prior to a fast slew-rate voltage buffering operational amplifier with a 50MHz bandwidth.

This is followed by a second high-bandwidth operational amplifier, which serves to both invert and scale the high potential, negative cathode voltage, and provide a low-impedance output to enable effective driving of a successive approximation Analogue-to-Digital Converter (ADC) operating with high sampling frequency. This result can be observed in Fig.61, below:

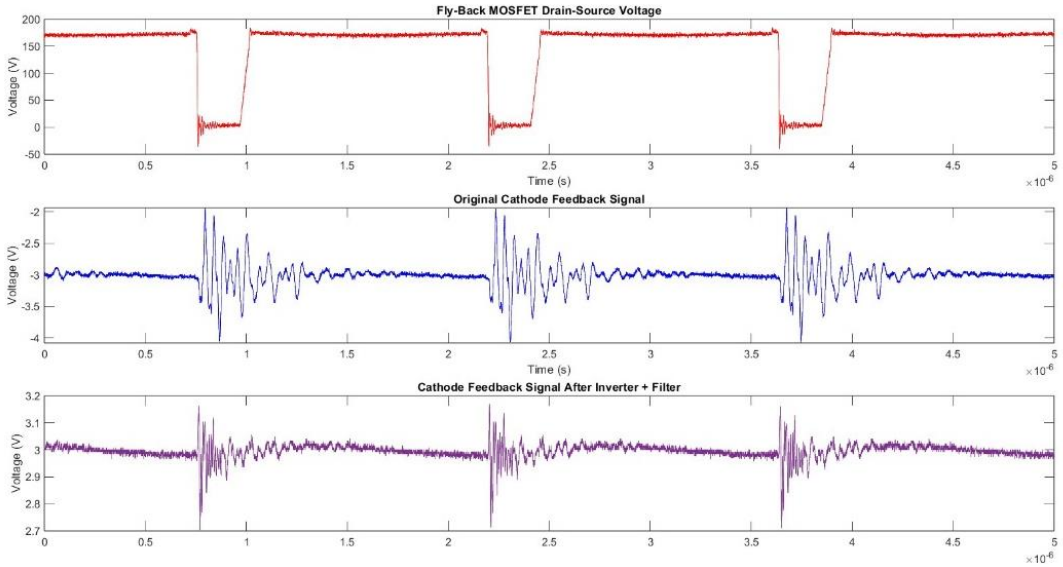

Fig.61: High Frequency Oscillations in Cathode Electrode Feedback Path.

Increasing the allowable dead-time during state transitions reduces the risk of hard-switching events, and allows removal of some high-frequency noise, particularly during fly-back switch turn-on. The variation in the cathode feedback signal, on a microsecond time basis, see Fig.62:

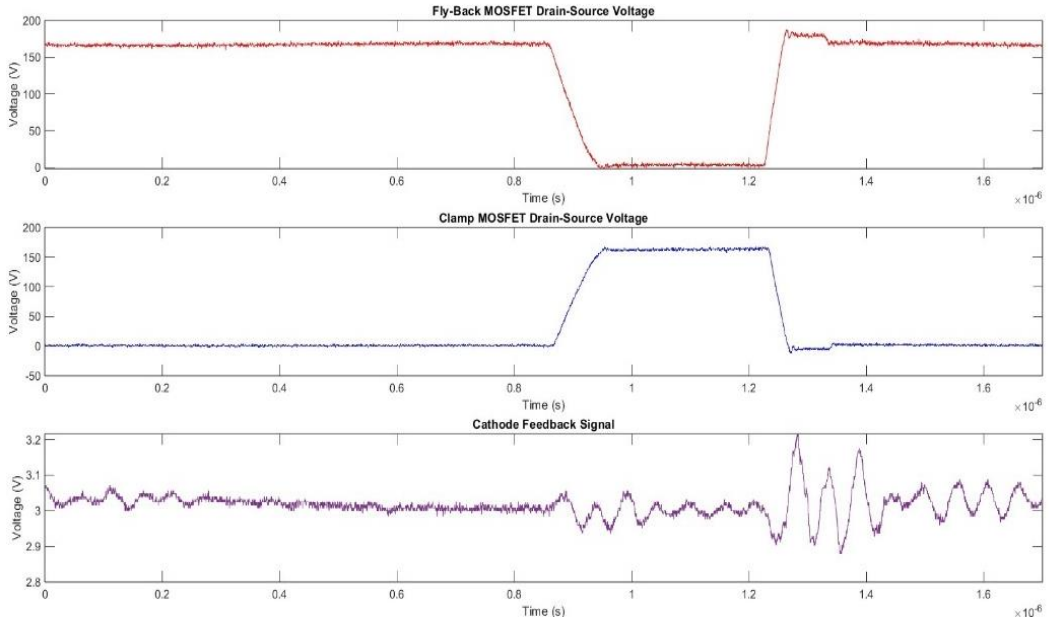

Fig.62: Cathode Feedback EMI Generation due to Hard-Switched Event at Fly-Back Switch Turn-Off.

One can clearly observe that the presence of low leakage inductance results in reduced discharge of the MOSFET output capacitance. This problem is exacerbated using a low DC input voltage, which results in a larger effective MOSFET output capacitance due to DC derating effects. Although the oscillations at fly-back switch turn on have been somewhat reduced, significant noise oscillation still exists during fly-back switch turn-on. Cross-over between the drain-source voltages exists in both state transitions, indicating soft switching is not fully achieved. It should be noted that noise oscillations are at a frequency substantially higher than the switching frequency of the ACF switches, which is beneficial regarding the ease at which they can be attenuated with minimal power dissipation. Following dissipation of the high frequency noise there is a point at where the feedback signal settles to 3V, which is representative of approximately -4kV within the cathode electrode.

One solution is therefore to sample the cathode voltage at this point where it can be assumed the oscillations have dissipated and the feedback voltage may be more indicative of the actual cathode DC level. This would require that the oscillations dissipate back to a steady state within a period that is smaller than the maximum off-time of the fly-back MOSFET. Operational amplifiers with EMI hardened inputs offer some restitution of signal quality, with limiting both maximum voltage slew-rate and bandwidth also significantly reducing noise susceptibility issues within the feedback chains. The issue with this technique is possible reductions in achievable converter bandwidth due to the phase characteristics of the operational amplifier interfering with the phase response of the power stage. The effect of utilizing a 2MHz bandwidth operational amplifier with a $5V/\mu S$ slew-rate is demonstrated in Fig.63.

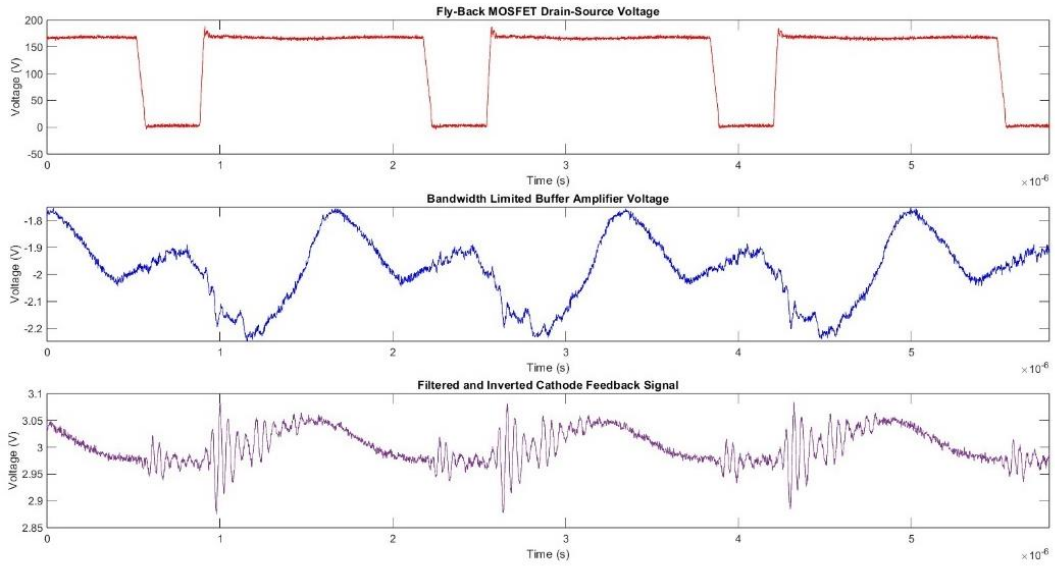

Fig.63: Filtered and Inverted Cathode Feedback Signal during Hard-Switching Event with Limited Bandwidth Buffer Operational Amplifier.

The above figure shows a notable improvement within the noise figures of the final feedback voltage to be passed to the ADC. A digital implementation of a low-pass filter may also provide further attenuation of the high frequency EMI signals imposed on the sensitive feedback signal. Although such methods are often computationally expensive, implementation within assembly language may enhance the overall control law speed. Utilization of a lower bandwidth of approximately ~20kHz would enable a substantial increase in the number of samples obtained with a given ADC sampling frequency, such that simple moving averaging techniques could provide a substantially fixed DC signal that can be used within the DSP control law. This would require larger output capacitance if similar transient response was to be obtained.

Despite the reduced observable noise when utilizing a low bandwidth operational amplifier, the final ADC voltage still exhibits some high frequency noise. This is most likely reintroduced by the inverting buffer amplifier, which must be sufficiently high bandwidth to produce a low impedance driving source to the ADC alongside an RC charge kick-back filter for replenishment of the internal ADC capacitors. Bandwidth limiting the ADC driving amplifier would severely reduce the precision of the data acquisition block and place strict requirements regarding the maximum ADC sampling frequency. A higher source impedance driving the ADC has also been known to introduce gain errors, settling time errors, and strong distortion effects. None of these qualities are conducive to the accurate control required for the cathode of a TWT amplifier. For an in-depth discussion regarding drawbacks of digital control, specifically compared to standard "infinite" resolution analogue control, refer to Appendix A.

There are multiple reasons why high frequency noise may be present within the feedback signals. The most likely issues are circuit board layout and circuit positioning due to reinforced isolation requirements – which can be seen in Fig. 52. PCB layout for high frequency converters is notoriously difficult since loop areas and all parasitics must be wholly minimized. Large loop areas create inductive coupling effects, particularly within sensitive, high impedance feedback lines within the MPM such as the output voltage feedback path. Locating the low-voltage feedback amplifiers, integrated gate drivers and high-voltage load networks in separate mechanical boxes resulted in large loop areas with long length wires passing parallel to significant high frequency noise sources such as the inverter, rectifier, and transformer.

The transformer gaps were implemented on all limbs of the ferrite core, and in the fly-back converter specifically this was a substantial level of the core height to maximize the SRF of the transformer and prevent saturation at the higher magnitude currents that were experienced within the design. Such arrangements have been shown to induce strong magnetic field coupling that is difficult to remove without the use of magnetic shunts.

In future work it is suggested that the gap only be made small to minimize these effects since the transformer capacitance has been shown to be accommodated by the switching topology. It is difficult to discern how much of the noise is present within the signal from that which is inductively coupled into the oscilloscope probes. This issue is particularly exacerbated within high voltage probes, where it is difficult to implement short ground loop measurement methods such as the use of a ground springs. There are two further issues associated with measurement of high voltage power regarding noise measurement, clearly visible in the results:

- 1:1000 attenuation probes: High voltage probes have large attenuation ratios to attenuate the voltage magnitude prior to processing within the ADC of a digital oscilloscope. This means that any noise coupled into the probe following the resistive divider may be amplified within the oscilloscope, and alternative methods must be utilized to measure AC voltage variations and accurate assessment of the DC level.

- Limited resolution of oscilloscope display: An 8-bit oscilloscope, particularly when used with high attenuation, high voltage probes and large voltage division ratios, may display a substantially higher AC voltage variation within the electrode than is present due to quantization effects. This effect can clearly be seen within any result which includes high voltage signals and is most severe within the cathode electrode measurements which implement the largest voltage per division ratio. A superior oscilloscope with more bits, and a digital voltage multi-meter, should provide more accurate results.

The alternative method, proposed in Fig.64 below, may be used to measure the AC voltage variations more accurately within the cathode electrode:

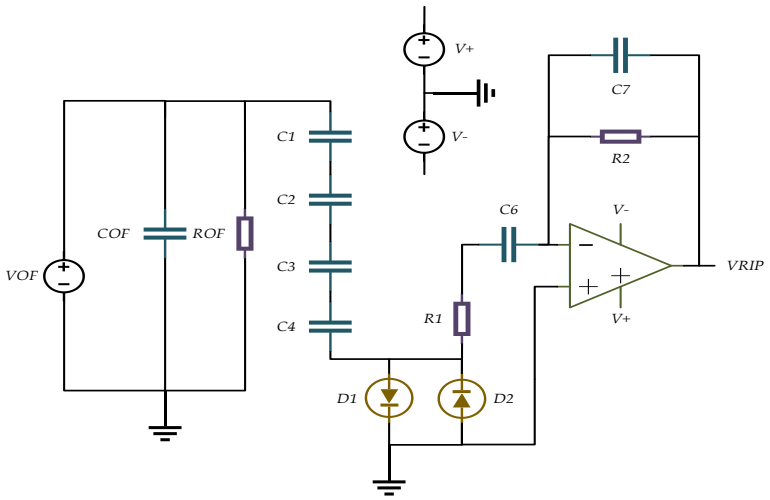

Fig64: Proposed Circuit Implementation for Measurement of AC Voltage Variation on the Critical Cathode Electrode Output.

This circuit utilizes 4 series connected AC-coupling X7R ceramic capacitors each rated to 3kV to provide reinforced isolation to 12kV for measurement by the user. Bipolar diodes provide additional protection. An operational amplifier before the oscilloscope measurement is provided in a band-pass filter arrangement to isolate the switching frequency ripple due to the assumption that the output capacitors and any additional passive filter should have substantially filtered out any higher frequency harmonics and to remove 50Hz interference from safety circuits and AC power supplies. The results in Fig.65 illustrate the measured AC voltage ripple imposed on the cathode electrode of the TWT load, alongside the fly-back switch drain-source voltage transitions to demonstrate the location of the high frequency EMI noise that is generated:

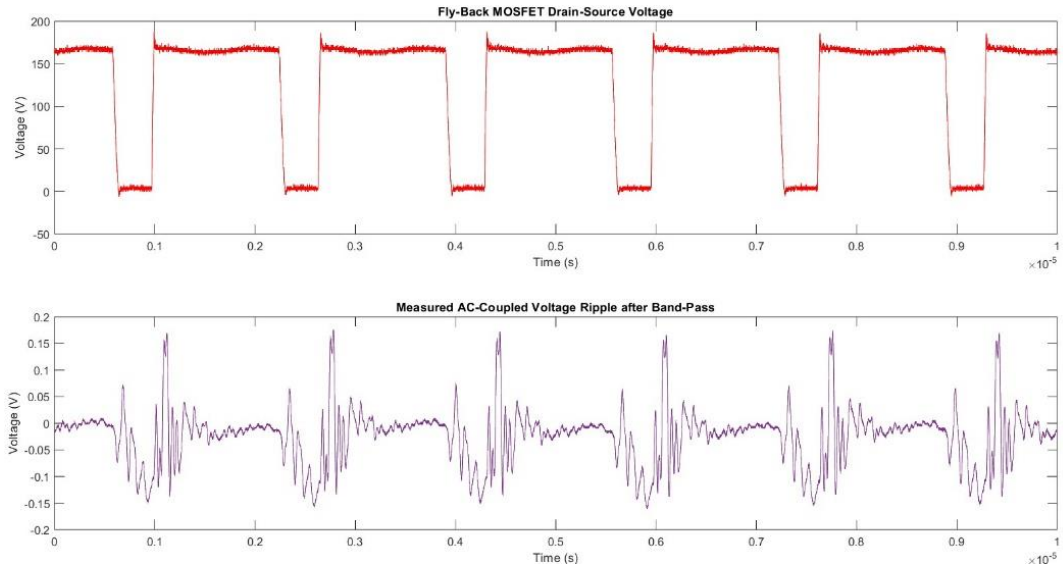

Fig65: AC Voltage Measurements within Cathode Utilizing Proposed AC-Coupled Circuit.

Particularly when attempting to accurately measure AC voltage measurements in the range of ~0.1V on a -4kV output voltage, noise pollution can clearly impede one's ability to verify performance. Additive noise within the signals is well above the switching frequency, particularly before the band-pass filter. High-frequency noise on the output of the band-pass filter could also be coupled through high frequency noise artifacts present within the operational amplifiers dedicated +/-5V power supply.

With 4 series connected 1nF capacitors, the effective capacitance is approximately 0.25nF. To calibrate the AC-feedback circuit, a simple 10V sinusoidal wave is fed into the output capacitance of the EPC. The resultant voltage following the bandpass filter was attenuated by a factor of approximately 32.258. The voltage ripple following the band-pass filter (see Fig.64) is 0.3V peak-to-peak, which is indicative of an AC-voltage variation in the region of 9.6774V. It can be observed, however, that following the settling of the high frequency EMI following a switching event, the

experienced voltage ripple is of substantially lower amplitude. It should also be noted that, since the calibration was performed with a low voltage sinusoid from a function generator, DC voltage derating effects of X7R dielectric ceramic capacitors are consequently low.

When a significant DC voltage component is imposed onto a ceramic capacitor with X7R dielectric, the actual effective capacitance of the package may drop substantially by more than 90% of the given nominal value in the data sheet. This means the voltage ripple attenuation factor may be higher in calibration than during practice, such that the voltage ripple may be significantly lower than would be predicted by theory. The use of a function generator also adds substantial amount of error to the measurement, due to the 50Ω output impedance forming an additional low-pass filter within the input-to-output response. As a result, future work should also place significant emphasis on improving the calibration method for measuring high-voltage ripple to ensure an accurate assessment is made of the cathode AC variations that are pivotal to enhancing phase-noise performance of the TWT amplification process. This should involve effective isolation of the switching ripple and attenuation of any generated EMI, as well as use of capacitors with higher grade ceramics which do not exhibit substantial derating with temperature, applied DC voltage, or time.

6 FUTURE WORK AND CONCLUSIONS

This research has concerned the design of a high voltage, high frequency EPC for supplying the demanding electrode voltages of a TWT amplifier within a compact MPM device for airborne multi-mode radar EW/ECM applications. To optimize phase-noise performance within the RF amplification process, the level of AC voltage variation within the cathode electrode is critical and of utmost importance, and voltage deviation due to the presence of highly dynamic behaviour of varying frequency and duty cycle within the load must be compensated with a sufficiently high closed-loop controller bandwidth. Both requirements are usually accommodated using analogue post-regulator circuits which are difficult to isolate and occupy essential PCB real-estate, which is detrimental to efforts to optimize power density within the EPC.

Rather, new WBG semiconductor devices have recently been proposed to allow operation of transistors at elevated switching frequencies to substantially reduce solution size, weight, and maximize phase-noise performance while enhancing the closed-loop controller characteristics without post-regulation techniques. Despite this, research regarding use of such devices within multi-kilovolt EPCs for MPMs is substantially lacking, likely due to the innate characteristics of high voltage physics at elevated switching frequencies coupled with the presence of significant levels of parasitic capacitance within safety isolation power transformers, which traditionally limit the achievable switching frequency. Through a literature review, only one EPC topology was identified that was able to operate at frequencies above 500kHz while generating the entirety of the power requirements of the cathode and collector electrodes of a TWT - but required multiple series connected transformer-rectifier modules due to the lack of advanced semiconductor material devices. A research study regarding the use of WBG semiconductors for a TWT EPC was included, but this did not attempt to generate the full voltage potentials required within the application. The collector and cathode electrode load configuration were also not indicative of a true TWT load, with no common voltage output for the electrodes – the study therefore did not consider the true current sharing behaviour that is present within a TWT amplifier.

The EPC of the TWT utilized within this research is composed of two main electrodes. The cathode electrode, operating at -6kV, accelerates an electron beam and amplifies an input RF signal through direct transfer of energy from the beam to the RF signal. The collector electrode, operating at a voltage of -3kV, recycles the electron beam to improve overall TWT efficiency. The EPC requirements for the individual electrodes, however, are considerably disparate.

The collector load constitutes more than 91% of the entire processed power, with the cathode regulator requiring only ~10mA and approximately 60W of power which is dissipated to the tube body. During periods of microwave transmission, any phase-shift between the RF input and output will severely degrade the radar's performance. The phase-pushing factor of the cathode electrode far exceeds that of the collector electrode, such that AC-voltage variations within the collector electrode have negligible effects on input-to-output phase modulation of the RF signal. Variable frequency operation of EPCs has been shown to hinder phase-noise performance through the generation of multiple switching frequency harmonics and their associated harmonics within the cathode output which must be adequately filtered. Furthermore, product verification becomes more difficult, as performance must meet strict requirements across every possible discrete switching frequency that is implemented within the EPC.

In high voltage EPCs that exhibit naturally high parasitic transformer capacitance and utilize capacitively filtered outputs, standard FHA analysis techniques in literature are not applicable due to complex non-linearities introduced by finite charge and discharge times and attenuation during periods of output diode conduction. Particularly in higher power resonant conversion systems, there exists substantial concerns regarding stability across line and loading conditions when attempting to close the controller feedback loop around the EPC due to non-linear relationships between switching frequency and output power, particularly close to the resonant peaks where the issue is most severe. It is common that such converters are designed to be conditionally stable, with acceptable behaviour at a defined operating voltage, frequency, and load. Such converters are, therefore, not suitable for use in many applications in their most basic form.

Particularly in multi-resonant converters such as "LCC" and "LLC" converters, there also exists a significant second-order response to changes in control voltage, such that a notable amount of switching instants are required to change the average output capacitor current. This places strict limitations on the achievable controller bandwidth, and it becomes difficult to verify stability over all line and loading conditions. Unstable behaviour at any operating point will substantially degrade the effectiveness of the EPC to provide the necessary quality of power delivery required. These control issues are of particular concern with multi-mode TWT loads since there exists highly dynamic behaviour where load current transitions from full-load to zero-load at widely varying frequencies and duty cycles. To ensure adequate transient response during pulsed operation, the cathode electrode must not deviate by more than +/-5V during any transient event. The requirements for the collector electrode are much less strict, with +/-200V deviations being considered acceptable before significant heat dissipation occurs within the tube due to non-optimal depression ratios and thus efficiency degradation.

In a standard EPC where the cathode and collector are generated with a single transformer and rectifier network, it becomes extremely difficult to avoid the collector supply from directly influencing the critical cathode electrode. This research therefore proposes a "hybrid" EPC structure which consists of two parallel connected EPCs connected to the common 270VDC line voltage. The first, intended to power the collector electrode, is a series parallel "LCC" multi-resonant converter. Since the heat-sinking system of the EPC typically constitutes a large portion of the overall solution size and weight, this converter is optimized for maximum efficiency through utilization of lower switching frequencies. This minimizes the heat removal system burden through minimizing transformer core and winding losses, as well as any other switching related losses that dissipate significant power which would need to be removed from the EPC through the grounded chassis of the MPM package.

The collector electrode EPC may be operated under variable switching frequency since the phase-pushing factor of this electrode is not critical to phase-noise performance of the radar. It is still prudent to minimize frequency bandwidth through utilization of large series-to-parallel capacitor ratios within the design to make reduce the number of frequencies the EPC must be verified across. Operating the series-parallel converter under duty cycle control when operating at high powers is incredibly difficult, since duty cycle variations required during transients are often severe due to wildly varying gains within the voltage transfer function during unloading. Voltage deviations during transient events were shown to be related to the controller bandwidth, output capacitance, and the magnitude of load current changes during dynamic events within the load. High controller bandwidths are notoriously difficult to achieve with high power resonant converters which are often restricted to VMC without specialist hardware modifications. This is due to wildly moving poles and zeroes within the voltage transfer function, second-order responses to changes in control voltage within VCOs, and nonlinear behaviour when operating close to high power resonant peaks.

By separating the converter into two separate EPCs each with dedicated control loops and output capacitances, the control loops for each EPC can also be optimized depending on their individual requirements. The cathode EPC capacitors need only be sized to adequately minimize voltage deviation during a load current transient event of substantially reduced magnitude and load current transitions within the collector do not affect the cathode. The cathode regulator control loop may also maintain precise control of the nameplate voltage despite significant deviations within the collector voltage during transient events, with the only drawback being increased power dissipation within the TWT due to a reduced ability to effectively recycle electrons from the amplification process due to a changing depression ratio. To minimize these effects, it is also proposed that the collector completely halt switching of the transistors during periods of no RF amplification through

utilization of the PRF information that is available within the MPM. The product then only needs to be verified for stability under varying line voltage at full load.

The critical cathode EPC is formed by a multi-resonant ACF converter, operating at fixed switching frequencies of at least 600kHz to minimize solution size and substantially attenuate any AC voltage variations within the output voltage without utilization of any analogue post-regulator circuits. Due to the processing of low power, substantially higher frequencies can be implemented while an exceptional overall efficiency can be maintained. The control-to-transfer voltage function nonlinearities which plague high-power resonant converter operation are forced into the linear region through operation further away from the non-linear resonant peaks of the converter for a given required voltage gain. This configuration presents considerable strengths over state-of-the-art converters.

Extended FHA methods already existing in literature were utilized to design and simulate a high-power (600W) EPC for the collector electrode of a TWT. These works were expanded upon to demonstrate frequency limitations of high voltage, high frequency conversion. It is proposed that, for a given load rectifier network, the product between the transformer turns ratio, parallel capacitor level, and angular switching frequency be utilized to examine the maximum output voltage than can be generated without respective increases in peak magnetizing currents within the transformer. As angular switching frequency increases, the achievable conduction angle for a given load rectifying network decreases exponentially. The frequency limitation product was more critical when considering low-power parallel resonant converters, however the peak currents required were of similar magnitude to those required in hard-switched converter topologies operating in DCM as magnetizing current is also a function of required load current.

It is likely, therefore, that the maximum output voltage is limited by peak operating flux density of the implemented transformer core and high frequency AC winding loss. Reducing the parasitic capacitance remains the main enabling factor for achieving high switching frequencies in the EPC, but higher parasitic capacitances can be accommodated through a reduced transformer turns ratio such that the capacitor must charge to lower voltage magnitudes within a given period. This concept is utilized to enable development of a modified design procedure for the proposed cathode EPC through simple modifications to equations that allow estimations of the changing diode conduction angles when operating with asymmetrical duty cycles. This essentially models a 50% duty cycle excitation within a "modified" switching period. This is in stark contrast to currently available literature which typically entails a rather involved set of calculations. It is shown that the proposed converter can achieve considerable voltage step-up while operating well above the non-

linear resonant peaks due to the combination of high parallel resonant quality factors and an increased effective tank RMS input voltage when compared to standard half-bridge converters.

Through asymmetrical duty cycle control, the converter may switch between two alternating resonant converter states; a series-parallel resonant state, and a parallel resonant state. This operation is akin to fixed-frequency variable impedance control of resonant converters commonly proposed in literature. This novel technique of regulation is particularly of interest in high voltage outputs that utilize full-bridge voltage multipliers. Each state has a corresponding rectifying diode and output capacitor, which are charged to different voltages depending on the duty-cycle selected and the passive component selection. Although the series resonant inductor and parallel capacitor are shared between each switching state, the insertion of an additional series capacitance allows modification of the tank impedance. The clamp capacitor value should be sufficiently larger than the parallel capacitance to avoid a large separation between the parallel resonant peaks of the two states for effective duty cycle control across loading conditions, while it should not be too large to impact transient response.

Through changing the fly-back switch duty-cycle, the achievable output voltage can be either increased or decreased through multiple mechanisms. First, reducing the conduction angle during the parallel state reduces the output voltage imposed on the output capacitor that corresponds to this state. This then effects a reduced clamp voltage during fly-back switch turn-off, reducing the effective tank RMS voltage of the converter. This, in turn, also attenuates any additional gain within the series-parallel state during periods of no RF amplification. Decreases in the duty cycle cause the opposite effect. The cathode voltage is formed by the average voltage across the two capacitors within the voltage multiplier. It seems, particularly when operating sub-resonance, that the converter can automatically minimize the difference between the parallel capacitor voltages through attenuation of the resonant inductor voltage.

Simulation results of both the high-power resonant collector regulator and the novel multi-resonant ACF were provided and showed very good agreement with the proposed design methodologies. The issues regarding control of high-power resonant converters are given, with VMC giving clearly poor results unless the PRF information is utilized as suggested. Simulation results are also provided for the novel ACF topology at both full and zero-load conditions. A complete set of transient performance results are also provided. Although performance with VMC is acceptable provided enough output capacitance is present, performance can be enhanced through ACMC which involves sensing of the series resonant inductor current, implementation of a current sense amplifier, and an additional average current mode control loop.

Practical results are provided which demonstrate operation of the collector electrode EPC in open-loop generating -2kV at 243V line voltage and -2.5kV at 297V line voltage at an increased switching frequency of 220kHz to achieve a constant 50% depression ratio. The converter demonstrated impressive efficiencies of ~95% across all line conditions. To generate the full -3kV at the intended switching frequency of ~180kHz, it is necessary to insert additional series resonant inductance within the primary and evenly distribute additional parallel capacitance across all four secondary windings to increase circuit gain. This additional capacitance will also reduce the required frequency bandwidth for regulation of output voltage across loading conditions.

The resonant behaviour and enhanced voltage gain capability of the ACF converter was not originally intended, as the transformer was eventually wound with each secondary in two separate layers. This led to a much larger capacitance than originally designed. Testing of the converter, therefore, led to many interesting and unexpected results. Since the switching frequency was at a point below the parallel resonant peaks of the two implemented states, the standard design procedure became invalidated due to, most likely, oscillatory waveforms due to insufficient level of resonant inductance and thus higher resonant frequencies than demanded by the design.

Additional equations and simulation results were provided to extend the given design procedure to include the effect of oscillatory voltages on the achievable voltage gain of the two states for a given set of voltage gain coefficients. It was demonstrated mathematically that the maximum parallel capacitor voltages can be expressed as a function of the voltage imposed on the series resonant inductance. This reinforced the proposed theory that oscillatory behaviour within the series resonant inductance waveforms when operating sub-resonance, which both attenuates achievable voltage gain and automatically limits maximum parallel capacitor voltage magnitudes, occurs irrespective of AC voltage variations within the clamp capacitor voltage.

Despite these significant issues, an output voltage of -4kVDC was generated at a line voltage of just 125VDC – a voltage gain of 32x. This corresponded very strongly with the simulation model utilizing the passive component values used within the original ACF design when operating from reduced line voltage levels. To demonstrate the accuracy of the remaining design procedure, the simplified conduction angle equation proposed was utilized. Alongside measurement of the series-parallel output diode waveform, and sensing of the peak series resonant inductor currents during each state, it was shown that the given design equations give good approximations of the achievable output voltage within the cathode electrode even during sub-resonance operation. The actual output voltage gain, when operating sub-resonance, can often be further attenuated by the high frequency current oscillations within the clamp circuit. Since the series-parallel output diode will still conduct current at the actual angular switching frequency, the magnetizing current magnitude

may be substantially less than the peak current that flows through the series resonant inductor and clamp capacitor. A novel expression for this effect is given and verified within simulations. Despite this, the full output voltage was developed. This may be due to the expressions utilized being slightly conservative, which was observed in the full load simulations. Direct measurement of the magnetizing or diode output currents during each state may provide greater insight, as the actual diode conduction angles can often be larger than is observed in the output diode voltage waveforms.

Significant issues existed regarding noise susceptibility of sensitive feedback lines when operating at elevated switching frequencies. Due to the implementation of low leakage inductance to minimize duty cycle loss in standard ACF converters, the rise and fall-times of the WBG semiconductor devices are most likely slower than could otherwise be achieved. Insertion of additional leakage inductance has also been known to substantially reduce EMI within the rectifier due to reduced current slew rates. Although slow rise and fall-times have been known to reduce EMI, they may have also led to hard-switching events which, coupled with sub-resonance operation, generated a considerable amount of noise pollution that was not alleviated by insertion of a critically damped EMI input filter. Capacitive operation of the isolation transformer during the individual switching states allowed a conduction path for high frequency EMI to the intended low-noise output. Due to poor circuit board layout and the requirement for physical isolation from the high voltage circuits, the loop areas and wire lengths were of inappropriate values. This led to the coupling of high magnitude EMI into sensitive feedback lines of frequency substantially higher than that of the switching frequency. The use of twisted pair cables with grounded shields offered some protection through decoupling of noise to the chassis. The use of passive filtering circuits, EMI hardened operational amplifiers, and limiting both bandwidth and slew-rate also offered good protection against interference, but due to time constraints closed-loop control could not be implemented.

The existence of high frequency EMI also severely degraded the ability to determine accurately the level of AC voltage variation within the critical cathode electrode. A proposed AC-coupled band-pass operational amplifier circuit was utilized to isolate the switching ripple frequency for assessment of phase-noise performance within the TWT load. Results show that a 4nF series connected AC-coupling capacitance chain attached to the cathode electrode output produced an equivalent voltage deviation during a switching event of just under 10V. It is clear from the data, however, that most of the noise is of a frequency substantially higher than the implemented switching frequency. Following dissipation of these high frequency oscillations, the actual AC-voltage variation magnitude is of a significantly lower value. It should also be noted that the dielectric quality of the implemented AC-coupling capacitors can also affect the magnitude of

apparent switching ripple with this method. Particularly with X7R dielectrics, DC voltage rating effects can reduce the effective capacitance of the package by up to 50%. Since the calibration was performed with a 10V sinusoid imposed on a low voltage DC signal, these effects were not considered in the calibration procedure. Other methods of measuring small scale AC-voltage variation on high voltage outputs therefore should be proposed, with corresponding calibration methods to ensure the high level of accuracy required is obtained with DC derating effects considered.

Future work should investigate the following points:

1. Operation of the novel cathode EPC with passive components calculated with the proposed design procedure, ensuring operation above all possible resonant peaks within each state is obtained. Net inductive operation must be ensured to minimize noise coupling through the transformer and attenuation of high frequency EMI within the switching signals through the formation of low-pass filters of much lower cut-off frequency within all resonant states. This will also remove current oscillations within the clamp circuit current, as well as oscillations within the resonant inductor voltage waveform experienced when operating sub-resonance which are detrimental to the given design procedure. This will allow more suitable AC voltage gain coefficients to be implemented, such that testing can be formed at the full DC line voltage due to a reduced tank gain within each state. Insertion of additional series inductance will considerably reduce EMI generation within the rectifier through a reduced current slew rate, while also reducing MOSFET output capacitance charge and discharge to enable soft-switching operation of the WBG transistors more easily. A variable driving resistor is included in the integrated gate drivers to allow variance within the voltage slew-rate of the GaN devices to further optimize performance if required.

2. With the above recommended circuit implementations, assuming high frequency EMI has been substantially attenuated, use of an FRA will allow full analysis of the open-loop gain and phase characteristics of the topology such that closing the feedback loop can be achieved through the proper compensation of the digital controller. This is essentially to assessing the dynamic performance of the proposed EPC under transient events typically required in multi-mode TWT radar transmitters.

3. Mitigation of the experienced levels of DC current within the power transformer due to asymmetrical duty cycle should be investigated. Equalising the output voltage on the individual capacitors within the full-bridge multiplier at steady-state and nominal line

conditions when phase-noise is most important should be implemented. Although this issue is not insurmountable, the presence of DC current within the transformer is detrimental to power density efforts due to the requirement for a larger transformer core to avoid high power dissipation or even flux saturation. This may be achieved with the implementation of a large magnetizing inductance which increases impedance at any given angular switching frequency, but this often degrades transient performance through the reduction in the RHPZ frequency location. The novel "LLCC" four-element ACF may allow minimization in DC current through providing better control of the AC voltage gain coefficients, and due to the enhanced voltage gain and bandwidth capabilities, should be investigated further.

4. Minimization of the transformer capacitance remains an absolute necessity for achieving elevated switching frequencies and thus optimization of solution power density in airborne EPCs. Smaller transformer capacitances allow faster voltage slew rates, such that larger voltage magnitudes may be achieved within reduced periods. Higher voltage outputs may be generated for the cathode electrode with reduced magnetizing currents and thus reduced core size for any imposed volt-second product. This becomes difficult with shrinking core size, however, as geometry plays a vital role in determination of transformer parasitics. Further research, therefore, should also focus on techniques to minimize transformer parasitic capacitance through novel winding geometry or techniques.

5. Investigation into the trade-offs between digital closed-loop controller accuracy and bandwidth of digital controllers in critical low-noise, high-accuracy power supplies such as those required in TWT devices. Research should also investigate the implementation of novel techniques for achieving this, such as those proposed within this thesis. Techniques may include the use of external high accuracy ADCs, enhanced high resolution pulse width digital modulators, and direct sensing and utilisation of the switching voltage ripple imposed on the cathode electrode voltage within the control loop.

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8 APPENDICES

The appendices of this thesis will briefly introduce and discuss additional bottlenecks that constrain design of high frequency, power dense EPCs within an MPM. Beyond that of the transformer parasitic components, implementation of digital controllers, transformer power losses and temperature rise, and PCB design are just some factors to consider. This chapter will also attempt to identify potential solutions to overcome these challenges to enable full utilization of WBG devices and the elevated switching frequencies that they are intended to operate at.

8.1 APPENDIX A: DIGITAL V ANALOGUE CONTROL TECHNIQUES

Particularly with the generation of ultra-low-noise outputs, the power supply is still fundamentally an analogue circuit – and even the most advanced software algorithms cannot overcome limitations within the power supply design. Digital controllers are essential for implementation of increasingly complex control systems, such as sliding mode [120], model predictive [121], and adaptive [122] controllers. Artificially intelligent controllers may implement machine learning and deep learning techniques such as Neural networks [123], fuzzy logic [124], and genetic algorithms [125]. Particularly of interest for resonant controllers is the introduction of non-linear control [126], which may provide control capability close to the high-power resonant peaks where the converter exhibits highly non-linear behaviour. When attempting to implement digital controllers for MPM EPCs, there are many factors to consider which may hinder performance significantly. These include central processing unit (CPU) limitations and achievable PWM resolution, ADC inaccuracies, choice of sampling times, and digital control delays and achievable bandwidth.

8.1.1 CPU Limitations and PWM Resolution

CPU clock speed dictates numerous features of the DSP such as the effective number of bits, required bits in the counter required to set desired switching frequency, and how many clock cycles are available within a given clock frequency. The achievable PWM resolution is the discrete change between neighbouring duty cycle implementations, or for variable frequency supplies, the separation between two neighbouring switching frequencies. A simple expression for the percentage duty cycle resolution $D_R(\%)$ for a given inverter switching frequency f_{SW} can be found:

$$D_R(\%) = \frac{f_{SW}}{f_{Clk}} * 100 \qquad (8.01)$$

Often, the PWM clock frequency f_{Clk} is not equal to the CPU clock frequency. In the F2387xD CPU, the maximum clock frequency is 200MHz – but the PWM clock frequency is limited to a maximum of 100MHz. For a switching frequency of 600kHz, this limits the duty cycle resolution to:

$$D_R(\%) = \frac{600kHz}{100MHz} * 100 = 0.6\% \qquad (8.02)$$

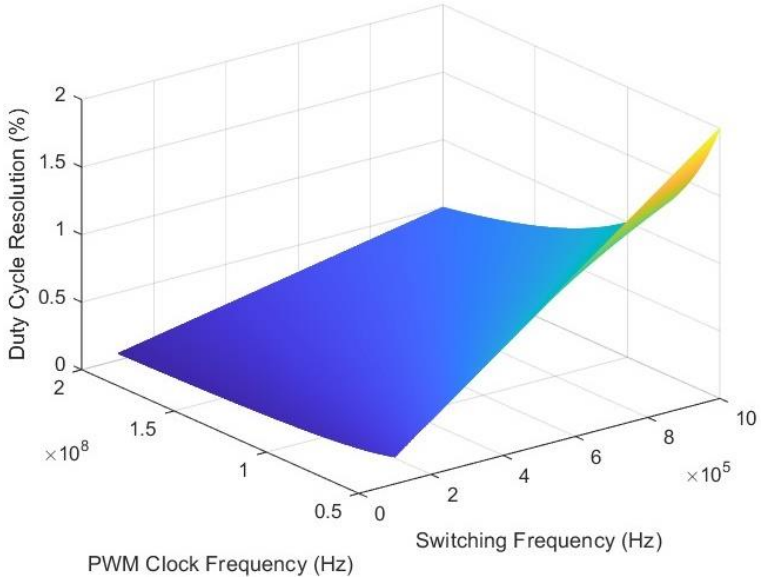

Fig.66: Visualization of Achievable Duty Cycle Resolution with Differing Switching Frequencies for Typical DSP CPU PWM Clock Rates.

This has significant implications regarding output voltage resolution of the cathode. The coarse output voltage adjustment that is possible during steady-state and transient operation is impacted as the changes in the clamp capacitor voltages and diode conduction angles have finite resolution. This can be considered in the ACF converter, as follows:

$$\Delta V_{CL} = N_F V_{O_P} + \frac{2L_{R_F} F_{S_F} P_{O_P}}{\alpha V_{DC} \Delta D_F (1 - \Delta D_F)} \quad (8.03) \quad \theta_F = 2\tan^{-1}\sqrt{\frac{\Delta D_F T_{S_F}}{2C_{P_F} R_{O_F} N_F^2}} \quad (8.04)$$

Where ΔD_F is the duty cycle resolution, which leads to further discretization effects in the actual, developed output voltages within both the parallel, and series-parallel power stages by discretization of the voltage coefficient and peak active-clamp capacitor voltage levels:

$$\frac{k_p \Delta \widehat{V_{T_r}}}{N_F \Delta k_{v_P}} = V_{O_P} \quad (8.05) \qquad \frac{k_l \Delta \widehat{V_{T_r}}}{N_F \Delta k_{v_L}} = V_{O_L} \quad (8.06)$$

This problem is only exacerbated if operating within a smaller range of duty cycles, as the voltage perturbation between neighbouring duty cycles and/or frequencies can be more severe. The effects within the collector regulator regarding maximum output voltage deviation due to a frequency change will be similar, but this is of secondary concern as the regulation requirements for acceptable phase-noise performance are much less strict. A further impact of duty cycle resolution is the number of clock cycles required for a given PWM pulse width. If the required duty cycle from the controller is 33.3%, the required on-time of the fly-back switch t_{ON_F} can be calculated:

$$t_{ON_F} = \frac{D_R}{F_{S_F}} = 555nS \qquad (8.07)$$

Immediately, since the switch on-time is related to the switching frequency, one should understand that utilizing a low clock frequency will affect the setting of the actual initial switching frequency. The accuracy is more severely affected, however, by the required number of PWM clock cyclesn_{clk} required to achieve the specified on-time. Assuming a 100MHz PWM clock:

$$n_{clk} = t_{ON_F} f_{CLK} = 55.5 \qquad (8.08)$$

A digital controller cannot output fractional clock cycles, and thus the closest integer number of cycles will be used. This again will severely impact the cathode regulator's ability to provide a substantially fixed voltage equal to that of the radar transmitter nameplate. One solution to this issue is inclusion of specialized, digital circuitry such as the High-Resolution Pulse Width Modulation (HRPWM) module within the F2837xD series of microprocessors. This substantially extends the capability of the PWM module to allow much finer time granularity control of the implemented timer period, duty cycle output, and even dead band between switching instants. This is achieved through implementation Micro Edge Positioner (MEP) technology, capable of positioning an edge very finely by sub-dividing one coarse system clock of a conventional PWM generator. As a result, time step accuracy can be increased to the order of 150pS [127]. The table below illustrates the comparable resolution with and without the use of an MEP:

PWM Freq	Regular PWM Resolution		Extended HRPWM Resolution	
(kHz)	Bits	%	Bits	%
20	12.3	0.02	18.1	0.000
50	11	0.05	16.8	0.001
100	10	0.1	15.8	0.002
150	9.4	0.15	15.2	0.003
200	9.0	0.2	14.8	0.004
250	8.6	0.25	14.4	0.005
500	7.6	0.5	13.4	0.009
1000	6.6	1	12.4	0.018
1500	6.1	1.5	11.9	0.027
2000	5.6	2	11.4	0.036

Table 6: Time-Base Resolution for Regular and Extended Precision PWM with Increasing Frequency for 100MHz Clock Frequency.

The above table clearly shows the significant improvements that are offered by utilizing a more fine-grained control of the PWM of the digital PWM implementation. However, even at a switching frequency of 500kHz and incorporation of HRPWM, the extended resolution offered is 0.009%, corresponding to an Effective Number of Bits (ENOB) of 13.4. Even if the switching frequency of the cathode was reduced to 500kHz to enable this ENOB, the output voltage sensitivity including just a 5% overvoltage allowance for full-range ADC sensing is 0.583V.

8.1.2 ADC Inaccuracies

There are numerous inaccuracies that are inherent to the process of converting an analogue-based signal to an "equivalent" digital representation. Resolution in an analogue based controller is essentially infinite, as it does not experience any kind of discretization effects. The resolution of an ADC rs_{adc} can be expressed as:

$$rs_{adc} = \frac{V_{Rf}}{2^{N_b}} \quad (8.09)$$

Where V_{Rf} is the implemented reference voltage and N_b is the number of discrete bits within the ADC. In high voltage outputs, it is of utmost importance to manipulate the above equation to include the effects of the resistive divider within the feedback path and the possibility of overvoltage. The F2837xD has a full-scale input voltage of 3.3V, and allowing for a 10% overvoltage condition results in the following resolutions for 8-bit, 12-bit, and 16-bit ADCs:

$$rs_{adc_8} = \frac{3.3}{2^8} = 12.9mV \qquad rs_{adc_{12}} = \frac{3.3}{2^{12}} = 805.7\mu V \qquad rs_{adc_{16}} = \frac{3.3}{2^{16}} = 50\mu V$$

Assuming a voltage divider of 1:2000, these correspond to actual output voltage resolutions V_σ within the cathode considering 8, 12, and 16-bit ADCs as follows:

$$V_{\sigma_8} = 25.8V \qquad V_{\sigma_{12}} = 1.6114V \qquad V_{\sigma_{16}} = 0.1V$$

Although suitable to measure the transient perturbations within the output voltage, a 12-bit ADC would be unsuitable for this application, as during steady-state a ~1.6V deviation from the cathode nameplate voltage could cause substantial issues in the stability of the amplification process. A 16-bit ADC will meet the criteria for this thesis, however in practice, additional bits may be required to compensate for further inaccuracies within the ADC. On many DSPs, including the F2837xD, the 16-bit ADC can only be utilized with differential signalling. Differential signalling has multiple benefits for low-noise voltage and current sensing due to the innate cancellation of common-mode noise generated elsewhere in the power supply. Unfortunately, the cathode electrode is a single-ended source, meaning it is not suitable for differential signalling in the current configuration. A Fully Differential Amplifier (FDA) [128, 129] is proposed in this work to directly translate a single-ended, ground referenced source to an equivalent differential signal to allow high resolution sampling:

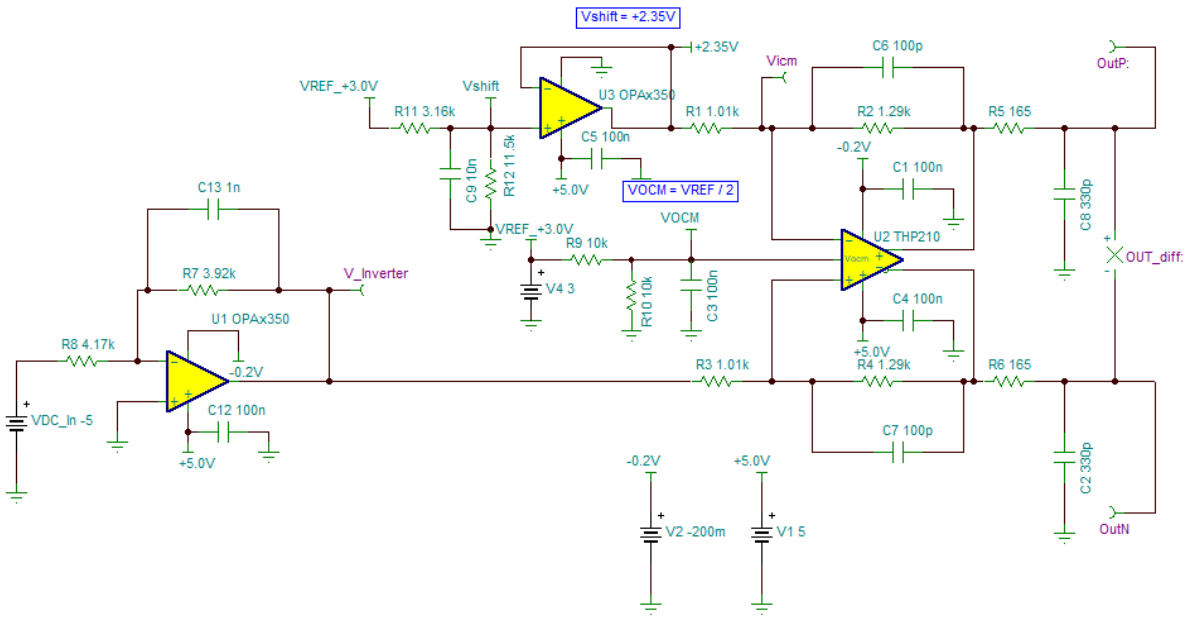

Fig.67: Utilizing a Fully Differential Amplifier to Translate a Single-Ended Source to an Equivalent Differential Signal for 16-bit Sampling.

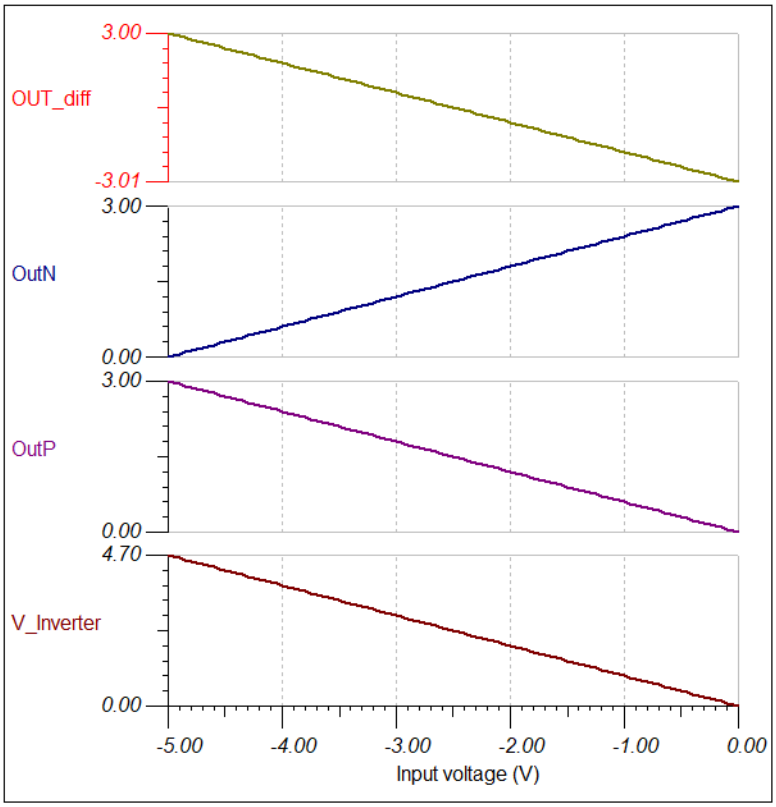

Fig.68: FDA Output Signals for a 0-5VDC Cathode Feedback Voltage.

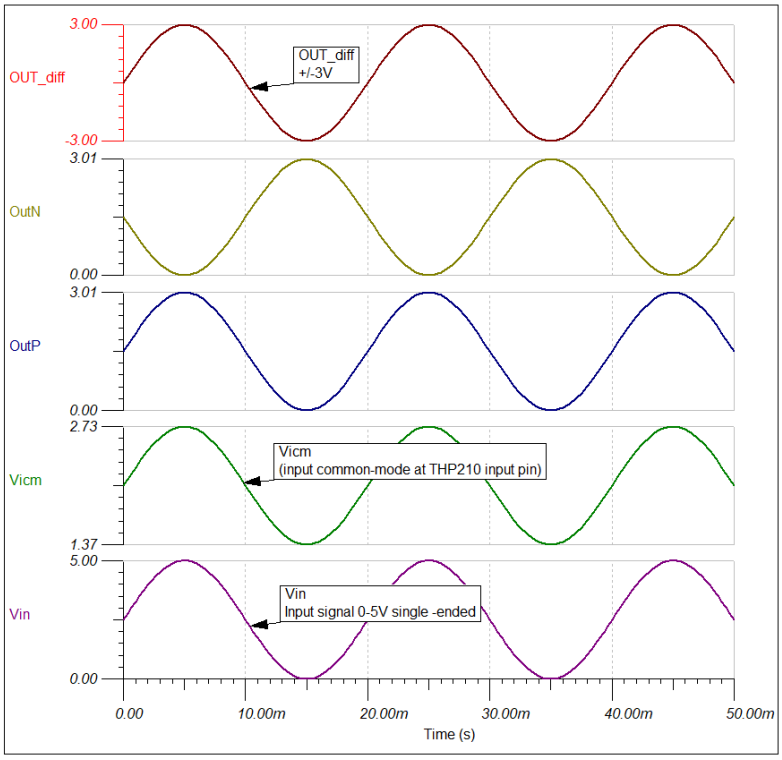

Fig.69: Translation of 0-5VDC Cathode Feedback Voltage to a Differential Output Voltage.

8.1.3 Limit Cycle Oscillation

Limit Cycle Oscillation (LCO) is produced when nonlinear interactions between the ADC and digital PWM quantization effects result in steady-state movements of the system state-space trajectory. This has been shown to cause power supply instability and may lead to severe effective AC variations on the critical cathode voltage, resulting in severely degraded phase-noise performance [130, 131, 132]. LCO can be avoided through the incorporation of integrator action within the control loop, coupled with meeting certain conditions regarding both digital PWM resolution $q_{v_o}^{DPWM}$ and ADC resolution $q_{v_o}^{\frac{A}{D}}$:

$$q_{v_o}^{DPWM} < q_{v_o}^{\frac{A}{D}} \quad (8.10)$$

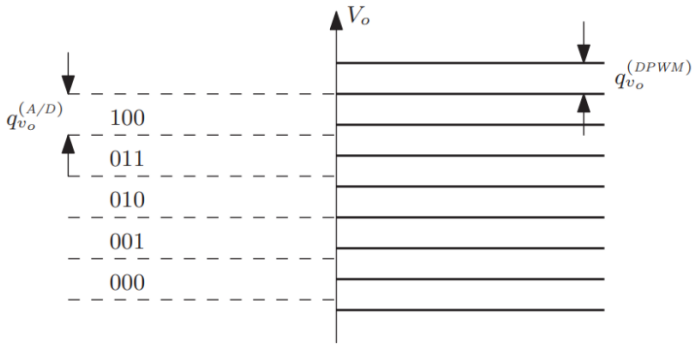

Fig.70: Conditional Requirement for Avoidance of Limit Cycle Oscillation [133].

This has several implications regarding the implementation of digital control for high-resolution, fine-grained control of sensitive output voltages.

1. Resolution of digital PWM resolution must exceed that of the ADC when both are expressed in terms of the output voltage quantization. Digital PWM resolution is therefore considered, by far, the most significant limiting factor for the application of digital control.

2. Maximum resolution of ADC in number of bits is strictly limited by the maximum ENOB of the digital PWM. Utilizing external, complex 24-bit ADC architectures will substantially degrade phase-noise performance through introduction of LCOs.

3. Incorporation of FDA techniques can improve output voltage resolution but may cause degradation of phase-noise performance through limit cycle oscillations within the cathode voltage unless blanking to a 14-bit word is performed.

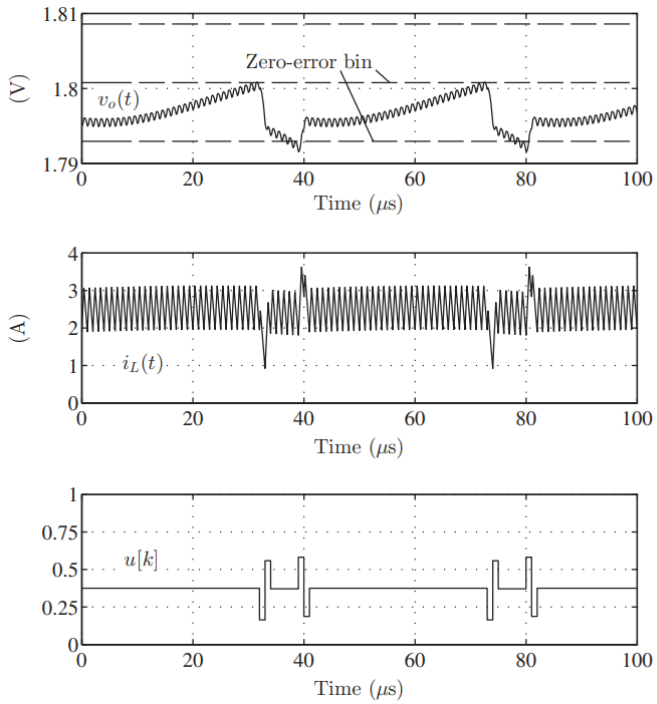

Fig.71: Limit Cycle Oscillation due to Coarse-Grained DPWM Duty Cycle Variations [133].

It can be concluded from the above results that the effectiveness of digital control in ultra-low-noise, high-voltage applications is severely restricted by the digital PWM resolution and avoidance of LCO. No amount of controller integral action will rectify this issue.

8.1.4 Time Delays

The presence of various delays within the system effects the achievable controller frequency response. Generally, these delays include both control and modulation delays. While delays are often considered undesirable, they do exhibit some benefits such as improved stability [134]. The control delay refers to the time interval between the sampling event and the instant that a digital modulator latches a corresponding control command output from the digital compensator. Such time delays should not exceed a fraction of the implemented switching frequency to not introduce significant phase-delay, which becomes more difficult as one approaches MHz levels of power conversion. Delay compensation techniques have been proposed to improve bandwidth in digital power supplies but requires topological modifications such as the interleaving of multiple out-of-phase switching stages [135]. Software compensation of time delays has been studied using linear extrapolation, which allowed bandwidth to be increased by two times [136], but switching frequency was limited to 10kHz. It is not known whether such techniques would be as applicable at 1MHz switching frequency where the delays are much more severe and influential regarding

system dynamics. Meeting this criterion often requires application-specific, optimized ADC systems, and the use of hardware-based controllers utilizing custom-integrated circuits.

A digital controller for a four-quadrant GaN-based tracking power supply proposed in [137] claims to have achieved a 100kHz bandwidth with a 1MHz switching frequency with an FPGA. In a DSP, assembly language functions may offer reduced control law execution time but will still often exceed that achievable with hardware-based implementations. Small-signal delays are introduced to the equation due to the sampled nature of signals within a digital modulator. The F2837xD is an example of a uniformly sampled PWM, whereby the modulating signal is sampled before comparing it to the carrier signal, and thus exhibits a nonzero delay between latching of the control command and generation of a corresponding modulating edge. Naturally sampled analogue based PWM systems exhibit no such modulation delay. As the ENOB increases, the required computational time is increased and the total number of samples per second throughput is reduced. Time-delay effects mimic the utilization a slow comparator in a purely analogue controlled supply which may not be acceptable when fast responses to rapidly changing parameters are required.

Digital controllers cannot replicate instantaneous reactions of analogue controllers. Conversion time has implications regarding controller bandwidth. In analogue controllers, output voltage is sampled every switching cycle, and the achievable switching frequency is limited only by the architecture of the implemented control chip. The maximum switching frequency of a digital implementation is further limited by the maximum number of samples/second before an input signal is no longer respectfully replicated without aliasing effects, described by the Nyquist criterion. Anti-aliasing and low-pass filters may offer some protection but require additional computational time. High performance microprocessors often have fast analogue-based comparators for implementation of peak-current mode control, but still suffer quantization effects due to the finite digital nature of the reference voltage.

8.2 APPENDIX B: TRANSFORMER DESIGN

As modern power converters move toward higher frequencies, modelling the loss mechanisms within the transformer becomes essential but increasingly complex. As core volume decreases substantially, the thermal resistance shows notable increases, such that much less power can be dissipated before thermal effects limit the design. Dowell's equations provide a mathematical representation regarding winding geometry impacts on the ratio of AC to DC winding resistance at a particular switching frequency. As the transformer solution size decreases, there may be substantial increases in the parasitic capacitances as the distance between windings is decreased, and achieving the proper level of isolation becomes extremely difficult. Creepage and clearance requirements are often a function of the switching frequency, due to the higher tendency for voltage to arc-over under high frequency conditions. In practice, the use of insulating compound with superior dielectric properties provides mitigation of stringent creepage and clearance distance requirements that would otherwise strictly limit achievable power density while preventing arc-over conditions between the windings.

8.2.1 Heat Transfer and Temperature Rise

Power is dissipated in the form of heat due to losses within the windings, core, and any dielectric insulating materials. Thermal effects of transformers include heat convection, conduction, and radiation [138]. The thermal resistances of the core and windings to ambient are related to the heat transfer coefficients of the core and winding materials and their geometry, as follows [139].

$$R_{T_{wa}} = \frac{1}{\lambda_w A_w} \quad (8.10) \qquad R_{T_{cv}} = \frac{1}{\lambda_{c_v} A_{c_v}} \quad (8.11) \qquad R_{T_{ch}} = \frac{1}{\lambda_{c_h} A_{c_h}} \quad (8.12)$$

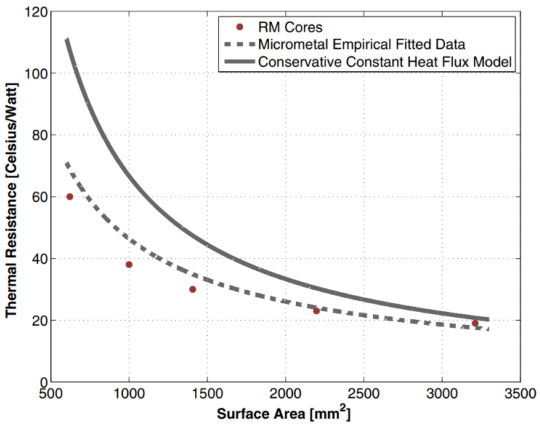

Fig.72: RM Core Thermal Resistances for Varying Surface Core Areas [140].

Where $R_{T_{wa}}$ is the thermal resistance of the windings and $R_{T_{cv}}/R_{T_{ch}}$ are the thermal resistances of the core vertical and horizontal surfaces, respectively. The values λ_w, λ_{c_v}, and λ_{c_h} are the respective heat transfer coefficients. The surface area of the windings and core are expressed as A_w, A_{c_v}, and A_{c_h}. The production of heat per unit volume varies across the transformer due to finite thermal conductivities, such that the rate of heat transfer varies at different positions within the assembly. Temperature rises impact transformer operation through increased AC and DC copper resistances, core losses, reduction of core saturation flux density, and degradation of isolating materials. As the core surface area decreases, the thermal resistance increases substantially, indicating that equivalent core loss across cores causes substantially higher temperature rise from ambient.

8.2.2 Core Loss Constraints

Updated models improve upon the general Steinmetz equation for core loss by extending the equation to allow application to non-sinusoidal waveforms [141], with further extensions allowing inclusion of duty cycle and temperature dependent effects [142]. Vorpérian suggested the use of simple fractal models to express anomalous residual losses in ferromagnetic with frequency and peak flux density, showing losses tend to be non-integer powers of the frequency of excitation [143]. Optimum core utilization involves selection of a specific optimum gap length, resulting in a specific effective permeability and energy storage capability. Three common, high power density transformer cores are given below:

	Core 1: RM8	*Core 2: ETD29/16/10*	*Core 3: PQ26/20*
Effective Volume (mm^3)	2440.0	5470.0	5470.0
Effective Length (mm)	38.4	72.0	45.0
Effective Area (mm^2)	63.0	76.0	121.0
Mass of Set (g)	13.0	28.0	30.0
Mean Length of Turn (mm)	42.0	52.8	56.0
Winding Width (mm)	8.6	19.4	8.8
Winding Area (mm^2)	30.9	97.0	33.0

Table 7: Comparative Core Characteristics for Typical High Power Density Transformer Shapes.

The required number of turns N_t for a given core operating with a peak operating flux density B_{op}:

$$N_t > \frac{E_t T_n}{B_{op} A_e} \qquad (8.13)$$

Where $E_t T_n$ is the volt-second product of the core and A_e is the effective ferrite core area. A frequency of 1MHz and advanced ferrite material 3F46 from Ferroxcube are considered to demonstrate limitations of such elevated switching frequencies, and parasitic capacitance is assumed to be incorporated in the switching topology such that core geometry and loss are considered as the only bottleneck. At 1MHz, with a peak flux density of 50mT and core temperature of 100°C. this material exhibits $150kW/m^3$ relative core loss density and therefore is the core loss limited peak flux density factor. The required primary turns ratios for three common, high density ferromagnetic cores is calculated below:

$$N_{t_1}(RM8) = \sim 17T \quad Nt_2(ETD29) = \sim 14T \quad Nt_3(PQ26) = \sim 9T$$

Gapped cores should be utilized since they significantly reduce the inductance factor tolerance, which is essential for resonant circuits and product-to-product consistency within the EPC. The air gap length should be kept small relative to the core height to minimize the effect of high intensity fringing effects which may cause substantial heating in the windings adjacent to the gap and generation of EMI that may interfere with sensitive feedback circuits [144]. Particularly in high frequency supplies, other loss mechanisms prevent optimum utilization of the given core. Winding area and achievable copper fill factor are substantially reduced with both shrinking core size in high voltage applications due to required insulation and high separation distances requirements. A reduced winding area substantially limits the implementable number of primary windings, and a corresponding amplification of core loss and temperature deviation from ambient if superior material is not utilized for the chosen frequency of excitation. The total core loss is related to the power loss density within the coreP_V and the core volume V_e:

$$P_C = P_V V_e \quad (8.14) \qquad P_{C_1} = 0.366W \quad P_{C_2} = P_{C_3} = 0.8205W$$

8.2.3 Winding Loss Constraints

The amount of winding loss within a transformer is often underestimated, particularly at elevated switching frequencies when AC losses are severe. The skin effect δ_{sk} [145] of a conductive layer, including the effects of porosity and the effect this phenomenon has on the current density J within the wire, is expressed below:

$$J = J_s e^{-\frac{d_w}{\delta sk}} \quad (8.15) \qquad \delta_{sk} = \sqrt{\frac{2\rho}{\omega \mu_o \sigma \eta}} \quad (8.16)$$

The porosity is defined as η. The factors σ and ρ are the conductivity and resistivity of the copper wire, respectively. This causes the current density within the conductor to decrease exponentially and become more localized within the outer diameter of the conductor. Proximity effect is of utmost importance in high power density transformers where the copper fill factor should be maximized and tends to be the limiting factor in the design. P. L. Dowell first proposed an enhanced method for calculating the effects of Eddy currents within transformer windings in 1966 [146], which explored how winding geometry impacted the ratio between AC and DC losses within conductors such that one could calculate the totality within a given arrangement with n_l layers:

$$P_d = b_w \sum_{i=1}^{n_l} \frac{l_i H_i^2}{h_i \eta_i \sigma} \left[\left(1 + \alpha_i^2\right) G_1(\Delta_i) - 4\alpha_i G_2(\Delta_i) \right] \quad (8.17)$$

$$G_1(\Delta_i) = \frac{\Delta_i (sinh2\Delta_i + sin2\Delta_i)}{cosh2\Delta_i - cos2\Delta_i} \quad (8.18) \qquad G_2(\Delta_i) = \frac{\Delta_i (sinh\Delta_i cos\Delta_i + cosh\Delta_i sin\Delta_i)}{cosh2\Delta_i - cos2\Delta_i} \quad (8.19)$$

Where l_i is the mean turn length of a layer, h_i is the height of a layer, and Δ_i is the normalised height of the layer relative to the skin depth h_i/δ_{sk}. The intensity of the magnetic field at the layer boundary, H_i, is dependent on the number of turns per layer, the total current of the conductors within the layer, and the winding breadth: $H_i = n_i I_i / b_w$. Finally, α_i is the ratio of the magnetic fields present on either side of a given winding layer. These effects can be normalised and into design curves that describe the effects of winding geometry on the ratio of AC/DC losses within conductors:

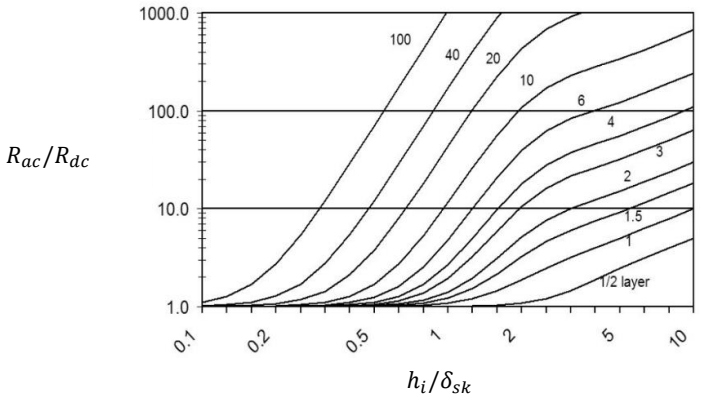

Fig.73: Normalized Dowell's Curves for AC/DC Winding Resistance with Differing Winding Configurations [147].

Optimal winding loss depends strongly on the number of layers and the normalised conductor thickness. At high frequencies associated with small skin depths, the conductor thickness should be minimized, often requiring flat copper foils or "Litz" wire. For a round conductor of diameter d_w, the normalized conductor thickness y_N is:

$$y_N = \frac{0.886 d_w}{\delta_{sk}} \quad (8.20)$$

At 1MHz, individual conductor diameters of 46AWG or 0.0398mm are typically recommended. C. R. Sullivan proposed an alternative method for calculation of winding proximity resistance factor F_r in [148], which shows how the magnitude of the additional AC frequency dependent loss was a function of the number turns N_t, of individual strands n_s, and their diameters d_w, but also on the winding breadth of the core b_c:

$$F_r = 1 + \frac{(\pi \omega \mu_0 N_t n_s)^2 d_w^6}{768(\rho b_c)^2} \quad (8.21)$$

A substantial increase in individual strands will be required as the processed RMS current is increased. New types of Litz wire pressed into thin rectangular profiles may offer substantially lower resistance factors through minimizing the winding layer height, while also allowing increased separation between primary and secondary windings which often causes substantial winding capacitance. A wider bobbin offers similar reductions in resistance factor.

8.2.4 Stray Capacitance Minimization

Although utilizing a single layer winding is often discussed regarding Dowell's equations and minimizing AC losses, this also has significant influence on the resultant winding capacitance and generation of complex EMI noise.

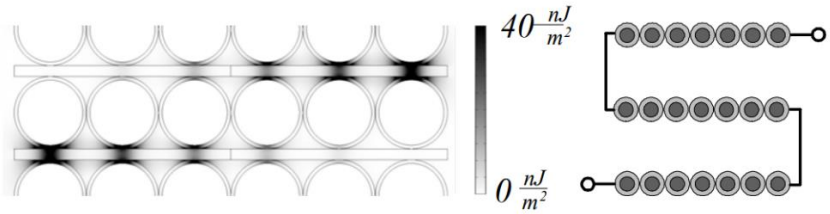

Fig.74: Energy Distribution of Multi-Layer Winding [149]

Energy distribution within high voltage windings mainly concentrates between two successive layers, with the energy between turns being substantially lower. The intra-winding capacitance is

severely impacted by the chosen winding geometry, and minimization of the electric field intensity and thus apparent parasitic capacitance involves pensive winding techniques. Such techniques also aim to minimize the energy storage E_S between adjacent conductive layers with assumed linear potential distributions, expressed as:

$$E_S = \frac{C_{tx}}{6}(U_s^2 + U_s U_t + U_t^2) \quad (8.22)$$

Where U_s and U_t are the potential differences between the conductive surfaces at the top and bottom of the implemented winding respectively. Minimizing the voltage gradients within the transformer for any given transformer capacitance C_{tx} substantially reduces the amount of electrostatic energy within the transformer structure. Commonly implemented winding architectures are shown below:

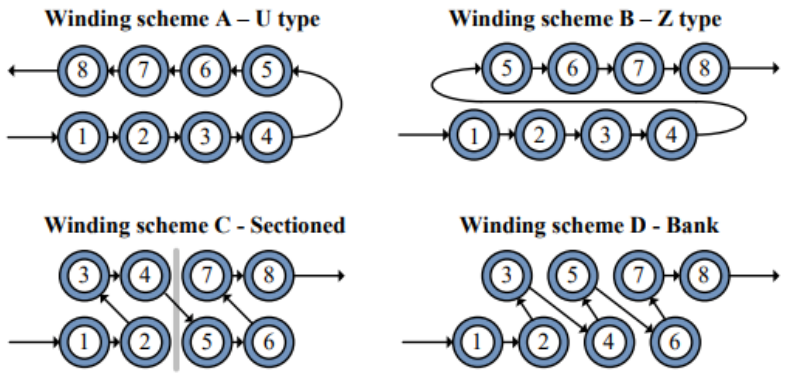

Fig.75: Commonly Implemented Transformer Winding Techniques [150].

Sectionalised and bank windings significantly decrease voltage gradients between layers and therefore are most appropriate when considering winding of high voltage transformers in TWT applications to enable optimization for high frequency power generation. It should be noted that sectionalised winding does require a custom bobbin, which impacts the achievable copper fill factor of the core impacting the achievable power density. To minimize generation of EMI from windings, one should place a grounded Faraday shield between the windings such that high frequency noise is decoupled from the low-noise output, while EMI can also be reduced through placement of the largest signal turn furthest away from the output ground. Optimising the transformer for minimum capacitance will result in a corresponding increase in leakage inductance, but assuming the power topology is able to accommodate such an increase, this may allow further power density optimization. Research has shown placement of a magnetic shunt between the transformer primary and secondary have shown notable increases in the achievable

leakage inductance, but quantification and measurement of the resultant parasitic capacitance has not been performed in currently available literature [151].

8.3 APPENDIX C: SIGNAL INTEGRITY

The final consideration is signal integrity, which includes design of the PCB regarding high di/dt switching loop area, circuit board parasitic magnitudes, shielding, grounding, and high coupling to sensitive feedback lines that include high impedance networks such as low-power operational amplifier circuits.

8.3.1 Mutual Inductance and Inductive Coupling

Mutual inductance and inductive coupling cause the separation of outward and return currents. The magnitude of the inductance created by a closed loop path is related to the loop area, significantly altering the equivalent AC impedance. Inductive coupling modelling is often utilized within printed circuit board spiral coils for inductive power transmission [152]. In most applications however, large areas enclosed by conductors produce extensive external magnetic fields, which may interact and interfere with neighbouring circuits causing unwanted coupling [153]. Large loop areas are themselves vulnerable to external magnetic field interactions. The induced voltage V_{ic} is related to the magnetic flux density B_{ic}, frequency of noise source ω_{ic}, and area of the signal loop A_{ic}:

$$V_{ic} = \omega_{ic} A_{ic} B_{ic} \quad (8.23)$$

The solution is to ensure that the impedance of the loops is minimized. However, creepage and clearance distances demand tracks be kept apart by a minimum amount determined by set international standards. Sensitive, low voltage feedback circuits should be placed as close as possible to the high voltage output to minimize the area of both the high frequency switching circuits and the sensitive DC feedback signals, which must be substantially free of induced noise.

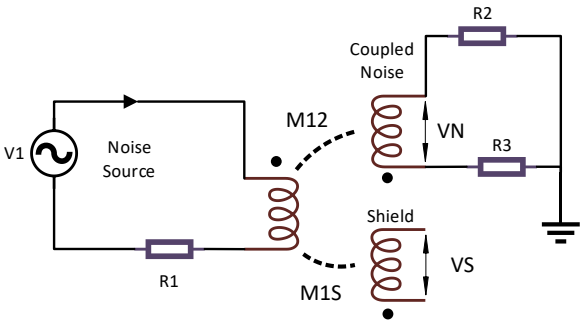

Fig.76: Coupled Noise due to Large Inductive Coupling Loop Areas.

This distance is dictated by the requirement for reinforced isolation between the high voltage output and any low-voltage area that must be considered safe under any combination of single-even fault conditions. In comparison to electrostatic shielding with Faraday shields, magnetic shielding is much more difficult to attenuate effectively. Some level of mitigation of noise generation due to inductive coupling can be achieved through inclusion of shielded non-magnetic screens [154], see (Fig.76). The magnitude of the magnetic flux density B_{ic} at a distance r_c from a round conductor carrying current I_r can be found through utilisation of the Biot-Savart Law for mutual inductive coupling:

$$B_{ic} = \frac{\mu I_r}{2\pi r_c} \qquad (8.24)$$

To minimize the effects of inductive coupling, it is prudent to ensure any sensitive feedback signals are also placed far away from any intense magnetic fields, such as those generated by the transformers within the EPC, further limiting the achievable power density of the solution. EMI generation from severe fringing field effects can be minimized by only implementing the optimum air gap required to achieve a designed inductance. Aggressive transient signals with short rise times result in noise signatures on adjacent lines which are a derivative of the aggressor current. The inductive noise generated will only appear synchronous with the switching current edge during signal transitions. This can easily be identified in sensitive feedback lines due to the settling of inductive crosstalk until it is below a particular measurement threshold. Substantially reducing the rise and fall-times of the signals in the power traces enables notable reductions in inductively coupled crosstalk.

8.3.2 PCB Stray Capacitance and Faraday Shielding

Capacitance is developed between any two conductors separated by a dielectric, including air and vacuum. A simple approximation for capacitance C_{px} in pF of area A_{px} separated by distance d_{px}:

$$C_{px} = \frac{0.00885\varepsilon_r A_{px}}{d_{px}} \qquad (8.25)$$

Even minute levels of capacitance influence circuit behaviour, particularly when the frequency of excitation, magnitude, and rise/fall-times of switching signals increases. Minimizing plate area, increasing separation distances, and utilizing high relative dielectric constant material does mitigate parasitic effects. A change in voltage in any conductor will cause an equivalent movement of charge within the other. Mathematically, the magnitude of voltage noise generation $V_{coupled}$ can be expressed as a function of the power circuit impedance Z_P, and the impedance caused by the parasitic circuit capacitances [155] when experiencing a voltage of magnitude V_N:

$$V_{coupled} = V_N \left(\frac{Z_P}{Z_P + \frac{1}{j\omega C_{px}}} \right) \qquad (8.26)$$

The coupled voltage becomes more severe as the frequency of excitation increases, due to a combination of decreases in the power supply impedance and increases in the impedance of the parasitic circuit capacitances. Utilization of power planes may be limited as one should also aim to minimize conductor area, despite power planes offering greater current carrying capability, heat dissipation, shorter current return paths, and improved decoupling characteristics. For transformers specifically, utilization of a grounded Faraday shield shows marked reductions in both the noise current generated from the power circuit impedance and thus coupled voltage appearing across it:

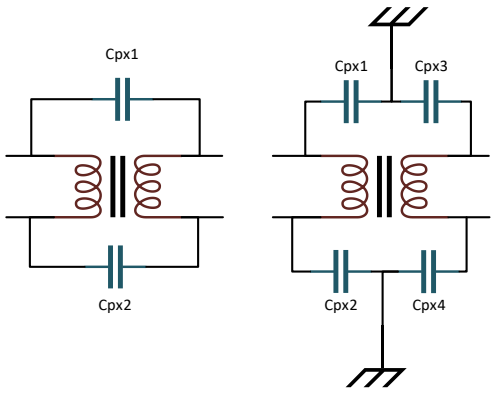

Fig.77: Inclusion of a Faraday Shield for Reducing Capacitive Coupling of Noise Voltage.

The net effect is decoupling of the noise voltage away from the power circuit impedance and towards a large, grounded conductor such as the chassis of an MPM. It is of utmost importance to ensure the connection diverts displacement current back to the source, without causing it to flow within sensitive parts of the circuit where conducted noise could be introduced due to the presence of grounding issues.

8.3.3 Grounding Issues

Signal return currents may flow in complex impedances that exist between two distinct grounding points, giving rise to voltage drops. Additional external currents may flow in this same path and generate uncorrelated noise voltage between these points. High current circuits within the same system may induce substantial noise within sensitive circuit regions elsewhere in the system if a ground loop is formed. Implementing ground connections with a "star" configuration, with each system having individual dedicated connections to the safety chassis ground plane, may alleviate these issues. Circular ground conductor patterns are particularly vulnerable to induced external magnetic fields such as those within the power transformer, which may interrupt the integrity of the implemented grounding. This may also be of concern with a hybrid converter approach, where a magnetic field in either converter may disrupt the grounding in the other. The issue of ground loops and generation of noise within a ground has shown improvement with advanced techniques such as utilization of ground isolation amplifiers, which allow minimization of ground error voltages between stages by rejecting common mode noise through differential signalling techniques.

8.3.4 Noise Susceptibility in High Circuit Impedances

In the feedback path, there are typically analogue based components for signal conditioning before they are processed by digital or analogue-based controllers such as operational amplifiers which incorporate higher value resistors to limit power, making them much more susceptible to the effects of externally induced radiated and conducted noise. The feedback path consists of 10 series connected 10MΩ resistors to minimize power dissipation and improve safety during any single component failures. Mutual inductance and stray capacitance can easily be of the order where significant conduction paths are created for noise penetration to occur within this path. Despite these signals being ideally low-noise DC, this assumption can no longer be made where such coupling effects exist if routing occurs near high radiated noise sources. For mitigation of this noise, utilization of operational amplifiers with EMI hardened inputs can be utilized, but these are

typically of limited bandwidth, which significantly effects the gain-phase characteristics of the feedback path, substantially limiting achievable bandwidth. For more information on high-frequency effects in PCBs, refer to [156, 157, 158, 159].

8.4 SUMMARY

The implementation of WBG devices is fully established at frequencies of 1MHz+ with little issue and is not a significant bottleneck when optimizing power density. For generation of ultra-low-noise outputs, analogue controllers offer unmatched performance due to their infinite resolution and lack of quantization effects. To ensure stability and avoidance of LCO, one must ensure that the resolution of the DPWM exceeds that of the implemented ADC configuration. As a result, implementation of external high-resolution ADCs provides no additional benefit without corresponding improvements in the DPWM quantization. External hardware such as FDAs offer common mode noise rejection and slightly improved resolution but remains constrained by the DPWM resolution.

Ferrite materials have been shown to exhibit low loss at high frequencies, assuming the peak flux density is limited to a value that constrains the core temperature. As the effective core surface area reduces, it becomes increasingly difficult to achieve a low integral number of primary turns for a given volt-second product without reaching thermal limitations of the core. The core volume limits the amount of power dissipation that is achievable before thermal limitations are reached, which makes optimum power balancing between the windings and the core near impossible as solution size reduces. Encapsulation of the transformer structure offers some resolve through insertion of material with superior dielectric properties.

Dowell's equations demonstrate that winding loss is minimized through utilizing the minimum number of layers of substantially low height which may require specialized flat wire composed of multiple individual strands with diameter much less than the penetration depth at the excitation frequency and custom, wide bobbins. Such solutions may lose effectiveness as frequencies exceed 1MHz+ when the thickness of individual strand insulation approaches the copper strand diameter. As current density increases such as within the high-power transformer, the wires demand a substantially higher overall diameter to minimize both DC and AC resistance and avoid thermal issues, which may require either reduced number of primary turns or a larger core winding area to accommodate them. This results in either substantially increased core loss and heat dissipation for a constant core geometry or alternatively the incorporation of a larger core. Either solution prevents optimum utilization of the ferrite core and has strong implications regarding the

achievable transformer power density. Core geometry is important, with cores of similar weight and volume displaying notable differences in their winding width and available winding window area, allowing reduction in winding loss, and thus enhanced power loss balancing. Utilizing very low transformer turns ratios does not offer any solace since this leads to both higher volt-seconds within the primary and higher current demand in the secondary windings.

This would require triple insulated wire and increased strand count conductors in the primary and secondary, respectively. Diode conduction angles will substantially decrease as the required voltage magnitude slew rate increases with low transformer turns ratios, further reducing the achievable output voltage achievable for a given switching frequency. Specialist winding techniques such as bank windings minimize electrostatic potentials between winding layers and thus should be incorporated to minimize parasitic effects without requiring custom bobbins, and noise can be minimized by incorporating electrostatic Faraday shields and placing large magnitude signals away from output ground.

Pollution of low-noise precision signals is of great concern as switching frequency and power density increase. Even small levels of parasitic capacitance between closely spaced traces or inductance from large loop areas may cause noise coupling into sensitive feedback lines. Electrostatic shielding of the transformer and magnetic shielding of feedback signals offer some respite of these effects, but low-pass filter circuits or EMI hardened operational amplifiers may be required, which are detrimental to the achievable controller bandwidth. Integrity of the implemented grounding system is quintessential to avoid uncorrelated noise generation between high current circuits through the formation of ground loops. Inductive and capacitive noise generation is of particular concern when implementing high impedance circuits and feedback paths, which are essential in high voltage power supplies considering the required step-down ratio of the high voltage outputs. Low-power operational amplifiers, used for signal conditioning before being processed by analogue or digital circuits, also suffer the same issues.