Condition Monitoring Techniques for Multi-chip Silicon IGBT Modules

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Abstract

Multi-chip Insulated Gate Bipolar Transistor (mIGBT) power modules (PMs) are broadly utilised for power system due to their high-voltage and high-current capabilities. However, mIGBT modules are fragile components and therefore prone to failures. For that reason, research focuses on monitoring the conditions of mIGBT PMs aiming to prevent catastrophic failure. Detecting the virtual junction temperature T_{vj} and bond wire lift-off are the two most common techniques in mIGBT condition monitoring. Thus, this research focuses on the condition monitoring of bond wire lift-off and T_{vj}.

Many techniques have been proposed for T_{vj} estimation. However, most of the existing techniques are either focused on single chip Insulated Gate Bipolar Transistor (IGBT) module or assuming homogeneous temperature distribution in mIGBTs which is not the case in practical application. Therefore, a comprehensive study was carried out on an mIGBT to investigate the impact of spatial distribution of temperature (SDoT) on existing T_{vj} estimation techniques.

Power converters are subjected to regular maintenance. During maintenance, various parameters of the converter are tested. Detailed health conditions on mIGBT PMs are so far not recorded. This thesis describes a technique to determine the health condition of bond wires when mIGBT PMs are offline. The technique requires a minor modification on mIGBT PMs that allows simultaneous measurement of the on-state voltage across the chips and the terminals of a PM. The proposed technique is able to detect early bond wire lift-offs as well as locate any lifted bond wire. To the author's knowledge, there has been no work published that addresses the location of lifted bond wires in mIGBT PMs.

In general, condition monitoring techniques are influenced by T_{vj} as well as bond wire condition. Thus, two or more techniques are required to determine both parameters online. In this thesis, a novel technique is proposed to decouple the influence between the bond wire lift-off and T_{vj}. The proposed technique injects high-frequency and low-power signals to the gate-emitter circuitry of an mIGBT PM. The frequency response of the gate-emitter impedance is analysed to determine the root cause. This technique can be embedded in a gate driver circuit and thereby monitor the conditions of mIGBT PMs during the operation of a power converter.

Keywords - bond-wire lift-off, T_{vj} estimation, multi-chip silicon IGBT modules, on-state voltage, signal sweeping

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Abbreviations

AE	Auxiliary Emitter
C	Collector
CMU	Condition Monitoring Unit
CTE	Coefficient of Thermal Expansion
DBC	Direct Bonded Copper
DUT	Device Under Test
E	Emitter
G	Gate
HTD	Homogeneous Temperature Distribution
IGBT	Insulated Gate Bipolar Transistor
IR	Infrared
ITD	Inhomogeneous Temperature Distribution
KE	Kelvin Emitter
mIGBT	Multi-chip IGBT
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient
PE	Power Emitter
PM	Power Module
PN Gen	Pseudo-Noise digital sequence Generator
PWM	Pulse Width Modulation
RFID	Radio-Frequency Identification
RLC	Resistor-Inductor-Capacitor
RTD	Resistive Temperature Detector
SDoT	Spatial Distribution of Temperature
SHE	Self-Heating Effect
SOA	Safe Operating Area
SSTDR	Spread Spectrum Time Domain Reflectometry
TDDB	Time-Dependent Dielectric Breakdown
TDR	Time Domain Reflectometry
TSEP	Temperature Sensitive Electrical Parameter

Symbols

A_C	The size of p region
a(t)	Envelope of the sweep signal
C	Capacitance
C_{GC}	Gate-collector capacitance
C_{GE}	Gate-emitter capacitance
C_{ies}	Input capacitance
C_O	Chargge extraction capacitance
Cox	Gate oxide capacitance
D_a	Ambipolar diffusion coefficient
dI_C / dt	Collector current slope
D_{nE}	Diffusion coefficient for minority carries in the p region
dV_{CE} / dt	Collector-emitter voltage slope
g_m	Transconductance
I_C	Collector-emitter current
$I_{C(load)}$	Load current
$I_{C(sense)}$	Sense current
$I_{C(tail)}$	Tail current of I_C
I_G	Gate current
$I_{G(peak)}$	Peak gate current
i_R	Current flowing through the resistor
J_C	collector current density
k	Boltzmann's constant
L	Inductance
L_a	Ambipolar diffusion length in the N-base region
L_{nE}	Diffusion length for electrons in the p+ collector region
L_σ	Parasitic inductor between power emitter and auxiliary emitter
N_{AE}	The minority carrier doping concentration
n_i	Intrinsic carrier concentration
p	The cell pitch of the n-drift region
p_0	Initial concentration of holes at the edge of the space charge region

q	Charge
R	Resistance
$R_{DS(on)}$	On-state resistance of MOSFET
R_{Ee}	Resistance across power emitter and auxiliary emitter
R_{Ee}	Equivalent resistance across power emitter and auxiliary emitter
R_g	Gate resistor including the external gate resistor and internal gate resistor
$R_{G(ext)}$	External gate resistor
$R_{G(int)}$	Internal gate resistor
$R_{G(int-chip)}$	Internal gate resistance of the IGBT chip
R_{wire}	Equivalent resistance of all the bond wires
$R_{wire@25°C}$	Equivalent resistance of bond wires at 25 °C
S_1	Surface area of Chip1
S_2	Surface area of Chip2
S_3	Surface area of Chip3
T	Absolute temperature
$T_{C1(avg)}$	average temperature within the surface of Chip1
$T_{C1(max)}$	maximum temperature within the surface of Chip1
$T_{C1(min)}$	minimum temperature within the surface of Chip1
$T_{C2(avg)}$	average temperature within the surface of Chip2
$T_{C2(max)}$	maximum temperature within the surface of Chip2
$T_{C2(min)}$	minimum temperature within the surface of Chip2
$T_{C3(avg)}$	average temperature within the surface of Chip3
$T_{C3(max)}$	maximum temperature within the surface of Chip3
$T_{C3(min)}$	minimum temperature within the surface of Chip3
$t_{d(off)}$	Turn-off delay
$t_{d(on)}$	Turn-on delay
T_j	Junction temperature
t_{Miller}	Miller plateau width
$T_{pre(VCE)}$	Temperature estimated by $V_{CE(on)}$
$T_{pre(VCK1)}$	Temperature estimated by $V_{CK1(on)}$
$T_{pre(VCK2)}$	Temperature estimated by $V_{CK2(on)}$
$T_{pre(VCK3)}$	Temperature estimated by $V_{CK3(on)}$

t_{Pulse}	Collector current pulse width
T_{vj}	Virtual Junction Temperature
u_C	Voltage across the capacitor
u_L	Voltage across the inductor
$V_{CE(on)}$	On-state voltage drop
$V_{CE(on\text{-}load)}$	On-state voltage drop at load current
$V_{CE(on\text{-}sense)}$	On-state voltage drop at sensor current
$V_{CE(peak)}$	Peak of the collector-emitter voltage during the turn-off transient
$V_{CK(on)}$	On-state voltage across collector and Kelvin emitter
$V_{CK(on\text{-}tile)}$	On-state voltage of each DBC tile
$V_{CK1(on)}$	On-state voltage of Chip1
$V_{CK2(on)}$	On-state voltage of Chip2
$V_{CK3(on)}$	On-state voltage of Chip3
V_{Ee}	Voltage drop across power emitter and auxiliary emitter
V_{FB}	Flat-band voltage
V_{GE}	Gate-emitter voltage
$V_{GE(Miller)}$	Miller plateau voltage
$V_{GE(off)}$	Gate-emitter voltage at off-state
$V_{GE(on)}$	Gate-emitter voltage at on-state
$V_{GE(th)}$	Threshold voltage
$V_{Incident}$	Incident signal
$V_{pre(th)}$	Pre-threshold voltage
$V_{Reflected}$	Reflected signal
V_{wire}	Voltage across the bond wires
W_N	The width of the N-drift region
Z_{GE}	Impedance of gate-emitter circuit
$Z_{GE(Imag)}$	Imaginary part of the gate-emitter impedance
$Z_{GE(Real)}$	Real part of the gate-emitter impedance
$\Delta^2 T_{S(avg)}$	The maximum temperature difference amongst $\Delta T_{C1(avg)}$, $\Delta T_{C2(avg)}$, $\Delta T_{C3(avg)}$
$\Delta^2 T_{S(max)}$	The maximum temperature difference amongst $\Delta T_{C1(max)}$, $\Delta T_{C2(max)}$, $\Delta T_{C3(max)}$
$\Delta^2 T_{S(min)}$	The maximum temperature difference amongst $\Delta T_{C1(min)}$, $\Delta T_{C2(min)}$, $\Delta T_{C3(min)}$
$\Delta T_{(avg)}$	Average temperature swing between t_0 and t_2

$\Delta T_{(max)}$	Maximum temperature swing between t_0 and t_2
$\Delta T_{(min)}$	Minimum temperature swing between t_0 and t_2
ΔT_{pre}	The estimated temperature difference
ΔT_{pre1}	Temperature difference between $T_{pre(VCK1)}$ and $T_{pre(VCE)}$
ΔT_{pre2}	Temperature difference between $T_{pre(VCK2)}$ and $T_{pre(VCE)}$
ΔT_{pre3}	Temperature difference between $T_{pre(VCK3)}$ and $T_{pre(VCE)}$
β	Temperature coefficient of bond wires
β_{PNP}	Current gain of the internal PNP bipolar transistor
μ	The absolute magnetic permeability of the conductor
ε_{ox}	Dielectric constants of oxide
ε_{si}	Dielectric constants of silicon
θ(t)	Phase of the sweep signal
Γ	Reflected coefficient

Chapter 1. Introduction

1.1. **Background**

Over the past years, there is drastic increment in electricity demand especially that generated from clean/green sources. For instance, Figure 1.1a depicts the exponential increase in electricity generation from renewable resources over the last three decades [1, 2]. The rapid increment of electricity generation elevates the requirement of the power handling capability of semiconductor switches, which are essential for any power converter. Power handling capabilities of power semiconductors are often expressed through maximum voltage and current levels. Figure 1.1b illustrates the electrical boundaries for traditional silicon power semiconductors [3]. Among them is the IGBT, which is one of the most common semiconductor types in power electronics because of its high current/voltage capabilities and low gate driver requirements [4-6]. To achieve the high current capabilities shown in Figure 1.1b, semiconductor manufacturers employ a multi-chip packaging technique, which complements the power density limitation of the material [7].

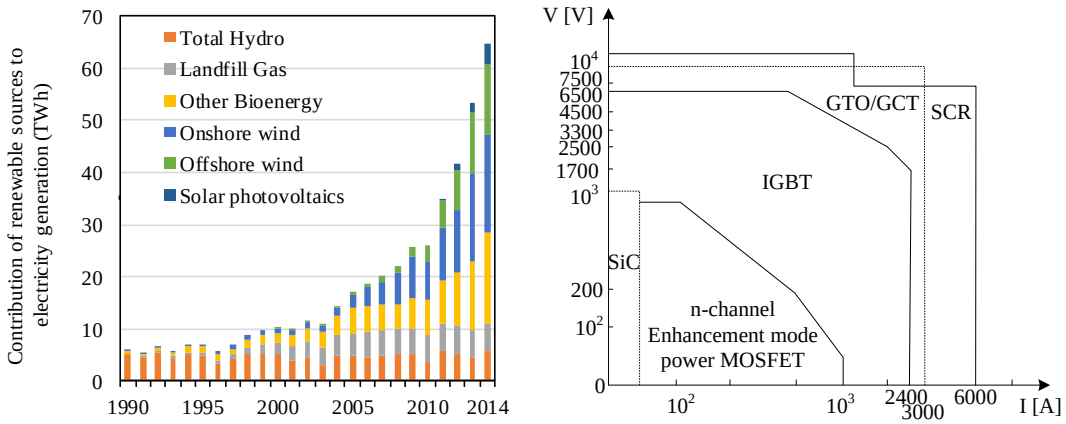
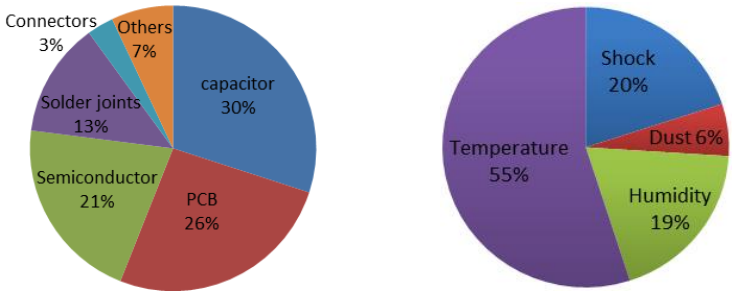


Figure 1.1 (a) Electricity generation by main renewable sources since 1990 [1, 2], (b) Electrical voltage and current ratings for silicon power semiconductor switches [3, 8]. GTO: Gate Turn-off Thyristor; GCT: Gate Commutated Turn-off Thyristor; SCR: Silicon-Controlled Rectifier.

Power semiconductor devices are indispensable elements of power systems. However, it has been stated in the literature that power semiconductor devices such as IGBT power modules are one of the most fragile components in power systems with a 21 % failure rate as shown in Figure 1.2a [9]. One of the main contributors that is responsible for the failure is the temperature and more specifically the temperature swing that causes mechanical stress within the different

layers that power modules are made of. Figure 1.2b shows that with 55% temperature is the main failure driver [10, 11] followed by vibration and shock, about 20% and humidity and moisture, about 19%. It has also been shown that for every 10°C increase in operational temperature, the failure rate nearly doubles [4].



(a) (b)

Figure 1.2 (a) Failure distribution in power systems [9]. (b) Failure drivers in electronic equipment [10, 11].

The reliability of these devices is critical. Unexpected failures lead to costly repairs and income loss in energy generation. For instance, according to the report in [12], the operation and maintenance fees are about 18% of the total cost of an offshore wind farm, which is a tremendous cost contributor throughout the lifespan of a wind farm. Therefore, lots of studies have focused on fault prognosis and diagnosis for IGBT modules to cut down unexpected failures, reduce maintenance costs and improve the reliability.

1.2. **Fundamentals of the IGBT power module**

1.2.1. Structure of the wire-bond IGBT module

Despite the development of advanced packages, wire-bond IGBT PMs are still the most common package on account of the low cost and excellent compatibility. Therefore, the research in this thesis focuses on wire-bond IGBT PMs. Figure 1.3 depicts the package of a standard half-bridge IGBT PM. The direct bonded copper (DBC) substrate is soldered on the base plate. The DBC substrate consists of three layers: one ceramic substrate layer (Al_2O_3 or AlN) sandwiched by two copper layers. The DBC substrate provides a thermal path for the cooling system as well as electrical insulation between the PM and the cooling system.

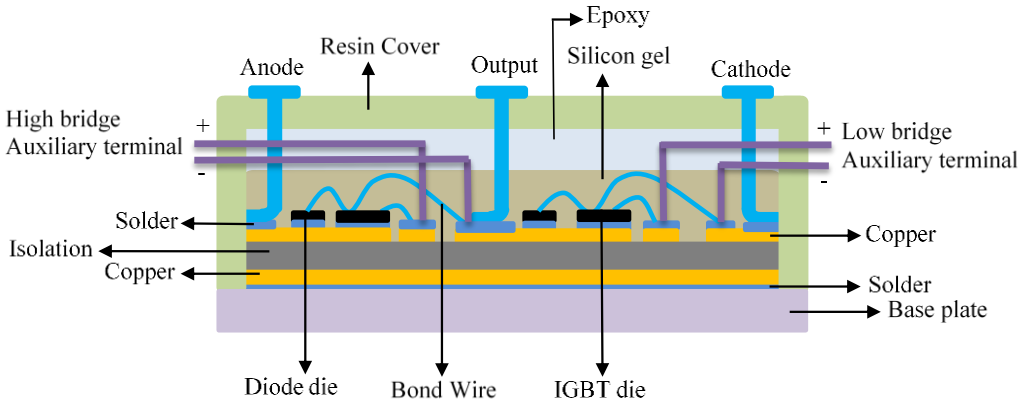


Figure 1.3 Package structure of a standard IGBT PM [13].

IGBT and diode chips are soldered on the top of the DBC substrate. The two sides of the IGBT chips are the two power ends. The end directly connected to the copper layer of the DBC substrate is the collector (C) of the IGBT. The other side is the emitter (E), which is connected to the DBC substrate via bond wires. In the case of mIGBT PM, there are several IGBT chips in parallel and each chip has a number of bond wires sharing the current that flows through the chip.

The resin cover is mounted on the base plate to hold the terminal leads and to house the PM. In general, silicone gel is filled in the PM to provide better insulation, mechanical protection, thermal conductivity and protection against contamination.

1.2.2. Failure modes

IGBT PM is a fragile component and fails due to various reasons throughout its lifespan. Figure 1.4 depicts the change of failure rate over time. In early failure stage, the failure rate is very high but drops sharply over time. Failures are mainly caused by pre-existing defects during manufacturing or human errors. These failures can be eliminated by proper screening or by paying attention while handling PMs. In the second stage, the failure rates stay very low. Random failures may occur suddenly due to excessive electrical and thermal stress. Failures during wear-out stage are caused by deterioration or ageing of PMs. They are predictable and can be prevented by appropriate maintenance. Therefore, research concentrates on the primary failure modes of the IGBT PMs during this stage. Failures can be divided into chip-related failure modes and package-related failure modes.

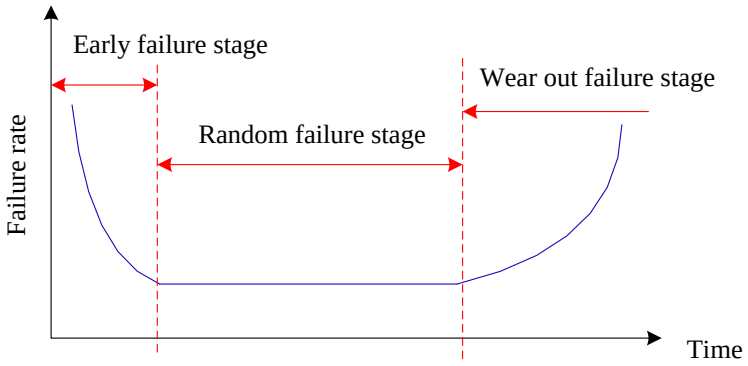


Figure 1.4 Time-dependent change in failure rate for PMs.

1.2.2.1. Chip-related failure modes

There are mainly three different chip-related failure modes: Gate oxide degradation, time-dependent dielectric breakdown (TDDB), safe operating area (SOA) failures, and brittle cracks.

Gate oxide degradation is caused by hot carriers which are highly charged electrons generated by high electric fields [14]. These hot carriers are interacting with the silicon dioxide (SiO2). They are either trapped in the silicon dioxide or in the interface between the silicon and SiO2, resulting in charge trap and interface state generation [15, 16]. This is also referred to as hot carrier injection. Hot carrier injection will lead to TDDB and the mitigation and degradation of semiconductors.

TDDB is induced by SiO_2 oxidation barrier deterioration under normal conditions [14]. SiO_2 oxidation barrier deterioration will lead to gate oxide breakdown, which will result in a loss of gate control eventually. TDDB failures are reliability issues.

SOA failures include overvoltage, overcurrent, electrostatic discharge and overheat. Overvoltage, overcurrent and fast *dI/dt* will lead to excessive heat dissipation, which will result in thermal damage. In addition, fast *dV/dt* may cause unexpected turn-on of the device. Because of the gate-emitter capacitor C_{GE}, high *dV/dt* will lead to large current flowing through the gate-emitter circuitry which will result in latch-up. Electrostatic discharge, which may be caused by an inappropriate way of handling the module, can partially puncture the gate oxide, which will result in loss of gate control and eventually lead to burnout failure [16]. The SOA failures are categorised as robustness related issues.

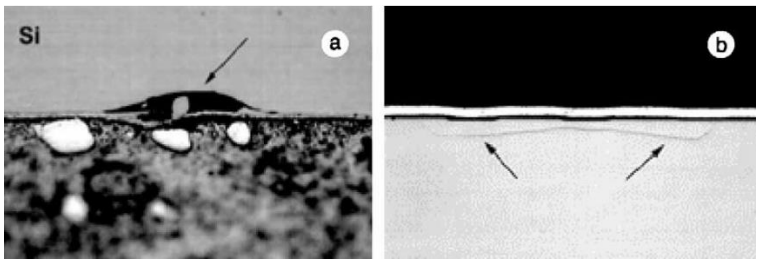


Figure 1.5 Brittle crack [17]: (a) Notch due to diamond sawing in a silicon chip, (b) Crack in silicon chip due to bending stress in the base plate.

Brittle cracks in an IGBT chip may cause short circuit. Figure 1.5 shows a crack in a silicon chip caused by perennial bending stress in the base plate. Brittle cracks are also reliability issues.

1.2.2.2. Package-related failure modes

Compared with chip-related failures, package-related failures are challenging and likely to be predicted because package related failures are caused by the thermal effect during power cycling and are developed gradually over time. Because the PM is constructed by different layers with different coefficients of thermal expansion (CTEs) as shown in Table 1.1, the mismatch of CTEs between the adjacent layers will lead to friction and dislocation. There are mainly three package-related failure modes: bond wire fatigue, solder layer deterioration and metallisation reconstruction. Bond wire fatigue and solder fatigue are two primary failure modes among them.

Table 1.1 Materials and CTEs for different parts [13, 17]

Parts	Material	CTE (ppm/°C)
Bond wire	Al	22
Chip metallisation	Al	22
Chip	Si	3
Copper layer	Cu	16.5
Isolation substrate	Al_2O_3	7
	AlN	4
Base plate	Copper	16.5
	AlSiC	8

(1) Bond wire fatigue

The difference in CTEs between IGBT chips and bond wires is the most significant; hence, bond wire fatigue is the most likely failure to happen during thermal cycling. There are two types of bond wire fatigue, namely, bond wire lift-off and bond wire heel cracking [17, 18]. During power cycling, change of yield strength causes elongations and contractions between IGBT chip and bond wires. With the continuance of power cycling, lift-off will initiate at the centre of the solder joint and propagate underneath until lift-off [17, 18]. The residence strength during soldering is another reason for the solder degradation. Since emitter bond wire carries load current, it suffers more severe power cycling compared with gate bond wire. Therefore, emitter bond wire lift-off is the primary failure mode.

Bond wire heel cracking rarely occurs in advanced IGBT PMs [13]. However, it does occur after a long endurance test. Because of the thermal-mechanical effect, expansions and contractions under temperature cycles lead to the flexure fatigue. Some heel cracks occur due to the shear stress from the bond wire coating layer.

(2) Solder layer deterioration

Solder layer deterioration includes solder fatigue and solder voids that mainly appear in the solder layer between the DBC substrate and base plate, where there is maximum temperature swing and the largest lateral dimensions. Solder fatigue will change the thermal resistance of the package and may lead to open circuit or high resistive path. Solder material also influences the solder fatigue mechanism. Typically, solder voids increase with the number of thermal cycles. Large solder voids will lead to dissipation performance degradation. Small solder voids will affect the overall thermal resistance of the multi-layer package [19].

(3) Metallisation reconstruction

Metallisation reconstruction mainly occurs on the chip metallisation. To release the thermal stress induced by thermal cycling, diffusion creeps, grain boundary sliding, or plastic deformation occur depending on the temperature swing and the stress amplitude. If the IGBT device is operated cyclically at maximum junction temperatures T_j, stress relaxation occurs mainly by plastic deformation. Metallisation reconstruction reduces the effective connection area and results in sheet resistance increment over time [17, 18, 20].

Typical failure modes are summarised in Table 1.2. Some of the failure modes may happen randomly or suddenly, which makes them unpredictable or unpreventable, such as exceeding SOA and brittle cracks. These failure modes are referred to as random failures. Other failure modes are caused by deterioration over time, which are called wear-out failures. Table 1.2 depicts the types and causes of typical failure modes. Random failures will lead to more severe effects compared with wear-out failures. However, wear-out failure is more of a concern because its influence can be restrained by maintenance before breakdown.

Table 1.2 Summary of the typical failure modes

Failure modes		Type	Stress
Chip failure	Gate oxide degradation	Random/Wear-out	Electrical
	TDDB	Wear-out	Electrical
	Exceeding SOA	Random	Electrical-thermal
	Brittle cracks	Random/Wear-out	Mechanical-thermal
Package failure	Bond wire fatigue	Wear-out	Thermal-mechanical
	Metallisation reconstruction	Wear-out	Thermal
	Solder fatigue, solder voids	Wear-out	Thermal

1.2.3. Condition monitoring for IGBT modules

Condition monitoring is the process of measuring the condition parameters of the device under test (DUT) to recognise a significant change which is an indicator of an evolving fault. In this thesis, the conditions of the IGBT PMs are divided into working conditions and ageing conditions. The monitoring of these conditions assists in the reliability improvement of IGBT PMs.

The conditions of IGBT PMs are shown in Figure 1.6. The working conditions include the forward blocking voltage V_{CE}, collector current I_C, the switching frequency f_{switch}, the circumstance conditions offered by the cooling system, environmental conditions like humidity, and so on. Ageing conditions mainly cover wear-out failure modes such as bond wire failure, solder degradation and metallisation reconstruction.

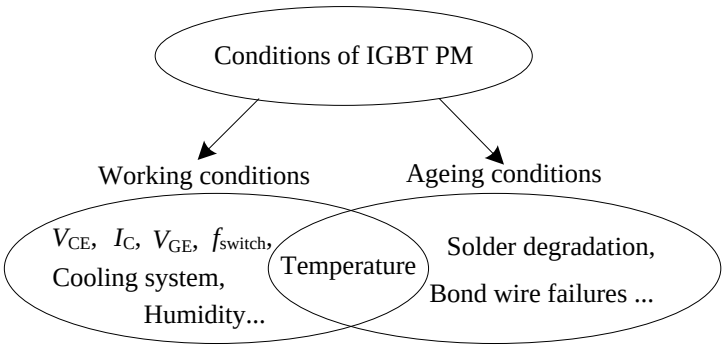


Figure 1.6 Conditions of an IGBT PM.

Even though temperature T_j does not directly reflect the ageing condition of the PM, T_j is one of the main factors and it is responsible for 55% of the failure in power electronics [11, 21]. Furthermore, for every 10 °C increment in average temperature, the failure rate nearly doubles [22]. Additionally, T_j is an essential parameter to estimate the thermal path degradation. Therefore, T_j is listed as a shared element between working conditions and ageing conditions in Figure 1.6.

Condition monitoring techniques aim to improve the reliability of IGBT modules and assist in identifying early failures that can cut down maintenance cost, especially for offshore wind power applications. In this thesis, T_j and bond wire lift-off are the major research interests.

1.3. **Objectives of the thesis**

Over the last two decades, lots of studies have been concentrated on condition monitoring for IGBT PMs to improve their reliability and cut down cost and downtime in case of failures. T_j and bond wire conditions are two of the major indicators of concern regarding condition assessment. However, most of the techniques for T_j monitoring are proposed on single-chip IGBT or mIGBT with uniform temperature distribution, which is rare in field application. Even though research on bond wire failure diagnosis is flourishing, the techniques proposed are generally influenced by T_j as well. Therefore, two or more tests or parameters have to be applied to assess the bond wire state. Furthermore, most of the techniques have not been developed for commercial applications.

Thus, the main objectives of this research are as follows:

First, to evaluate the thermal profile of an mIGBT module during operation, investigate the influence of thermal distribution regarding T_j estimation and identify the suitable technique for T_j estimation.

Second, to develop an offline monitoring technique for bond wire failure diagnosis in mIGBTs, aiming to provide an application-oriented approach for health monitoring during maintenance.

Third, to provide an applicable online method to decouple the influence of T_{vj} and bond wire failure and simplify the monitoring procedure.

1.4. **Thesis outline**

This thesis consists of seven chapters and is structured as follows.

Chapter 1 contains an introduction of the research background. The research objectives are also discussed, followed by the thesis outline and a summary of the contribution.

In Chapter 2, published techniques regarding the estimation of T_j and bond wire state are reviewed and summarised. A comparison is conducted of different techniques to comprehend their features. Moreover, the corresponding research gaps are examined.

Chapter 3 studies the virtual junction temperature T_{vj} in the mIGBT PM. Power cycling tests are carried out to investigate SDoT in mIGBT PM. Afterwards, the research extends to the impact of SDoT on T_{vj} estimation. Experimental tests are conducted at both homogeneous temperature distribution (HTD) condition and inhomogeneous temperature distribution (ITD) condition. The results are compared to appraise the feasibility of the existing techniques regarding T_{vj} estimation.

A novel offline technique is proposed in Chapter 4 to detect the bond wire lift-off in mIGBTs. The technique is based on the on-state voltage of the IGBT switch and IGBT chip. First, the principle of the proposed technique is explained. Next, the operation of the proposed technique is illustrated on two mIGBT modules with dissimilar packages to evaluate the effectiveness of the technique. Finally, the influence of the bond wire failure has also been evaluated regarding the collector current distribution and thermal distribution.

A condition monitoring unit (CMU) is constructed in Chapter 5 to implement the proposed technique in Chapter 4. The design of the hardware prototype and experimental results are presented in this chapter. The experimental results demonstrate that the CMU can effectively detect bond wire failure.

In Chapter 6, an applicable online technique is proposed to decouple the influence of bond wire lift-off and T_{vj}. The proposed approach relies on injecting sweep signal across the gate and emitter terminals of an unbiased IGBT module. In the beginning, the influence of bond wire lift-off and T_{vj} is discussed. A small signal model for the gate-emitter circuit is built up to implement the technique in the simulation. Practical tests are subsequently conducted and results are used to verify the proposed technique and demonstrate the monitoring procedure.

Chapter 7 is the conclusion of the thesis. It highlights the research outcome and reveals the potential research areas to extend the current findings.

1.5. **Contribution to knowledge and industrial world**

The techniques and findings proposed in this research are novel and original. They are listed below.

- The SDoT within a multi-chip IGBT module has been researched on both the chip level and switch level. Significant SDoT is observed during the power cycling test. The research is then extended to investigate the impact of the SDoT on techniques for T_{vj} estimation in mIGBT PMs.
- A new offline technique is proposed to detect the bond wire lift-off in mIGBTs. Compared with existing techniques, the proposed technique can not only identify the lift-offs at an earlier stage but also locate the lifted bond wire. Furthermore, the technique can appraise the current redistribution after the bond wire fault.
- An CMU prototype is constructed to implement the offline technique. The CMU can be applied during the maintenance stage, which can detect the earlier stage failure indicators and provide a health condition estimation for field devices.
- A novel technique is proposed in this thesis that can decouple the influence of bond wire failures and T_{vj}. The bond wire conditions and T_{vj} can then be extracted within one test. Last but not least, this technique is applicable online.

Publications about the PhD research are presented below.

[1] C. Chen, V. Pickert, M. Al-Greer, et al., "Signal Sweeping Technique to Decouple the Influence of Junction Temperature and Bondwire Lift-off in Condition Monitoring for Multi-chip IGBT Modules," in CIPS 2018; 10th International Conference on Integrated Power Electronics Systems, 2018, pp. 1-6.

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Contributed publications:

[1] L. Xiang, C. Cuili, M. Al-Greer, V. Pickert, and C. Tsimenidis, "Signal processing technique for detecting chip temperature of SiC MOSFET devices using high frequency signal injection method," in 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia), 2017, pp. 226-230.

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[3] R. Mandeya, C. Chen, V. Pickert, R. T. Naayagi and B. Ji, "Gate-emitter Pre-threshold Voltage as a Health Sensitive Parameter for IGBT Chip Failure Monitoring in High Voltage Multichip IGBT Power Modules," in IEEE Transactions on Power Electronics. Online available.

Chapter 2. Overview of condition monitoring technique

T_j and bond wire failure are of paramount importance for the reliability of IGBT PMs. Numerous researches have been published in this area. This chapter summarises these techniques and compares them.

2.1. **Techniques for junction temperature estimation**

In general, junction temperature is referred to as T_j, which is the temperature of the junction region in the IGBT chip. In mIGBT PMs, the junction temperature does not precisely match the junction temperature of one of the chips [23, 24]. Thus, in mIGBTs, the term "virtual junction temperature" (T_{vj}) is used. Unlike T_j, T_{vj} is the 'global' temperature [25], which was initially introduced to define the average thermal impedance between IGBT chips and case [23, 24]. Since T_{vj} is one of the primary failure drivers, many researchers have attempted to estimate T_{vj} in IGBT PMs. These techniques can be divided into three categories: temperature sensors, thermal model and temperature sensitive electrical parameters (TSEPs). An overview of these techniques is presented below.

2.1.1. Temperature sensors

Various temperature sensors have been applied to mIGBT PMs. Most commonly, manufacturers such as Infineon add a negative temperature coefficient (NTC) thermistor on the base plate of PMs. However, it is well known that base plate temperature sensors do not measure T_{vj} because of the thermal impedance between the semiconductor chips and base plate, which causes errors. Thus, contact sensors are proposed that can be applied directly on the IGBT chip. Contact sensors can be divided into resistive temperature detectors (RTDs) [26], semiconductor sensors [27, 28], radio frequency identification (RFID) sensors and optical sensors [18, 29] as shown in Figure 2.1.

Figure 2.1a shows an RTD sensor. It is made of high purity conductive materials whose electrical resistance is temperature dependent. This material is added on top of the existing semiconductor chip such that the RTD sensor is measuring the surface temperature of the chip directly.

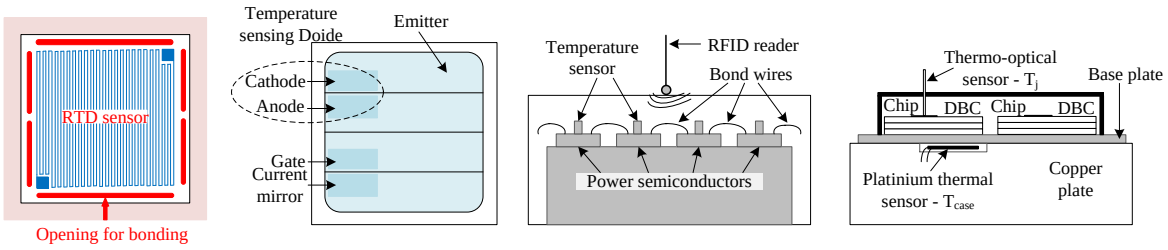


Figure 2.1 Various sensors for T_{vj} measurement: (a) RTD sensor, (b) Diode, (c) Temperature sensor, (d) Optical sensor.

Figure 2.1b illustrates a diode sensor that is integrated into the semiconductor structure. The pn junction of the diode is biased externally. This diode can read the temperature due to the temperature dependency of the forward voltage. Figure 2.1c makes use of RFID technology. On the top of each chip, small coils with different length are added. Rising temperatures extend the chip and therefore the length of the coil, which is used for temperature measurement. Communication takes place via RFID. An optical sensor is presented in Figure 2.1d. The optical sensor depends on the relationship between the temperature and intensity, phase, frequency and polarisation state of the transmitted light.

Due to the dissimilarity in operation principles, there are distinct variations in the response time and sensitivity of the temperature sensors. Thermistors and RTD sensors take the longest time to respond to sudden temperature change. The thermistor shows good sensitivity compared to RTD, but the temperature dependency of the thermistor is not linear because of the intrinsic characteristic. Semiconductor sensors, RFID techniques, and optical sensors exhibit faster thermal response as well as better accuracy. However, even though optical sensors are very accurate, the associated temperature capturing equipment is complicated and expensive. Thus, they are generally employed in laboratory environment.

2.1.2. Techniques based on thermal models

To apply temperature sensors, modification to the IGBT module is inevitable. Thermal modelling technique is one of the techniques proposed that can avoid modification. Thermal models are created to imitate the thermal path between the IGBT chips and base plate of the PM. Since electrical parameters can mimic thermal parameters [13], the electrical network is employed to simulate the thermal path. In general, there are two empirical thermal models, namely, Foster and Cauer, as shown in Figure 2.2. The models are built based on the assumption

that heat is generated uniformly at the upper surface of the device and that all of the heat flows perpendicular to the lower surface [30].

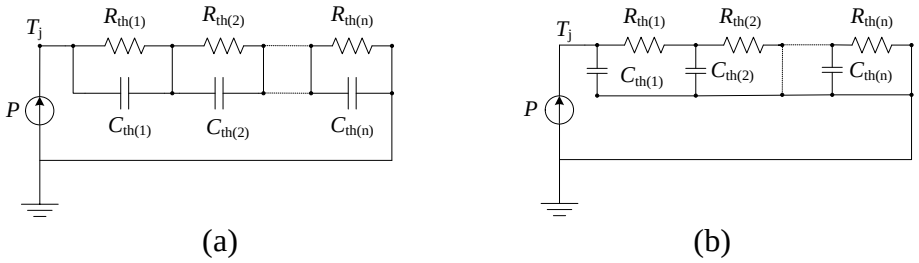


Figure 2.2 Thermal model [30]: (a) Foster model, (b) Cauer model.

Foster network is only a mathematical model. There is no physical relationship between each resistor-capacitor cell and the physical layer. It can only predict T_j. However, Cauer network can predict the temperature of each physical layer in the IGBT module. The node voltage in the model corresponds to the average temperature of the layer. Thermal models for mIGBT are more complicated because of the sophisticated thermal conduction and thermal coupling among the IGBT chips.

2.1.3. Estimation based on TSEPs

TSEPs are electrical parameters of the IGBT that are temperature dependent. These parameters can be measured without any modification to the module. Thus, they are widely populated for T_{vj} estimation.

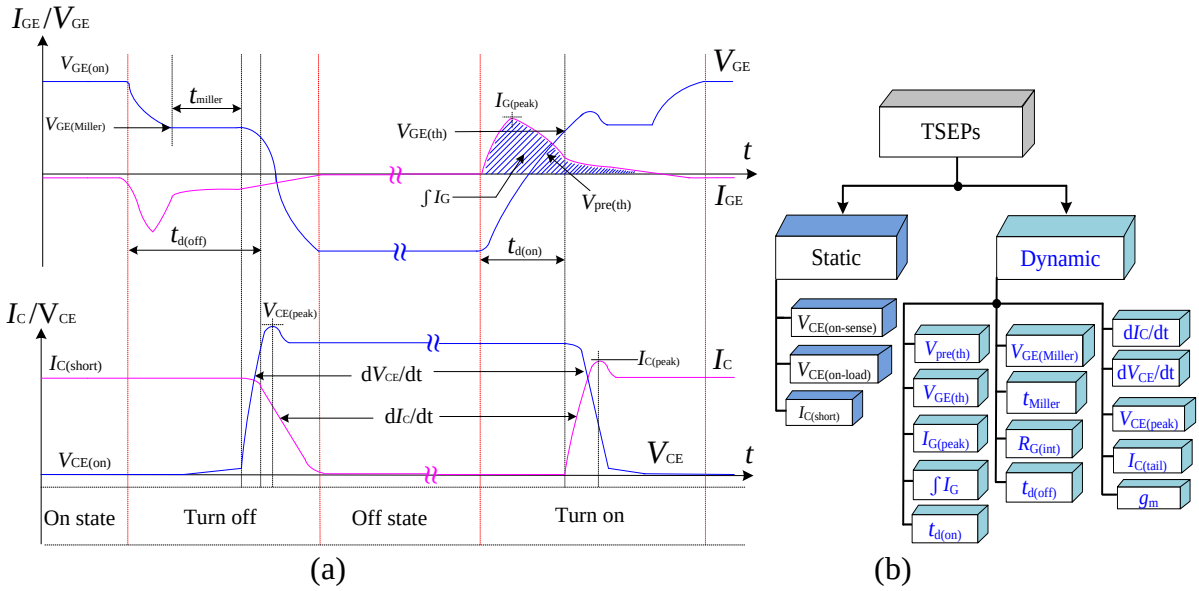


Figure 2.3 (a) Switching waveform of an IGBT PM, (b) Classification of TSEPs.

Figure 2.3a is the typical switching waveform of an IGBT PM. Various TSEPs have been reported for T_{vj} estimation and they are highlighted in Figure 2.3a. These electrical parameters are collected and classified into static TSEPs and dynamic TSEPs as shown in Figure 2.3b. Static TSEPs are the parameters measured during on-state or off-state. Dynamic TSEPs are measured during turn-on transient or turn-off transient.

2.1.3.1. Static TSEPs

The on-state voltage $V_{CE(on)}$ is the most comprehensive approach due to its high reliability and sophisticated monitoring technique. The on-state voltage $V_{CE(on)}$ of the IGBT module is expressed in (2.1). The temperature dependency of V_{BE} is influenced by the number of hot carriers. Higher temperature will provide more hot carriers which will reduce the resistivity and lead to lower on-state voltage. Thus, V_{BE} shows NTC. However, the on-state resistance $R_{CE(on)}$ and the bond wire resistance R_{wire} have positive temperature coefficient. Therefore, when a small sense current $I_{C(sense)}$ is injected into the IGBT, the on-state voltage $V_{CE(on-sense)}$ is dominated by the forward voltage V_{BE} of the base terminal of the transistor in the IGBT chip. Thus $V_{CE(on-sense)}$ shows NTC. However, when load current $I_{C(load)}$ is injected to the IGBT, the on-state voltage $V_{CE(on-load)}$ is mainly influenced by the on-state resistance of the IGBT, which has positive temperature coefficient [13]. Thus, the temperature coefficient of $V_{CE(on-load)}$ is positive. It can also be noted that between $I_{C(sense)}$ and $I_{C(load)}$, there is a I_C where the temperature dependency of the is negligible. This point is called the inflexion point in the forward characteristic of the IGBT module. Both $V_{CE(on-sense)}$ and $V_{CE(on-load)}$ have been employed for T_{vj} estimation [13, 20, 25, 31-33]. However, $V_{CE(on)}$ is also affected by I_C and gate-emitter voltage V_{GE}.

$$V_{CE(on)} = V_{BE}(T) + R_{CE(on)}(T) \cdot \frac{I_C}{1+\beta_{PNP}} + R_{wire} I_C \tag{2.1}$$

Where $R_{CE(on)}$ is the equivalent on-state resistance, β_{PNP} is the current gain of internal PNP transistor in IGBT, R_{wire} is the equivalent resistance of bond wires.

Short circuit current $I_{C(short)}$ has also been investigated to predict T_{vj} [34]. The results show that $I_{C(short)}$ has a NTC with good sensitivity. In [34], $I_{C(short)}$ is captured with the help of an extra bypass switch. However, the mIGBT would need to be operated to its limit. Consequently, in practice, it is not a good temperature measurement.

2.1.3.2. Dynamic TSEPs

Some electrical parameters during the switching transient have also been reported to be temperature dependent. In this thesis, these parameters are referred to as dynamic TSEPs. An overview of these dynamic TSEPs is provided in this section.

Pre-threshold voltage $V_{pre(th)}$ was first proposed in [35]. In this paper, the gate emitter loop is equivalent to resistor-capacitor in series as shown in Figure 2.4. The internal gate resistor $R_{G(int)}$ includes the resistance of the surface mount resistor, the resistance of copper track, bond wires resistance as well as the resistance of the gate pad. $R_{G(int)}$ is temperature dependent and has a positive temperature coefficient. Before the threshold point, the gate-emitter voltage can be derived as (2.2). The change of $R_{G(int)}$ will lead to the variance of the time constant of the gate circuit. Therefore, the pre-threshold transient will shift against temperature change. $V_{pre(th)}$ can then be measured at a fixed time instant to indicate the temperature variation.

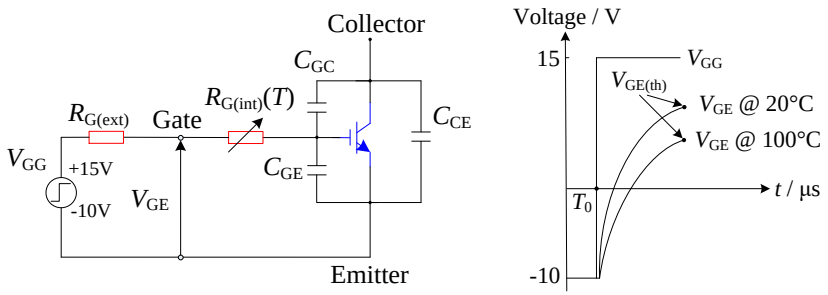


Figure 2.4 RC circuit forming the waveform of V_{GE} from the PWM trigger event T_0 to $V_{GE(th)}$ during turn-on.

$$V_{GE} = (V_{GE(th)}(T) - V_{GE(off)})(1 - e^{\frac{-t(x)}{R_{G(int)}(T)(C_{GE}+C_{GC})}}) + V_{GE(off)} \tag{2.2}$$

Where C_{GE} is the gate-emitter capacitor, C_{GC} is the gate-collector capacitor, $V_{GE(off)}$ is the gate-emitter voltage at off-state.

Threshold voltage $V_{GE(th)}$ is the gate voltage at which an IGBT turns on, and collector current begins to flow, as shown in Figure 2.3a. The threshold voltage of the IGBT is given in (2.3) [25, 36-39]. The threshold voltage is mainly influenced by the intrinsic carrier concentration. The increment in the junction temperature will active more carriers which will lead to the decrement of the threshold voltage as expressed in (2.3). Both I_C and V_{GE} should be monitored to obtain $V_{GE(th)}$.

$$V_{GE(th)} = V_{FB} + 2\frac{kT}{q}\ln\frac{N_A}{n_i} + \frac{\sqrt{2\varepsilon_{ox}\varepsilon_{si}qN_A(2\frac{kT}{q}\ln\frac{N_A}{n_i})}}{C_{ox}} \quad (2.3)$$

Where V_{FB} is flat-band voltage. k is Boltzmann constant. T is absolute temperature. q is charge. N_A is acceptor impurity density. n_i is intrinsic carrier concentration. C_{ox} is gate oxide capacitance. ε_{ox} and ε_{si} are dielectric constants of oxide and silicon, respectively.

The Miller plateau has two TSEPs: the voltage of the plateau $V_{GE(Miller)}$ and the duration of the plateau t_{Miller}, as expressed in (2.4) and (2.5), respectively [40-44]. It should be highlighted that the characteristic of the $V_{GE(Miller)}$ is highly dependent on the IGBT chip structure. The IGBT chip used in the first three reference is trench field stop IGBTs.

$$V_{GE(Miller)} = V_{th}(T) + \frac{I_C}{g_m(T)} \quad (2.4)$$

$$t_{Miller} = \frac{R_g(T)C_{GC}(V_{CE} - V_{CE(on)}(T))}{(\frac{I_C(T)}{g_m(T)} + V_{GE(th)}(T))} \quad (2.5)$$

Where R_g is the gate resistor, including the external gate resistor and internal gate resistor. C_{GC} is the gate-collector capacitor. g_m is the trans-conductance.

The literature also measures the internal gate resistance of the chip $R_{G(int\text{-}chip)}$, which is temperature dependent. Two techniques have been proposed: measurement of the peak gate current $I_{G(peak)}$ [45-48] and of resonant signal injection during off state [49-51].

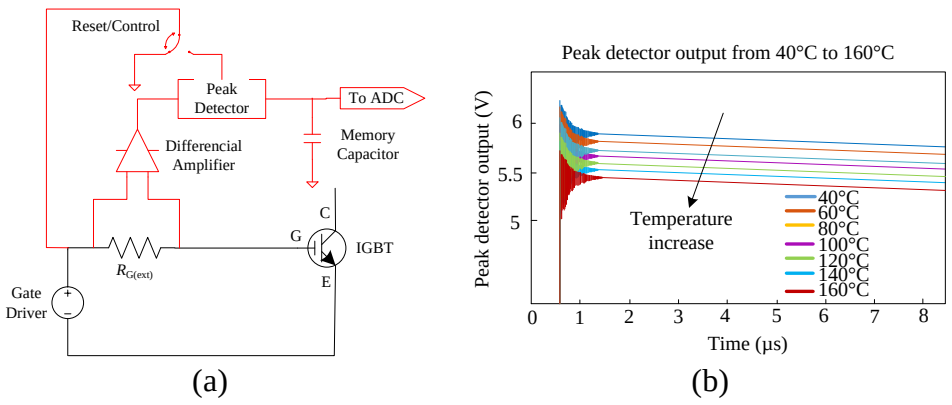


Figure 2.5 $I_{G(peak)}$ approach [45-48]: (a) Schematic of the peak detector, (b) $I_{G(peak)}$ variation with temperature.

The gate current I_G is determined by $R_{G(int\text{-}chip)}$ during turn-on, when it charges the gate capacitors. I_G reaches the peak when the gate impedance is pure resistive, which means only the gate resistor affects $I_{G(peak)}$. The variation of $R_{G(int\text{-}chip)}$ caused by T_{vj} will, therefore, be reflected in $I_{G(peak)}$. Figure 2.5 shows the $I_{G(peak)}$ detector circuit and temperature dependency of $I_{G(peak)}$. To maximise the temperature influence, Nick et al. and Niu proposed employing the integration of the gate voltage $\int V_{GE}$ to estimate T_{vj} [45]. Results showed better sensitivity due to the integration.

Denk proposed superimposing a sinusoidal signal between gate and emitter terminals to detect the T_{vj} variation [49-52]. The signal is injected during the off state of the IGBT switch. The frequency of the injected signal is specially selected to form resonance among the parasitic components in the gate-emitter circuitry. The frequency response is then solely dependent on $R_{G(int\text{-}chip)}$. Figure 2.6 depicts the implementation of the approach and its preliminary results. The signal injection circuit is integrated within a conventional gate driver. An inductor L_s is added to trigger the resonance phenomenon at a lower frequency. The voltage across the external gate resistor is recorded for analysis. Both $I_{G(peak)}$ and the resonant signal injection approach display good linearity against temperature alteration.

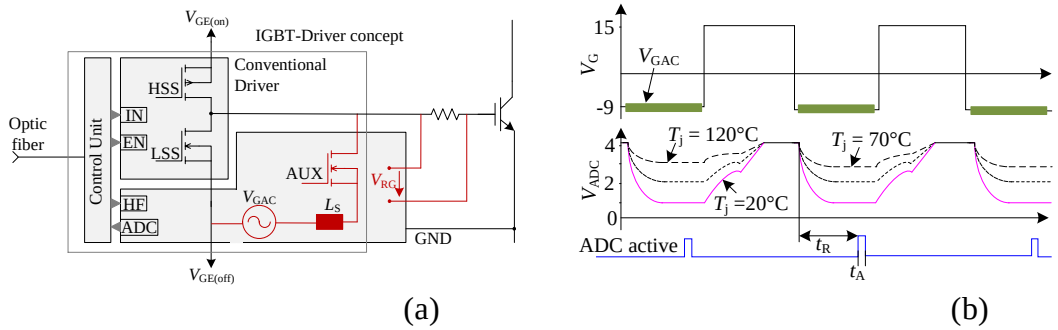


Figure 2.6 Resonant signal injection approach: (a) Schematic of the signal injection approach, (b) Measurement results.

The collector-emitter voltage slope dV_{CE}/dt during turn-off is also temperature dependent. dV_{CE}/dt is expressed in (2.6) [53] and has therefore also been proposed as TSEP.

$$\frac{dV_{CE}}{dt} = \frac{1}{R_g(T)C_{GC}}\left(\frac{V_{GE(on)} - V_{GE(off)}}{1+(C_O / g_m(T)R_g(T)C_{GC})}\right) \tag{2.6}$$

Where C_O is defined as charge extraction capacitance. $V_{GE(on)}$ and $V_{GE(off)}$ are the voltage of the gate drive under on-state and off-state, respectively.

In the second stage of the turn-off transient, the collector current $I_{C(tail)}$ is reported to be temperature dependent and the current can be derived from (2.7) [54].

$$I_{C(tail)} = \frac{qD_{nE}p_0^2}{L_{nE}N_{AE}}A_C \tag{2.7}$$

Where q is charge. D_{nE} is the diffusion coefficient for minority carriers in the p region. p_0 is the initial concentration of holes at the edge of the space charge region. L_{nE} is the diffusion length for electrons in the p+ collector region. N_{AE} is the minority carrier doping concentration. A_C is the size of p region. Results in [44] show that the tail current is feasible for T_{vj} estimation due to good linearity and sensitivity.

Additionally, $I_{C(peak)}$ during turn-on and $V_{CE(peak)}$ during turn-off have been proposed to estimate T_{vj} [55, 56] and show good linearity with temperature.

The turn-on delay $t_{d(on)}$ is defined as time duration from when $V_{GE(off)}$ increases to 90% of its beginning value to the time when V_{CE} decreases to 90% of its beginning value or, as an alternative, the time when I_C increases to 10% of its final value. The turn-off delay $t_{d(off)}$ is defined as the time duration from when $V_{GE(on)}$ decreases to 90% of its beginning value to the time when V_{CE} decreases to 90% of its final value (or, as an alternative, the time when I_C decreases to 90% of its beginning value). Turn-on delay $t_{d(on)}$ and turn-off delay $t_{d(off)}$ are expressed in (2.8) [44, 57] and (2.9) [44], respectively.

$$t_{d(on)} = R_g(T)C_{GE}\ln(1-\frac{V_{GE(th)}(T)}{V_{GE}}) \tag{2.8}$$

$$t_{d(off)} = R_g(T)C_{ies}\ln(\frac{I_C}{g_m(T)\cdot V_{GE(th)}(T)}+1) \tag{2.9}$$

Where C_{ies} is input capacitance.

Trans-conductance g_m is introduced in [58] as TSEP. The expression of g_m is shown in (2.10). The challenge of this method is that several parameters must be measured to calculate g_m, which increases the number of sensors.

$$g_m = \frac{dI_C}{dV_{GE}} = \left[\frac{1}{1-\beta_{PNP}}\right]\left[\mu(T)\cdot C_{OX}\cdot\frac{W}{L}\cdot(V_{GE}-V_{GE(th)}(T))\right] \tag{2.10}$$

Where μ is the mobility of the electrons/holes. W is the width of the channel. L is the length of the channel. C_{OX} is the capacitance of the gate oxide.

The voltage across the power emitter (PE) and auxiliary emitter (AE) have also been reported to be temperature dependent [59-61]. The parasitic inductor L_σ between the PE and AE helps to convert the differential parameters to voltage V_{eE}, which can be easily captured. For instance, the collector current slope dI_C/dt can be derived as (2.11). Therefore, V_{eE} is temperature dependent and can be used to estimate T_{vj}.

$$di_C/dt = V_{eE}/L_\sigma \tag{2.11}$$

The voltage across the PE and AE V_{eE} provides, therefore, an alternative for a few TSEPs. As V_{eE} measurement is more convenient, it is a promising approach for T_{vj} estimation.

Table 2.1 Summary of selected TSEPs

TSEPs	Single chip/Multi-chip	Sensitivity(/°C)	Number of parameters that need to be measured
$V_{CE(on\text{-}load)}$	Both	1 mV–4 mV ↑[(1)]	1
$V_{CE(on\text{-}sense)}$	Both	4 mV–10 mV ↓[(2)]	1
$I_{C(short)}$	Single chip	0.345 A ↓	1
$V_{GE(th)}$	Single chip	2 mV–10 mV ↓	2
$R_{g(int\text{-}chip)}$	Both	0.9 mΩ–2.8 mΩ ↑	1
$\int V_{GE}$	Multi-chip	70 mV ↓	1
$\int I_{GE}$	Single chip	0.3 nC ↑	1
$t_{d(on)}$	NA[(3)]	1.875 ns ↑	2
$t_{d(off)}$	NA	1.57 ns ↑	2
$V_{GE(Miller)}$	NA	4.5 mV ↓	1
t_{Miller}	Multi-chip	0.8 ns–3.4 ns ↑	1
dV_{CE}/dt	NA	6 V/μs ↓	2
$I_{C(tail)}$	NA	51 mA ↑	1
g_m	Multi-chip	1.54 AV ↓	3
$V_{pre(th)}$	Multi-chip	2.2 mV ↓	1
V_{eE}	Multi-chip	68 mV ↑	1

[(1)]TSEP has positive temperature coefficient.
[(2)]TSEP has NTC. [(3)]Not applicable.

Table 2.1 provides a summary of the TSEPs about their temperature dependency. The on-state voltage $V_{CE(on\text{-}sense)}$ is the most popular approach for T_{vj} estimation. The dynamic TSEPs share a common challenge that high bandwidth measurement circuitry is necessary to achieve reasonable accuracy. For g_m, several sensors are required to obtain its value. The increasing the number of sensors will introduce more errors, thus, this is a less attractive option. When applying TSEPs on the high voltage side, high-voltage isolation issues will need to be addressed.

2.1.4. Discussion

Various approaches have been proposed for T_{vj} estimation. The main drawback of contact temperature sensors is the response time regarding online application. Another issue is the loss of chip space that can be used for emitter bond wire connections. The thermal model approach offers a solution to estimate T_{vj} without any modification to the IGBT module. However, the thermal model for mIGBT modules is very complicated considering the thermal conduction and thermal coupling among all IGBT chips. In addition, the thermal characteristics of the IGBT module change over time, which means the model should also be updated according to the degradation status. Techniques based on TSEPs are the most prevalent approaches because they rely on the linear relationship between electrical parameters and T_{vj} and do not need any modification to the IGBT module.

Most of the research that aims to determine T_{vj} focuses on single-chip IGBTs or multi-chip module assuming HTD. HTD is, however, an unrealistic assumption due to intrinsic package differences and variation in the degradation speed of each chip. Thus, the thermal distribution within mIGBTs is not uniform. Considering the importance of T_{vj}, it is necessary to evaluate the impact of SDoT on TSEPs as well as the operation of the IGBT module.

2.2. **Techniques for Bond wire lift-off estimation**

2.2.1. The terminal layout of an IGBT module

Figure 2.7a shows the structure of a half-bridge wire-bond IGBT PM with one IGBT switch on the top and the other switch on the bottom. There are three IGBT chips in each switch, and each IGBT chip has an anti-parallel diode. The IGBT chip in this module is with trench gate field stop structure. It is the fourth generation IGBT chip. Compared with punch-through IGBT, n+

buffer layer is lower doped and is only to stop the electric field [62]. Compared with the non-punch-through IGBT, the N-drift layer is thinner [62]. The field stop IGBT keeps the design concept of the low carrier injection and no lifetime control [62, 63]. The structure reduces on-state voltage and turn-off losses. The trench gate also helps to reduce the on-state voltage. In addition, the inflexion point of a field stop IGBT is lower than that of punch through IGBT. This is because the linear part of the forward characteristic curve is a function of mobility and lifetime [64]. Due to the fact that field stop IGBT does not use lifetime control and the mobility declines with temperature, the on-state voltage increases drastically which results in a lower inflexion point [64].

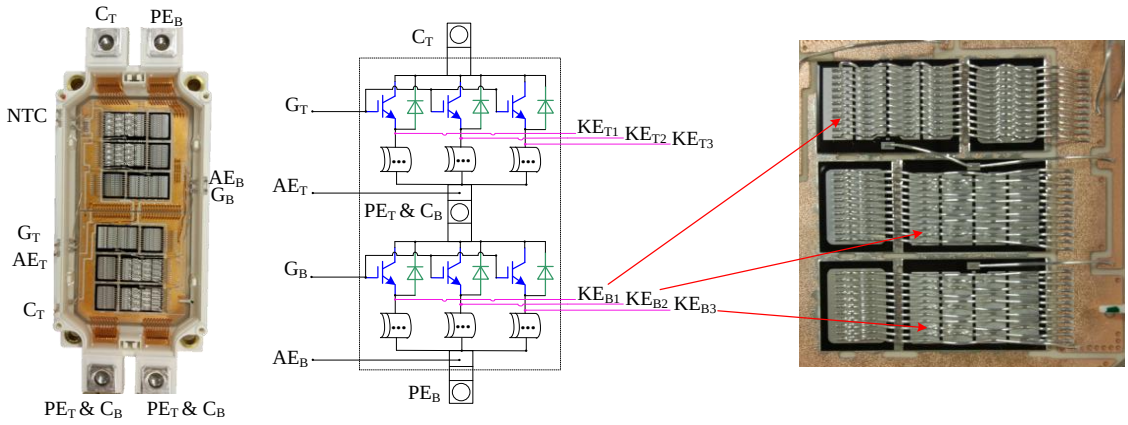


Figure 2.7 Infineon 1.7 kV 600 A half-bridge IGBT PM (FF600R17ME4): (a) Interior view, (b) Terminal illustration, (c) Zoom in for KE.

As shown in Figure 2.7b, the emitter can be further categorised as PE for load power flow, AE for gate driving and Kelvin emitter (KE). KE is the point that is directly attached to the IGBT chip surface as illustrated in Figure 2.7c. Electrical parameters measured from the individual terminal are linked with the health condition of the corresponding parts. Therefore, they are naturalised as health-sensitive signatures. In this thesis, these signatures are categorised into intrinsic signatures and induced signatures according to the features of the measured signals. These techniques are detailed in the following sections.

2.2.2. Intrinsic signatures

Intrinsic signatures refer to electrical parameters that are direct reflections of the operation condition and can be acquired without extra excitation. In general, these parameters can be measured via the different emitter terminals of an mIGBT module.

2.2.2.1. Signatures from the PE

Signatures on the PE are easily assessable without any modification to the package. This makes them appealing for detecting bond wire lift-off.

The on-state voltage $V_{CE(on)}$ across C-E has been broadly exploited to monitor bond wire conditions. Generally, $V_{CE(on)}$ is measured across C-PE during the on-state. Therefore, it includes the voltage across the IGBT chip as well as the voltage across bond wires.

The voltage across the IGBT chip should be measured across C-KE. It is called $V_{CK(on)}$. Figure 2.8a shows the chip structure of a non-punch through IGBT. It is a MOSFET structure with an additional p layer. When the IGBT is on, V_{GE} is well above the threshold voltage. At this stage, the MOSFET part is working in the linear region. The on-state model of the IGBT chip can then be simplified as a P-i-N rectifier in series with a MOSFET as shown in Figure 2.8b [54].

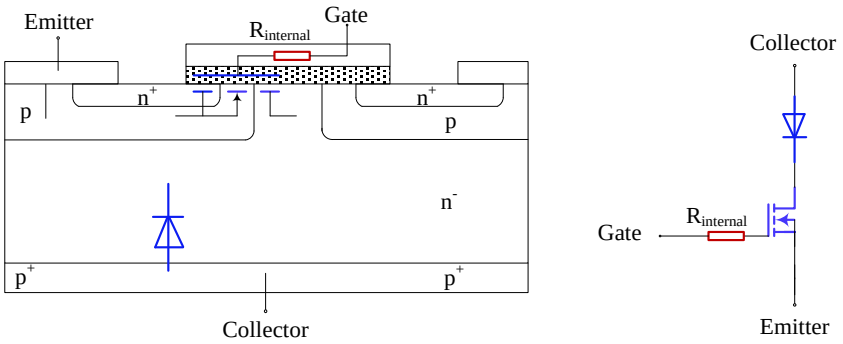


Figure 2.8 IGBT chip: (a) Chip structure, (b) The simplified equivalent circuit at on state.

The on-state voltage of the chip is the summation of the voltage in the rectifier portion and the MOSFET portion. The on-state voltage can then be described as (2.12). The first part is the voltage across the P-i-N rectifier, and the second part is that across the MOSFET portion [54].

$$V_{CK(on)} = \frac{2kT}{q}\left[\frac{J_C W_N}{4qD_a n_i F(W_N / 2L_a)}\right] + \frac{pL_{CH} J_C}{\mu_{ni} C_{OX}(V_G - V_{GE(th)})} \qquad (2.12)$$

Where, k is the Boltzmann's constant, T is the absolute temperature, q is the electron charge, J_C is the collector current density, W_N is the width of the N-drift region, D_a is the ambipolar diffusion coefficient, n_i is the intrinsic carrier concentration, L_a is the ambipolar diffusion length in the N-base region, p is the cell pitch of the n-drift region, L_{CH} is the channel length, μ_{ni} is the

inversion layer mobility, C_{OX} is the capacitance of the gate oxide, and $V_{GE(on)}$ is the gate bias voltage.

The voltage across the bond wires V_{wire} is caused by current flowing through the pure resistance, which is described as (2.13). R_{wire} is the equivalent resistance of all the bond wires.

$$V_{Wire} = R_{wire} \times I_C \tag{2.13}$$

Therefore, $V_{CE(on)}$ can be expressed as (2.14).

$$V_{CE(on)} = \frac{2kT}{q}\left[\frac{J_C W_N}{4qD_a n_i F(W_N / 2L_a)}\right] + \frac{pL_{CH} J_C}{\mu_{ni} C_{OX}(V_G - V_{TH})} + R_{wire} \times I_C \tag{2.14}$$

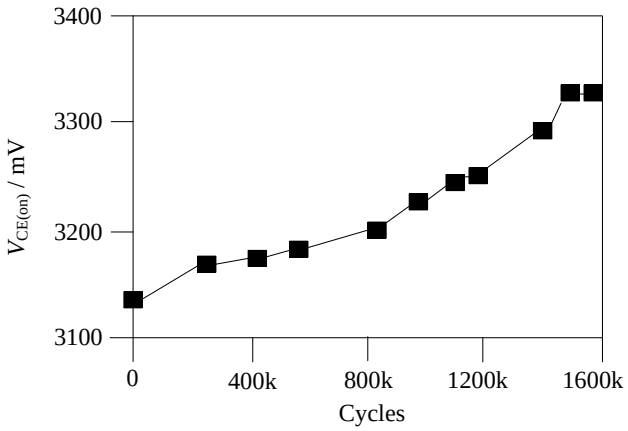


Figure 2.9 $V_{CE(on)}$ as a function of power cycles at the static state [20].

Bond wire fatigue will lead to a rise in the equivalent resistance R_{wire}, which will also cause an increment in $V_{CE(on)}$. Consequently, $V_{CE(on)}$ rise can be used as a failure indicator [20]. In [20], $V_{CE(on)}$ is measured at rated current and thermal steady state. Thus, if there is any variation in $V_{CE(on)}$, it must come from the degradation of bond wires. The test results are shown in Figure 2.9. $V_{CE(on)}$ increases with the weariness of the module. Additionally, 5% increment upon $V_{CE(on)}$ is used as failure criteria for the module in this paper. A similar experiment is conducted in [65]. Likewise, a rise in $V_{CE(on)}$ is observed with the accelerated ageing process over time.

However, $V_{CE(on)}$ has also been popularised as a TSEP because of its linear relationship with T_{vj} variation at constant I_C. Therefore, $V_{CE(on)}$ has to be measured at the same thermal static state to appraise the bond wire state. However, the same thermal static state is difficult to achieve during normal operation. Thus, the issue of how to eliminate the influence of T_{vj} on $V_{CE(on)}$ arises, and

it has been studied extensively. Many viable solutions have been proposed that have been discussed in detail.

Authors in [66] proposed measuring the $V_{CE(on\text{-}sense)}$ at sense current (100 mA) as well as $V_{CE(on\text{-}load)}$ at load current. Compared to $V_{CE(on\text{-}load)}$, the behaviour of $V_{CE(on\text{-}sense)}$ is dominated by the first two parts in (2.14). V_{wire} is too small to be influential. Thus, $V_{CE(on\text{-}sense)}$ is solely dependent on T_{vj}. The combination of $V_{CE(on\text{-}sense)}$ and $V_{CE(on\text{-}load)}$ can then decouple the influence of T_{vj} and bond wire lift-off with the help of a reference table. A current pulse train is used to implement the approach, as shown in Figure 2.10. It is found that there is approximately 1% increment on the first broken wire. Further, 7% is claimed to be the warning criteria for the module tested. This approach has now been generally recognised [67-69] as an appropriate in-situ health monitoring technique for IGBT PMs.

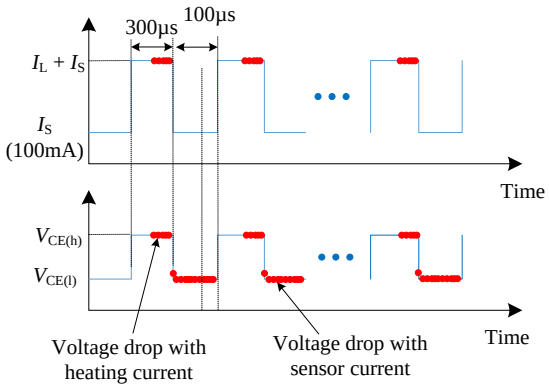


Figure 2.10 Current pulse trains for bond wire health monitoring in [66].

In [70-72], authors introduced another alternative approach to exclude the temperature influence. This technique takes advantage of the inflexion point where $V_{CE(on)}$ has a zero temperature coefficient. Figure 2.11a shows the forward characteristics of an IGBT. Below the inflexion point where I_C is low, $V_{CE(on)}$ has a strong positive correlation with T_{vj} as shown in [54] and vice versa. In between, there is a point when the temperature dependency of $V_{CE(on)}$ is negligible. This point is called the inflexion point.

Therefore, the impact of bond wires can be observed through $V_{CE(on)}$ at the inflexion point without being affected by T_{vj}. Hence, $V_{CE(on)}$ is employed to monitor the bond wire state. Figure 2.11b describes the deviation of $V_{CE(on)}$ during the ageing process. A sudden jump in $V_{CE(on)}$ occurs when there is bond wire failure.

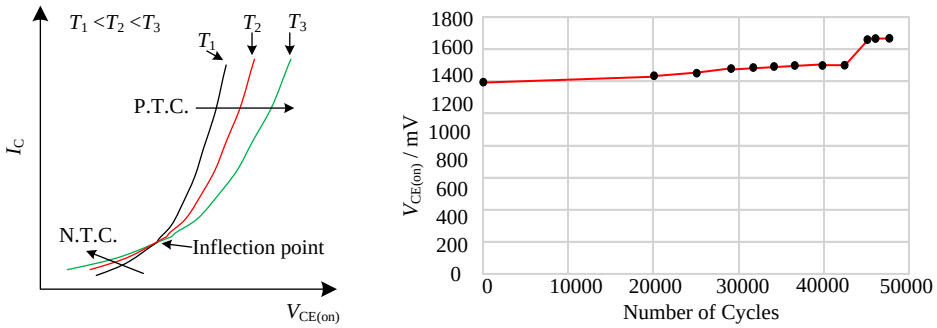


Figure 2.11 (a) Forward characteristics of an IGBT, (b) Detection of bond wire failure measuring $V_{CE(ON)}$ at the inflexion point.

Despite the two techniques listed above, advanced algorithms have been proposed to reduce the influence of T_{vj}. A recursive least square algorithm is presented in [73]. In [73], $V_{CE(on)}$ and I_C are used by the RLS algorithm to estimate $R_{CE(on)}$. Although $R_{CE(on)}$ is a function of both T_{vj} and bond wire state, the algorithm eliminates the influence of T_{vj} such that the linear transformation Z – which is the output of RLS – is only sensitive to bond wire failure. Figure 2.12 is the estimation from the RLS algorithm. In the figure, $R_{CE(on)}$ increases with bond wire failure and there is a clear pattern between the linear transformation Z and number of bond wire failures.

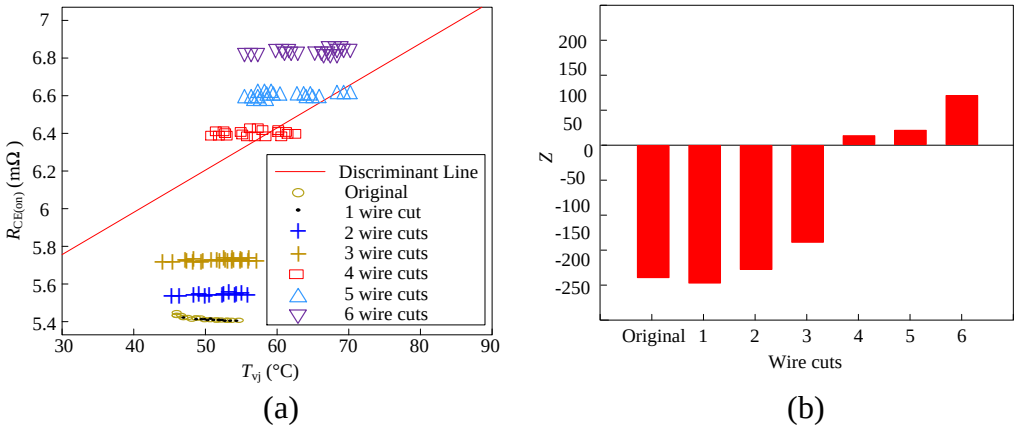


Figure 2.12 (a) Discriminant line and estimated data points ($R_{CE(on)}$, T_j) as wires on the chip are cut, (b) The corresponding value of the linear transformation Z. [73]

In addition to the flourishing research on the measurement of static electrical parameters, investigations of the transient features at PE also show effective estimation of the bond wire state. Figure 2.13a is the typical turn-off transient of V_{CE} and I_C. There is an overshoot in V_{CE}. The overshoot ΔV_{CE} is a function of I_C and the parasitic inductors in the C-PE circuitry, as shown in (2.15) [74].

$$\Delta V_{CE} = L \times \frac{dI_C}{dt} \tag{2.15}$$

The parasitic inductors in the C-PE circuitry are depicted in Figure 2.13b, which includes the inductance from C and PE connectors, the inductance from C and PE copper track and the inductance from the bond wires. The first two parts are generally treated as constant during the whole lifespan of the IGBT switch. Bond wire lift-offs will result in inductance rise, which will cause higher overshoot in V_{CE}. This phenomenon is an indicator of bond wire lift-off estimation and is studied in [75]. The results are described in Figure 2.14. TR1, TR2 and TR3 correspond to zero, four and nine bond wire lift-offs, respectively.

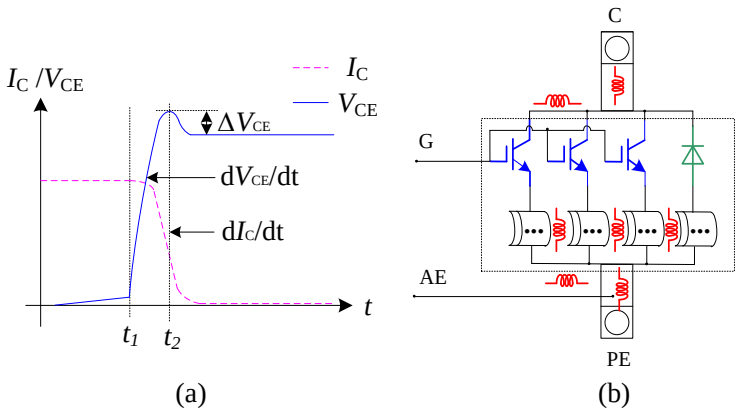


Figure 2.13 (a) Turn-off transient of V_{CE} and I_C in an IGBT PM, (b) Parasitic inductors in an IGBT switch.

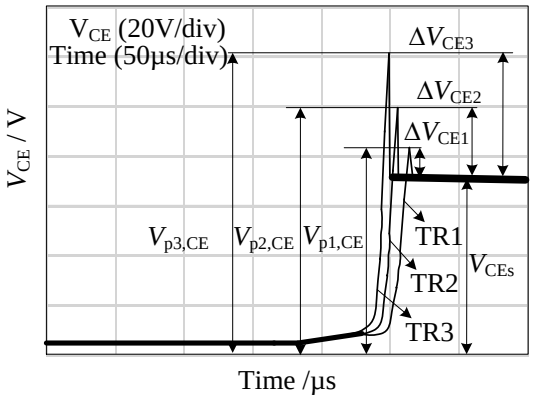


Figure 2.14 IGBT turn-off voltage across the collector and PE [75].

2.2.2.2. Signatures via the AE

AE is a connection drawn from the copper track of the PE, which is used for gate drive. There will not be any load current flowing through AE. Approaches derived from AE reveal the features of the gate circuitry.

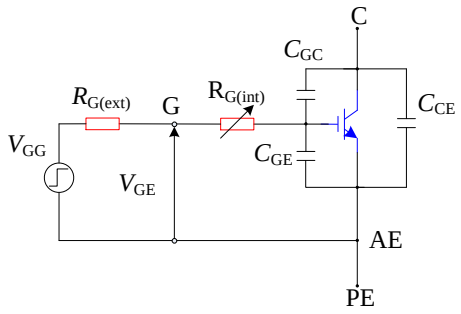


Figure 2.15 The equivalent G-AE circuitry of an IGBT PM.

The G-AE circuitry can be simplified as the RLC (resistor, inductor and capacitor in series) circuit presented in Figure 2.15. C_{GE}, C_{GC} and C_{CE} are the equivalent capacitors of G-AE, G-C and C-AE, respectively. The turn-on transient can be regarded as the charging of these capacitors. A typical turn-on waveform is given in Figure 2.16. When there is chip failure, which means there is an effective loss of parallel capacitors, the charging procedure will shift. In this case, because of the reduced capacitance, the charging slew rate will speed up. This is reflected in V_{GE} and I_G. Therefore, V_{GE} during the turn-on process and $I_{G(peak)}$ are proposed to estimate bond wire conditions in [75-79]. The results are presented in Figure 2.17.

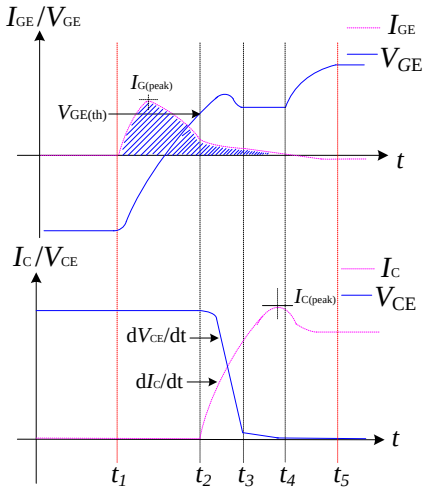


Figure 2.16 Turn-on transient of an IGBT PM.

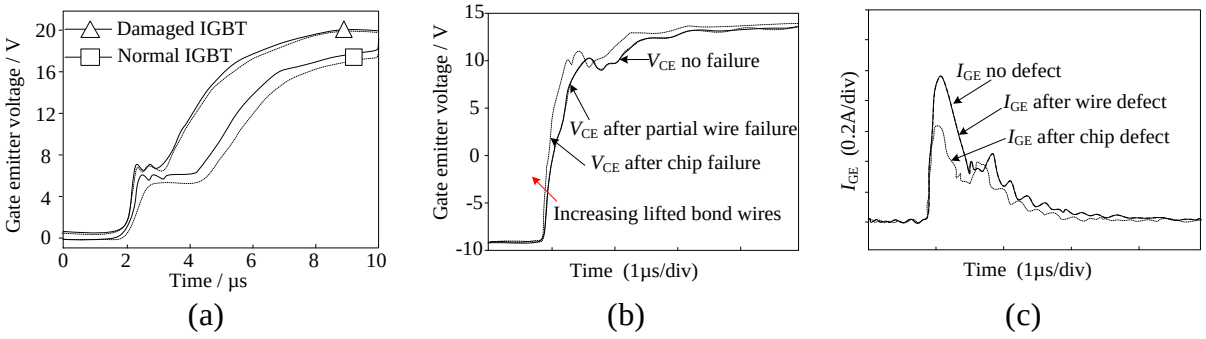


Figure 2.17 (a) The waveform of V_{GE} during IGBT turn-on process [76]: (b) Turn-on waveforms of V_{GE} at different health states [77], (c) Turn-on waveforms of I_G at different health states [78].

It is apparent that the rising rate of V_{GE} in damaged IGBT is more rapid than fault-free IGBT before and after the Miller plateau. The main reason for this is the decrease in C_{ies} during these periods. This is also captured in I_G. The peak gate current $I_{G(peak)}$ of damaged IGBT is reduces compared with that of a fault-free IGBT.

Another technique is proposed in [80]. It measures the resistance R_{Ee} across PE and AE to determine the bond wire conditions. R_{Ee} is recorded during power cycling of different IGBT chips, as shown in Figure 2.18. The shape of the curve is an indicator of reliability. For instance, a steeper change indicates a weaker device and a flat change suggests a robust device. The change can be derived from the first and second derivatives of R_{Ee}.

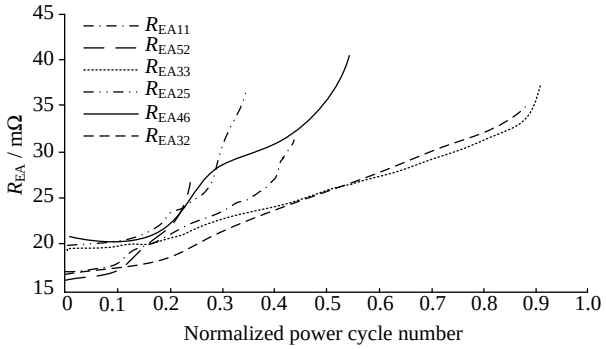
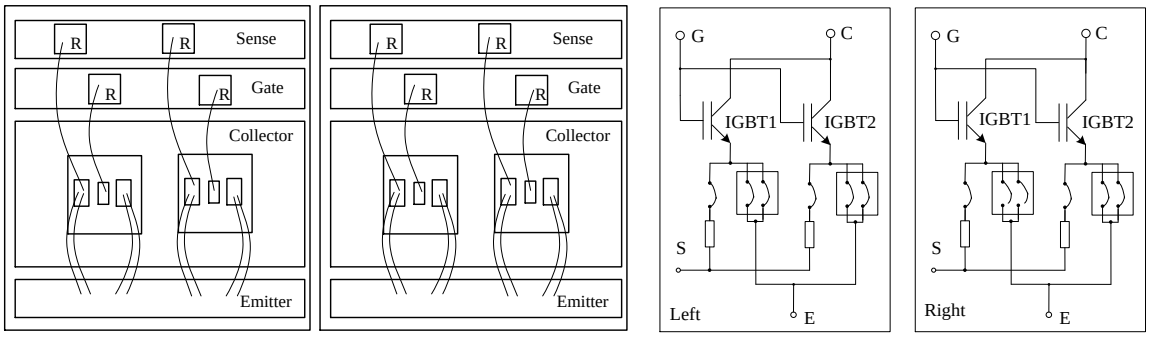


Figure 2.18 Degradation of resistance between PE and AE [80].

2.2.2.3. Signatures through KE

KE is directly attached to the surface of the IGBT chip as detailed in Figure 2.7c. In [81], extra bond wires are soldered to KE to generate sensing points. The modification is illustrated in Figure 2.19a. The equivalent circuit diagrams with and without bond wire lift-off are compared in Figure 2.19b. When there is bond wire lift-off, the voltage at the sensing point will shift. The

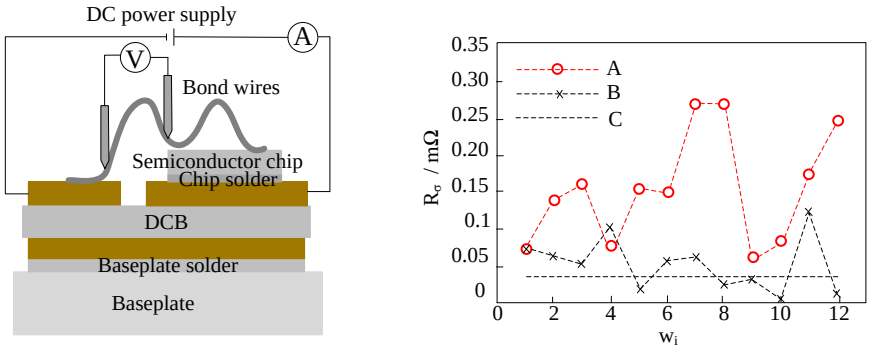
shift is then used to predict bond wire lift-offs. However, the PM requires substantial modifications to the DBC layout.



(a) (b)

Figure 2.19 (a) Modified DBC layout (simplified), (b) Equivalent circuit with and without bond wire lift-off [81].

In [82, 83], a four-point probing method is demonstrated where DC current (1 A to 5 A) is injected to the C-PE, and voltages are measured in various positions to determine the resistance of the corresponding part. Figure 2.20 illustrates the four-point probing measurement technique applied to one part of the bond wire. The measured resistance can then be analysed to detect the ageing influence on bond wires. Dashed lines in Figure 2.20b correspond to resistance deviation of bond wires between new and aged IGBT modules. In Figure 2.20b, the resistance increases with the number of power cycles in all these PMs.



(a) (b)

Figure 2.20 (a) Four-point probing measurement method on a single bond wire, (b) Resistance deviation of wires in different sections in three IGBT modules (A, B and C) [82].

2.2.3. Induced signatures

Induced signatures have been studied in addition to intrinsic signatures. These methodologies apply an additional signal to the device. The response of the excitation signal, as an induced signature, is investigated to evaluate the bond wire state.

In [84], electromagnetic induction thermography is applied to an IGBT. The schematic of the setup is shown in Figure 2.21. The IGBT is placed at the centre of coils. When there is current flowing through the coil, a magnetic field is generated. The conductive material in the magnetic field will be heated by the eddy current. In this case, pure resistive heat is produced in the bond wires. The heat generated is reflected in temperature distribution. When there is a defect in the bond wires, the temperature will change accordingly.

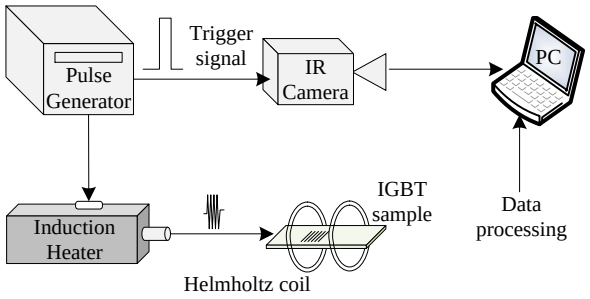


Figure 2.21 Eddy current pulsed thermography system diagram [84].

The temperature distributions of good and defective bond wires are compared in Figure 2.22. The defected bond wire generates more heat, which leads to a higher temperature variation. This technique is suitable for post-diagnosis.

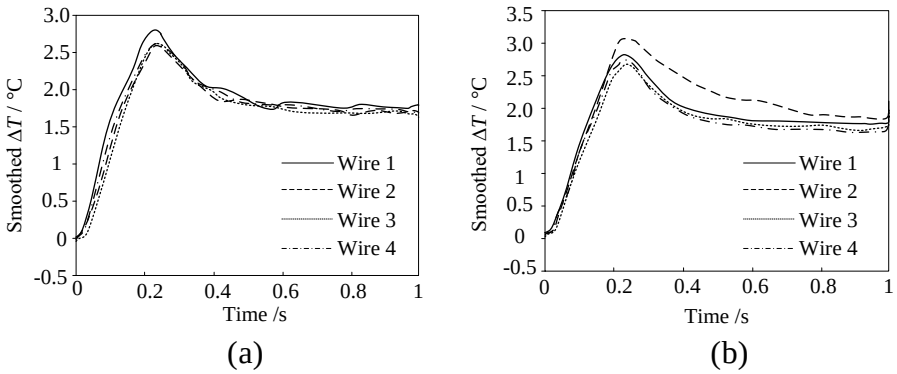


Figure 2.22 Experimental results under uniform magnetic field excitation: (a) The temperature distribution of well-bonded wires, (b) The temperature distribution when wire 2 is defective.

In [85], the deteriorating condition of the IGBT module is estimated via spread spectrum time domain reflectometry (SSTDR) technique. Figure 2.23 illustrates the operational principle of the SSTDR technique. First, the sine wave is converted into a square wave by what is called a shaper. The square wave is then used to drive the pseudo-noise digital sequence generator (PN Gen). The output of the PN Gen is multiplied with the sine wave. The product is injected into the DUT. A signal is reflected back from the DUT. The captured reflection signal and the reference signal are reproduced and fed into an integrator for analysis. Any fault in the DUT

will cause a change in the impedance. This will lead to a variation in the received signal. Therefore, the difference between the received signal and the reference signal is examined to diagnose the fault.

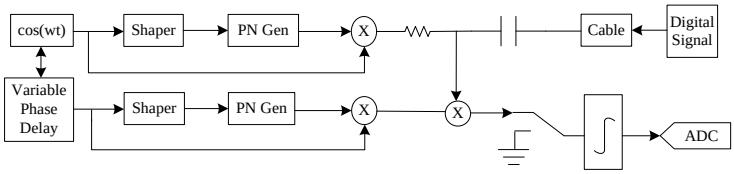


Figure 2.23 SSTDR technique [86].

As explained in Figure 2.15, the circuitry between different terminals in an IGBT module is equivalent to an RLC circuit. Degradation of the IGBT will lead to variation in the RLC circuitry. Authors in [85] applied the SSTDR technique to C-PE and G-AE to detect the deviation caused by ageing. Figure 2.24 and Figure 2.25 are the results at different load conditions. There is a pattern between SSTDR amplitude and the degradation.

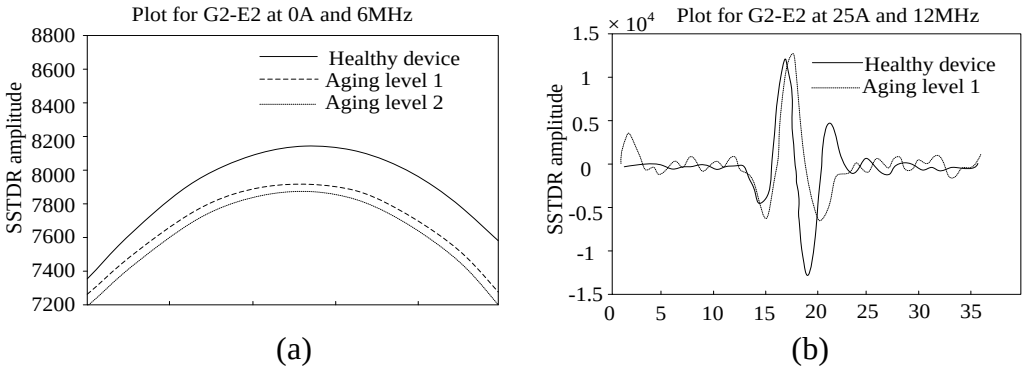


Figure 2.24 SSTDR auto-correlated amplitude plot with SSTDR applied across the gate-emitter terminals: (a) The plot at 0 A and 6 MHz, (b) The plot at 25 A and 12 MHz.

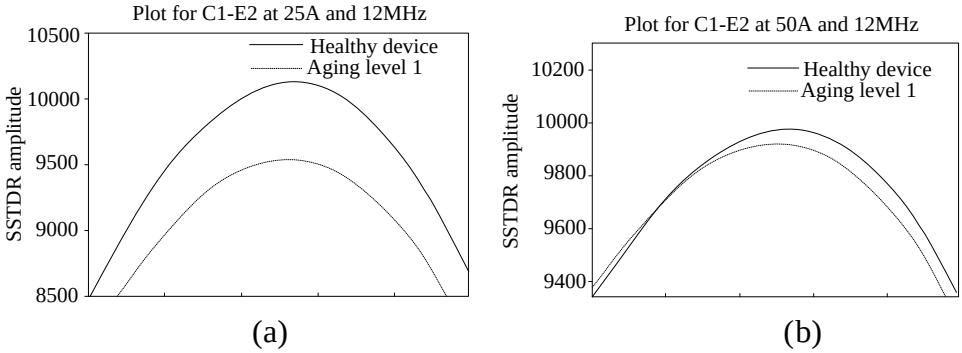


Figure 2.25 SSTDR auto-correlated amplitude plot with SSTDR applied across the collector-emitter terminals: (a) The plot at 25 A and 12 MHz, (b) The plot at 50 A and 12 MHz.

2.2.4. Discussion

The approaches proposed so far are summarised in Table 2.2. Among them, on-state voltage is the most popular technique for bond wire state diagnosis, because its variation against bond wire lift-off is detectable and it can be measured without any modification to the IGBT module.

The advantage of the techniques developed at AE is that they are measured on the low voltage side. The disadvantage is the low sensitivity that only chip failures (not individual bond wires) is detectable. Sense point method and four-point probe method are more useful for characterisation of mIGBTs. The four-point probing method requires many tests as each bond wire must be tested individually and tests on different positions in the same bond wire must be conducted as well. SSTDR approach is very promising because it can be employed in online application.

In conclusion, most of the existing techniques are applied to single-chip devices and only bond wire state is monitored. When these approaches are utilised in multi-chip PMs, the detection of the first few bond wire lift-offs will be challenging because of a large number of bond wires. Moreover, some of the techniques require multiple tests or parameters to eliminate the influence of T_{vj}.

Furthermore, bond wire lift-off in one chip will lead to current redistribution across all the chips, and as such some chips will work under a higher stress load than others and be pushed to work towards their limitations. Consequently, these chips will fail earlier. Estimation of the current redistribution helps to identify the electrical pressure on these chips. Therefore, it is essential to investigate the bond wire state in mIGBT PMs, locate the bond wire lift-off and estimate the current sharing after a fault occurs.

Table 2.2 Comparison of existing techniques for bond wire state estimation

Category	Location	Signatures	Number of IGBT chips	Number of bond wires[2]	Variation at bond wire lift-off
Intrinsic signatures	PE	$V_{CE(on)}$ [20]	1	NA[1]	NA[1], 200 mV increase by end of life
		$V_{CE(on)}$ [66]	1	6	20 mV for first lift-off
		$V_{CE(on)}$ at inflexion point (Peng et al., 2017)	1	NA[1]	180 mV (Discrete IGBT used) for first lift-off
		$R_{CE(on)}$ (Eleffendi and Johnson, 2017)	2	8	0.1 mΩ for second lift-off
		$\Delta V_{CE(turn\text{-}off)}$ (Bryant et al., 2006)	2	24	20 V increase for four lift-offs
	AE	V_{GE} (Zhou et al., 2013a)	2	12	Only visible variance at chip failure
		I_G (Zhou et al., 2013b)	2	12	Only visible variance at chip failure
		R_{Ee} (Farokhzad et al., 1996)	1	NA[1]	25 mΩ increment by end of life
	KE	Sense point (Lehmann et al., 2003)	2	4	0.7 V difference for first lift-off
		Four-point probe (Pedersen et al., 2015)	2	12	0.15 mΩ increment by end of test
Induced signatures	NA[1]	Eddy current (Li et al., 2014)	1	4	0.5 °C increment for first wire defect
	PE	SSTDR (Hanif et al., 2018)	3	24	2% change by end of life
	KE	SSTDR (Hanif et al., 2018)	3	24	5.53% change by end of life

[1]Not applicable means there is no information about the property in the paper.
[2]Total number of bond wires in the test module.

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2.3. **Summary**

It is essential to obtain information of T_{vj} and bond wire state for IGBT modules regarding health monitoring. This chapter provides an overview of techniques for T_{vj} estimation and bond wire lift-off monitoring. A brief comparison between different techniques has also been conducted based on the findings to understand the advantages and drawbacks of each technique. Research gaps have also been identified accordingly.

Chapter 3. T_{vj} estimation in multi-chip IGBT modules

Chapter 2 highlights that most research on T_{vj} estimation is either conducted on single-chip IGBTs or conducted based on the assumption that the mIGBT has uniform temperature distribution among all chips. This assumption, however, is unrealistic as the temperature for each semiconductor chip varies in an mIGBT, which is mainly due to intrinsic package differences and variations in degradation over time. For instance, in [87] and [51], the temperature variations measured between chips is about 5 °C and 15 °C, respectively. About 10 °C variance is captured across the chip surface by [88]. The difference in T_{vj} between different chips is remarkable and therefore should not be ignored. Consequently, it is of paramount importance to scrutinise the SDoT in an mIGBT. Comprehensive investigation of the impact of SDoT on mIGBTs is carried out in this chapter.

3.1. **Existing research on the impact of SDoT**

So far, only a few publications exist that investigate SDoT. In 2014, Sundaramoorthy explored the impact of SDoT on T_{vj} estimation in a two-chip IGBT module. In [41, 42], a lateral temperature difference is created between IGBT chips with a heater and fan cooler. A double pulse test is conducted to capture the Miller plateau width t_{Miller} for T_{vj} estimation. The baseplate temperature is measured to represent the temperature of the IGBT chips. However, the measurement point is not an accurate assumption of the chip temperature.

In 2015, $V_{CE(on\text{-}load)}$ and $V_{CE(on\text{-}sense)}$ were studied to estimate T_{vj} during power cycling [89]. A current pulse train was injected into the IGBT module. Then, the temperature of the IGBT chip was measured using an infrared (IR) camera (SC5500/SC7500 MWBB). The results showed that there was significant temperature divergence within one chip at the end of the current pulse. Furthermore, a notable estimation error of $V_{CE(on\text{-}load)}$ was reported. A complementary approach was provided in the paper to improve the dynamic response of $V_{CE(on\text{-}load)}$.

Internal gate resistor $R_{g(int\text{-}chip)}$ is another parameter that has been studied for T_{vj} estimation in mIGBT [51]. In this paper, both $R_{g(int\text{-}chip)}$ and $V_{CE(on\text{-}sense)}$ are captured for an mIGBT PM. The ITD condition is created between two IGBT chips, with one chip kept at 100 °C and the T_{vj} of the other chip varying from 60 °C to 140 °C. It is found that the temperature predicted by $R_{g(int\text{-}chip)}$ is close to T_{vj}, whereas the temperature predicted by $V_{CE(on\text{-}load)}$ is slightly higher than T_{vj}.

Table 3.1 Summary of research on SDoT in T_{vj} estimation

Reference	T distribution	ΔT / °C[3]	T tested	TSEPs studied	Estimation T
[41, 42]	Switch level[1]	16–50	Base plate	t_{Miller}	$T = T_{vj}$
[89]	Chip level[2]	25.1–68.3	Chip surface	$V_{CE(on\text{-}load)}$	$T < T_{vj}$
				$V_{CE(on\text{-}sense)}$	$T = T_{vj}$
[51]	Switch level	0–20	Chip surface	$R_{g(int\text{-}chip)}$	$T = T_{vj}$
				$V_{CE(on\text{-}load)}$	$T > T_{vj}$

[1]SDoT across chips in one IGBT switch of the PM
[2]SDoT within one chip in the IGBT switch
[3]$\Delta T = T_{max} - T_{min}$

Table 3.1 contains a comparison of existing SDoT researches. The comparison investigates whether a study focused on temperature distribution across the whole IGBT switch 'switch level' or within one IGBT chip 'chip level', the measured disparity of temperature ΔT, the point where temperature was measured, the applied TSEPs and how the predicted temperature by the TSEP differs from T_{vj}.

In Table 3.1, TSEPs do not always capture T_{vj}. In this case, TSEPs should be chosen cautiously to estimate T_{vj}. Furthermore, an antithetical estimation is found in $V_{CE(on\text{-}load)}$. Additionally, SDoT should be considered at both chip level and switch level to provide a thorough thermal profile.

Table 3.1 shows two outcomes. First, at ITD conditions, the temperature measured with $V_{CE(on\text{-}load)}$ does not represent T_{vj}. Second, there is not enough research conducted in the field of SDoT and often simplistic assumptions have been made, resulting in errors in applications such as thermal model in [90, 91].

Consequently, research on SDoT and T_{vj} estimation in mIGBT is lagging. To rectify this, a comprehensive study is carried out in the following sections to investigate SDoT in an mIGBT module.

3.2. **Investigation of SDoT on FF600R17ME4**

To inspect the temperature distribution within an mIGBT, power cycling experiments are conducted on FF600R17ME4. SDoT is examined at both chip level and switch level, which provide exhaustive SDoT assessment.

3.2.1. Power cycling test setup

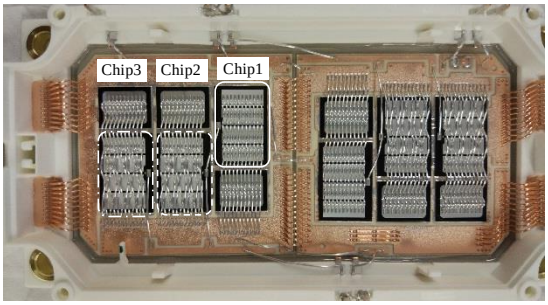


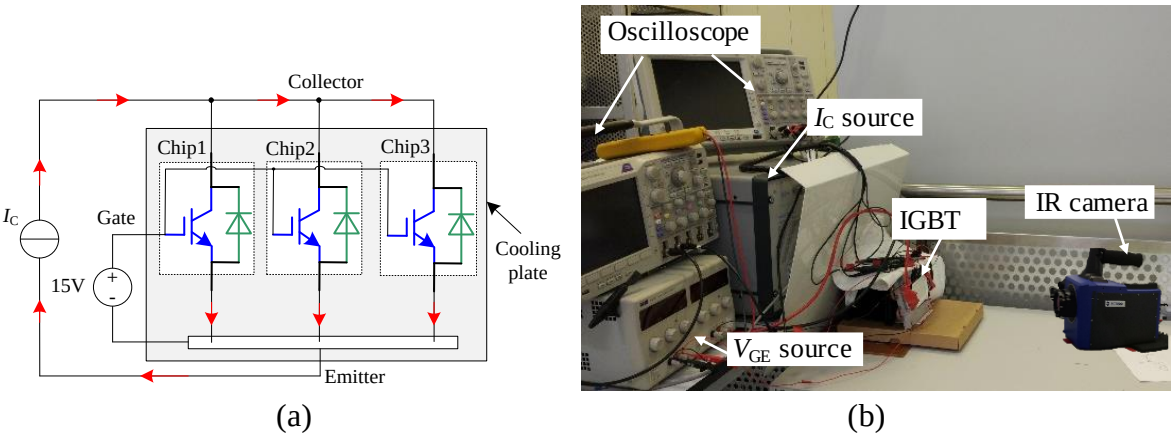
Figure 3.1 Layout of FF600R17ME4 IGBT module.

The FF600R17ME4 IGBT is a 1700 V/600 A half-bridge module from Infineon with three IGBT chips for each switch as shown in Figure 3.1. The chips in one switch are highlighted. These three chips are referred to as Chip1, Chip2 and Chip3. To capture SDoT with the IR camera, the IGBT switch is coated with black matt paint to increase the emissivity of the chip surface. After coating, the emissivity is about 0.95 [84]. Then, the IGBT module is mounted on a water-cooling plate controlled by a chiller (Liquid Cooler WAR7042N07ZTP0 7035). The temperature of the chiller is set to 20 °C. However, in the experiment, the temperature will fluctuate between 17 °C to 22 °C due to the control system of the chiller.

Figure 1.2a shows the schematic of the test rig. During operation, the IGBT is switched on with +15 V on the G-E terminal. Then, a current pulse train is injected into the IGBT through the C-E terminals by the TopCon DC power supply. The IR camera monitors the temperature distribution of the IGBT chips during the test. The test rig is shown in Figure 3.2b. Table 3.2 lists the injected current during the experiment and the ratio of the injected current to the rated current of the PM.

Table 3.2 Load conditions of the IGBT module under test

Test current	180 A	300 A	420 A	540 A
Ratio to rated current / %	30	50	70	90

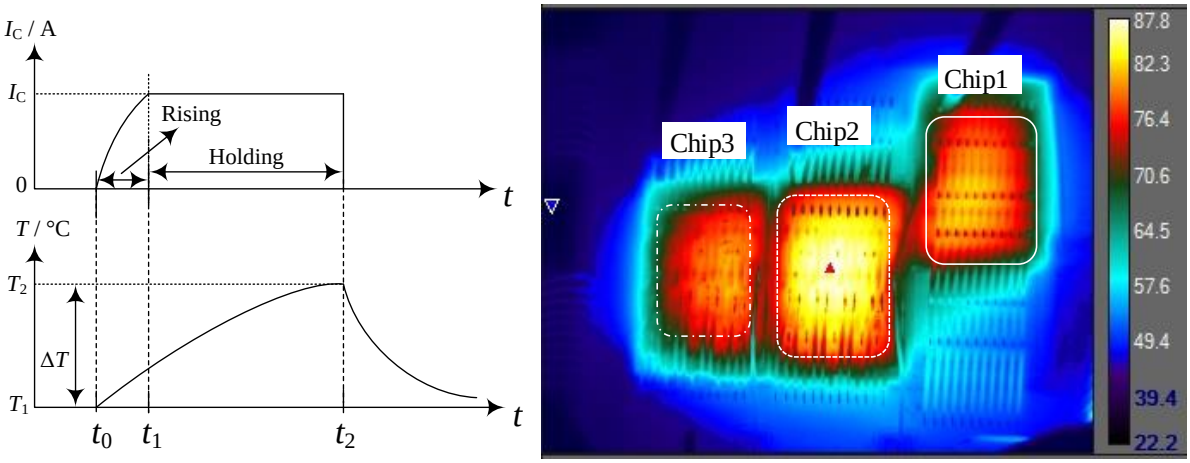


(a) (b)

Figure 3.2 (a) Schematic of the test setup, (b) Setup for $V_{CE(on\text{-}load)}$ measurement.

3.2.2. SDoT assessment

Power cycling tests are carried out to assess the SDoT of the IGBT switch. The device has been excited at different operating conditions by regulating the pulse lengths and load current levels as shown in Figure 3.3.



(a) (b)

Figure 3.3 (a) The current pulse against temperature variation, (b) SDoT after the current (300 A) injection with pulse width t_{pulse} = 12 s.

The temperature variation caused by the injected current is demonstrated in Figure 3.3a. At t_0, the measured temperature is T_1 and the current starts to ramp up. With current injection the temperature will increase too. At t_1, the current reaches the set value which results in a further

increase of the temperature. At t_2, the current is switched off and the temperature has reached its maximum value of T_2. From this point onward the temperature drops until it reaches T_1. The change T_2-T_1 is the temperature swing ΔT. Figure 3.3b shows a snapshot of the temperature distribution of the switch, which is excited by 300A for a pulse length (t_2-t_1) of 12s. The triangle at the centre indicates the hottest spot within the scope of the camera, whereas the triangle at the edge shows the coldest point. The temperature of the chip is higher than that of the bond wires and the temperature of Chip2 is the highest. The full thermal image of the IGBT allows to evaluate the temperature distribution across the three IGBT chips. The rectangles of the thermal image shown in Figure 3.3b map to the active IGBT chip areas of concern. Within each box/chip, there is the maximum temperature, the minimum temperature and the average temperature at each time instant, denoted by $T_{(\max)}$, $T_{(\min)}$, $T_{(\text{avg})}$ respectively.

As mentioned in the previous section, the temperature of the water-cooling plate will fluctuate between 17 °C to 22 °C due to the control system of the chiller. This means the temperature measured at t_0, which is T_1, will fluctuate between 17 °C to 22 °C. The fluctuation will influence the evaluation of spatial temperature distribution if only the temperature at t_2 T_2 is used. For example, with the same pulse length, a higher T_1 with lower inject current may end up with a higher T_2 than that of a low T_1 with high inject current, even through the thermal dispissitation caused by the high inject current is larger. Therefore, the temperature swing ΔT is introduced in Figure 3.3a to represent the thermal influence caused by the current injection. $\Delta T_{(\max)}$, $\Delta T_{(\text{avg})}$ and $\Delta T_{(\min)}$ are the corresponding changes of the maximum temperature $T_{(\max)}$, average temperature $T_{(\text{avg})}$ and minimum temperature $T_{(\min)}$ in the case of current pulse.

The temperature shown in Figure 3.3b is the surface temperature of the IGBT chip. For each IGBT chip, there is a maximum, average and minimum temperature within the chip surface. The temperature swing $\Delta T_{(\max)}$, $\Delta T_{(\text{avg})}$ and $\Delta T_{(\min)}$ are obtained according to (3.1).

$$\begin{aligned} \Delta T_{(\max)} &= T_{(\max)\_t2} - T_{(\max)\_t0} \\ \Delta T_{(\text{avg})} &= T_{(\text{avg})\_t2} - T_{(\text{avg})\_t0} \\ \Delta T_{(\min)} &= T_{(\min)\_t2} - T_{(\min)\_t0} \end{aligned} \tag{3.1}$$

Table 3.3 List of the symbols for temperature difference

Symbol	Maximum	Average	Minimum
Chip1	$\Delta T_{C1(max)}$	$\Delta T_{C1(avg)}$	$\Delta T_{C1(min)}$
Chip2	$\Delta T_{C2(max)}$	$\Delta T_{C2(avg)}$	$\Delta T_{C2(min)}$
Chip3	$\Delta T_{C3(max)}$	$\Delta T_{C3(avg)}$	$\Delta T_{C3(min)}$

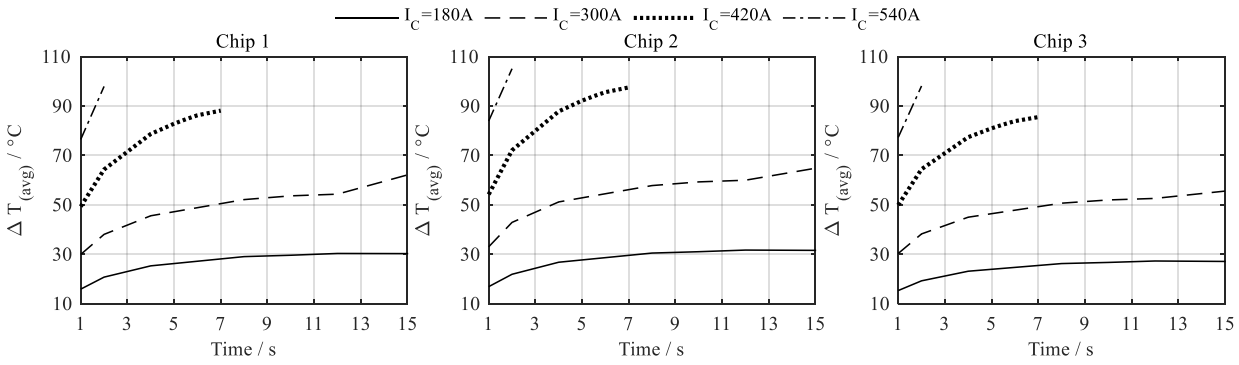


Figure 3.4 $\Delta T_{(avg)}$ against the current level and pulse width.

Notations for the temperature swing of three IGBT chips are listed in Table 3.3. Figure 3.4 displays the average temperature swing $\Delta T_{(avg)}$ for each IGBT chip during the power cycling test. t_{Pulse} varies from 1 s to 15 s. Test at I_C = 420 A is halted at t_{Pulse} = 7 s and test at I_C = 540 A is halted at t_{Pulse} = 2 s. This is to ensure that T_{vj} of the IGBT switch does not exceed the safe operation boundary. Figure 3.4 depicts that $\Delta T_{(avg)}$ of each chip climbs with the rise of the current level I_C as well as t_{Pulse}. The temperature eventually will level out if t_{Pulse} is long enough. The fashion of the temperature increment varies slightly from chip to chip. The chip in the middle (Chip2) is always the hottest, whereas Chip3 is the coldest.

3.2.2.1. SDoT within each chip

SDoT within each chip is evaluated through the maximum temperature difference ($\Delta T_{C(max)}$– $\Delta T_{C(min)}$) on the chip surface. Results for all three chips are depicted in Figure 3.5 as a function of I_C and t_{Pulse}. Figure 3.5 shows that the temperature difference between the hottest and the coldest points of the chips is small for a load current of 180 A. However, a dramatic increase in temperature variance is observed for all three chips at a load current of 300 A, which is 50% of the rated current. The maximum temperature difference in Chip2 ($\Delta T_{C2(max)}$ - $\Delta T_{C2(min)}$) reaches about 60 °C at I_C = 540 A. Overall, the maximum temperature difference ($\Delta T_{C(max)}$ - $\Delta T_{C(min)}$) of each chip varies between 8 °C and 60 °C. Consequently, the SDoT is significant. This will lead to inhomogeneous thermal stress for the IGBT chip, which will cause non-uniform thermal expansion within the silicon IGBT chip layer.

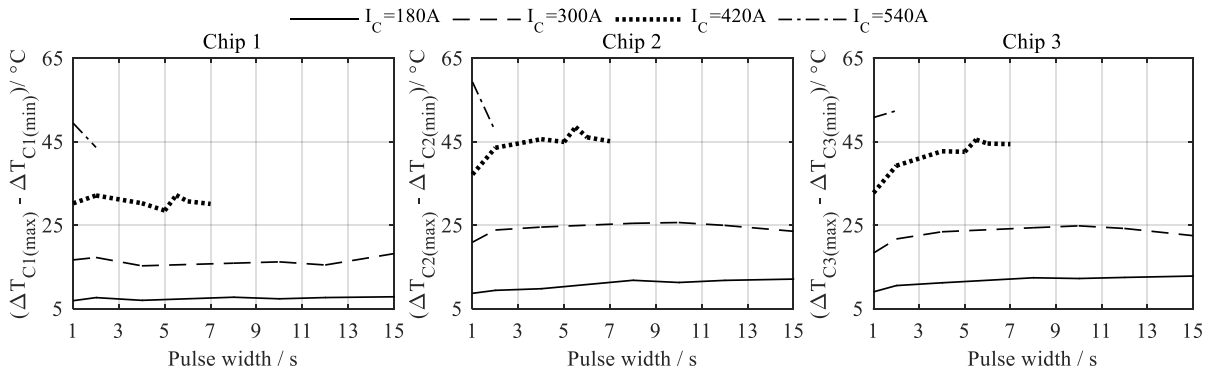


Figure 3.5 Temperature disparity ($\Delta T_{(max)} - \Delta T_{(min)}$) within the IGBT chip.

3.2.2.2. SDoT within the IGBT switch

SDoT within the IGBT switch is evaluated via the maximum disparity of the temperature swing among the three IGBT chips. It should be pointed out that the maximum disparity is compared in the same category. Therefore, corresponding to $\Delta T_{C(max)}$, $\Delta T_{C(avg)}$ and $\Delta T_{C(min)}$, the maximum disparities within the IGBT switch are classified into $\Delta^2 T_{S(max)}$, $\Delta^2 T_{S(avg)}$ and $\Delta^2 T_{S(min)}$. The definitions of the disparity are expressed in (3.2).

$$\begin{aligned}
\Delta^2 T_{S(\max)} &= \max(\Delta T_{C1(\max)}, \Delta T_{C2(\max)}, \Delta T_{C3(\max)}) - \min(\Delta T_{C1(\max)}, \Delta T_{C2(\max)}, \Delta T_{C3(\max)}) \\
\Delta^2 T_{S(avg)} &= \max(\Delta T_{C1(avg)}, \Delta T_{C2(avg)}, \Delta T_{C3(avg)}) - \min(\Delta T_{C1(avg)}, \Delta T_{C2(avg)}, \Delta T_{C3(avg)}) \\
\Delta^2 T_{S(\min)} &= \max(\Delta T_{C1(\min)}, \Delta T_{C2(\min)}, \Delta T_{C3(\min)}) - \min(\Delta T_{C1(\min)}, \Delta T_{C2(\min)}, \Delta T_{C3(\min)})
\end{aligned} \tag{3.2}$$

The maximum disparity among three IGBT chips is illustrated in Figure 3.6. In general, the $\Delta^2 T_{S(max)}$, $\Delta^2 T_{S(avg)}$ and $\Delta^2 T_{S(min)}$ still rise with I_C and t_{Pulse} increase. Since the disparity is acquired in the same category, the disparity among the three chips is between 2 °C to 16 °C. The $\Delta^2 T_{S(max)}$ of the IGBT switch is 2 °C - 10 °C, which is about 2 °C lower than $\Delta^2 T_{S(avg)}$. The highest disparity is observed in $\Delta^2 T_{S(min)}$, which is 2 °C - 16 °C. Unlike the other two, $\Delta^2 T_{S(min)}$ is almost the same at all current levels when the current pulse width is narrow. The reason is that the minimum temperature is apt to designate the temperature of the bond wires. When the pulse width is short, the temperature deviation caused by the current is negligible.

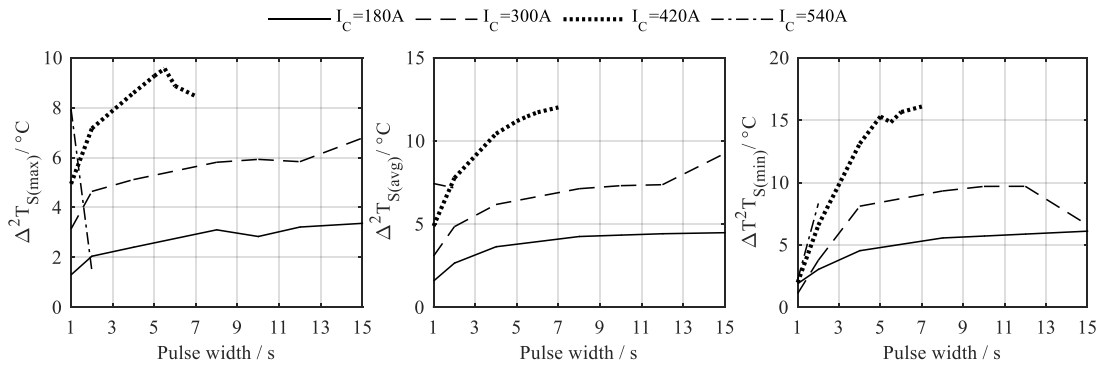


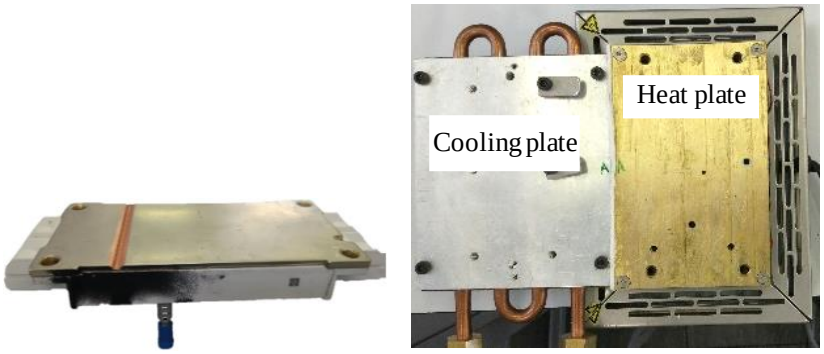
Figure 3.6 Temperature disparity among three IGBT chips.

The SDoT across three IGBT chips will lead to unsynchronised switching behaviour as well as the distinct health condition level of each chip. These, in turn, will influence the health condition of the IGBT module. Therefore, it is imperative to quantify the influence of the SDoT on the characteristics of the IGBT module.

3.3. **Experimental setup for TSEP measurement**

The experimental setup is designed to capture different TSEPs of an IGBT PM that experiences either HTD or ITD. The setup of the test bench is introduced in this section. The captured results are utilised to assess the impact of SDoT on T_{vj} estimation and current distribution in mIGBT modules in the following section.

For HTD tests, an IGBT module is mounted on a controllable heating plate. The module is heated for enough time to form a uniform temperature distribution condition prior to the measurement. For ITD tests, a temperature distribution emulator is constructed to set the temperature of chips individually. A trapezoidal slot is grooved on the base plate of the IGBT module, as shown in Figure 3.7a. The slot is between Chip2 and Chip3. A thermal isolation layer (calcium-magnesium silicate thermal insulation sheet) is inserted into the slot to maximise the thermal isolation between the adjacent chips. The modified IGBT is then placed on a specially designed heat plate in Figure 3.7b. The heat plate combines a water-cooling plate and an electronic heater plate. The water-cooling plate is connected to a liquid chiller, and the temperature is kept constant. The temperature of the heat plate is regulated via Weller WHP300 and can, therefore, be varied. With this arrangement, the temperatures of Chip1 and Chip2 can be adjusted so that they are different from Chip3.



(a) (b)

Figure 3.7 (a) Groove in the baseplate of the IGBT, (b) Heat plate for T_{vj} control.

3.3.1. Static TSEP test bench

On-state voltage $V_{CE(on\text{-}load)}$ and $V_{CE(on\text{-}sense)}$ are the two prevalent TSEPs. The test rig shown in Figure 3.2a was modified to test $V_{CE(on\text{-}load)}$ and $V_{CE(on\text{-}sense)}$ at both HTD and ITD conditions. The complete test rig is shown in the appendix. $V_{CE(on\text{-}load)}$ is measured at 300 A and $V_{CE(on\text{-}sense)}$ is measured at 100 mA.

3.3.2. Dynamic TSEP test bench

Dynamic TSEPs are captured using a double pulse circuit, as shown in Figure 3.8a. The double pulse circuitry is equivalent to an RLC circuit. Their relationship can be expressed as (3.3).

$$\left.\begin{aligned} C\frac{dV_{DC}}{dt} &= -I_C \\ L\frac{dI_C}{dt} &= V_L \\ V_L &= V_{DC} - V_R \end{aligned}\right\} \tag{3.3}$$

Where, R is the resistance. L is the inductance. C is the capacitance. V_L and V_C are the voltages across the inductor and capacitor, respectively. I_C is the current flowing through the circuit.

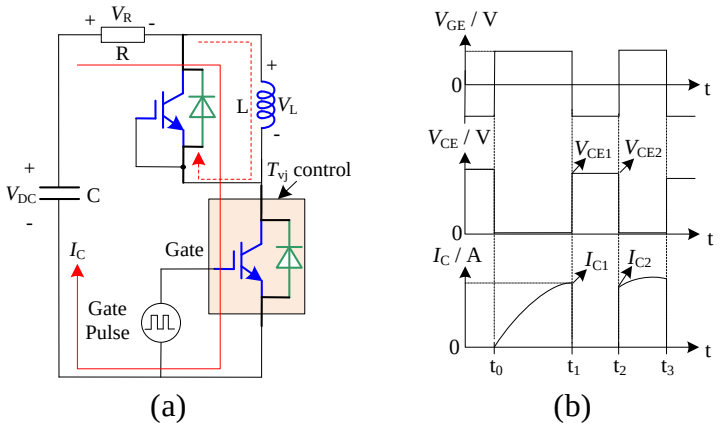


Figure 3.8 (a) Double pulse test circuitry, (b) Double pulse switching sequence.

Equation (3.4) can be derived from (3.3).

$$LC\frac{d}{dt}\left(\frac{dV_{DC}}{dt}\right)+CR\frac{dV_{DC}}{dt}+V_{DC}=0 \tag{3.4}$$

Equation (3.4) is a second-order homogeneous equation. The general solution for it is (3.5).

$$\left.\begin{aligned} V_{DC} &= c_1e^{r_1t}+c_2e^{r_2t} \\ I_C &= -C(c_1r_1e^{r_1t}+c_2r_2e^{r_2t}) \end{aligned}\right\} \tag{3.5}$$

Where c_1 and c_2 are the coefficient, $r_1=\dfrac{-\dfrac{R}{L}+\sqrt{\dfrac{R^2}{L^2}-\dfrac{4}{LC}}}{2}$, $r_2=\dfrac{-\dfrac{R}{L}-\sqrt{\dfrac{R^2}{L^2}-\dfrac{4}{LC}}}{2}$.

The switching sequence is detailed in Figure 3.8b. Phase t_0 - t_1 is intended to allow the current to build up. Phase t_1 - t_2 is designed so that deviations of I_C and V_{CE} at t_1 and t_2 are acceptable. The time between t_0 and t_1 is determined by the voltage level of the DC-link capacitor and the current level required. The time between t_1 and t_2 should be long enough to cover the switching transient and short enough to reduce the current decrement during turn-off. The pulse width should be chosen so that (3.6) is satisfied.

$$\left.\begin{aligned} V_{CE(t_1)} &\approx V_{CE(t_2)} \\ I_{C(t_1)} &\approx I_{C(t_2)} \end{aligned}\right\} \tag{3.6}$$

The right pulse width guarantees that TSEPs are captured in the same operational conditions so that I_C and V_{CE} always have the same level, respectively. In addition, V_{GE} is kept constant during the test. With this control arrangement, electrical parameters during the turn-off and turn-on

transient are solely subjected to T_{vj} variance. The operation conditions of this experiment are listed in Table 3.4.

Table 3.4 Operation condition of the double pulse test

Parameter	Value
Current limiting resistor	1.6 Ω
Inductor	400 µH
DC link capacitor	780 µF
$\|t_1\text{-}t_0\|$	300 µs
$\|t_2\text{-}t_1\|$	100 µs
$\|t_3\text{-}t_2\|$	100 µs

The electrical parameters that have been recorded are illustrated in Figure 3.9. V_{GE}, I_G, V_{CE} and I_C are measured to acquire the TSEPs mentioned in Chapter 2. Additionally, the collector current of Chip1 and Chip3 are also recorded (I_{C1} and I_{C3}). The chip current is measured through the Rogowski coil (CWT Ultra mini, CWTUM/6/B) with all the emitter bond wires in the coil. The placement can be seen in the appendix. The collector current of Chip2 is calculated using Kirchhoff's law. The data are used to study the impact of SDoT on the current distribution among the IGBT chips.

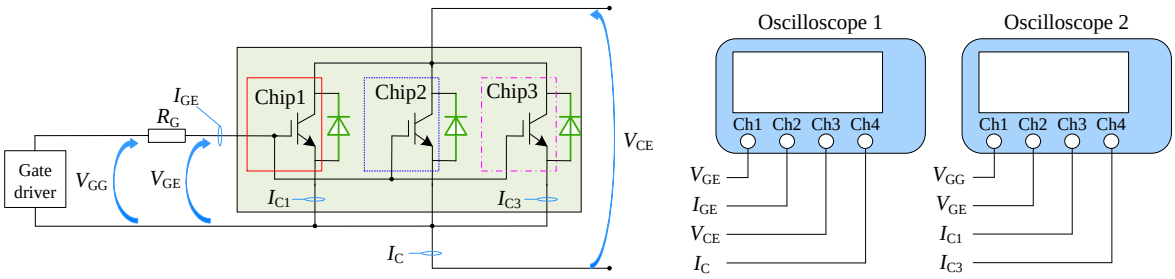


Figure 3.9 Schematic of the parameter measurement.

Several assumptions are made when interpreting the results. First, the shielding effect caused by bond wires is not considered when using the IR camera. Thus, it is assumed that the measured average surface chip temperature is equal to T_{vj}. Second, it is assumed that the power loss caused by a single switch sequence is insignificant, so temperature variation caused by self-heating is negligible.

3.4. **Homogenous temperature distribution tests**

Static and dynamic TSEPs tests have been conducted to capture the electrical parameters V_{GE}, I_G, V_{CE} and I_C with the oscilloscope. The temperature is varied with an electronic heater. Once a new temperature is applied, enough heating time is given prior the commencement of the test to ensure that HTD has been met. In this thesis, the average temperature of the IGBT switch is treated as T_{vj}. The average temperature of the three-chip IGBT is deduced according to (3.7).

$$T_{vj} = T_{S(avg)} = \frac{T_{C1(avg)} \times S_1 + T_{C2(avg)} \times S_2 + T_{C3(avg)} \times S_3}{S_1 + S_2 + S_3} \tag{3.7}$$

Where, S_1, S_2 and S_3 are the areas of the surface of Chip1, Chip2 and Chip3, respectively.

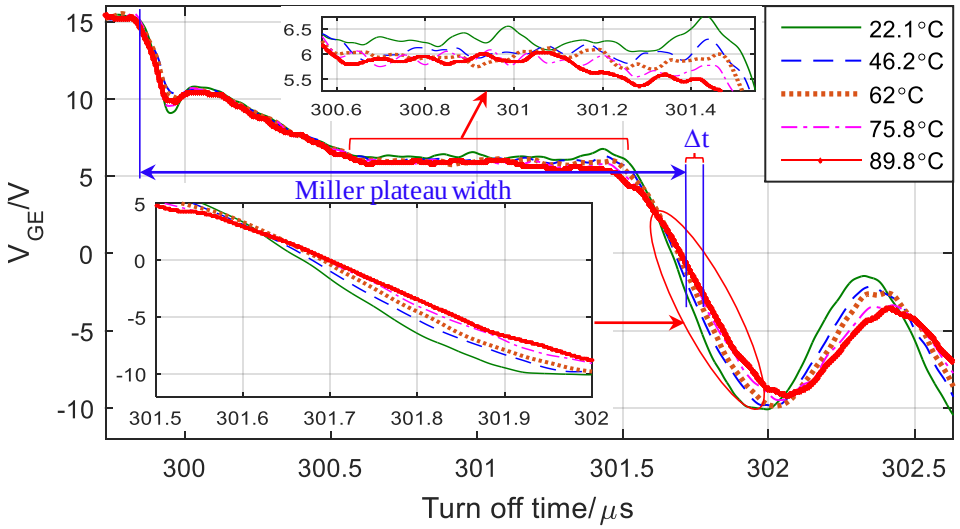


Figure 3.10 Turn-off transient of V_{GE}.

Figure 3.10 shows the turn-off transient of V_{GE} against T_{vj}. The temperature dependency of the $V_{GE(Miller)}$ and T_{Miller} are due to the donor and acceptor number increment in the drift region at high temperature. This lead to the increment of depletion capacitance and Miller capacitance. The increment of the miller capacitance lead to the longer plateau width and lower Miller plateau voltage [41].

Overall, the Miller plateau voltage decreases with temperature rise. However, there are fluctuations in the waveforms, so the root mean square value of the Miller plateau voltage $V_{GE(Miller)}$ is deployed for T_{vj} estimation. The duration between the first descent of V_{GE} and the second descent of V_{GE} is treated as the Miller plateau width T_{Miller} [43]. A reproducible shift is

detected in the waveform, which is the variation caused by T_{vj} change. The detailed temperature dependency is shown in

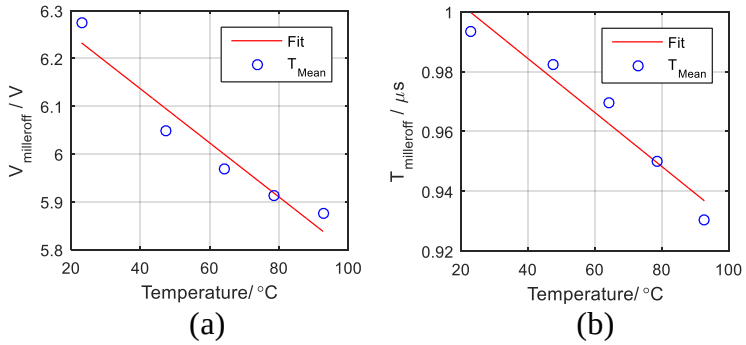


Figure 3.11 Turn-off transient of V_{GE}. TSEPs at HTD condition: (a) V_{Miller}, (b) T_{Miller}.

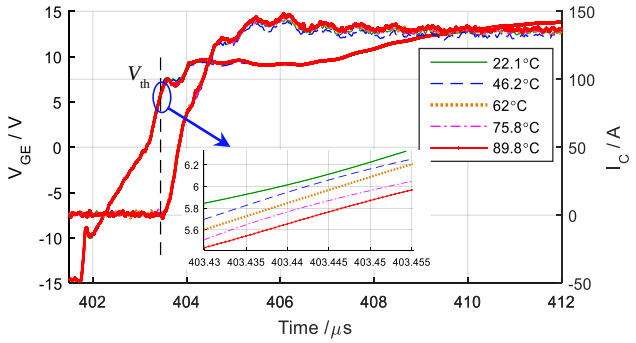


Figure 3.12 Turn-on transient of V_{GE}.

Figure 3.12 is the turn-on transient of V_{GE}. Threshold voltage V_{th} varies linearly against temperature. Figure 3.13 describes the turn-off transient of I_C and V_{CE}. Reproducible shifts are established with temperature variation. TSEPs from I_C including the current slope dI_C/dt during the first stage and the current tail $I_{C(tail)}$, which is defined as the start current during the second stage of the turn-off transient. The on-state voltage drop of IGBT is smaller compared to MOSFET with the same current density and voltage range due to the injection of minority carriers. The minority carriers are injected are injected at turn-on and have to be recollected at turn-off. This causes the tail current during turn-off. High temperature lead to the longer lifetime of the carriers and slow down the recombination speed. Thus, dI_C/dt shows negative temperature coefficient. dV_{CE}/dt and $V_{CE(peak)}$ are the TSEPs from the turn-off transient of V_{CE}.

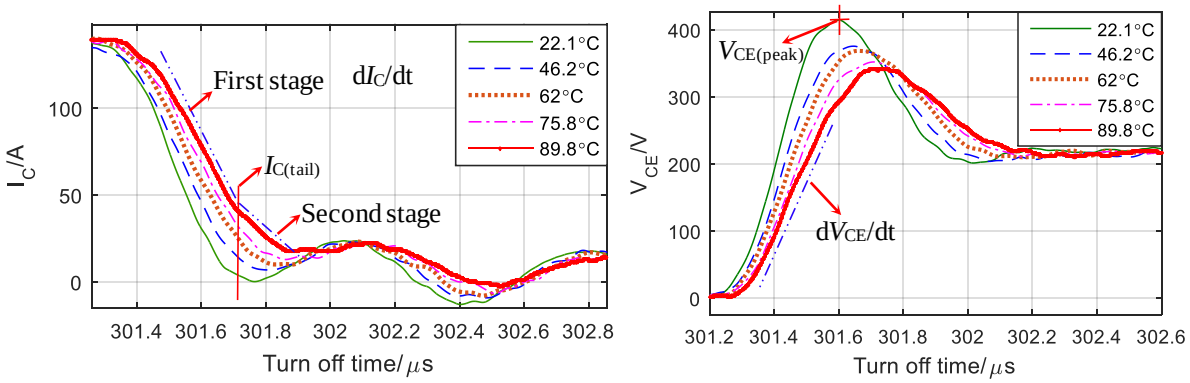


Figure 3.13 Turn-off transient of I_C and V_{CE}.

Most TSEPs express good linearity against T_{vj} at HTD condition. A detailed comparison among the TSEPs is listed in Table 3.5. The sensitivities of the measured TSEPs are similar to the sensitivities reported by other researchers, which are provided in Table 2.1.

In Table 3.5, the widely popularised $V_{CE(on)}$ displays outstanding linearity. In terms of T_{vj} estimation, the sensitivity of $V_{CE(on\text{-}load)}$ is slightly better than $V_{CE(on\text{-}sense)}$. For TSEPs at the low voltage side, the threshold voltage $V_{GE(th)}$ and $V_{GE(Miller)}$ provides a similar sensitivity, 5.7 mV/°C and 5.6 mV/°C, respectively. At the high voltage side, despite the extremely short switching transient, dynamic TSEPs still demonstrate superb linearity. C-E voltage slope dV_{CE}/dt delivers remarkable sensitivity. Overall, the best linearity is provided by $V_{CE(on\text{-}sense)}$ and $I_{C(tail)}$. The linearity of dI_C/dt, however, is not as good as that of others and is therefore not recommended for T_{vj} estimation.

Table 3.5 Sensitivity of TSEPs

	TSEPs	Sensitivity(/°C)	Temperature coefficient	Linearity
On State	$V_{CE(on\text{-}load)}$	2.75 mV	Positive	0.9921
	$V_{CE(on\text{-}sense)}$	2.069 mV	Negative	0.9948
Turn on	$V_{GE(th)}$	5.7 mV	Negative	0.9894
	T_{Miller}	0.9 ns	Negative	0.9411
	$V_{GE(Miller)}$	5.6 mV	Negative	0.9393
	dV_{CE}/dt	10.06 V/μs	Negative	0.9838
Turn off	dI_C/dt	2.007 A/μs	Negative	0.8892
	$V_{CE(peak)}$	1.02 V	Negative	0.9645
	G_m	0.9358 S	Negative	0.9861
	$I_{C(tail)}$	0.563 A	Positive	0.9958

3.5. **ITD tests**

The temperatures of the chiller and electric heater are controlled to differentiate the temperature of each IGBT chip. Three tests are conducted with the temperature of the chiller set at a constant 15 °C and the temperature of the electronic heater setting at 48 °C, 70 °C and 90 °C, respectively. The tests are referred to as Test 1, Test 2 and Test 3 in the following context. Figure 3.14 is an example of the temperature profile of Test 3. The temperature of Chip1 is always the hottest.

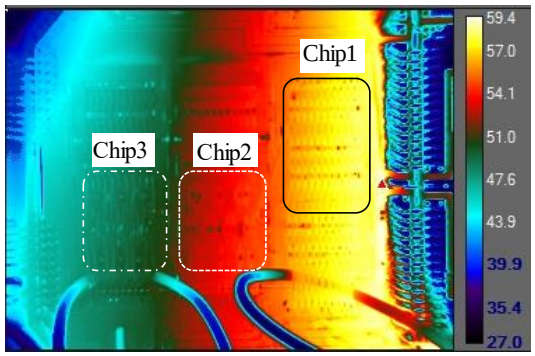


Figure 3.14 Thermography of the mIGBT under test. Chiller set at 15 °C and heater set at 90 °C (Test 3).

The temperature distribution of each chip is analysed. The three boxes in Figure 3.14 highlight the area used for the temperature reading of each chip. The boxes for Chip2 and Chip3 are shrunk intentionally to avoid the influence of the current sensor. The maximum, average and minimum temperature within each box are recorded. The temperatures of the three-chip IGBT switch are deduced according to (3.7) and (3.8). The temperature values are shown in Table 3.6.

$$T_{S(\max)} = \max(T_{C1(\max)}, T_{C2(\max)}, T_{C3(\max)})$$
$$T_{S(\min)} = \min(T_{C1(\min)}, T_{C2(\min)}, T_{C3(\min)}) \quad (3.8)$$

For the three tests (Test 1, Test 2 and Test 3), the average temperatures of the IGBT switch are 32.5 °C, 43.5 °C and 52.4 °C, respectively. The maximum temperature disparity is between Chip1 and Chip3. The maximum temperature differences across the three IGBT chips are 4.3 °C, 6.2 °C and 8.8 °C for the three tests. This falls into the same range as shown in Figure 3.6, which links the tests closely to the real operation condition. In general, Chip2 and Chip3 have a higher difference between the maximum and minimum temperature of the chip. This is

mainly because the groove lies between Chip2 and Chip3, which brings down the minimum temperature and expands the temperature variation.

Table 3.6 Temperatures for ITD tests

T / °C		$T_{(max)}$	$T_{(avg)}$	$T_{(min)}$	$\Delta T_{(max)}$
Test 1	Chip1	35.5	34.6	33.3	2.2
	Chip2	34	33	31.5	2.5
	Chip3	32	30.8	29	3
	$\Delta T_{(max)}$	3.5	3.8	4.3	NA[(1)]
	IGBT switch	35.5	32.5	29	6.5
Test 2	Chip1	48	45.7	44.2	3.8
	Chip2	45.4	44	40.8	4.6
	Chip3	42.1	40.4	38	4.1
	$\Delta T_{(max)}$	5.9	5.3	6.2	NA
	IGBT switch	48	43.5	38	10
Test 3	Chip1	58.6	56.9	53.2	5.4
	Chip2	55.1	53	48.1	7
	Chip3	50.4	48.2	44.4	6
	$\Delta T_{(max)}$	8.2	8.7	8.8	NA
	IGBT switch	58.6	52.4	44.4	14.2

[(1)]Not applicable.

3.5.1. Impact of ITD on TSEPs for T_{vj} estimation

Figure 3.15 and Figure 3.16 show the turn-off transients of the C-E side at ITD condition. The results for 22.1 °C and 89.8 °C at HTD are added for comparison with the ITD results. Regardless of the uneven temperature distribution, there is still a clear shift against temperature variation. The shift can be acknowledged in both V_{CE} and I_C.

Figure 3.17 and Table 3.7 summarise the results. Figure 3.17 displays each TSEP against T_{vj} at both HTD and ITD conditions. The closest fit between HTD and ITD is from $V_{CE(on\text{-}sense)}$, indicating that $V_{CE(on\text{-}sense)}$ is a good TSEP for T_{vj} estimation in mIGBTs. However, the temperature estimations from $V_{CE(on\text{-}load)}$, dV_{CE}/dt and $V_{CE(peak)}$ are lower than T_{vj}, and the temperature estimations from g_m and $I_{C(tail)}$ are higher than T_{vj}. It can be concluded that SDoT must be considered when determining the T_{vj} with TSEP. TSEPs should be selected cautiously when they are applied to mIGBT PMs for T_{vj} estimation. The possible reasons for this are analysed in the following sections.

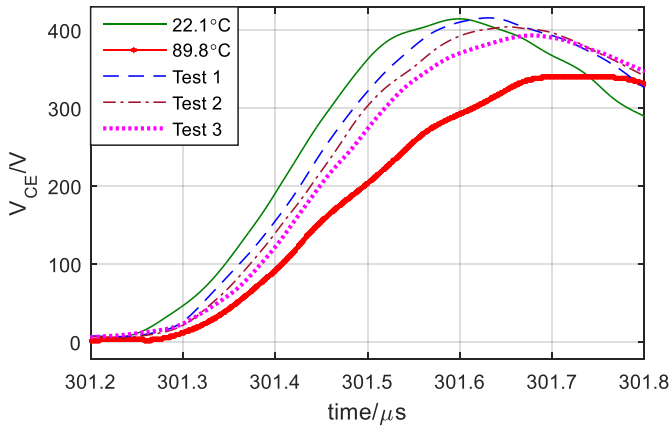


Figure 3.15 V_{CE} during turn-off transient. Solid line: HTD tests. Dashed line: ITD tests.

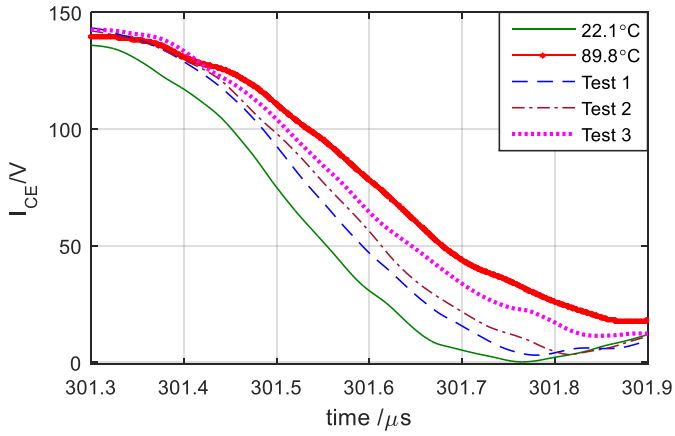


Figure 3.16 I_C during turn-off transient. Solid line: HTD tests. Dashed line: ITD tests.

Table 3.7 Estimation comparison of selected TSEPs

	TSEPs	Predicted T
On State	$V_{CE(on\text{-}load)}$	$T < T_{vj}$
	$V_{CE(on\text{-}sense)}$	$T \approx T_{vj}$
	dV_{CE}/dt	$T < T_{vj}$
Turn off	$V_{CE(peak)}$	$T < T_{vj}$
	g_m	$T > T_{vj}$
	$I_{C(tail)}$	$T > T_{vj}$

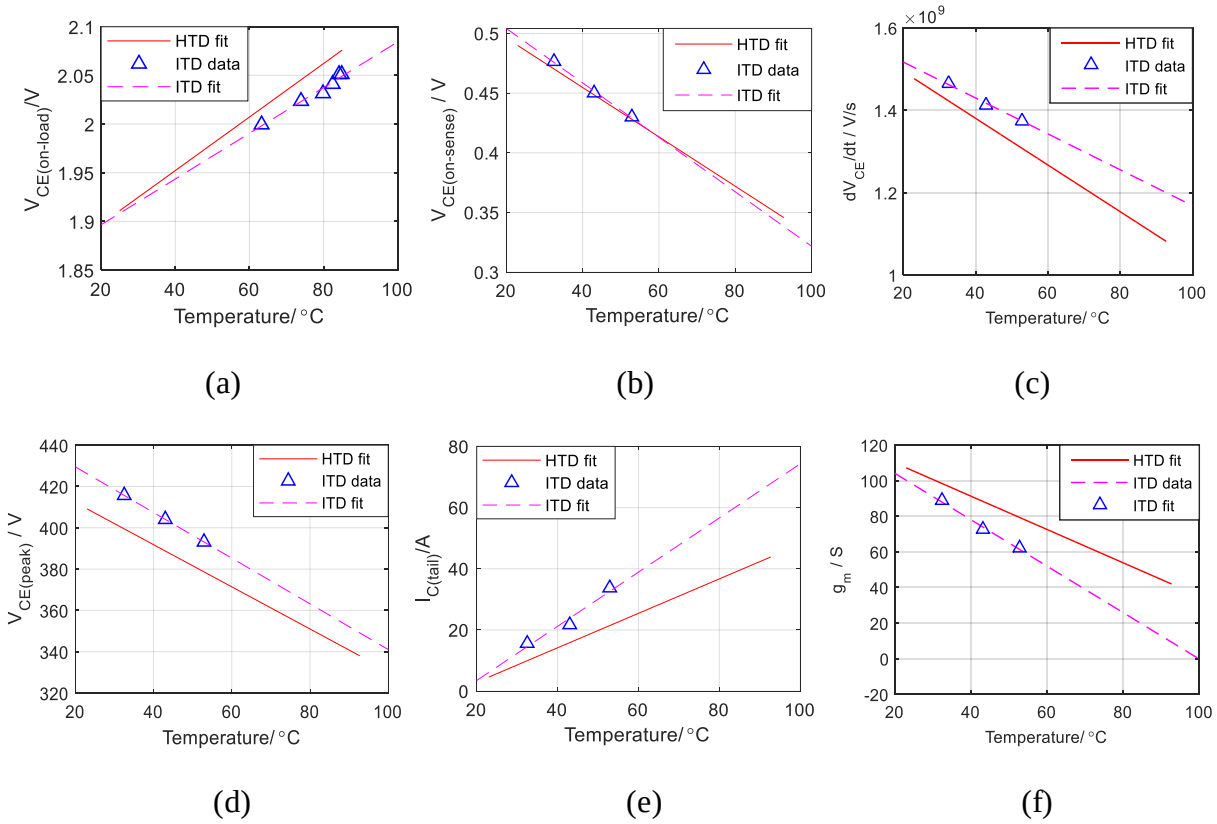


Figure 3.17 TSEPs for T_{vj} in the mIGBT: (a) $V_{CE(on\text{-}load)}$, (b) $V_{CE(on\text{-}sense)}$, (c) dV_{CE}/dt, (d) $V_{CE(peak)}$, (e) $I_{C(tail)}$, (f) g_m.

3.5.2. Influence of ITD on collector current I_C distribution

Figure 3.18 is an example of I_C distribution at HTD condition. The current distributions of all the tests are described in the appendix. Noticeably, the current distribution is not uniform among the three IGBT chips. The current share in Chip2 is the largest and that of Chip3 is the smallest.

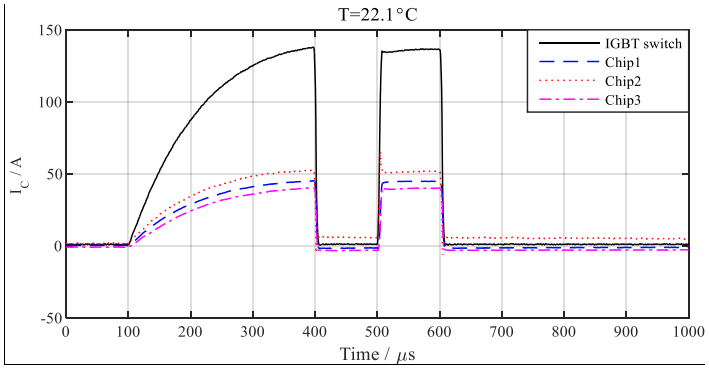
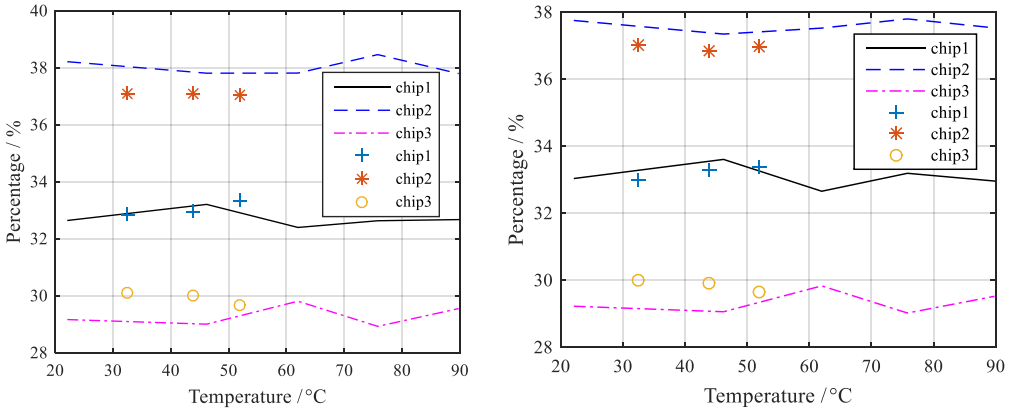


Figure 3.18 Example of collector current distribution. HTD test with T_{vj} = 22.1 °C.

The shares of the current at different temperature conditions are displayed in Figure 3.19. The percentage of each chip is derived with (3.9). The use of the percentage eliminates the influence

of the current fluctuation, which is a common phenomenon between the turn-off transient t_2 of the first pulse and the turn-on transient t_3 of the second pulse in Figure 3.8.

$$Percentage = \frac{I_{C(Chip)}}{I_C} \times 100\% \tag{3.9}$$



(a) (b)

Figure 3.19 Collector current distribution: (a) Collector current just before t_2 in Figure 3.8b, (b) Collector current right after t_3 in Figure 3.8b. Line plot: HTD test. Scatter plot: ITD test.

Figure 3.19a and Figure 3.19b depict the current distribution in the IGBT switch just before the turn-off transient t_2 of the first pulse and the current distribution right after the turn-on transient t_3 of the second pulse. In both figures, as long as the temperature distribution is uniform, the current distribution is constant and will not be severely influenced by the temperature level. However, at ITD condition, the current distribution will change. Even though the average temperature of the IGBT switch is still the same, the current share of the coldest chip, Chip3, increases. The current share of Chip2 decreases. The IGBT chip in this module is with trench gate field stop structure. Since field stop IGBT does not use lifetime control and the mobility declines with temperature, the on-state voltage increases drastically which results in a lower inflexion point [64], the IGBT switch works in the positive temperature coefficient region in its forward characteristics. Therefore, the coldest chip tends to share more current to reduce the thermal stress of the hotter chip. This is the self-balancing principle of the IGBT switch which makes it can work reliably with several chips in parallel.

3.5.3. Consistent shifts caused by ITD

The antecedents of the prediction drift are analyzed in this section. ITD between IGBT chips not only causes current redistribution but also leads to consistent shifts in the turn-on and turn-off characteristics of the IGBT switch. This scenario is captured in V_{CE} and I_C.

Figure 3.20 and Figure 3.21 describe the shift in V_{CE} during the off state in the two pulses. The forward blocking voltage V_{CE} increases at ITD conditions compared to HTD conditions. This means the voltage stress on the device is rising. A larger forward blocking peak voltage and steeper rise of V_{CE} during the turn-off transient is also shown at ITD compared to HTD at higher temperatures. Hence, dV_{CE}/dt and $V_{CE(peak)}$ are higher than those observed at HTD condition. Consequently, the temperature estimations for dV_{CE}/dt and $V_{CE(peak)}$ are lower than T_{vj}.

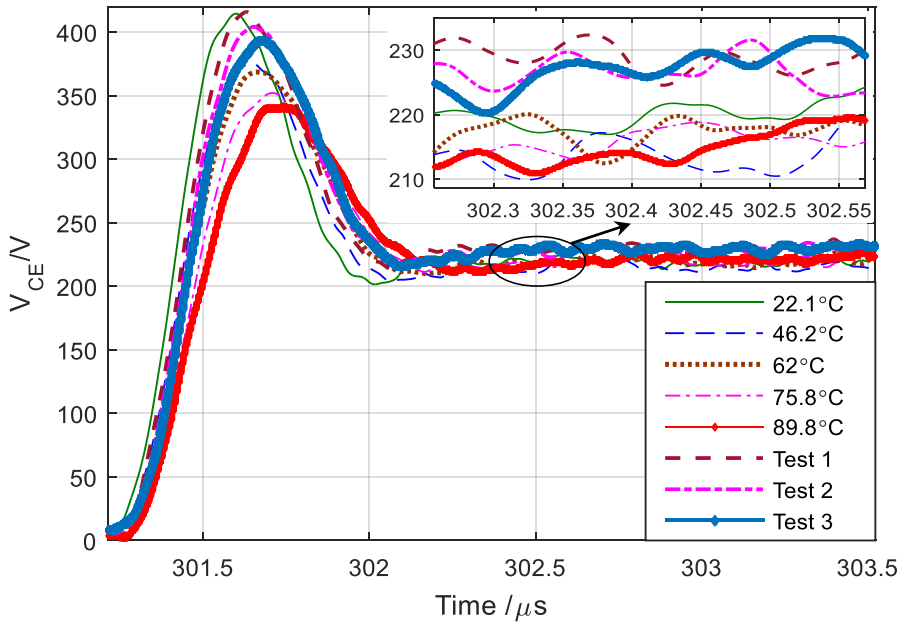


Figure 3.20 Shifts in V_{CE} at off-state captured during the first pulse.

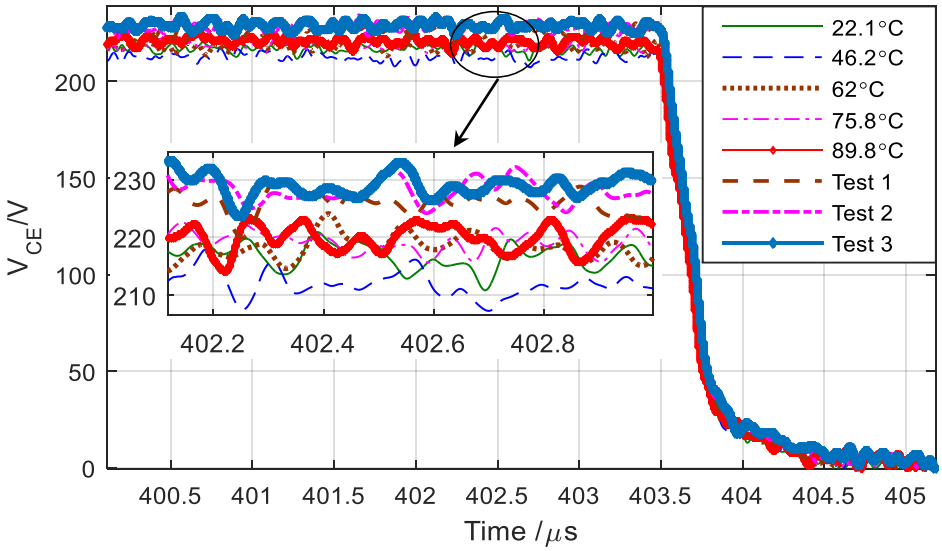


Figure 3.21 Shifts in V_{CE} at the off-state captured during the second pulse.

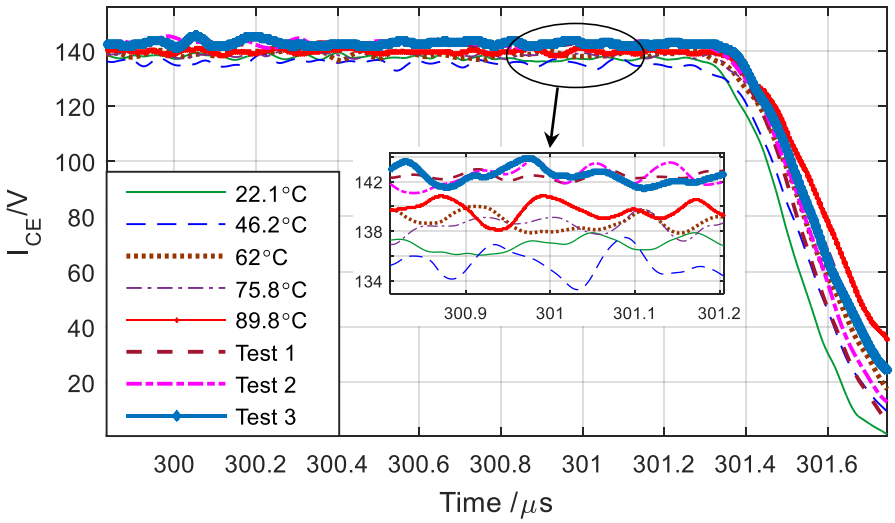


Figure 3.22 Shifts in I_C during the first pulse.

Figure 3.22 illustrates the shifts in I_C during the first pulse. The on-state current I_C goes up from Test 1 to Test 3. This means a higher tail current appears during the turn-off transient. Because of the positive temperature coefficient of $I_{C(tail)}$, the estimation from $I_{C(tail)}$ is higher than T_{vj}. The current rise can be caused by the reduction of the 'on-state' resistance of the IGBT switch. Because the IGBT switch is at ITD condition, the parallel of the 'on-state' resistance of each IGBT chip is smaller than the 'on-state' resistance of the IGBT switch in the HTD test. The estimation from $I_{C(tail)}$ is close to the highest temperature but not be able to predict the worst condition.

3.6. **Summary**

This chapter investigats the T_{vj} estimation in the mIGBT module that considers the influence of SDoT. A research gap was identified in the field of SDoT after a review of existing research, and a test rig was constructed to conduct SDoT to address the research gap. The temperature dissimilarity within each IGBT chip is considerable – about 8 °C to 60 °C – depending on the current level and pulse width. The difference between IGBT chips is about 10 °C. This temperature distribution is significant and should not be neglected.

SDoT causes consistent shift in switching characteristics. Consequently, TSEPs such as dV_{CE}/dt, $V_{CE(peak)}$ and $I_{C(tail)}$ are not feasible for T_{vj} estimation. dV_{CE}/dt and $V_{CE(peak)}$ predict higher than T_{vj}, whereas $I_{C(tail)}$ predicts lower than T_{vj}.

Additionally, SDoT causes C-E current redistribution among the IGBT chips. Despite the current imbalance caused by the intrinsic package difference, the SDoT causes more current to flow through the colder chip and less current to flow through the hotter chip.

In conclusion, there is severe SDoT within the mIGBT module during normal operation and the impact of SDoT must be considered when employing a TSEP for T_{vj} estimation in an mIGBT module. According to the test conducted in this chapter, $V_{CE(on\text{-}sense)}$ is the best for T_{vj} estimation in an mIGBT.

Chapter 4. Offline bond wire fault detection

In power applications, it is common to have regular maintenance intervals on the power converter. In this situation, the power converter is switched off so no power is generated. During maintenance various tests are conducted on the inverter. Health status test of the IGBTs have so far not been included in these tests. This chapter proposes a condition monitoring technique that is able to detect bond-wire lift off during maintenance activities. The main novelty of the proposed technique is that the proposed method is able to locate the lifted bond wires. To the author's knowledge, localizing lifted bond wires in closed power modules have so far not been reported. In addition, compared with techniques listed in Chapter 2, the proposed method is able to identify early bond wire lift-off. In some power applications such as offshore wind power farm, it is imperative to recognise the failures well in advance which provides enough time to schedule the further maintenance.

As discussed in Chapter 2, the on-state voltage measurement is the most promising technique in terms of accuracy. Thus, in this chapter, a condition monitoring technique is proposed based on the on-state voltage. Of all the different on-state voltage measurements, this work makes use of $V_{\mathrm{CK(on)}}$ and $V_{\mathrm{CE(on)}}$.

4.1. Proposed diagnostic approach based on $V_{\mathrm{CK(on)}}$ and $V_{\mathrm{CE(on)}}$

The general structure of the IGBT chip and its equivalent circuit is described in Figure 2.8a. The on-state voltage across collector and Kelvin emitter $V_{\mathrm{CK(on)}}$ is the on-state voltage of the IGBT chip. At constant load condition and operation condition, $V_{\mathrm{CK(on)}}$ is a function of chip temperature T_{vj} and the current I_{Chip} as depicted in (4.1).

$$V_{CK(on)} = f(I_{Chip}, T_{vj}) \tag{4.1}$$

Whereas, the on-state voltage of the module $V_{\mathrm{CE(on)}}$ includes $V_{\mathrm{CK(on)}}$ as well as the voltage of bond wires V_{Wire} as expressed in (4.2). V_{Wire} is influenced by T_{vj}, I_{C} and the state of the bond wires.

$$V_{CE(on)} = f(I_C, T_{vj}, V_{wire}) \tag{4.2}$$

Assuming that the equivalent resistance of the bond wires is R_0 at T_0. The temperature coefficient of the bond wire is β. The voltage across the bond wire is described as (4.3).

$$V_{BondWire} = \left[R_0 + \beta(T_{vj} - T_0) \right] \times I_{Chip} \tag{4.3}$$

The setup for on-state voltage measurement is shown in Figure 4.1. The IGBT module under test is the Infineon module FF600R17ME4, which is rated at 1.7 kV and 600 A and has 11 bond wires connecting Chip1, 13 bond wires connecting Chip2 and 13 bond wires connecting Chip3.

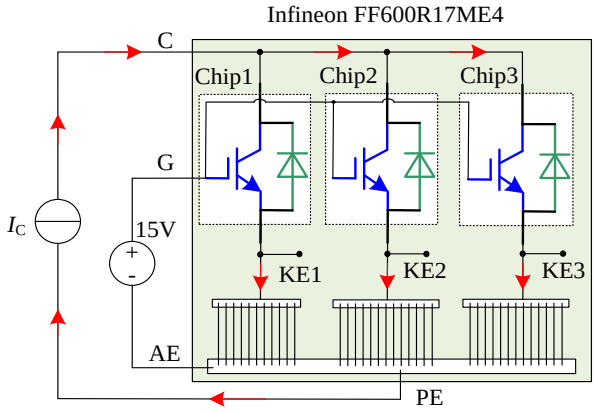


Figure 4.1 On-state voltage measurement for the IGBT PM under test.

Assuming that there is bond wire lift-off in Chip1, the equivalent resistance of the remaining bond wire will increase. Thus the equivalent resistance of Chip1 branch will rise. This will lead to the current redistribution amongst the three IGBT chips. The collector current flowing through Chip1 will decline. However, the current of the other two chips will climb. The current imbalance will lead to the variation of chip on-state voltage as expressed in (4.4).

$$V_{CK1(on)} \downarrow, \quad V_{CK2(on)} \uparrow, \quad V_{CK3(on)} \uparrow \tag{4.4}$$

In the case of bond wires, the voltage variation is the product of the resistance change and the current share as derived in (4.5). (4.5) assumes an equal current share among Chip2 and Chip3. The resistance change of bond wires connecting Chip1 $\Delta V_{\text{BondWire\_Chip1}}$ is amplified by the collector current. Thus, $\Delta V_{\text{BondWire\_Chip1}}$ will be higher than $\Delta V_{\text{BondWire\_Chip2}}$ and $\Delta V_{\text{BondWire\_Chip3}}$ which are the voltage variation of bond wires connecting Chip2 and Chip3 respectively.

$$\Delta V_{BondWire\_Chip1} \approx \Delta R_{BondWire} \times (I_{Chip} - \Delta I_{Chip})$$
$$\Delta V_{BondWire\_Chip2} = \frac{1}{2}\left[R_0 + \beta(T_j - T_0)\right] \times \Delta I_{Chip} \quad (4.5)$$
$$\Delta V_{BondWire\_Chip3} = \frac{1}{2}\left[R_0 + \beta(T_j - T_0)\right] \times \Delta I_{Chip}$$

Where $\Delta R_{\mathrm{BondWire}}$ is the equivalent resistance increment of bond wires in Chip1 caused by the lift-off. ΔI_{Chip} is the current decrement in Chip1 caused by the lift-off.

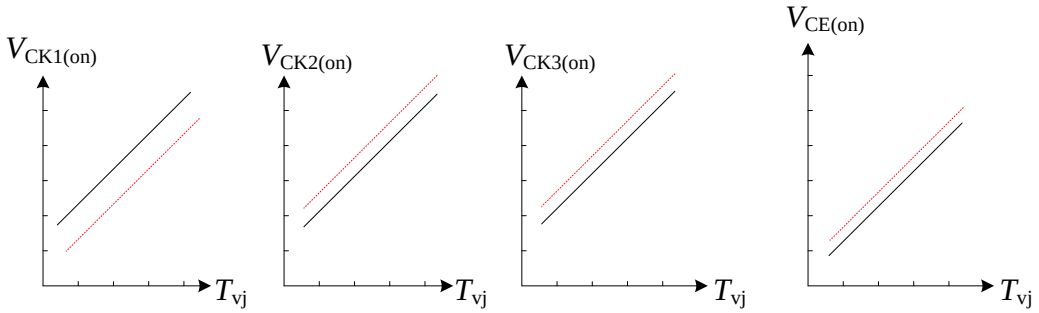


Figure 4.2 On-state voltage variation in the case of bond wire lift-off. Solid line: Healthy. Dotted line: Lift-off in Chip1.

The on-state voltage variation in the case of bond wire lift-off is illustrated in Figure 4.2. In the case of bond wire lift-off, the on-state voltage of the corresponding chip will decrease. However, on-state voltage of other chips will increase as well as the on-state voltage of the IGBT switch. This information can be employed to monitor the health condition of mIGBT modules and locate the bond wire failure. In addition, compared with the conventional on-state voltage approach, the proposed technique can detect early stage failure in a mIGBT.

4.2. **Experimental test**

4.2.1. Test setup

A test rig was developed to verify the theory. The test rig is shown in Figure 4.3. It is set up according to Figure 4.1. The IGBT under test is mounted on a heat plate. T_{vj} is varied through the electric heater.

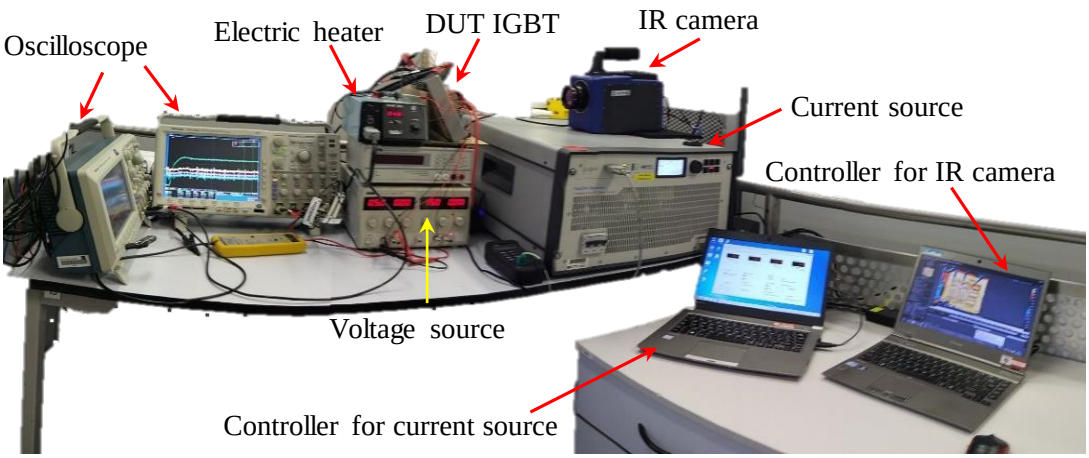


Figure 4.3 Test rig set up.

Firstly, the IGBT is switched on by the voltage source. Then, a current pulse is injected into the IGBT by the TopCon power source, which is controlled by the computer on the left side. The thermal characteristics of the devices are also recorded by the IR camera, which is controlled by the computer on the right side. The two oscilloscopes capture electrical parameters.

4.2.2. The output characteristic of the IGBT

The proposed $V_{CE(on)}$ and $V_{CK(on)}$ approach is tested on the FF600R17ME4 module. The output characteristic I_C - $V_{CE(on)}$ illustrates the temperature dependency of the on-state characteristic of the IGBT module. It is an essential part of the fundamental research.

Figure 4.4 depicts the output characteristic for Chip1, Chip2, Chip3 and the IGBT switch. The on-state voltage declines with temperature rise above the inflexion point and vice versa below the inflexion point. The inflexion point of the IGBT switch is at I_C = 100 A as shown in the zoomed figure of $V_{CE(on)}$. It should be pointed out that the curves for I_C - $V_{CE(on)}$ at different temperature do not cross over each other at the same point. It is a region which means the temperature dependency of the on-state voltage is not strictly zero. This will reduce the sensitivity of the fault detection approaches based on the inflexion point, such as the technique in [70].

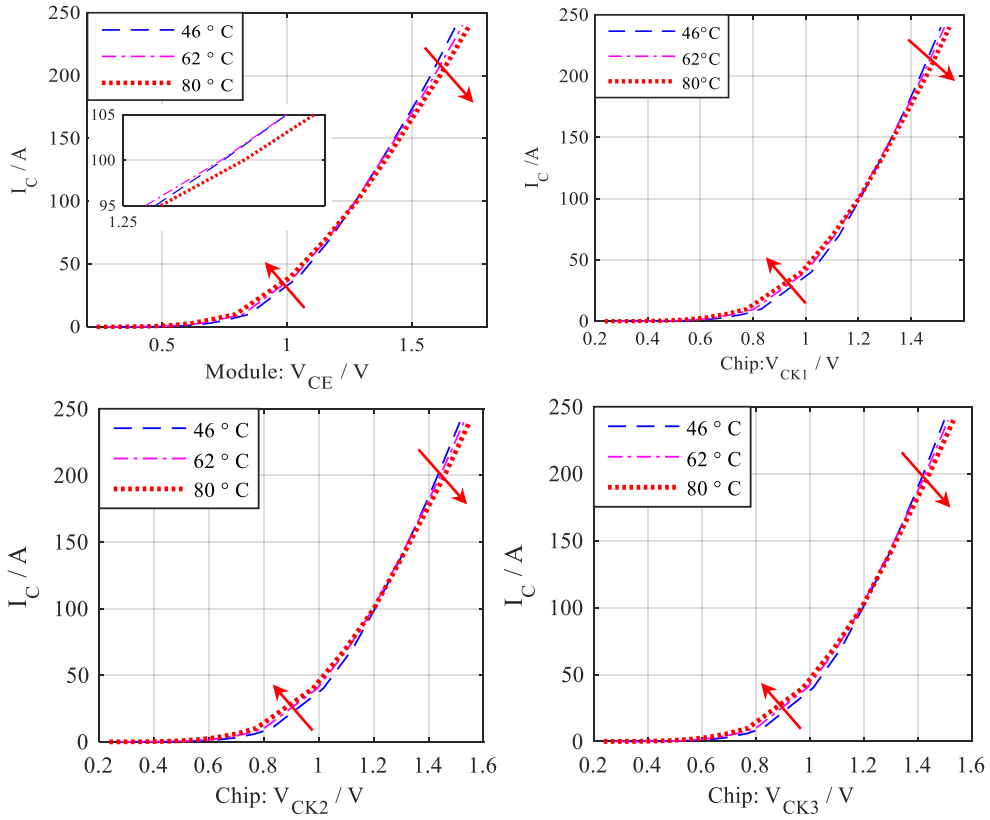


Figure 4.4 Output characteristic of the IGBT module and the IGBT chips. V_{GE} = 15V.

4.2.3. Test conditions

Bond wires were cut to imitate the lift-off failure. A defined sequence in bond wire cutting have been applied in order to measure $V_{CE(on)}$ and $V_{CK(on)}$ at different bond wire lift-offs. Table 4.1 shows that various failure conditions have been created for each chip.

Table 4.1 List of test conditions

Health condition	Healthy	Fault in Chip1				Fault in Chip1 and Chip2		Fault in Chip1, Chip2 and Chip3		
Chip1	0	1	2	3	4	4	4	4	4	4
Chip2	0	0	0	0	0	2	4	4	4	5
Chip3	0	0	0	0	0	0	0	2	4	6

4.2.4. Results for bond wire lift-offs

The on-state voltage of the IGBT switch as well as the IGBT chips within the switch is measured with the test rig shown in Figure 4.3. $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ denote the on-state voltage of Chip1, Chip2 and Chip3 respectively. $V_{CE(on)}$ denotes the on-state voltage of the IGBT switch under test. On-state voltages at 40A, 100A and 240A are investigated to represent the forward characteristics of the region below, at and above the inflexion point respectively.

Figure 4.5 depicts the on-state voltage variation upon the bond wire lift-off in Chip1. When there is bond wire lift-off in Chip1, $V_{CK1(on)}$ decreases. Whilst the voltage of the healthy chips $V_{CK2(on)}$ and $V_{CK3(on)}$ rise. The voltage variation grows with an increasing number of bond wire cuts. Also the higher the current level, the more significant the variation in voltages upon first bond wire lift-off. At I_C = 40 A, it is difficult to predict the first bond wire lift-off, but there is about 7 mV decline in $V_{CK1(on)}$ at the second bond wire lift-off. At 100 A, the first bond wire cut produces already a detectable voltage of 4 mV. When I_C = 240 A, $V_{CK1(on)}$ decreases about 7 mV upon the first bond wire lift-off. However, $V_{CK2(on)}$, $V_{CK3(on)}$ and $V_{CE(on)}$ only increases slightly as shown in the figure. Therefore, if $V_{CE(on)}$ of the IGBT switch alone is used, the deviation of the first bond wire lift-off would be too small to be detected.

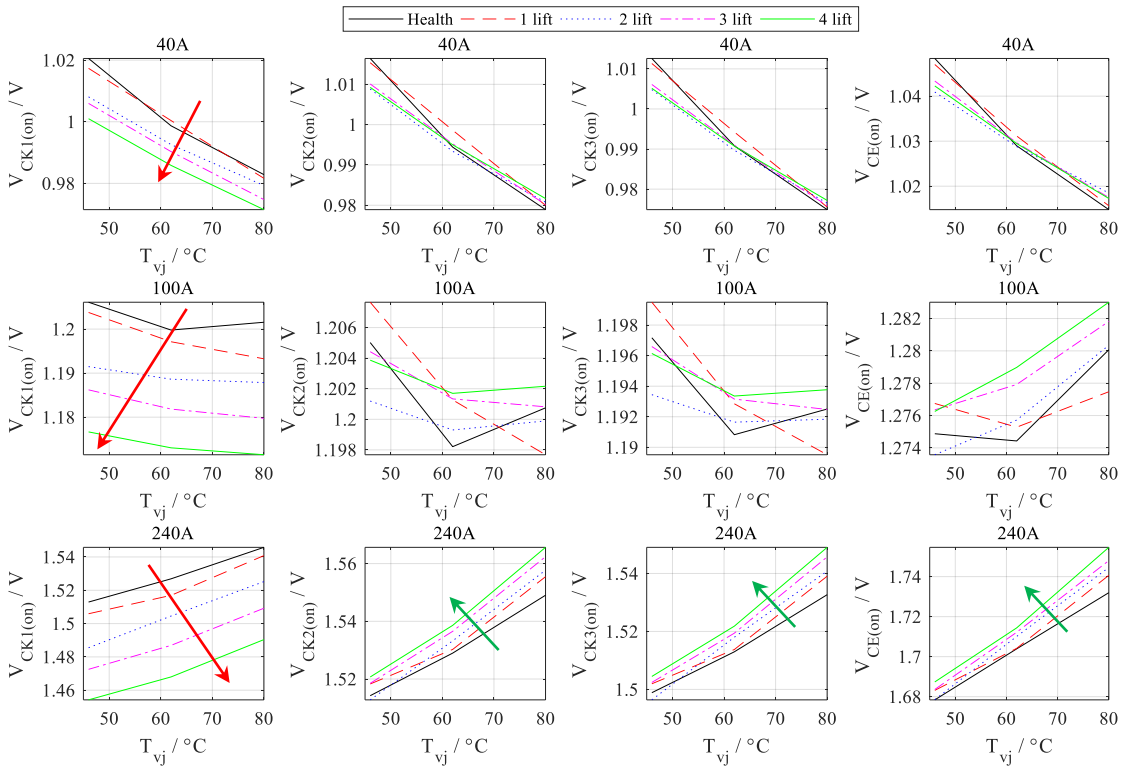


Figure 4.5 $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and $V_{CE(on)}$ at various T_{vj} and bond wire cuts in Chip1.

Figure 4.5 shows results only for cutting bond wires on Chip1. Bond wires were also cut for Chip2 and Chip3 as detailed in Table 4.1. Figure 4.6 and Figure 4.7 present results for these scenarios. Compared to the results where four bond wires were cut in Chip1, $V_{CK2(on)}$ starts to decrease when cutting bond wires in Chip2 and $V_{CE(on)}$, $V_{CK1(on)}$ and $V_{CK3(on)}$ rise slightly. The trend of results shown in Figure 4.7 resembles that in Figure 4.6. When there is bond wire failure in Chip3, $V_{CK3(on)}$ goes down, however, $V_{CE(on)}$, $V_{CK1(on)}$ and $V_{CK2(on)}$ goes up. The variation rises with the current increment.

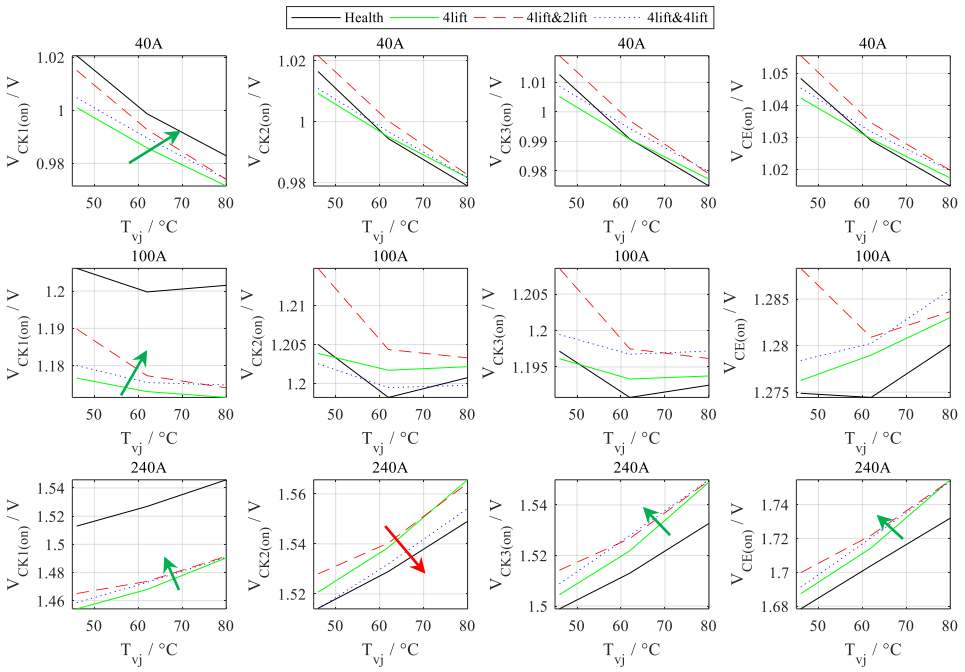


Figure 4.6 $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and $V_{CE(on)}$ at various T_{vj} and bond wire cuts in Chip1 and Chip2. (4lift: four lift-offs in Chip 1 only; 4lift&2lift: four lift-offs in Chip1 and two lift-offs in Chip2; 4lift&4lift: four lift-offs in both Chip1 and Chip2.)

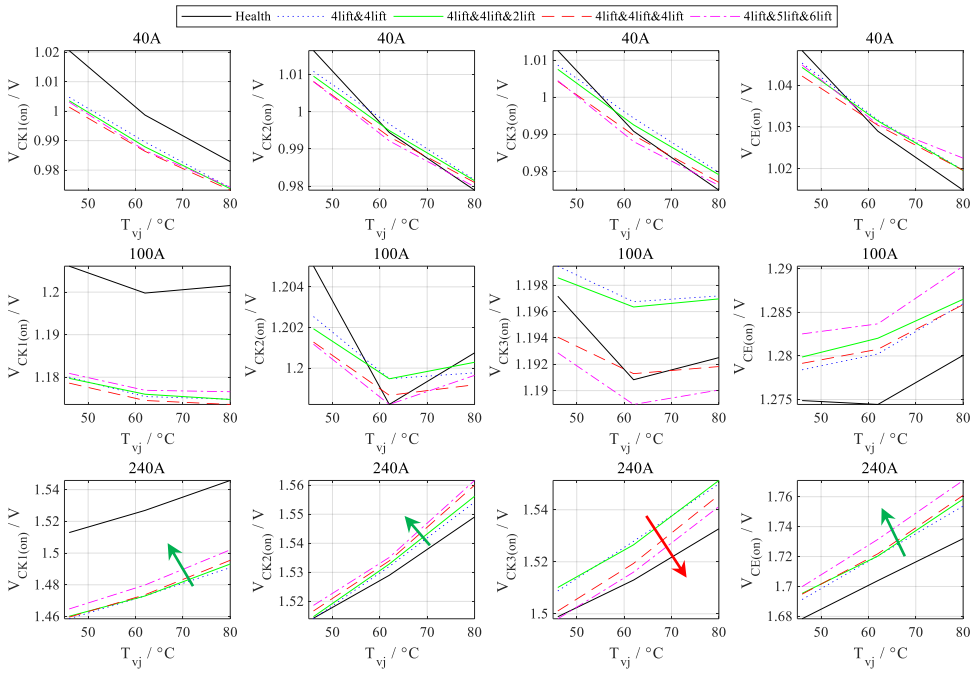


Figure 4.7 $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and $V_{CE(on)}$ at various T_{vj} and bond wire cuts in Chip1, Chip2 and Chip 3. (4lift&4lift&2lift: four lift-offs in both Chip1 and Chip2 and two lift-offs in Chip3; 4lift&4lift&4lift stand for four lift-offs in Chip1, Chip2 and Chip3; 4lift&5lift&6lift: four lift-offs in Chip1, five lift-offs in Chip2 and six lift-offs in Chip3.)

In conclusion, test results have confirmed the theory in section 4.1. $V_{CE(on)}$ and $V_{CK(on)}$ change with bond wire cuts. $V_{CK(on)}$ always declines at the chip where a bond wire is cut and the voltage across the other chips increases. Voltage variations rise with the collector current level. Further

analysis is carried out in the following sections to illustrate how to detect the bond wire flift-off and locate the failure.

4.3. **Bond wire lift-off detection and location**

4.3.1. Procedure for fault diagnosis

This section describes the bond wire fault diagnosis in detail. The procedure is illustrated in Figure 4.8. At first, baselines for $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ are established by characterising the mIGBT PM at different temperatures which act as the reference for a healthy module. At the second stage, the measurements for $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ are carried out during maintenance work. Finally, the measurements are analysed with the reference table in the first stage to determine the bond wire state and locate the faulty chip when there is lift-off. Below is an illustration about the procedure.

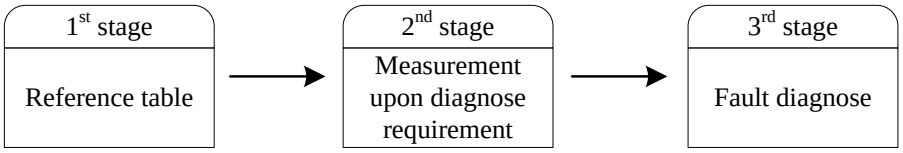


Figure 4.8 Diagnose procedure.

a) 1st Stage

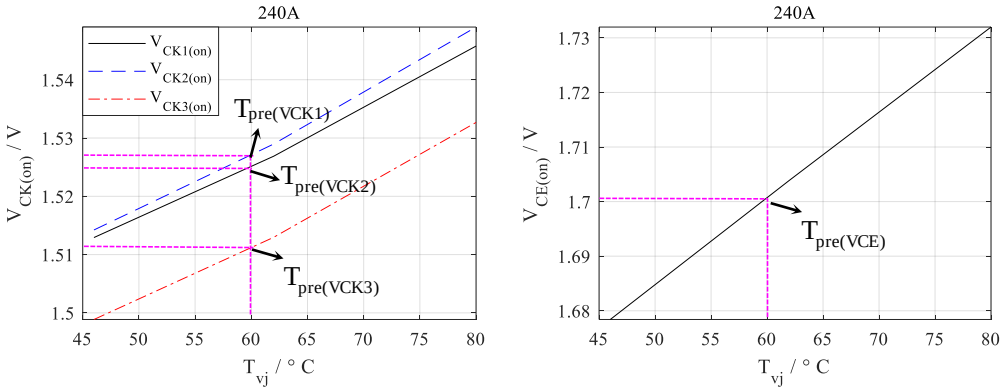


Figure 4.9 Reference table for bond wire lift-off estimation at I_C = 240 A.

The on-state voltage of the IGBT module is characterised at different temperatures with a constant current flowing through C-E. In this case, I_C is 240 A. The baselines are shown in Figure 4.9. Data from Figure 4.9 have been stored in a reference table which is used for temperature estimation in the third stage.

b) 2nd Stage

$V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ are captured again during maintenance at the same current level to estimate the ageing state of the IGBT switch. In this example, the measurements are the results presented in Figure 4.5, Figure 4.6 and Figure 4.7 with lift-offs.

c) 3rd Stage

At this stage, results from 2nd stage are compared with the reference to determine bond wire degradation. It should be pointed out that T_{vj} is not known. As the power converter is switched off during maintenance, the assumption can be made that the temperature distribution is uniform in the IGBT module.

i. The IGBT module under test is healthy

T_{vj} predicted by $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ will be the same as described in Figure 4.9 with the dotted line. It can be written as (4.6).

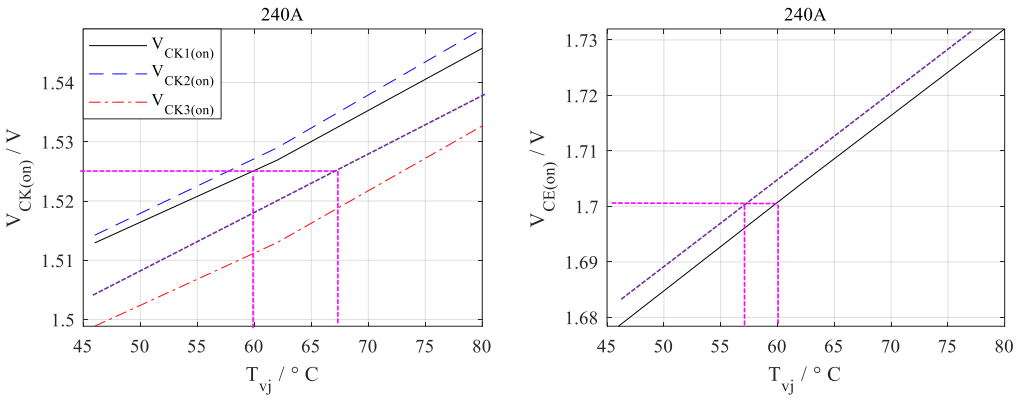
$$T_{pre(V_{CK1})} = T_{pre(V_{CK2})} = T_{pre(V_{CK3})} = T_{pre(V_{CE})} \tag{4.6}$$

Where $T_{pre(V_{CK1})}$, $T_{pre(V_{CK2})}$, $T_{pre(V_{CK3})}$ and $T_{pre(V_{CE})}$ are the temperature predicted by $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and $V_{CE(on)}$ respectively.

ii. Example: Bond wire lift-off at Chip1

In this case, $V_{CK1(on)}$ will decline as illustrated with the dotted line in Figure 4.10a. However, since the solid line in Figure 4.10a is still utilised as a reference for T_{vj} estimation, the estimated temperature $T_{pre(V_{CK1})}$ is lower than T_{vj} as illustrated in (4.7).

$$T_{pre(V_{CK1})} < T_{vj} \tag{4.7}$$



(a) (b)

Figure 4.10 Estimation change in the case of bond wire lift-off at I_C = 240 A.

However, $V_{CE(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ rise because of the lift-off in Chip1. The rise in $V_{CE(on)}$ is shown in Figure 4.10b with the dotted line. Since the solid line in Figure 4.10b is used for temperature estimation, $T_{pre(V_{CE})}$ is then higher than T_{vj}. Estimation from $V_{CK2(on)}$ and $V_{CK3(on)}$ resemble the tendency of $V_{CE(on)}$. Their relationship is expressed in (4.8).

$$\begin{aligned} T_{pre(V_{CK2})} &> T_{vj} \\ T_{pre(V_{CK3})} &> T_{vj} \\ T_{pre(V_{CE})} &> T_{vj} \end{aligned} \tag{4.8}$$

iii. Fault diagnosis (detection and location)

The temperature estimation gap between $T_{pre(V_{CK1})}$, $T_{pre(V_{CK2})}$, $T_{pre(V_{CK3})}$ and $T_{pre(V_{CE})}$ is represented by ΔT_{pre1}, ΔT_{pre2} and ΔT_{pre3}. They are obtained according to (4.9).

$$\begin{aligned} \Delta T_{pre1} &= T_{pre(V_{CK1})} - T_{pre(V_{CE})} \\ \Delta T_{pre2} &= T_{pre(V_{CK2})} - T_{pre(V_{CE})} \\ \Delta T_{pre3} &= T_{pre(V_{CK3})} - T_{pre(V_{CE})} \end{aligned} \tag{4.9}$$

The estimation gap is used to estimate the bond wire state and locate the fault. Figure 4.11 describes the temperature estimation gap for different bond wire lift-off conditions at I_C = 240 A.

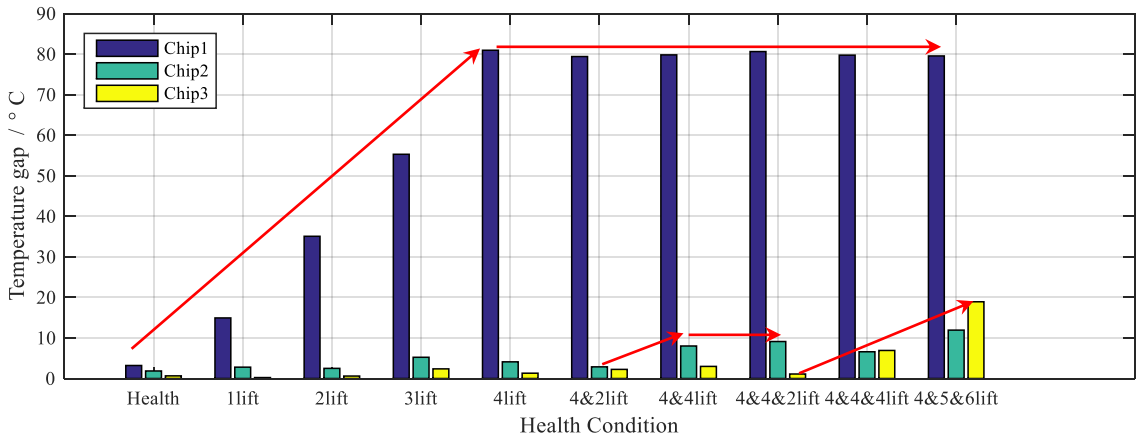


Figure 4.11 Predicted temperature gap for different bond wire lift-off conditions.

The arrows in Figure 4.11 denote the tendency of ΔT_{pre} for each IGBT chip. On the condition of lift-off in Chip1, ΔT_{pre1} shoots up with the rise of bond wire failure and maintains almost the same when there is lift-off in the other two chips. ΔT_{pre2} and ΔT_{pre3} are almost zero mainly due to the small rise of the on-state voltage. In the case of lift-off in Chip1 and Chip2, ΔT_{pre2} goes up. When there is bond wire lift-off in Chip3, ΔT_{pre3} starts to rise. All the temperature estimation gap is collected to predict the number of bond wire lift-off as well as identify the location of the lift-off. This supports to obtain more information about the health condition of the IGBT module.

4.3.2. Fault influence on the current distribution

The propose method aid to assess the collector current redistribution among three IGBT chips. The current sharing process upon bond wire failure is presented in Figure 4.12. Currents are presented as percentages for simplicity. The percentages are the ratio of the chip currents I_{C1}, I_{C2} and I_{C3} to I_C. Each figure in Figure 4.12 includes three sets of plots indicated with open braces and each set indicates one chip. The top set shows the percentage of current sharing for Chip2, the second for Chip1 and the last for Chip3. At healthy state, the current share for Chip1, Chip2 and Chip3 are 32.5 %, 38 % and 29.5 % respectively. When there is bond wire lift-off in Chip1, the current share of Chip1 declines. On the contrary, the current share of Chip2 and Chip3 goes up. Figure 4.13 also shows that the variation of the percentages increases with the increment of the lifted bond wires. The trends shown in Figure 4.12 is the same for all tests at I_C = 40 A, I_C = 100 A and I_C = 240 A. However, the deviation of the current share upon the first lift-off varies with the current level. For instance, the deviation upon the first lift-off at 40 A is 0.170 %. This increases to 0.507 % at 240 A. This indicates that the current redistribution becomes severe when the injected current is high.

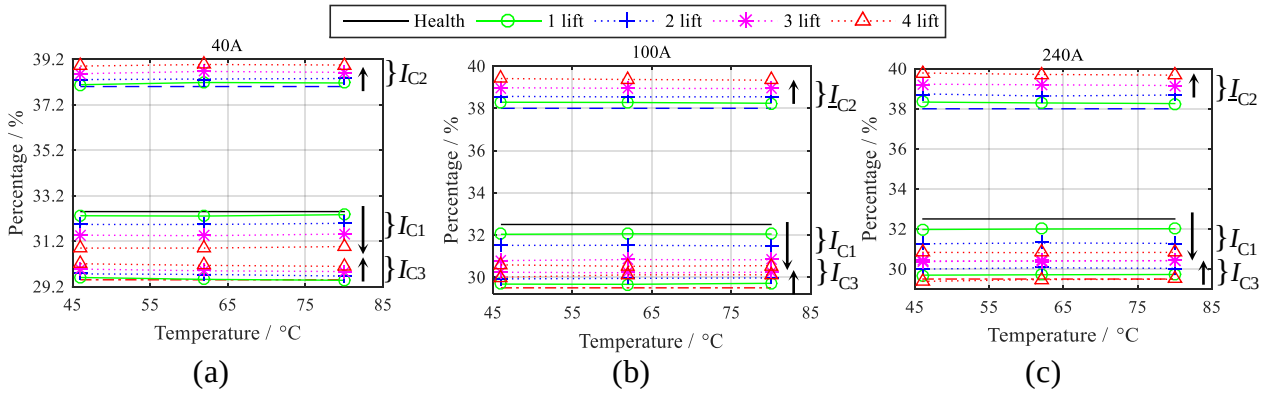


Figure 4.12 Current share upon bond wire lift-off in Chip1: (a) I_C = 40 A, (b) I_C = 100 A, (c) I_C = 240 A.

Figure 4.13 describes the current share of each chip at I_C = 240 A. It can be noted that the current share fluctuates with the temperature. However, it does not express any dependency on temperature. Further analysis of other failure conditions is included in Appendix.

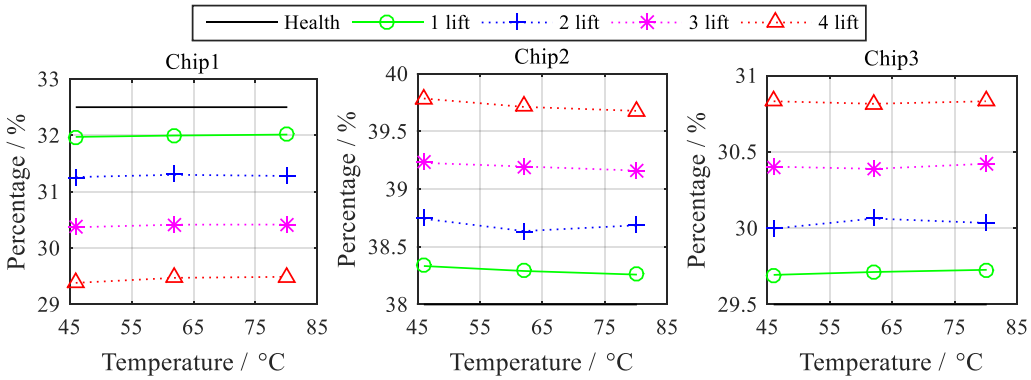


Figure 4.13 Current distribution upon bond wire lift-off in Chip1 at I_C = 240 A.

4.3.3. Fault influence on temperature variation

The proposed method is not influenced by self-heating. It is well known that when there is current flowing through the IGBT, the power dissipation will heat the device. This is the self-heating effect (SHE). In this section, SHE is evaluated to identify its influence on the fault diagnosis. The sequence of the current pulse and the heating up process are described in Figure 4.14a. The injected current gradually increase to the expected value and then holds for certain time. In this test, 20 ms is used. T_{vj} starts to increase when there is current flowing and reaches the peak at t = 20 ms. T_{vj} decreases right after the current is switched off and goes back to the initial value in about 2 s.

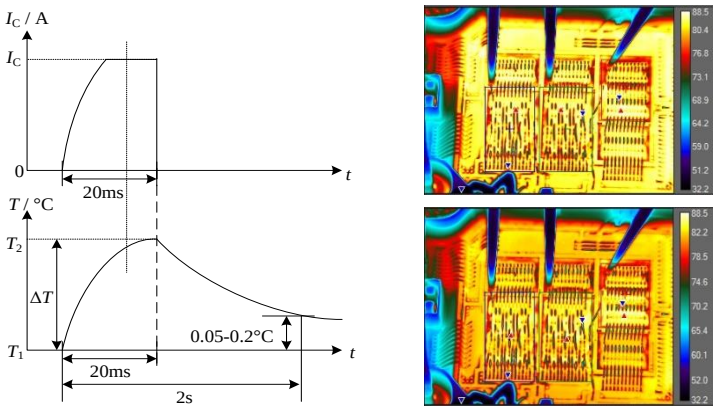


Figure 4.14 Self-heating effect: (a) The current pulse and the corresponding temperature variation, (b) The thermal profile of the IGBT switch at 85 °C: before and after current injection.

The self-heating can be identified through the IR image of the PM in Figure 4.14b. As can be seen from the image, when there is current flowing through the PM, the temperature of the IGBT rises. It can be noted that the temperature of the bond wire is much lower than the temperature of the IGBT chip. When current flows through, the temperature of the IGBT chip is higher than the other area. The deviation ΔT between T1 and T2 in Figure 4.14 is utilised to quantify SHE. Since there are average temperature and maximum temperature for each IGBT chip, the deviation is divided into maximum temperature deviation $\Delta T_{(max)}$ and average temperature deviation $\Delta T_{(avg)}$ accordingly.

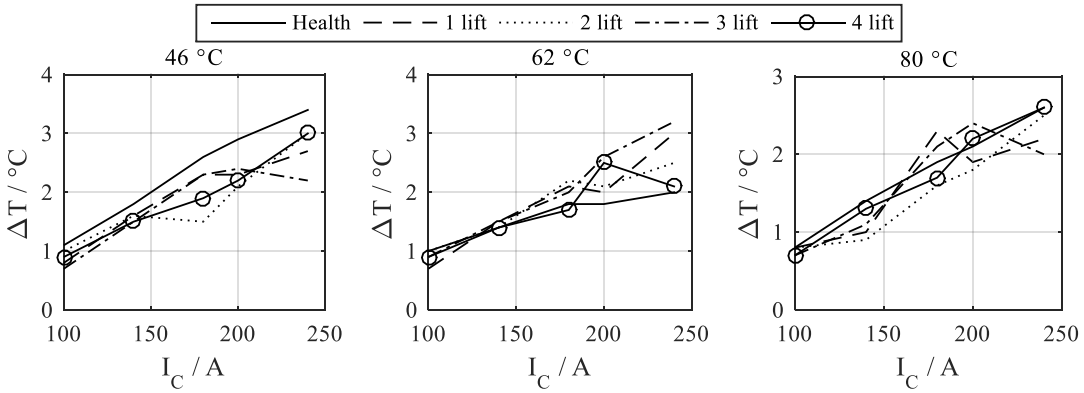


Figure 4.15 Maximum temperature deviation $\Delta T_{(max)}$ of Chip3 upon bond wire lift-off.

Figure 4.15 and Figure 4.16 depict SHE in Chip1. Both $\Delta T_{(max)}$ and $\Delta T_{(avg)}$ climb with current increment and $\Delta T_{(max)}$ is higher than $\Delta T_{(avg)}$. At I_C = 240 A, $\Delta T_{(max)}$ is about 3 °C, 2 °C higher than $\Delta T_{(avg)}$. The deviations under different bond wire lift-off conditions are also covered in Figure 4.15 and Figure 4.16. The deviation goes up with the current level, but it does not show dependency on the bond wire lift-offs. In conclusion, the temperature variation caused by self-heating is minimal and does not influence bond wire fault diagnosis.

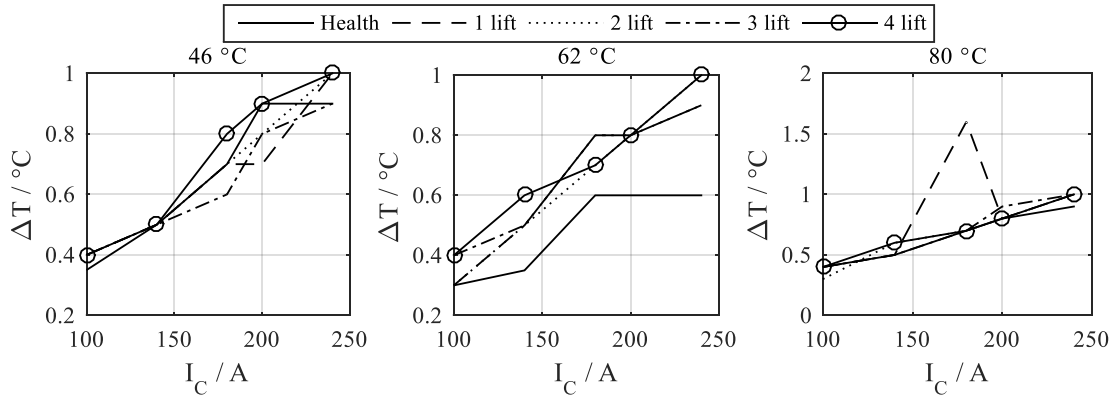


Figure 4.16 Average temperature deviation $\Delta T_{(avg)}$ of Chip3 upon bond wire lift-off.

4.4. **Repeat test on Dynex module**

A repeat test is carried out on the Dynex DIM400NSM33-F000 IGBT module. This is to investigate the influence of the package on the proposed method.

4.4.1. Fundamentals of the Dynex module

The layout of the Dynex DIM400NSM33-F000 IGBT module is illustrated in Figure 4.17. There are four DBC tiles in the single switch IGBT module as shown in Figure 4.17a. Each DBC tile has two IGBT chips and one diode chip. They are depicted in Figure 4.17b.

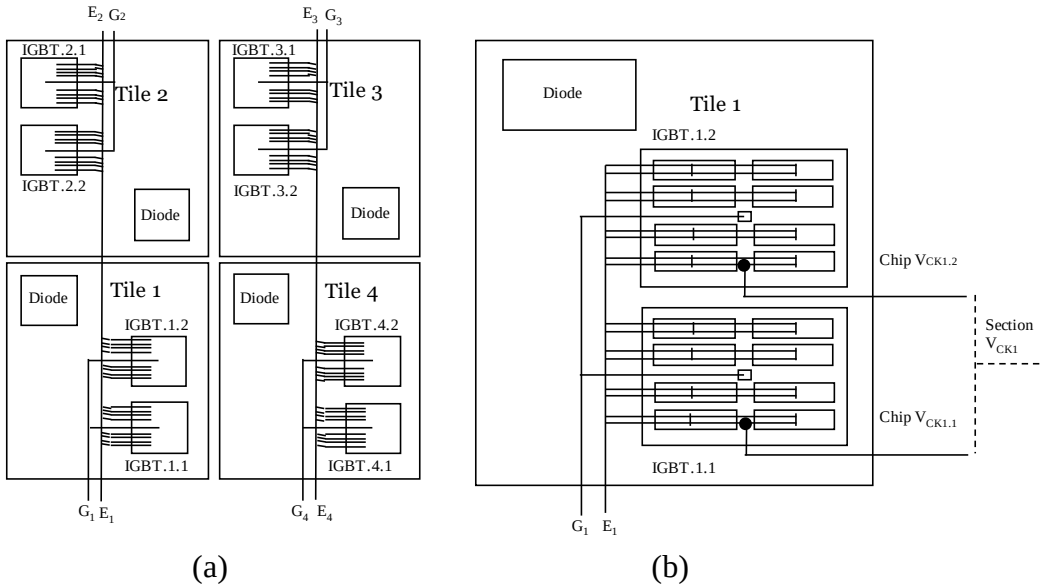


Figure 4.17 Layout of the Dynex DIM400NSM33-F000 IGBT module: (a) The IGBT module, (b) Section 1 in the IGBT module.

DIM400NSM33-F000 is 400 A 3.3 kV module with 8 IGBT chips and 64 bond wires. The numbering of each IGBT chip and DBC sections are shown in Figure 4.17a. When the power

rate increases, the number of chips in the module will increase. This means that the number of the measurement points in the proposed method will rise which increases the measurement complexity in large PMs. Thus, another approach which combines the on-state voltage of each DBC tile $V_{CK(on\text{-}tile)}$ with $V_{CE(on)}$ is proposed. This approach helps to reduce measurement points for bond wire state estimation in large IGBT PMs. The on-state voltage of each section is measured between collector and the common point of two IGBT chips as shown in Figure 4.17b.

The output characteristic of the IGBT module is shown in Figure 4.18. The inflexion point of this IGBT module is at $I_C \approx 12.5$ A. During the test, the IGBT module is tested at 320 A which is near the rated current.

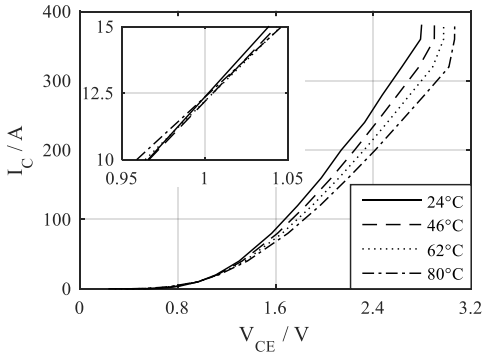


Figure 4.18 The output characteristic of the DIM400NSM33-F000 IGBT module.

4.4.2. Test conditions

The proposed $V_{CE(on)}$ and $V_{CK(on)}$ approach is tested on the DIM400NSM33-F000. There are eight IGBT chips in the module. Different lift-off conditions are created on each section as listed in Table 4.2.

Table 4.2 Bond wire lift-off conditions

Lifted bond wire	Healthy	Fault in Section 1			Fault in Section 2			Fault in Section 3			Fault in Section 4		
Chip 1.1	0	3	5	7	7	7	7	7	7	7	7	7	7
Chip 2.1	0	0	0	0	3	5	7	7	7	7	7	7	7
Chip 3.1	0	0	0	0	0	0	0	3	5	7	7	7	7
Chip 4.1	0	0	0	0	0	0	0	0	0	0	3	5	7
Chip 1.2	0	0	0	0	0	0	0	0	0	0	0	0	0
Chip 2.2	0	0	0	0	0	0	0	0	0	0	0	0	0
Chip 3.2	0	0	0	0	0	0	0	0	0	0	0	0	0
Chip 4.2	0	0	0	0	0	0	0	0	0	0	0	0	0

During the test, the on-state voltage of each IGBT chip, each DBC tile and the IGBT switch are recorded. Due to the introduction of $V_{CK(on\text{-}tile)}$, the proposed $V_{CE(on)}$ and $V_{CK(on)}$ technique is divided into the $V_{CK(on\text{-}chip)}$ & $V_{CE(on)}$ technique and the $V_{CK(on\text{-}tile)}$ & $V_{CE(on)}$ technique. Both techniques are investigated in this research.

4.4.3. Experimental tests

Test rig for DIM400NSM33-F000 is implemented according to Figure 4.3. The IGBT module under test is shown in Appendix. Figure 4.19 and Figure 4.20 are the experimental results for the on-state voltage at the chip level and the tile level respectively. In this case, 3, 5 and 7 bond wires are lifted in IGBT chip 1.1.

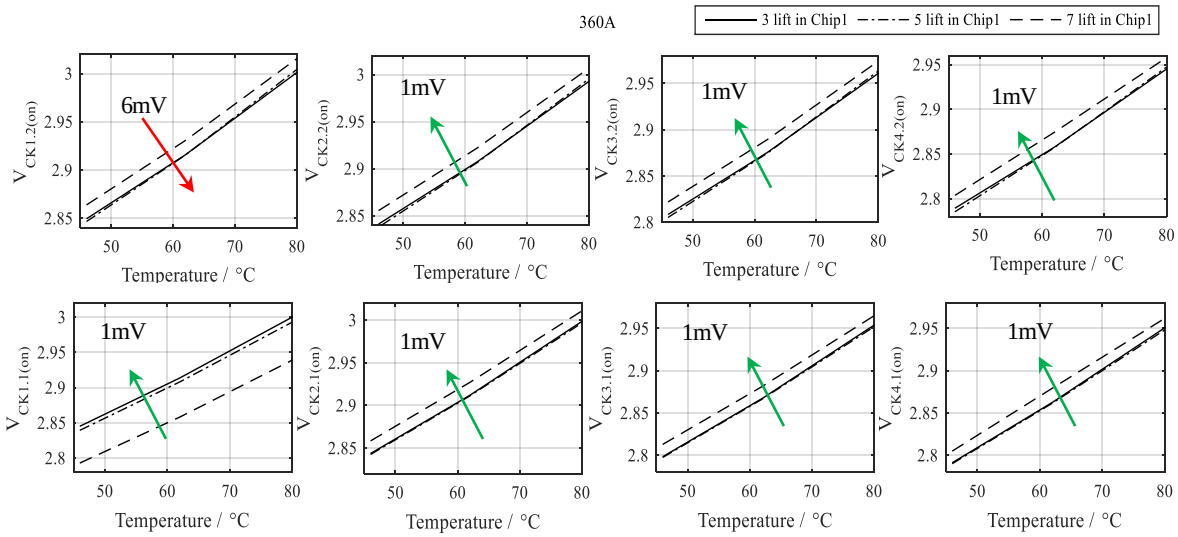


Figure 4.19 Experimental results at chip level: On-state voltage change upon bond wire lift-off in Chip1.1.

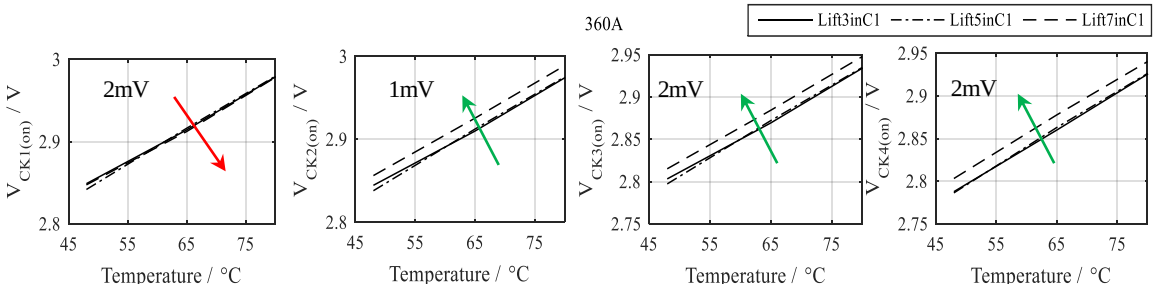


Figure 4.20 Experimental results at tile level: On-state voltage change upon bond wire lift-off in Chip1.1.

In Figure 4.19, the first three bond wire lift-off leads to 6 mV decline in $V_{CK1.1(on)}$ and about 1 mV increment in the on-state voltages of other IGBT chips. A similar trend is observed for $V_{CK(on\text{-}tile)}$. However, compared with $V_{CK1.1(on)}$, the shift of $V_{CK1(on)}$ is smaller as shown in Figure

4.20. There is only 2 mV decrease in V_{CK1} upon the first three bond wire lift-off which means that the bond wire failure is becoming more difficult to be detected with the $V_{CK(on\text{-}tile)}$ & $V_{CE(on)}$ technique.

In conclusion, when there is bond wire lift-off, $V_{CK(on\text{-}chip)}$ and $V_{CK(on\text{-}tile)}$ will decrease. Whilst, $V_{CK(on)}$ of other chips and tiles go up. The experimental results on the Dynex module are consistent with that from the Infineon module. It confirms the proposed method is applicable to various power modules with different DBC layouts.

4.5. **Modification for the extra Kelvin connection**

The modification for the extra Kelvin connection can be equipped to the IGBT module. A demonstration is shown in Figure 4.21. Extra Kelvin terminals are added to each IGBT chip in the mIGBT. Since the Kelvin point is only for measurement, the bond wire can be thin in diameter. In this project, 50 μm aluminium bond wire is used.

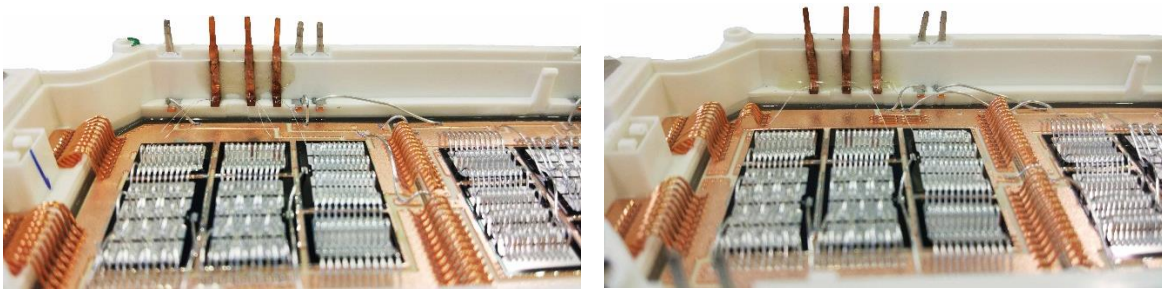


Figure 4.21 Modification for the extra Kelvin pins in the IGBT module.

For mIGBTs that are constructed with several tiles, the Kelvin connection can be chosen between chip connection and DBC tile connection. Compared with the chip connection, the DBC tile connection reduces the number of measurement point used. However, earlier bond wire failures may not be detected and the location of the failure can only be identified regarding the DBC tile but not the individual chip.

Overall, the extra Kelvin connection can be simply constructed in mIGBTs. The Kelvin connection can be chosen according to the detection requirement. The IGBT module can be tailored for the specified application which has a unique advantage regarding bond wire state estimation.

4.6. **Summary**

A novel approach is proposed in this chapter to diagnose bond wire failure. The technique is based on the measurement of on-state voltage of each IGBT chip and the IGBT switch. At first, the proposed $V_{CE(on)}$ and $V_{CK(on)}$ technique is verified on a three-chip Infineon IGBT module. The approach can assess the health condition of bond wires as well as locate the fault when there is bond wire failure. The influence of the bond wire failure on temperature, current distribution and self-heating are investigated. It is found that the bond wire failure can be detected regardless the working temperature environment. Bond wire failure will cause current decrement in the faulty chip which reduces the on-state losses electrical pressure on the faulty chip and attributes to the parallel operation of mIGBT.

In terms of self-heating, the temperature deviation ΔT does go up with the collector current rise. However, ΔT does not show any dependency on the fault condition. This could due to the narrow test pulse and the current decrement caused by the current redistribution. Finally, a repeat of the tests is carried out on a power module using a different DBC layout (Dynex module). Results show the same tendency as observed in the test with the Infineon module. This means that the proposed technique is versatile and can be applied to mIGBT with various packages.

Chapter 5. Offline condition monitoring unit

A number of testers have been developed for IGBTs and other semiconductor devices. Samples are shown in Figure 5.1. These testers can be applied either before assembling IGBT PMs or for troubleshooting. On the one hand, testers help to recognise damaged products for customers which effectively reduce the downtime of the system. On the other hand, they support to reduce the unsubstantiated rejects to manufactures.

(a) (b)

Figure 5.1 (a) DCA75 (Atlas DCA Pro) from Peak Electronics, (b) SKiiP tester developed and produced by Ing. Büro M.Billmann.

However, functions of the testers remain limited. For example, testers do not provide any information about the degradation of IGBT modules such as bond wire state. Although various techniques on bond wire lift-off have been proposed in publications, none of them have been ever designed as a complete unit for field application. In the previous chapter, measurements are taken with the help of oscilloscopes using voltage and current transducer with high bandwidth which is normally used in a laboratory environment. This chapter proposes a CMU that does not require sophisticated instrumentation but still provides the accuracy required to detect bond wire lift-off.

5.1. **Hardware design**

The CMU is constructed based on the proposed $V_{CK(on)}$ & $V_{CE(on)}$ technique described in Chapter 4. The CMU intends to monitor the condition of IGBT modules during maintenance. The aim is to develop a portable device for qualified technicians to diagnose the condition of bond wires in a mIGBT PM.

5.1.1. Structure of the CMU

The structure of the CMU is depicted in Figure 5.2. The CMU is powered by a battery which makes it a standalone system. Semiconductor fuses are used to protect the battery during charging and discharging. Charge terminals are prepared. The circuit breaker S_1 disconnects all DC/DC converters with the battery or to power up all DC/DC converters when the CMU is ready for bond wire state diagnosis.

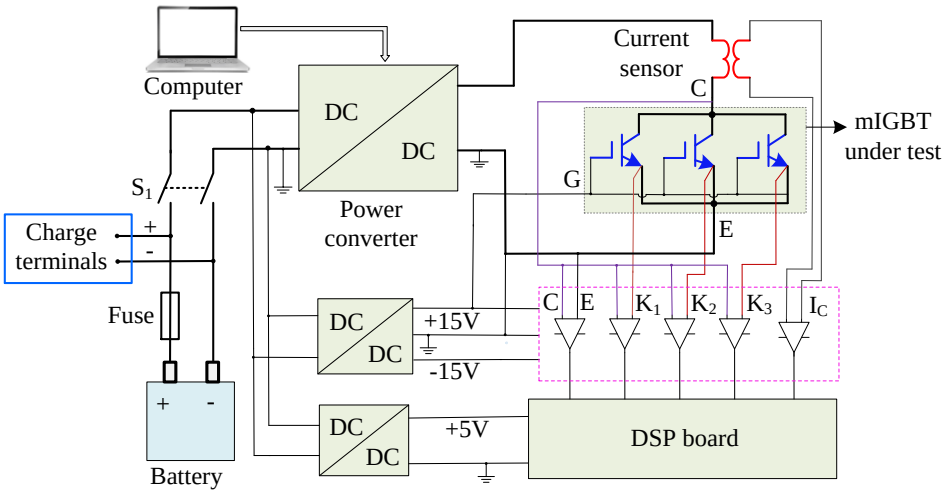


Figure 5.2 Structure of the CMU.

During the diagnose stage, the power DC/DC converter produces a current pulse to inject into the IGBT module. The injected current I_C is measured by the current sensor. Prior the current injection, the IGBT is turned on with +15V on the gate-emitter. The on-state voltage of the IGBT switch and each IGBT chip is regulated with the signal conditioning circuitry and measured via the analogue-to-digital converter (ADC) integrated in the digital signal processor (DSP).

5.1.2. The DC/DC power converter

The DC/DC power converter is the most critical part of the CMU. The unit should be able to deliver low voltage and high current (less than 2 V and up to 100A) to the IGBT module from the 12V battery with high efficiency. The output should be adjustable to deal with various mIGBT PMs. Figure 5.3 lists schematics of several approaches proposed during the design stage. Figure 5.3a shows a current pulse generator inspired by the double pulse technique. When Q1 is turned on, energy is stored in the inductor. When Q1 is switched off, the current in the inductor is injected into the IGBT module Q2. Particular attention should be paid to the

commutation of the switching of Q1 and Q2. Furthermore, I_C is not stable which will cause misleading results because the on-state voltage is affected by I_C.

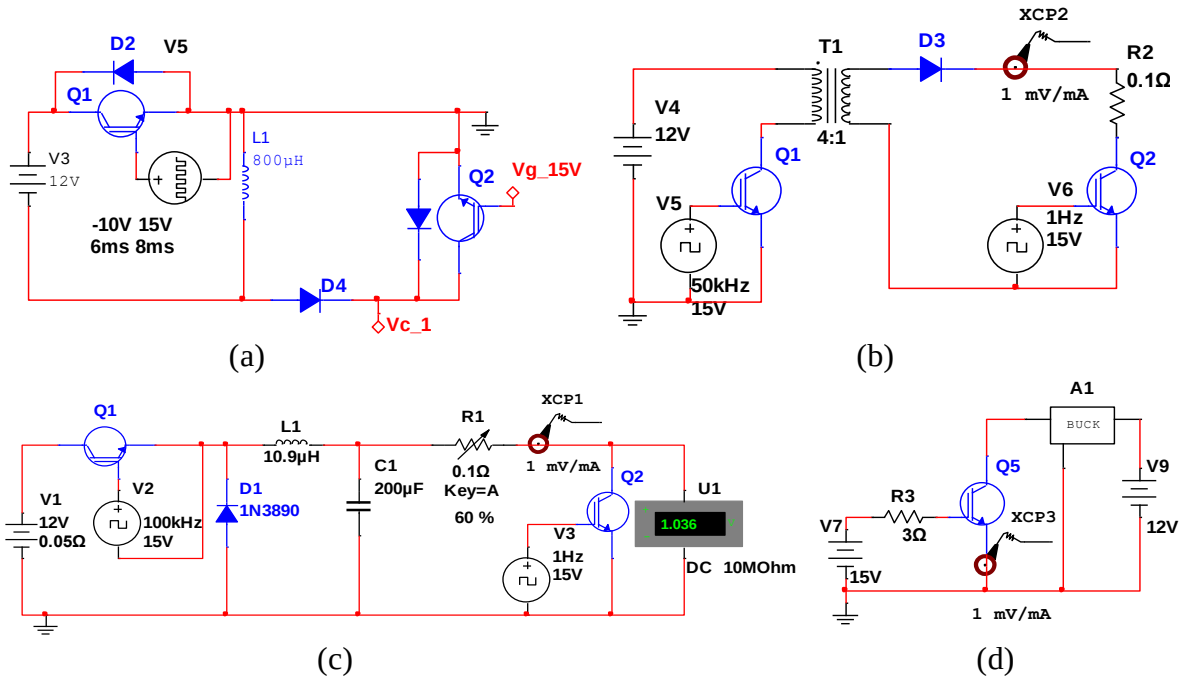


Figure 5.3 Topologies for the DC/DC power converter: (a) Current pulse generator, (b) Flyback converter, (c) Buck converter, (d) Commercial available converter.

Figure 5.3b and Figure 5.3c are a buck converter and a flyback converter respectively. I_C is measured and then be used to control the drive signal for Q1. The buck converter and flyback converter techniques are straightforward solutions. However, additional switching devices and passive components are essential for these two approaches.

Figure 5.3d is the implementation with a commercially available converter from TDK Lambda UK. The DC/DC converter is the iJC series evaluation kit. The kit is able to deliver 0.6 V - 1.5 V and up to 100 A to the IGBT module. The efficiency is about 91.5 % at V_O = 1.5 V. The converter can be easily controlled by the GUI interface. This is the approach employed in this research due to its simplicity, high efficiency and flexibility.

The other components used in the CMU are listed in Appendix.

5.1.3. The prototype of the CMU

Figure 5.4 illustrates the prototype of the CMU. The CMU is powered by a small lead acid battery. Two semiconductor fuses are added in the circuit. Fuse 1 is to protect the battery during

the charging process. Fuse 2 is to protect the battery from high discharging current during the CMU operation. The output of Fuse 2 is connected to the circuit breaker S_1 which powers up/down the remain components of the unit. The output of S_1 is connected to the voltage measurement circuit as well as the DC/DC converter. The voltage measurement circuit provides the signal conditioning for $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and I_C. In addition, the voltage measurement circuit also offers ±15 V and 5 V voltage sources. 15V is to turn the IGBT switch on. The power generated from the DC/DC converter is then injected to the IGBT switch via the C-E terminals. $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ and I_C are captured by the DSP controller.

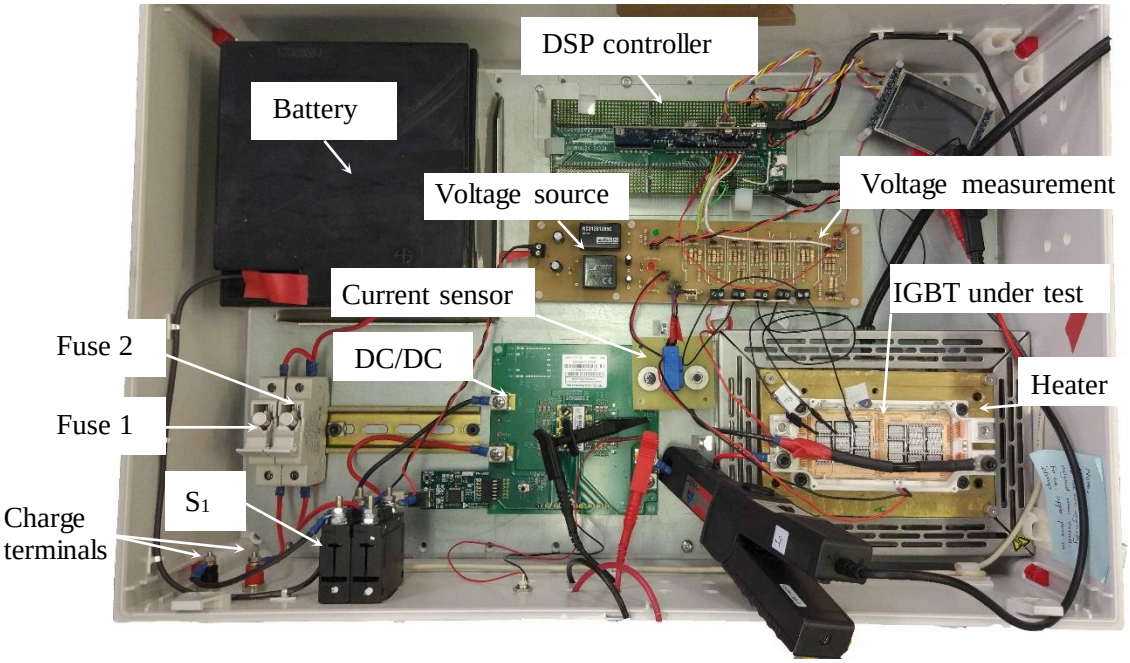


Figure 5.4 The prototype of the CMU.

5.2. **Experimental test**

The operation of the CMU is described in Figure 5.5. The DC/DC converter is a voltage source power supply, its output can be adjusted from the 0.6 V to 1.5 V and the current can go up to 100 A. $V_{CE(on)}$, I_C, $V_{CK1(on)}$, $V_{CK2(on)}$, $V_{CK3(on)}$ at various conditions can be obtained via the CMU.

Bond wire failure detection with the CMU can be divided into two steps, characterisation stage and maintenance stage. The device should be characterised at healthy state. At this stage, the output voltage of the DC/DC converter is adjusted to vary the injected current to the IGBT module. T_{vj} of the IGBT is also changed by the electronic heater. Based on these tests, the output characteristic of the IGBT switch is obtained. Ultimately, the reference tables for $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ are acquired at expected current level. During the maintenance

stage, the output characteristic of the IGBT switch is measured again. The $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ at the set current level is gained as shown in Figure 5.5. The on-state voltage obtained during the maintenance stage is then compared with the reference table to estimate the degradation of the device.

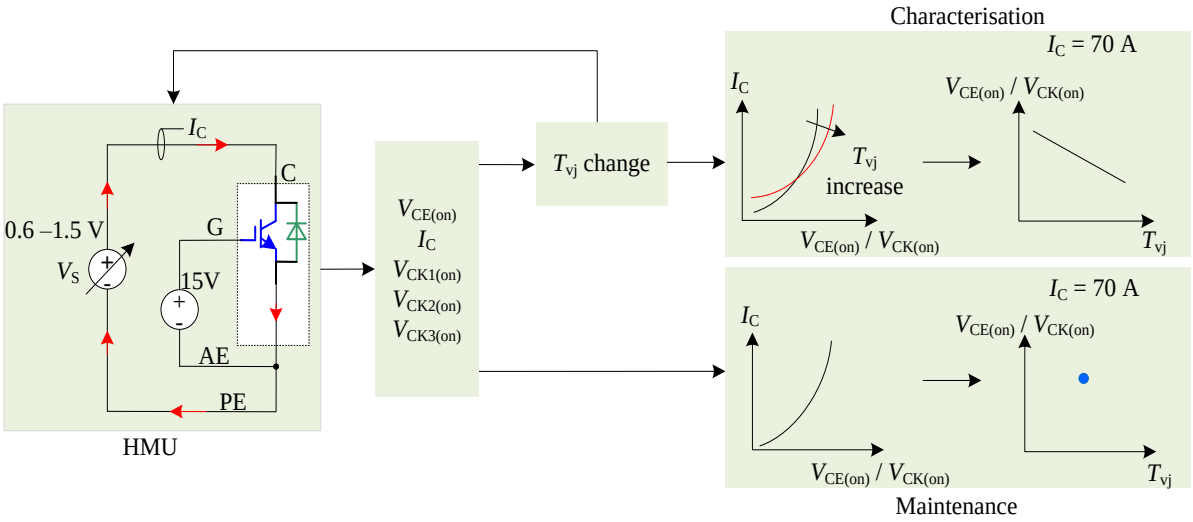


Figure 5.5 Operation procedure of the CMU for failure detection.

One IGBT switch in the half-bridge module FF600R17ME4 is tested to verify the proposed theory and demonstrate the operation procedure of the CMU. The results are presented below.

5.2.1. Characterisation

The healthy IGBT switch is characterised with the CMU as shown in Figure 5.6. The injected current is below the inflexion point, therefore, $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ decline with the increment of T_{vj}. The constant shift is observable in Figure 5.6 which reflect the effective measurement from the CMU. Figure 5.7 depicts the resolution of $V_{CE(on)}$ regarding T_{vj} estimation. The resolution falls in the same range with the measurement from the oscilloscope.

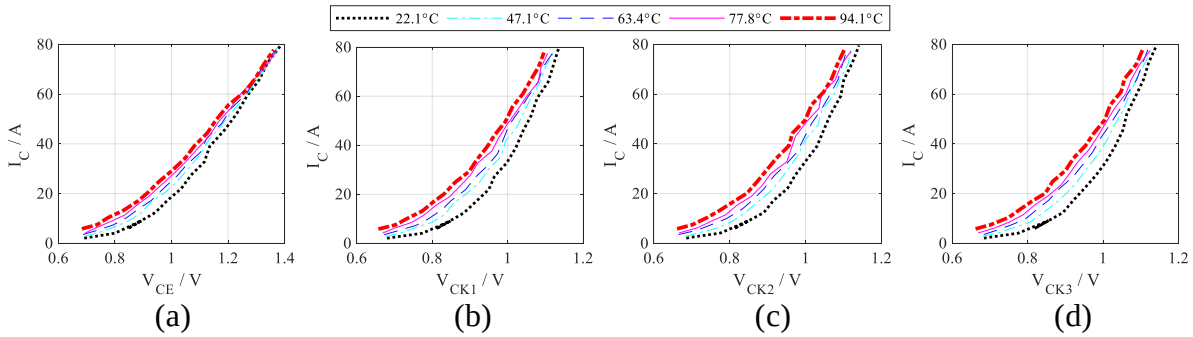


Figure 5.6 Output characterisation for the IGBT switch: (a) V_{CE}, (b) V_{CK1}, (c) V_{CK2}, (d) V_{CK3}.

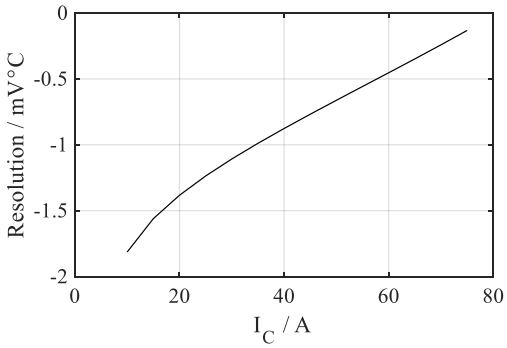


Figure 5.7 Resolution of V_{CE} regarding temperature estimation.

5.2.2. Fault detection

Bond wires are cut to imitate the lift-off during normal working conditions. The test results are illustrated in Figure 5.8. One to four bond wires are cut in Chip1. At I_C = 40 A, the first and the second bond wire failure could not be detected. There is a slight shift upon the third and fourth lift-off. However, these are within the region of the measurement error. Therefore, estimations are not reliable.

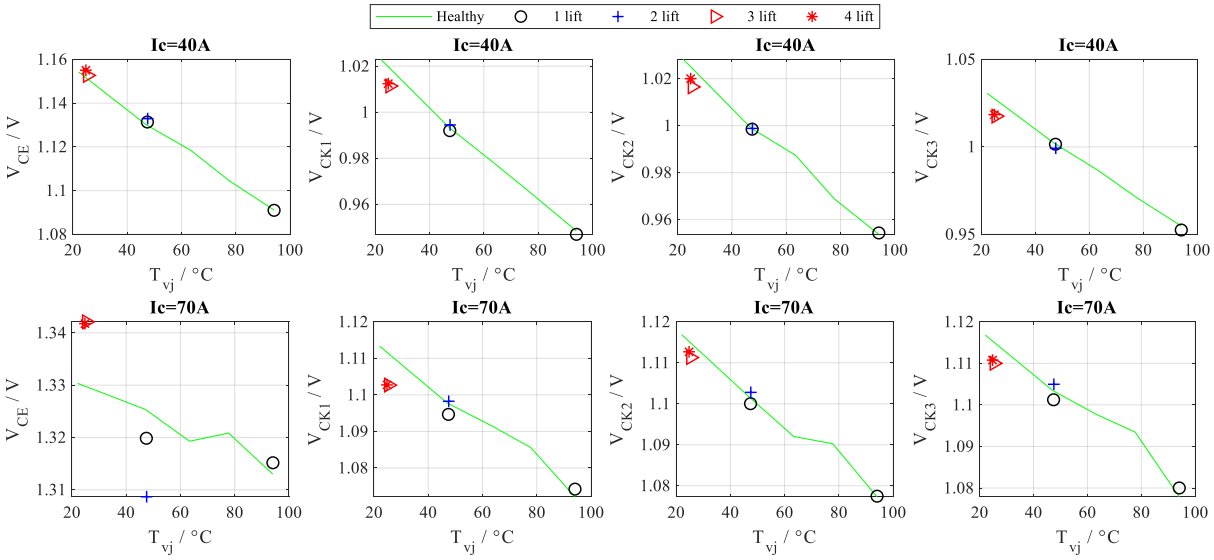


Figure 5.8 Experimental results upon bond wire lift-off at I_C = 40 A and I_C = 70 A.

At I_C = 70 A, there is not any apparent variation upon the first two bond wire failures. Minor changes of $V_{CE(on)}$ and $V_{CK1(on)}$ kick in at 3 and 4 bond wire failures and noticeable changes will be at more than four bond wire lift-offs. The results show therefore that the proposed CMU can be employed for bond wire failure detection. However, compared with results captured by oscilloscope, only more than four bond wire lift-offs can be identified with the CMU due to errors in the circuitry and the accuracy limitation of components.

5.2.3. Sources of errors

The reduced sensitivity of the CMU is due to the limited accuracy of the measurement components. Firstly, part of the error comes from the ADC sampling circuitry. Figure 5.9 shows the curve fitting results when the ADC sampling of the DSP processor is transferred to the voltage. The coefficient of determination of the curve fitting is more than 0.99. The model indicates a good replicate the original data.

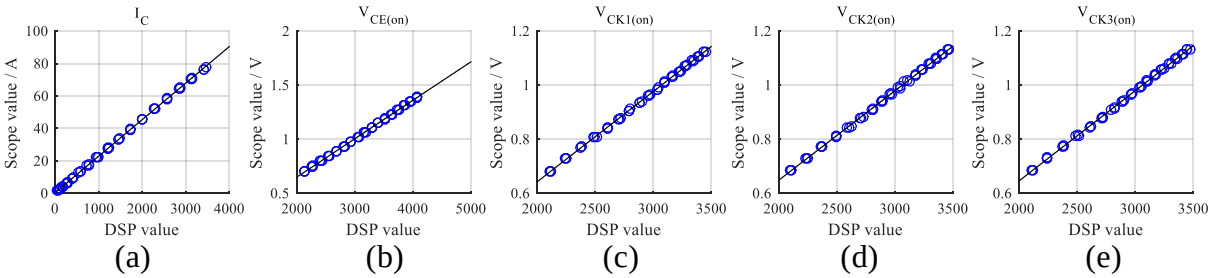


Figure 5.9 Curve fitting for ADC samples: (a) I_C, (b) $V_{CE(on)}$, (c) $V_{CK1(on)}$, (d) $V_{CK2(on)}$, (d) $V_{CK3(on)}$.

However, this curve fitting for ADC introduces errors. The error caused by the curve fitting is illustrated in Figure 5.10. The region between the dashed lines is the error margin where 95% of the samples fall into. In this thesis, this is referred to as the error region. The error region for I_C, $V_{CE(on)}$, $V_{CK1(on)}$, $V_{CK2(on)}$ and $V_{CK3(on)}$ are - 0.5 A to 0.5 A, -9.1 mV to 9.1 mV, -5 mV to 5 mV, -7.1 mV to 7.1 mV and -7 mV to 7 mV respectively. According to the characterisation, a 0.5 A shift in I_C could lead to 1 mV - 3mV variation in the on-state voltage.

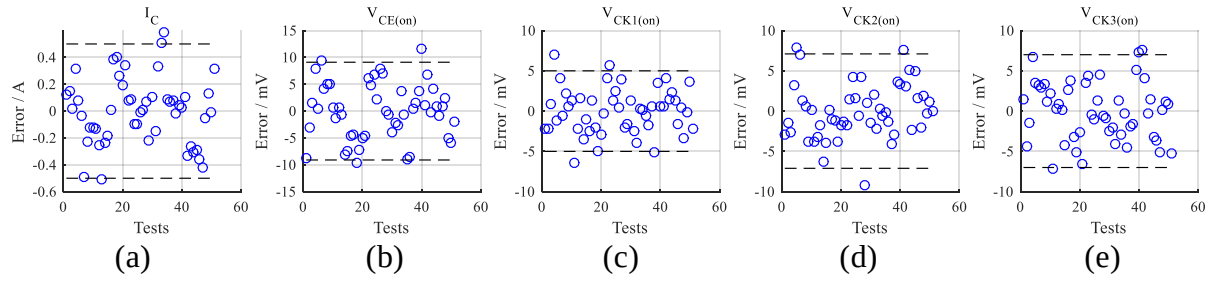


Figure 5.10 Error during induced by the curve fitting: (a) I_C, (b) $V_{CE(on)}$, (c) $V_{CK1(on)}$, (d) $V_{CK2(on)}$, (d) $V_{CK3(on)}$.

There are also errors induced by the DC/DC power converter. The input and output characteristics of the power DC/DC converter is shown in Figure 5.11. The converter generates a pulse current for the IGBT switch. Due to the sudden change, the battery voltage V_{in} plunges. The decrement varies from 0.03 V to 0.55 V depending on the output power. When the converter switches off, V_{in} rebounds to a lower value. Since the voltage source is also powered by the battery, the sudden voltage decline in the battery could affect the output of the voltage

source in Figure 5.4, which is the power supply for the amplifiers and the DSP processor. Furthermore, the voltage source is also utilised to turn on the IGBT. The instability may lead to a shift in the output characteristic of the IGBT switch.

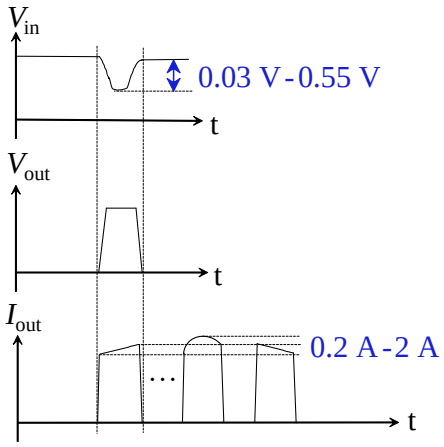


Figure 5.11 Fluctuation in the DC/DC converter.

In addition, the output current I_{out}, which is injected into the IGBT, is not flat. Various shapes appear during the test as illustrated in Figure 5.11. The fluctuation will lead to minor changes in the on-state voltage. The changes do not have a regular pattern and are not predictable or amendable. The fluctuation of I_{out} will also cause an error during the test.

5.3. **Discussions**

The preliminary results verified the effectiveness of the proposed schematics for the CMU. However, there are modifications that could be done to improve the accuracy of the unit if required.

Figure 5.12 shows the error source in the HMU. The error source has been divided into three stages according to their occurrence in during the measurement. In the first stage, the error comes from the power source. Stable I_C provides stable response of the on-state voltage and helps improve the accuracy. At the second stage, the current and the on-state voltage are captured and regulated before they are sending to the DSP processor. At this stage, the working condition or the accuracy of the current sensor is vital. At the third stage, the ADC is utilized to obtain the analogue value. The resolution and the working condition of the ADC will also influence the accuracy.

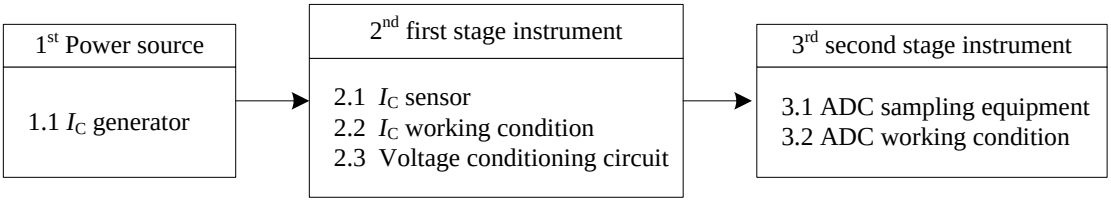


Figure 5.12 Error source.

The preliminary results verified the effectiveness of HMU. The following steps can be implemented to improve the accuracy of the unit.

1) For this implementation, the DC/DC converter is voltage source. In order to compare the on-state voltage, measurements have to be transferred to the same current level. This process could introduce secondary errors. To improve this, the power DC/DC converter can be modified as a current source. Moreover, multiple DC/DC converters can be paralleled for higher output current which makes the device versatile. This technique helps to reduce the error caused in the power source as list in 1.1 in Figure 5.12.
2) The current sensor A current sensor with higher resolution. This technique helps to reduce the error caused in 2.1 in Figure 5.12.
3) Increase resolution of ADC from 12-bit to 16-bit. This technique helps to reduce the error caused in 3.1 in Figure 5.12.
4) A separate battery could be used to provide a stable voltage power supply. This technique helps to reduce the error caused in 2.2, 2.3 and 3.2 in Figure 5.12.

5.4. **Summary**

This chapter introduces the prototype of the CMU which can be applied in field application. The implementation and the test results are presented and analysed. Finally, suggestions are provided about improvements of the CMU.

Chapter 6. Signal sweeping technique for online condition monitoring

In condition monitoring for IGBT modules, generally, three aspects are highly concerned, namely T_{vj}, solder degradation and bond wire failure. T_{vj} and bond wire lift-off are the focus of this thesis. Typically, each of existing techniques can only estimate one condition, either T_{vj} or bond wire failure. Thus, multiple tests or multiple health indicators must be applied in order to decouple their influence and determine the root cause. For example, in [66], the integrated diagnostic system measures $V_{CE(on\text{-}sense)}$ and $V_{CE(on\text{-}load)}$. $V_{CE(on\text{-}sense)}$ is used for T_{vj} estimation, while $V_{CE(on\text{-}load)}$ is recorded to trace bond wire lift-off. Similarly, the combination of $V_{CE(on\text{-}sense)}$ and $R_{CE(on)}$ has been employed for the estimation of T_{vj} and bond wire failure respectively [73].

A signal sweeping technique is proposed in this chapter. This technique is able to decouple the influence of bond wire lift-off and T_{vj} and applicable online. The proposed technique is applied to a mIGBT module through the gate-emitter terminals.

6.1. **Sweep signal and its application**

Sweep signal is also called chirp signal which originates from the chirping sound from the bird. A sweep signal is a signal whose frequency increases or decreases with time [92]. The waveform can be expressed as (6.1).

$$s(t) = a(t)\sin[\theta(t)] \tag{6.1}$$

Where θ(t) is the phase, a(t) is the envelope.

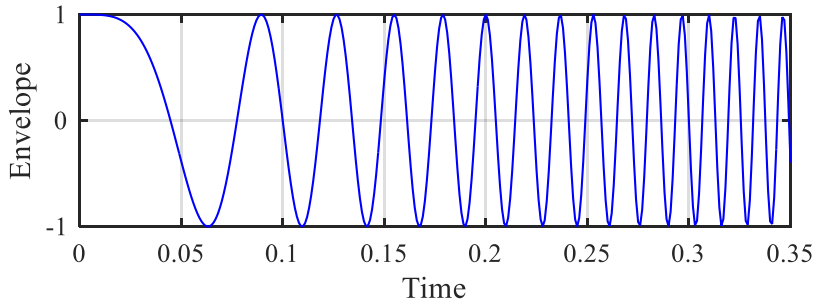


Figure 6.1 Example of a sweep signal.

Figure 6.1 is an example of a sweep signal. Sweep signals have been employed in spread spectrum communications to obtain high immunity against radio frequency noise. This technique has also been combined with the time domain reflectometry (TDR) to detect fault in

live wire. An extension of TDR is Spread Spectrum Time Domain Reflectometry (SSTDR) and combined with chirp signals the ageing of a MOSFET is detected by monitoring $R_{DS(on)}$ [93].

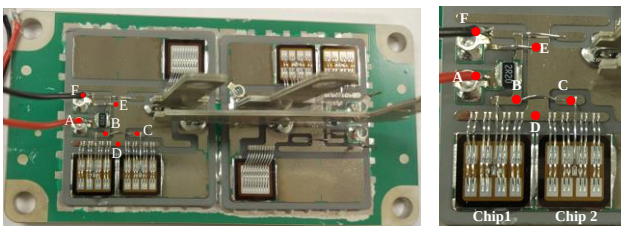
6.2. **Modelling of the gate-emitter circuitry in an IGBT module**

Modelling of IGBTs are required to investigate the gate-emitter circuit behaviour [94]. A few of the proposed modeling methods include parasitic components of the package which are important to consider the impact of transient parameters. A small signal model for the IGBT PM was derived in [77] with the help of an LCR meter. However, LCR meters only measure cumulative resistance and inductance, which does not reflect the detailed parasitic information regarding individual components. Another experimental technique is proposed in [95] which measures parasitic inductors and capacitors for a three-phase, six-pack IGBT PM. In [95], the parasitic elements between different IGBT switches were studied.

In the scope of this thesis, the main concern is the parasitic parameters amongst individual IGBT chips within an IGBT switch. Therefore, a small signal model for the IGBT switch has been developed.

6.2.1. Parasitic components in the gate-emitter circuitry

In this study, the proposed technique is investigated on a Dynex 3.3kV, 100A IGBT PM (DIM100PH-M33-F). The open module is shown in Figure 6.2a. This is a half-bridge module with two IGBT chips and one diode chip in each switch. The two parallel connected IGBT chips represent one IGBT switch which are highlighted in Figure 6.2b.



(a) (b)

Figure 6.2 DIM100PH-M33-F IGBT module: (a) Open IGBT PM, (b) Zoom in diagram for the IGBT chip section.

The gate-emitter circuit is divided into several parts in order to derive the electrical model of circuit. The assignation is denoted with the red dot in Figure 6.2b. These components can be categorised as bond wires, copper tracks, the surface mount resistors and IGBT chips. The

copper tracks and bond wires are represented with a parasitic resistor in series with a parasitic inductor. These include the copper tracks from A to B, from D to E and all the bond wires. The surface mount resistor is represented with the circuit shown in Figure 6.3.

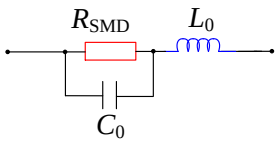


Figure 6.3 Small signal model for the surface mount resistor.

The IGBT chip itself is characterised as a combination of an ideal IGBT switch with intrinsic capacitors C_{GE}, C_{GC}, C_{CE} and intrinsic gate resistor $R_{G(int\text{-}chip)}$ as shown in Figure 6.4.

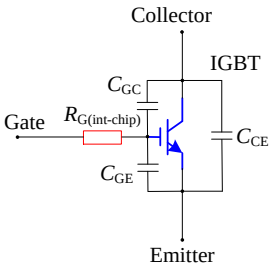


Figure 6.4 Small signal model for the IGBT chip.

The electrical model for gate-emitter circuit of the IGBT switch is depicted in Figure 6.5. Starting from A in Figure 6.2, this small-signal model consists of parasitic resistor R_{AB} and parasitic inductor L_{AB} of the copper track between the point A and the point B without the surface mount resistor. The surface mount resistor is represented by an equivalent circuit consisting a resistor (R_{SMD}), an inductor (L_0) and a capacitor (C_0) so that the high frequency behaviour is reflected. The gate bond wire from the point B to the gate of the chip 1 on the left is represented with R_{g1} and L_{g1} . The bond wire between the point B and the point C is represented with R_{BC} and L_{BC}. The gate bond wire from the point C to the gate of the chip 2 on the right is represented with R_{g2} and L_{g2}. There are eight emitter bond wires for each chip which are represented with eight individual resistor R_{eWire} and inductor L_{eWire}. All these bond wires are connected on the copper track and then linked to the point D. These parasitic parameters for this part are represented as R_{e1D}, L_{e1D} for the chip1 and R_{e2D}, L_{e2D} for the chip2. The emitter copper track from the point D to the point E is shown as L_{DE} and R_{DE}. The emitter interconnection bond wire from the point E to the point F is represented with L_{EF} and R_{EF}.

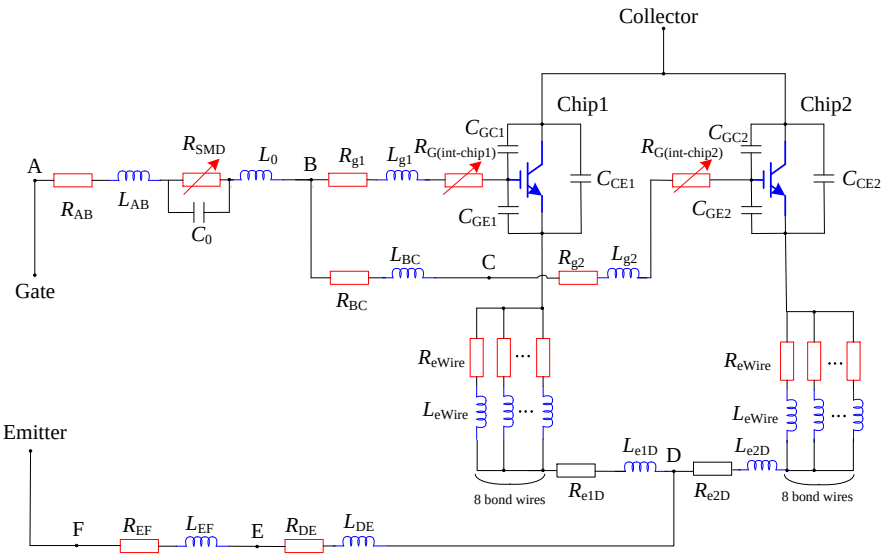


Figure 6.5 Schematic of the equivalent model for the gate-emitter circuit.

6.2.2. Impact of T_{vj} and bond wire lift-off on the parasitic components

T_{vj} mainly influences the characteristics of the components within the IGBT chip, such as the $R_{G(int-chip)}$ and C_{ies}. C_{ies} is the summation of C_{GE} and C_{GC}. Change of the T_{vj} will lead to variation in C_{ies} as shown in Figure 6.6. During the off state, C_{ies} remains nearly the same regardless of the value of V_{CE} and changes slightly when T_{vj} varies. However, when V_{GE} is just below 0V, C_{ies} changes significantly with V_{CE} and T_{vj}. More specifically, C_{ies} declines with V_{CE} rise and increases with T_{vj} growth. During the on state, the input capacitance does not vary with V_{CE} but grows dramatically with T_{vj} rise.

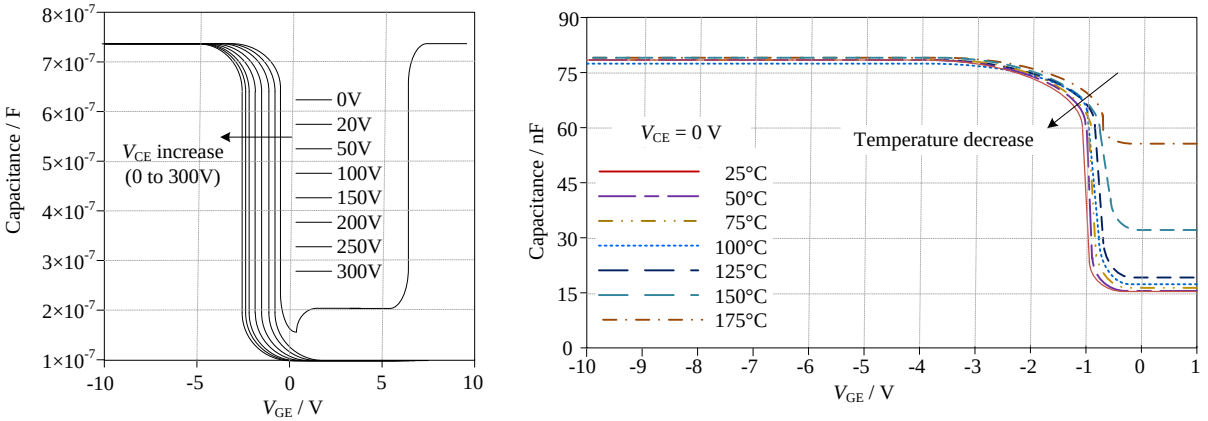


Figure 6.6 Impacts of working condition on C_{ies}: (a) Influences from V_{CE} and V_{GE} [96], (b) Influences from V_{GE} and T_{vj} [46].

Table 6.1 Temperature coefficient of resistance

Material	Components	Temperature coefficient of resistance
Aluminium	Bond wires	0.004308
Copper	Cooper track	0.004041

The change of T_{vj} will also lead to variation in R_{SMD} as well as minor changes in the copper track and the bond wires in Figure 6.2b. Table 6.1 illustrates the temperature coefficient of resistance for aluminium and copper which can quantify the variation in copper tracks and bond wires. This change will affect the electrical characteristics of the IGBT module.

In terms of the bond wire lift-off, the equivalent resistance of the bond wire parts will increase as well as the equivalent inductance. In general, bond wire lift-off does not influence the capacitance of the gate-emitter circuitry. In the case of the Dynex IGBT module in Figure 6.2, it has eight silver metallization area for each IGBT chip as shown in Figure 6.2b. The silver tiles are connected meaning that even if all bond wires of a section are lifted off, the capacitor of the corresponding IGBT chip remains because of the connection from other bond wires. Hence, bond wire lift-off will not influence the capacitance of the gate-emitter circuit.

6.3. **Proposed signal sweeping technique**

The proposed technique is based on radio frequency signals. This method sweeps very low power high-frequency AC signals to the IGBT module through the gate-emitter loop. An impedance curve for the gate-emitter circuitry is obtained. In this test, the frequency of the sweep signal ranges from 300 kHz to 100 MHz and the amplitude is 5 mV peak-to-peak. The frequency range of the sweep signal is determined by the capacitance C, inductance L and resistance R in the circuit. The variation of L, R, C value can only be captured when the contribution of these three parts are comparable. Otherwise, the influence of the parameter (C, L or R) would be too small to be considered. In this example, the input capacitance is 18nF, the gate resistance is 2.2Ω. The contribution of these parameters are considered comparable when their impedance ratio is between 1/3 and 3. This means $2\pi fC/R$ should be between 1/3 and 3. After calculus, it can be obtained that the frequency should be 1.3MHz to 12MHz. Therefore, the frequency is chosen to be 300 kHz to 100 MHz to provide enough margin. The amplitude of the sweep signal is a compromised so that it is large enough to capture and small enough not to change the state of the IGBT.

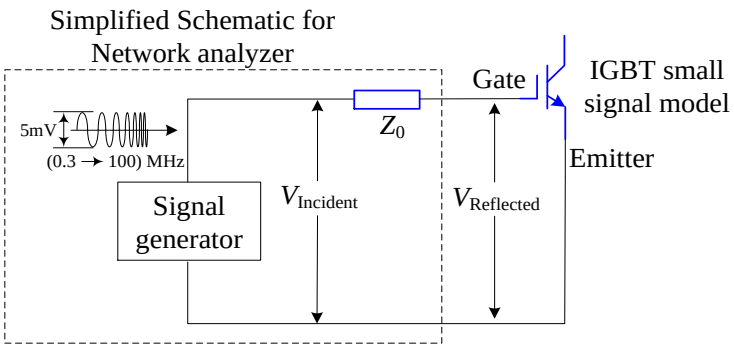


Figure 6.7 Signal sweeping technique for IGBT PM.

The circuit used in the proposed technique is shown in Figure 6.7 where sweep signal is injected into the gate-emitter circuit through a transmission line Z_0 = 50 Ω. The impedance mismatch between the signal source and the gate-emitter circuit will cause a reflection of the incident signals. The reflected signal $V_{Reflected}$ combined with the incident signal $V_{Incident}$ are deployed for the reflected coefficient as described in (6.2).

$$\Gamma = \frac{V_{Reflected}}{V_{Incident}} \tag{6.2}$$

This reflection coefficient is processed to deduce the frequency response of the gate-emitter impedance Z_{GE}, according to (6.3).

$$Z_{GE} = \frac{1+\Gamma}{1-\Gamma} Z_0 \tag{6.3}$$

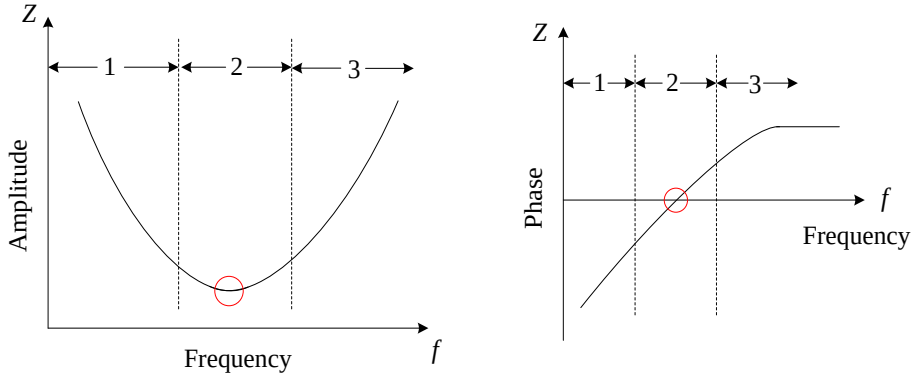


Figure 6.8 Frequency response of gate-emitter impedance Z_{GE}: (a) Amplitude, (b) Phase.

Frequency response of Z_{GE} is shown in Figure 6.8. At lower frequencies, the capacitor dominates the frequency response, which is indicated in Zone 1. At higher frequencies, the inductor dominates the frequency response, which is depicted in Zone 3. The resonant frequency locates in Zone 2 when the amplitude reaches the minimum value, and the phase is zero. When T_{vj} changes, the equivalent resistance will change, as a result the magnitude at the

resonant point will change. However, the inductance and capacitance, which influence imaginary part, will not influence the resonant behaviour of the gate-emitter circuit. Variation in T_{vj} or bond wire state will alter the Z_{GE} and thereby affect its frequency response. Consequently, the frequency response of Z_{GE} can be analysed to estimate T_{vj} and predict the bond wire lift-off.

It should be noted that the IGBT module in the test is not biased, so there is not any voltage across collector and emitter.

6.4. **Simulation**

The small-signal model for the Dynex 3.3kV, 100A IGBT module is characterised. The proposed technique is applied to the IGBT model in SaberRD for validation.

6.4.1. Model Characterization

6.4.1.1. Characterisation for package layout

In general, parasitic parameters of the IGBT package are determined by the module layout. To simplify the calculation, material in different segments is assumed to be pure copper or pure aluminium. At high frequency, the self-inductance of a straight wire can be calculated as (6.4) [97].

$$L = 0.002l\left[\ln(\frac{4l}{d}) - 1.0 + \frac{d}{2l} + \frac{\mu r T(x)}{4}\right](\mu H) \tag{6.4}$$

Where $T(x) \approx \sqrt{\frac{0.873011 + 0.00186128x}{1 - 0.278381x + 0.127964x^2}}$ and $x = 2\pi r\sqrt{\frac{2\mu f}{\sigma}}$.

In (6.4), d is the diameter in cm, l is the length in cm, f is the frequency in Hz, r is the radius of the conductor in cm. σ is the conductance in S/m, and μ is the absolute magnetic permeability of the conductor.

The copper layer from the DCB substrate is treated as a flat wire. Thus, its inductance can be expressed as (6.5) [98].

$$L = 0.002l\left[\ln(\frac{2l}{w+t}) + 0.5 + 0.2235(\frac{w+t}{l})\right](\mu H) \tag{6.5}$$

Where l is the length in cm, w is the width in cm, and t is the thickness in cm.

Regarding the resistor, it is well known that the resistance can be obtained as (6.6).

$$R = \rho\frac{l}{S} \tag{6.6}$$

Where ρ is resistivity of the material, l is length and S is the cross-section area.

6.4.1.2. Parasitic parameters for IGBT chip

The small-signal model for the surface mount resistor is shown in Figure 6.3. It is equal to a capacitor in parallel with a resistor and then in series with a parasitic inductor. The impedance response of the R_{SMD} used in the PM was measured and is shown in Figure 6.9. The impedance magnitude reaches the lowest at a resonant frequency. Capacitor C_0 will affect the frequency response before the resonant point, while inductor L_0 dominates after resonant point. According to the frequency response, R_{SMD} is equal to 2.17 Ω, L_0 is equal to 5.7 nH and capacitor C_0 is equal to 22.9 pF.

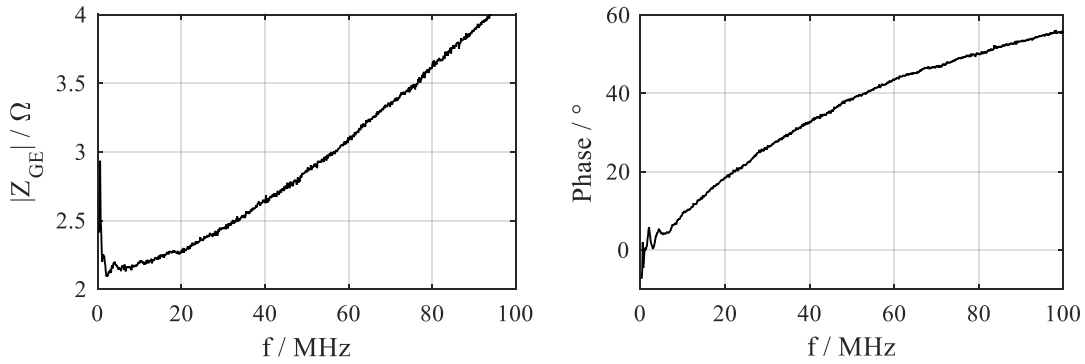


Figure 6.9 The frequency response of R_{SMD}: (a) Magnitude, (b) Phase.

6.4.1.3. Parasitic parameters for the IGBT chip

As illustrated in Figure 6.4, the IGBT chip is modeled by a combination of an ideal IGBT switch with intrinsic capacitance C_{GE}, C_{GC}, C_{CE} and intrinsic resistance $R_{G(int\text{-}chip)}$. The capacitance of the module is determined according to the datasheet values as shown in

Table 6.2 [99]. The input capacitance of the module has been taken as about 18 nF. Since there are two IGBT chips in each switch, it is assumed that the input capacitance for each chip is 9

nF. The turn-on delay can be obtained with (6.7) [47]. Therefore, the gate resistor on each chip $R_{G(\text{int-chip})}$ is approximately 1.12 Ω.

$$t_{don} \approx (R_{G(on)} + R_{SMD} + R_{G(\text{int}-chip)}) \times C_{ies} \tag{6.7}$$

Table 6.2 Parameter from Datasheet

Symbol	Parameter	Test Conditions	Typical Value
C_{ies}	Input capacitance	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz	18 nF
C_{res}	Reverse transfer capacitance		0.28 nF
t_{don}	Turn on delay time	C_{GE} = 33 nF, $R_{G(on)}$ = 33 Ω @ 25°C	1180 ns

Detailed information of all inductive and resistive parameters is presented in Table 6.3.

Table 6.3 Parasitic parameter for IGBT layout

Position & material		Physical Size *l*/cm	*w*/cm	*t*/cm	L/ nH	R/ mΩ	L_{total}/ nH	R_{total}/ mΩ
	Cu	0.4	0.05	0.03	2.28	0.45		
AB	Cu	0.6	0.20	0.03	2.69	0.17	6.13	0.51
	Cu	0.6	0.30	0.03	2.30	0.11		
BC	Al	1.2	0.05	0.05	9.17	1.62	9.17	1.62
B to Chip1	Al	1.7	0.05	0.05	14.15	2.30	14.15	2.30
C to Chip2	Al	1.7	0.05	0.05	14.15	2.30	14.15	2.30
Bond wire	Al	1.9	0.05	0.05	16.23	2.57	16.23	2.57
e1 to D	Cu	0.2	0.2	0.03	0.5	0.06	0.5	0.06
e2 to D	Cu	0.2	0.2	0.03	0.5	0.06	0.5	0.06
DE	Cu	1.4	0.40	0.03	6.84	0.20	6.84	0.20
	Al	1.0	0.05	0.05	7.28	1.35		
EF	Cu	0.6	0.20	0.03	2.69	0.17	11.11	1.75
	Cu	0.4	0.05	0.03	2.28	0.45		

l is length, *w* is the width, *t* is thickness.

6.4.2. Simulation and analysis

The extracted small-signal model for the gate-emitter circuit is tested in SaberRD to evaluate the proposed technique. The implementation of the simulation is described in Figure 6.10.

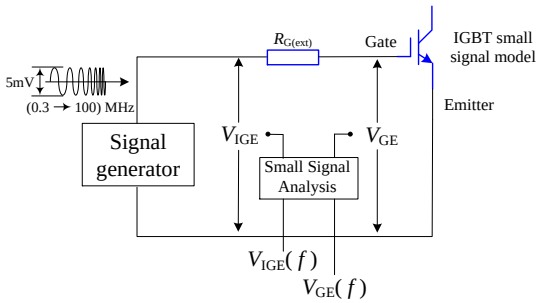


Figure 6.10 Simulation implementation.

The sweep signal is injected into the gate-emitter circuit. The signals before and after the external gate resistor $R_{G(ext)}$ are incident gate-emitter signal $V_{Incident}$ and V_{GE} respectively. They are recorded and transferred to the frequency domain through small signal analysis. The frequency response of Z_{GE} is then generated according to equation (6.8).

$$Z_{GE} = \frac{V_{GE}}{V_{Incident} - V_{GE}} \times R_{G(ext)} \tag{6.8}$$

Simulation tests are carried out with different T_{vj} and various bond wire conditions. After that, the captured data are processed in MATLAB to generate the frequency response of Z_{GE} as shown in Figure 6.11. At low frequency, the response is dominated by the capacitor. At high frequency, Z_{GE} is mainly affected by the inductors. On the other hand, T_{vj} primarily influences the resistance part of the impedance. Therefore, distinct deviation of Z_{GE} against T_{vj} is observed in the frequency band between 5 MHz and 14 MHz.

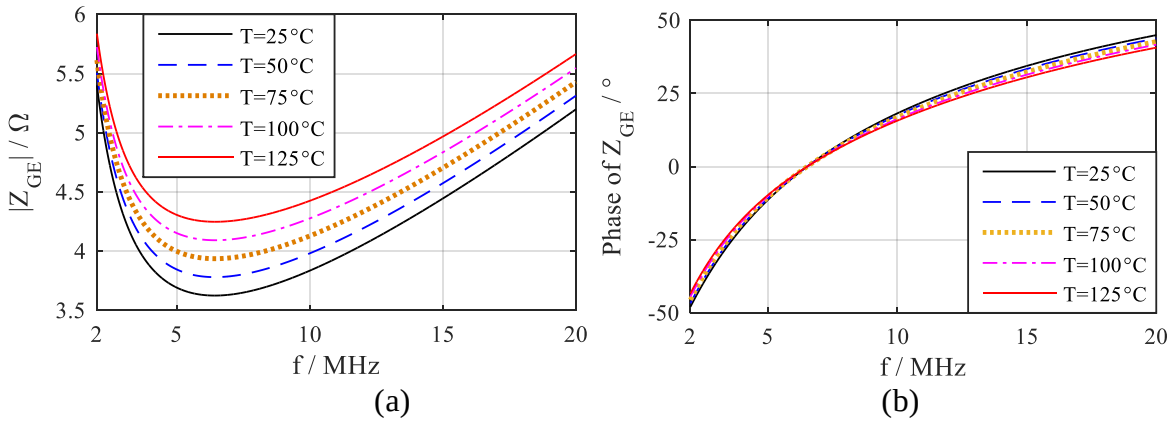


Figure 6.11 Simulation results of the frequency response of Z_{GE} against T_{vj}: (a) Amplitude, (b) Phase.

Figure 6.12 and Figure 6.13 depict the variation of Z_{GE} in case of T_{vj} change and bond wire failure. These values are obtained at 6.5MHz. Figure 6.12 illustrates the variation of the real part of Z_{GE}, which is denoted as $Z_{GE(Real)}$. $Z_{GE(Real)}$ goes up with the rise of T_{vj} and bond wire lift-offs. The change in the imaginary part $Z_{GE(Imag)}$ is described in Figure 6.13. $Z_{GE(Imag)}$ declines

with T_{vj} increment. However, $Z_{GE(Imag)}$ rises with the increasing number of bond wire lift-offs. Thus, the impacts of T_{vj} and bond wire failure are completely different in $Z_{GE(Imag)}$. This phenomenon can be utilised to decouple the influence caused by T_{vj} and bond wire failure. According to Figure 6.12 and Figure 6.13, it can also be noticed that the variation of $Z_{GE(Imag)}$ against T_{vj} is smaller compared to that of $Z_{GE(Real)}$. It indicates that $Z_{GE(Real)}$ has better resolution regarding T_{vj} estimation in comparison with $Z_{GE(Imag)}$. In conclusion, simulation results verify that the imaginary part could be utilised to determine bond wire lift-off and $Z_{GE(Real)}$ can be applied to estimate T_{vj}. The proposed technique is novel, because, in the past two different measurement techniques must be applied to detect bond wire lift off and T_{vj}. For the first time it is shown that only one measurement technique is sufficient to distinguish both parameters.

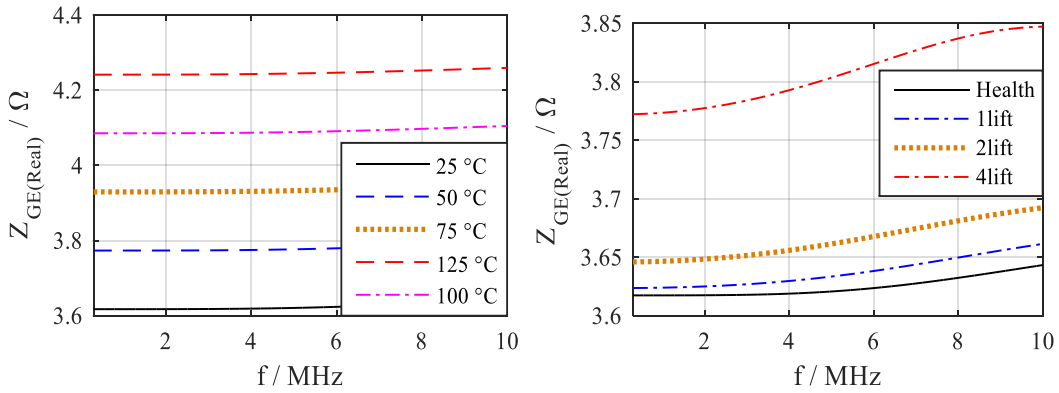


Figure 6.12 Simulation results for $Z_{GE(Real)}$: (a) Variation against T_{vj}, (b) Variation with bond wire lift-off @ 25°C.

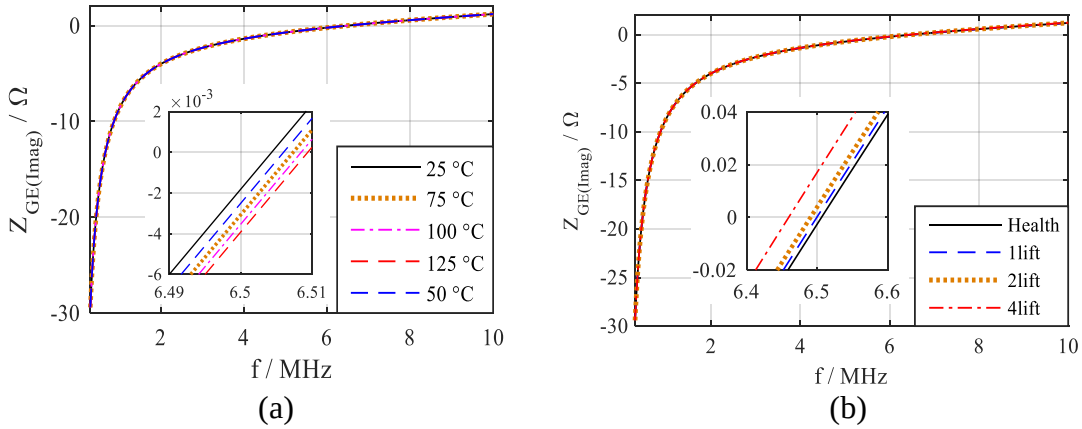


Figure 6.13 Simulation results for $Z_{GE(Imag)}$: (a) Variation against T_{vj}, (b) Variation with bond wire lift-off @ 25°C.

6.5. **Experimental tests**

6.5.1. The setup

The proposed technique has also been verified practically with a network analyser (Agilent Keysight E5071B). The test setup is illustrated in Figure 6.14. The mIGBT PM is mounted on a heat plate which is controlled by an electronic heater to vary T_{vj}. During the test, the IGBT is heated beforehand to ensure T_{vj} equals the temperature of the heat plate. Afterwards, the sweep signal generated by the network analyser is injected into the PM through a coaxial connector.

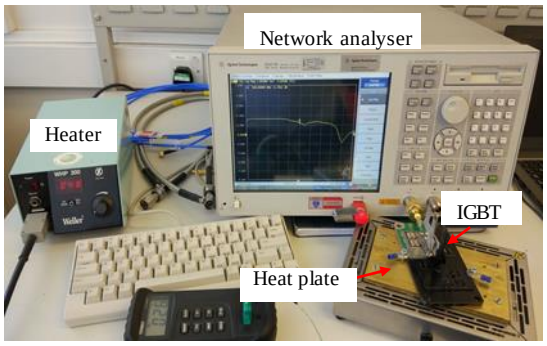


Figure 6.14 Experimental setup.

The reflection coefficient is recorded and processed in MATLAB. According to equation (6.3), the frequency response of Z_{GE} is acquired. Bond wires have been cut to investigate its influence on the frequency response of Z_{GE}.

6.5.2. Junction temperature estimation

Figure 6.15 shows the frequency response of Z_{GE} against T_{vj}. The amplitude of the Z_{GE}, which is referred to as $|Z_{GE}|$, decreases with the frequency increment and reaches minimum-value at the resonant point. Afterwards, $|Z_{GE}|$ bounces back with frequency rise. This is the empirical frequency response of a RLC circuit.

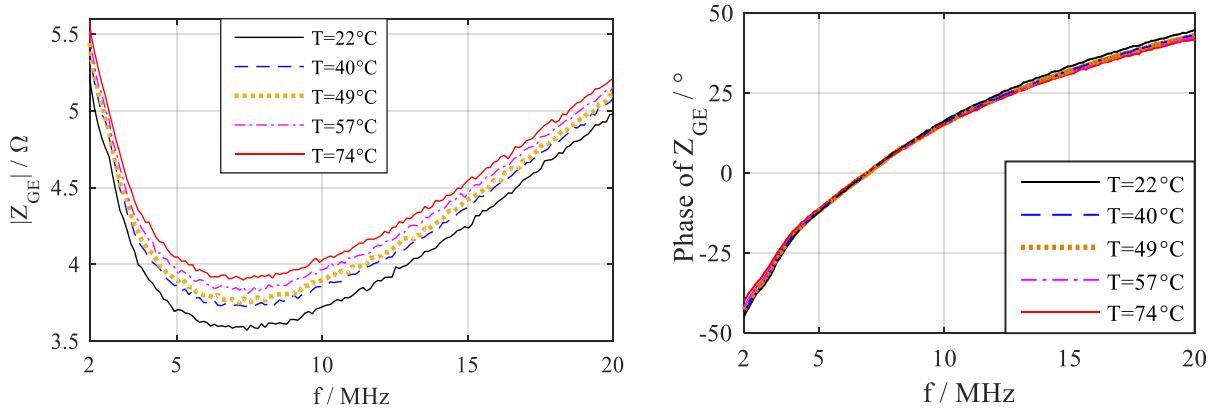


Figure 6.15 Experimental results for the frequency response of Z_{GE} against T_{vj}: (a) Amplitude, (b) Phase.

Figure 6.15 demonstrates that $|Z_{GE}|$ at a resonant point changes linearly with temperature which can be used as T_{vj} indicator. The sensitivity of $|Z_{GE}|$ changes with frequency. The results from simulation and experimental test are shown in Figure 6.16. The resolution of $|Z_{GE}|$ reaches the peak near the resonant point. Even though the resolution tendency of experimental results resemble that of the simulation, there is difference between them which could be caused by the approximation during the characterising of the simulation model and the tolerance between data sheet and each IGBT module.

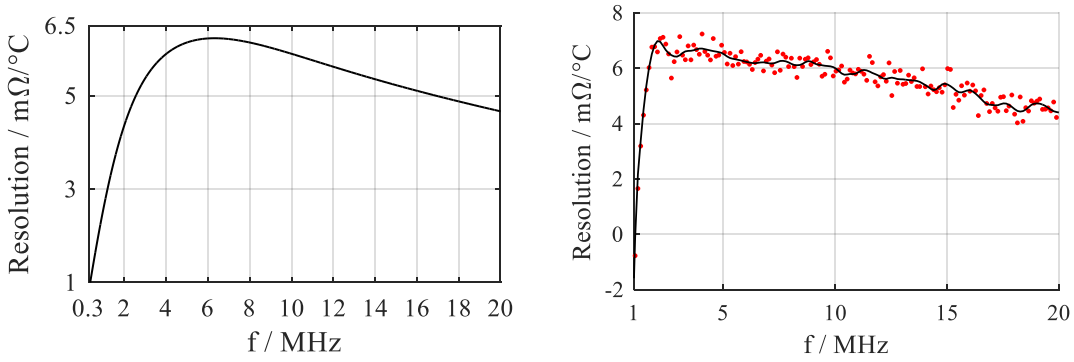


Figure 6.16 Resolution of the frequency response of Z_{GE} as a TSEP: (a) Resolution from simulation, (b) Resolution from the experimental test. Dots: Measured data points. Line: Interpolation of the measured data.

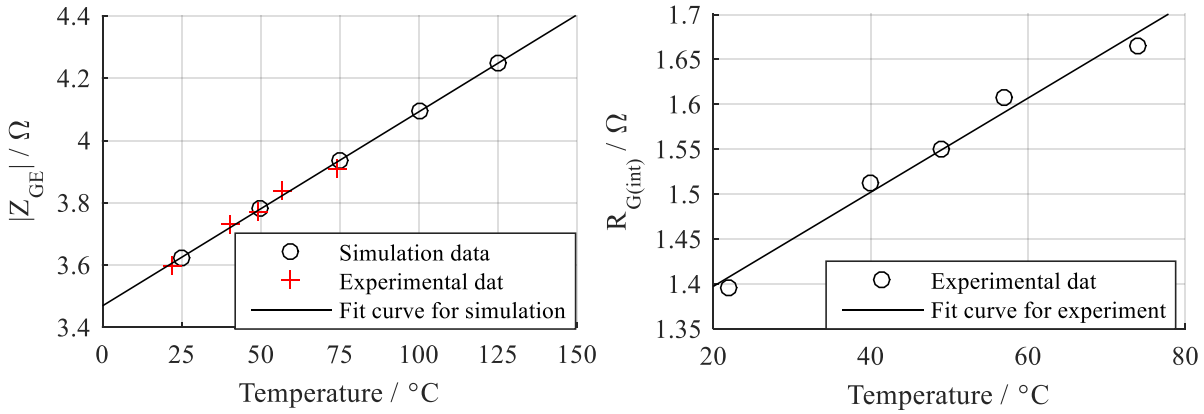


Figure 6.17 (a) Change of $|Z_{GE}|$ with T_{vj} at resonant point, (b) Variation of $R_{G(int\text{-}chip)}$ with T_{vj}.

Figure 6.17 depicts the change of $|Z_{GE}|$ at the resonant point against temperature. Simulation and experimental results match with each other. Results present that the sensitivity is approximately 6.1 mΩ/°C, which represents a practical value to be detected.

The equivalent internal gate resistance $R_{G(int\text{-}chip)}$ is also plotted against the temperature as shown in Figure 6.17b. The sensitivity of $R_{G(int\text{-}chip)}$ against T_{vj} is 5.2 mΩ/°C. The sensitivity is comparable to techniques proposed in other literatures. For example, in [47], the internal gate resistance was calculated from the peak gate current, the resolution is 0.9 mΩ/°C. In [49], a fixed high-frequency signal superimposed with the gate signal is injected into the gate, and the internal gate resistance is estimated from voltage and current measurements. The resolution is 3.5 mΩ/°C.

6.5.3. Bond wire lift-off analysis

Experimental tests under different bond wire lift-off conditions have also been carried out. Bond wires have been cut to imitate the degradation during general power cycling. Figure 6.18 and Figure 6.19 show the experimental results.

In these plots, the values in simulation are different from that in experimental tests. But their variations are similar. The imaginary part is illustrated in Figure 6.19. When there is bond wire lift-off, $Z_{GE(Imag)}$ rises. Whereas, the increment of T_{vj} will lead to decline in $Z_{GE(Imag)}$. $Z_{GE(Real)}$ is presented in Figure 6.18. $Z_{GE(Real)}$ will increase due to either bond wire lift-off or T_{vj} increment. The results confirm that the proposed technique is able to provide information for both T_{vj} and bond wire lift-off with only one test.

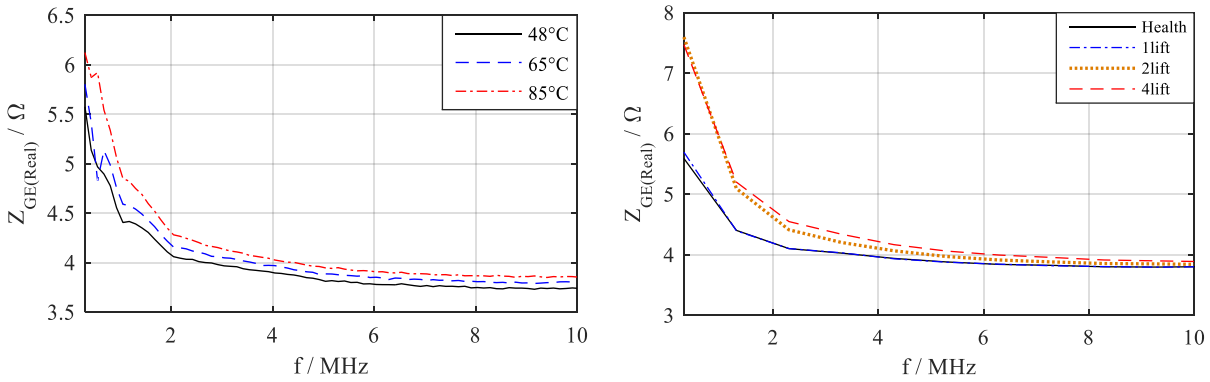


Figure 6.18 Experimental results for $Z_{GE(Real)}$: (a) Variation with T_{vj}, (b) Variation with bond wire lift-off @ 48°C.

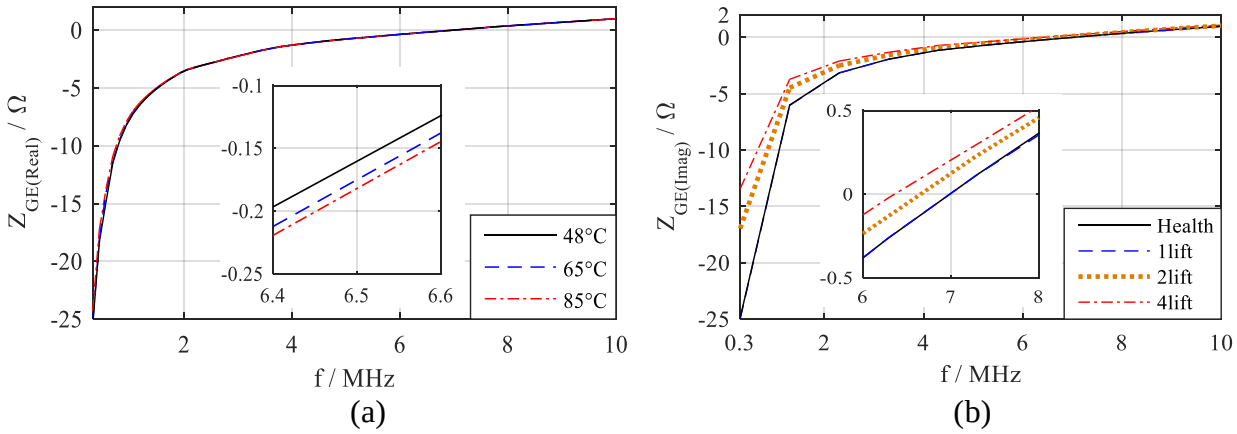


Figure 6.19 Experimental results: (a) Imaginary part $Z_{GE(Imag)}$ variation with T_{vj}, (b) Imaginary part $Z_{GE(Imag)}$ variation with bond wire lift-off @ 48°C.

6.5.4. Simultaneous identification procedure

Figure 6.20 illustrates the application of the proposed technique. A healthy module is tested to provide a reference table which is the baseline highlighted. The dashed line and the dotted line are the characteristic/failure criteria for the IGBT module upon bond wire failure.

The IGBT module ages while operating in the system. During maintenance stage, the aged module is tested. The profile of Z_{GE} is captured as shown in Figure 6.20. After that, the comparison is made between the present profile and the reference table. $Z_{GE(Imag)}$ is compared with the reference table to distinguish between temperature change and the bond wire failure. The failure criteria are defined with $Z_{GE(Imag)}$. When $Z_{GE(Imag)}$ of a module is equal to or less than the baseline value, the IGBT module is healthy. If $Z_{GE(Imag)}$ of a module is greater than the dashed line, it indicates there is bond wire failure in the IGBT module. Once the health condition is assured, $Z_{GE(Real)}$ is applied for T_{vj} estimation.

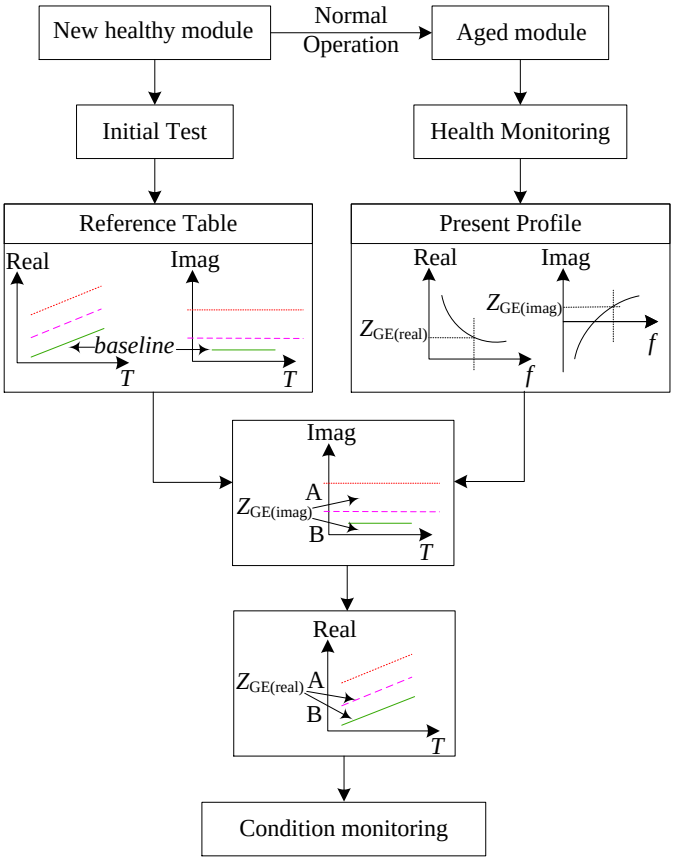


Figure 6.20 Application of the signal sweeping technique.

The experimental results are processed to demonstrate the procedure in Figure 6.20. According to simulation and experimental results, 6.5 MHz is chosen as a preferred frequency for the reference table. The impedance response at 6.5 MHz is displayed in Figure 6.21 as the reference table for identification. There are three horizontal lines in Figure 6.21a. The lines divide the figure into four sections corresponding to the healthy condition, one bond wire lift-off, two bond wire lift-offs and four bond wire lift-offs respectively. This is utilised to determine the health condition of the IGBT module. The baseline for the real part is depicted in Figure 6.21b. This is employed for T_{vj} estimation under different experimental conditions.

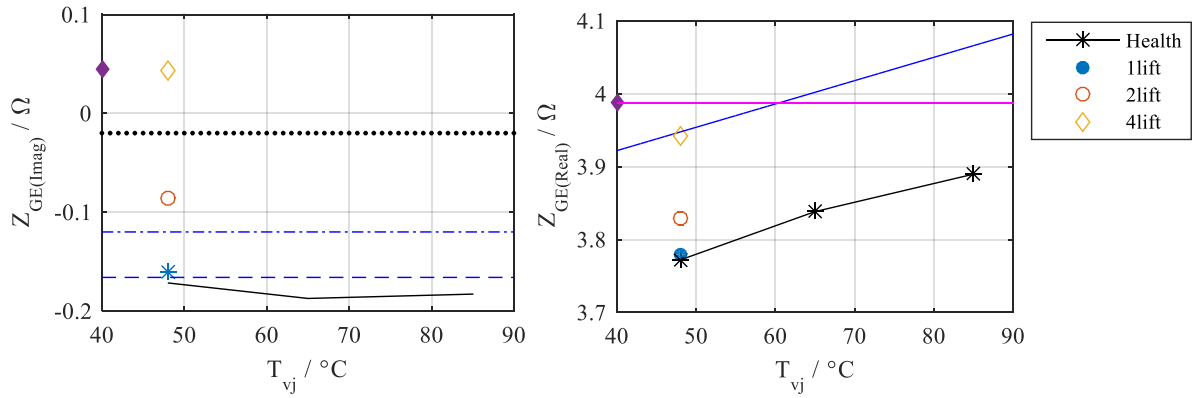


Figure 6.21 Reference table for identification: (a) Imaginary part $Z_{GE(Imag)}$, (b) Real part $Z_{GE(Real)}$.

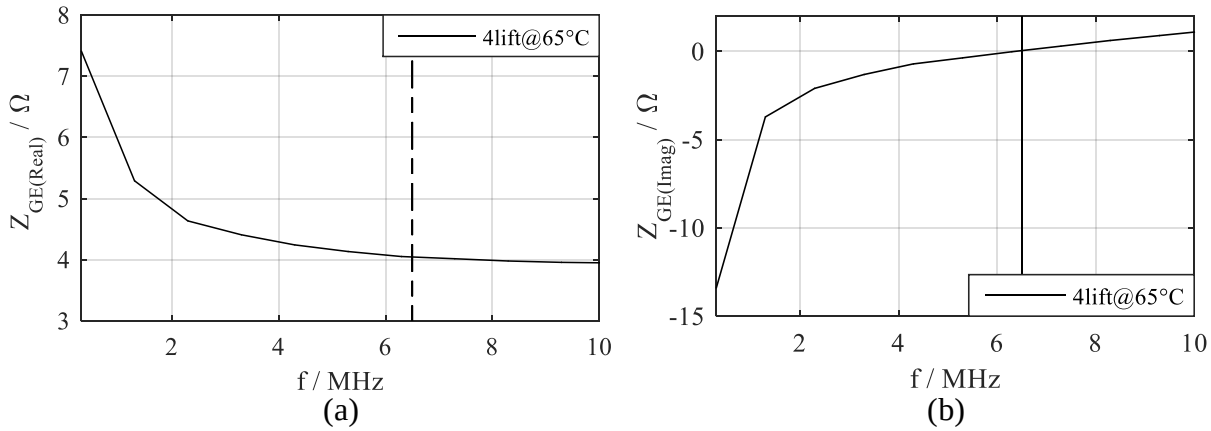


Figure 6.22 Experimental results for four bond wire lift-offs at 65°C: (a) Real part $Z_{GE(Real)}$, (b) Imaginary part $Z_{GE(Imag)}$.

Experimental results for four bond wire lift-offs at 65 °C are treated as the test profile during the maintenance stage. Figure 6.22 describes $Z_{GE(Real)}$ and $Z_{GE(Imag)}$ for four bond wire lift-offs at 65 °C. According to Figure 6.22, $Z_{GE(Real)}$ at 6.5 MHz is 4.0442 Ω. $Z_{GE(Imag)}$ at 6.5 MHz is 0.0451 Ω. These values are labelled with a filled diamond mark in Figure 6.21. The imaginary part is above the highest line in Figure 6.21a. Therefore, four bond wires are predicted to be lifted off in this condition. Afterwards, a reference line (the line which crosses over the empty diamond mark.) is generated as shown in Figure 6.21b which is the reference line for T_{vj} estimation at four bond wire lift-offs. According to the reference line, the estimated T_{vj} is 60.6°C, which is close to 65°C with an acceptable difference.

This demonstration shows that the proposed approach can be employed for monitoring bond wire state and junction temperature estimation simultaneously. In this technique, $Z_{GE(Imag)}$ can be used to determine the bond wire state and based on this information, T_{vj} can be predicted by $Z_{GE(Real)}$.

6.5.5. Major implication cost

Major components are suggested in Table 6.4 for the implication of the signal sweeping technique. In this approach, the sweep signal will be generated by the EVAL Board for CN0304 and the controller EVAL-SDP-CS1Z. The frequency of the signal can go up to 37.5MHz which is sufficient for bond wire lift-off detection and temperature estimation. The injected signal is coupled into the gate drive signal with the telecom transformer. The F28379D DELFINO experimenter kit supports to acquire the response signal. The EVAL-ADUM4160EBZ help to prevent the contamination of the generated signal. The major cost of the lab implementation is about £400. This cost can be reduced when it is commercialized. Besides, the developed device can be shared between IGBTs in the same power converter.

Table 6.4 Major components and their price

Component	Specifications	Price
Telecom Transformer	1:1 Through Hole Telecom Transformer, 2.5mH	£5.04
EVAL-ADUM4160EBZ	USB Isolator, Evaluation Board	£70.91
EVAL BOARD FOR CN0304	Signal generator	£73.51
EVAL-SDP-CS1Z	controller for signal generator	£42.29
F28379D DELFINO EXPERIMENTER KIT	16bit ADC included and control	£191.16

6.6. **Summary**

An online applicable health monitoring technique is proposed in this chapter. The technique relied upon the injection of sweep signals to the gate-emitter circuit of the IGBT module. The presented approach can decouple the influence of T_{vj} and the bond wire lift-off. A small signal model is extracted for the IGBT module and simulation is carried out in SaberRD. Experimental tests have also been implemented with the IGBT module under different operation conditions including the variation from T_{vj} and the bond wire status. Both simulation and experimental results verify the effectiveness of the proposed approach. In the final section of the chapter, an example is presented to demonstrate the operation procedure of the health monitoring technique.

Chapter 7. Conclusions and future work

This chapter summarizes the work in the thesis followed by the suggestions for future work.

7.1. **Conclusion**

Condition monitoring techniques are of paramount importance for IGBT power module based applications, such as renewable energy power system. The research outcome in this thesis can be divided into three aspects, T_{vj} estimation in mIGBTs, the offline health monitoring technique and the online applicable health monitoring technique.

- T_{vj} estimation in mIGBTs

The measurement of T_{vj} in mIGBTs is more challenging compared with that in single chip IGBT module. The intrinsic nature of multi-chip geometry leads to spatial distribution of temperature in mIGBTs. Power cycling tests were carried out to evaluate spatial distribution of temperature and results are described in Chapter 3. For the evaluation, temperature distributions within individual chip and between chips were recorded at different load profiles. Results depict significant temperature distributions in both chip level and switch level. 6 - 60 °C temperature variations were captured within individual chip and 2 - 10 °C amongst different chips. The information gained from this research work is used to investigate the accuracy of TSEPs applied to mIGBTs. Results suggest that dV_{CE}/dt, $V_{CE(peak)}$ and $I_{C(tail)}$ are not suitable TSEPs. $V_{CE(on\text{-}sense)}$ is more immune the SDoT while $V_{CE(on\text{-}load)}$ are prone to error in the case of thermal disequilibrium.

The work presented in Chapter 3 investigates the T_{vj} estimation in mIGBTs. In general, techniques used for bond wire lift-off is influenced by T_{vj}. Therefore, T_{vj} investigation is prerequisite for both online and offline bond wire lift-off detection.

- An offline bond wire lift-off monitoring technique

An offline bond wire lift-off technique is proposed in Chapter 4 aimed to assist the health condition monitoring of mIGBT PMs during the maintenance stage. The method can not only predict the number of bond wire failures but also locate the lifted bond wires. The location of the lifted bond wires is unique and has not been reported in previous publications. Furthermore,

the method shows outstanding performance regarding the earlier stage failure detection which is appealing to critical applications like offshore wind farm. The new method was verified in simulation and experimental test. The technique has also been applied to mIGBT modules with different geometry. Test results show that the proposed technique can be applied to mIGBT with popular packages. A CMU prototype has been constructed to demonstrate the proposed technique in the field. The CMU is a standalone device powered a battery and the circuit can be used as a prototype for future mass manufacturing.

- An online applicable condition monitoring technique

This study has proposed a new measurement technique which can decouple the influence of bond wire lift-off and T_{vj}. The proposed technique helps to extract information of T_{vj} and bond wire state simultaneously with only one measurement. The technique is carried out with a network analyser which injects sweep signals across the gate and emitter terminals of an unbiased IGBT module. Besides interpreting the absolute value of the impedance, this work investigates $Z_{GE(Real)}$ and $Z_{GE(Imag)}$ as well. In the proposed technique, $Z_{GE(Imag)}$ is utilised to distinguish between T_{vj} and bond wire lift-off. Based on this information, T_{vj} is then predicted by $Z_{GE(Real)}$. The identification procedure is illustrated with a validation test. The technique provides the correct number of lifted bond wires. There is about 4.4°C deviation in T_{vj} estimation. The identification result confirms the effectiveness of the proposed approach.

It is important to point out that sweep signal is injected during the off state of the IGBT when applied online. Consequently, the method will not be influenced by I_C as there is no current flowing through the device. Likewise, V_{CE} is constant. Therefore, the method is not influenced by V_{CE}.

Finally, it is emphasized that the conclusions are validate on the IGBT types researched and should not be generalized on other IGBT types without confirmation.

7.2. **Future work**

Based on the research conducted so far, there are several potential areas recommended for further research. They are listed as follows.

- SDoT and T_{vj} perdition

Investigation about SDoT and T_{vj} estimation should be expanded to Wide Band Gap (WBG) devices such as SiC mIGBT/MOSFET as well as press-pack IGBT modules. Regarding the estimation of T_{vj} in mIGBT, on the one hand, it is essential to study how to complement TSEPs so that they can predict accurate T_{vj}, on the other hand, it is beneficial to explore alternative techniques. Furthermore, the impact of SDoT on the estimation of thermal degradation shall be identified.

- Offline HMU

In order to get the HMU prototype closer to a commercial product the accuracy of the HMU measurement should be improved. In addition, the technique developed in this thesis can be extended to how to apply the proposed offline system for online/in-situ applications. In the future, condition monitoring-oriented layout design of IGBT module should be promoted. The condition monitoring concept should also be included during package or layout design. Considering the interaction of various ageing mechanisms, the tailored design will improve the accuracy of the condition monitoring technique and finally the reliability of the IGBT module.

- Signal sweeping technique

The signal sweeping technique can be integrated into the gate driver and tested in a converter. The technique can be demonstrated in a real-time application and it can also be applied to WBG devices. More test can be carried out on power modules with different packages and IGBT chip types to investigate the suitability for universal applications.

In addition, the characteristics of the IGBT module at low frequency, for example lower than 5MHz, should be examined. Characteristics in this frequency range may be able to give an insight about the physical process of the devices. This can then be potentially applied to detect the defected products in the manufacture side.

Finally, modified control approach or switch pattern of the power converter can be developed to imitate the signal sweeping technique. This can be further combined with the system identification concept for advanced condition monitoring.

A. Appendix Overview

Table A. 1 compares the temperature sensors according to their material, response time as well as their sensitivity.

Table A. 1 Summary of temperature sensors

		Sensitive material	Response time	Sensitivity
Thermistor		Ceramic	3 s - 20 s	100 -10 k Ω/°C
RTD sensor		Conductor	5 s -10 s	< 1 Ω / °C
Semiconductor	Diode	Semiconductor	Nearly real time	2 mV / °C
sensor	CMOS	Semiconductor	Depends,1 s - 5 s	2 mV / °C
Optical sensor		Optical fiber	< 0.5 ms	Not known

Figure A. 1 illustrates two models for each branch in Cauer model, L model and T model the [13]. Since there are two resistors in the same value to represent the thermal resistance on both sides, this structure allows the model to represent the temperature in the centre of any particular layer. However, the first layer and the bottom layer are different, since a step change of the input power will not lead to a step change of temperature in practice, and it is the same with the bottom layer. Therefore, a capacitor is used. Thermal models for mIGBT are more complicated because of the sophisticated thermal conduction and thermal coupling among the IGBT chips.

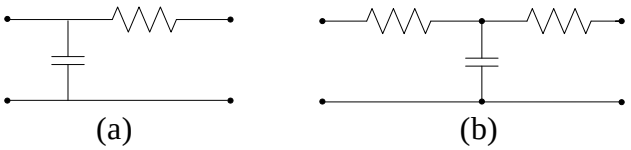


Figure A. 1 Thermal model[13]: (a) L model, (b) T model.

B. Appendix TSEPs for multichip IGBT

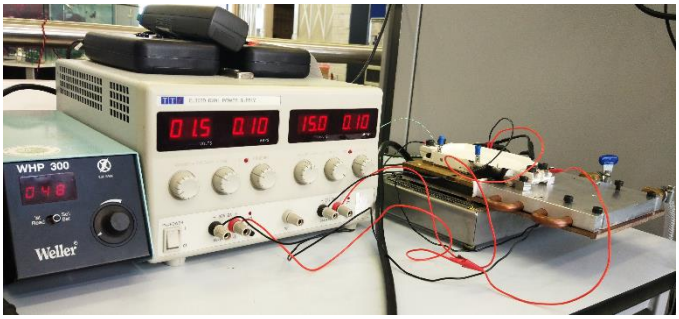
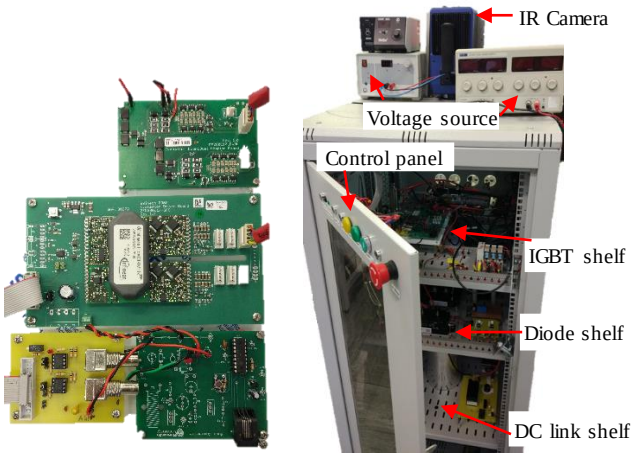


Figure B. 1 Set-up for $V_{CE(on\_sense)}$ measurement.



(a) (b)

Figure B. 2 (a) Gate driver, (b) Double pulse test platform.

The IR camera shown in Figure B. 2b is SC5500/SC7500 MWBB. The camera serial is 211054. The lens name used is L0106 whose focal length is 50mm. The frame rate is 190Hz. The integration time is 0.25 ms. The temperature range is 5 °C – 300 °C.

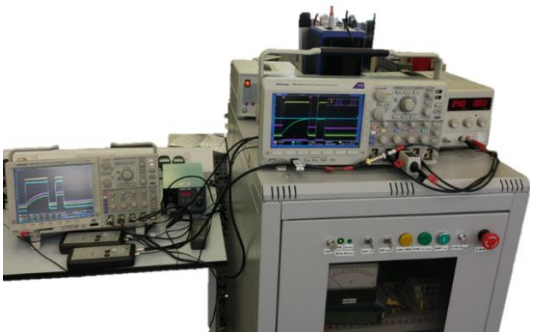


Figure B. 3 Ongoing test.

Figure B. 4 illustrates how the IGBT chip current is measured with the Rogowsky coil. A miniature coil is used so that all the emitter bond wires of one chip can go through the coil.

Figure B. 4 Chip current measurement with Rogowsky coil.

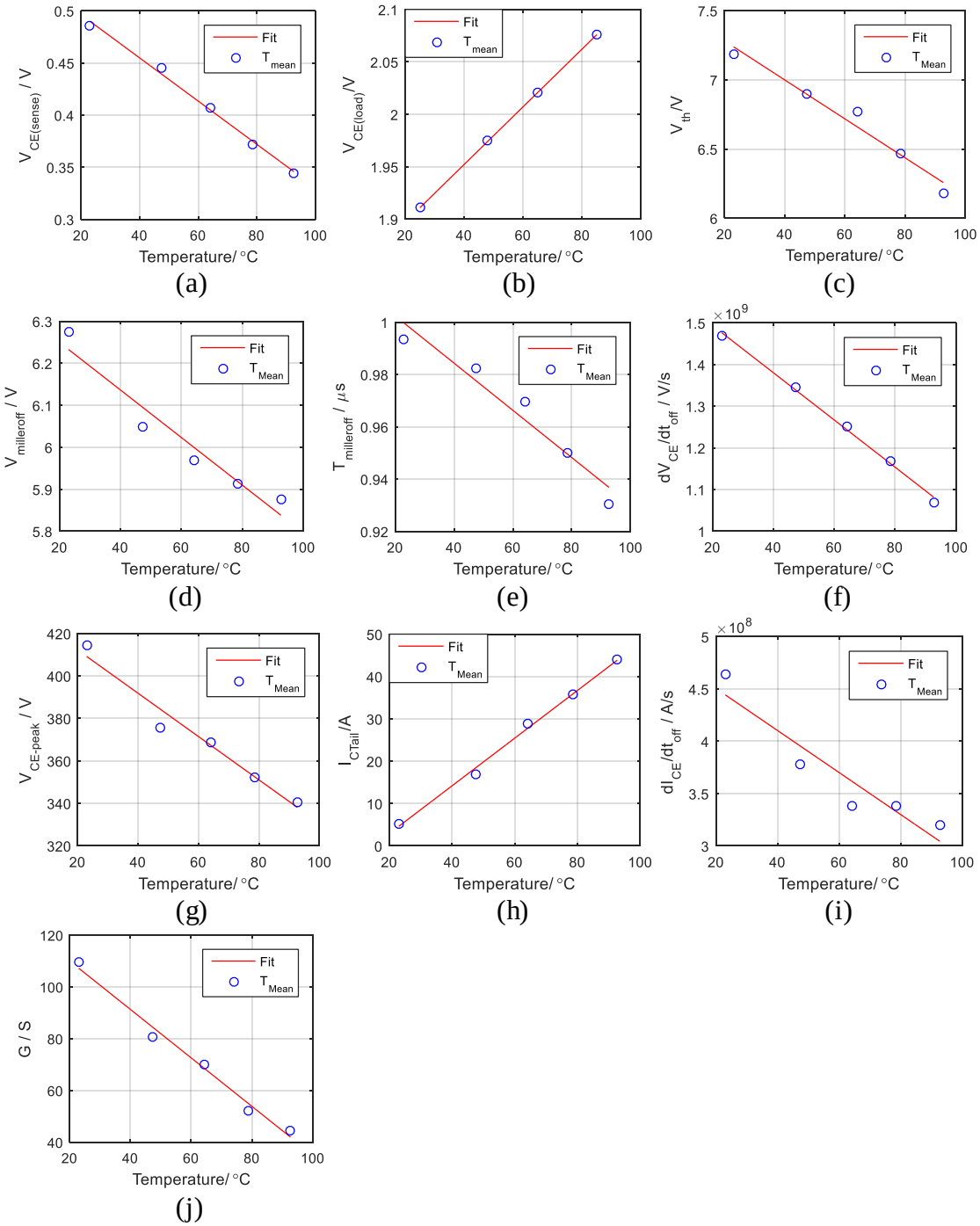


Figure B. 5 TSEPs at HTD condition: (a) $V_{CE(on\text{-}sense)}$, (b) $V_{CE(on\text{-}load)}$, (c) V_{th}, (d) V_{Miller}, (e) T_{Miller}, (f) dV_{CE}/dt, (g) Overshoot voltage during turn-off $V_{CE(peak)}$, (h) dI_C/dt, (i) Tail current $I_{C(tail)}$, (j) Trans-conductance g_m.

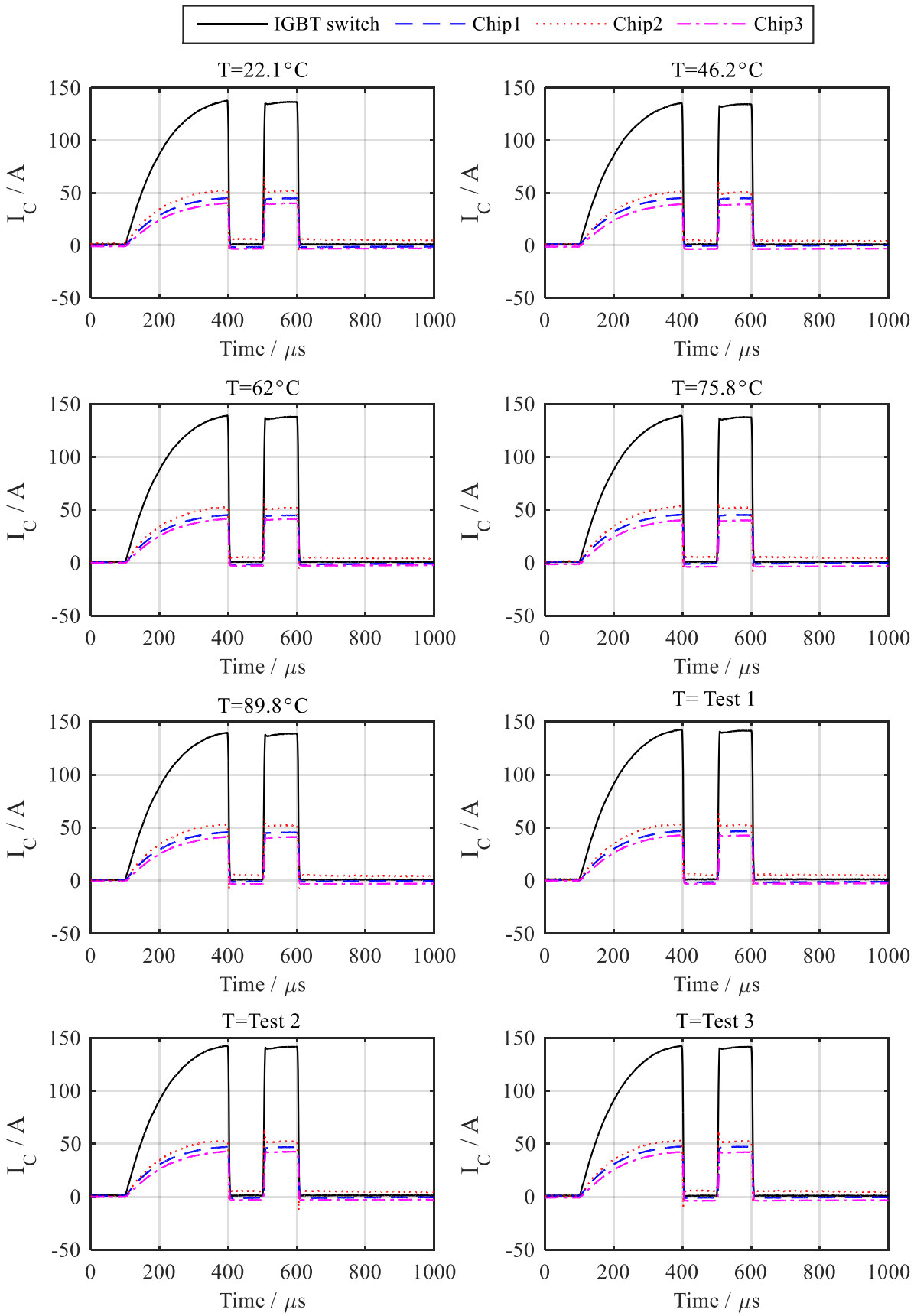


Figure B. 6 Current distribution of HTD tests and ITD tests.

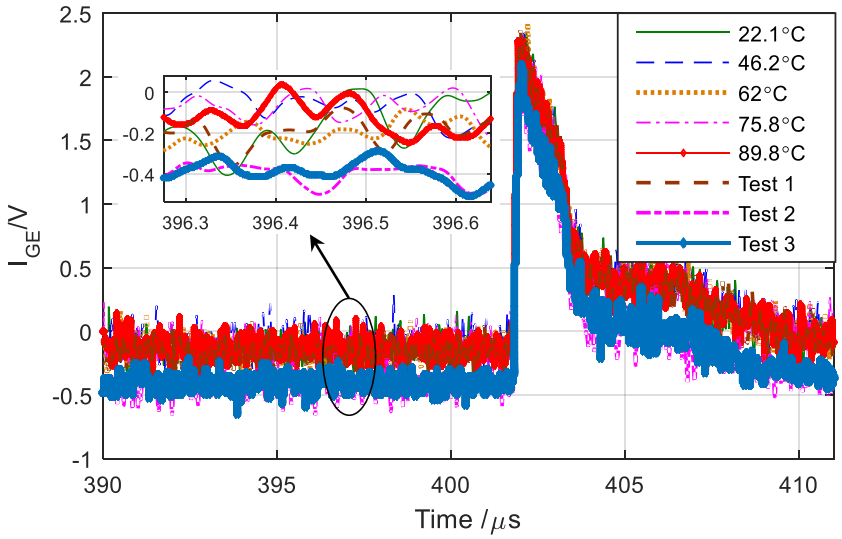


Figure B. 7 Shifts in I_{GE} during the turn-on transient.

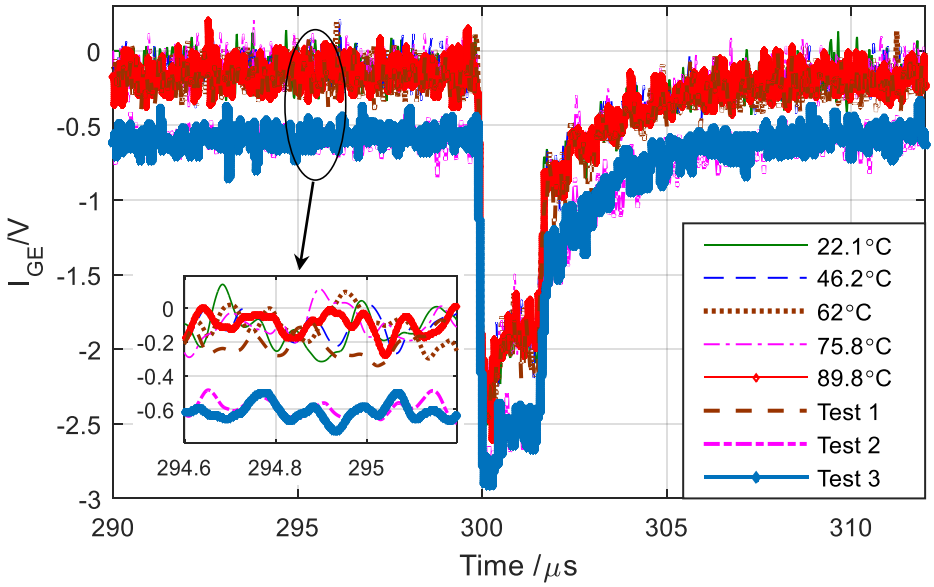


Figure B. 8 Shifts in I_{GE} during the turn-off transient.

Figure B. 7 and Figure B. 8 show shifts in the gate current. The gate current is continuously shifting towards the negative direction. This can be caused by the current circulation of the emitter side. The TSEPs which takes advantage of the peak gate current will not be applicable for T_{vj} estimation because of the shift. More research on this part should be carried out in the future.

C. Appendix Fault diagnosis with on-state voltages

Additional results are added in this section to support the research work.

The temperature dependency of the on-state voltage $V_{CE(on)}$ is tested for the Infineon FF600R17ME4 module as shown in Figure C. 1. The temperature coefficient of $V_{CE(on)}$ peaks at I_C = 100 mA and it is about 2.6 mV/°C. The inflexion point is at about I_C = 100 A, the temperature coefficient is less than 0.2 mV/°C. After the inflexion, the temperature coefficient climbs again with the rise of the current and reaches about 1.6 mV/°C at I_C = 240A.

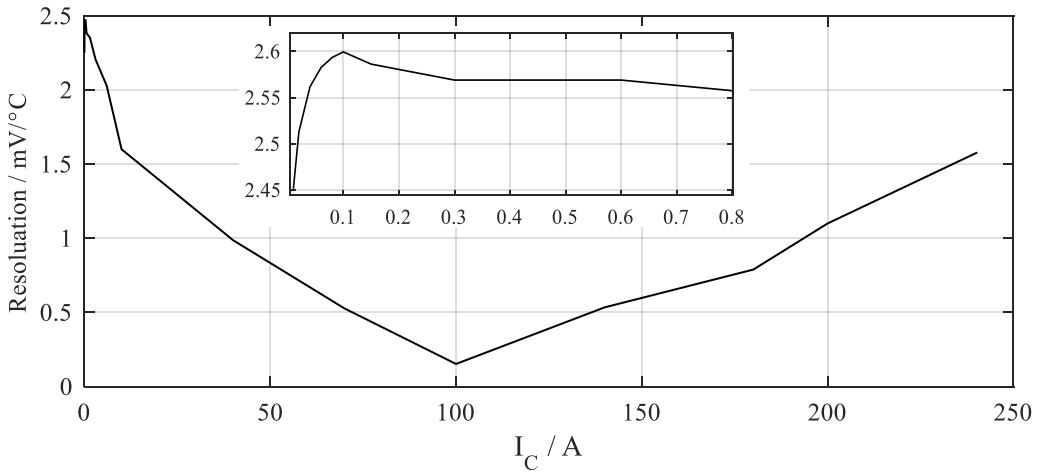


Figure C. 1 Variation of temperature coefficient against collector current.

Figure C. 2 - Figure C. 12 are the current redistribution analysis for bond wire failures in Chip2 and Chip3. Overall, the current share of one chip decreases when there is bond wire failure in this chip. Moreover, the current share of other chips increases. Furthermore, the current share does not show any dependency on temperature.

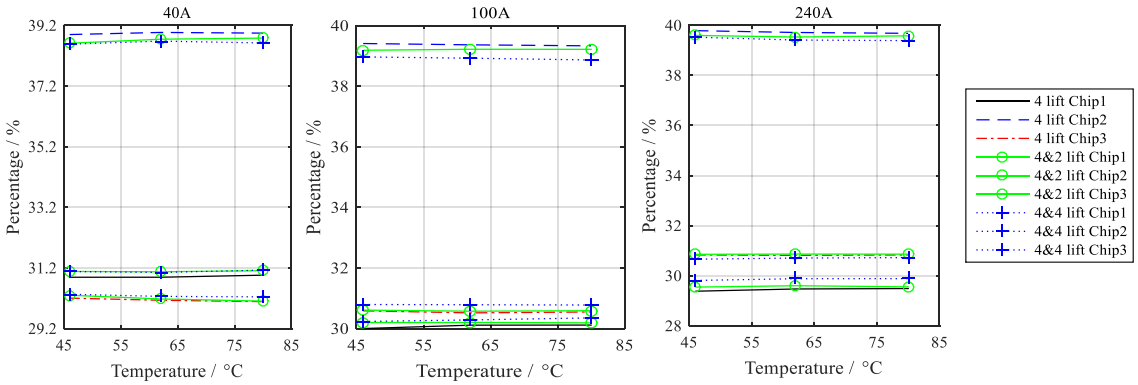


Figure C. 2 Current share upon bond wire lift-off in Chip1 and Chip2.

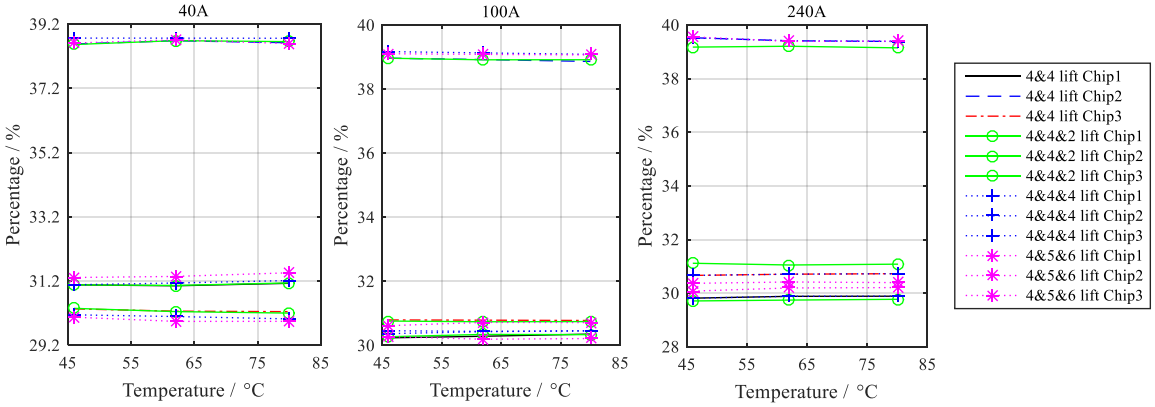


Figure C. 3 Current share upon bond wire lift-off in Chip1, Chip2 and Chip3.

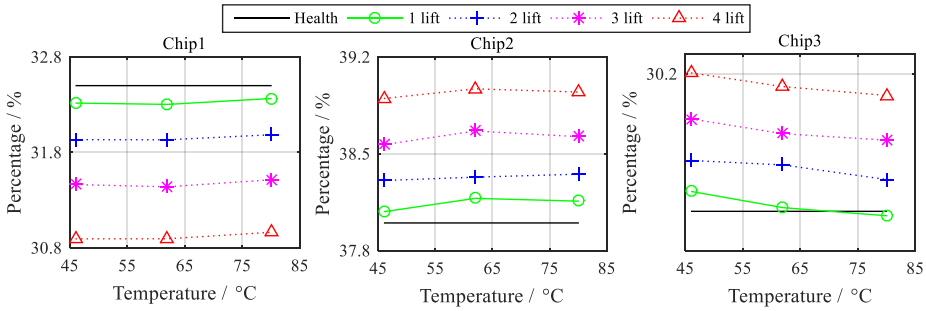


Figure C. 4 Current distribution upon bond wire lift-off in Chip1 at I_C = 40 A.

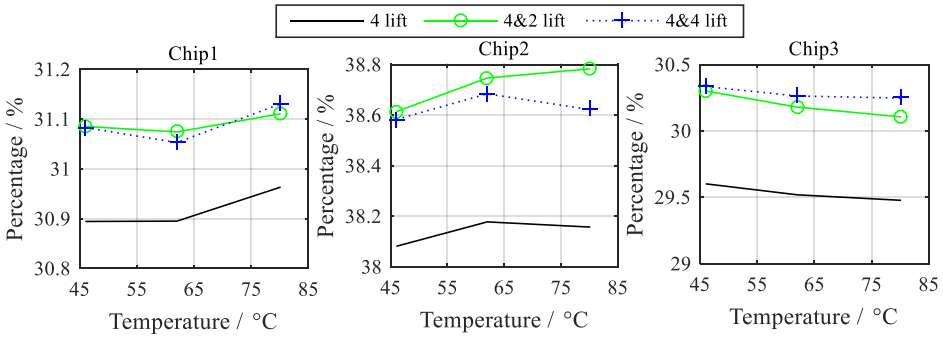


Figure C. 5 Current distribution upon bond wire lift-off in Chip1 and Chip2 at I_C = 40 A.

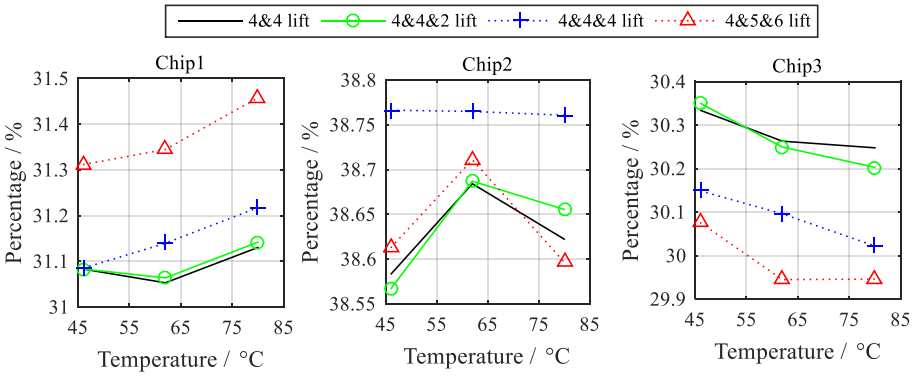


Figure C. 6 Current distribution upon bond wire lift-off in Chip1, Chip2 and Chip3 at I_C = 40 A.

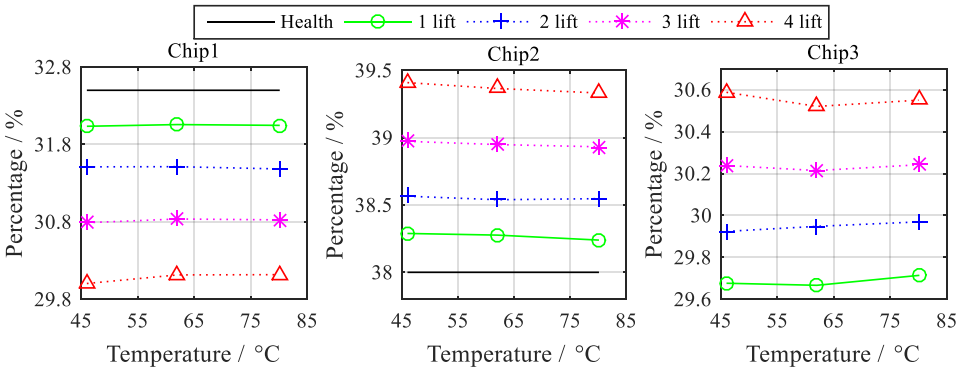


Figure C. 7 Current distribution upon bond wire lift-off in Chip1 at I_C = 100 A.

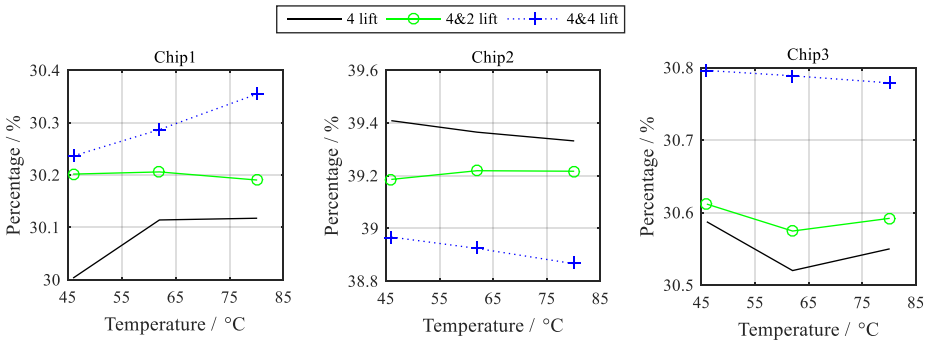


Figure C. 8 Current distribution upon bond wire lift-off in Chip1 and Chip2 at I_C = 100 A.

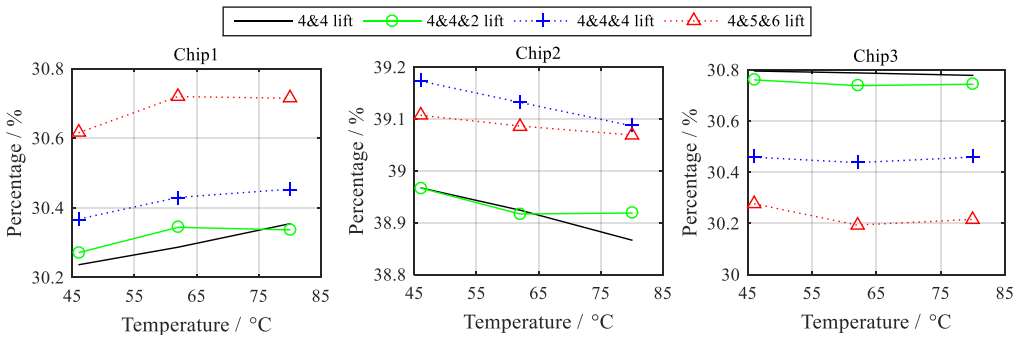


Figure C. 9 Current distribution upon bond wire lift-off in all three chips at I_C = 100 A.

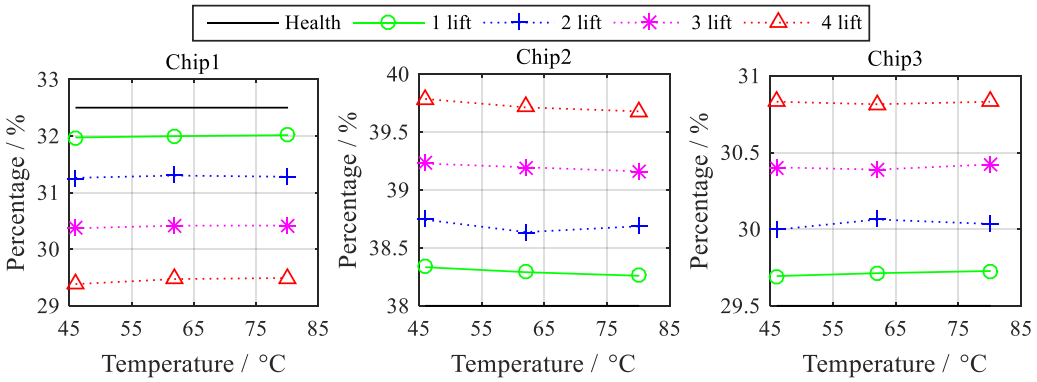


Figure C. 10 Current distribution upon bond wire lift-off in Chip1 at I_C = 240 A.

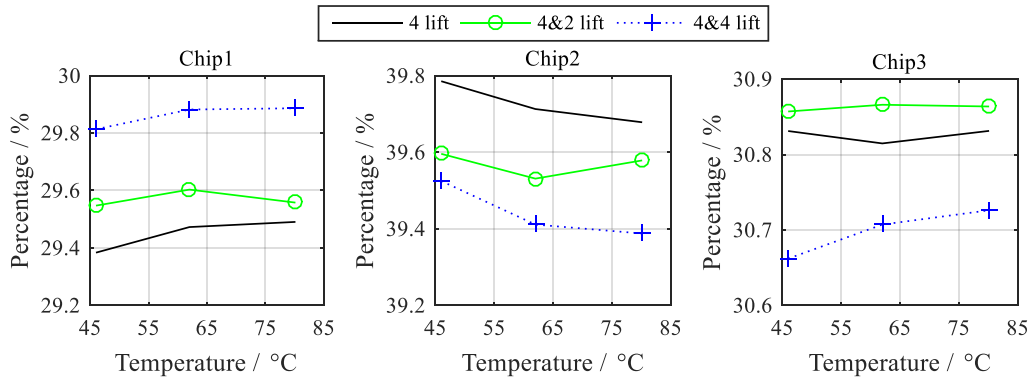


Figure C. 11 Current distribution upon bond wire lift-off in Chip1 and Chip2 at I_C = 240 A.

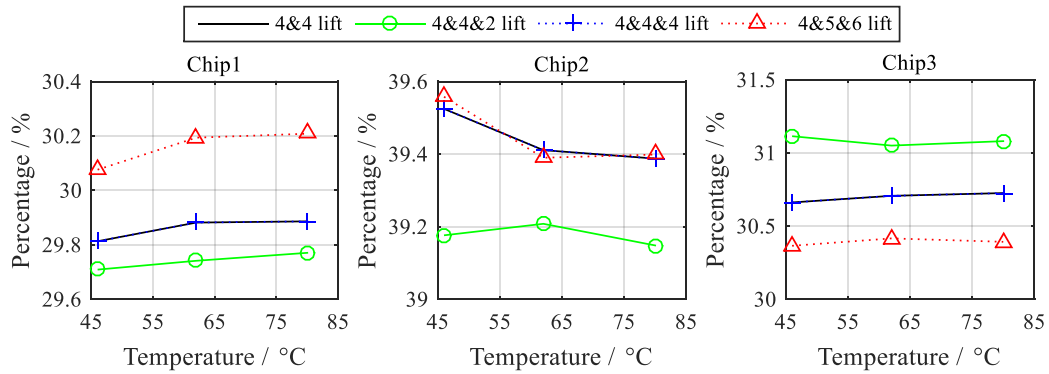


Figure C. 12 Current distribution upon bond wire lift-off in all three chips at I_C = 240 A.

Figure C. 13 - Figure C. 18 illustrate the temperature change upon bond wire lift-off in Chip2 and Chip3. ΔT_{max} and ΔT_{avg} at different failure conditions are presented as well as the temperature distribution amongst the three IGBT chips. In conclusion, even though the temperature deviation rises with the current increment, it does not show any dependency on the bond wire lift-off. This is due to the narrow current pulse and the current redistribution.

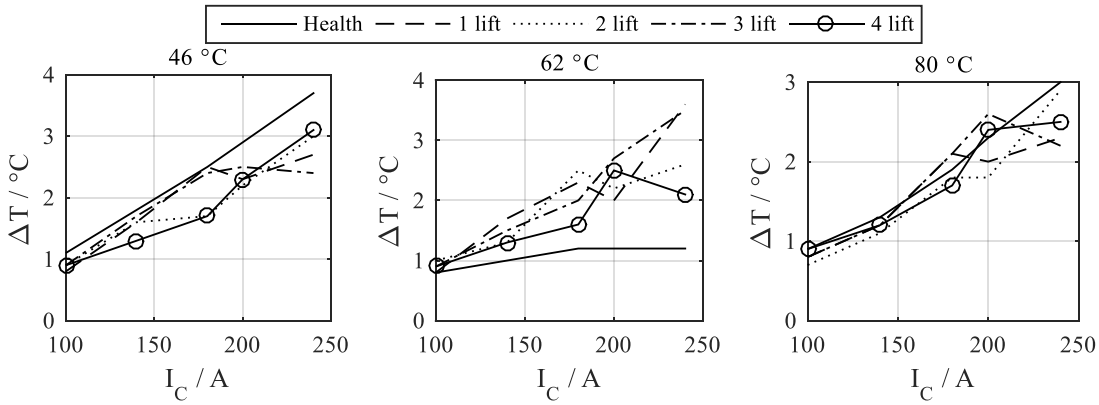


Figure C. 13 ΔT_{max} of Chip2 upon bond wire lift-off.

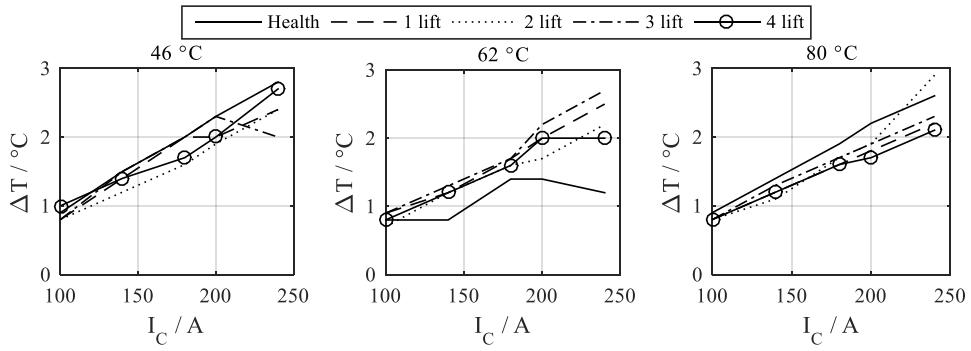


Figure C. 14 Maximum temperature change of Chip3 upon bond wire lift-off.

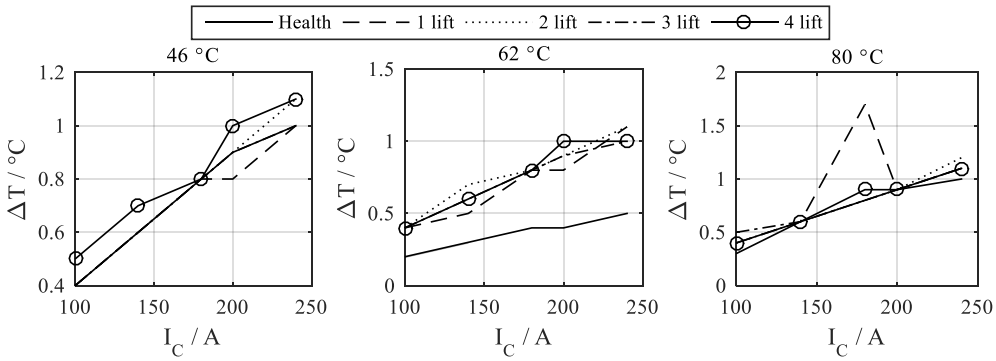


Figure C. 15 Average temperature change of Chip2 upon bond wire lift-off.

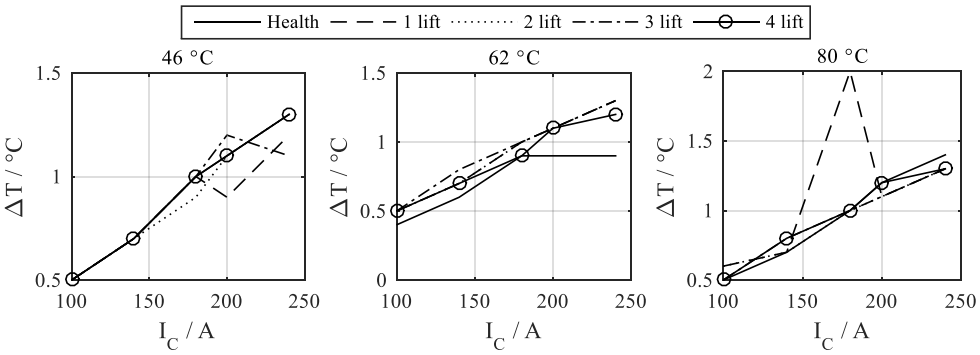


Figure C. 16 Average temperature change of Chip3 upon bond wire lift-off.

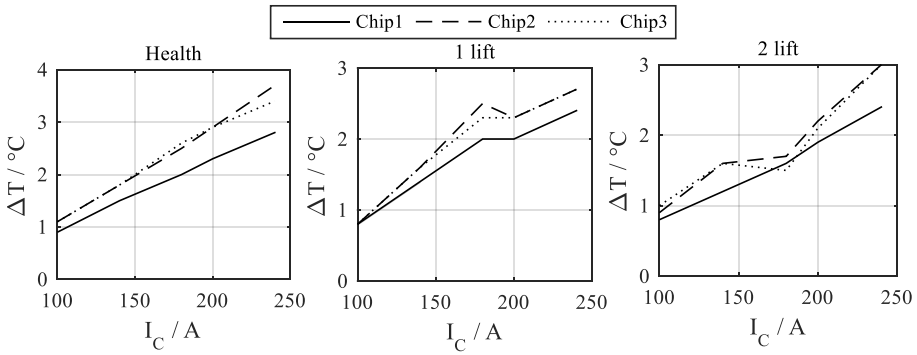


Figure C. 17 Distribution of ΔT_{max} amongst the three chips.

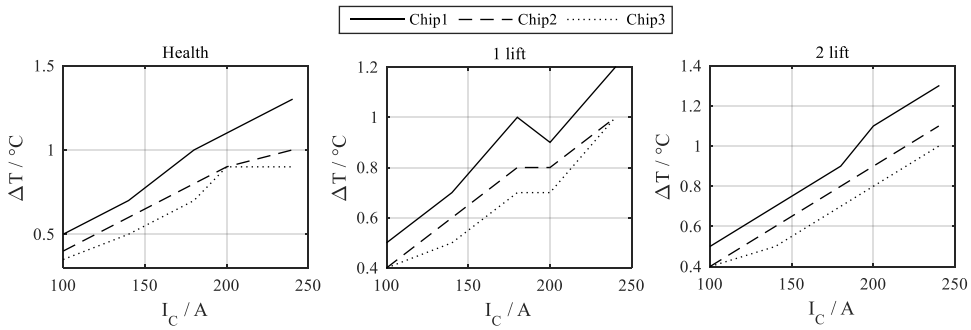


Figure C. 18 Distribution of ΔT_{avg} amongst the three chips.

Simulation has been done for the Dynex module in SaberRD. The schematic of the simulation model is shown in Figure C. 19 which is built according to Figure 4.1.

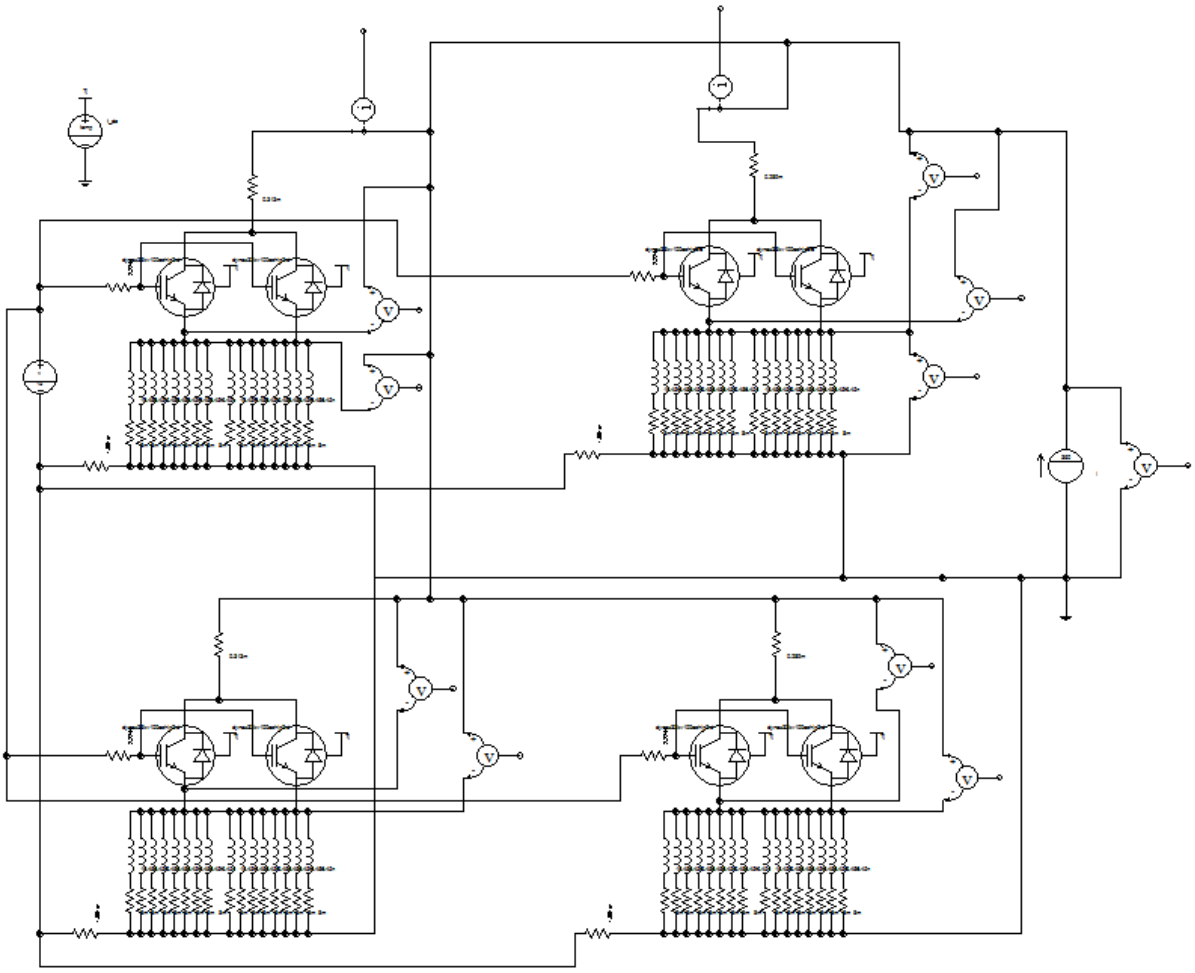


Figure C. 19 Schematic of the simulation for DIM400NSM33-F000.

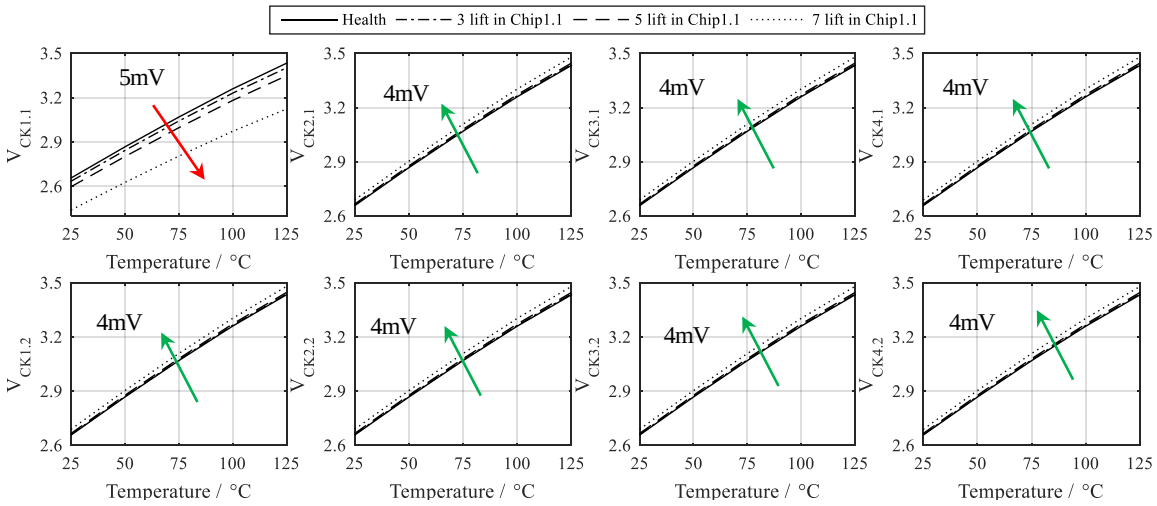


Figure C. 20 Simulation results at chip level: On-state voltage change upon bond wire lift-off in Chip1.1 at I_C = 360 A.

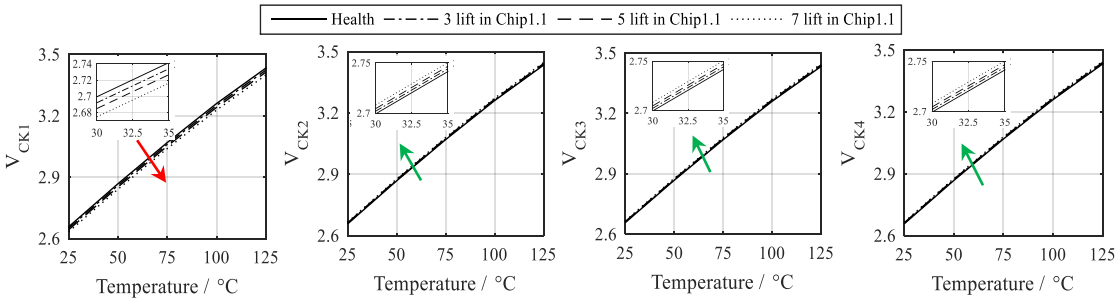


Figure C. 21 Simulation results at section level: On-state voltage change upon bond wire lift-off in Chip1.1 at I_C = 360 A.

Simulation results for bond wire lift-off in IGBT chip1.1. 3, 5 and 7 bond wires are lifted out of 64 bond wires. All other chips are healthy. Figure C. 20 presents the on-state voltage of each IGBT chip. There is a 5mV drop in $V_{CK1.1}$ upon the first three bond wire lift-off and the $V_{CK(on)}$ of all the other chips rises. The change of V_{CK} of each section is shown in Figure C. 21. V_{CK1} drops about 8mV upon the first three bond wire failure and the V_{CK} of the other sections increases about 3mV. Overall, the on-state voltage of the failed chip and failure section behaves similarly.

The Dynex module under test is displayed in Figure C. 22. The IGBT is painted with black Matt paint for thermal analysis. Figure C. 22 shows the thermal profile of one DBC tile in the IGBT module. Figure C. 22a is the thermal profile at the beginning of the current pulse. And Figure C. 22b is the thermal profile at the end of the current pulse. There is about 7 °C variation in the maximum temperature due to the high current injection.

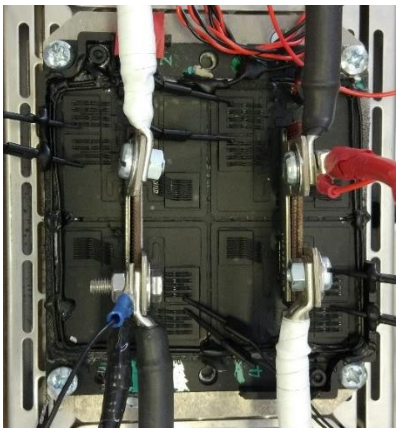
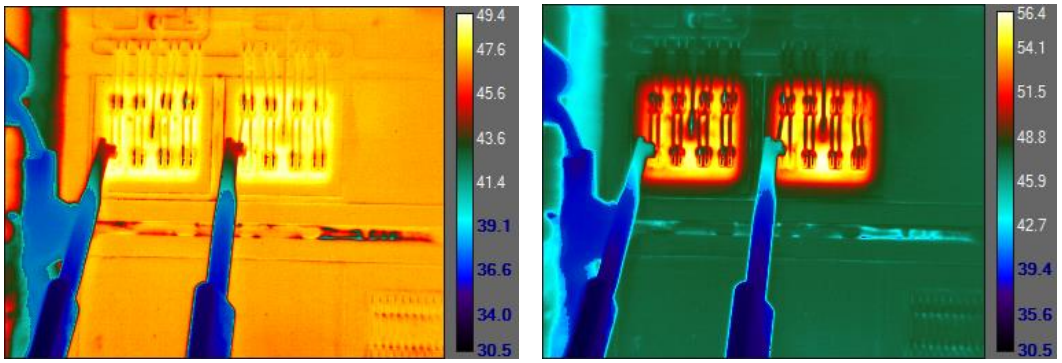


Figure C. 22 The Dynex module under test.



(a) (b)

Figure C. 23 Thermal profile of section 1 in the IGBT module at 320A: (a) At the beginning of the current pulse, (b) At the end of the current pulse.

The output characteristic of the Dynex module has been measured. The temperature sensitivity of the on-state voltage is described in Figure C. 24. Below the inflexion point, the best resolution is 2.6 mV/ºC at I_C = 20 mA. After that, the resolution increases with the current rise and reaches the peak of 6.646 mV/ºC at 320 A.

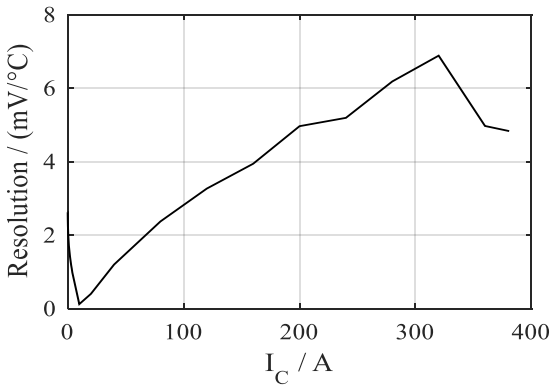
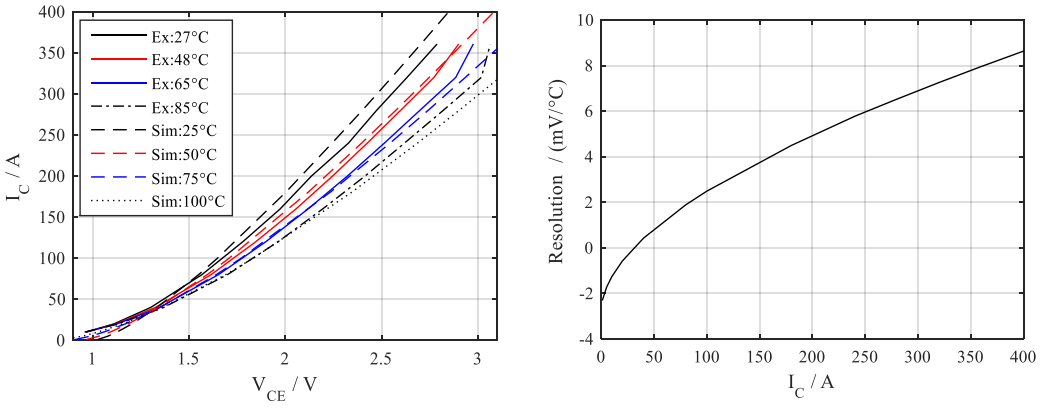


Figure C. 24 Resolution of the on-state voltage as a TSEP.

Figure C. 25a is the comparison of the on-state characteristic between the simulation results and the experimental test. The simulation results match with the experimental tests. It verifies the effectiveness of the simulation model. According to the temperature sensitivity of $V_{CE(on)}$ in Figure C. 25b, the inflexion point is at $I_C \approx 30$ A for the simulation model. In conclusion, the simulation model can reflect the on-state characteristic of the IGBT module.



(a) (b)

Figure C. 25 (a) Comparison of the output characteristic between the simulation and experimental results. (b) Resolution of the on-state voltage as a TSEP in the simulation.

Figure C. 26 and Figure C. 27 are the experimental results for the test on the Dynex module. The results illustrate the change of the on-state voltage upon the bond wire failures in IGBT chip2.1, IGBT chip3.1 and IGBT chip4.1. Overall, the on-state voltage of the IGBT chip/section decreases when there is bond wire failure in the corresponding chip/section. Moreover, the on-state voltage rises on the other chips/sections. This phenomenon can then be utilised for bond wire state estimation and failure location.

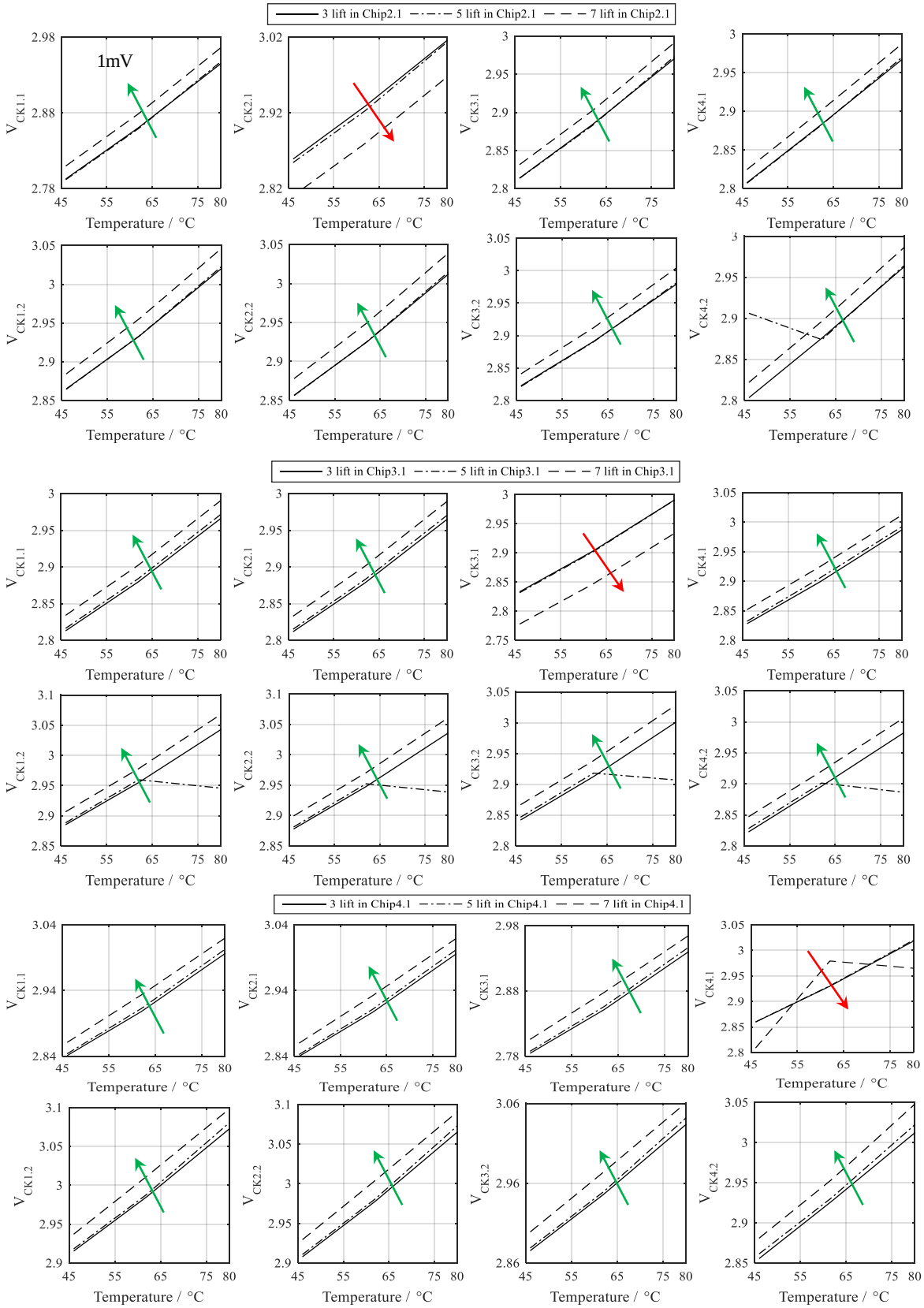


Figure C. 26 Experiment results for Dynex module at chip level: on-state voltage change upon bond wire lift-off in Chip2.1, Chip3.1 and Chip4.1.

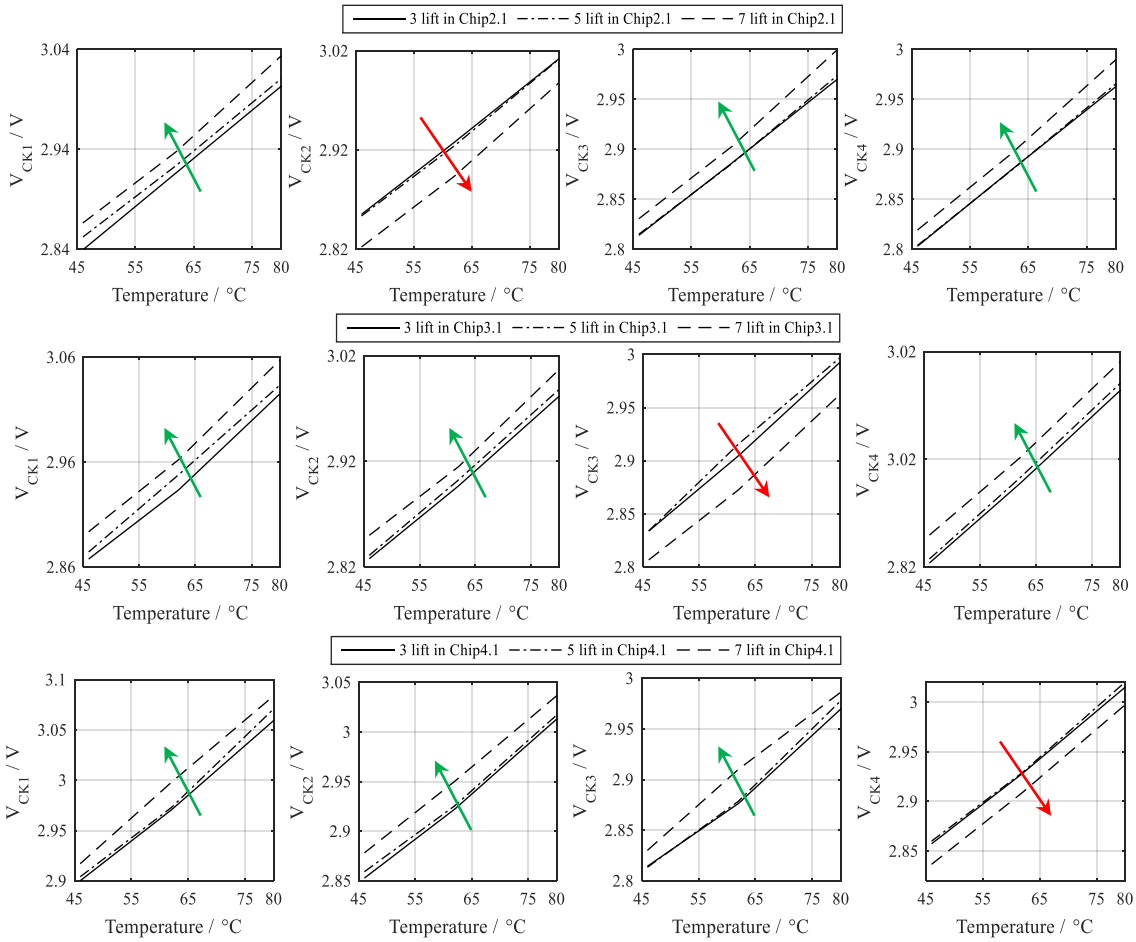


Figure C. 27 Experiment results for Dynex module at section level: On-state voltage change upon bond wire lift-off in Chip2.1, Chip3.1 and Chip4.1.

D. Appendix Health Monitoring Unit

The other components used in the circuitry.

Table D. 1 List of components used in the HMU

Function	Components ordered	Characteristics
Battery	Yuasa NP24-12I 12V Lead Acid Battery, 24Ah	About 100 min discharge time at 10A
Control board	TMDSDOCK28379D - Experimenter kit C2000 Delfino™ TMS320F28379D MCU	Integrated AD sampling Flexible connection
Voltage source	JTK3024D15 from XP Power NCS12 12W from Murata Power Solutions	Output: ± 15 V / 1 A Output: 5 V / 2.4 A
Current sensor	LEM LAH Series Closed Loop Current Sensor	Nominal Current:100A Bandwidth: DC to 200 kHz Accuracy: ±0.25 %
Fuse	Semiconductor fuse 125A, 30A, 20 A	Ultra-rapid protection
Circuit breaker	W68-X2Q110-25V from TE Connectivity Potter & Brumfield Relays	Current rating: 25A AC voltage rating: 415V

E. Appendix Signal sweeping technique

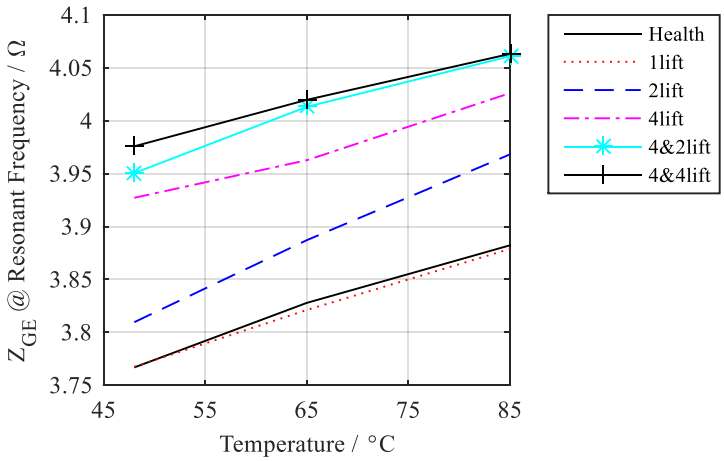


Figure E. 1 Experimental results of $|Z_{GE}|$ at the resonant point for T_{vj} estimation.

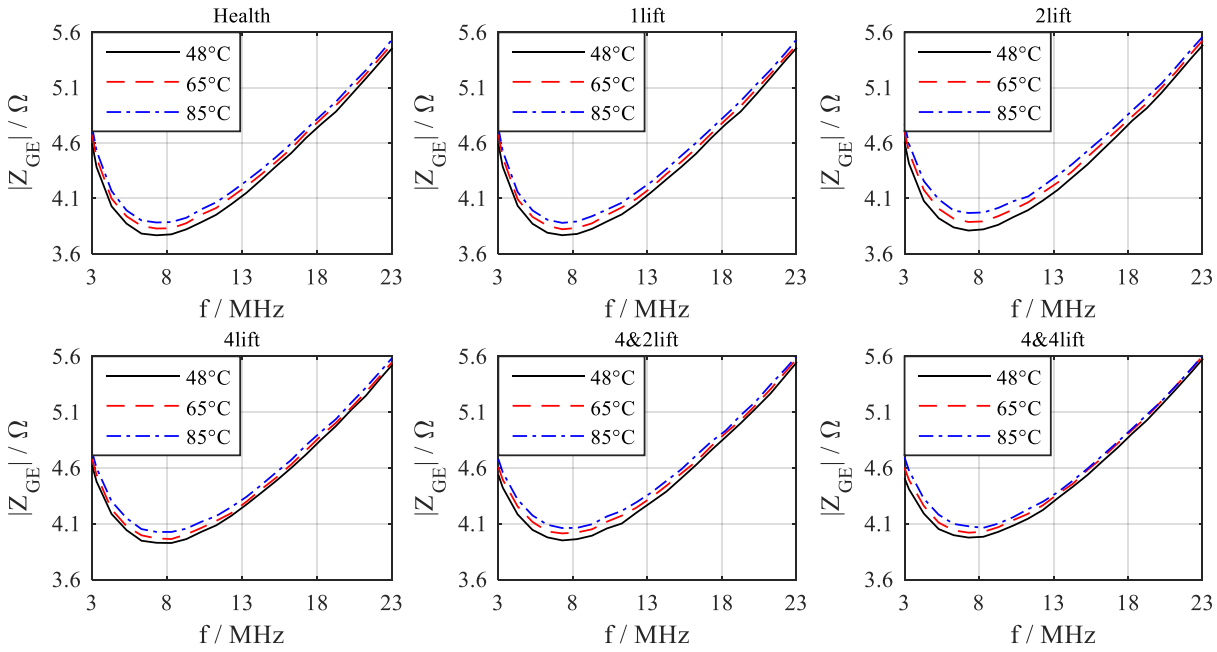


Figure E. 2 Experimental results of the frequency response of $|Z_{GE}|$ at various conditions.

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