Assessment of Novel Power Electronic Converters for Drives Applications

Dipl. -Ing. Volker Pickert

A thesis submitted for the degree of
Doctor of Philosophy

Department of Electrical Engineering
University of Newcastle upon Tyne

Abstract

In the last twenty years, industrial and academic research has produced over one hundred new converter topologies for drives applications. Regrettably, most of the published work has been directed towards a single topology, giving an overall impression of a large number of unconnected, competing techniques. To provide insight into this wide ranging subject area, an overview of converter topologies is presented. Each topology is classified according to its mode of operation and a family tree is derived encompassing all converter types. Selected converters in each class are analysed, simulated and key operational characteristics identified. Issues associated with the practical implementation of analysed topologies are discussed in detail.

Of all AC-AC conversion techniques, it is concluded that softswitching converter topologies offer the most attractive alternative to the standard hard switched converter in the power range up to 100kW because of their high performance to cost ratio. Of the softswitching converters, resonant dc-link topologies are shown to produce the poorest output performance although they offer the cheapest solution. Auxiliary pole commutated inverters, on the other hand, can achieve levels of performance approaching those of the hard switched topology while retaining the benefits of softswitching. It is concluded that the auxiliary commutated resonant pole inverter (ACPI) topology offers the greatest potential for exploitation in spite of its relatively high capital cost.

Experimental results are presented for a 20kW hard switched inverter and an equivalent 20kW ACPI. In each case the converter controller is implanted using a digital signal processor. For the ACPI, a new control scheme, which eliminates the need for switch current and voltage sensors, is implemented. Results show that the ACPI produces lower overall losses when compared to its hardswitching counterpart. In addition, device voltage stress, output dv/dt and levels of high frequency output harmonics are all reduced. Finally, it is concluded that modularisation of the active devices, optimisation of semiconductor design and a reduction in the number of additional sensors through the use of novel control methods, such as those presented, will all play a part in the realisation of an economically viable system.

Acknowledgements

Well I suppose the biggest thanks goes to my supervisor Mark. He pointed me in the right direction when sometimes something turned wrong or when I got stuck with some problems.

Life would be boring in the UG-Lab if there hadn't been people in it who made the research life easy and the social life enjoyable. Special thanks goes to Pete who answered many of my questions in my first year, Jim H. who helped me from time to time when I couldn't find the hardware failures and Ken who finally got my DSP card to work. My social life was often highlighted by one guy called Bernhard. If some of the readers feel bored on a Friday night or at the weekend then this is the person to contact.

Other inmates who I would like to thanks are: Adil, Alan, Andy, Anthony, Brian, Cidik, Chris F., Gavin, Howard, Husain, Ibrahim, Jaward, Jim K., Mohammed and Roger.

In addition notable are all the newcomers in the lab: Chris M., Christian, Hassan, Oystein, Phil, Simon, Steve and Wander.

The Ph.D. project was not only dependent on the guys already listed above. People are needed with practical skills and office work as a great deal of organisation must be carried out. In the electronics workshop thanks go to Brian, Graham, James, Jeff, Jim, Steve and Tom. In the mechanical workshop thanks go to Allen, Bob, Dave, Jack, John, Lesley and Patrick. In the office thanks go to Helen, Lynn, Sarah and Yvonne.

On the thesis writing front thanks go to Mark for general guidance and the painful corrections.

Like most things in life these days money comes into the equation at some points and nothing would happen without it. Thanks go to the Research Committee of the University of Newcastle upon Tyne who offered me a scholarship for 3 years research.

An dieser Stelle möchte ich mich auch bei meinen Eltern bedanken, die mir immer dann Mut zuredeten wenn es nötig war. Dank geht auch an meinen Bruder, der mir viele Tips und Ratschläge gab, was die Bedienung eines Computers angeht.

To all the names listed so far one is still missing. This person will probably never understand what I have done in the last three years, but has had to contend with the drawbacks of living together with a researcher. Thanks, Gillian, for your patience.

Table of Contents

List of Figures

In the following the first digit of the figures is related to the chapter, the second to the section and the third to the serial number in this section (this does not apply for figures in Appendix E).

List of Tables

In the following the first digit of the tables is related to the chapter, the second to the section and the third to the serial number in this section (this does not apply for the table in Appendix D).

List of Symbols and Abbreviations

Abbreviations

Synonyms used when talking about power semiconductors

BJT	Bipolar Junction Power Transistor
FBSOA	Forward Biased Safety Operation Area
GTO	Gate Turn-Off Transistors
IGBT	Insulated Gate Bipolar Transistor
MCT	Metal Oxide Surface Field-Effect Thyristor
MOSFET	Metal Oxide Surface Field-Effect Transistor
NPT	Non-Punch-Through
PT	Punch-Through
RBSOA	Reverse Biased Safety Operation Area
RCT	Reverse-Conducting Thyristor
SCR	Silicon Controlled Rectifier
SI	Silicon
SIT	Static Induction Transistor
SITH	Static Induction Thyristor
SOA	Safety Operation Area

Synonyms used when talking about topologies

ac	active clamp
AC	Auxiliary Circuits
ACPI	Auxiliary Commutated Resonant Pole Inverter
ADPI	Auxiliary Diode Commutated Resonant Pole Inverter
ARPI	Auxiliary Resonant Pole Commutated Inverter
D-CRSI	Delta-Configured Auxiliary Resonant Snubber Inverter
HF-converter	High Frequency converter
N-LRPI	Non-Linear Commutated Resonant Pole Inverter
pc	passive clamp
PCI	Pole Commutated Inverter (Converter)
PRC	Parallel Resonant Converter
PRDCL	Parallel Resonant DC-Link Inverter
q-RDCL	quasi - Resonant DC-Link Inverter
RDCL	Resonant DC-Link Inverter (Converter)

RPI	Resonant Pole Commutated Inverter
S-CRSI	Star- Configured Auxiliary Resonant Snubber Inverter
SRC	Series Resonant Converter
TADPI	Transformer Assisted Auxiliary Diode Commutated Resonant Pole Inverter
VS	Voltage Source
ZCS	Zero Current Switching
ZCT	Zero Current Transition
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

Synonyms used when talking about control techniques

cs	circuit specific
DPM	Discrete Pulse Modulation
DSP	Digital Signal Processor
EPROM	Electric Programmable Read Only Memory
FPGA	Field Programmable Gate Array
mPWM	modified Pulse Width Modulation
mPWM2	modified Pulse Width Modulation with two changed poles during one modulation period
mPWM3	modified Pulse Width Modulation with three changed poles during one modulation period
MFLOPS	Million Floating-Point Instructions Per Second
PROM	Programmable Read Only Memory
PWM	Pulse Width Modulation
RAM	Random Access Memory
S/H	Sample and Hold
SRAM	Static Random Access Memory
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

Synonyms used when talking in general terms

B-H	Magnetic flux - magnetic force curve
D-FF	Delay-Flip-Flop
EMI	Electro-magnetic Interferences
FFT	Fast Fourier Transformation
HVDC	High Voltage DC Transmission

LC	Inductor-Capacitor Arrangement
ppm	Part per million
RC	Resistor-Capacitor Arrangement
RCD	Resistor-Capacitor-Diode Arrangement
TK	Temperature Coefficient

Symbols

In the following '$_x$' is related to any integer number

A_L	Ratio between core cross section and square number of turns
AS_x	Auxiliary IGBT (auxiliary switch)
c_p	Coupling factor
c_x	Mathematical constants
C	Capacitor
C_{auxx}	Auxiliary capacitor
C_{clamp}	Clamp capacitor
C_{Diode}	Capacitor parallel to Diode (used in simulations)
C_{IGBT}	Capacitor parallel to IGBT (used in simulations)
C_{nonx}	Non-Linear Capacitor
C_r	Resonant capacitor
C_{snu}	Snubber capacitor of the simplified PRDCL circuit
C_{sup}	Suppresser capacitor
$C_{transformer}$	Capacitor parallel to transformer (used in simulations)
D	Diode
D_a	Ambi-polar diffusion coefficient
D_{ASx}	Antiparallel diode of auxiliary IGBT AS_x
D_{auxx}	Auxiliary diode
D_{clamp}	Clamp diode
D_f	Freewheel diode
D_{MSx}	Antiparallel diode of main IGBT MS_x
D_r	Resonant diode
E_c	Critical field in silicon
f_{out}	Output frequency
f_s	Switching frequency
$f_{s,aux}$	Switching frequency of the auxiliary circuit
h	Height of core material

i_x	Current
i_c	Collector current
i_{clamp}	Clamp current
i_r	Resonant current
i_{r1}	Resonant current of the main inductor of the passive clamp q-RDCL topology
i_{r2}	Resonant current of the auxiliary inductor of the passive clamp q-RDCL topology
$\underline{I}_{act}$	Actual current vector
I_b	Boost current
I_{load}	Constant output load current
$I_{load,\ max}$	Maximum phase load current
I_{max}	Maximum current
I_{peak}	Peak current
$I_{ph,rms}$	RMS phase output current
$I_{ph,1,rms}$	RMS phase output current at 50Hz
I_{polex}	Pole current
I_{rx}	Threshold current
$I_{r,max}$	Maximum reverse recovery current
I_{th}	Threshold current
J_c	Collector current density
k	Clamp factor
k_x	Constant
kV_{dc}	Clamp voltage
K	Constant
L	Inductor
L_m	Main inductor
L_r	Resonant inductor
L_{r1}	Main inductor of the passive clamp q-RDCL topology
L_{r2}	Auxiliary inductor of the passive clamp q-RDCL topology
L_σ	Inductor representing stray inductor
m_a	Amplitude modulation index
MS_x	Main IGBT (main switch)
n	Constant
n_p	Turns of primary windings

n_s	Turns of secondary windings
N	Number of turns
N_{pu}	Number of notches of inverter input voltage
pu	Per-unit
$P_{losses,\ on\text{-}state}$	On-state power losses
P_{sup}	Power losses in suppresser resistor
r_i	radius to the inner edge of core
r_o	radius to the outer edge of core
R	Resistor
R_{PWM}	PWM range
R_{sup}	Suppresser resistor
s	Laplacian operator
S	Switching device
S_{clamp}	Clamp switch
S_r	Resonant switch
t	Time
t_b	Minimum pulse width time
t_{DIn}	Commutation time Diode-IGBT at negative load current (ACPI)
t_{DIp}	Commutation time Diode-IGBT at positive load current (ACPI)
t_{IDn}	Commutation time IGBT-Diode at negative load current (ACPI)
t_{IDp}	Commutation time IGBT-Diode at positive load current (ACPI)
$t_{h,min}$	Minimum times for which a high voltage state is applied
$t_{l,min}$	Minimum times for which a low voltage state is applied
t_{NB}	n-base diffusion time
t_r	Half the resonant time. t_r is not current dependent (ACPI)
t_{ri}	Current rise time
t_{reso}	Half the resonant time. t_{reso} is current dependent (ACPI)
t_{rf}	Rise and fall time
t_{rv}	Softswitching voltage transition time
t_{ss}	Softswitching transition time
T	Transformer
T_{com}	Period of one commutation process
T_{inv}	Total modulation period
T_p	Period of one resonant cycle

T_S	Switching time
T_0	Resonant time of resonant circuit
TK_x	Temperature coefficient
$TK_{parallel}$	Parallel Temperature Coefficient
TK_{series}	Series Temperature Coefficient
v_c	Collector emitter voltage
V_x	Voltage
$\underline{V}_x$	Voltage vector
V_{BR}	Break reverse voltage
V_{cx}	Voltage across resonant capacitor
V'_{cx}	First derivative of voltage across resonant capacitor
V_{Crx}	Actual voltage across resonant capacitor
V_{CE}	Collector-emitter voltage
V_{dc}	Constant dc voltage source
V_{dem}	Demand voltage
$V_{Diode-IGBT}$	Voltage at commutation process Diode-IGBT
V_{eff}	Effective voltage amplitude of resonant pulse
$V_{IGBT-Diode}$	Voltage at commutation process IGBT-Diode
V_{inv}	Inverter input voltage
V_L	Voltage across inductor
V_{mid}	Midpoint voltage
V_{out}	Phase output voltage
$V_{ph,rms}$	RMS phase output voltage
$V_{ph,1,rms}$	RMS phase output voltage at 50Hz
V_R	Voltage across resistor
w_{NB}	Width of the n-base region
Z_x	Resonant tank
Z_c	Impedance of capacitor
Z_R	Resonant impedance
$\%THD_i$	Total current harmonic distortion in percentage
Δ_{PWM}	PWM resolution
Δi	Difference in actual current
ΔI	Difference in current
Δt	Difference in time

ΔT	Difference in Temperature
ΔV	Difference in applied voltage across resonant inductor of ACPI
ζ	Damping coefficient
η_s	Relative PWM range
υ	Counter variable
μ	Permeability
π	3,1416
τ	Lifetime of carriers in the n-base
Φ	Phase
$\underline{\Psi}$	Flux vector
ω_x	Resonant angular frequency

Chapter 1

INTRODUCTION

The successful application of power electronics has led to rapid growth in the market for induction motor drives. The vast majority of these drives cover the power range below 100kW. To most customers, the initial capital cost of the converter is probably the most important criterion for selection although other important factors can include: spectral performance, dv/dt induced motor insulation stress, electrical efficiency, electro-magnetic interference (EMI) compatibility, size of any input and output filter and size and weight of the converter.

Presently, the three phase, six switch voltage source bridge converter is employed almost exclusively in this application on account of its high performance to cost ratio. The continuing requirements for improved drive performance do, however, create challenges for the converter designer. Minimisation of output harmonic levels, improved dynamic performance and reduction in the size and cost of output filter components all require high switching frequencies. Regrettably, high switching frequencies imply increased switching losses, leading to increased heatsink costs, and higher levels of dv/dt stress in the case of unfiltered outputs. One possible solution to the inevitable compromise is the use of resonant techniques or softswitching. Here the active devices in the inverter are switched at zero voltage (ZVS) or zero current (ZCS), minimising the switching losses. In addition, the switching transitions take place under conditions of controlled dv/dt or di/dt, thus avoiding the high stresses associated with hardswitching. If softswitching can be implemented without increasing the overall cost of the system then there is an obvious benefit to both drives manufacturer and customer.

In the last twenty years, interest in the application of resonant techniques to converters has spawned a wide variety of novel topologies (over 100 topologies). Regrettably, most of the published work has concentrated on the mode of operation and supposed advantages of the topology rather than on providing a complete assessment including a discussion of limitations and possible area of applications.

The lack of a comprehensive comparison of novel converter topologies leads to confusion for converter designers, manufacturers and academic researchers. In addition, the multitude number of topologies with their individual abbreviations and synonyms lead to puzzlement, misunderstanding and lag on information.

1.1 Objectives and Contributions to Knowledge

The Research Committee of the University of Newcastle upon Tyne offered a scholarship to assess novel converter topologies for drives applications up to 100kW. The objectives of the project were:

- Overview of state of the art converter topologies for induction motor drives up to 100kW
- Gain a deep understanding of the various operation modes of each novel converter
- Evaluate and compare the different converter topology operations
- Critical assessment of the different converter topologies using simulation
- Experimental comparison between the most promising novel converter and a hardswitching converter

As will shown in the following chapters of this thesis, all of the objectives have been met. The following points outline what are believed to be new areas of work, previously unpublished by other authors.

- State of the art family tree of novel converter topologies, including a bibliography of 73 published papers in the last twenty years
- Comprehensive and critical assessment of novel converter topologies
- Identification and explanation of the fundamental limitations of dc-link resonant converters
- Implementation of a DSP (digital signal processor) controlled Auxiliary Commutated Resonant Pole Converter (ACPI)
- Implementation of a sensorless control scheme for the Auxiliary Commutated Resonant Pole Converter (ACPI)

1.2 Overview of Thesis

This thesis has two main sections: the Chapters and the Appendices. Chapters describe the theory, simulation and experimental results obtained for hardswitching and softswitching converters. The appendices provide detail aspects such as simulation set-ups, hardware and software circuits and mathematical descriptions.

This chapter concludes with a look at the state of the art in power electronics, before **Chapter 2** introduces the family tree of converter topologies. A general comparison of all topologies is made and a first selection quantifies which topologies are most suitable for induction motor drives. **Chapter 3** and **Chapter 4** describe in detail operation modes of various converter topologies. Simulation results of the discussed topologies are shown in Appendix A. **Chapter**

5 assesses the different operation modes. It describes benefits, limitations and drawbacks of various converter topologies. The schematics of all discussed topologies are presented in Appendix D. Finally Chapter 5 selects the most promising converter topology for drives applications. The following chapter, **Chapter 6**, describes the set-up of two converter types: hardswitching and softswitching. The softswitching converter is the selected converter from Chapter 5. A more detailed description of circuits and programs are given in Appendix B. The set-up have been pictured and is shown in Appendix E. Chapter 6 describes also a novel control algorithm applied on the designed softswitching converter. The theoretical work on the control algorithm is given in Appendix C. **Chapter 7** shows waveforms and other practical results. A comparison between both converter types is given. **Chapter 8** concludes the work and provides an overall assessment of the different converter topologies.

1.3 Electrical Machine Drives

Electrical machine drives play a vital role today, with applications in almost every aspect of life. Domestic and automotive applications provide a vast market for low power applications, with manufacturing and process industries providing a lower volume higher value market for medium and high power drives.

In the high power market, variable speed drives and servo drives represent a large and varied market from pumps through robot systems to rail traction. This was once the preserve of brushed DC machines with variable resistance or Ward-Leonard supplies, but the advent of electronics has opened up a wide range of machine types for variable speed operation. Today's variable speed drives incorporate both DC and AC machines including induction motors, synchronous machines, permanent magnet motors and switch reluctance motors. Induction motors now dominate the market and is seen as future workhorse in variable speed applications.

Drives manufacturers prefer AC induction motors, because of their cost effectiveness compared to all other motor types. When combined with advanced control structures, AC induction motor drives deliver a level of dynamic performance previously only available from DC drives while maintaining the advantages of robustness, no brushes and lower cost. The global AC motor drives market is expected to expand from $ 3 billion in 1995 to $ 10 billion in the year 2000 [1.1].

1.4 Power Electronics and its Constituent Technologies

Power electronics deals with the conversion and control of electrical power in various industrial, commercial and residential applications. Almost all electrical converters are static electric power converters that change the energy flow from the supply to the load by using power switches. In welfare countries, 65% of distributed energy is converted into mechanical rotation energy [1.2].

The history in power electronics started with the invention of the mercury-arc rectifier at the beginning of this century. At this time switching devices of gas tubes were used to allow controlled power flow. Most industrial applications of the mercury-arc rectifier lasted until the first silicon-controlled rectifier device was developed by Bell Laboratories in 1956. It was this development that facilitated the start of modern power electronics.

Today, power electronics is a multiple technology discipline (Figure 1.4.1). Each of the constituent component technologies interact and converter designers need knowledge in all of these different disciplines.

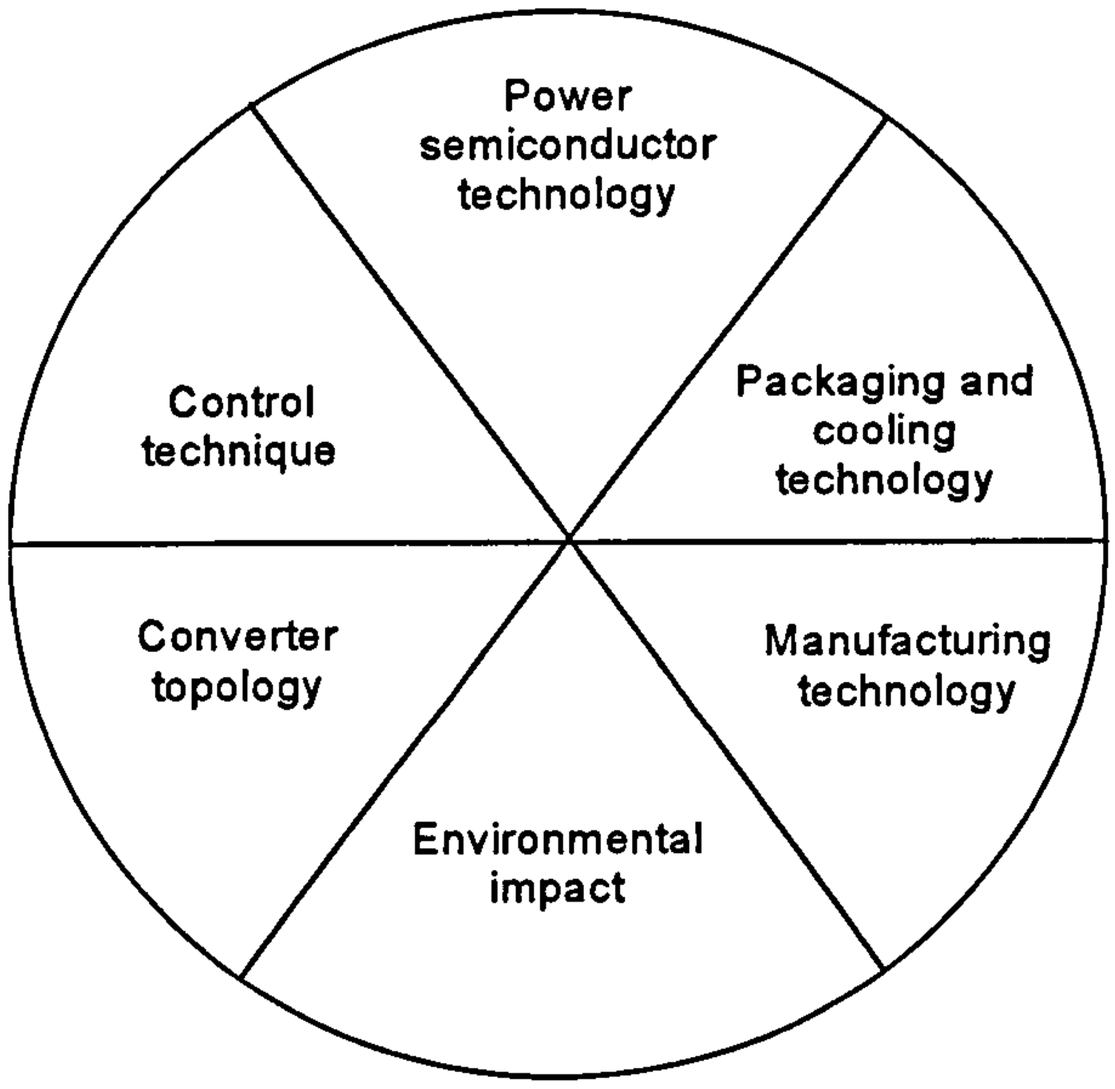


Figure 1.4.1: Constituent technologies in power electronics

With no doubt the most progressive disciplines of all six technologies are the development of electronic power semiconductor device technology, control techniques and converter topologies.

1.4.1 Power Semiconductor Technology

Probably the first power device was mentioned in 1882 by Jemin and Meneuvrier [1.3]. They experimented with an atmospheric mercury-arc rectifier and gave an account of property of an electric arc established between mercury and carbon electrodes, mentioning that the current will flow in one direction only. In 1892 Arons made the first vapour lamps by enclosing the arc in an evacuated vessel. Ten years later during investigations of these lamps Cooper-Hewitt came up with the idea to convert alternating current to direct current. The mercury-arc rectifier family developed from this beginning. Between 1920 and 1930 a relatively large-scale of practical applications of mercury-arc rectifiers were produced. With the first solid-state device [1.4] in 1925 and the development of the first controlled solid-state power electronic device , the Silicon Controlled Rectifier or thyristor displaced mercury-arc rectifiers (Mercury-arc rectifiers sustained in high voltage dc transmission (HVDC) installations until the early 1970s because thyristor technology was not yet sufficiently advanced).

The remarkable feat in understanding, controlling and utilising device physics has extended the switching frequency, the operational voltage and current range and the reliability of the devices. Parallel to this development, a drop-off in prices for silicon and an aggressive competition market has resulted in today's cost-efficient semiconductor devices. The global power semiconductor market is expected to increase from $ 5 billion in the year 1996 to $ 11 billion in the year 2000 [1.1].

1.4.2 Control Techniques

Beside the rapid development in power device technology, motion control was also influenced by the use of integrated signal electronics that simplified the electronic control hardware. The IC industry was and still is on a self-prescribed course to greater triumphs: ever-smaller devices and faster circuits. Results are the introduction of microcontrollers (1970) and DSPs (1980). These powerful tools add intelligence as well as diagnostic capability to the motion control system and are today indispensable in drives.

The advent of microcontrollers allowed control engineers implementations of varieties of control techniques. Microcontrollers permit simplification of control hardware, improve reliability and eliminate drift problems. Constant improvement in faster execution times, increased range of mathematical data processing and fast access time to memory marked their success. But with more complex and computationally intensive control schemes insufficient processing power is available from a microcontroller. This has led to an increase adoption of digital signal processors (DSPs) using the latest VLSI\ULSI (very \ ultra large scale

integration) technology to allow new architectures in hardware. Toady's manufactured DSPs from Texas Instruments led to an increasing adoption of their developed DSP first sold in 1982 [1.5]. The advanced capabilities of DSPs, with instruction execution times of less than 40ns and 55 million floating-point instructions per second (MFLOPS) and higher, for a volume price of $ 10 a piece leads to the belief that DSPs will dominate the commercial drives market in the near future.

In a like manner, software control algorithms had the same tremendous development. Software enables the implementation of universal control strategies, which offer flexibility but may easily be optimised for a given application. The use of Neural networks [1.6] and Fuzzy logic [1.7] are the latest software packages available, but still suffer from the large number of weights and rules required to implement a high performance induction motor drive.

1.4.3 Converter Topologies

The first known converter topology was the rectifier. The converter was only able to convert an ac signal to a dc signal and dates back to 1902. Performing the inverse of the rectification process provided more difficulties until 1906 when Steinmetz inverted a dc signal to an ac signal using a 'switching tube'. This tube had a single-cathode and four anodes in which the discharge spontaneously switched from anode to anode in predictable order. Nineteen years later Prince developed the 'Parallel Inverter' using two plitron tubes. This inverter used natural commutation and was not able to handle any reactive power. In 1931 Steenbeck and Petersen further developed Prince's 'Parallel Inverter' and introduced a line commutated converter that handled any reactive power. The 'Parallel Inverter' is seen as the first converter that converts an ac input signal into a controlled ac output signal at different frequencies. This converter type became later known as the cycloconverter, when semiconductor devices were used instead of switching tubes (historical data given in this section have been published in detail in reference [1.8]).

The AC-AC conversion technique of the cycloconverter is supplied from many unipolar switches (18, 36, or more), which is seen as an inherent disadvantage. In addition using thyristors, the cycloconverter was phase-controlled meaning that a firing angle for each individual device controlled the power flow (natural commutation). It is well known that any phase-controlled converter topology produces harmonics in load voltage and line current and the inherent lag between line fundamental current and line voltage diminish the power factor [1.5].

Today's converter design for AC motor drives is based on the Direct DC-Link Converter topology (section 1.6). This type of topology uses a three-phase input rectifier and a three-phase output inverter. Reduced output harmonics, fewer switches and simplicity in control diminish further implementation of the cycloconverter and marked the success of the Direct DC-Link Converter.

Latest converter design for AC motor drives concentrates on further reduction of output harmonics, decrease in converter sizes (eliminating the dc-link capacitors, reducing output filters) and reduction in switching losses. Examples of novel topologies are: the matrix converter with its eighteen unipolar switches for high power applications (no dc-link capacitor), the multilevel converter for high voltage applications and the resonant converter that allows reduction in switching losses.

1.5 Power Semiconductor Devices--State of the Art

The present range of controlled power devices seems to be narrowing down to thyristors, gate turn-off transistors (GTOs), bipolar junction power transistors (BJTs), metal oxide surface field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), with promise still in MOS-controlled thyristors (MCTs; Figure 1.5.1). New devices such as static induction transistors (SITs) and static induction thyristors (SITHs) are under development and show promise for induction heating applications [1.9].

Figure 1.5.1 shows that thyristors dominate in the fields blocking voltage and current capability. Blocking voltage of 6000V and a carrier current of 3500A have been reported [1.10], but the switching frequency is limited, because of the need of the long critical hold-off interval and the long gate-controlled turn-on time. Thyristor converters are used for power distribution, as in HVDC or in phased-controlled heavy load drives applications.

GTOs are the successors of the thyristors. The turn-off capability is an indubitable advantage over the thyristor but compared to other turn-off devices the switching frequency is strongly limited to around 2kHz. That is because of the need of large snubber circuits for the device. During turn-off, dv/dt on the device has to be limited, otherwise a breakdown failure would damage the device. Using a RCD-Snubber circuit (resistor, capacitor, diode) the snubber controls the dv/dt stress but the resistor causes turn-off losses with increasing switching frequency. Beside the use of the snubber, a large anode tail current during device voltage build-up causes still additional power dissipation in the device resulting in a large heatsink configuration. Resistors and heatsinks of GTO circuits are to be designed large, whereby complex snubber circuits with low power dissipation are necessary to avoid above problems

resulting in the need to have an expensive and bulky converter when using GTOs. In drives applications GTOs are mainly used for heavy drives where pulse width modulation (PWM) with relatively high switching frequency is required.

With respect to the GTOs, BJTs are devices with limited need for snubber circuits. That is because of its almost rectangular forward bias safe operation area (FBSOA) and reverse bias safe operation area (RBSOA). But nevertheless design of the converter has to be well considered, because both safe operation areas are strongly dependent on variations in temperature. An increase of the temperature decreases the safe operation area and limits the operating forward current and blocking voltage. BJTs were implemented in many converter applications before the commercialisation of the IGBTs started, but robustness of IGBTs and the simplicity of IGBT drivers diminished further implementation of BJTs in the drives market.

Power MOSFETs are clearly the fastest devices of all (100kHz). The low power capability makes this device very popular in low-voltage, low power applications, such as dc-dc power supplies. The major problem is the voltage conduction drop between source and drain caused by the internal source-drain resistor and the consequent conduction losses. Nevertheless continuing research seeks to increase the power range for MOSFETs using new materials such as gallium arsenide, silicon carbide or more sophisticated diamond.

The physical structure of the IGBT allows the device to have a relatively constant FBSOA and RBSOA regarding variations of temperature. Higher switching frequency, like the BJT and higher current density, like the MOSFET, allow the IGBT to dominate in a power range from 1kW to 100kW. Simplicity of gate drives, simplicity of protection and power circuit integration capability, marked today's success of IGBTs. With the latest device from ABB (1200A and 2500V [1.11]) IGBTs will dominate not only power ranges around 100kW but far beyond and could even replace GTOs in high power applications.

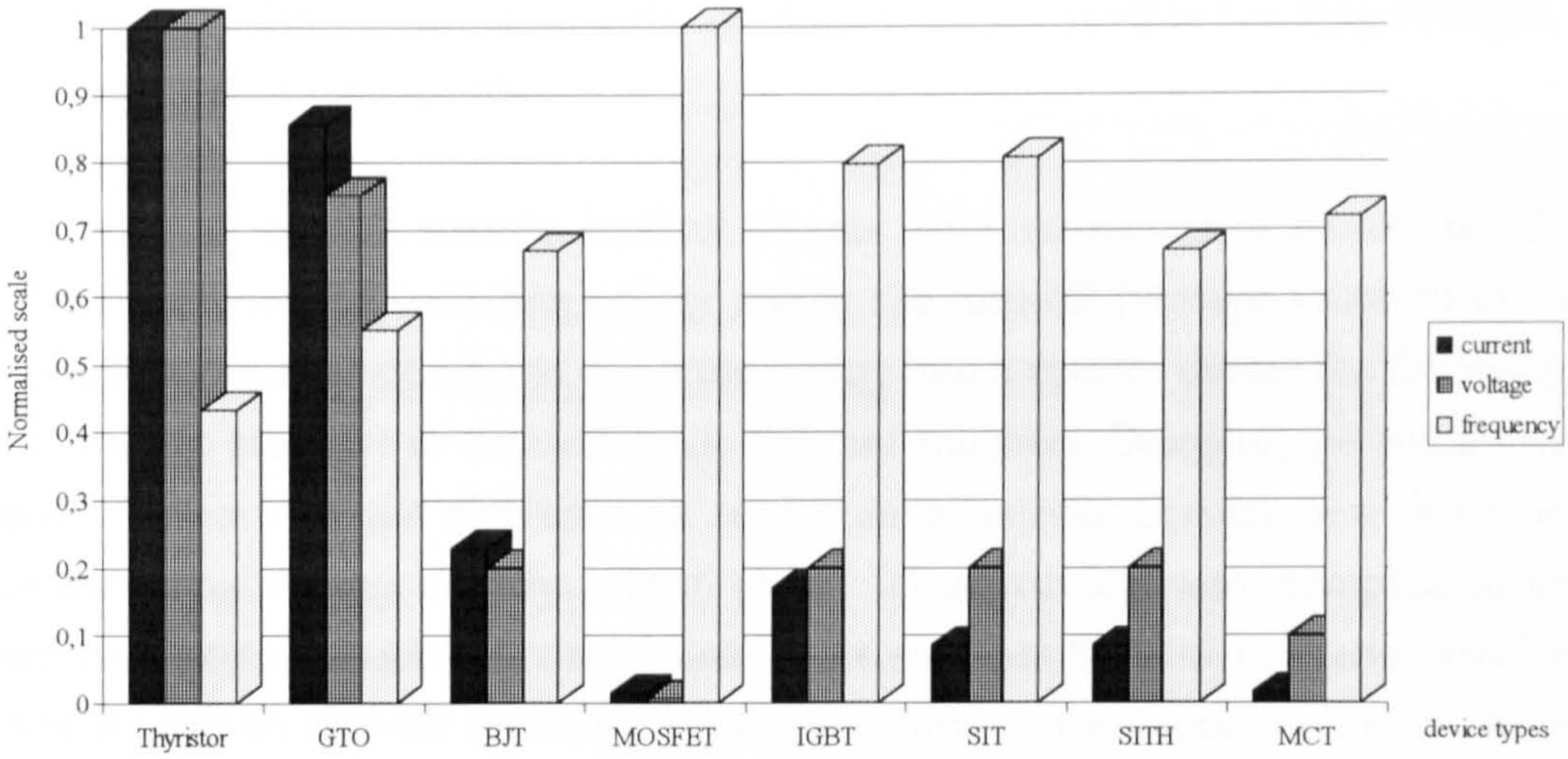


Figure 1.5.1: Comparison of power semiconductor devices. Normalisation index: Thyristor: 3500A, Thyristor: 6000V, MOSFET: 1MHz (Logarithmic scale for the frequency: value 1≡1MHz, value 0.5≡1kHz) [1.9]

1.6 Direct DC-Link Converter

With the first SCR devices available, researchers developed various converter topologies to meet a range of load applications. The demands of synchronous motor and induction motor drives require mostly a conversion of a three phase ac voltage at fixed frequency into a variable voltage, variable frequency three phase supply. The three phase, six switch voltage source bridge converter, also called Direct Voltage DC-Link Converter, was seen as an ideal converter topology for this application, mainly because the Direct Voltage DC-Link Converter uses a small number of unipolar switches.

1.6.1 Direct Voltage DC-Link Converter

The Direct Voltage DC-Link Converter is shown in Figure 1.6.1 (using diodes for the rectifier and IGBTs and antiparallel diodes for in the inverter).

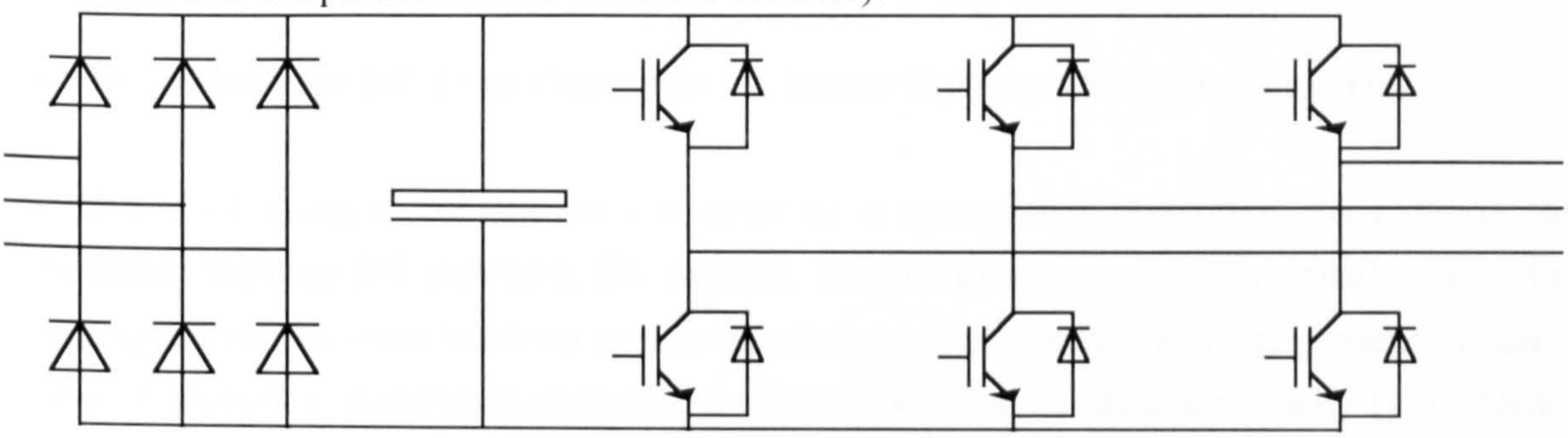


Figure 1.6.1: Direct Voltage DC-Link Converter

In the early days, the operational characteristics of Direct Voltage DC-Link Converters were limited by the technology of the first SCRs, suffering from low reverse blocking voltages, small di/dt rates and no turn-off capability.

To limit voltage or current stresses snubber circuits were introduced to protect the devices. Snubber circuits store the switching energy during the turn-off (voltage snubber) or turn-on (current snubber) transition time and dump the energy into a resistor during the following turn-on mode (voltage snubber) or turn-off mode (current snubber). Dumping the energy worsens the overall efficiency of the converter so regenerative snubber circuits were introduced to feedback the stored energy into the system [1.12]. These circuits were complicated and the integrated regenerative snubber circuits counts more switches than the converter itself had. In addition SCRs had no turn-off capability, thus only natural commutation took place, leading to problems with input and output harmonics. Much effort was expended in the development of so called SCR Force Commutation Technology. A resonant circuit was placed in parallel or in series to the SCR. The resonant circuit, usually including one or two additional auxiliary SCRs forced the current flowing through the main SCR to zero. Using this technique, turn-off capabilities became available in the SCRs. However, the availability of the gate turn-off technology led to the gradual obsolescence of forced commutation.

With the introduction of turn-off devices such as the IGBT, force commutation could be applied across the Direct Voltage DC-Link Converter. Thus beside phase-control novel control schemes such as PWM control was applied. PWM control is seen as the most efficient control method of the Direct Voltage DC-Link Converter and is in industry well established. It is today's most common drive set-up for induction motor drives.

Parallel to the development of Direct Voltage DC-Link Converter was the development of the Direct Current DC-Link Converter. The main difference is the use of a large inductor between rectifier and inverter in a Direct Current DC-Link Converter, whereas a dc-link capacitor is integrated in a voltage-fed converter. In addition the rectifier of the current-fed converter is a controlled rectifier.

1.6.2 Direct Voltage DC-Link Converter vs. Direct Current DC-Link Converter

The choice of using a voltage-fed converter or a current-fed converter, depends on the application. Voltage-fed inverters, for instants, do not operate in all four quadrants in the torque-speed plane (when fed from an uncontrolled rectifier), but do allow instantaneous drive of several motors in parallel. A current-fed inverter is a one machine drive only [1.9]. Under

consideration of size and weight, current-fed inverters are less attractive, because of the need of associated output filter capacitors and the need of a heavy dc-link inductor.

	VOLTAGE-FED INVERTER	**CURRENT-FED INVERTER**
operation modes	two-quadrant operation when using an uncontrolled rectifier	four-quadrant operation
number of parallel drives	multi-machine drive	single-machine drive
short circuit allowance	no allowance of short circuit between two inverter legs	momentary allowance of short circuit between two inverter legs
performance	fast performance	sluggish performance
performance under light load conditions	handles no-load conditions	requires minimum load
required filter	need inductors for output filter	need inductors and capacitors for output filter
required type of rectifier	need either uncontrolled or controlled rectifier	need controlled rectifier
cost	dc-link capacitor is lighter and cheaper than a dc-link inductor	dc-link inductor is heavier and more expensive than a dc-link capacitor

Table 1.6.1: Pros and cons of voltage-fed inverters and current-fed inverters

Table 1.6.1 shows pros and cons of both inverter types. General advantageous for current-fed inverters are in drives application with low dynamic performance and the need of a four-quadrant operation. In practice current-fed inverters have to be used in the power range of at the least 50kVA to economically compete with the voltage-fed inverter [1.13]. Therefore the most used inverter type in drives application up to 100kW is the voltage-fed inverter and is mainly discussed in this dissertation.

1.6.3 Demands on Novel Converter Topologies

Drives performances can be improved when increasing the inverter switching frequency of the Direct DC-Link Converter. At higher frequency levels the output harmonics improve, the output current ripple is reduced, the output filter size decreases and the audible noise is reduced. However, higher switching frequency means higher losses resulting from overlapping of voltage across the device and current through them during turn-on and turn-off process. In addition, higher switching frequencies lead to higher dv/dt stress across the device and, in the

case of unfiltered outputs across the motor windings themselves. Demands on novel converter topologies can be summarised as follows:

- Reduction or elimination of output filters
- Higher switching frequency for better drives performance
- Reduction in dv/dt reduces stress across the device and on motor isolation
- Reduction in overall size and weight
- Reduction of heatsink size
- Switching frequency outside audible noise
- Use of low number of devices
- Elimination of dc-link capacitors
- Less maintenance work
- Easy manufacturing
- High reliability
- Low cost

1.7 Softswitching vs. Hardswitching

Devices that switches rapidly between the supply rails switch under hardswitching conditions. The device must be able of handling the resulting switching stress (Figure 1.6.1). During inductively loaded, hard switched turn-on and turn-off, the product of voltage across the device and current through the device leads to switching losses. In addition during conduction time of the device conduction losses must be added. The loss during the time where the device is off is negligible. Figure 1.7.1 shows voltage, current and power losses waveform. In addition Figure 1.7.1 shows the switching trajectory.

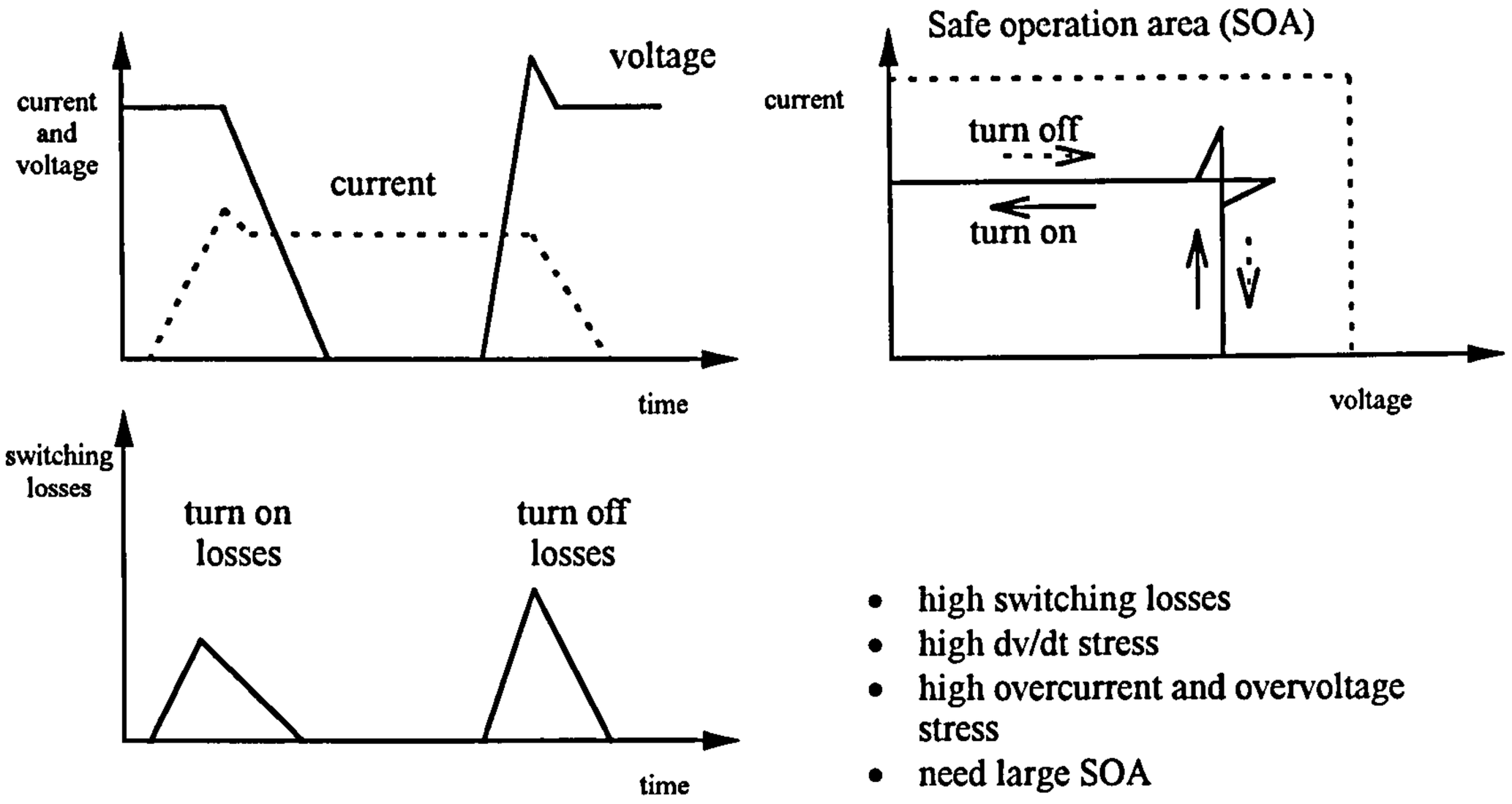


Figure 1.7.1: Hardswitching waveforms

An alternative to hardswitching is softswitching technique. A softswitching converter keeps a power device from switching except when there is nearly zero voltage across the device or zero current through it (or both). Switching losses plummet, so that switching frequencies and control bandwidth can be increased, in some cases by up to an order of magnitude, while at the same time the voltage rate of change and the EMI are decreased.

Softswitching can be accomplished in a variety of ways. Most of the approaches work by diverting and recovering switching loss energy. It is diverted from the device into capacitors or inductors. Then the trapped energy is recovered in the course of natural consequence of the operation (resonance) within the converter circuit (Note, regenerative snubbers generally use an auxiliary converter whilst softswitching topologies recover energy directly through the resonant tank). Figure 1.7.2 shows current, voltage and losses waveforms of zero voltage softswitching (ZVS) and zero current softswitching (ZCS). The trajectory curve of Figure 1.7.2 shows that the switching safe operation area can be reduced when softswitching is applied.

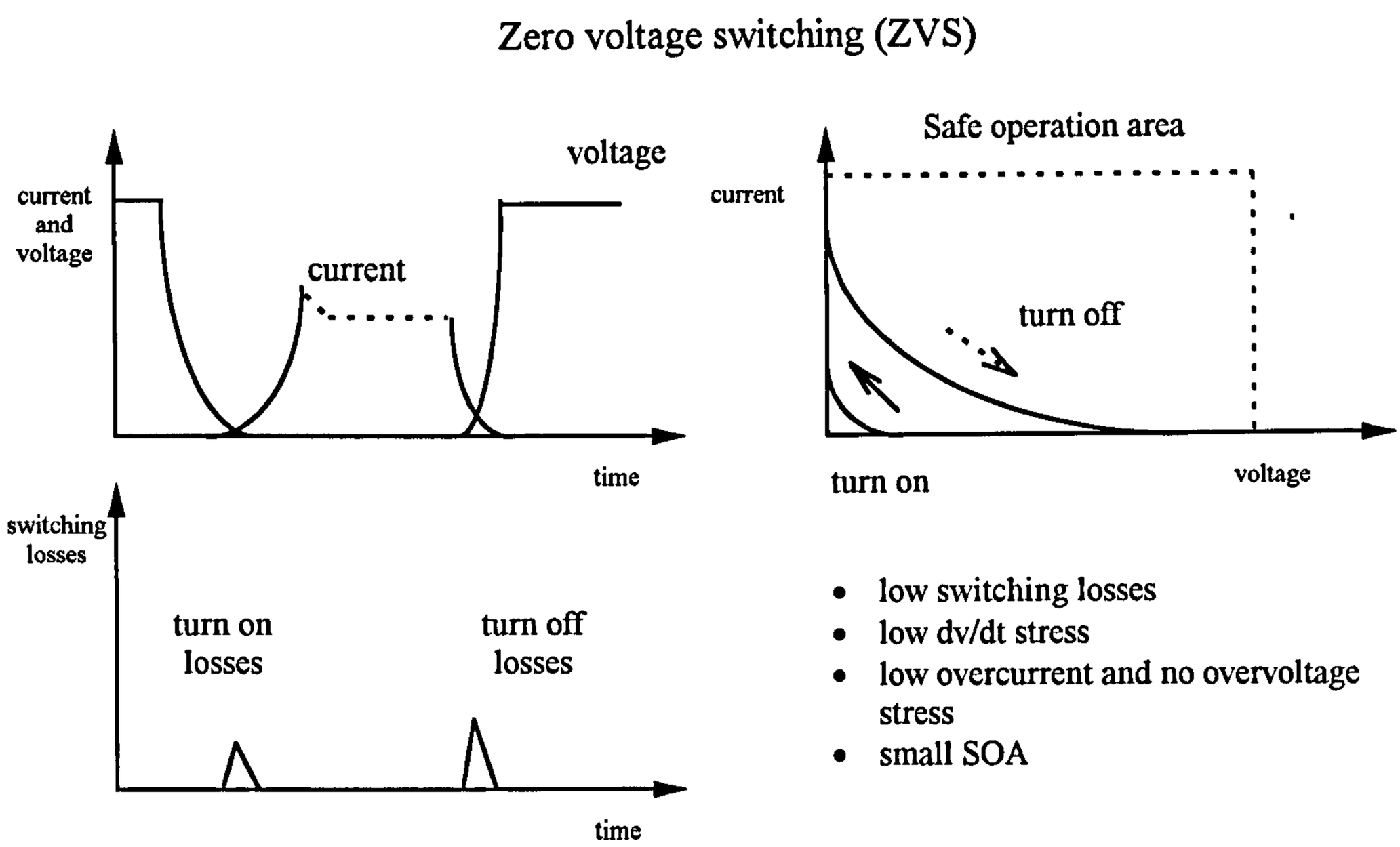


Figure 1.7.2: Softswitching waveforms

One speaks of zero voltage switching (ZVS), when the on-state voltage across the device is forced to zero and stays zero during the switching event. One speaks of zero current switching (ZCS), when the current through the device is forced to zero and stays zero during the switching event. Some topologies make use of both techniques meaning that current and voltage is forced to zero and stays zero during the whole switching event.

The question which technique (ZVS or ZCS) is the most preferable can not easily be answered. For instance the MOSFET for example, is well suited for ZVS, because of its very short current fall time at turn-off and the absence of a tail current that occurs with the use of IGBT devices. However, MOSFETs can not be used in the higher power range.

Another example is given in reference [1.14]. Reference [1.14] compared various generations of IGBTs. The paper concludes that IGBTs of the third and forth generation are more suitable for ZVS than IGBTs from the first and second generation. The reason for that is because IGBTs of the first and second generation have a much longer turn-off time and higher and longer tail current than IGBTs of the third and fourth generation. Reference [1.15] compared high speed IGBTs and low loss IGBTs of the forth generation under ZVS conditions. The outcome of the paper is that high speed IGBTs are useful for high switching frequencies, but losses increase at lower switching frequencies, whereas low saturation IGBTs show the opposite behaviour. Reference [1.15] and reference [1.16] also describe the differences in switching behaviour of Punch-Through IGBTs and Non- Punch-Through IGBTs. In general it can be concluded that NPT IGBTs show higher switching losses than PT IGBTs under ZVS conditions. Chapter 6 describes in detail the differences and the effect on the switching behaviour.

Besides the device type, the switching behaviour is also influenced by the effect of parasitic elements in the switching device module and parasitic elements caused by additional passive devices that are included in the converter design such as capacitors or inductors. Turn-off switching losses of diodes are more easily controlled when using ZCS. At ZCS the change of current rate is defined by the resonant inductor. Thus the diode is softened and rates of changes of voltage and current at the switching instants are limited. [1.17].

However the final decision of whether ZVS or ZCS applies across a device is determined by the converter topology, because the arrangement of passive elements determine finally the switching techniques (see Chapter 3 and Chapter 4).

1.8 Control Techniques for Three-Phase Inverters

All the known control principles can be divided into two large families: control techniques with and without carrier signals. The switches of the former controlled converter are switching synchronously to a defined constant carrier frequency. Thus the control scheme produces discrete harmonics in the output spectrum, whereas techniques without carrier signals produces a whole range of harmonics in the output spectrum. The most well known control techniques without carrier signals are predictive current control and hysteresis control. Well

known members of control techniques with carrier signals are pulse-width modulation (PWM) and square-wave modulation control.

Fig. 1.8.1 shows the mechanism of sinusoidal PWM control. A sinusoidal voltage reference curve with adjustable amplitude and frequency are scanned by a repetitive signal (usually a triangular voltage) of constant amplitude. At the intersection points of the two curves the corresponding inverter branch is switched from plus to minus or reverse. Sinusoidal PWM control was first described in reference [1.18]. In the meantime variations have been realised like harmonic elimination PWM control [1.19] or regular sampling PWM control [1.20]. Sinusoidal PWM is used for open loop control or for closed loop control on the basis of field orientation.

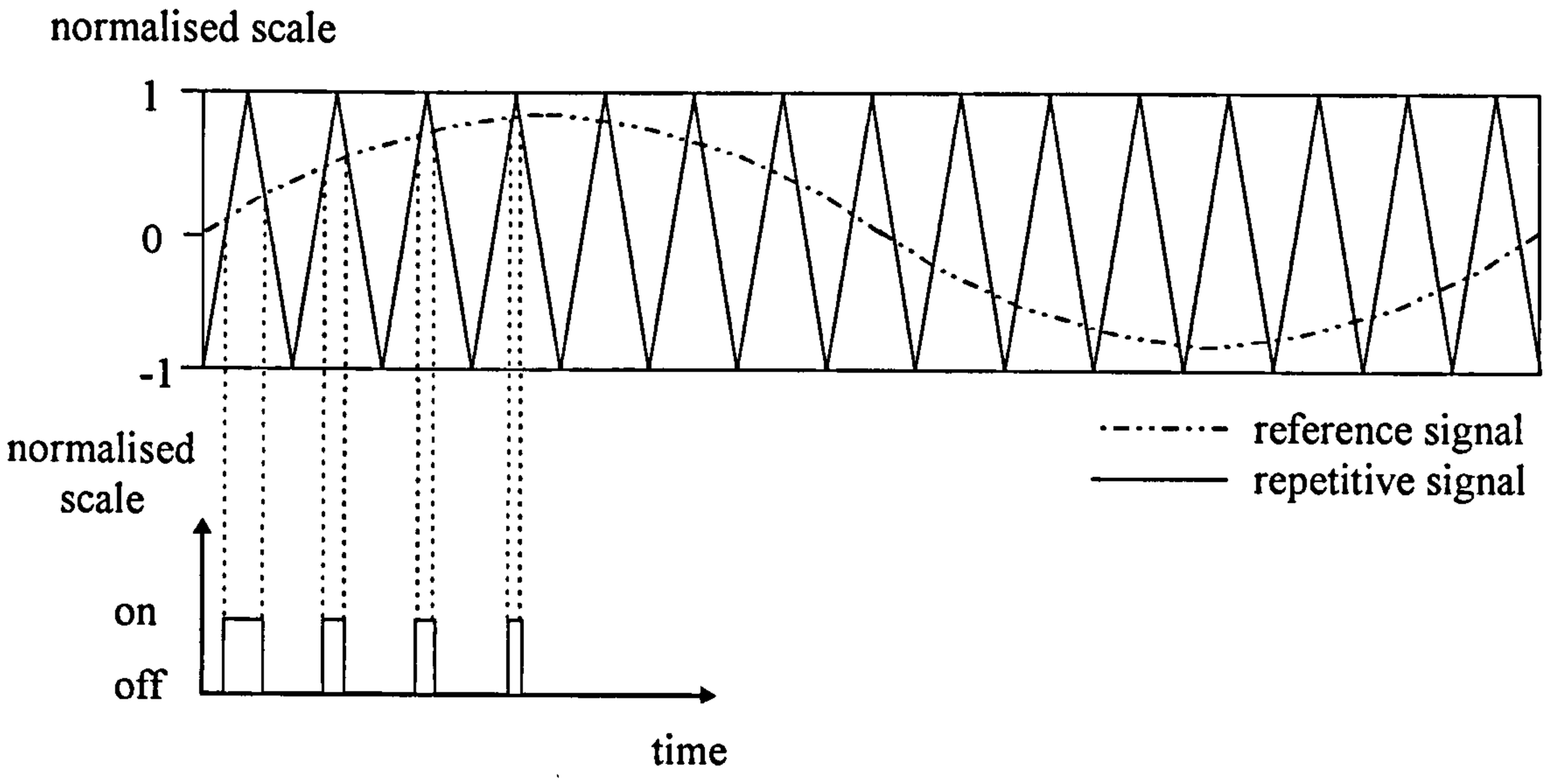


Figure 1.8.1: Sinusoidal PWM control

AC drives control involving field orientation is called space vector control [1.21 and 1.22] (Figure 1.8.2). The idea is to approach the continuously turning space vector of a sinusoidal supply by time dependent interpolation of the adjacent space vectors of the inverter supply. In space vector control the three-phase output current is converted, by a demodulating transformation into two right-angled currents. A characteristic feature of such control system is that, thanks to applied three-two co-ordinate transformations, the two output currents are dc-components, and with the use of linear PI regulators very high accuracy in the steady state can be attained. This allows the control of the induction motor with the same performance as the dc motor.

Sinusoidal PWM and space vector control share an analytical relation that was shown in reference [1.23]. It was derived that space vector control can also performed by sinusoidal PWM. In this case a third harmonic has to be superimposed on the sinusoidal reference voltage [1.24].

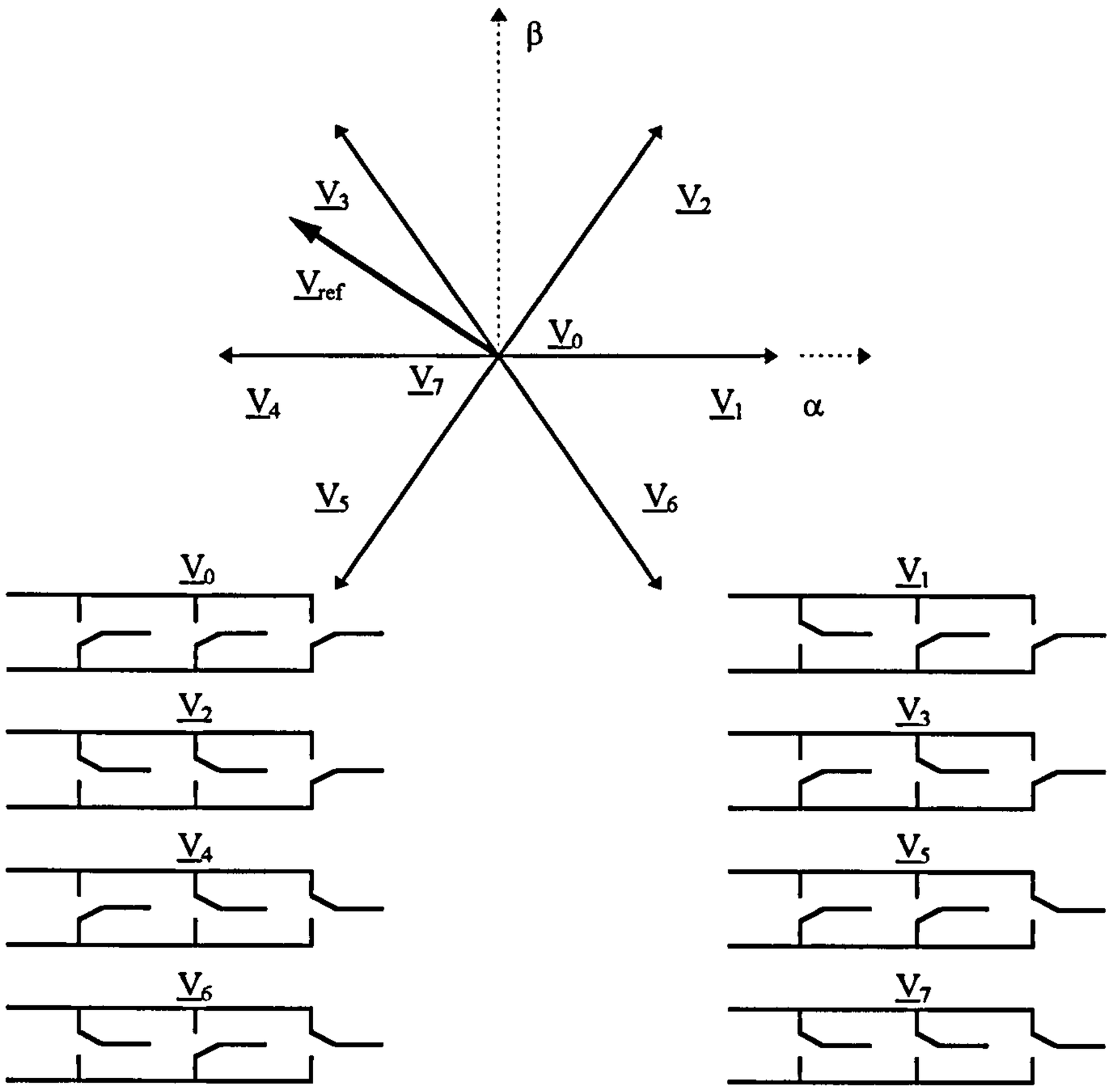


Figure 1.8.2: Voltage space vectors and inverter switching states in the α, β plane. The α, β plane delineates the stator reference frame

A similar performance to space vector control can be achieved using direct self control [1.25] (Depenbrock method). Fig. 1.8.3 shows the stator flux trajectory in the α, β plane. The points on the track mark a constant flux during a certain amount of time defined by the controller. When stopping the flux vector periodically by interposing zero voltage vectors the speed and the stator voltage are reduced without decreasing the flux vector. This is desired in applications where change of speed is desired while keeping the flux constant.

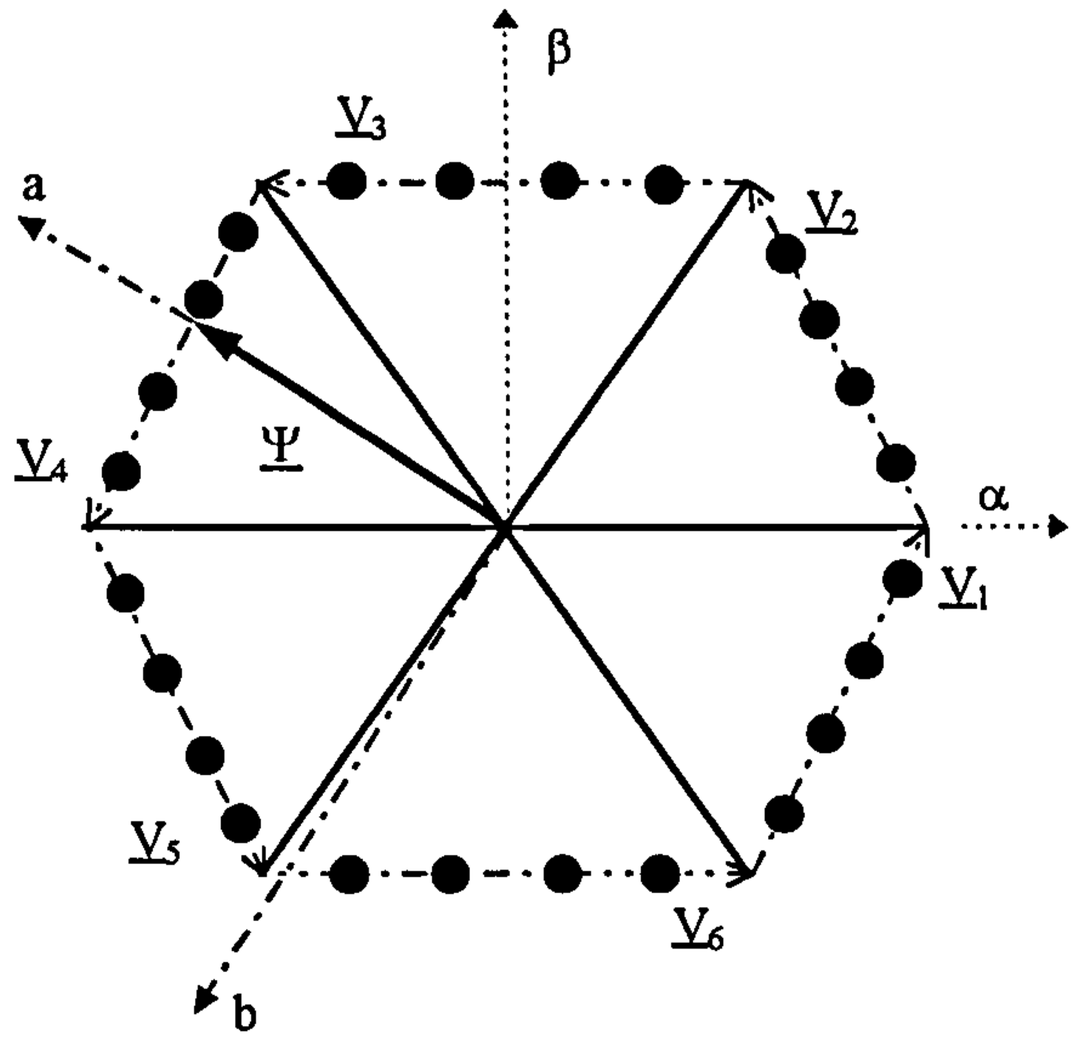


Figure 1.8.3: Stator flux trajectory of direct self control (Depenbrock control method). The corresponding switching states for each voltage vector is shown in Fig. 1.8.2. a and b delineates the rotor reference frame and α and β delineates the stator reference frame

Another way of controlling the flux is to move the flux vector along a circle, thus approaching sinusoidal voltage supply [1.26] (Takahashi method). The torque is controlled by switching back and forth between two zero voltage vectors and two adjacent voltage vectors. The adjacent voltage vectors guide the flux inside the hysteresis band, whereas the zero voltage vectors cause the flux vector to stop at the points marked in Fig. 1.8.4.

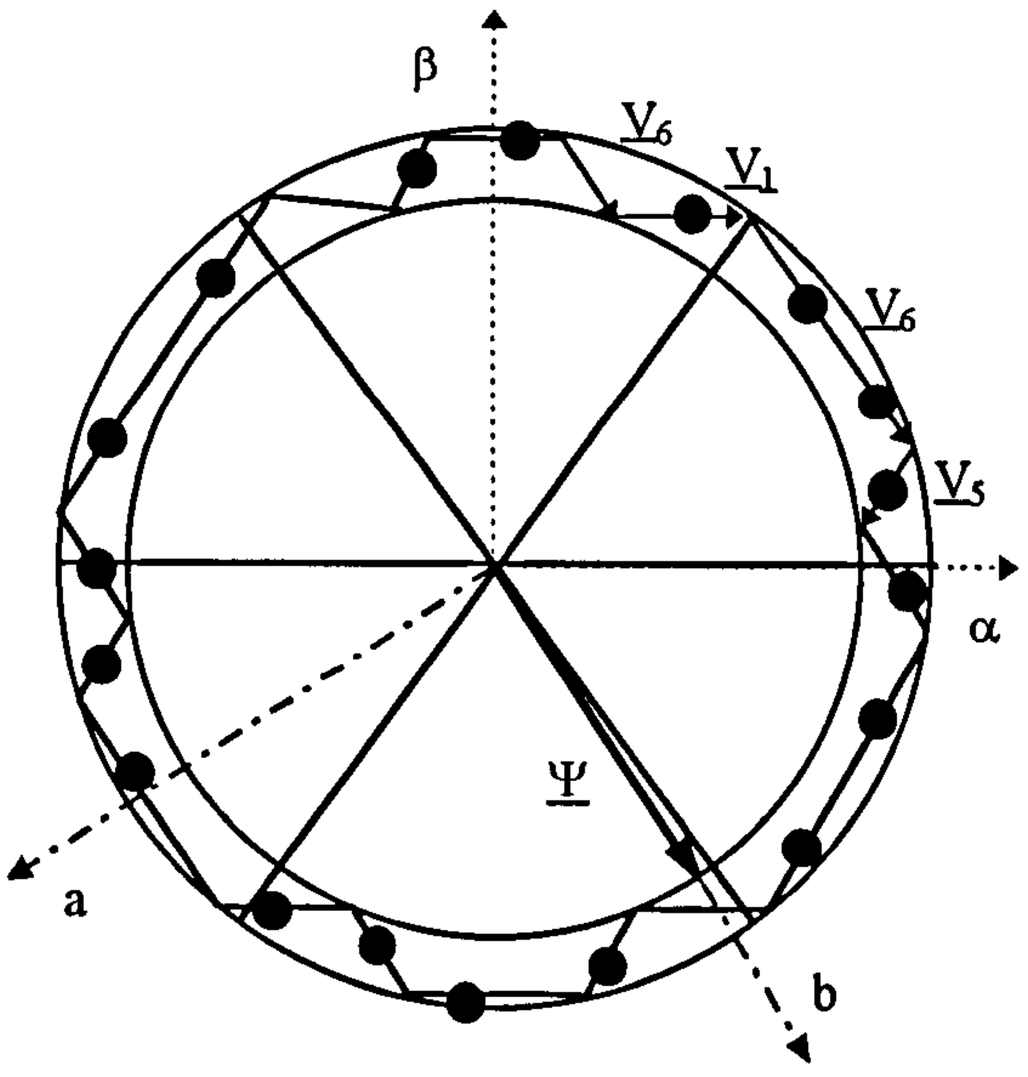


Figure 1.8.4: Stator flux trajectory of direct torque control (Takahashi control method). The corresponding switching states for each voltage vector is shown in Fig. 1.8.2. a and b delineates the rotor reference frame and α and β delineates the stator reference frame

A comparison between vector control and direct torque control is given in reference [1.27]. In this paper it was found that direct torque control is less complex, the torque response time is faster than for vector control and vector control is more parameter sensitive than direct torque control. That is because of rapidly variation of resistance change due to the skin effect. The temperature variation is difficult to adapt and wrong estimated parameters degrade the drive performance. Direct torque control is characterised by not having a co-ordination transformation, not requiring a voltage or current modulator and not needing a voltage or current decoupling network. At the moment only ABB is using the direct torque control technique in commercial drives applications [1.28]. Most of today's AC drives use PWM control or space vector control in the case of servo drives.

Square-wave controllers are used for hardswitching dc-link inverters for heavy load applications. The upper and lower switch of a phase leg conduct 180° and the three phase groups are mutually phase shifted by 120° to generate a six-step line voltage wave at the inverter output. The six-step output voltage is rich in harmonics, leading to current heating in the machine windings and torque pulsation's. Therefore square-wave controlled inverters need heavy filtering to avoid these problems [1.5].

The so far above described control methods control the output voltage of the inverter. The hysteresis control method is based on controlling the output current and the simplest regulation scheme is based on a non-linear feedback loop with two-level hysteresis comparators. It is characteristic for the hysteresis regulator that the instantaneous current is kept exact in tolerance band (Figure 1.8.5).

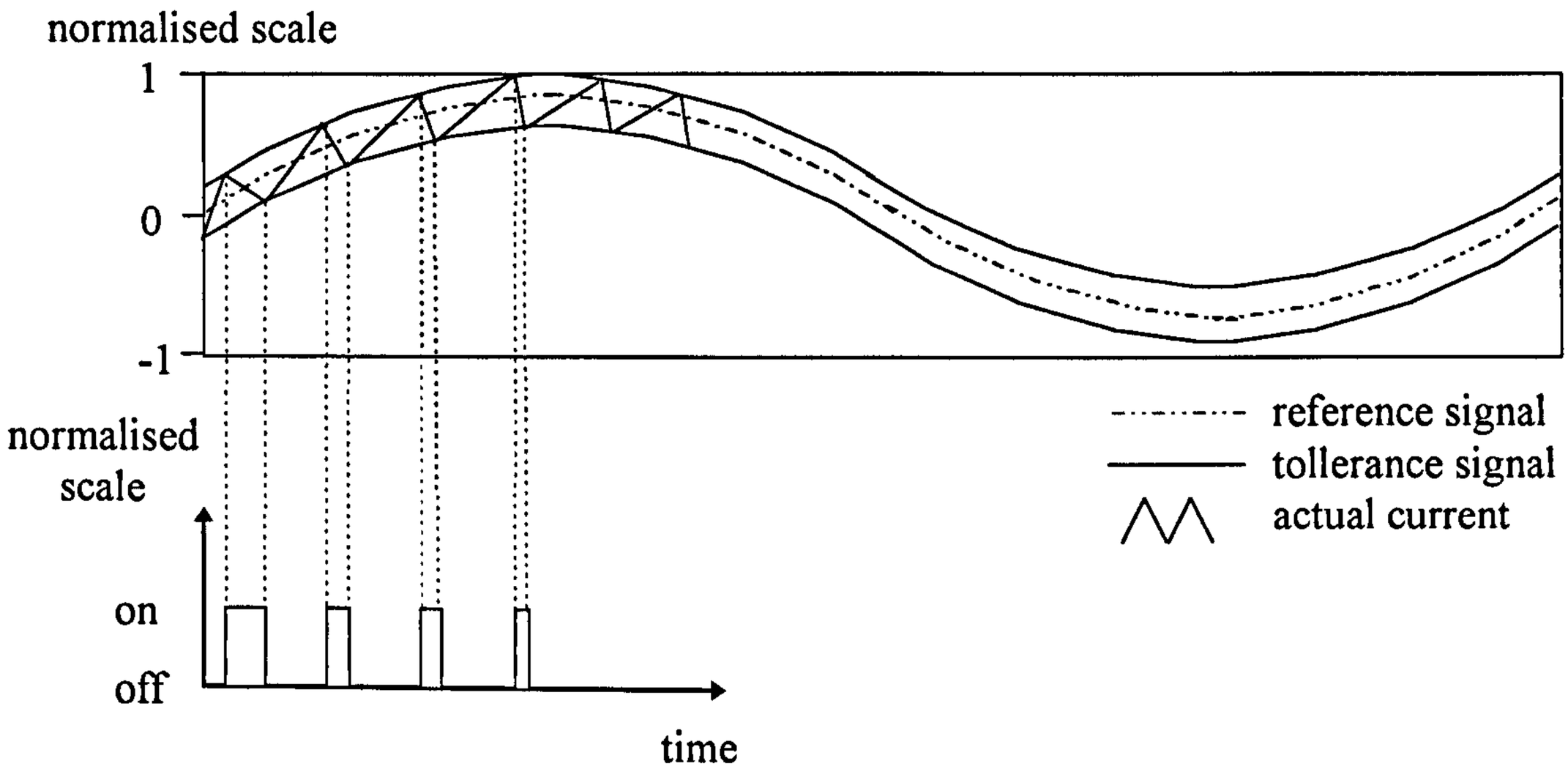


Figure 1.8.5: Hysteresis controller

New advanced current regulators as described in reference [1.29] overcome two major drawbacks of hysteresis control schemes: wide spread of harmonics in output spectral performance and difficulty in protection of the inverter caused by the randomness of switching frequency [1.30]. The new controlled current regulators improved these drawbacks. Further benefits are control simplicity, load parameters change independence, lack of tracking errors and extremely good dynamics [1.26].

A special class of hysteresis controller is the delta modulation controller. Here a sample and hold block is applied to the controller allowing switching frequency limitation to the sampling frequency. This type of regulator has found a wide application in three-phase resonant dc-link converter and is further discussed in Chapter 3.

Chapter 2

CONVERTER TOPOLOGIES

Definition of the term 'converter'

A power electronic converter controls and changes fixed input values of given electrical quantities into load specific output values with the help of a switching arrangement. The electrical quantities are: magnitude of voltage or current, frequency of voltage or current, number of input and output phases and phase delays.

2.1 Classification of Converter Topologies

Most commercial and industrial induction motors are supplied from a three-phase ac power supply. Exceptions may be found for isolated operation drives or in railway applications. However to convert the fixed input values to controlled three-phase output values either amplitude converters or cascaded converters are used. The former converter type uses bi-directional switches inserted in every phase to control the slip of the induction motor. However, characteristics such as poor efficiency and distortion factor problems make them unpopular in induction motor drives [2.1]. The latter converter type is a cascaded system of one or more sub-converters (the definition of a sub-converter is equal to the definition of the converter).

Cascaded converter types are classified according to the link strategy between their sub-converters. Theoretically, only three link strategies are possible: steady (or DC) link, alternating (or AC) link and direct link. Direct link converters connect the input of the power supply straight with the output. This direct AC-AC converter includes only one cascaded sub-converter system. Therefore the terminology converter is used instead of sub-converter.

Direct AC-AC converters may be divided into matrix converters [2.2-2.4] and cycloconverters [2.5] (Figure 2.1.1). Both converter types do not need energy storage elements between the three-phase input and the three-phase output. This allows conversion without changing the voltage or the current waveform and therefore without having additional conversion losses.

The principal of the ac-link converters [2.6 and 2.7] (Figure 2.1.1) is based on a high frequency link between the input and output sub-converters. The high frequency is achieved by a resonant circuit that connects both sub-converters. A controller controls the bipolar switches (12 in both

sub-converters) in such a way that a high frequency power signal flows between the sub-converters. The output sub-converter of the parallel resonant converter (PRC) is a voltage-fed converter and the output sub-converter of the series resonant converter (SRC) is a current-fed converter.

DC-Link converters were already described in Chapter 1. They convert the three-phase input voltage or current into a dc voltage or current by using a rectifier and converting the dc value into three-phase output values by using an inverter. The dc-link converter buffers the energy in relatively large storage elements such as capacitors or inductors.

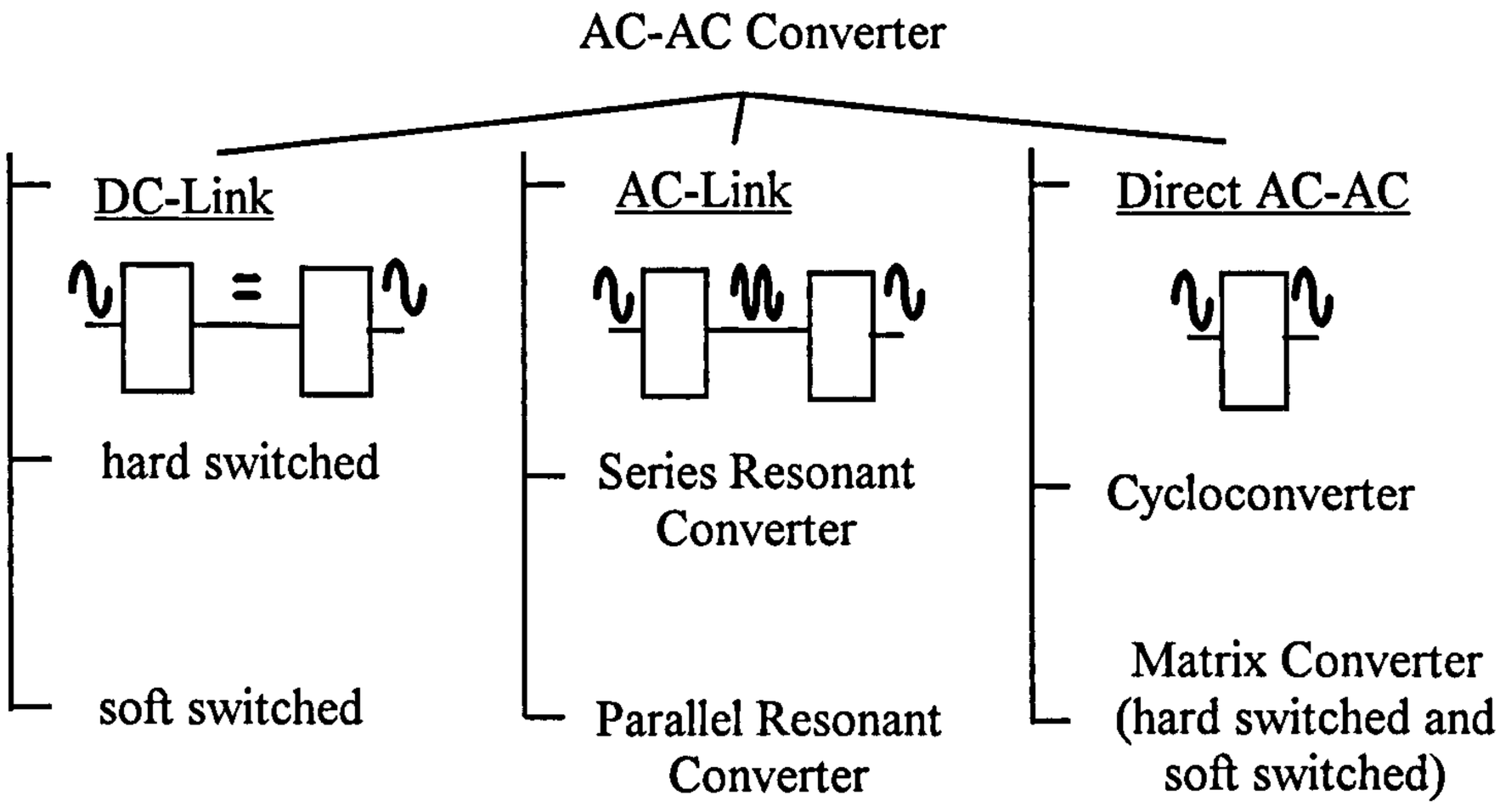


Figure 2.1.1: General family tree of AC-AC converters

Figure 2.1.1 does not show the class of multi-level topologies and they are not further discussed in this thesis. That is because multi-level converters are seen to offer advantages only for very high voltage systems, above 2kV. The highest breakdown voltage for standard IGBTs is classified to 3300V using the thumb rule: twice dc-link voltage is equal breakdown voltage of the device 1600V dc-link can be used. An increase of this voltage can not be handled from a standard device. Thus devices must be connected in series or multi-level converters have to be used. An assessment of different multi-level converters can be found in references [2.8 and 2.9].

2.2 Direct AC-AC Converters

As shown in Figure 2.1.1 direct AC-AC converters can be subdivided into cycloconverters and matrix converters. The matrix converter (Figure 2.2.1) was considered in the late 1970's [2.10] and considerable progress was made by Venturini [2.11]. The converter needs nine bi-directional semiconductor switches to connect each input terminal with each output terminal.

There is no power storage between input and output and therefore no energy store losses. In addition, devices in a matrix converter do not need to be rated as highly as devices in other converter topologies. This is firstly because of the lower reverse voltage drop across the device. The maximum applied voltage across each switch of the matrix converter is equal to the peak value of the line to line voltage of the voltage supply grid. Switches of a dc-link converter have to be at least rated to the 1,35-fold of the peak value of the line to line voltage. Secondly each switch of the matrix converter carries only a third RMS current than a switch that is integrated in dc-link converter. The reason for that is simple. 18 switches of the matrix converter must transfer the same RMS current than six switches of the dc-link converter when assuming a constant current source [2.4]. Nevertheless, bi-directional switches with high power ratings and a fast switching time are not yet available and must, therefore, be realised using a combination of unipolar switches with antiparallel diodes. This consequently increases the cost and complexity of the overall system. Another inherent problem is the change of input and output impedance. In a matrix converter the input must appear as a voltage source whereas the output must appear as a current source (or vice versa). This means the switching function of the converter must ensure that the side that appears as a voltage source is not short circuited and the other side that appears as a current source is not open-circuited. A failure means that voltage sources or current sources with unequal magnitudes are directly connected, creating an unacceptable condition. Other problems are limitation in output voltage to $\sqrt{3}/2$ of the input voltage and protection problems [2.11].

However, the matrix converter has attracted more and more researchers in academic and industrial fields, principally it offers the potential to have a 'one silicon block' converter with no additional passive components (although in practice an input filter is required).

Although the devices in a matrix converter usually operate under hardswitching conditions, softswitching techniques can also be applied. Reference [2.12] use additional components to achieve softswitching techniques in the megawatt power range. Six additional switches and several passive components are needed. An easier way of achieving softswitching techniques is reported in reference [2.4]. Here a defined control pattern is used allowing natural soft current commutation without any additional devices.

Future prospects for matrix converters will depend largely on improvements in silicon device technology. If the semiconductor industry can produce and manufacture a 'one silicon block' converter, the initial cost of a matrix converter will be reduced significantly compared to today's hard switched dc-link converters.

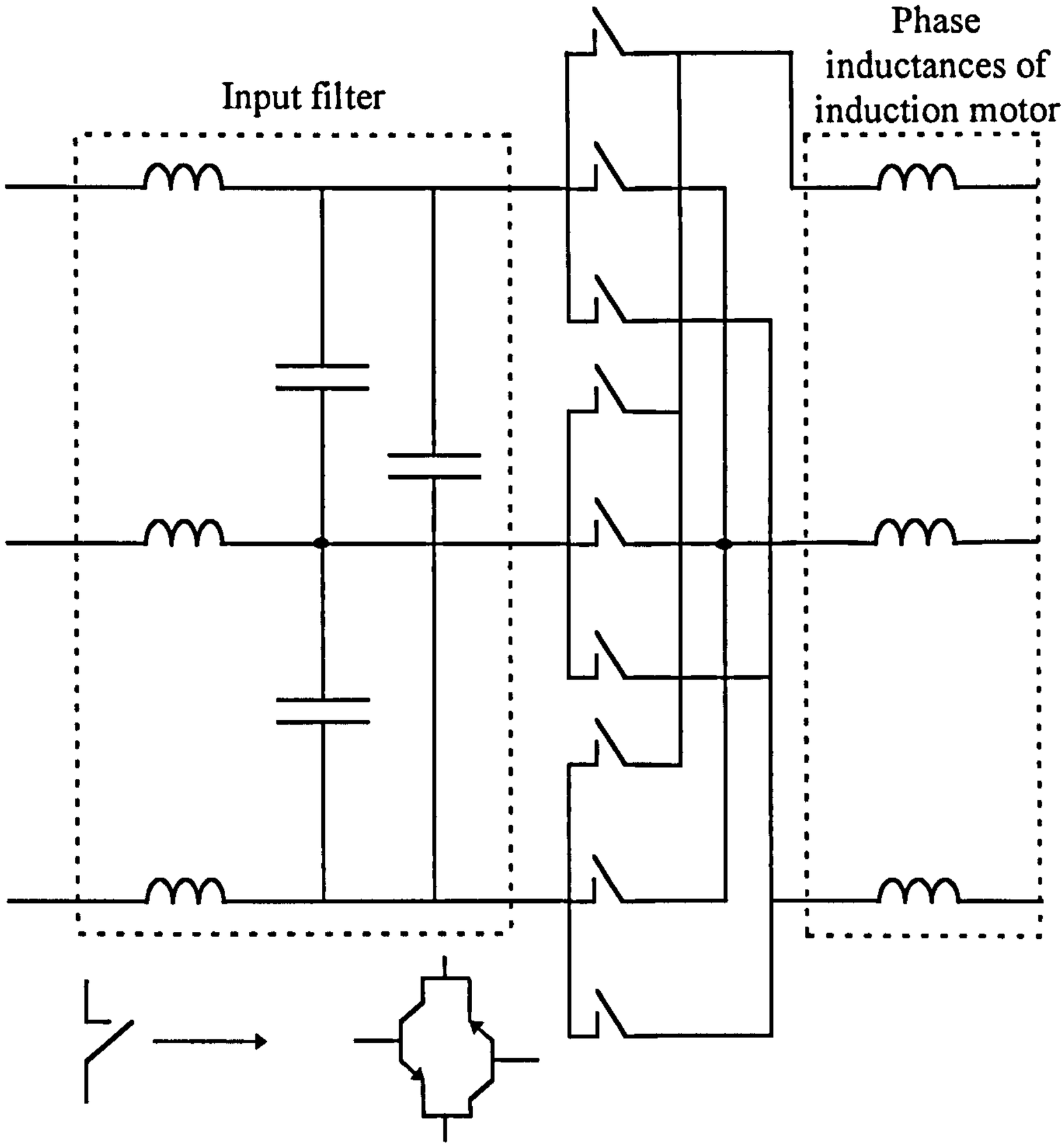


Figure 2.2.1: Matrix Converter

Cycloconverters are realised by the parallel connection of three Direct DC-Link Converters. Isolation between every sub-converter is done by transferring reactors (Figure 2.2.2) between them to prevent short circuit situations and limits circulating current caused by harmonics. The output frequency varies between 0Hz and above the input frequency. Because cycloconverters only operate economically in large power applications when phase-controlled, the output frequency is limited to one third of the input frequency. The frequency limitation is necessary to minimise the line output distortions when using phase-control techniques [2.1].

The firing angle of each phase group is modulated sinusoidal to fabricate a mean sinusoidal voltage. The other phase groups are identical except phases shifted by 120°. A minimum of 18 unipolar devices are necessary for a cycloconverter, but cycloconverter using 36 or more devices are reported to increase the power rating. Although cycloconverters were the first converter topology, today its applications are limited to heavy drives applications, constant frequency applications or voltage stabilisation of transmission and distribution lines [2.1].

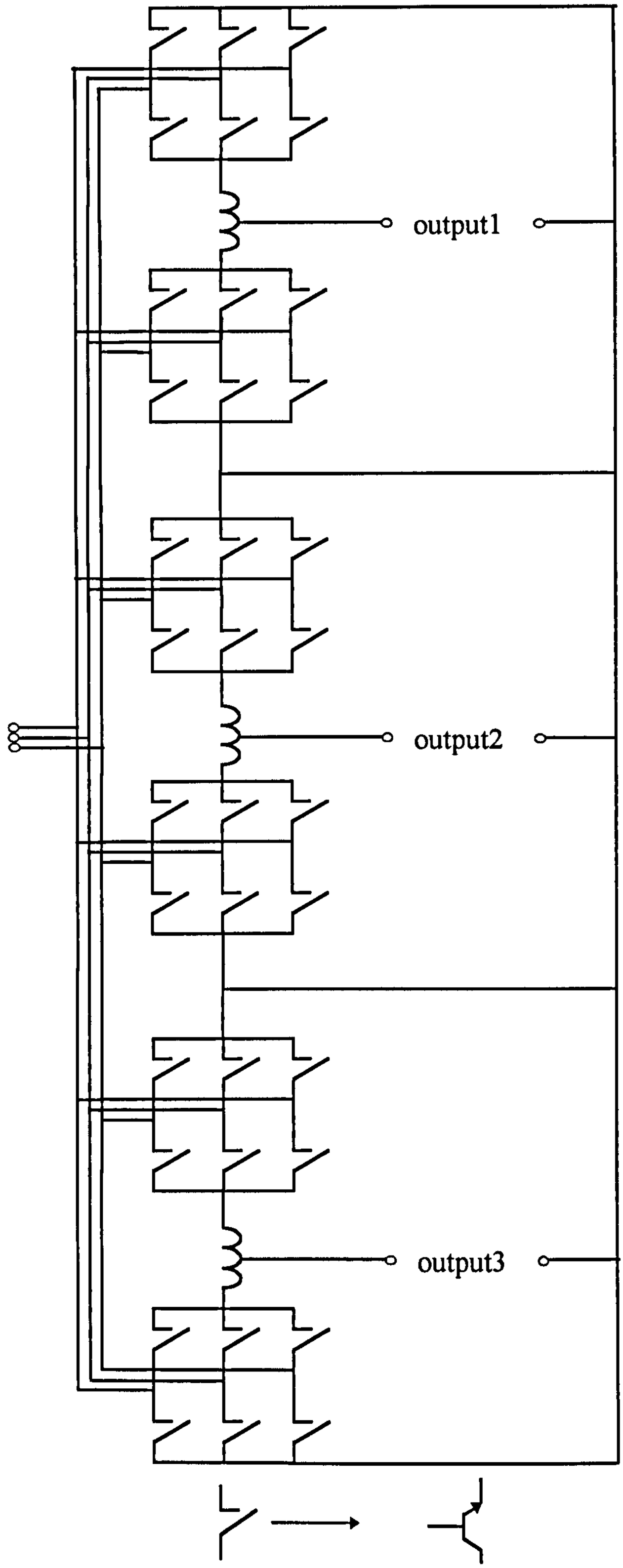


Figure 2.2.2: Cycloconverter

2.3 AC-Link Converters

A Series Resonant Converter (SRC) [2.13 and 2.14] is shown in Fig. 2.3.1. The SRC belongs to the current-fed converter type and each of the input supply lines is connected via a high-frequency filter (capacitors) to a four-quadrant controlled sub-converter. The sub-converter generates with the output sub-converter a modulated single-phase high-power frequency carrier current. This carrier current is than selectively converted by the output sub-converter. The high-frequency content is removed by a high-frequency output filter. The result is a low-frequency three-phase output current.

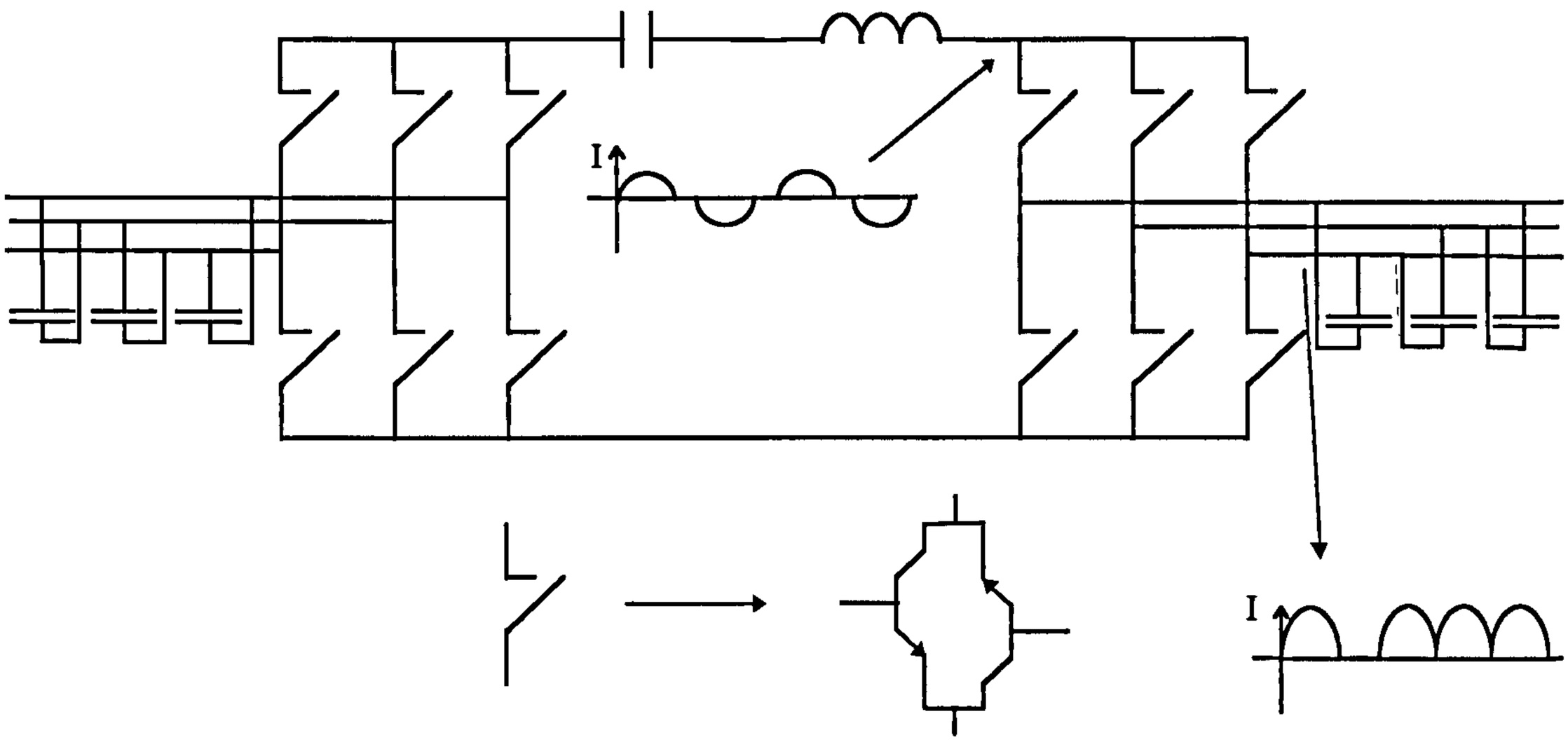


Figure 2.3.1: Series Resonant Converter

The resonant elements in the SRC carry the main power, which leads to high losses and is, therefore a major drawback of this converter type. The benefit of the series link configuration is that switching occurs at zero-current, allowing easy use of thyristors as power devices.

The parallel Resonant Converter (PRC) [2.15] works in a similar way, except that the PRC is a voltage-fed inverter and generates a modulated single-phase high-frequency carrier voltage. This carrier voltage is achieved by using a resonant circuit parallel to both sub-converters.

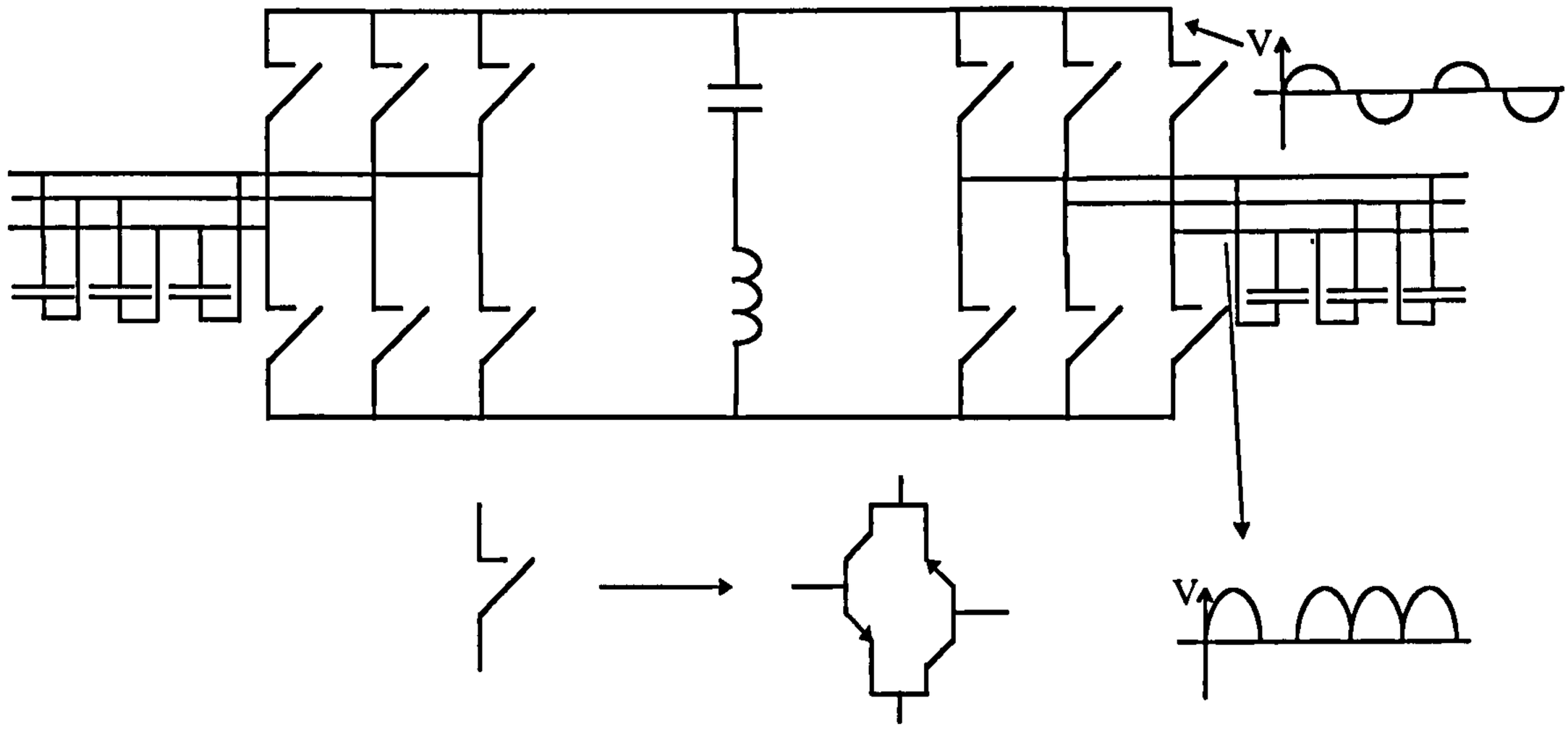


Figure 2.3.2: Parallel Resonant Converter

The PRC has the advantage that resonant elements are not in the main power path. For that reason, the resonant components may have lower ratings than the main devices and will introduce relatively small losses into the system. Problems with the PRC occur by having an imbalance between the input and output current. In this case it is difficult to balance the link energy [2.16] resulting in the resonant circuit becoming over-excited (voltage reaches unacceptable high levels) or under-excited (resonant voltage collapses) [2.16].

In the same manner as the matrix converter, both ac-link converters need bi-directional switches. Again unipolar switches have to be used, which increase the number to 24 unipolar switching power devices and 24 antiparallel diodes. In addition to the high number of devices, ac-link converters always need input and output filters. In an effort to reduce the number of devices modified circuits have been suggested to halve the number required [2.17 and 2.18], but power factor control seems to be unattainable [2.17] and a reduction of the line-to-line voltage by factor of $\sqrt{3}$ limits the application areas [2.19]. Nevertheless, applications for ac-link converters are reported: for example in variable-speed generation to excite rotor windings of a doubly-fed generator [2.20]. The ac-link converter should prove to be a viable alternative to other converter topologies in the near future when bi-directional power devices become readily available.

2.4 DC-Link Converters

DC-Link converters use relative large energy storage elements to buffer reactive power. Figure 2.1.1 shows that dc-link converters are sub-divided into hard switched and soft switched dc-link converters which are introduced in the following two sections.

2.4.1 Hardswitching DC-Link Converters

The hardswitching converter has already been discussed in Chapter 1. This section shows the hardswitching dc-link converter again only for completeness (Figure 2.4.1). Table 2.4.1 summarises the drawbacks of this topology.

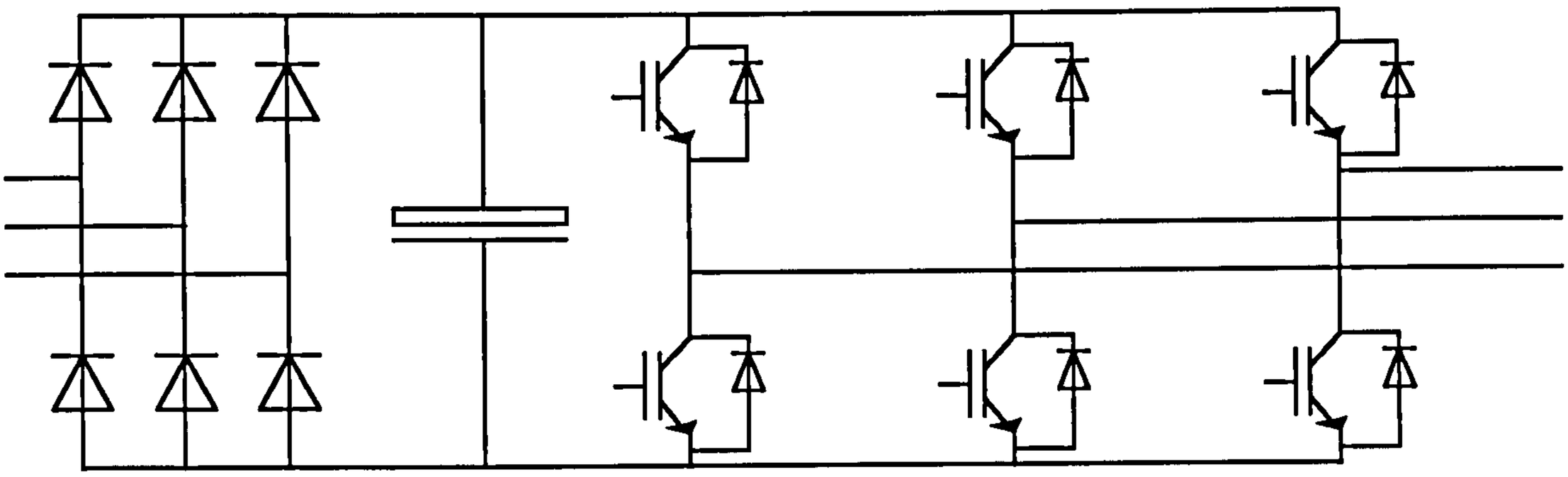


Figure 2.4.1: Toady's standard converter type in drives applications

	PROBLEM	CONSEQUENCE
switching frequency	operational switching frequency is limited, because switching losses increase proportional with switching frequency	limited drive performance, problems with torque pulsation, relative slow response time, windings heating, acoustic noise problems
switching losses	overlapping of dc-link voltage across the device and load current through the device	limitation in converter efficiency, need of relative large heatsinks increase weight and size
transition speed	to reduce losses high transition speed is needed	EMI problems, damage on motor isolation

Table 2.4.1: Inherent drawbacks of hardswitching six-bridge voltage-fed converters

The drawbacks summarised in Table 2.4.1 are becoming more important in growing markets such as servo drives. Servo drives are usually applied to a high performance variable speed drive, which often has the ability to control position as well as speed. Servo drives offer the highest performance of common drives systems, with a typical torque bandwidth of 1000Hz [2.21]. As a result they require a high switching frequency, good output spectral performances and low torque ripple. It has been estimated by Frost and Sullivan that the world wide market

for servo drives will be worth $ 1813 million in 1999 [2.22]. It is therefore worth investigating possible solutions to the limitations of the hard switched inverter.

2.4.2 Softswitching DC-Link Converters

Softswitching converters claim to overcome the problems of hardswitching converters. Softswitching converter allow reduction in switching losses, by forcing either current or voltage to zero before the switching event occurs. Thus higher switching frequencies can be achieved leading to better drive performances. In addition dv/dt stress and di/dt stress can be controlled, because of the use of defined resonant components (LC-circuit). EMI is therefore controllable. In the following some examples are given, describing fields of application for softswitching.

The idea of using resonant circuits for power conversion is not new and goes back to the earliest days in the evolution of power electronics. At this time thyristors were the principal type of device employed and turn-off was achieved only when the current flowing through the thyristor reached zero. Since natural commutation techniques limit the range of converter topologies that may be implemented, forced-commutated circuits were introduced. Force commutated converters use additional auxiliary thyristors and additional passive components such as capacitors and inductors to resonate the current flowing through the thyristor to zero [2.23].

Another application of resonant circuits in power electronics lies in induction heating [2.24]. Here an inductive load is connected in parallel to a capacitor, creating a parallel resonant circuit. The switches of the converter excite the load and the thyristors are commutated by resonance of the load current (load commutation).

As already mentioned GTO devices need RCD snubber circuits for voltage protection and the energy dissipation in the resistor leads to bad efficiency. To increase the efficiency regenerative circuits were introduced to transfer the stored switching energy of the snubber back to the supply [2.23]. Again resonant circuits were needed to shift the energy away from the snubber circuits.

Another example of integration of LC combinations was the development of high frequency link converters (HF-converter) [2.25-2.27]. HF-converters are the predecessor of the ac-link converters. A resonant circuit and an excitation converter are inserted between two sub-converters (one input and one output sub-converter). The excitation converter is of a lower power rating than the sub-converters and is needed to start up the voltage oscillation in the

HF-circuit. HF-converters have found application in dc-dc conversion and in power transmission over 1MW.

In the past softswitching circuits took their course for load resonant converters. Here the load (LC circuit) provides already all elements for the energy transfer. In some load application it is easy to add one missing resonant component onto the load i.e. either L in case for high-frequency fluorescent lightning [2.5] or in case for induction cooking [2.5]. In induction motor drives however the load is determined by the inductance of the motor windings and a build-on of capacitors on a standard motor is unlikely. Therefore the hard switched dc-link topology using gate turn-off devices gained more and more acceptance in drives, simply because of easy design, limited control complexity and robustness.

A mile stone in the development of softswitching was the publication from Prof. Divan [2.28]. 1986. This paper describes the first softswitching dc-link converter: the resonant dc-link inverter (RDCL, Figure 2.4.2). The RDCL is typified by a single resonant tank, inserted into the dc-link, which must undergo a resonant transition each time any inverter leg changes its switching state. From that many other topologies followed. In the last twenty years of development of softswitching topologies two other important papers have been published that have to be cited, because of their impact on novel topologies.

While the inverter input voltage of the converter based on Prof. Divan's oscillates continuously, Prof. Malesani designed a RDCL topology that allows only resonant oscillations if the inverter changes its switching status [2.29]. This was a major step especially for the controllability of the RDCL. The converter type has been later called quasi resonant dc-link converter (q-RDCL). Both types are discussed in detail in Chapter 3.

Prof. DeDoncker published his pole commutated inverter (PCI) [2.30] in 1990. By way of contrast, every pole (or leg) has its own resonant circuit which undergoes a resonant transition at every switching instant of that leg (Figure 2.4.2). As it happened for RDCL many sub-topologies on PCI have been also proposed. Some of them are discussed in Chapter 4.

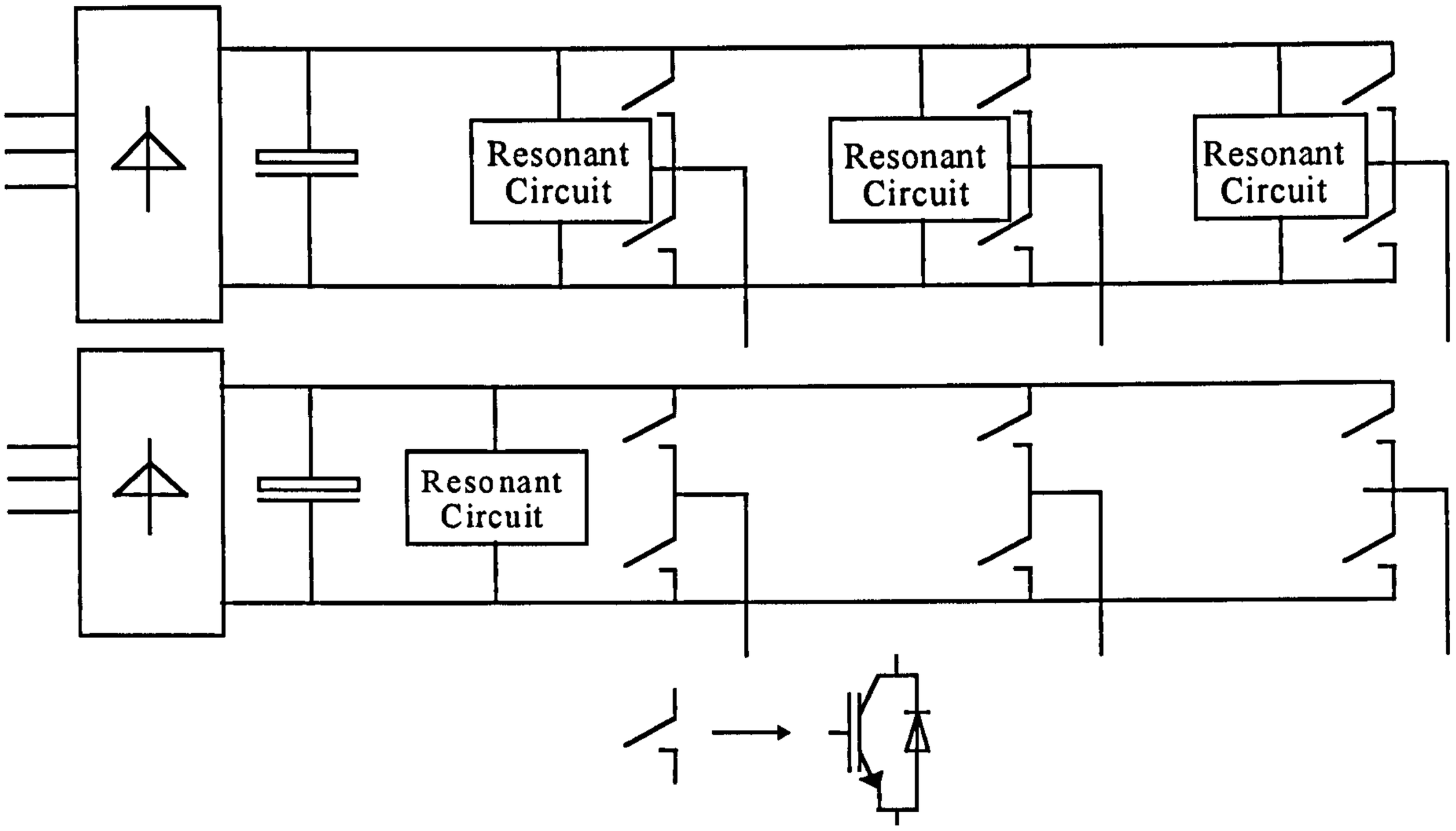


Figure 2.4.2: Comparison pole commutated inverters (top) and resonant dc-link inverters (bottom)

In view of the high number of the different published topologies a family-tree summarises the main topologies and show the link to each other (Figure 2.4.3).

PCIs, which require a larger number of active and passive components than their RDCL counterparts, can be divided into resonant pole commutated inverters (RPI) and auxiliary resonant pole commutated inverters (ARPI). The RPI topology does not need an additional switch to achieve zero voltage or zero current switching, whereas the ARPI needs support from one or more auxiliary switches..

The RDCL group is subdivided into two sub-groups: basic resonant dc-link inverters (basic RDCL) [2.28], and parallel resonant dc-link inverters (PRDCL) [2.31] (Figure 2.4.3). In the basic RDCL topology, the inverter is connected to the reservoir capacitors via an inductor. As this effectively decouples the inverter leg voltage from the fixed reservoir voltage, some form of clamping is usually applied to prevent high voltage transients being applied to the inverter switches. This is reflected in the modified topologies of the active clamped (ac) and passive clamped (pc) basic RDCL inverters.

The principal feature of all PRDCL inverters is the series device in the dc-link. When the switch is closed, the dc link voltage is applied to the inverter. When the switch is opened a resonant transition occurs allowing zero voltage switching of the bridge switches.

PWM techniques are well established in induction motor drives and are, therefore, a desirable feature of any proposed converter topology. All PCIs and PRDCL inverters meet this aim to some degree and the basic RDCL inverter can be PWM controlled with the aid of auxiliary circuits (ACs). Figure 2.4.3 shows the principal circuits of PWM controlled RDCLs, often referred to q-RDCLs [2.29, 2.32-2.37]. The number of the different arrangements of the ACs is large and Chapter 3 explains some of them. Figure 2.4.4 gives two of possible auxiliary circuit arrangements.

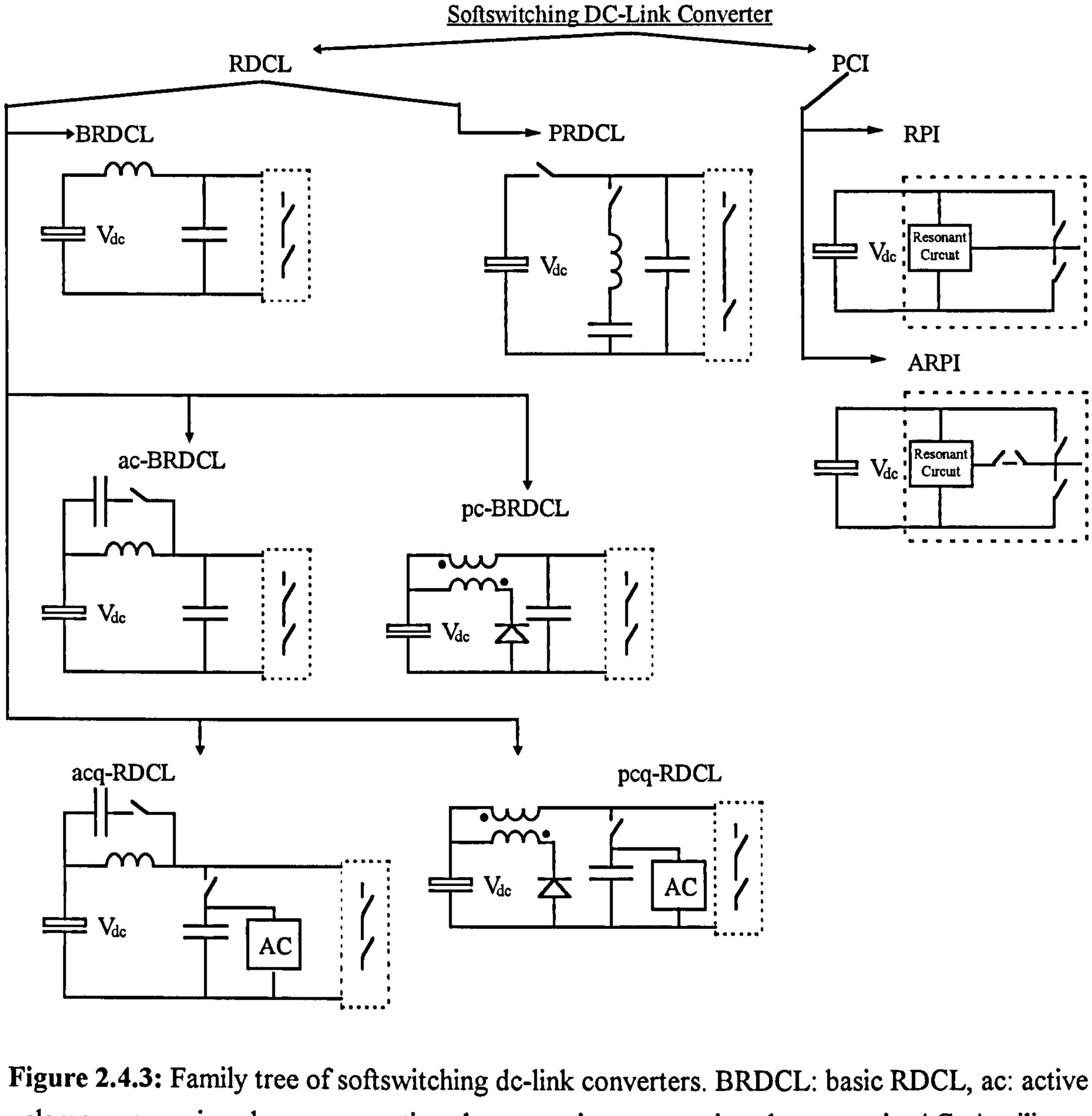


Figure 2.4.3: Family tree of softswitching dc-link converters. BRDCL: basic RDCL, ac: active clamp, pc: passive clamp, acq: active clamp quasi-, pcq: passive clamp quasi-, AC: Auxiliary Circuit. The circuitry shown in the dotted square appears three times

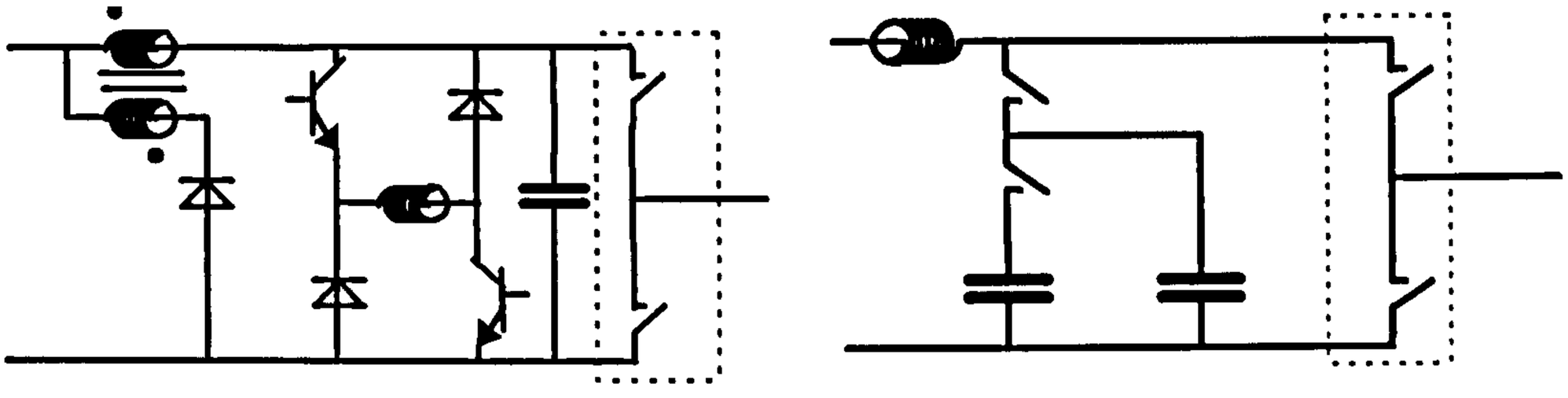


Figure 2.4.4: Two examples of possible auxiliary circuit arrangements in quasi RDCL converters. Left: passive clamp quasi-RDCL [2.38]; Right: active clamp quasi-RDCL [2.39]

All the various converter topologies shown in Figure 2.4.3 claim to overcome the drawbacks of hardswitching converters. Table 2.4.2 summarises the characteristics and claimed benefits of softswitching dc-link topologies.

	CHARACTERISTICS	CLAIMED BENEFITS
switching frequency	higher	better output spectral performance, no audible noise
switching losses	lower	higher efficiency, smaller heatsinks
dv/dt stress	lower	lower stress on motor isolation, less EMI problems, smaller output filters
snubber ?	no	less amount of passive components
size and weight	smaller and lighter	less package problems
cost	additional components and devices but smaller heatsinks and filters	Reduction in cost of heatsinks and filters outweigh cost of components and devices

Table 2.4.2: Characteristics and claimed benefits of resonant converters compared to the hardswitching dc-link converter

2.5 Comparison between the three major AC-AC Converter Topologies

The list of desirable features identified in section 1.6.3 may be used as the basis for a comparative assessment of novel converter topologies Table 2.4.3 summarises a qualitative comparison of the different topologies compared to the hardswitching dc-link converter. It should be stressed, however, that at power ranges under 100kW, cost is by far the most important single factor in determining the choice of topology. In this power range converter circuits are mass-produced and every small increase in cost must be outweighed by a large increase in performance.

	SOFTSWI. DC-LINK	AC-LINK	SOFTSWI. MATRIX CONVERTER	DIRECT AC-AC
reduction in output filter	+	-	+	0
higher switching frequencies	++	++	++	-
reduction in dv/dt stress	++	++	++	-
reduction in size and weight	0	-	--	-
reduction in heatsink size	+	0	-	--
switching frequency outside audible noise	+	+	+	0
reduction in output spectral performances	++	+	+	-
low number of devices	-	--	--	--
elimination of dc-link capacitor	0	++	++	++
less maintenance work	0	+	+	+
easy manufacturing	-	+	-	-
high reliability	-	--	--	--
low cost	0	--	--	--

Table 2.4.3: Vague comparison of various converter topologies compared to the hardswitching dc-link converter based on demands on drives applications. (++ well enhanced, + improved, 0 no improvement, -less beneficial, --worse)

One benefit of both, ac-link converter and direct AC-AC converter, is the elimination of the large dc-link capacitor essential in the dc-link topology. This capacitor can cause problems because of its limited life performance, its size and its cost. In addition, the missing link arrangement (direct AC-AC) or the small link arrangement (ac-link) improves

manufacturability. Input and output filters are, however, required for these topologies, which increases both weight and size. In spite of the significant gains to be made in eliminating the dc link, the additional costs of bi-directional switches make the ac-link converter and direct AC-AC converter unattractive. At the moment, bi-directional switches are not available thus unipolar devices must be used. This increases the overall cost and diminishes reliability. Both converter topologies need at least twelve switching devices more than the hardswitching dc-link converter with uncontrolled rectifier. In addition more driver circuits are needed and a much more complex control structure has to be implemented increasing further the initial cost.

Table 2.4.3 shows that softswitching dc-link converters are expected to display similar performance when compared to their ac counterparts. Given that the costs of a dc link inverter and uncontrolled rectifier will always be much lower than those of any ac link or direct AC-AC topology, there is little doubt that the dc-link inverter is the preferred topology. For this reason, ac-link converters and direct AC-AC converters are unlikely to be commercialised in the 1kW-100kW power until cost effective bi-directional switches can be implemented. Therefore neither converter types will be discussed further in this thesis. If cost effective bi-directional devices do become available then the matrix converter might have sufficient economic leverage to penetrate the drives market in this power range.

To conclude this chapter one can say that the softswitching dc-link converter is the only promising topology for induction motor drives application up to 100kW. The next three chapters review the number of variations in softswitching dc-link topologies, describe their operation modes and summarise the different topologies in terms of cost, losses and stress. Chapter 3 introduces RDCL topologies whereas Chapter 4 analysis PCI topologies. Chapter 5 assesses all the various topologies and suggests the most promising softswitching dc-link converter.

Chapter 3

RESONANT DC-LINK INVERTERS

This chapter analyses various RDCL topologies. It describes the principals and theories of the different circuits and investigates their performances using PSPICE simulation. In keeping with the requirement for a low initial cost, only those circuits using less than two active devices and a low number of passive components were taken into account. The simulation results are presented in Appendix A.

The study of each topology is based on an introduction of a simplified circuit followed by a step by step analysis of each individual operation mode. To develop an equivalent circuit the following assumptions have been made:

a) The dc-link capacitor is larger than the resonant capacitor thus the input side can be simplified by a constant dc voltage source (V_{dc}). For clarity the inverter input voltage is written as V_{inv}.
b) The resonant transition occurs only during a very short period of time. As a result the individual phase currents can be assumed to remain constant during this time.
c) The motor inductance is much greater than the resonant inductor of the inverter. Given that assumption, the inverter and the load can be simplified by using a switching device (S), a diode (D) and a current source (I_{load}). The current source I_{load} remains constant during the switching period and depends on the individual phase currents and the state of all six inverter devices.
d) All components are ideal except where specifically noted.

3.1 Basic Resonant DC-Link Inverter (basic RDCL)

The basic RDCL [3.1 and 3.2] with its equivalent circuit is shown in Figure 3.1.1. A resonant inductor (L_r) and resonant capacitor (C_r) are inserted between the dc-link capacitor and the inverter. The LC combination allows the inverter input voltage (V_{inv}) to resonate. Once the voltage V_{inv} is equal to zero a change in the switching status of the inverter is enforced under zero voltage conditions.

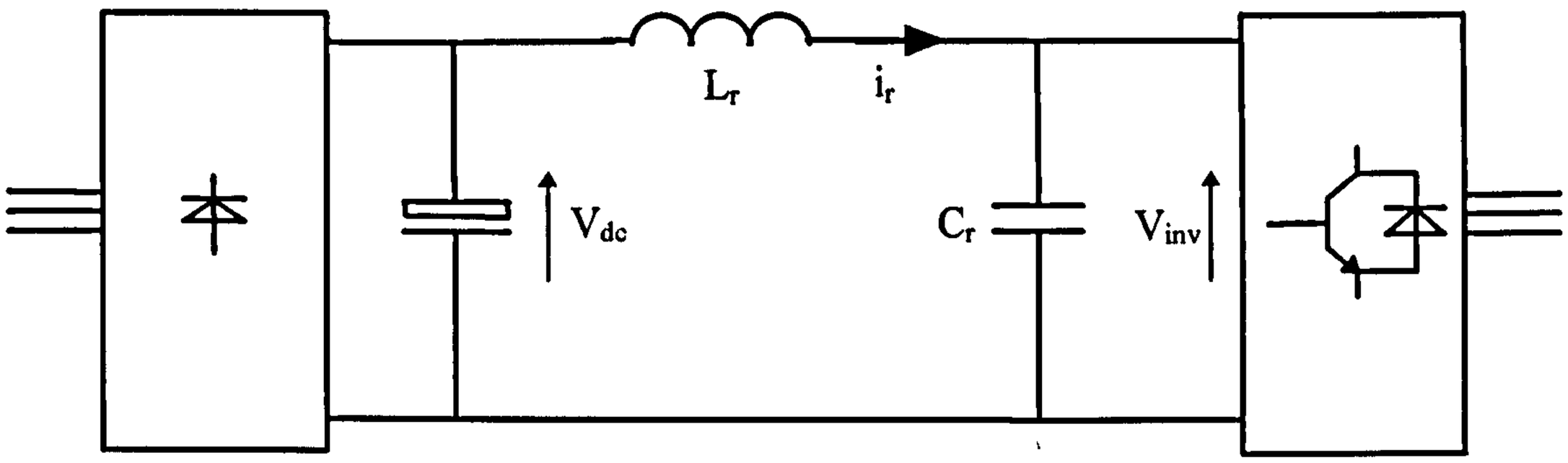


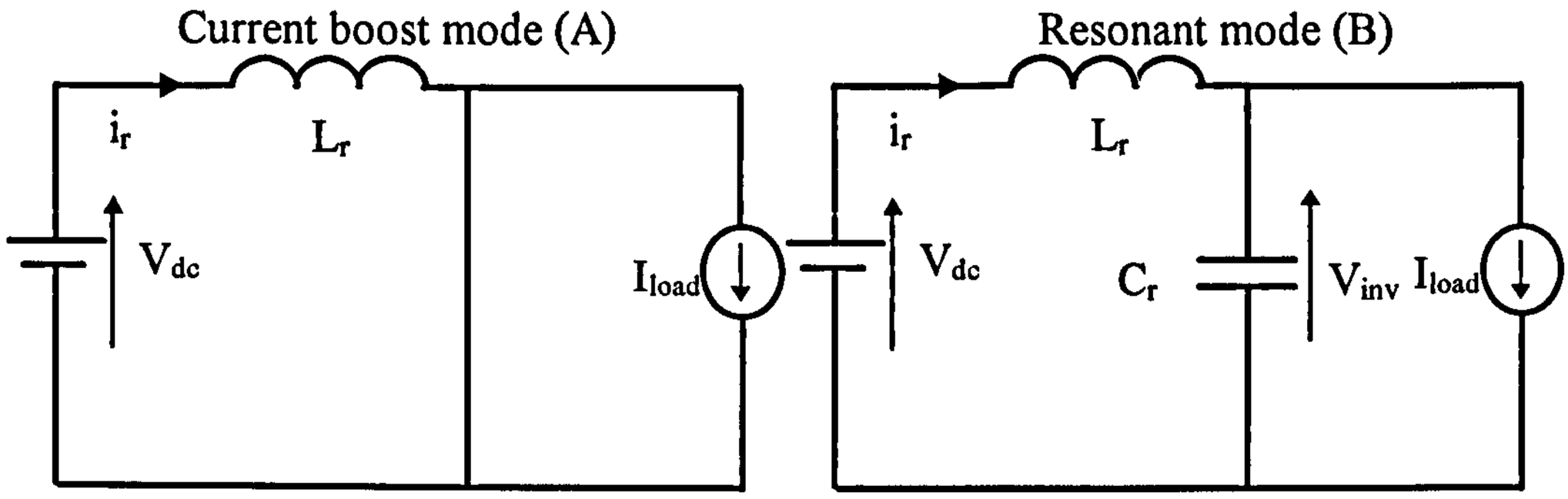
Figure 3.1.1: Schematic and equivalent circuit of the basic RDCL

3.1.1 Operation Modes of the basic RDCL

The basic RDCL operation can be divided into two operation modes (see Figures 3.1.2 and Figure 3.1.3).

Current boost mode (A): When the switch S is conducting, the inductor L_r is clamped across the dc-link. Thus the resonant current (i_r) ramps-up allowing L_r to store enough energy for the resonant cycle. Once i_r reaches the threshold I_{r1} switch S opens (I_{r1} is a function of the losses in the system and the load current).

Resonant mode (B): The voltage source V_{dc} is used to resonate the LC network. The oscillation of this network gives rise to instants of zero voltage. Once the voltage V_{inv} is zero the antiparallel diode D conducts and S can switch on under zero voltage conditions. When the current i_r reverses switch S starts to conduct and a new current boost mode starts.



$$V_{inv}(t) = 0V \tag{3.1.1}$$

$$i_r(t) = I_{load} + \frac{V_{dc}}{L_r}t \tag{3.1.2}$$

$$V_{inv}(t) = V_{dc}(1 - \cos\omega_0 t) + + Z_0(I_{r1} - I_{load})\sin\omega_0 t \tag{3.1.3}$$

$$i_r(t) = I_{load} + \frac{1}{L_r}\int(V_{dc} - V_{inv}(t))dt \tag{3.1.4}$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{3.1.5}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{3.1.6}$$

I_{r1} is the remaining current stored in the inductor L_r after the switch S is turned off.

Figure 3.1.2: Operation modes A and B of the basic RDCL

As shown in Figure 3.1.2 each individual operation mode is expressed with equations describing the inverter input voltage V_{inv} and the resonant current i_r. Equations 3.1.5 and 3.1.6 describe the typical characteristic equations of any resonant circuit: resonant frequency ω_0 and resonant impedance Z_0. Both equations are determined only by L_r and C_r. From both equations it can be shown that by keeping the value L_r constant and decreasing the value of C_r the resonant frequency and impedance increases. When keeping the value of C_r constant and decrease the value of L_r than the outcome is a higher resonant frequency but a decreased resonant impedance.

The resonant frequency ω_0 is related to dv/dt and di/dt stress on devices and passive components. A high resonant frequency may destroy underrated devices or damage isolations on capacitors and inductors. In addition EMI problems start with high dv/dt and di/dt stress. The resonant impedance Z_0 is an indicator of voltage and current peak stress. In addition a low impedance results in an unsuccessful resonant oscillation meaning that voltage or current does not reach the zero level. This is explained with the help of equation 3.1.3. The voltage V_{inv}

does not reach zero when the absolute value of the second term is smaller than the absolute value of the first term. That is the case when Z_0 is too low.

Both equations (3.1.5 and 3.1.6) show that resonant converter designs have to compromise between stress in voltage peak, stress in current peak, voltage transition time and current transition time.

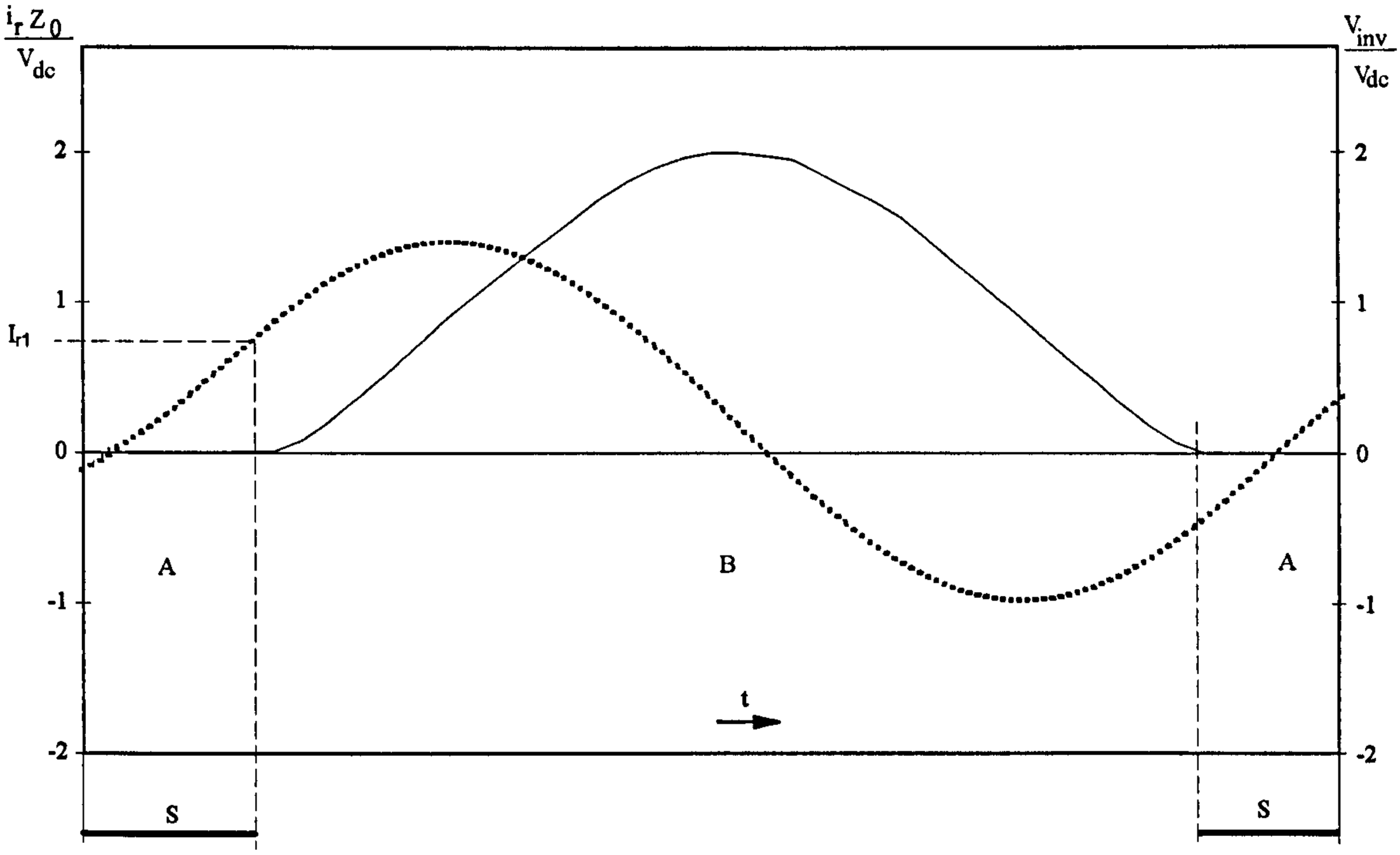


Figure 3.1.3: Normalised waveforms V_{inv} (solid line) and i_r (dashed line) over one cycle of resonant period of the basic RDCL

Since the link waveform is periodic and nearly sinusoidal, the interval between allowed switching times is fixed by the link frequency and the output must be synthesised from discrete pulses. This means that well-established modulation techniques such as PWM are not suitable. The following section describes optimised control techniques for the basic RDCL.

3.1.2 Discrete Pulse Modulation Techniques (DPM)

To control the basic RDCL discrete pulse modulation techniques have to be applied. Classical techniques for discrete pulse generators are: the linear delta modulator and the sigma delta modulator. More unconventional modulators are the exponential sigma delta modulator, current regulated delta modulator, modified sigma delta modulator and adjacent state current regulator [3.3-3.7]. In addition, fuzzy logic and neural networks have also been applied on

pulse modulation techniques as shown in reference [3.8]. Considering the varieties of these control schemes only the two classical control systems are further discussed.

Figure 3.1.4 shows the block diagram of the linear delta modulator [3.9]. The modulator encodes a band-limited analogue input signal, into a two-level output. The output binary waveform is fed back through an integrator and compared with the reference signal. The error signal is quantised into one of two possible levels depending on polarity. The output signal of the quantiser is regularly sampled by the link frequency signal (detecting zero volts across the inverter input) to produce a binary code for the inverter switches.

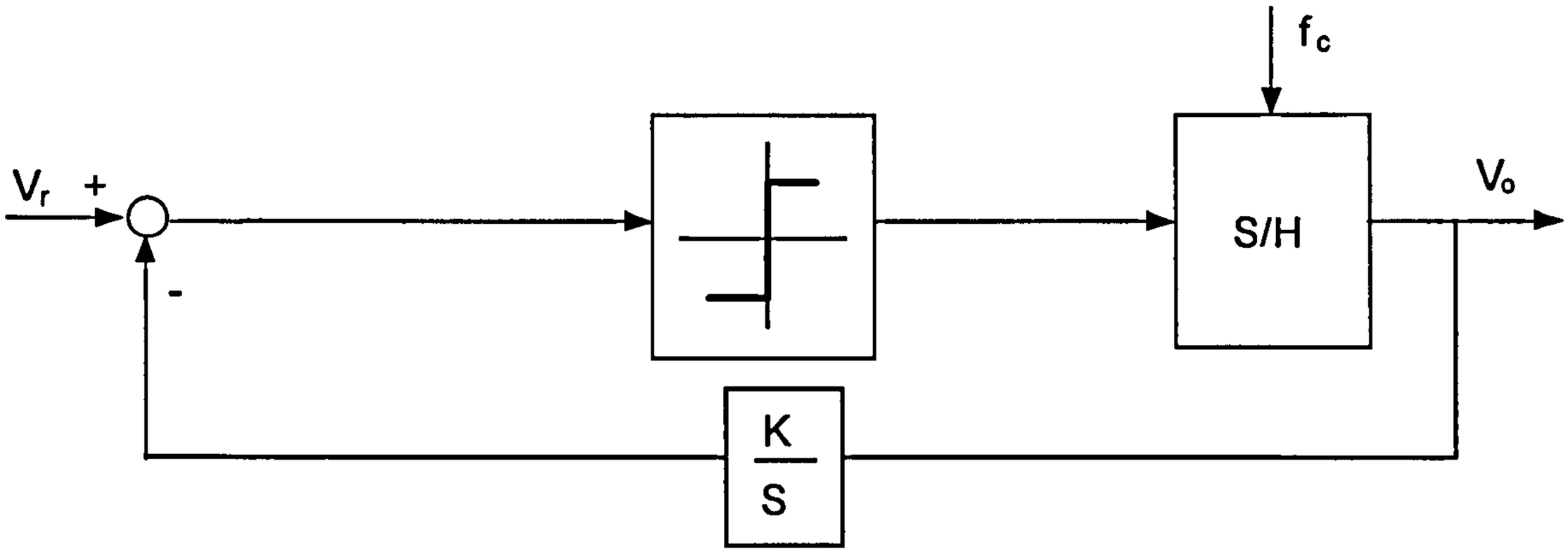


Figure 3.1.4: Block diagram of a linear delta modulator

The block diagram of the sigma delta modulation is shown in Fig. 3.1.5. This control scheme is implemented by calculating the difference between output voltage and the voltage reference resulting in an error. This error function is integrated and dependent on the sign of the integrator output the switching signal generates. The synchronisation of this signal to the resonant link frequency is done again by a sample and hold (S/H) term.

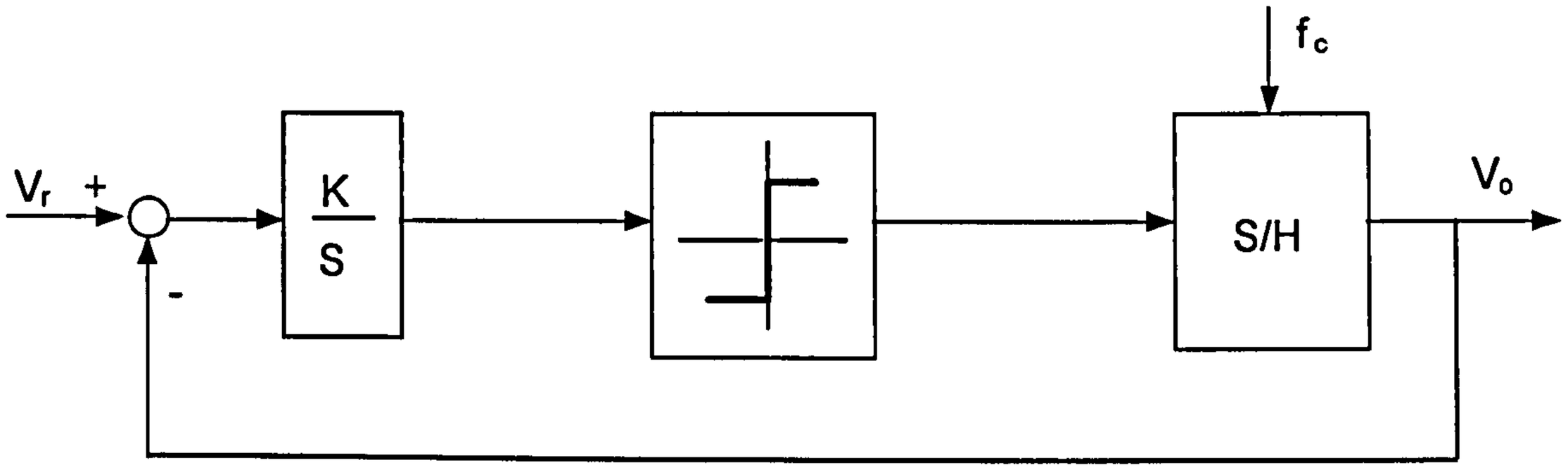


Figure 3.1.5: Block diagram of a sigma delta modulator

A comparison of different delta modulation controllers is given in references [3.3, 3.6-3.8, 3.10]. From most interest is thereby the results of the output spectral performance between

PWM controlled hard switched inverters and delta modulated resonant dc-link inverters. That is because delta modulated controlled hard switch converters were well known for their spread spectrum in the voltage output spectral performance. References [3.6 and 3.7] compared the output spectral performance between PWM controlled inverters and delta modulated resonant dc-link inverters. The authors describe that given a tenfold increase in link frequency, a delta-modulated resonant link-type inverter will show an improvement in voltage harmonic distortion over an equivalent hard switched inverter employing PWM. This improvement is of the order of three times. However, because of the inherent wide spread of the voltage output spectrum when applying delta modulation techniques, low-frequency voltage harmonics are significantly higher compared with PWM control techniques and are difficult to remove. Reference [3.10] compared both inverter types concerning the total current output harmonic distortion (THDi). It was shown, that the PWM controlled hard switched inverter shows lower THDi values in the low current range compared to its counterpart, and similar THDi values in the higher current range.

Even modified modulation techniques as mentioned before could not significantly improve the voltage or current harmonics in the lower frequency spectrum range [3.3-3.7]. These unsatisfactory results lead to the conclusion, that resonant converters driven by DPM control do not improve the drive performance.

3.2. Clamp Basic Resonant DC-Link Inverter (clamp basic RDCL)

A significant problem of the basic RDCL is the periodical voltage over shoot from the input voltage of the inverter. Thus, seen from the devices in the inverter, every device must be capable of at least double the dc-link voltage under steady state conditions. However, under transient conditions, when instantaneous power flow reverse and dc link switches and current flows back to the dc supply, a one-cycle transient is obtained where peak voltage stress occurs during the resonant cycle, exceeding the steady-state values [3.11]. To constrain the steady-state and transient stress, techniques have been developed to clamp the inverter input voltage to a certain percentage of the dc-link voltage. This can be done by either an active clamped circuit or a passive clamped circuit.

3.2.1 Principles of the active clamp basic RDCL

The circuit schematic of the active clamp basic RDCL inverter [3.11-3.13] is similar to the basic RDCL discussed in section 3.1. Figure 3.2.1 shows that additional elements are the clamp switch (S_{clamp}), the clamp diode (D_{clamp}) and a pre-charged capacitor (C_{clamp}). The latter is larger than the resonant capacitor C_r but smaller than the dc-link capacitor. In a manner similar to the

basic RDCL the dc bus is shorted to allow a pre-charging of the inductor L_r. On releasing the bus short, the link voltage resonates towards its natural peak. Instead that of V_{inv} overshooting to twice the dc-link voltage, V_{inv} gets clamped to a certain level. This level is determined by the clamp factor (k), where k results from the voltage across the pre-charged clamp capacitor C_{clamp}, and the dc-link voltage V_{dc}. Once V_{inv} reaches the voltage (kV_{dc}), diode D_{clamp} turns on and clamps the bus voltage. With D_{clamp} conducting, S_{clamp} is switched on under a lossless manner.

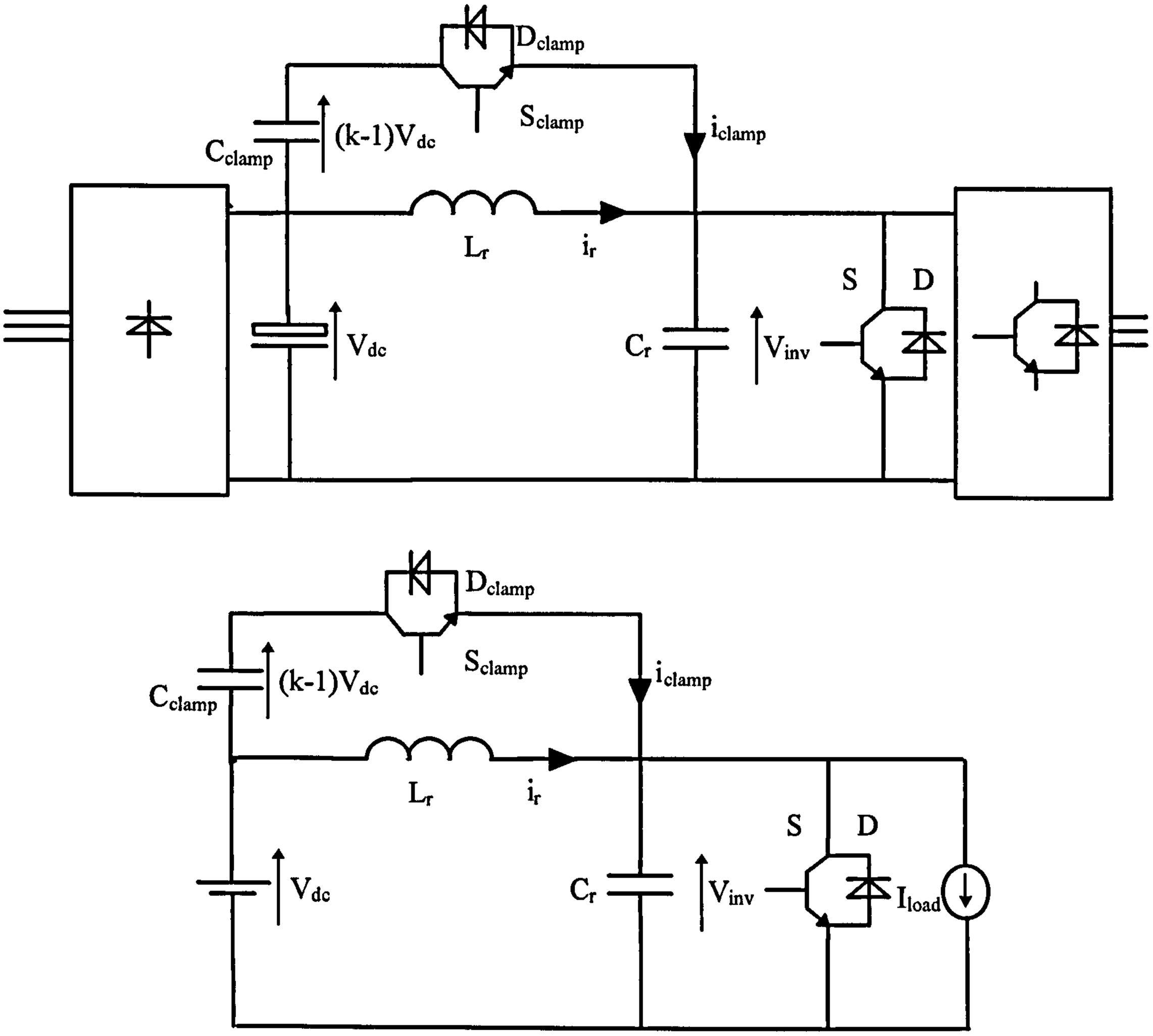


Figure 3.2.1: Schematic and equivalent circuit of the clamp basic RDCL

3.2.2 Operation Modes of the active clamp basic RDCL

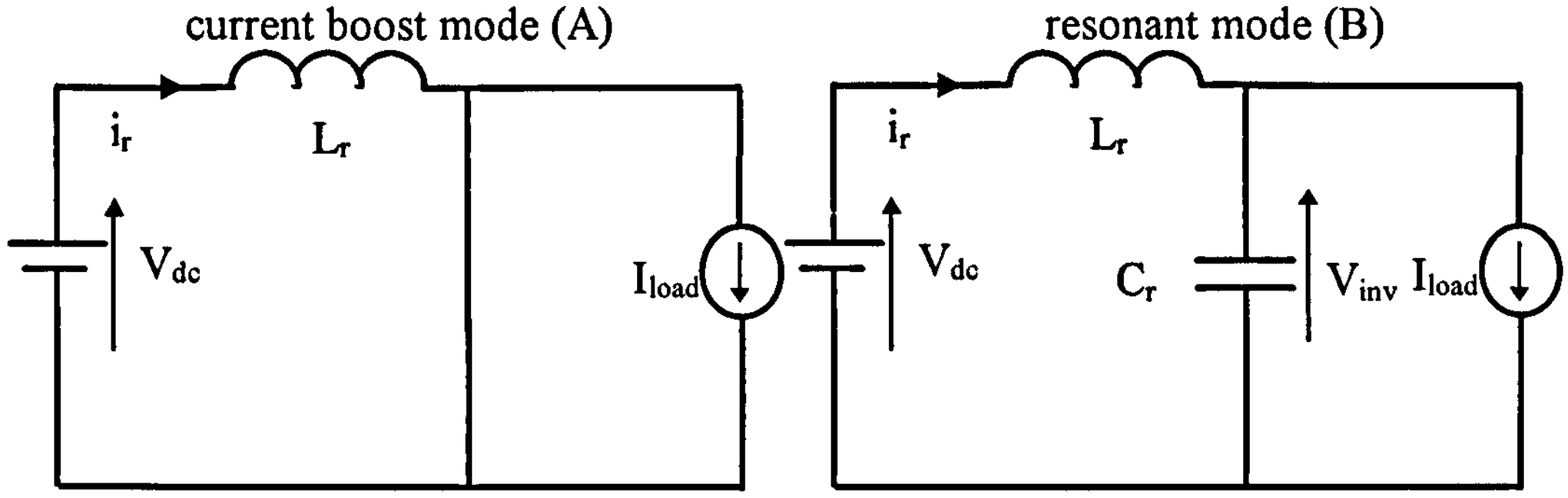
The circuit analysis of the active clamp basic RDCL is based on four operation modes (Figures 3.2.2 and 3.2.3).

Current boost mode (A): The first mode is the current boost mode already discussed in section 3.1.

Resonant mode (B): Once the switch S is released a resonant mode starts. Again this mode is identical to the resonant mode of the basic RDCL and all equations in section 3.1 can be applied. At the end of the resonant mode the voltage V_{inv} reaches the voltage kV_{dc} and diode D_{clamp} starts conducting.

Clamp mode (C): With D_{clamp} is conducting device S_{clamp} is turned on in a lossless manner and eventually the current i_{clamp} transfers from the diode D_{clamp} to the device S_{clamp}. The charge transferred to the capacitor C_{clamp} when D_{clamp} conducts is recovered during the interval when S_{clamp} conducts. When the net charge transferred to C_{clamp} equals zero, S_{clamp} must be turned off and the clamp mode has finished.

Resonant mode (D): The LC circuit is released from the clamp voltage and V_{inv} resonates towards zero. When V_{inv} reaches zero the current boost mode takes over.



$$V_{inv}(t) = 0V \qquad (3.2.1)$$

$$i_r = I_{load} + \frac{V_{dc}}{L_r}t \qquad (3.2.2)$$

$$V_{inv}(t) = V_{dc}(1 - \cos\omega_0 t) + Z_0(I_{r1} - I_{load})\sin\omega_0 t \qquad (3.2.3)$$

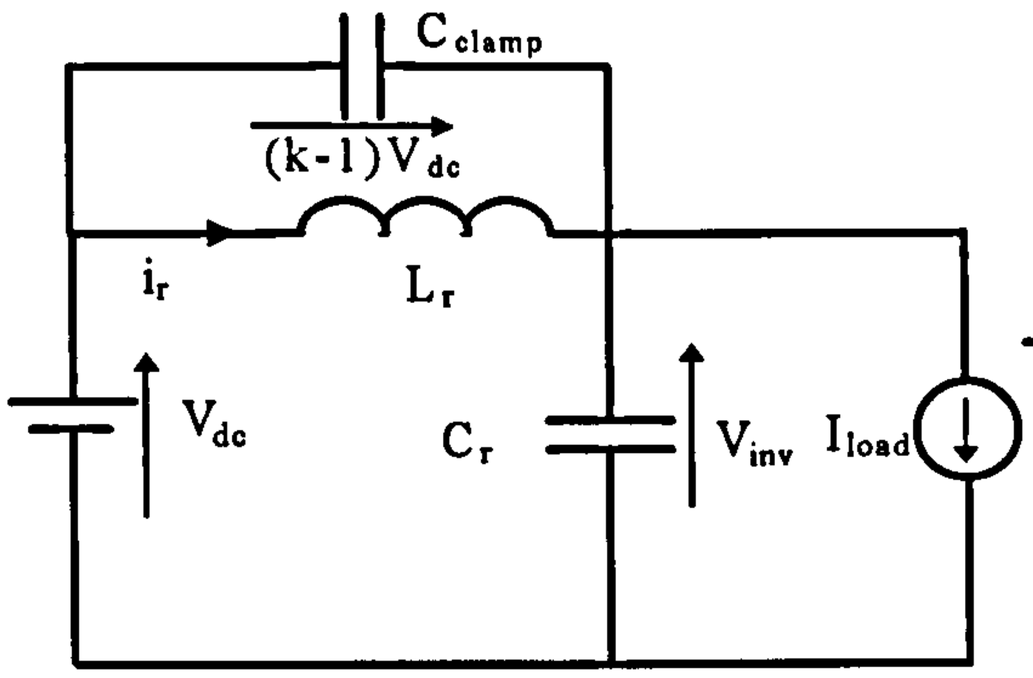
$$i_r = I_{load} + \frac{1}{L_r}\int(V_{dc} - V_{inv})dt \qquad (3.2.4)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \qquad (3.2.5)$$

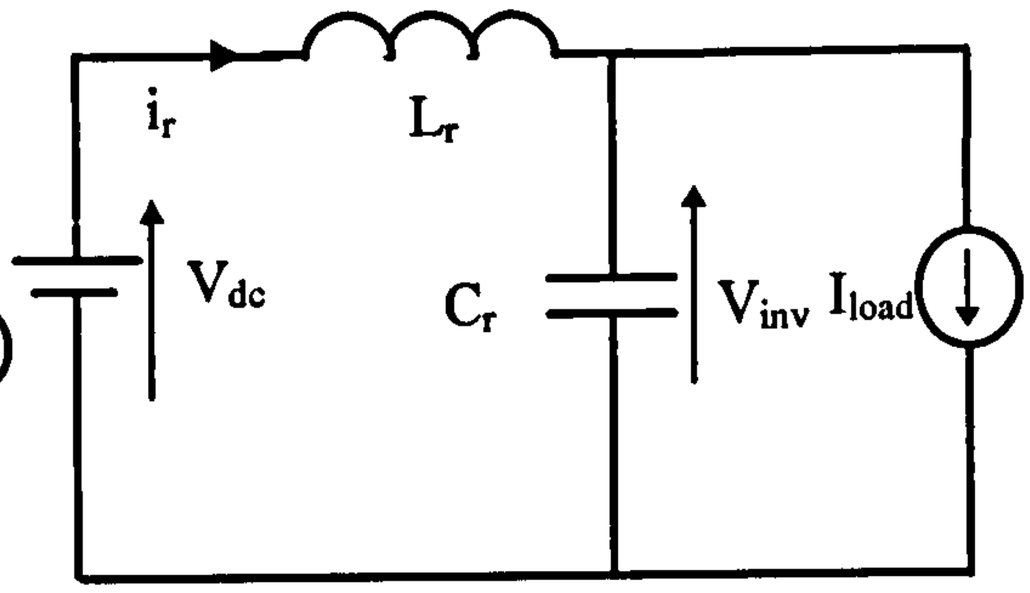
$$Z_0 = \sqrt{\frac{L_r}{C_r}} \qquad (3.2.6)$$

I_{r1} is the remaining current stored in the inductor L_r after the switch S is turned off.

clamp mode (C)



resonant mode (D)



$$V_{inv}(t) = V_{dc}(1-\cos\omega_1 t) + Z_1(I_{r2} - I_{load})\sin\omega_1 t \quad (3.2.7)$$

$$i_r = I_{load} + \frac{1}{L_r}\int(kV_{dc} - V_{dc})dt \quad (3.2.8)$$

$$\omega_1 = \frac{1}{\sqrt{L_r(C_r + C_{clamp})}} \quad (3.2.9)$$

$$Z_1 = \sqrt{\frac{L_r}{C_r + C_{clamp}}} \quad (3.2.10)$$

$$V_{inv}(t) = V_{dc}(1-\cos\omega_0 t) + Z_0(I_{r3} - I_{load})\sin\omega_0 t \quad (3.2.11)$$

$$i_r = I_{load} + \frac{1}{L_r}\int(V_{dc} - V_{inv})dt \quad (3.2.12)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad (3.2.13)$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \quad (3.2.14)$$

I_{r2} is the remaining current stored in the inductor L_r after D_{clamp} starts conducting. I_{r3} is the remaining current stored in the inductor L_r after S_{clamp} is turned off.

Figure 3.2.2: Operation modes A to D of the active clamp basic RDCL

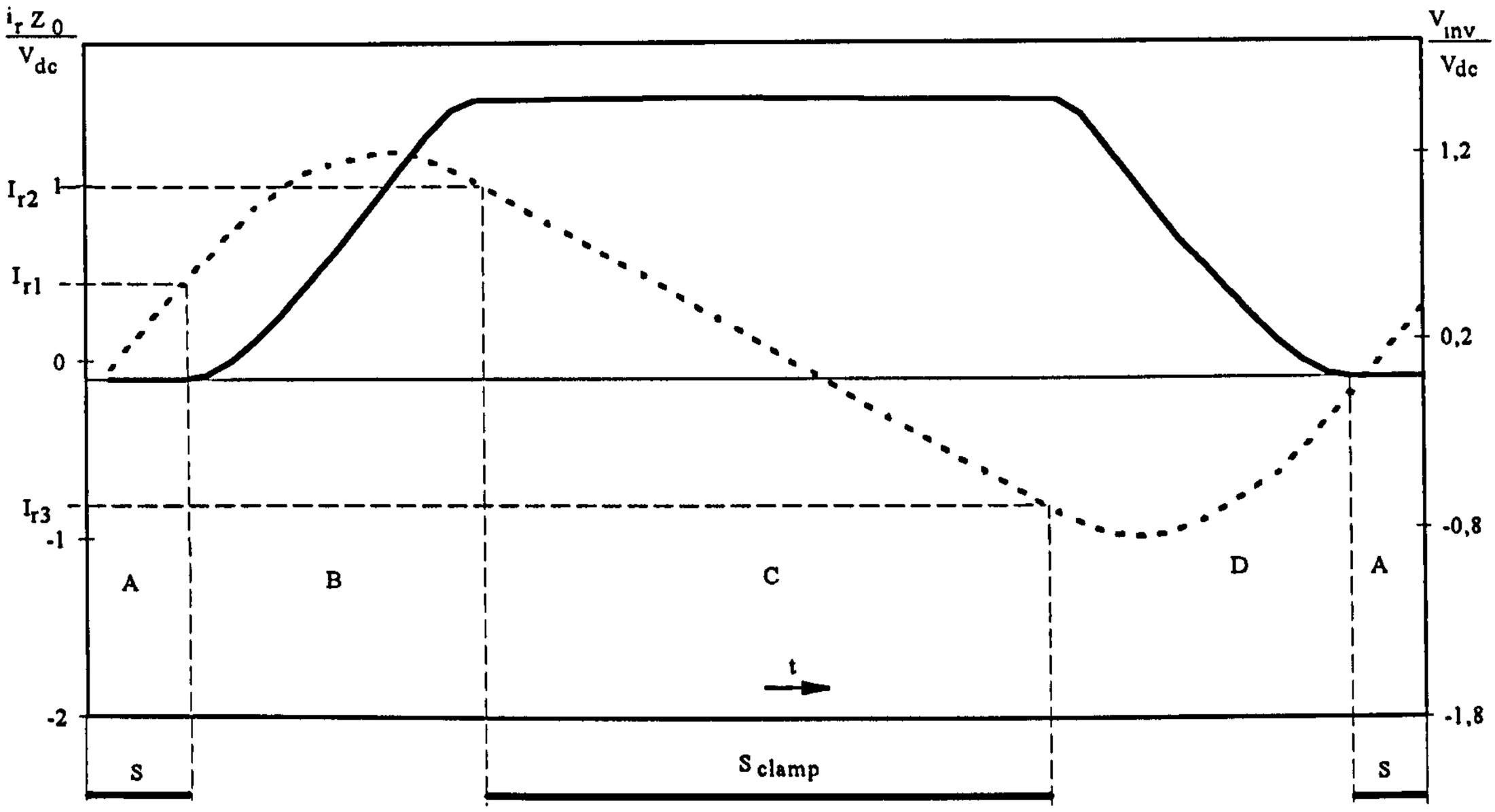


Figure 3.2.3: Normalised waveform of V_{inv} (solid line) and i_r (dotted line) over one cycle of resonant cycle of the active clamp basic RDCL with k=1.4

In the active clamp basic RDCL topology the clamping voltage has to be always greater than the steady-state peak voltage. The clamp diode ensures that the voltage across the clamp capacitor reaches at least the dc-link level. The stored energy in the inductor leads to an increase of the clamp voltage. The resulting clamp factor k defines finally the clamp time. A low clamp factor means a long clamp time. The choice of the k factor was investigated in reference [3.11]. In [3.11] it was shown that k is a function of the resonant LC elements and the time period of the resonant link cycle. The following relation was given:

$$T_p = 2\sqrt{L_r C_r}\left(\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right) \qquad (3.2.15)$$

where T_p is the period of one resonant link cycle. T_p includes the rise and fall time, the clamp time and the current boost time of V_{inv}.

Figure 3.2.4 shows a plot of equation 3.2.15 with the values L_r=5μH and C_r=1μF. The case for k>2 degenerates into a natural clamping part as happens for the basic RDCL. For clamping voltages less than $2V_{dc}$ any attempt to further increase the link frequency can only be achieved with the sacrifice of an increase in the clamp factor.

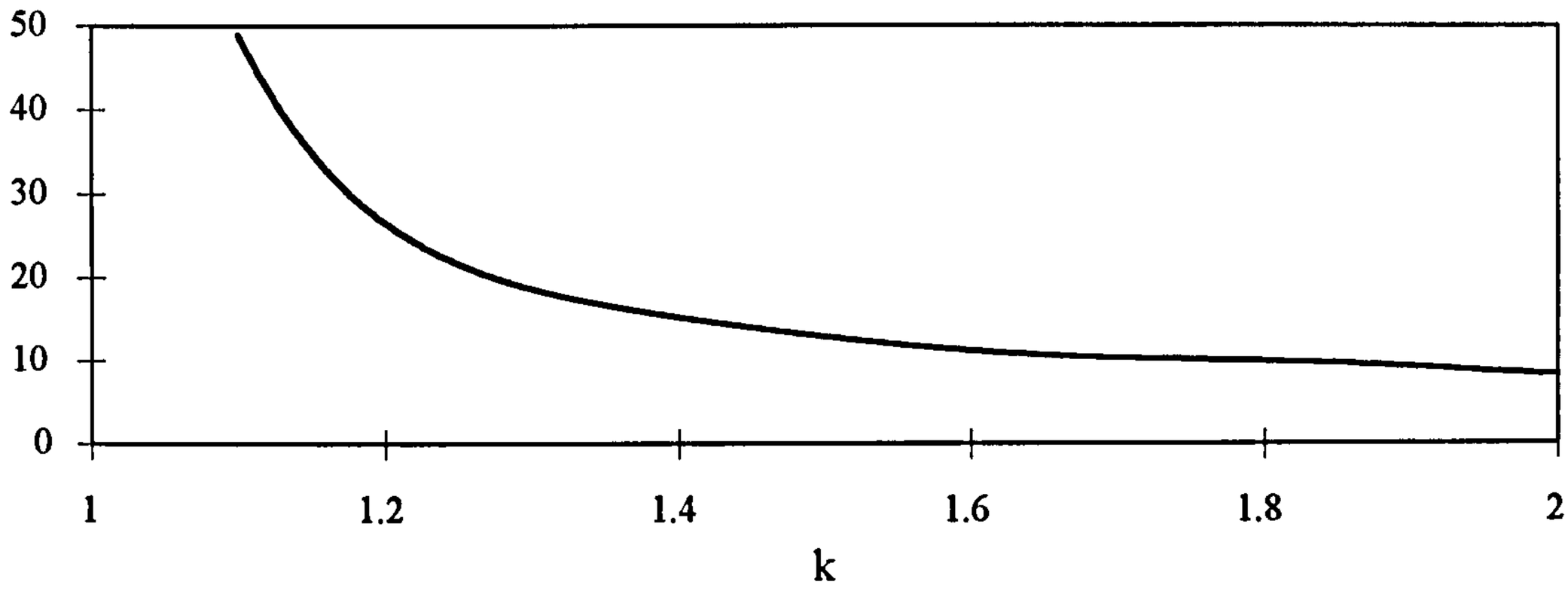


Figure 3.2.4: Clamp factor k as a function of the link cycle period T_p [3.11]

So far the active clamp basic RDCL needs one additional switch more than its predecessor the basic RDCL. However reference [3.14] suggests a way of removing this additional switch. The author proposes to exchange S_{clamp}, D_{clamp} and C_{clamp} with a non-linear capacitor (C_{non}). A non-linear capacitor can be manufactured as single- and multilayered ceramic capacitor that is saturable depending on charge. Thus, the capacitance is dependent on voltage as seen in Figure 3.2.5.

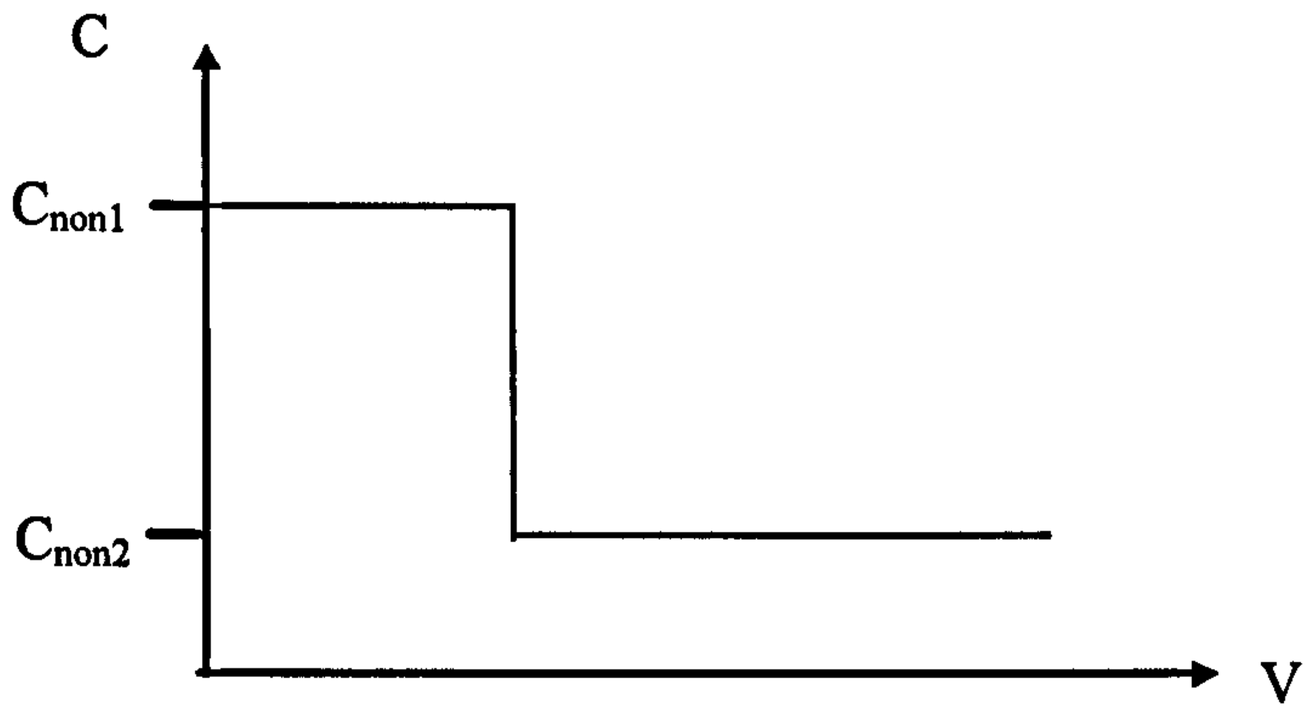


Figure 3.2.5: Idealised capacitance voltage characteristics of a non-linear capacitor

With this component the link frequency of V_{inv} can be manipulated without controlling the clamp circuit. If the inverter input voltage is lower than kV_{dc} the resonant frequency is:

$$\omega_0 = \frac{1}{\sqrt{L_r C_{non1}}} \tag{3.2.16}$$

and during the clamp mode

$$\omega_1 = \frac{1}{\sqrt{L_r C_{non2}}} \tag{3.2.17}$$

So far no practical results have been published but research work is increasing in this area as seen in references [3.15-3.18]. Another concept for eliminating the switch S_{clamp} is to insert a transformer in the resonant circuit. This topology is called the passive clamp basic RDCL topology.

3.2.3 Principles of the passive clamp basic RDCL

In contrast to the active clamp basic RDCL using a non-linear capacitor, passive clamp basic RDCLs have been practically completed in the research laboratories [3.19, 3.20]. A transformer-coupled clamp circuit limits the peak value of the inverter input voltage similar to the active clamp version. Figure 3.2.6 shows the circuit and the equivalent circuit:

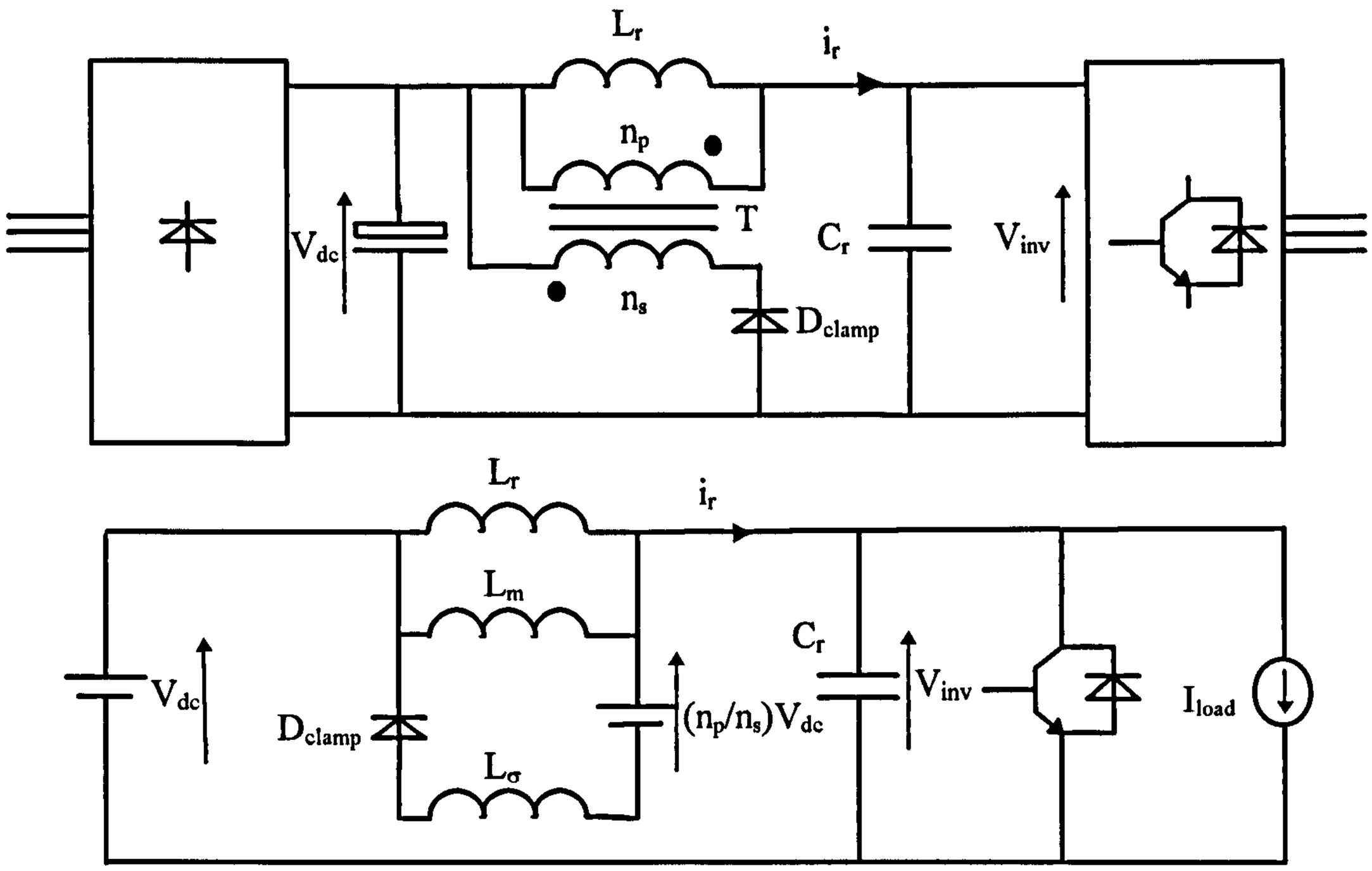


Figure 3.2.6: Schematic and equivalent circuit of the passive clamp basic RDCL

The designer of a passive clamp converter topology has mainly to focus on the dimensioning of the clamp transformer T [3.19-3.21]. As shown in Figure 3.2.6 the transformer is expressed as main inductance (L_m) and stray inductance (L_σ). Inductance L_m is proportional to the product of the primary winding $(n_p)^2$ and the core permeability (μ). The stray inductance L_σ can be expressed as:

$$L_\sigma = L_m \frac{1 - c_p^2}{c_p^2} \tag{3.2.18}$$

with $(c_p)^2$ represents the coupling factor. As seen from Figure 3.2.6 L_m is parallel to L_r. To ensure that the resonance parameters do not change too much, L_m has to be set much larger than L_r resulting in a large number of turns on the primary side. Furthermore it has to set into account that the stray inductance must be as small as possible, because a high L_σ prevent unsuccessful voltage oscillation of V_{inv} after the clamp mode [3.19].

The analysed four operation modes of the active clamp version can also be applied to the passive clamp technique. The only equations that have to be changed are the equations 3.2.7 to 3.2.10. During the clamp mode diode D_{clamp} conducts and therefore current is flowing through the secondary winding n_p of the transformer. Thus V_{inv} gets be clamped to:

$$V_{inv}(t)=kV_{dc} \tag{3.2.19}$$

with

$$k = (1 + \frac{n_p}{n_s}) \tag{3.2.20}$$

whereas for k=1 the resonant frequency ω_0 remains zero and Z_0 is equal zero.

Although the passive and active clamp basic RDCL meet the target of limiting the overshoot voltage to less than twice the dc-link voltage, both topologies suffer from the disadvantage of being DPM controlled.

3.3 Parallel Resonant DC-Link Inverter (PRDCL)

The obstacles of the converter topologies discussed so far are: subharmonic problems resulting from DPM control, high device stresses and conduction loss in the resonant inductor. So, the possibility of applying PWM control and reducing the voltage stress was quite a desirable objective in the development of new resonant dc-link inverter topologies. As a consequence effort reached into the Parallel Resonant DC-Link Inverter described in references [3.22-3.29].

3.3.1 Principles of the PRDCL

The typical design characteristics are a power switch between the dc-link capacitor and the input of the inverter and small snubber capacitors connected parallel to each switching device in the inverter as seen in Fig. 3.3.1. The snubber capacitors are used to achieve turn-off under near zero voltage conditions. Once a resonant mode is activated and the voltage V_{inv} reaches zero volts, the snubber capacitors will be discharged.

Most of the time V_{inv} is connected straight to V_{dc} via S_{clamp}. When the switch opens, a resonant oscillation is activated, resonating the inverter input voltage to zero and backwards. Once the inverter input voltage again reaches the value V_{dc} the clamp switch S_{clamp} is switched on and clamps the inverter input voltage to the dc-link value.

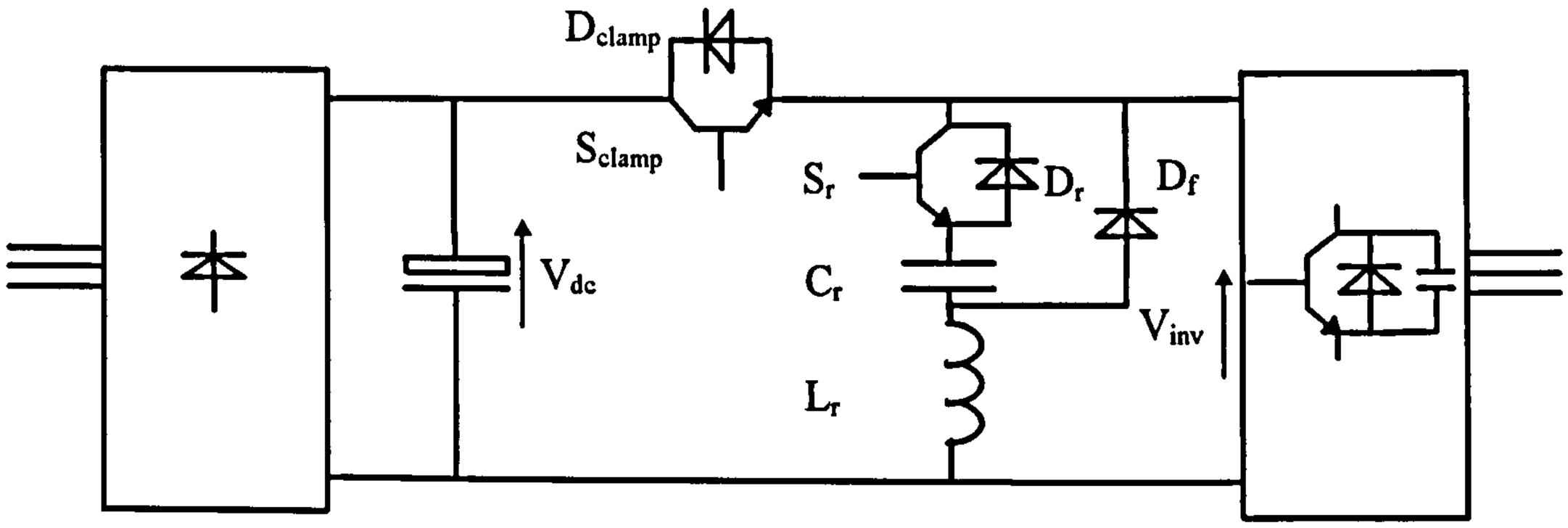


Figure 3.3.1: Schematic circuit of the PRDCL proposed in reference [3.27]

The principle of operation of the PRDCL is discussed with the help of the circuit given in reference [3.27]. Any other PRDCL topology works in a similar but design distinctive way. For the circuit analysis the following equivalent circuit can be presented:

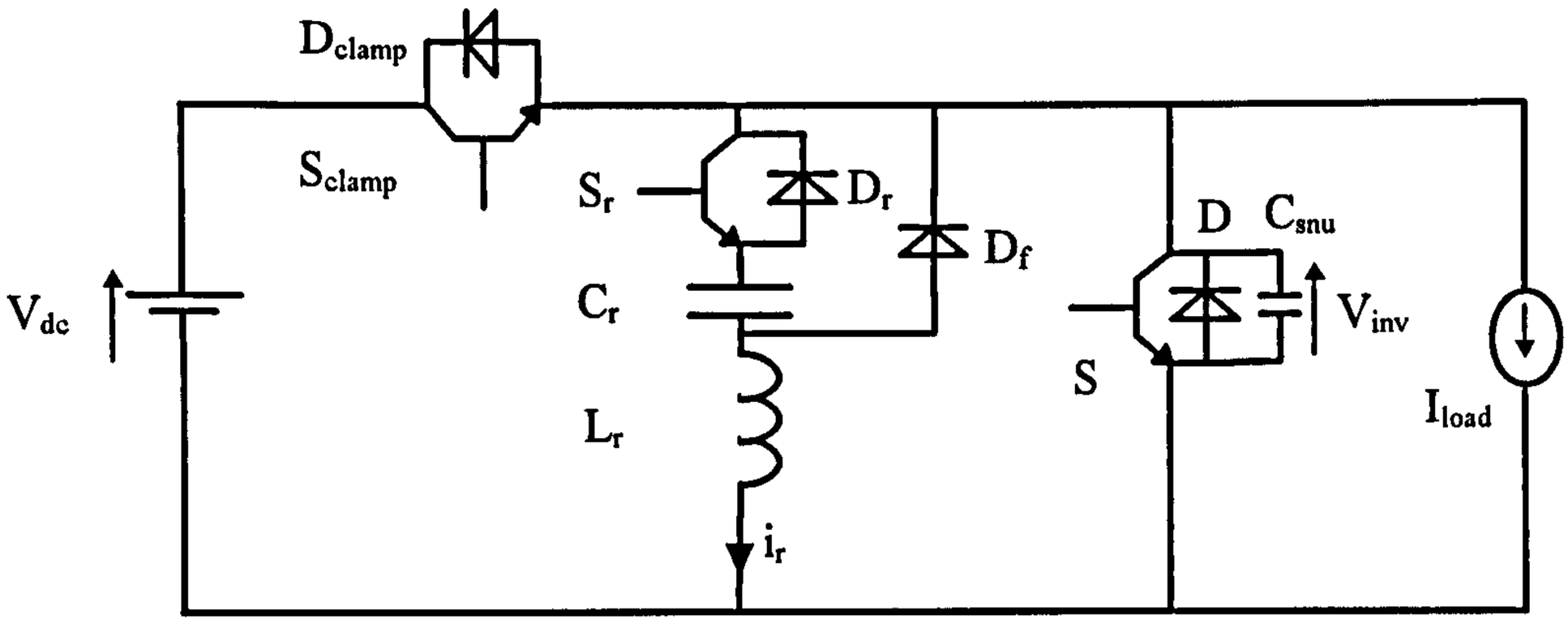


Figure 3.3.2: Simplified circuit of the PRDCL proposed in reference [3.27]

The capacitor C_{snu} in the simplified circuit is the equivalent capacitor across the bus during the switching period. Knowing C_{snu} the capacitance parallel to each device can be calculated to:

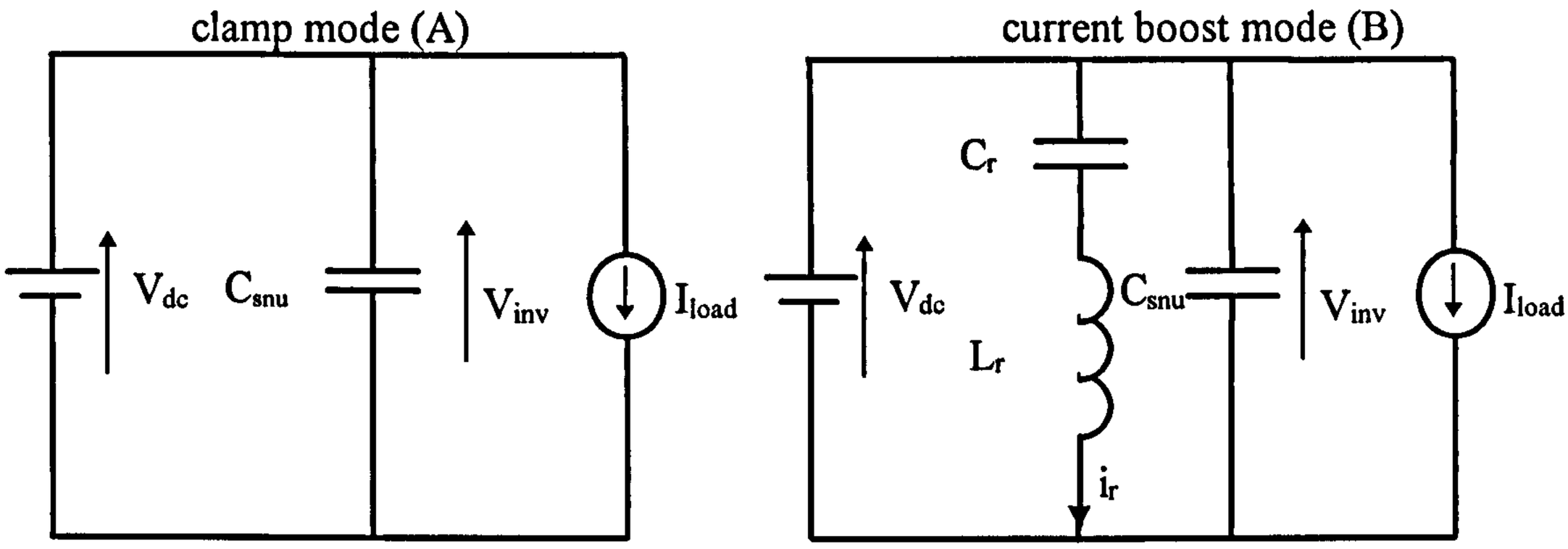
$$C = \frac{C_{snu}}{3} \tag{3.3.1}$$

3.3.2 Operation Modes of the PRDCL

The resonant cycle can be divided into seven operation modes which are now analysed (see Figure 3.3.3 to Figure 3.3.7).

Clamp mode (A): In the first mode the resonant circuit is in steady state S_{clamp} or D_{clamp} is conducting and S_r and S are off.

Resonant mode (B): When a control signal is commanded to turn S_r on, S_r turns on under zero current conditions. Thus resonant current i_r starts to resonate and energy will be stored in L_r and C_r.



$$V_{inv}(t) = V_{dc} \qquad (3.3.2)$$

$$i_r(t) = 0A \qquad (3.3.3)$$

$$V_{inv}(t) = V_{dc} \qquad (3.3.4)$$

$$i_r(t) = \frac{1}{L_r}\int (V_{dc} - V_{Cr}(t))dt \qquad (3.3.5)$$

$$V_{dc} = L_r C_r \frac{dV_{Cr}^2(t)}{d^2t} + V_{Cr}(t) \qquad (3.3.6)$$

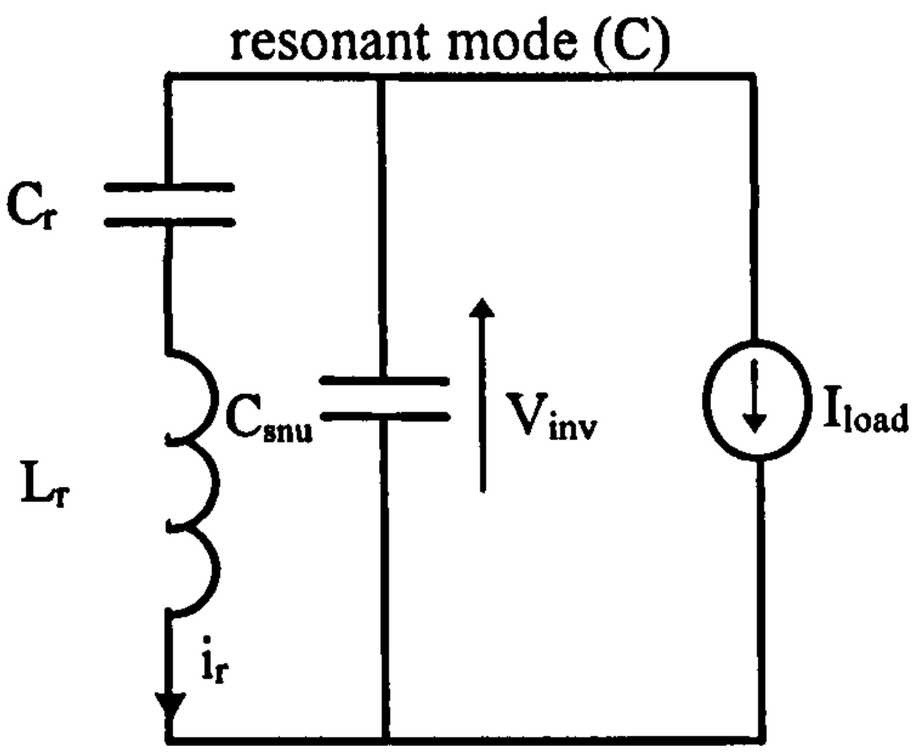
$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \qquad (3.3.7)$$

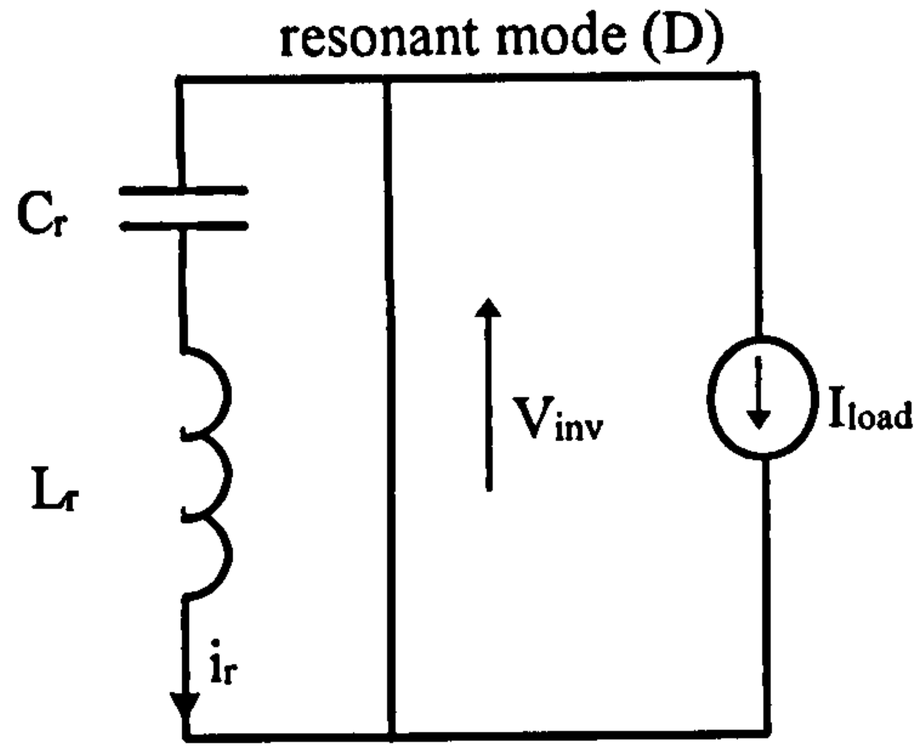
$$Z_0 = \sqrt{\frac{L_r}{C_r}} \qquad (3.3.8)$$

Figure 3.3.3: Operation modes A and B of the PRDCL

Resonant mode (C): As soon as i_r reaches a current level I_{r1} that provides the circuit with enough energy to overcome the internal losses (I_{r1} is a function of the load current and losses in the resonant circuit), switch S_{clamp} opens. The voltage of the inverter is now released from the dc-link supply and a resonant oscillation takes place between the capacitor C_r, the snubber capacitors of the inverter C_{snu} and the inductor L_r.

Resonant mode (D): Once V_{inv} is equal to zero all snubber capacitors are discharged and voltage V_{inv} remains at zero for a while. In this condition, S can be turned on under zero voltage. The oscillation continues now between C_r and L_r and the current i_r decreases, reverses and increases in the opposite direction (see Figure 3.3.7) so that i_r is flowing through diode D_r resulting that device S_r can be switched off under zero voltage conditions.





$$V_{inv}(t) = c_1(V_{dc} - V_{Cr1}) + Z_1(c_1 I_{load} + I_{r1}) * \\ * \sin\omega_1 t + c_2 V_{dc} + c_1 V_{Cr1} - \frac{I_{load}}{C_{snu} + C_r} \qquad (3.3.9)$$

$$V_{inv}(t) = 0V \qquad (3.316)$$

with

$$c_1 = \frac{C_r}{C_{snu} + C_r} \qquad (3.3.10)$$

$$c_2 = \frac{C_{snu}}{C_{snu} + C_r} \qquad (3.3.11)$$

$$i_r(t) = \frac{1}{L_r}\int (V_{dc} - V_{Cr}(t))dt \qquad (3.3.12)$$

$$i_r(t) = \frac{1}{L_r}\int (-V_{Cr}(t))dt \qquad (3.3.17)$$

$$V_{dc} = L_r(C_r + C_{snu})\frac{dV_{Cr}^2(t)}{d^2t} + V_{Cr}(t) \qquad (3.3.13)$$

$$0V = L_r C_r \frac{dV_{Cr}^2(t)}{d^2t} + V_{Cr}(t) \qquad (3.3.18)$$

$$\omega_1 = \frac{1}{\sqrt{\frac{L_r C_r C_{snu}}{C_{snu} + C_r}}} \qquad (3.3.14)$$

with ω_0 from equation 3.3.7

$$Z_1 = \frac{1}{\omega_1 C_{snu}} \qquad (3.3.15)$$

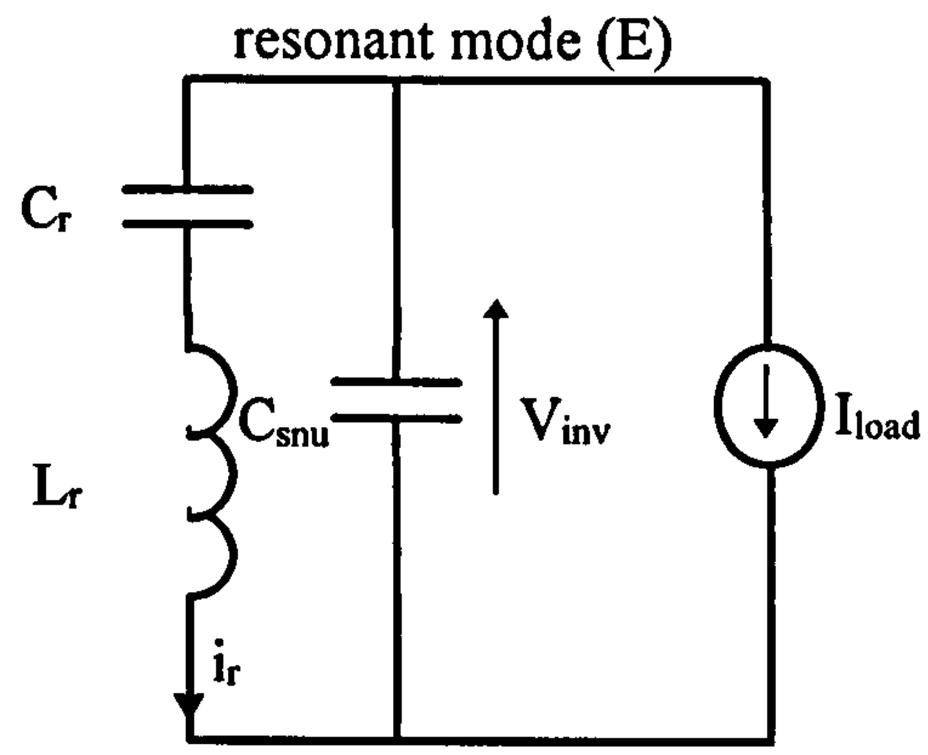
with Z_0 from equation 3.3.8

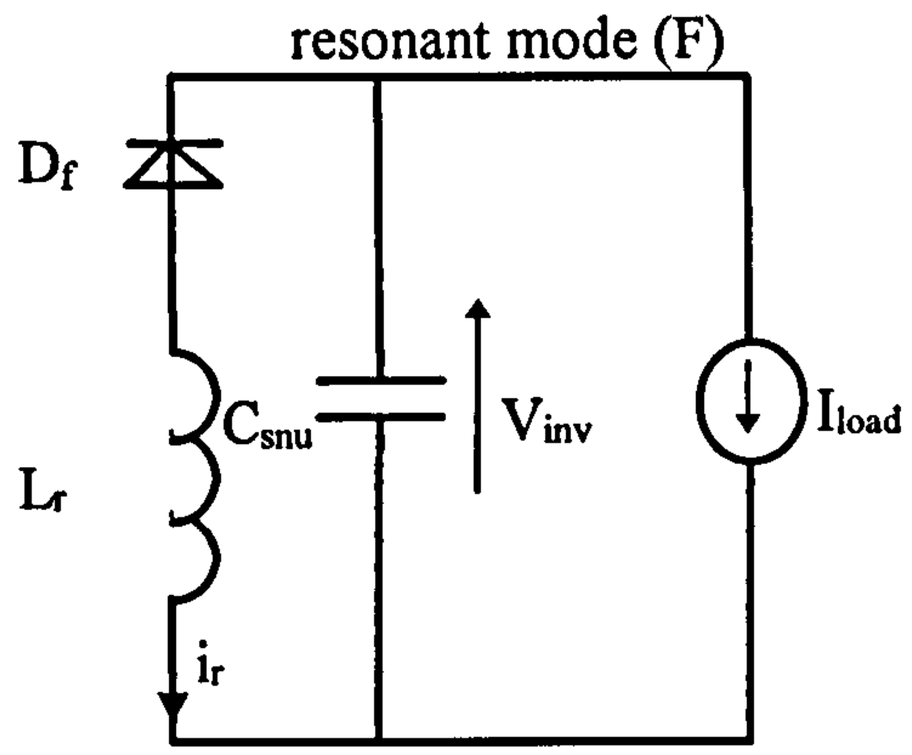
V_{Cr1} is the actual voltage across the resonant capacitor C_r at the time when S_{clamp} switches off. I_{r1} is the remaining current in the inductor at this time.

Figure 3.3.4: Operation modes C and D of the PRDCL

Resonant mode (E): When the current i_r is equal to the reference value I_{r2} switch S is turned off allowing a resonance between C_r, L_r, and C_{snu}. I_{r2} must be large enough to allow a successful backswing of the inverter input voltage.

Resonant mode (F): The capacitor voltage V_r falls to zero and D_f becomes forward biased. A new resonant mode between L_r and C_{snu} takes place (see Figure 3.3.5).





$$V_{inv}(t) = c_1 V_{Cr2}(1-\cos\omega_1) - Z_1(c_1 I_{load} + \\ + I_{r2})\sin\omega_1 t - \frac{I_{load}}{C_{snu}+C_r} \qquad (3.3.19)$$

with c_1, from equations 3.3.10

$$i_r(t) = \frac{1}{L_r}\int(-V_{Cr}(t))dt \qquad (3.3.20)$$

$$0V = L_r(C_r + C_{snu})\frac{dV_{Cr}^2(t)}{d^2t} + V_{Cr}(t) \qquad (3.3.21)$$

with ω_1 from equation 3.3.14

with Z_1 from equation 3.3.15

$$V_{inv}(t) = -Z_2 I_{r3}\sin\omega_2 t \qquad (3.3.22)$$

$$i_r(t) = \frac{1}{L_r}\int(-V_{Cr}(t))dt \qquad (3.3.23)$$

$$0V = L_r C_{snu}\frac{dV_{Cr}^2(t)}{d^2t} + V_{Cr}(t) \qquad (3.3.24)$$

$$\omega_2 = \frac{1}{\sqrt{L_r C_{snu}}} \qquad (3.3.25)$$

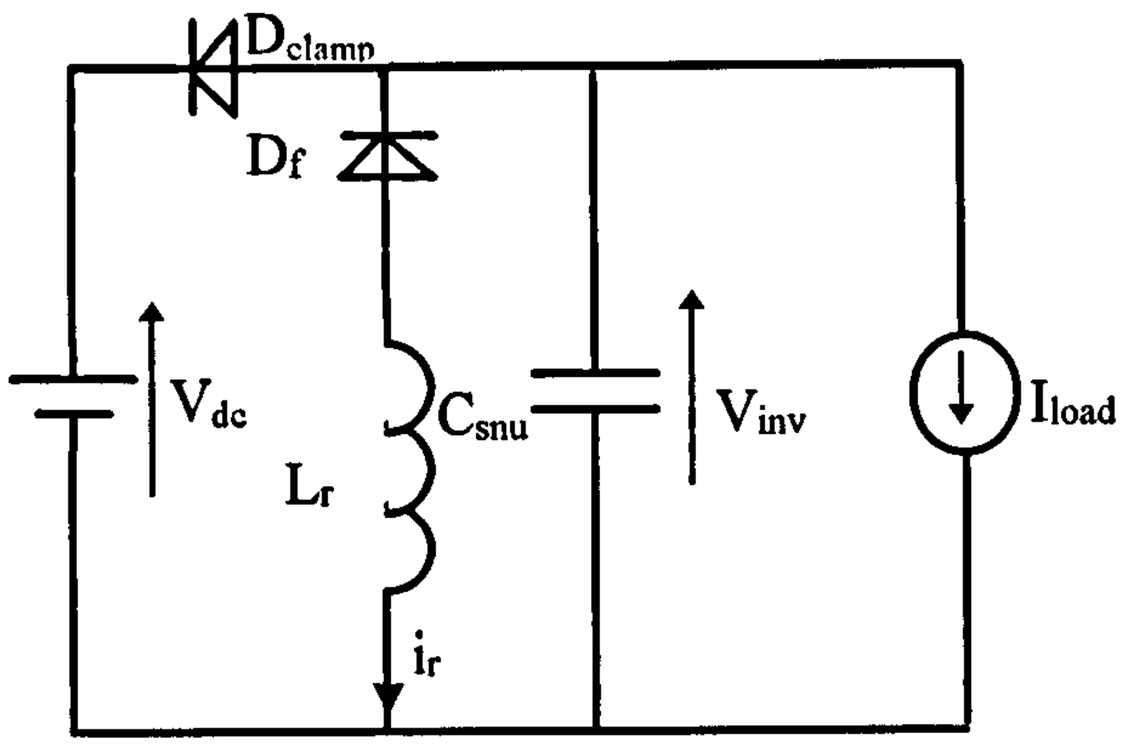
$$Z_2 = \sqrt{\frac{L_r}{C_{snu}}} \qquad (3.3.26)$$

V_{Cr2} is the actual voltage across the resonant capacitor C_r when S has been turned off and I_{r2} is the remaining current at this status. I_{r3} is the remaining current.

Figure 3.3.5: Operation modes E and F of the PRDCL

Clamp mode (G): The link voltage V_{inv} is restored to the dc-link voltage V_{dc}. Thus D_{clamp} gets forward biased and is able to conduct. Now S_{clamp} can be switched on under zero voltage conditions. The current i_r decreases linearly to zero (Figure 3.3.6).

clamp mode (G)



$$V_{inv}(t) = V_{dc} \tag{3.3.27}$$

$$i_r(t) = I_{r4} + \frac{V_{dc}}{L_r}t \tag{3.3.28}$$

I_{r4} is the remaining current in L_r when D_{clamp} starts conducting.

Figure 3.3.6: Operation mode G of the PRDCL

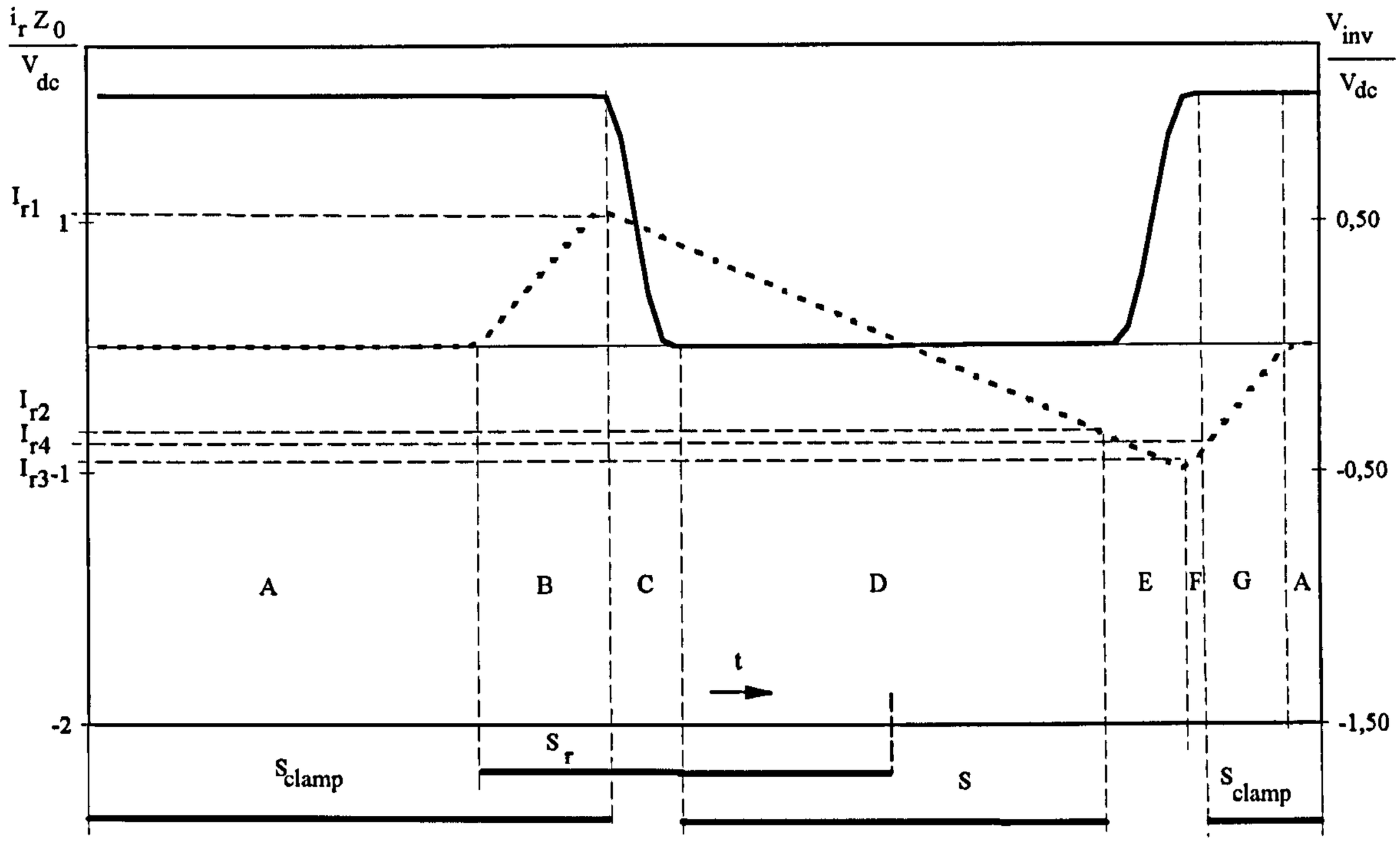


Figure 3.3.7: Normalised waveforms V_{inv} (solid line) and i_r (dashed line) of the PRDCL

Figure 3.3.7 represents only one resonant cycle in one modulation period. With PWM control the switching status of the inverter is changing six times in one modulation period. Thus the

dc-link voltage is shaped with six notches during one inverter switching period (Figure A.2.7 in Appendix A). This effect decreases the average dc-link voltage and leads to an substantial reduction of the average voltage supply to the motor and consequently a reduction in supplied power. Thus the method of 'true' PWM control must be changed for the PRDCL. This leads to the development of modified PWM control techniques where the number of notches is limited over one modulation period.

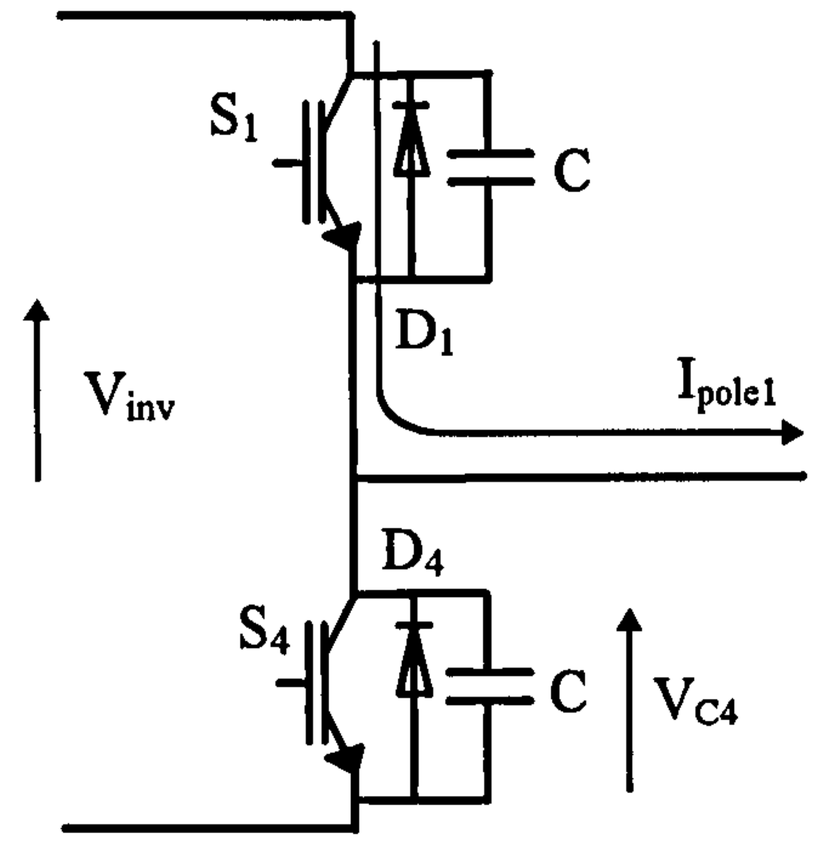
3.3.3 Modified PWM Control Schemes

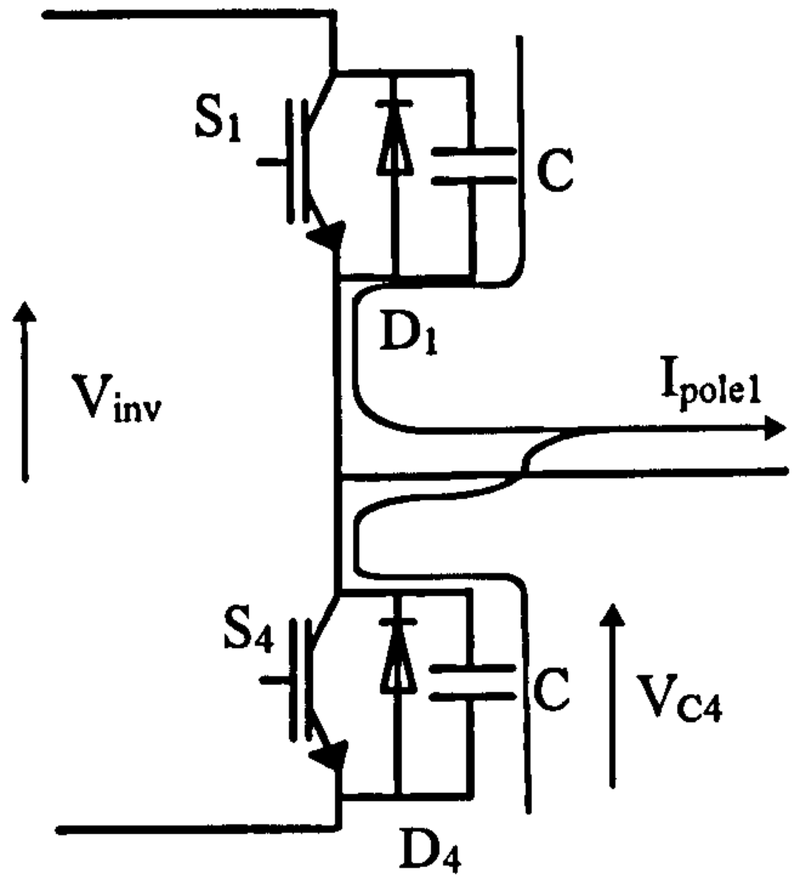
The demand of reducing the number of notches and still allowing a certain degree of PWM control can be accomplished when using capacitors C as turn-off snubbers (Figure 3.3.8). The introduction of snubber capacitors allows a new mode called 'snubber mode'. The snubber mode can only be activated when the switching device is carrying the load current. If so the parallel capacitor acts as a snubber during the turn-off process of the switching device and the turn-off process occurs under zero voltage conditions. The commutation process IGBT-Diode is completed when the antiparallel diode carries the load current. Once this diode conducts the parallel switching device can be turned on likewise under zero voltage conditions. Thus the whole commutation process IGBT-Diode is under a lossless manner. To commutate the conducting antiparallel diode the resonant circuit must be activated to clear the voltage across the charged snubber capacitor. That has already been discussed in section 3.3.1.

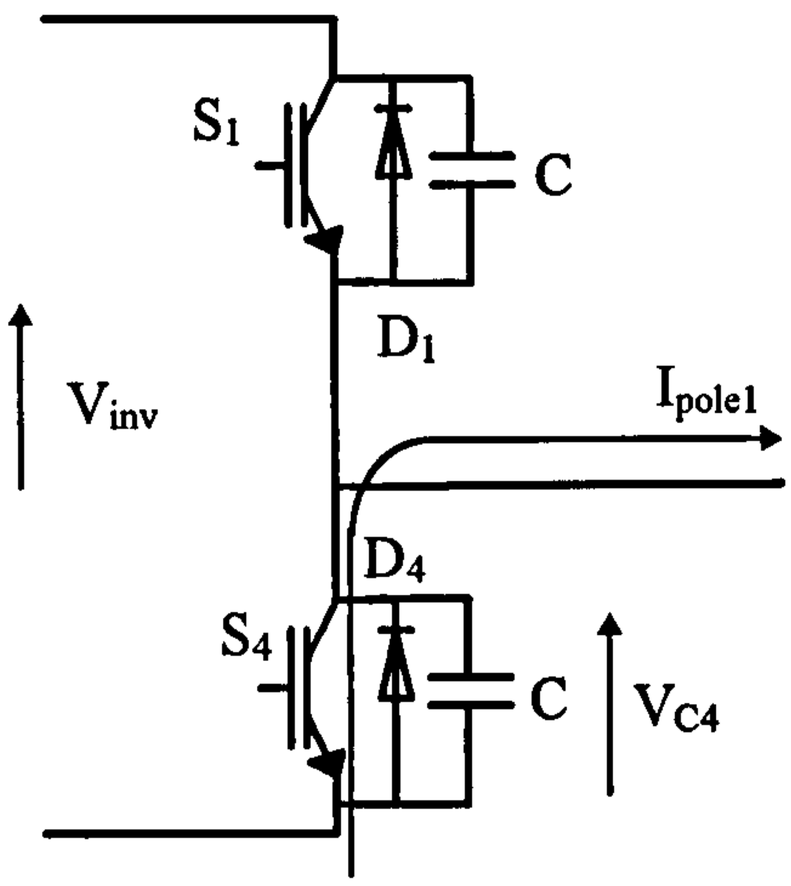
Fig. 3.3.8 illustrates the snubber mode for clarity. The load current I_{pole1} is constant during the commutation process. When S_1 is commanded to turn-off, the current is shunting into the two snubber capacitors C. The voltage V_{C4} falls linearly at a rate proportional to the load current magnitude. When V_{C4} falls below the negative dc rail, D_4 becomes forward biased and immediately picks up the load current. Once D_4 is conducting S_4 can be switched on under zero voltage conditions.

The opposite commutation (S_4 is commanded to turn-off whilst D_4 is conducting) requires the resonant mode of the dc-link, because resonating the dc-link voltage to zero is the only way to discharge the snubber capacitor parallel to S_1.

Using both different modes the number of resonant oscillation is therefore reduced. However applying modified PWM schemes means that at any state information must be given about the direction of the three load currents and information is needed of the switching status of each device in the inverter.







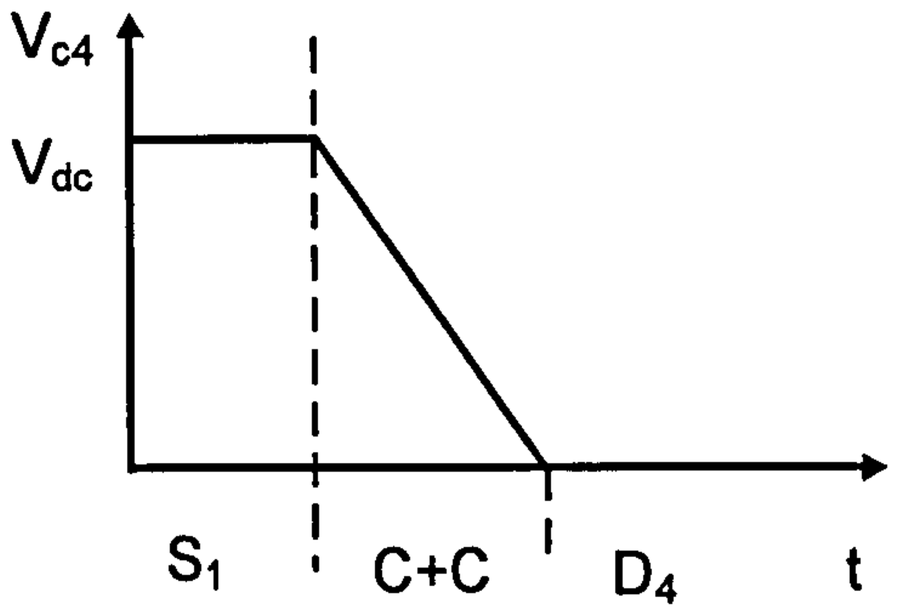
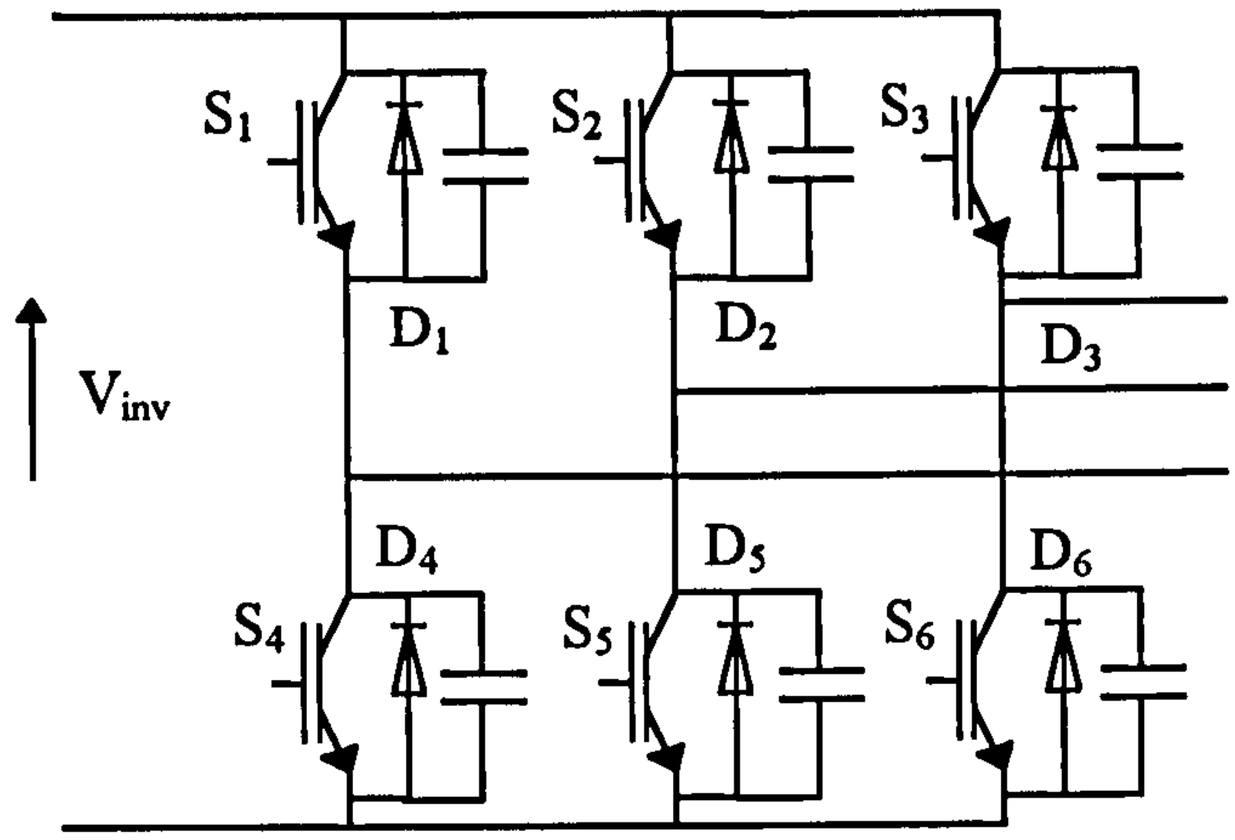
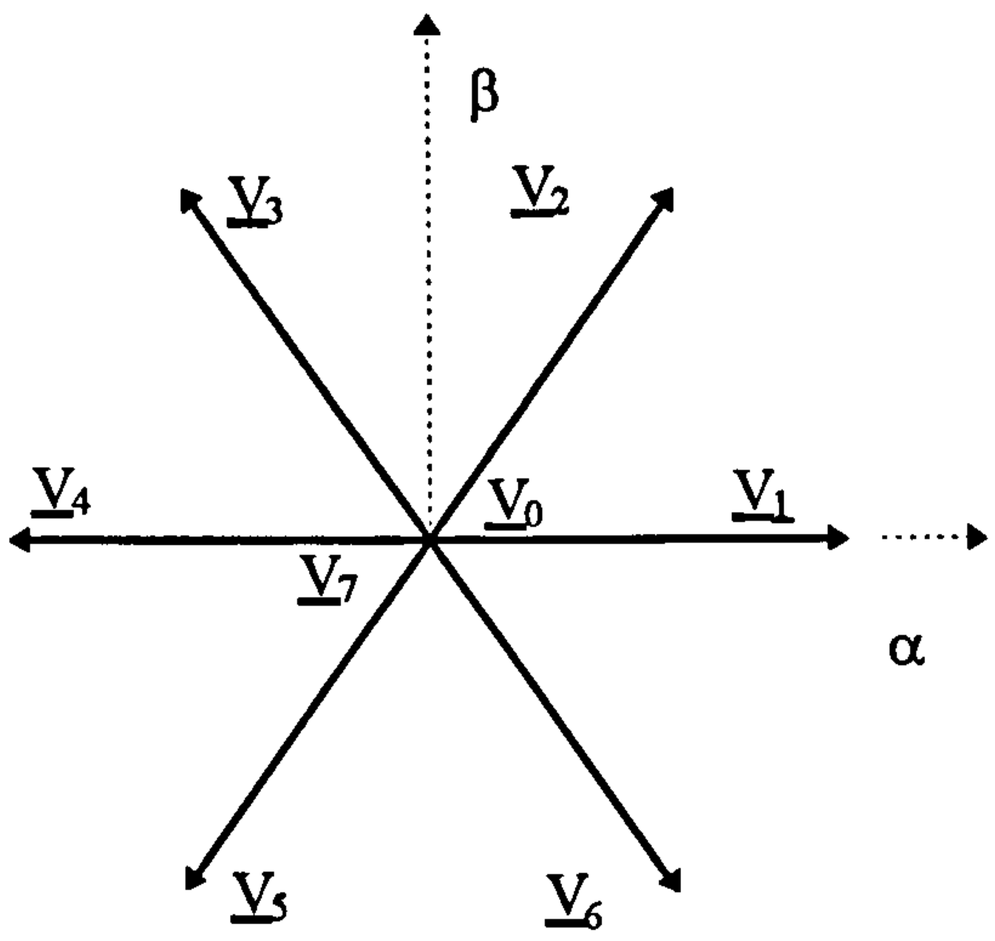


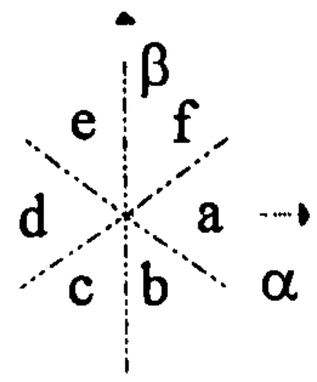
Figure 3.3.8: Commutation effect when using snubber capacitors

In the literature several modified PWM (mPWM) schemes have been suggested and can be summarised to two classical schemes that are now discussed. In spite of the fact that in literature no standardised abbreviation of these control schemes are given, the following two control schemes are called mPWM3 and mPWM2. The number represents the number of poles switched during one modulation period.

For further discussion of these PWM techniques the voltage space vector diagram from Figure 1.7.4 is shown again.







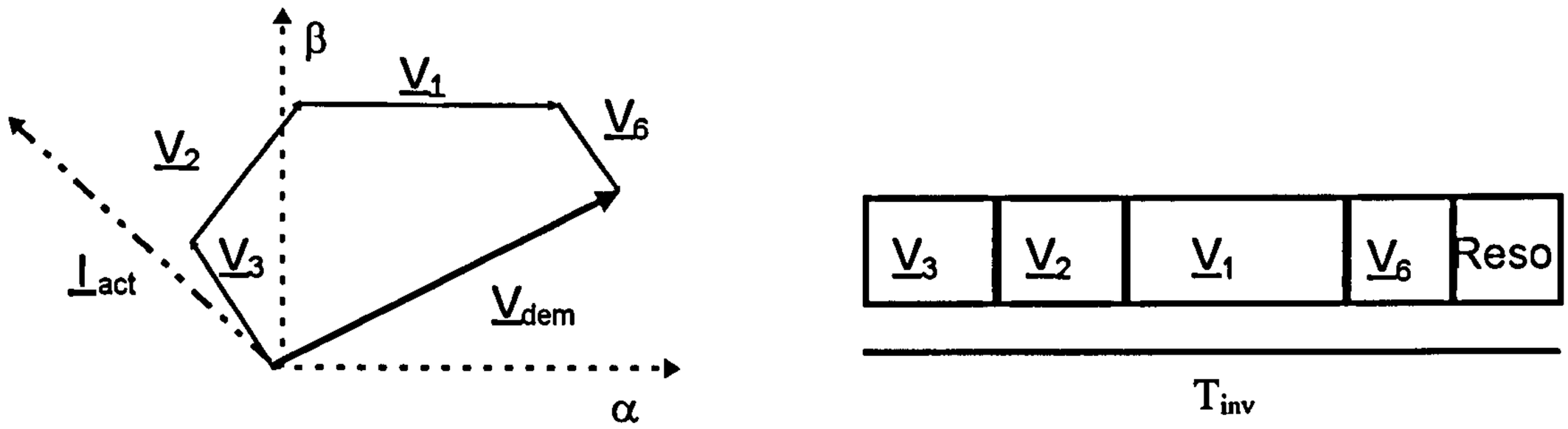
forcing vectors		zero vectors	
$\underline{V}_1$	(100)	$\underline{V}_0$	(000)
$\underline{V}_2$	(110)	$\underline{V}_7$	(111)
$\underline{V}_3$	(010)		
$\underline{V}_4$	(011)		
$\underline{V}_5$	(001)		
$\underline{V}_6$	(101)		

e.g. (010)=(S_1,off;S_2,on;S_3,off)

Figure 3.3.9: Switching patterns of the space vector diagram in the stator stationary reference frame

Fig. 3.3.10 shows an example of the switching status of the mPWM3 control. After the resonant mode is activated, the inverter input voltage V_{inv} is zero, therefore all snubber capacitors are discharged. To start the switching sequence the voltage vector whose direction is nearest to the actual current vector $\underline{I}_{act}$ has to be chosen. In this example the switching pattern (010) corresponding to $\underline{V}_3$ is applied. The inverter voltage resonates back to its dc-link value and charges all capacitors that are connected to the remaining open switches. By choosing the nearest voltage vector to the actual current vector $\underline{I}_{act}$ every turned-on switch is also conducting. During the modulation period, only one turn-off commutation per converter leg can be applied. To obtain the demand voltage V_{dem} only aligned voltage vectors must be used (in this example the sequence $\underline{V}_2$, $\underline{V}_1$ and $\underline{V}_6$ is applied). Once $\underline{V}_6$ is activated, a resonant oscillation is needed to discharge all snubber capacitors because now only diodes are conducting and no zero voltage switching can be carried out using the snubber capacitors. The

total modulation period T_{inv} of the inverter results in the on-state times of the different applied forcing vectors and the time of the whole resonant process as seen in Fig. 3.3.10.

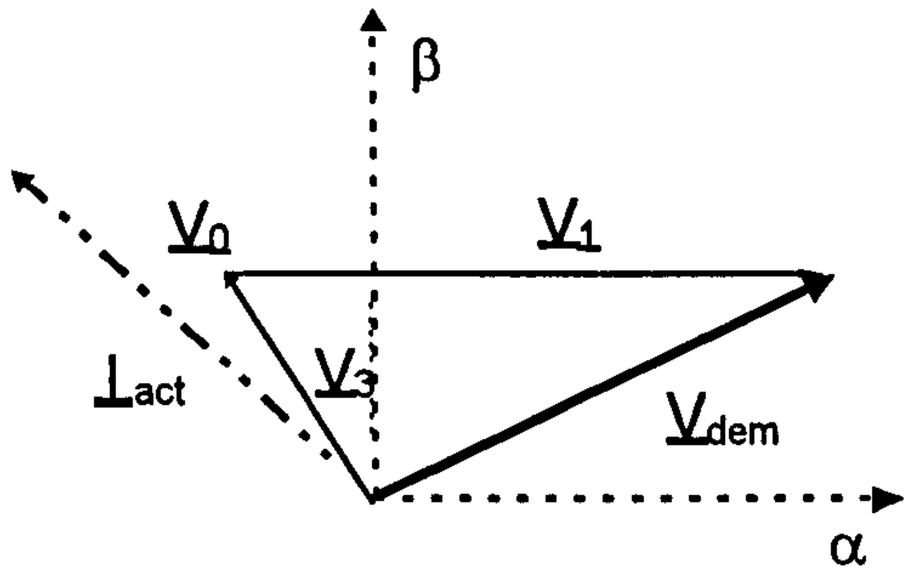


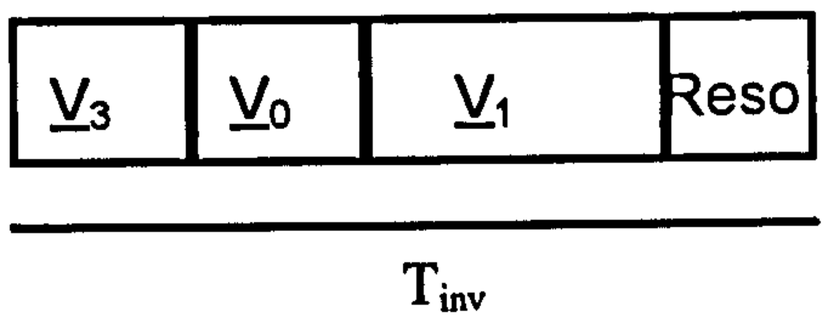
'Reso' stands for resonant mode.

Figure 3.3.10: Switching status and time period of the mPWM3 control method

The mPWM3 control scheme implies that every pole must change during one modulation period. This operation is violated in the case where commutation in one pole is required regardless of the current direction. This happens, for instance, if the inverter enters the so-called six-step condition, where inverter switches must be kept on for half the period of the fundamental frequency, irrespective of the current direction.

The mPWM2 control scheme changes only two poles during one modulation period (see Fig. 3.3.11). Again once the resonant mode is activated and the inverter voltage is zero the voltage vector that is nearest to the actual current vector has to be chosen (e.g. $\underline{V}_3$). Thus all snubber capacitors are zero and therefore all switches switch under zero-voltage conditions. When the on-state time of the first vector has been completed, all upper switches (or lower switches) must be switched off. In the space vector diagram, turning off all upper switches corresponds with the zero vector $\underline{V}_0$, whereas turning off all lower switches corresponds with $\underline{V}_7$. The choice of zero vector depends on the current vector. If the current vector is in sectors a,b,c, V_o must be chosen, otherwise $\underline{V}_7$ (Figure 3.3.9). In our example ($\underline{V}_3$ is applied) switch S_2 turns off and S_5 turns on resulting in $\underline{V}_0$. Now all lower devices are on and the load current flows through S_4, S_6 and D_5. The choice of the following vector is determined by the vector that approaches closest the demand vector $\underline{V}_{dem}$ and that uses only one or two of the remained unchanged poles. In this example it is vector $\underline{V}_1$. Once the on-state time of the second forcing vector has finished the resonant circuit must be activated again.





'Reso' stands for resonant mode.

Figure 3.3.11: Switching status and time period of the mPWM2 control method

So far both techniques need the help of the snubber mode. As the commutation time is proportional to the reciprocal of the load current it increases under light load conditions. This can be expressed with the equation (3.3.29):

$$V_{dc} = \frac{1}{2C}\int I_{load}\,dt = \frac{I_{load}\,T_{com}}{2C} \qquad (3.3.29)$$

with T_{com} is the time of the commutation process IGBT-Diode.

To avoid the extension of the commutation time with decreasing load current a resonant mode is needed that is faster than the commutation time when using snubber capacitors. This leads to the conclusion that under light load conditions the number of switching events of the resonant mode has to increase.

References [3.25, 3.30 and 3.31] investigated the output spectral performance of a hard switched inverter applying the conventional PWM scheme and the mPWM2 scheme where one pole is clamped to the upper or lower rail during one modulation period. (also called bus clamped space vector modulation). The results show that the bus clamped space vector modulation has a poor performance of the output spectral performance compared to the conventional PWM scheme at hardswitching converters. It is assumed that a comparison will come to the same conclusion [3.32] when applying both control schemes at PRDCL.

3.4 Quasi-Resonant DC-Link Inverter (q-RDCL)

The q-RDCL is the forth sub-topology in the RDCL family branch. The q-RDCL is a cross between the PRDCL and the clamp basic RDCL. Most of the proposed q-RDCL claim 'true' PWM controllability, improving the output spectral performance. Again many circuits have been proposed [3.33-3.42], but not all of the cited circuits show 'true' PWM control.

Two circuits are in the following further discussed because both of them show relatively good PWM performance [3.40 and 3.41]. The q-RDCL uses a clamp technique known from the basic clamp RDCL topology. Thus the q-RDCL must be divided into the active clamp q-RDCL topology and the passive clamp q-RDCL topology. The topology proposed in reference [3.41] uses an active clamp technique and the topology suggest in reference [3.40] uses the passive clamp version. Topology [3.41] is discussed first. All other cited topologies work in a similar but design distinctive way. Regrettably space does not permit explanation of all individual operation modes of each converter.

3.4.1 Principles of the active clamp q-RDCL

The operation modes during the resonant cycle are identical to the modes A, B, C (current boost mode, resonant mode and clamp mode) as discussed in the active clamp basic-RDCL topology in section 3.2. Differences between topology [3.41] and an active clamp basic RDCL include the position of the clamp capacitor and its operating voltage level. In section 3.2 the clamp capacitor is placed parallel to the resonant inductor and the capacitor is pre-charged to a lower level than that of the dc-link voltage. Topology [3.41] inserts the clamp capacitor parallel to the inverter and the capacitor is pre-charged to around 120% of the dc-link voltage.

Figure 3.4.1 shows the circuit and equivalent circuit of the proposed active clamp q-RDCL. An auxiliary zero voltage switching circuit is inserted between dc voltage source and the conventional inverter. The additional circuitry includes two switches (S_{clamp}, D_{clamp} and S_r, D_r), the clamp capacitor C_{clamp} and the resonant components L_r and C_r. To start the resonant cycle S_{clamp} and S_r are activated thus 120% of V_{dc} (the clamp voltage) appears across the inverter. The voltage drop across L_r allows to energy to be pumped into the inductor. Once enough energy is stored device S_c is switched off and a resonant mode is activated between C_r and L_r. The inverter input voltage reaches zero, swings back and is clamped via the clamp diode D_{clamp}. Six operation modes describe the converter operation.

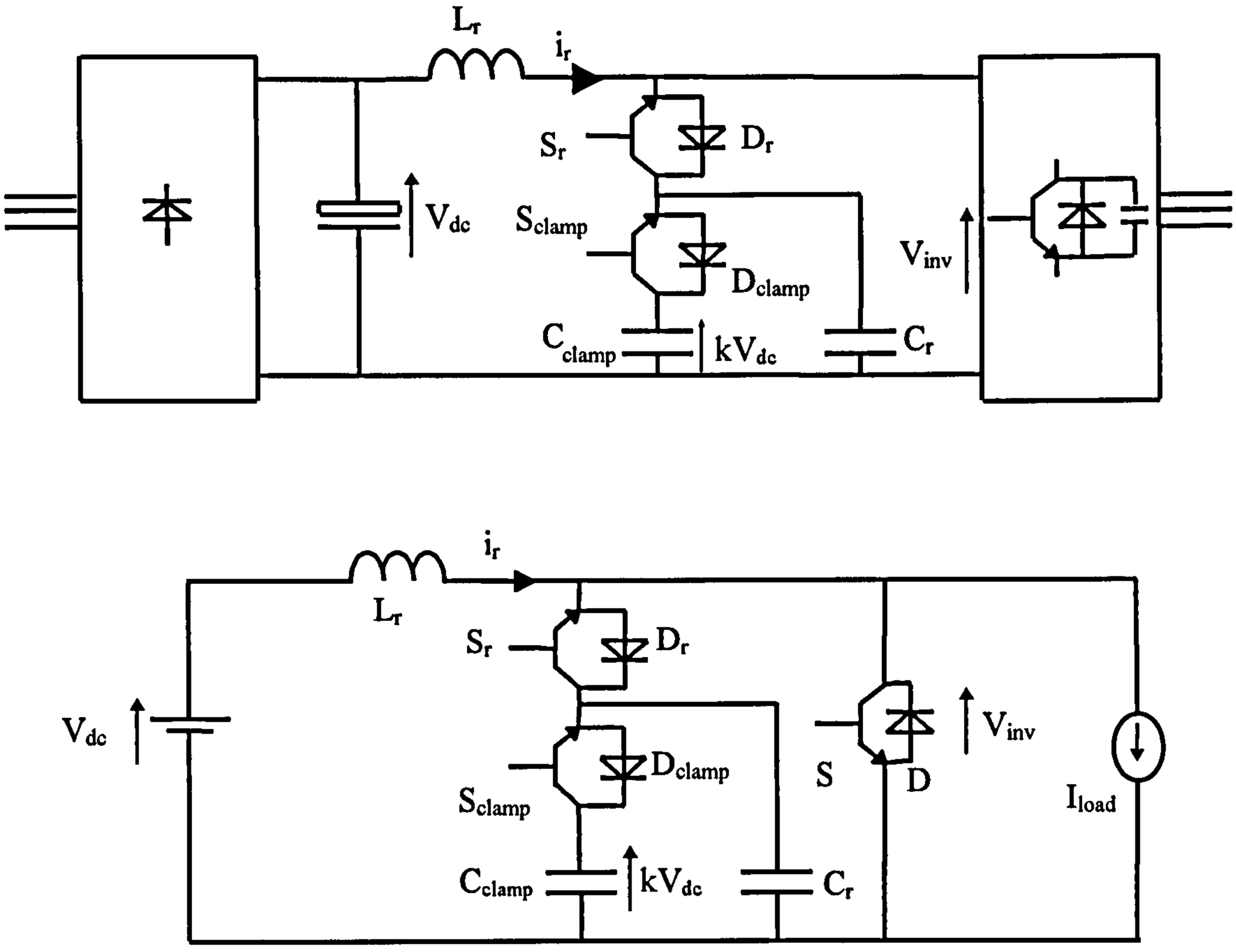


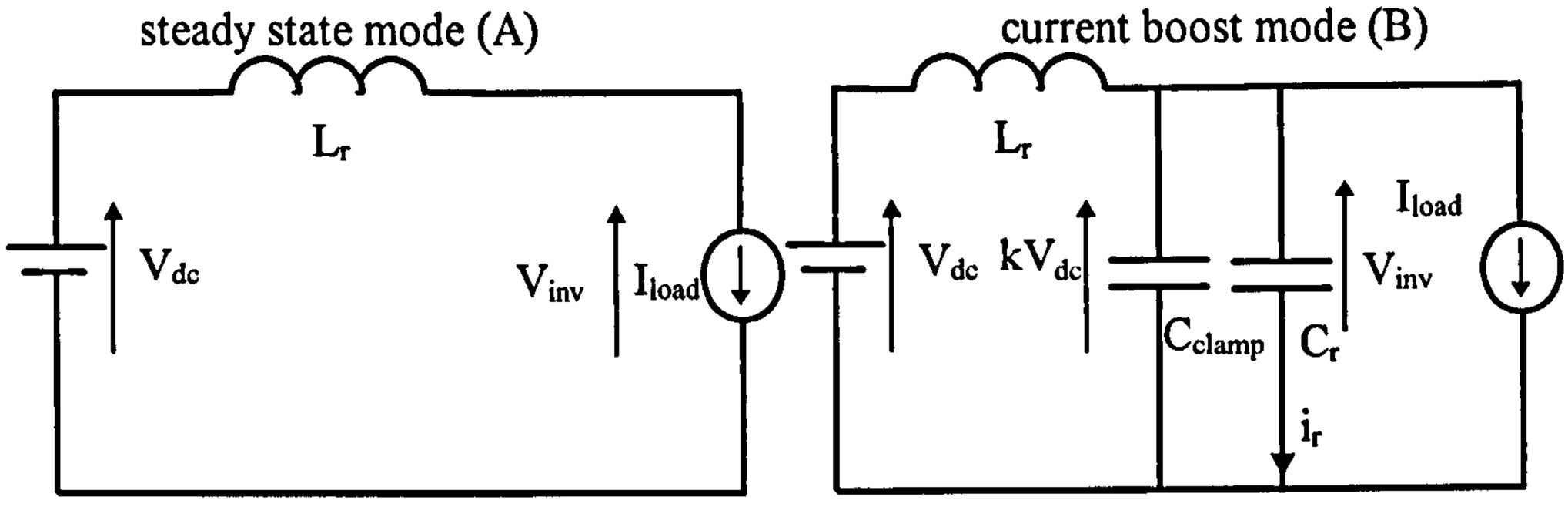
Figure 3.4.1: Schematic and equivalent circuit of the active clamp q-RDCL from reference [3.41]

3.4.2 Operation Modes of the active clamp q-RDCL

The operation modes of the active clamp q-RDCL are illustrated in Figure 3.4.2 to 3.4.5.

Steady state mode (A): S_{clamp} and S_r are off and the dc-link voltage is applied across the inverter input.

Current boost mode (B): When one of the switches in the inverter like to change its status both auxiliary devices are turned on and V_{inv} gets clamp to the defined voltage kV_{dc} across the clamp capacitor. In that time an increasing current is flowing from C_{clamp} to the dc-link capacitor.



$$V_{inv}(t) = V_{dc} \quad (3.4.1)$$

$$i_r(t) = 0A \quad (3.4.2)$$

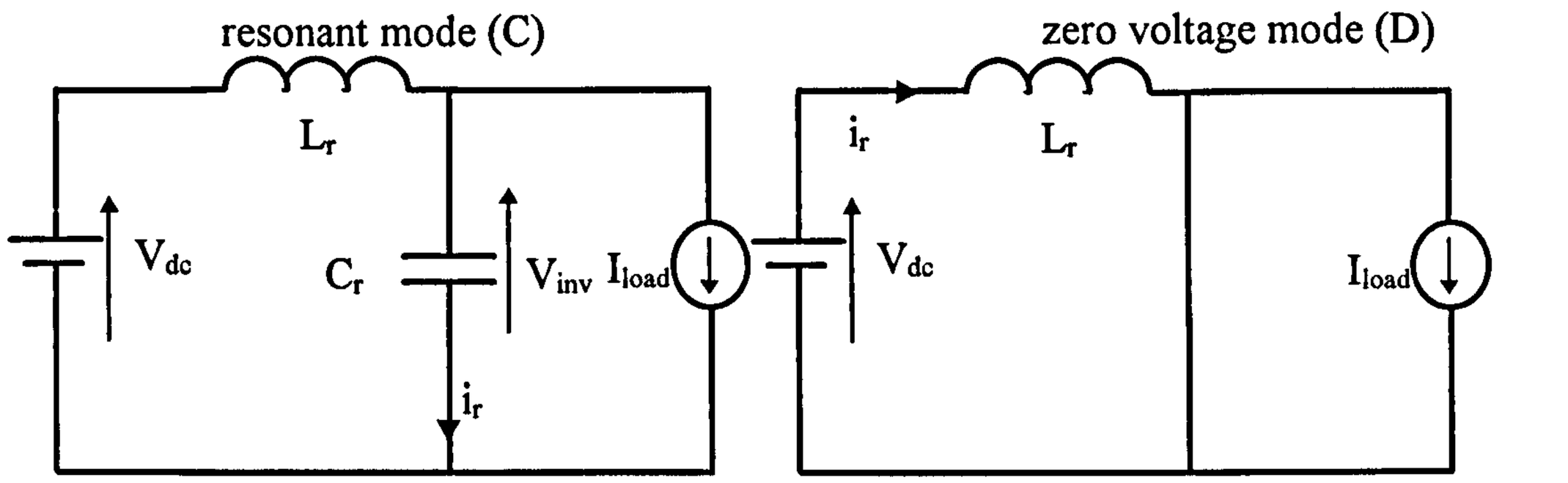
$$V_{inv}(t) = kV_{dc} \quad (3.4.3)$$

$$i_r(t) = \frac{1}{L_r}\int (kV_{dc} - V_{dc})dt \quad (3.4.4)$$

Figure 3.4.2: Operation modes A and B of the active clamp q-RDCL

Resonant mode (C): Once enough energy is stored in L_r (I_{r1}) the clamp device is switched off under zero voltage condition. Thus the input of the inverter is released from the clamp capacitor and the voltage V_{inv} resonates towards zero.

Zero voltage mode (D): The inverter input voltage reaches zero and the change of the inverter status can be carried out. During this time diode D is conducting and S is switched on under a lossless manner.



$$V_{inv}(t) = V_{dc}(1 - \cos\omega_0 t) + Z_0(I_{r1} - I_{load})\sin\omega_0 t \quad (3.4.5)$$

$$i_r(t) = \frac{1}{L_r}\int V_{inv}(t)dt \quad (3.4.6)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad (3.4.7)$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \quad (3.4.8)$$

$$V_{inv}(t) = 0V \quad (3.4.9)$$

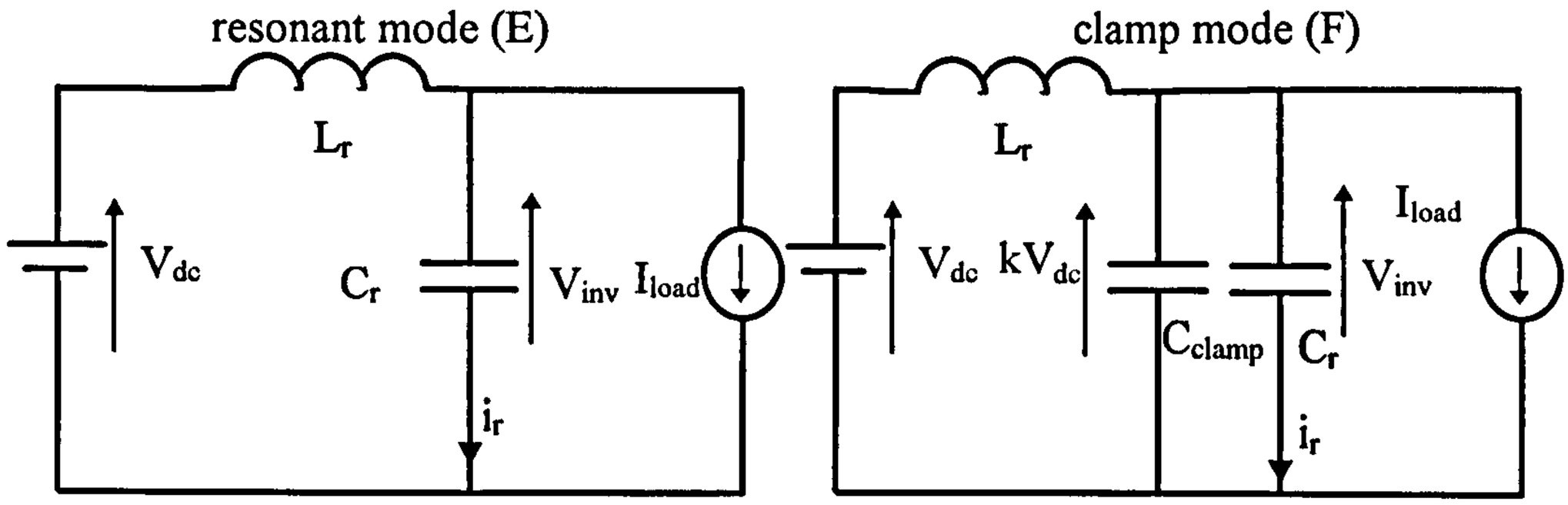
$$i_r(t) = \frac{V_{dc}}{L_r}t \quad (3.4.10)$$

I_{r1} is the remaining current stored in the inductor L_r after the device S_{clamp} is turned off.

Figure 3.4.3: Operation modes C and D of the active clamp q-RDCL

Resonant mode (E): The current direction flow of i_r changes from S_r to D_r, and S_r can be switched off under zero voltage conditions. The voltage V_{inv} resonates towards the dc-link value and overshoots.

Clamp mode (F): When V_{inv} is equal to the clamp voltage across the clamp capacitor $C_{clamp,}$, D_{clamp} gets forward bias. With D_{clamp} conducting the inverter input voltage is clamped. Once the energy is restored in the clamp capacitor the current flowing through D_{clamp} reaches zero Ampere and the voltage V_{inv} drops down to the dc-link value V_{dc}.



$$V_{inv}(t) = V_{dc}(1-\cos\omega_0 t) + Z_0(I_{r2} - I_{load})\sin\omega_0 t \quad (3.4.11)$$

$$i_r(t) = \frac{1}{L_r}\int V_{inv}(t)dt \quad (3.4.12)$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad (3.4.13)$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \quad (3.4.14)$$

$$V_{inv}(t) = kV_{dc} \quad (3.4.15)$$

$$i_r(t) = \frac{1}{L_r}\int (kV_{dc} - V_{dc})dt \quad (3.4.16)$$

I_{r2} is the remaining current stored in the inductor L_r after diode D_{clamp} starts conducting.

Figure 3.4.4: Operation modes E and F of the active clamp q-RDCL

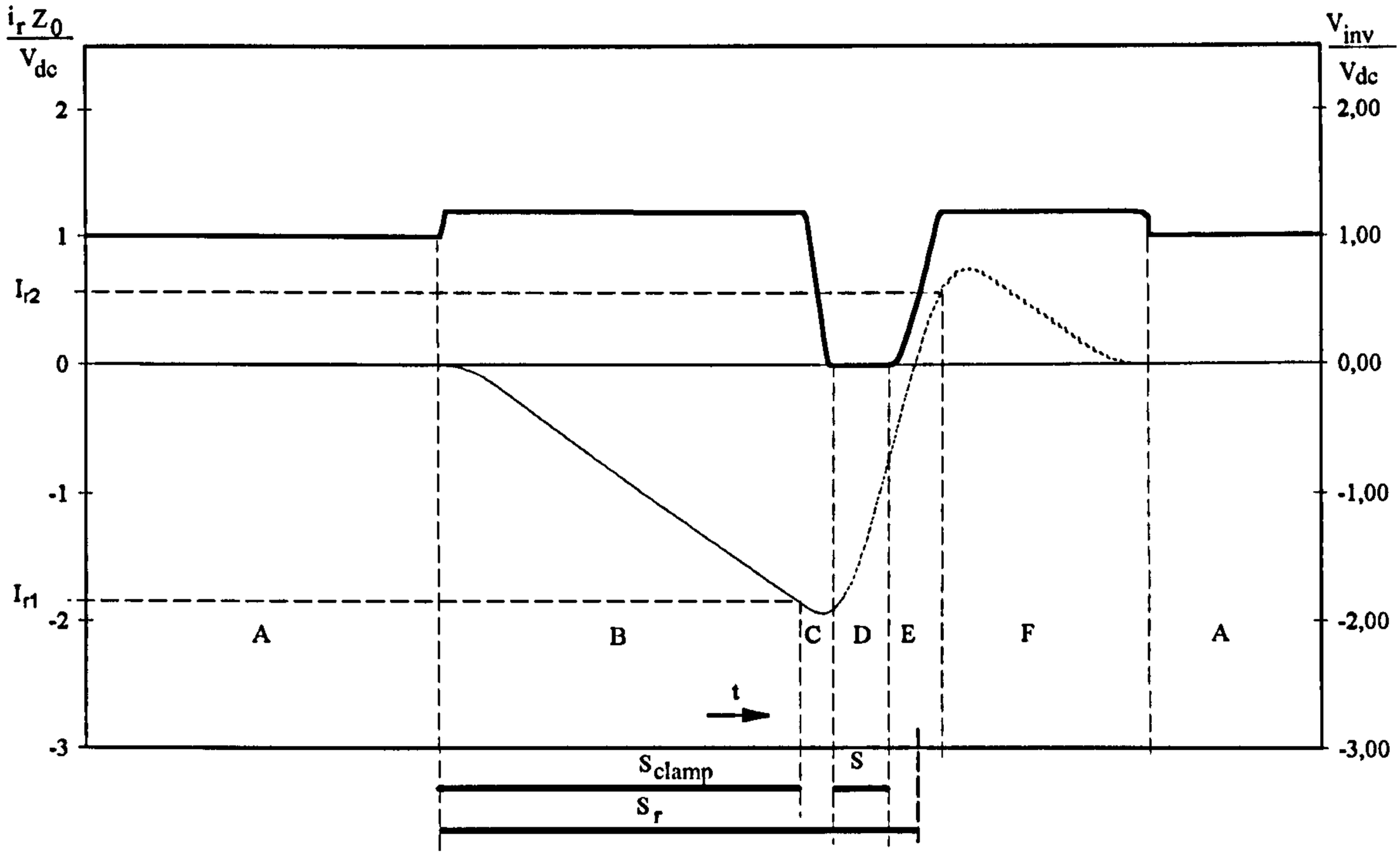


Figure 3.4.5: Normalised waveforms V_{inv} (bold line) and i_r (solid line) of the active clamp q-RDCL [3.41]

3.4.3 Principles of the passive clamp q-RDCL

The author in reference [3.40] inserts a transformer between dc-link capacitor and input of the inverter allowing the voltage to be clamped using the passive clamp technique. In addition, the circuit consists of a small additional inductor, two switches, which are driven from the same gating signal and two diodes (see Figure 3.4.6). This additional circuitry is needed to allow PWM control. Because the resonant mode and clamp mode are exactly the same as already discussed in the passive clamp basic RDCL topology the operation modes will not be discussed in detail here.

The general operation can be described as follows: Before a resonant cycle is initiated the inverter input voltage is clamped to the dc-link voltage (assuming the resonant inductance is small compared to the load inductance), the auxiliary inductor L_{r2} is reset to zero current conditions and both auxiliary switches are off. Whenever a PWM switching command is generated, both auxiliary switches are turned on (under zero current conditions) to initiate a resonant transition. The dc-link voltage is applied via C_r and forces the inductor current i_{Lr2} to increase. Once i_{Lr2} is larger than the load current a second resonant mode is activated (resonant circuit: C_r-L_{r1}-L_{r2}) and the inverter input voltage resonates to zero. This mode will be maintained (circuit: L_{r1}-L_{r2}) until the auxiliary switches turn-off. Than the voltage resonates towards the dc-link value and overshoots this value until it reaches kV_{dc}, k is the clamp factor

given in equation 3.2.20. The current in L_{r2} flows through both auxiliary diodes and decays to zero. Once this current reaches zero the steady state mode remains.

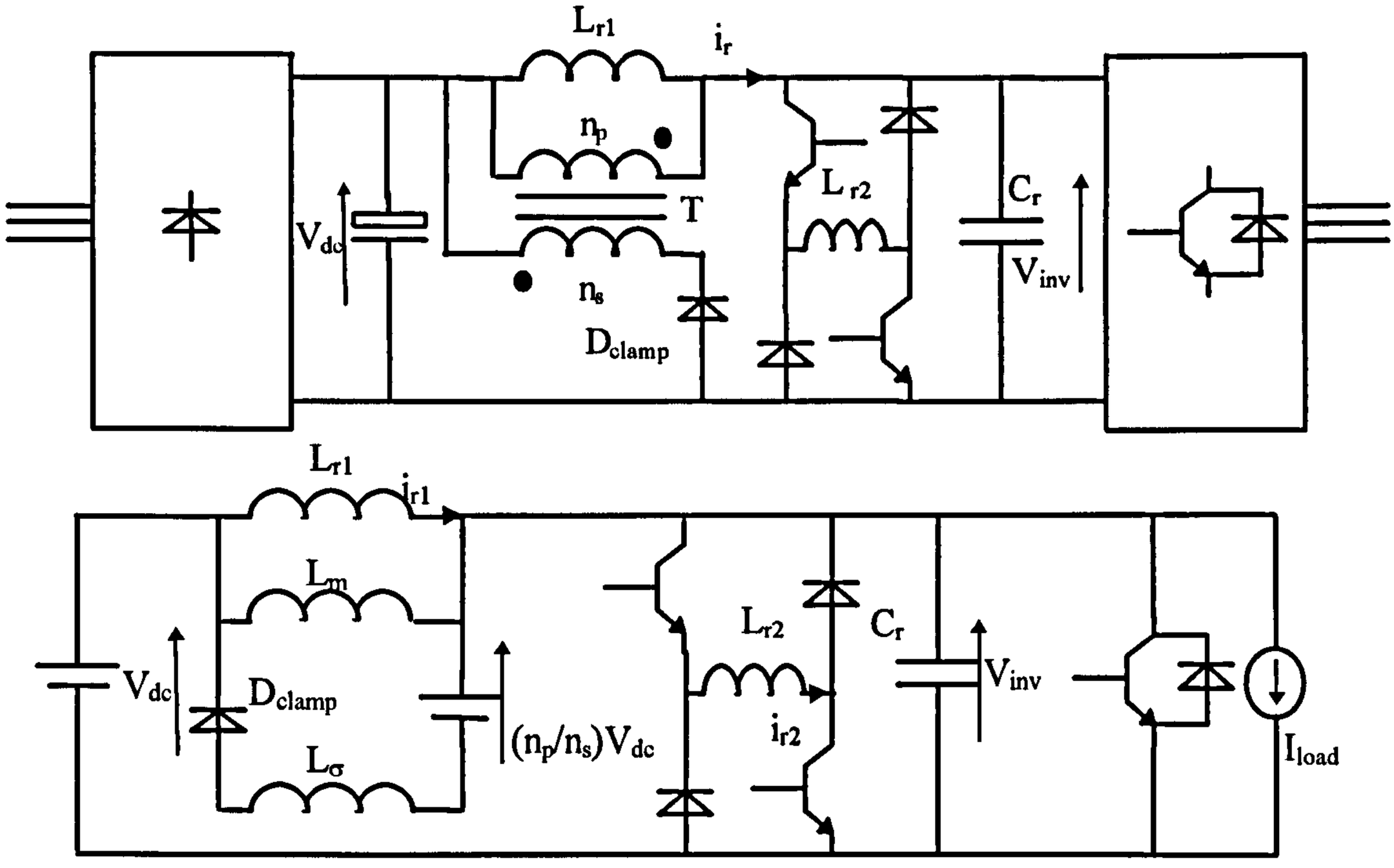


Figure 3.4.6: Schematic and equivalent circuit of the passive clamp q-RDCL proposed in reference [3.40]

Figure 3.4.7 shows the inverter input voltage of the passive clamp q-RDCL from reference [3.40] over one resonant cycle. As can be seen, the voltage oscillates during the clamp mode. The reason for this ringing is the leakage inductance between the primary and secondary winding. Own simulation results showed on one hand that the ringing becomes worse if the leakage inductance increases, on the other hand an increase in the clamp factor leads to a shorter on-state time of the clamp mode. A small clamp factor leads to the extreme that the clamp mode suppress the steady-state mode. In this case current circulates continuously in the transformer leading to high losses.

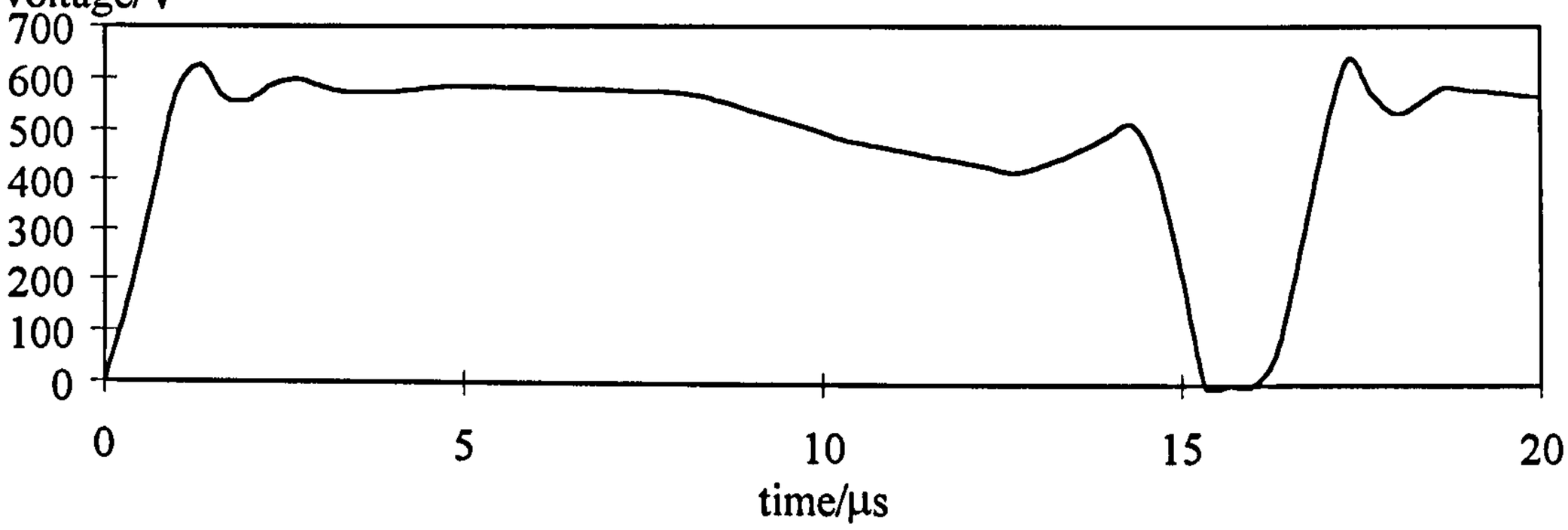


Figure 3.4.7: Simulated inverter input voltage waveform of the passive clamp q-RDCL [3.40] (see also Appendix A)

Chapter 4

POLE COMMUTATED INVERTERS

Chapter 4 analyses Pole Commutated Inverters (PCIs) in the same manner as Chapter 3 analysed RDCL topologies. Again the study of each topology is based on an introduction of a simplified circuit followed by a step by step analysis of each individual operation mode. In spite the fact that PCIs using three identical resonant circuits for each pole, only one pole of each topology is analysed and drawn in the schematic. All statements and theoretical expressions apply therefore to the other two poles. Concerning the development of the equivalent circuit, the assumptions described at the beginning of Chapter 3 are once again assumed. Simulation results are given in Appendix A.

PCIs can be classified into two subgroups: Resonant Pole Inverters (RPI) and Auxiliary Resonant Pole Inverters (ARPI). The RPI topology does not need an additional switch to achieve zero voltage or zero current switching, whereas the ARPI needs support from one or more auxiliary switches. Figure 4.1 shows the family tree of the PCI.

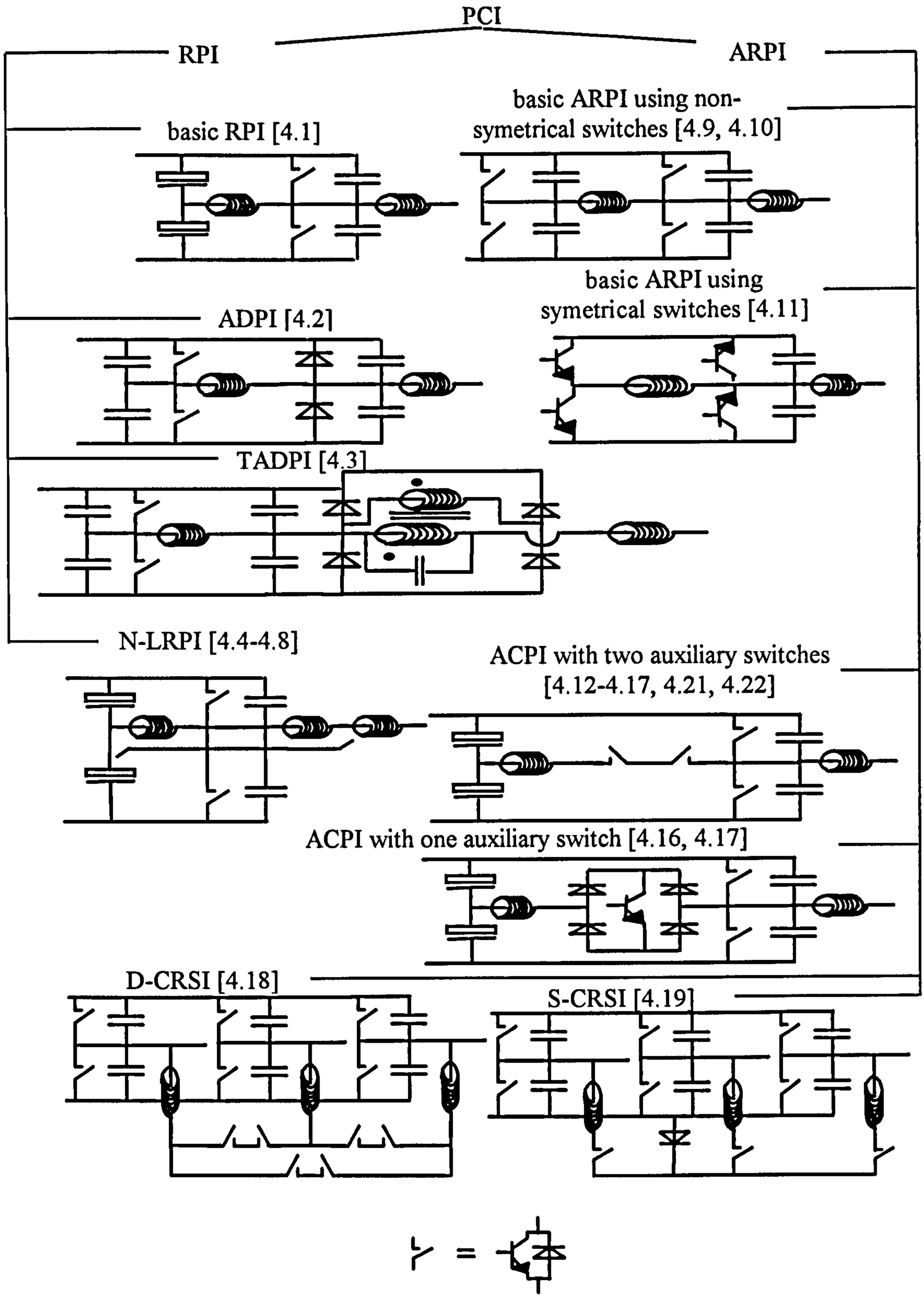


Figure 4.1: Family tree of the PCI topology. All schematics show only one pole including the phase motor inductance (except D-CRSI and S-CRSI where the complete inverter is shown).

4.1 Resonant Pole Inverters (RPI)

The principles of all RPI inverters are generally speaking the same. A resonant inductor is inserted, connecting the output phase with auxiliary components, that are joined to the dc-link. The inductor carries permanently the current during the operation time of the inverter and has two major functions. Firstly it offers a 'freewheeling mode' or sometimes called 'clamp mode'. In this mode the switching status of the pole remains constant and a constant current is flowing through the inductor (except in the basic RPI, where the current is further increasing [4.1]). Depending on the direction of the load current the freewheeling current is larger or smaller than the load current level. Secondly the inductor offers the resonant mode allowing to change the pole status under softswitching conditions. Both main modes: freewheeling mode and resonant mode, alternate frequently controlled from the PWM controller.

The principle of the RPI is analysed with the help of the Auxiliary Diode Commutated Resonant Pole Inverter (ADPI) [4.2]. The principals of the other RPI topologies are similar and can be abbreviated from the operation modes of the ADPI circuit.

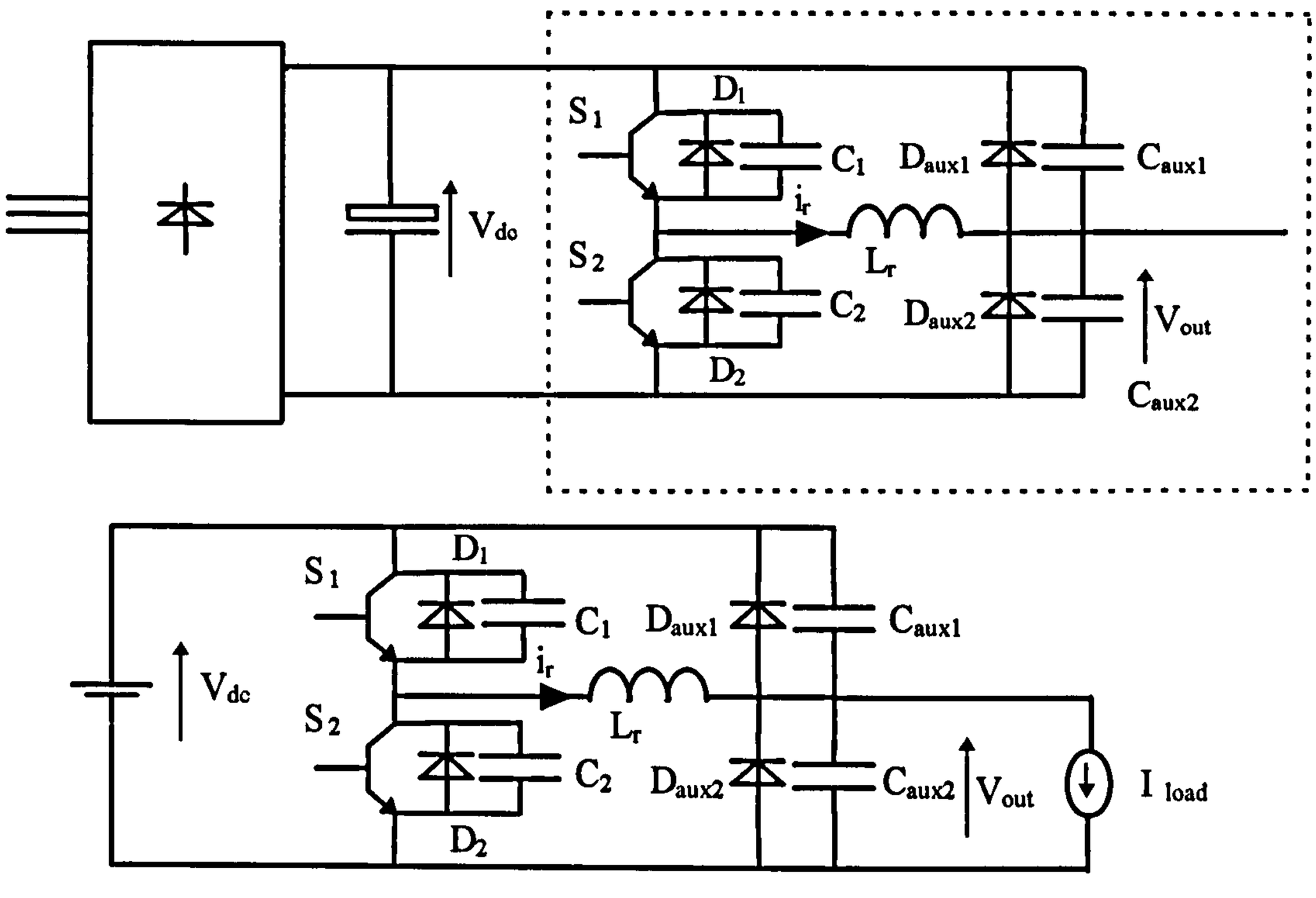
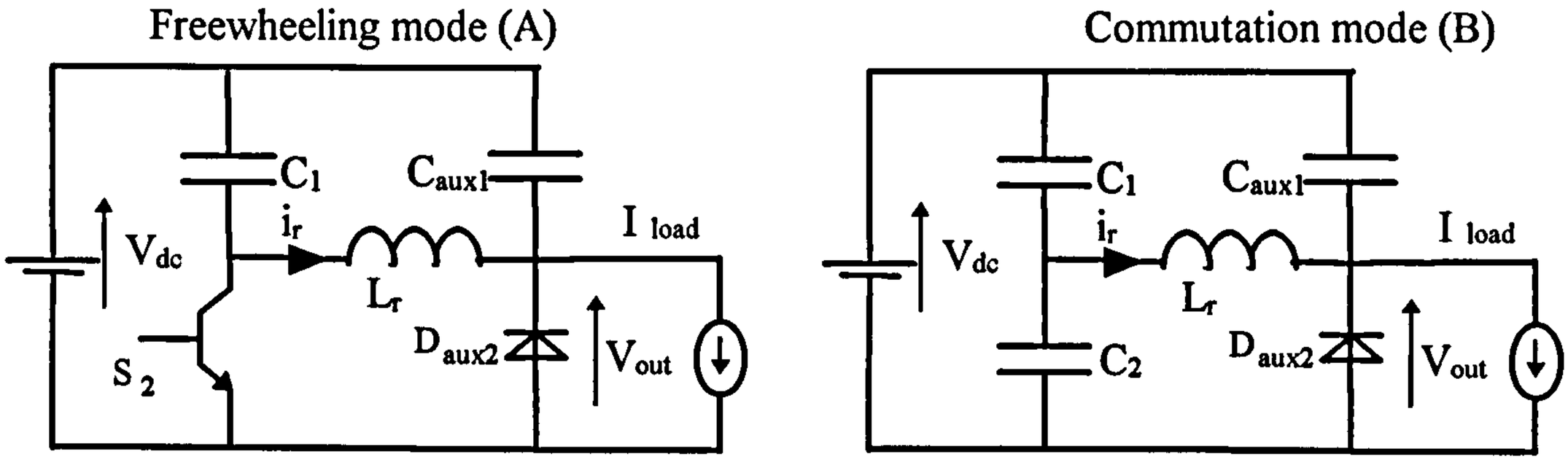


Figure 4.1.1: Schematic and equivalent circuit of one pole of the ADPI

The circuits analysing the operation modes of the ADPI are given in Figures 4.1.2 to 4.1.6. Figure 4.1.7 shows the normalised waveform of inductor current i_r and phase output voltage (V_{out}).

Freewheeling mode (A): To start with, it is assumed that the freewheeling diode D_{aux2} and the IGBT S_2 are conducting (Figure 4.1.2). D_{aux2} conducts the load current I_{load} and the current i_r and switch S_2 conducts the current i_r. The current i_r is negative (I_{r1}) and the voltage V_{out} is clamped to zero. This mode stays on for so long until the controller commands to change the pole status.

Commutation mode (B): With IGBT S_2 conducting the device turns-off and commutation takes place between S_2 and D_1. The commutation process is provided with the help of capacitor C_2 that acts as snubber capacitor. Because the impedance of inductor L_r is larger than the impedance of both capacitors C_1 and C_2 the current i_r remains constant at I_{r1} during the commutation mode B.



$$V_{out}(t) = 0V \qquad (4.1.1)$$

$$i_r(t) = I_{r1} \qquad (4.1.2)$$

$$V_{out}(t) = 0V \qquad (4.1.3)$$

$$i_r(t) = I_{r1} \qquad (4.1.4)$$

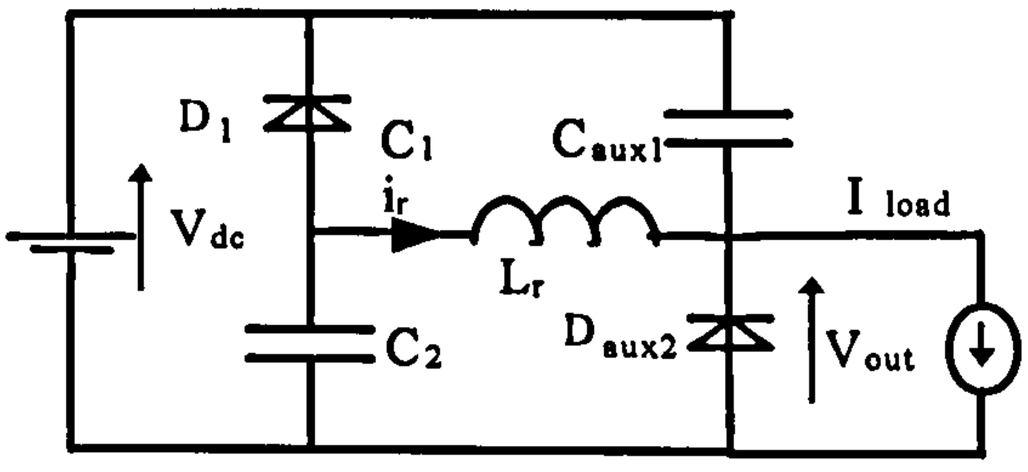
I_{r1} is the remaining current stored in the inductor L_r during the previous freewheeling mode.

Figure 4.1.2: Operation modes A and B of the ADPI

Current ramp-up mode (C): With diode D_1 conducting the current i_r increases towards positive current levels. The source of the current ramp-up operation is the positive applied voltage V_{dc} across inductor L_r.

Current ramp-up mode (D): The current direction of i_r reverses its direction and IGBT S_1 carries the inductor current. The voltage V_{out} is still clamped to zero volts.

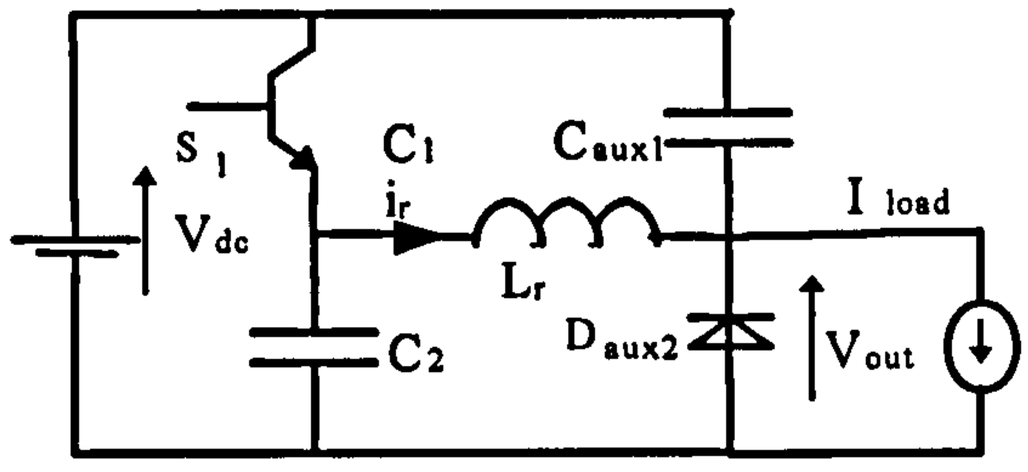
Current ramp-up mode (C)



$$V_{out}(t) = 0V \qquad (4.1.5)$$

$$i_r(t) = I_{r1} + \frac{V_{dc}}{L_r}t \qquad (4.1.6)$$

Current ramp-up mode (D)



$$V_{out}(t) = 0V \qquad (4.1.7)$$

$$i_r(t) = I_{r1} + \frac{V_{dc}}{L_r}t \qquad (4.1.8)$$

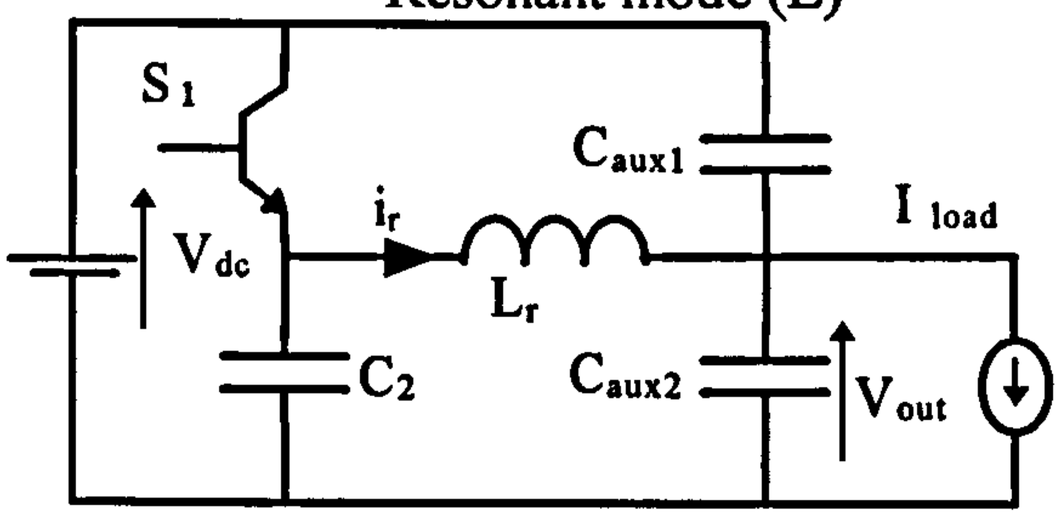
I_{r1} is the remaining current stored in the inductor L_r during the previous freewheeling mode.

Figure 4.1.3: Operation modes C and D of the ADPI

Resonant mode (E): The current i_r is equal I_{load} and the circuit becomes a resonant circuit with the elements L_r , C_{aux1} and C_{aux2} . The current i_r resonates upwards above the load current. The voltage across C_{aux1} resonates to zero and the voltage across C_{aux2} resonates to the dc-link value. The resonant transition stops when diode D_{aux1} gets forward biased.

Freewheeling mode (F): Diode D_{aux1} conducts and the inductor L_r carries at least twice the load current. This stage remains until the next incoming control signal commands to change the switching status of the pole.

Resonant mode (E)



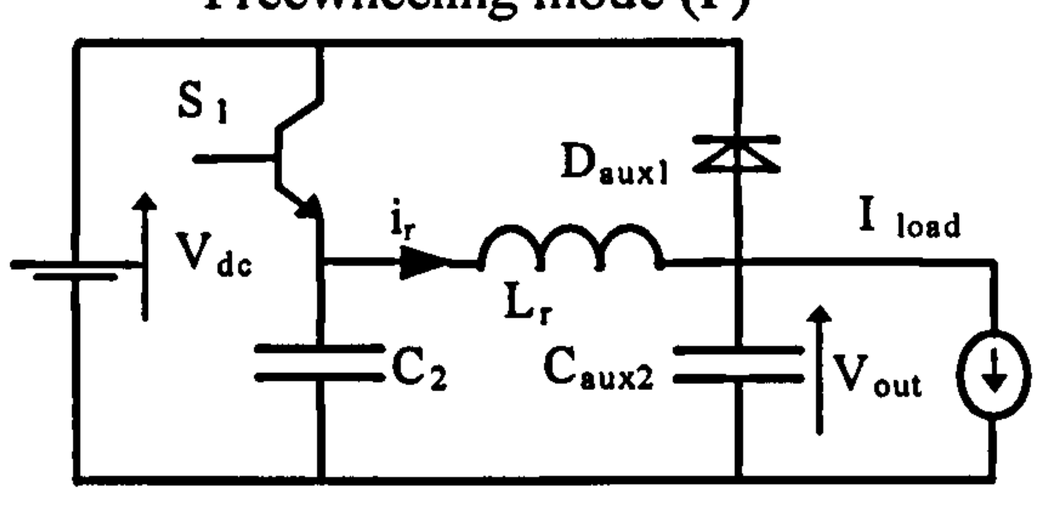
$$V_{out}(t) = V_{dc}(1 - \cos\omega_0 t) + I_{load} Z_0 \sin\omega_0 t \qquad (4.1.9)$$

$$i_r(t) = I_{load} + \frac{1}{L_r}\int (V_{dc} - V_{out}(t))dt \qquad (4.1.10)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_{aux1} + C_{aux2})}} \qquad (4.1.11)$$

$$Z_0 = \sqrt{\frac{L_r}{C_{aux1} + C_{aux2}}} \qquad (4.1.12)$$

Freewheeling mode (F)



$$V_{out}(t) = V_{dc} \qquad (4.1.13)$$

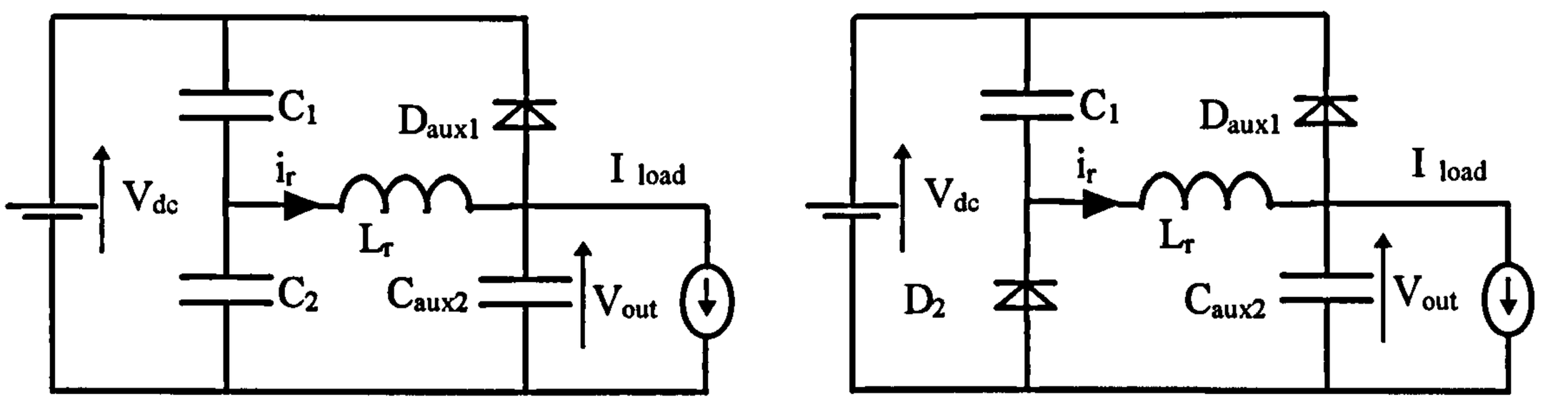
$$i_r(t) = I_{load} + \frac{V_{dc}}{Z_0} \qquad (4.1.14)$$

with Z_0 from equation 4.1.12

Figure 4.1.4: Operation modes E and F of the ADPI

Commutation mode (G): Before the pole status is changed, IGBT S_1 turns off and the current in the inductor L_r forces the voltage across diode D_2 to zero with the help of capacitor C_1 (see snubber mode section 3.3.2).

Current ramp-down mode (H): Diode D_2 conducts and a negative voltage V_{dc} is applied across inductor L_r. Thus current i_r starts to decrease.



$$V_{out} = V_{dc} \quad (4.1.15)$$

$$i_r(t) = I_{load} + \frac{V_{dc}}{Z_0} \quad (4.1.16)$$

with Z_0 from equation 4.1.12

$$V_{out} = V_{dc} \quad (4.1.17)$$

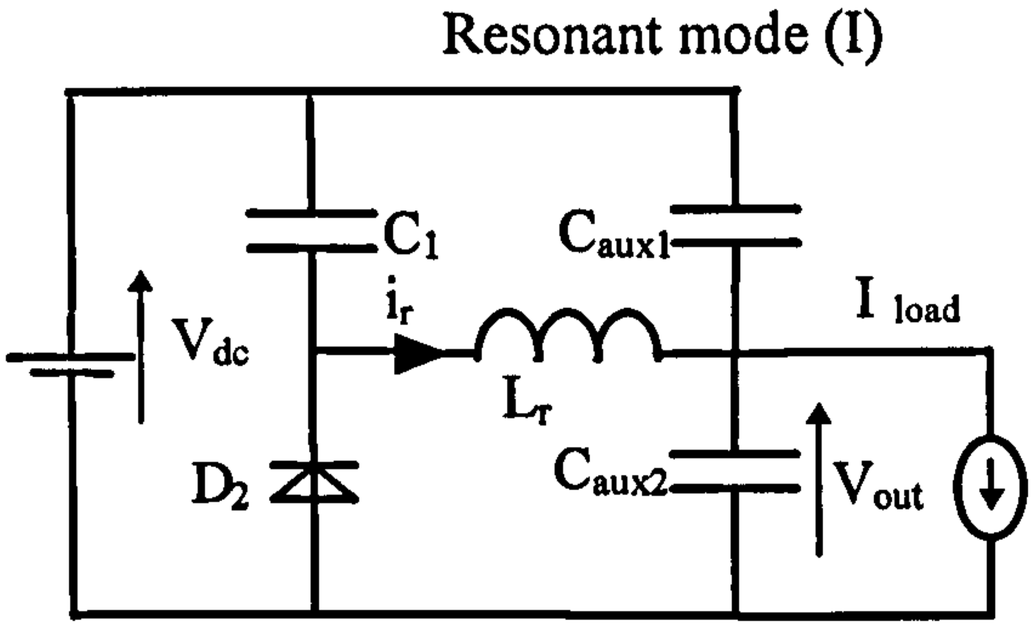
$$i_r(t) = I_{load} + \frac{V_{dc}}{Z_0} - \frac{V_{dc}}{L_r}t \quad (4.1.18)$$

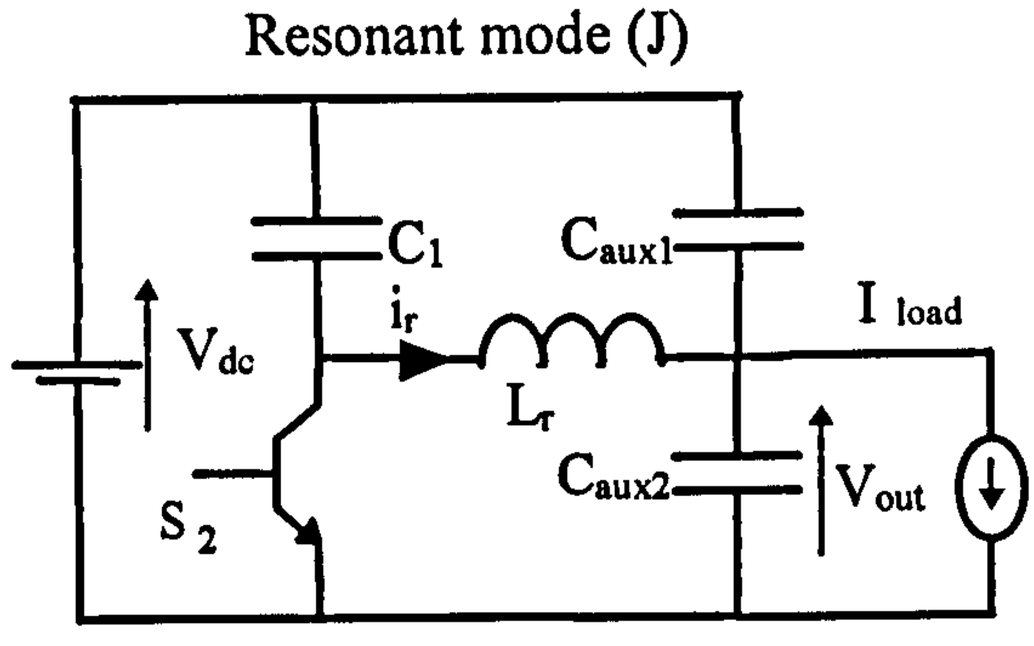
with Z_0 from equation 4.1.12

Figure 4.1.5: Operation modes G and H of the ADPI

Resonant mode (I): The current i_r ramps down until it becomes equal the load current I_{load}. The resonant inductor L_r resonates with C_{aux1} and C_{aux2}. The resonant current i_r commutates from D_2 to S_2 naturally as i_r reverses (Figure 4.1.7).

Resonant mode (J): The current direction of i_r is negative and IGBT S_2 conducts. The voltage V_{out} resonates to zero during the resonant mode and gets clamped to zero volts once diode D_{aux2} takes over to carry the load current.





$$V_{out}(t) = V_{dc}\cos\omega_0 t + I_{load} Z_0 \sin\omega_0 t \qquad (4.1.19)$$

$$i_r(t) = I_{load} - \frac{1}{L_r}\int V_{out}(t)dt \qquad (4.1.20)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_{aux1} + C_{aux2})}} \qquad (4.1.21)$$

$$Z_0 = \sqrt{\frac{L_r}{C_{aux1} + C_{aux2}}} \qquad (4.1.22)$$

$$V_{out}(t) = V_{dc}\cos\omega_0 t + I_{load} Z_0 \sin\omega_0 t \qquad (4.1.23)$$

$$i_r(t) = I_{load} - \frac{1}{L_r}\int V_{out}(t)dt \qquad (4.1.24)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_{aux1} + C_{aux2})}} \qquad (4.1.25)$$

$$Z_0 = \sqrt{\frac{L_r}{C_{aux1} + C_{aux2}}} \qquad (4.1.26)$$

Figure 4.1.6: Operation modes I and J of the ADPI

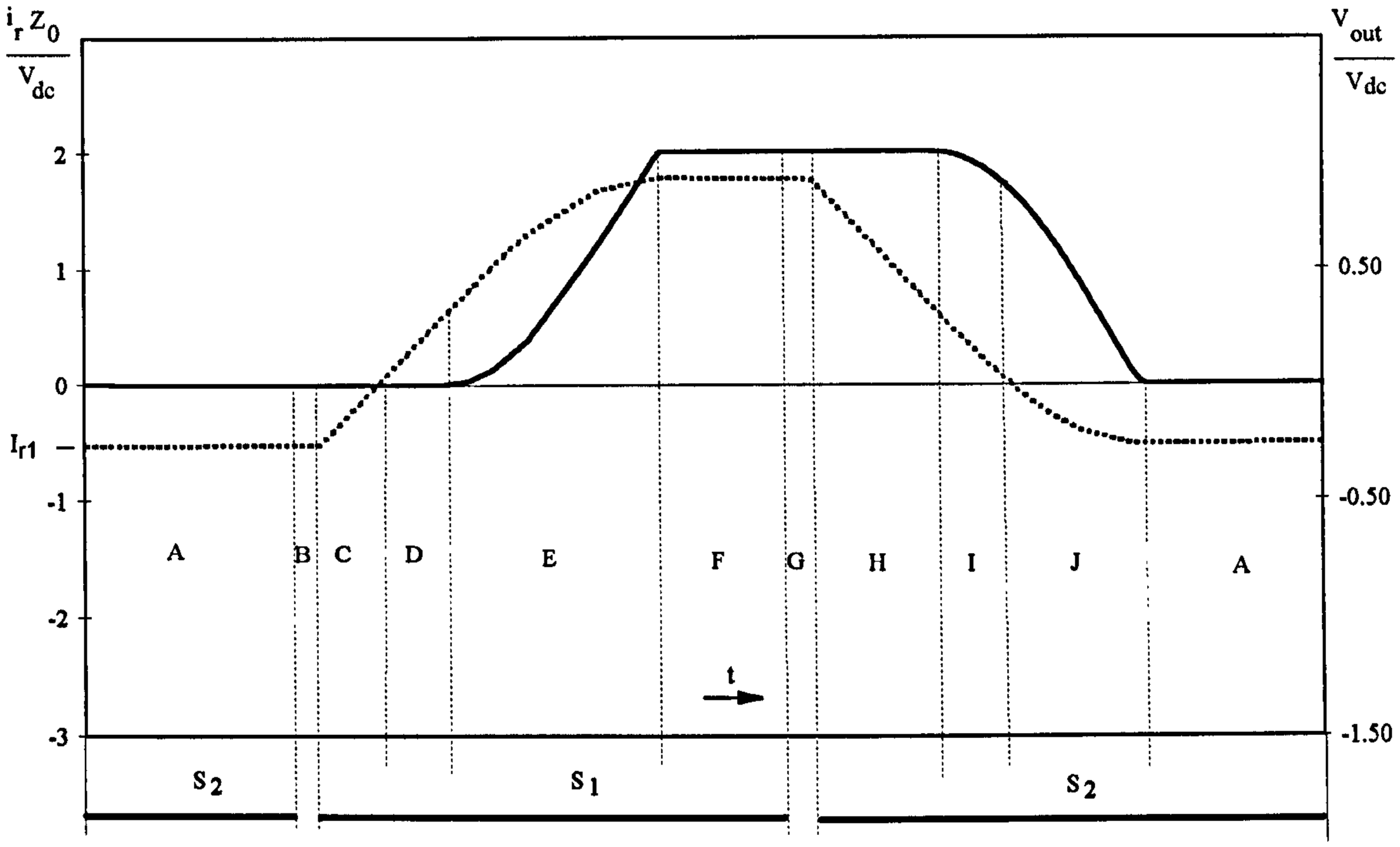


Figure 4.1.7: Normalised waveform of V_{out} (solid line) and i_r (dashed line) over one pole commutation cycle of the ADPI

The high freewheeling current of the ADPI topology is reduced when inserting a transformer into the output phase of the ADPI. This is reported in reference [4.3] and the topology is called

Transformer assisted ADPI (TADPI in Figure 4.1). Both topologies make use of additional diodes connected at the phase output (called D_{aux1} and D_{aux2} in the ADPI topology) allowing control over both the inductor freewheeling time and the peak inductor current. Figure 4.1.8 shows a simulation result comparing both topologies under same load conditions. The maximum freewheeling current level of the TADPI is reduced by around 20% compared to the ADPI topology (simulation parameters are given in Appendix A).

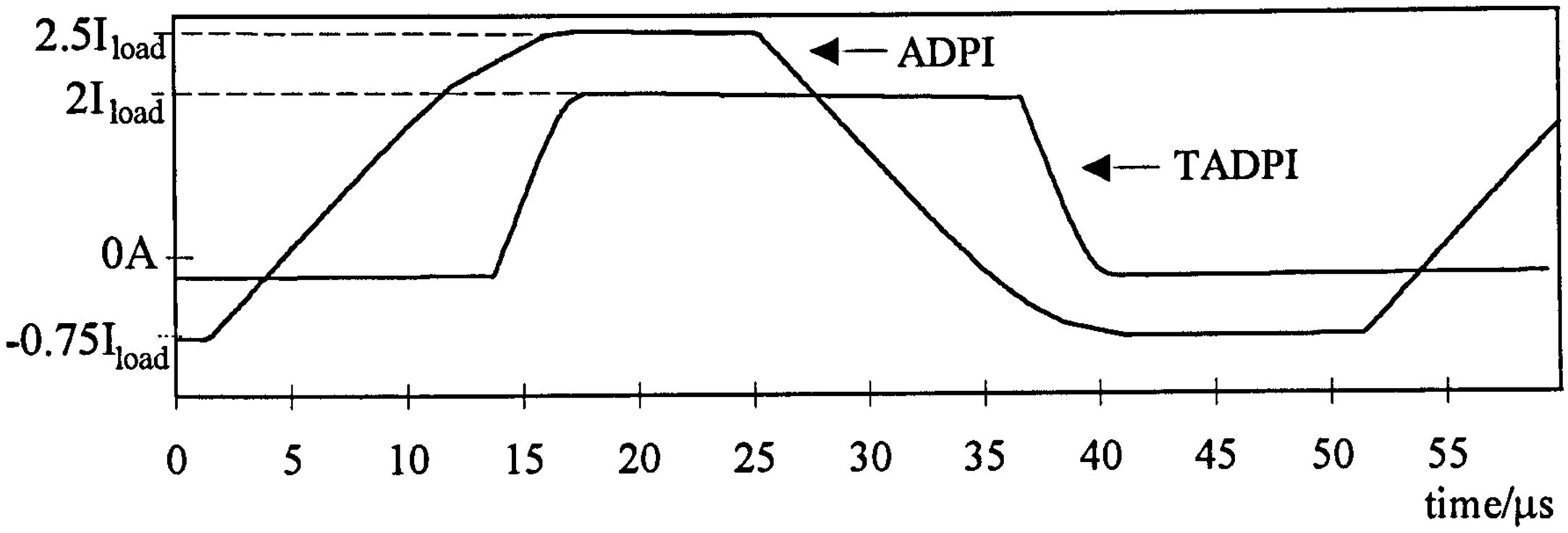


Figure 4.1.8: Inductor current waveforms of the ADPI and TADPI (Simulation results from Appendix A)

In contrast to ADPI and TADPI the basic RPI [4.1] (Figure 4.1) operates without freewheeling current. Instead the current ramps up and down in the resonant inductor. When the controller commands a change in the switching status the current in the inductor is high enough to supply the resonant circuit with sufficient energy. Regrettably the range of PWM control is limited by the need to transfer sufficient energy into the resonant inductor at low duty ratios whilst keeping the inductor current within sensible limits at high duty ratios. To allow a reasonable degree of PWM control, the peak current has to be higher than 3 p.u. [4.1].

All RPI circuits suffer from the high current flow in the inductor that results in losses. The current waveform of a Non-Linear Commutated Resonant Pole Inverter (N-LRPI) [4.4-4.8], displays a considerably lower inductor current. The freewheeling current can be reduced to as low as the load current (1 p.u.), however the saturable reactor that enables a low freewheeling current also requires a variable frequency control technique to be applied [4.8].

4.2 Auxiliary Resonant Pole Inverters (ARPI)

The inherent freewheeling current of the RPI topology limits PWM controllability, because of the long transition time between building up and transferring current into the resonant inductor especially under light load conditions. To increase PWM controllability additional switches are needed to control the inductor current in a more appropriate way. The topology that makes

use of additional devices in a Pole Commutated Inverter is known as Auxiliary Resonant Pole Inverter (ARPI, Figure 4.1).

The dc-link converter provides in general three of theses sources: upper rail (full dc-link voltage), lower rail (zero volts) and midpoint of the dc-link capacitors (half the dc-link voltage). This allow to determine when to force current flow into the inductor and the amount of current. The Auxiliary Commutated Resonant Pole Inverter (ACPI) makes use of the midpoint of the dc-link voltage (Figure 4.1), whereas all other ARPIs tap the upper and lower rail of the dc-link voltage or are connected to the neighbouring phases (D-CRSI, S-CRSI in Figure 4.1). In the following, the basic ARPI and the ACPI topologies are discussed in detail.

4.2.1 Basic Auxiliary Resonant Commutated Pole Inverter (basic ARPI)

The arrangements of the auxiliary switches varies with the topology (Figure 4.1). Reference [4.11] uses devices without antiparallel diodes. In this configuration all devices must withstand the dc-link voltage under forward and reverse blocking voltage. Thus symmetrical devices are the backbone of this topology. At the moment only symmetrical thyristors are commercially available (Chapter 1). In addition the inverter is unable to be PWM controlled [4.20], thus hysteresis control must be applied.

Its counter part is presented in reference [4.1] and makes use of four IGBTs with antiparallel diodes as known in conventional hardswitching converters. This arrangement allows PWM control. In addition the four switches can be controlled in two different ways, either pole commutation takes place with a freewheeling current or without freewheeling current [4.10], as it is shown later. This section describes now in detail the operation modes of the topology proposed in reference [4.1].

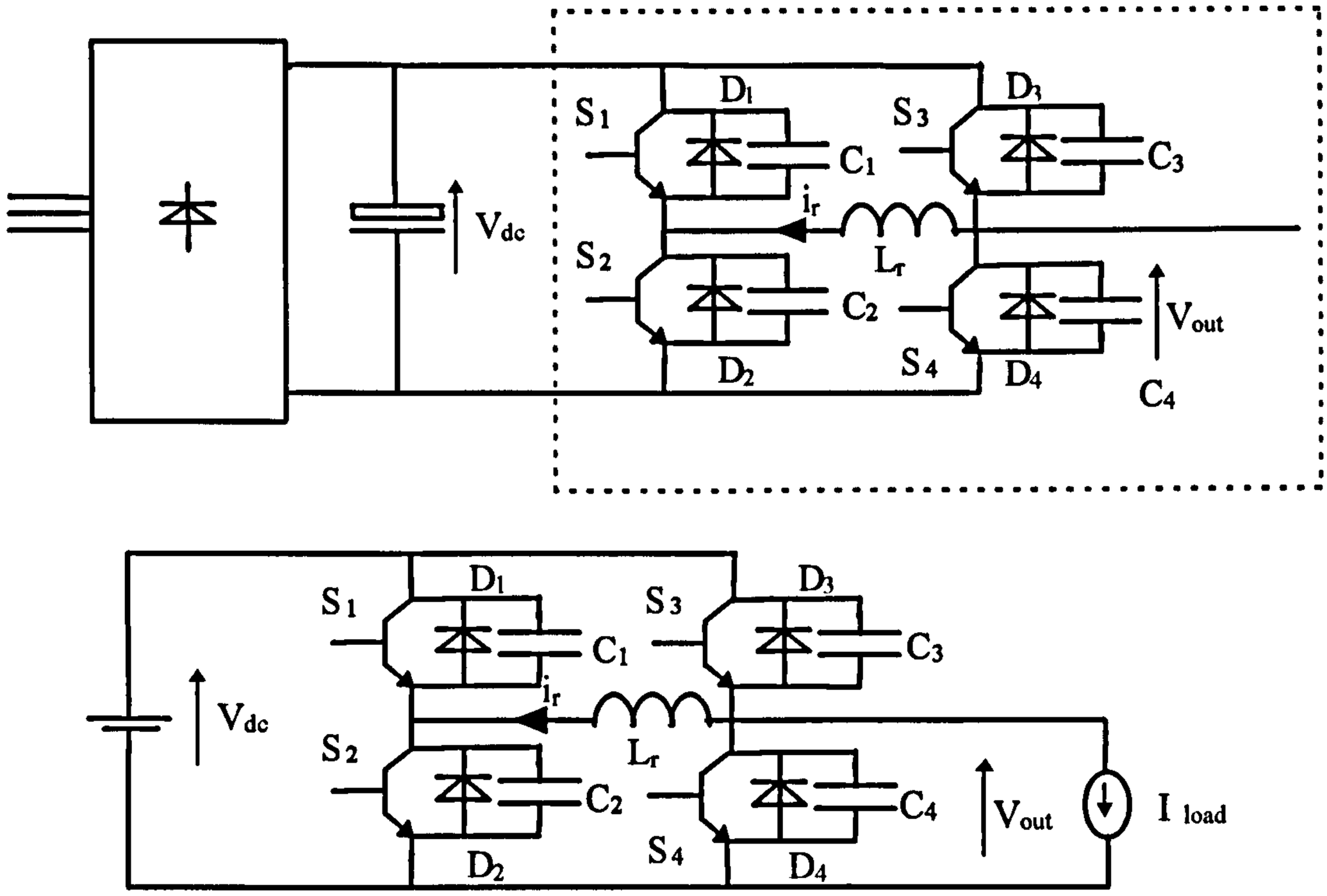


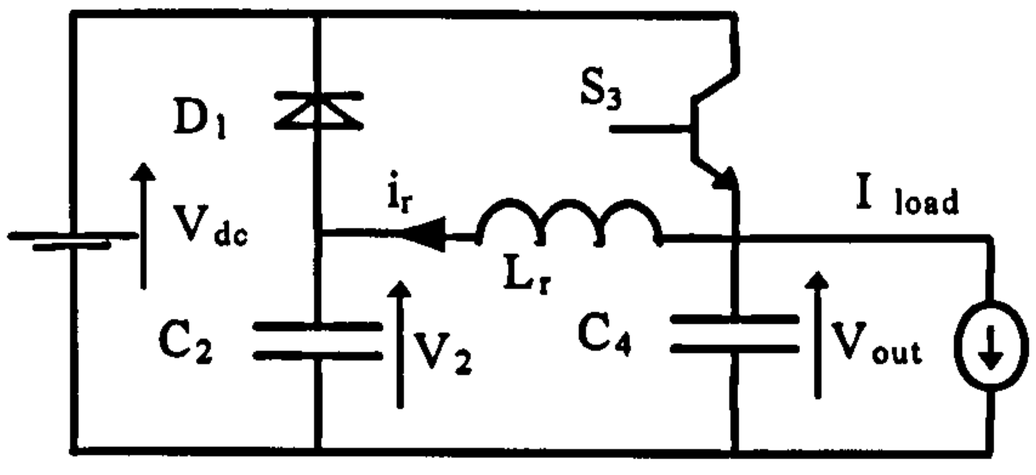
Figure 4.2.1: Schematic and equivalent circuit of one pole of the basic ARPI using non-symmetrical switches

The circuit analysis of the basic ARPI is based on twelve operation modes (Figures 4.2.2 to 4.2.8).

Freewheeling mode (A): A constant current I_{r1} is flowing through IGBT S_3, diode D_1 and inductor L_r. The current I_{r1} is larger than the load current I_{load}. The voltages V_{out} and V_2 are clamped to the dc-link voltage V_{dc}. This status remains until the controller demands change in pole status.

Resonant mode (B): Turning off IGBT S_3 results in oscillation between inductor L_r and capacitors C_3 and C_4. The voltage V_{out} resonates to zero, whereas voltage V_2 remains at the dc-link voltage level. The inductor current i_r starts to ramp down.

Freewheeling mode (A)

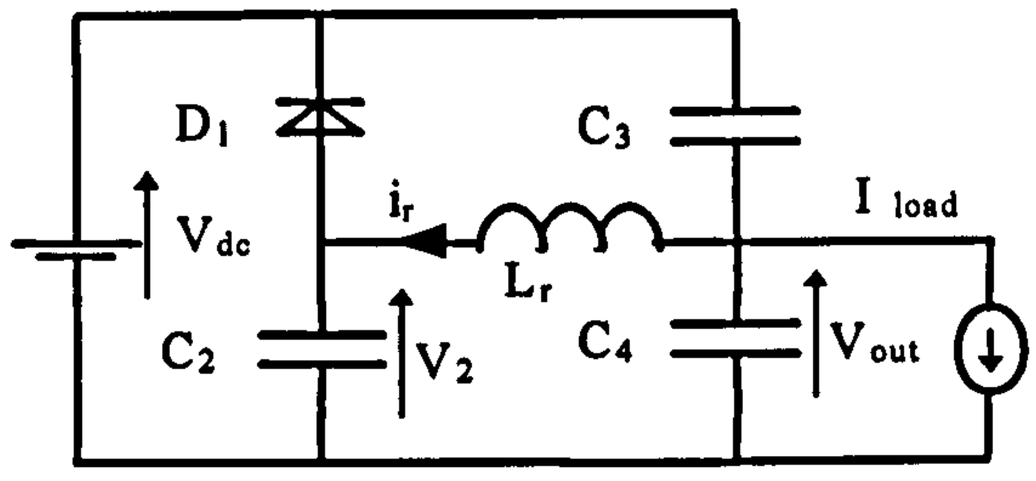


$$V_{out}(t) = V_{dc} \qquad (4.2.1)$$

$$V_2(t) = V_{dc} \qquad (4.2.2)$$

$$i_r(t) = I_{r1} \qquad (4.2.3)$$

Resonant mode (B)



$$V_{out}(t) = V_{dc}\cos\omega_0 t - I_{r1}Z_0 \sin\omega_0 t \qquad (4.2.4)$$

$$V_2(t) = V_{dc} \qquad (4.2.5)$$

$$i_r(t) = I_{r1} - \int (V_{dc} - V_{out}(t))dt \qquad (4.2.6)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_3 + C_4)}} \qquad (4.2.7)$$

$$Z_0 = \sqrt{\frac{L_r}{C_3 + C_4}} \qquad (4.2.8)$$

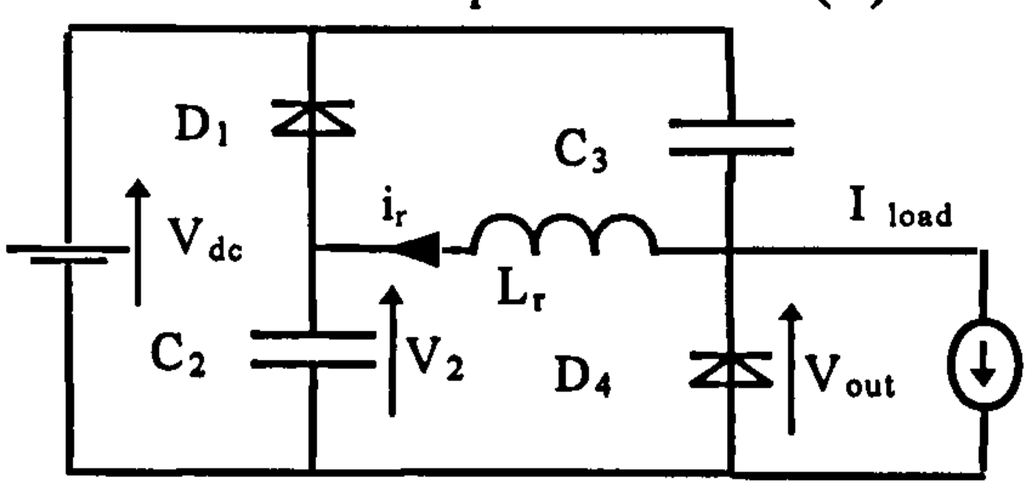
I_{r1} is the stored current in the inductor L_r from the previous pole commutation.

Figure 4.2.2: Operation mode A and B of the basic ARPI

Current ramp-down mode (C): Once the voltage V_{out} reaches zero diode D_4 picks up the load current and clamps the voltage V_{out} to zero. The current i_r decreases further.

Current ramp-down mode (D): The current i_r reaches the zero threshold and changes its polarity (Figure 4.2.8). IGBT S_1 provides the path for the negative current in the inductor L_r.

Current ramp-down mode (C)

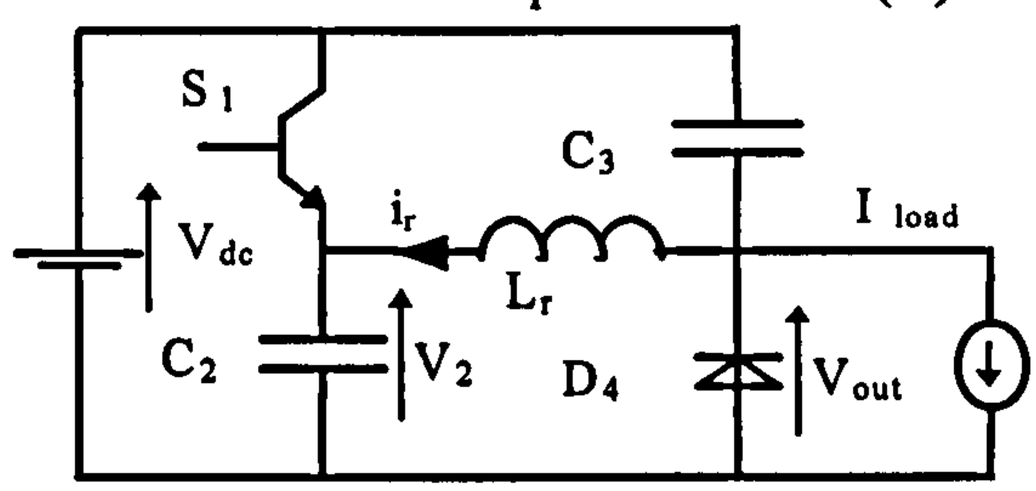


$$V_{out}(t) = 0V \qquad (4.2.9)$$

$$V_2(t) = V_{dc} \qquad (4.2.10)$$

$$i_r(t) = I_{r1} - \frac{V_{dc}}{L_r}t \qquad (4.2.11)$$

Current ramp-down mode (D)



$$V_{out}(t) = 0V \qquad (4.2.12)$$

$$V_2(t) = V_{dc} \qquad (4.2.13)$$

$$i_r(t) = I_{r1} - \frac{V_{dc}}{L_r}t \qquad (4.2.14)$$

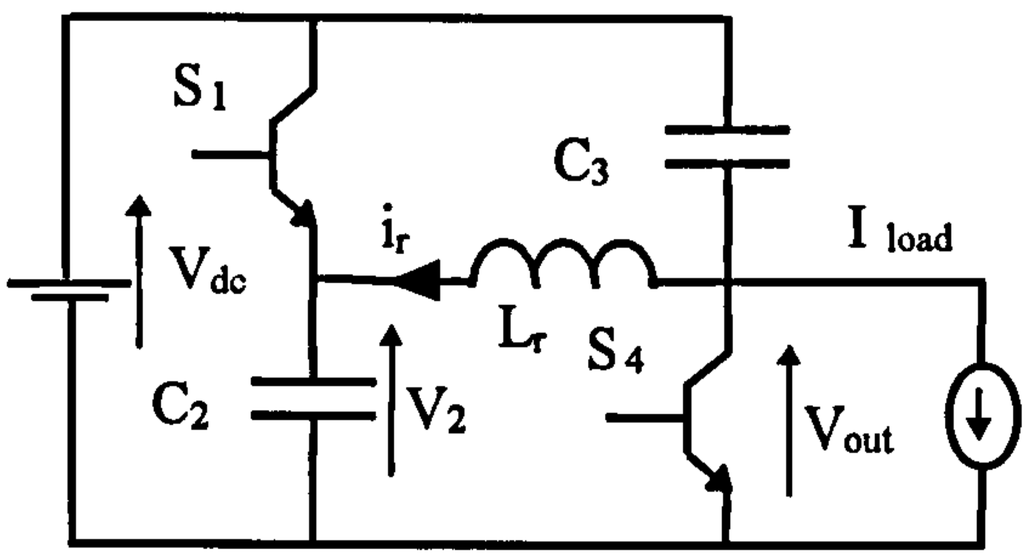
I_{r1} is the stored current in the inductor L_r from the previous pole commutation.

Figure 4.2.3: Operation modes C and D of the basic ARPI

Current ramp-down mode (E): Current i_r ramps towards the negative value of the load current. When the inductor current i_r reaches this threshold IGBT S_4 takes over to carry the additional current. Voltage V_2 stays constant during the whole ramp down mode.

Resonant mode (F): IGBT S_1 turns off initiating a resonant mode. The resonant frequency is determined by the values of the resonant inductor L_r and the capacitors C_1 and C_2. During resonant mode (F) voltage V_{out} remains zero.

Current ramp-down mode (E)

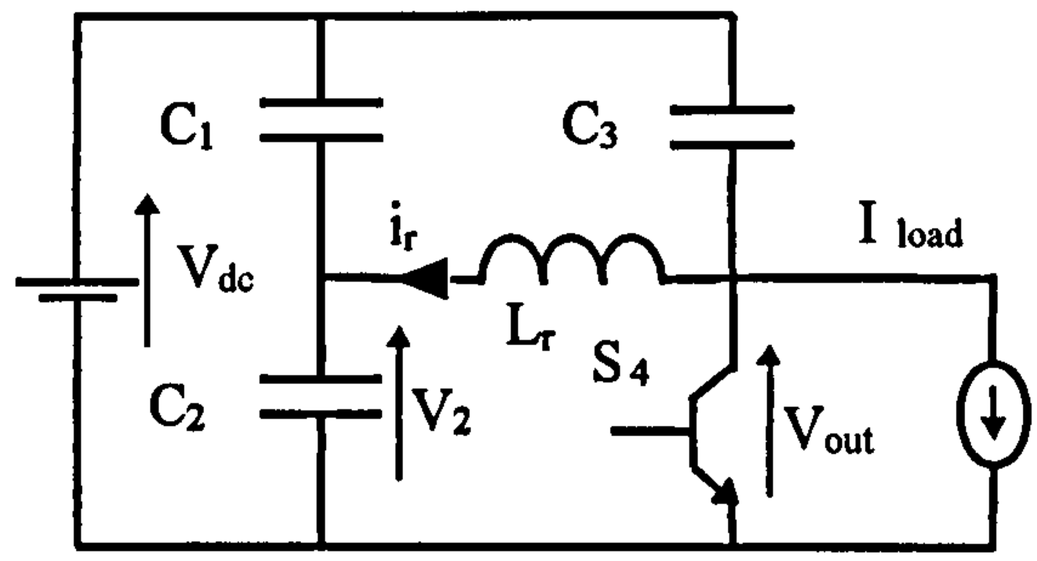


$$V_{out}(t) = 0V \quad (4.2.15)$$

$$V_2(t) = V_{dc} \quad (4.2.16)$$

$$i_r(t) = I_{r1} - \frac{V_{dc}}{L_r}t \quad (4.2.17)$$

Resonant mode (F)



$$V_{out}(t) = 0V \quad (4.2.18)$$

$$V_2(t) = V_{dc}\cos\omega_1 t - I_{r3}Z_1 \sin\omega_1 t \quad (4.2.19)$$

$$i_r(t) = I_{r3} - \int \frac{V_2(t)}{L_r}dt \quad (4.2.20)$$

$$\omega_1 = \frac{1}{\sqrt{L_r(C_1 + C_2)}} \quad (4.2.21)$$

$$Z_1 = \sqrt{\frac{L_r}{C_1 + C_2}} \quad (4.2.22)$$

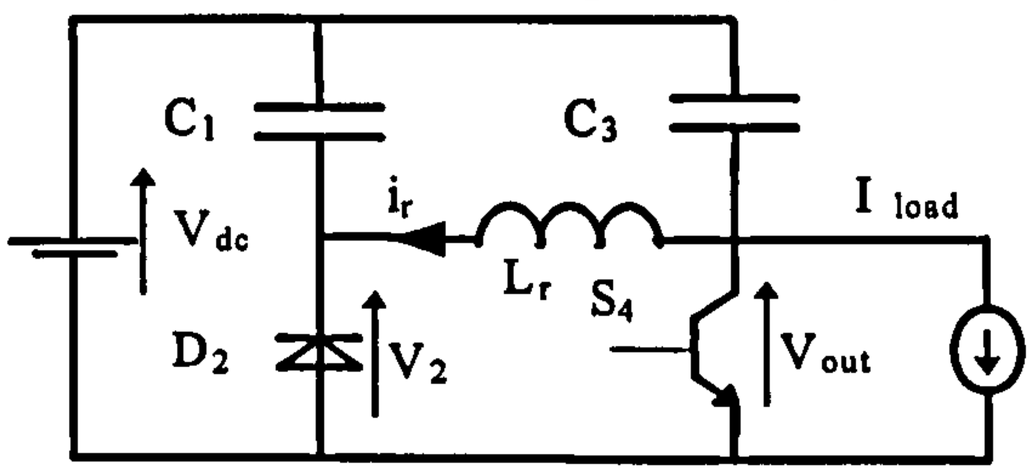
I_{r3} is the stored current in the inductor L_r when IGBT S_1 turns off.

Figure 4.2.4: Operation modes E and F of the basic ARPI

Freewheeling mode (G): With enough energy stored in inductor L_r the voltage across capacitor C_2 reaches zero and diode D_2 starts conducting. The conducting diode clamps the voltage to zero and the voltage difference across the resonant inductor L_r is zero. Zero voltage across the resonant inductor leads to freewheel the stored current I_{r2} in inductor L_r via diode D_2 and IGBT S_4.

Resonant mode (H): When the controller demands that the pole is returned to its original status, the IGBT S_4 is forced to turn-off. Resonance occurs between the elements L_r, C_1 and C_2. Voltage V_2 remains zero during resonant mode (H) and current i_r increases.

Freewheeling mode (G)

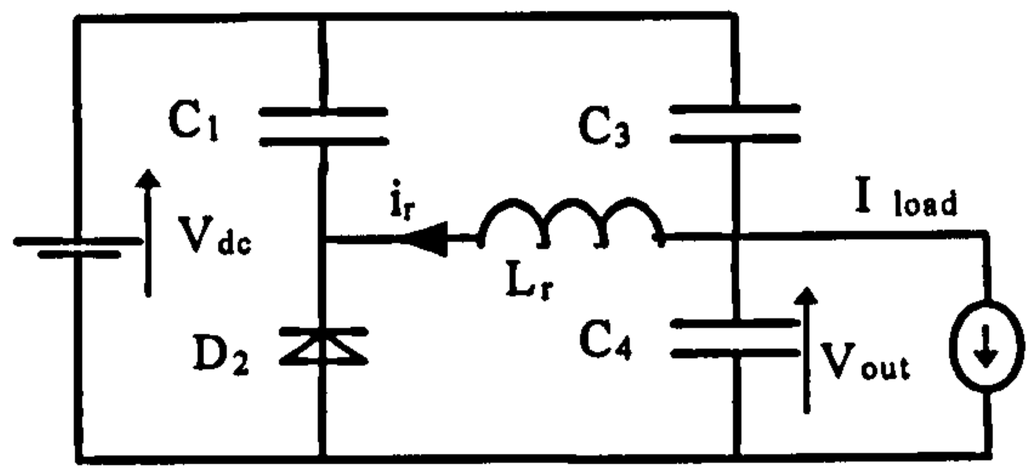


$$V_{out}(t) = 0V \quad (4.2.23)$$

$$V_2(t) = 0V \quad (4.2.24)$$

$$i_r(t) = I_{r2} \quad (4.2.25)$$

Resonant mode (H)



$$V_{out}(t) = V_{dc}(1 - \cos\omega_0 t) - I_{r2} Z_0 \sin\omega_0 t \quad (4.2.26)$$

$$V_2(t) = 0V \quad (4.2.27)$$

$$i_r(t) = I_{r2} + \int \frac{V_{out}(t)}{L_r} dt \quad (4.2.28)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_3 + C_4)}} \quad (4.2.29)$$

$$Z_0 = \sqrt{\frac{L_r}{C_3 + C_4}} \quad (4.2.30)$$

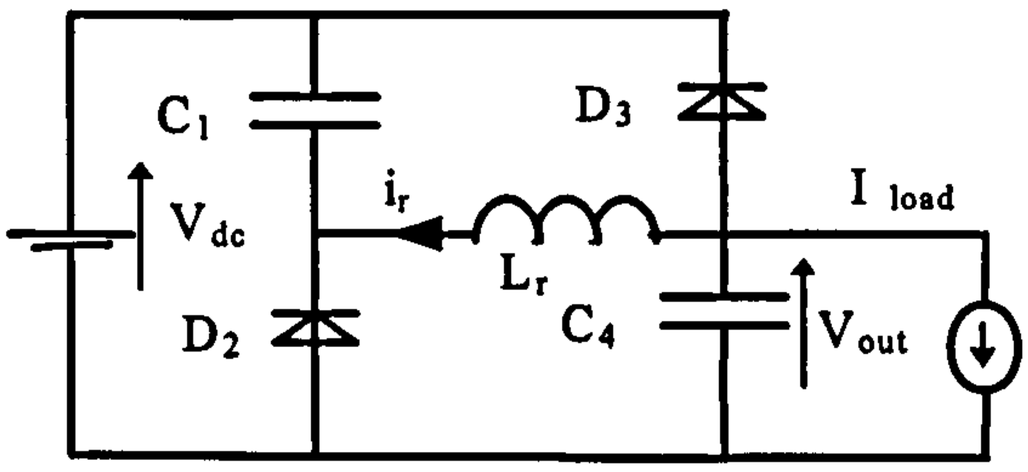
I_{r2} is the stored current in the inductor L_r once diode D_2 starts conducting.

Figure 4.2.5: Operation modes G and H of the basic ARPI

Current ramp-up mode (I): With zero voltage across the capacitor C_3 diode D_3 starts conducting. A positive voltage is applied across inductor L_r and the current i_r ramps further up.

Current ramp-up mode (J): During the time when diode D_3 is conducting IGBT S_3 is turned on under zero-voltage conditions. The current i_r reaches zero and changes its direction (Figure 4.2.8). Thus IGBT S_3 conducts.

Current ramp-up mode (I)

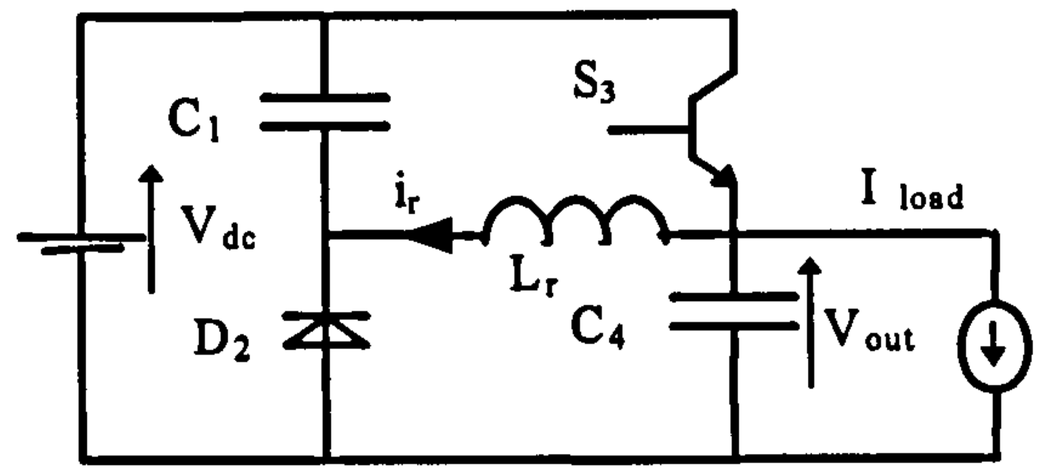


$$V_{out}(t) = V_{dc} \quad (4.2.31)$$

$$V_2(t) = 0V \quad (4.2.32)$$

$$i_r(t) = I_{r3} + \frac{V_{dc}}{L_r} t \quad (4.2.33)$$

Current ramp-up mode (J)



$$V_{out}(t) = V_{dc} \quad (4.2.34)$$

$$V_2(t) = 0V \quad (4.2.35)$$

$$i_r(t) = I_{r3} + \frac{V_{dc}}{L_r} t \quad (4.2.36)$$

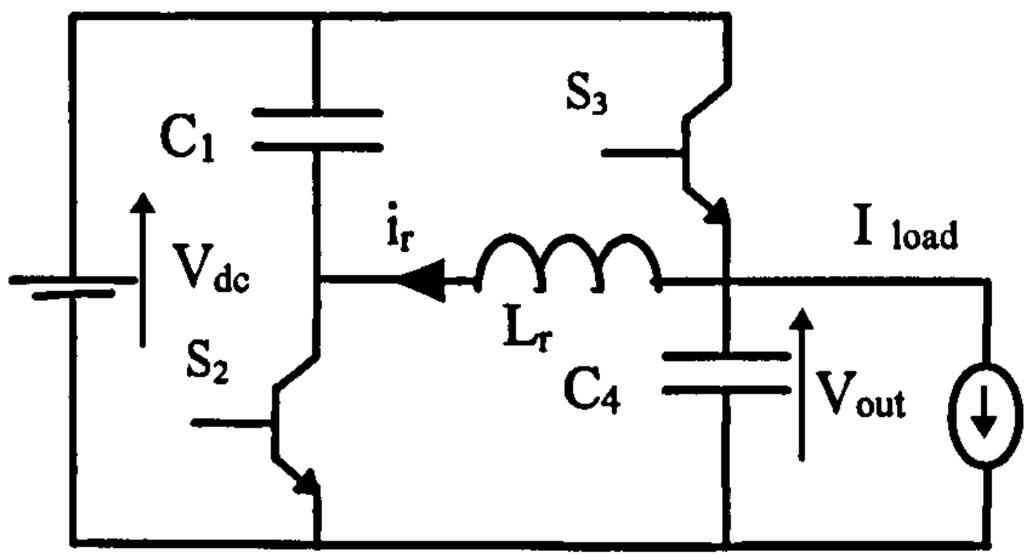
I_{r3} is the stored current in the inductor L_r once diode D_2 starts conducting.

Figure 4.2.6: Operation modes I and J of the basic ARPI

Current ramp-up mode (K): Current i_r changes its polarity and is boosted up to higher levels. IGBT S_2 picks up eventually the positive current flowing through inductor L_r. During the whole boost mode voltage V_2 is clamped to zero volts.

Resonant mode (L): With IGBT S_2 conducting the device is turned off. A resonant cycle takes place between the resonant inductor L_r and both capacitors C_1 and C_2. When the voltage across capacitor C_1 reaches zero volts diode D_1 starts to conduct. The freewheeling mode (A) takes over with a stored current of I_{r1} in the inductor L_r (assuming zero losses in the converter system).

Current boost mode (K)

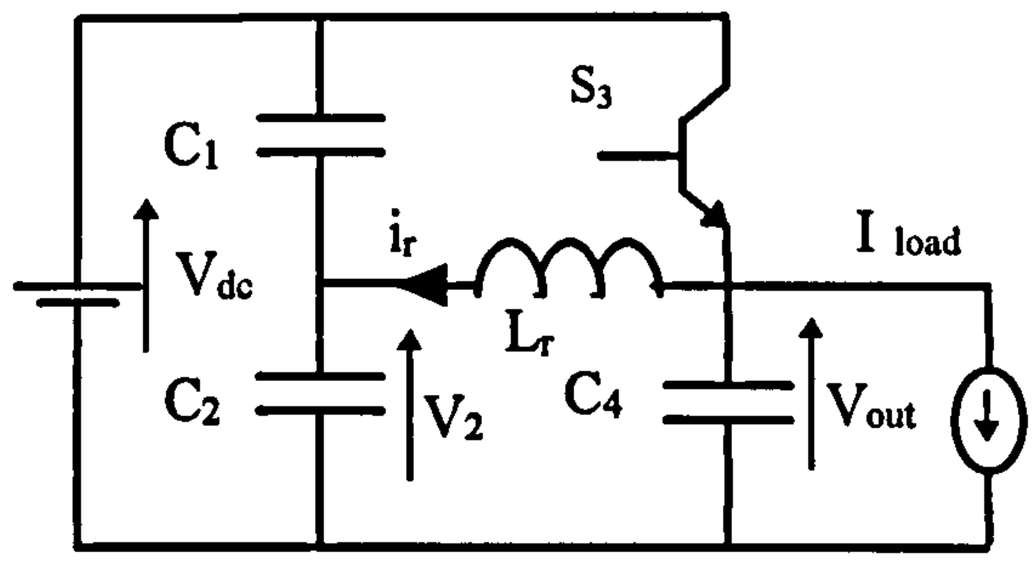


$$V_{out}(t) = V_{dc} \qquad (4.2.37)$$

$$V_2(t) = 0V \qquad (4.2.38)$$

$$i_r(t) = I_{r3} + \frac{V_{dc}}{L_r}t \qquad (4.2.39)$$

Resonant mode (L)



$$V_{out}(t) = V_{dc} \qquad (4.2.40)$$

$$V_2(t) = V_{dc}(1-\cos\omega_1 t) - I_{r3}Z_1 \sin\omega_1 t \qquad (4.2.41)$$

$$i_r(t) = I_{r3} + \int \frac{V_{dc} - V_2(t)}{L_r}dt \qquad (4.2.42)$$

$$\omega_1 = \frac{1}{\sqrt{L_r(C_1 + C_2)}} \qquad (4.2.43)$$

$$Z_1 = \sqrt{\frac{L_r}{C_1 + C_2}} \qquad (4.2.44)$$

I_{r3} is the stored current in the inductor L_r once diode D_2 starts conducting.

Figure 4.2.7: Operation modes K and L of the basic ARPI

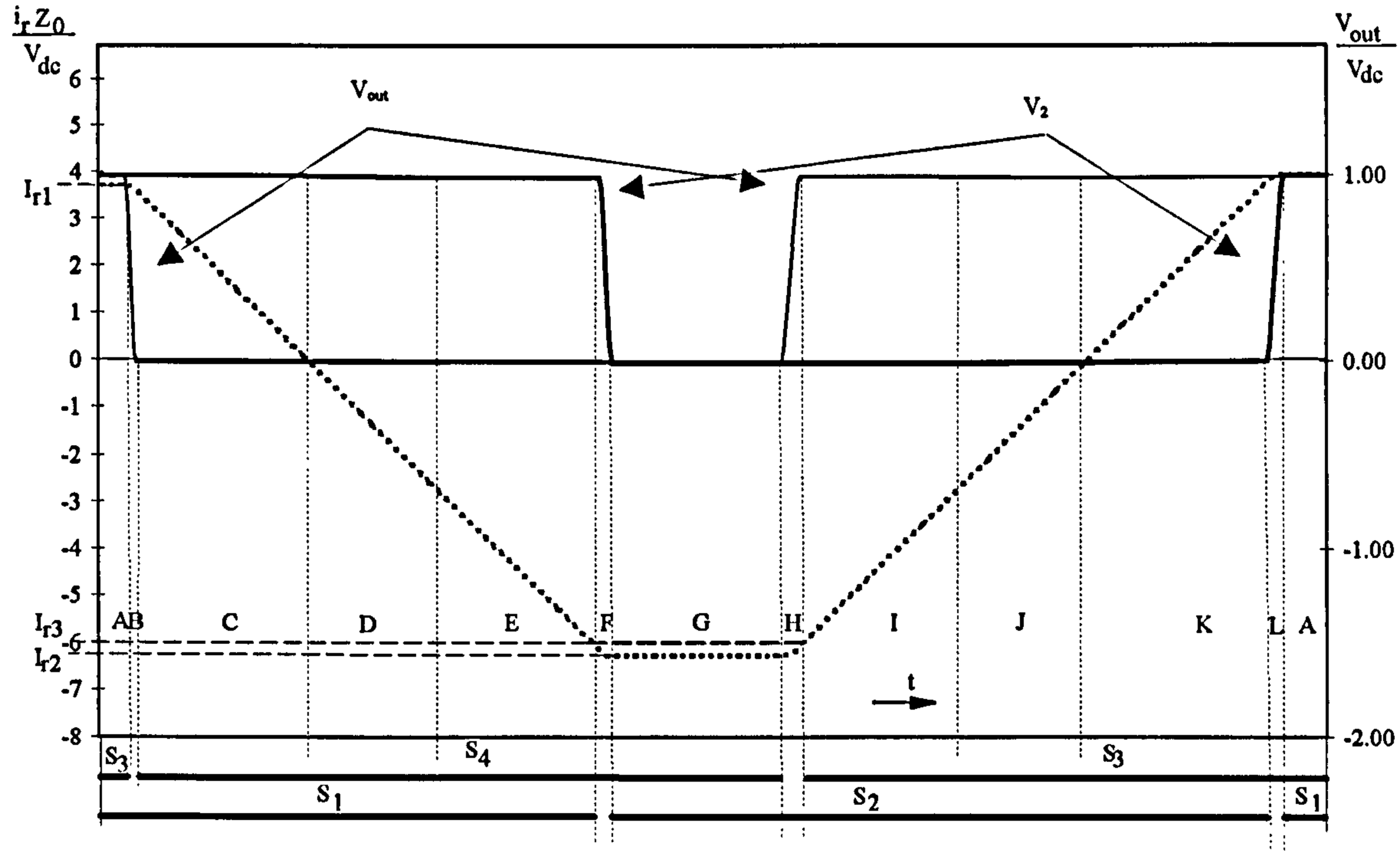
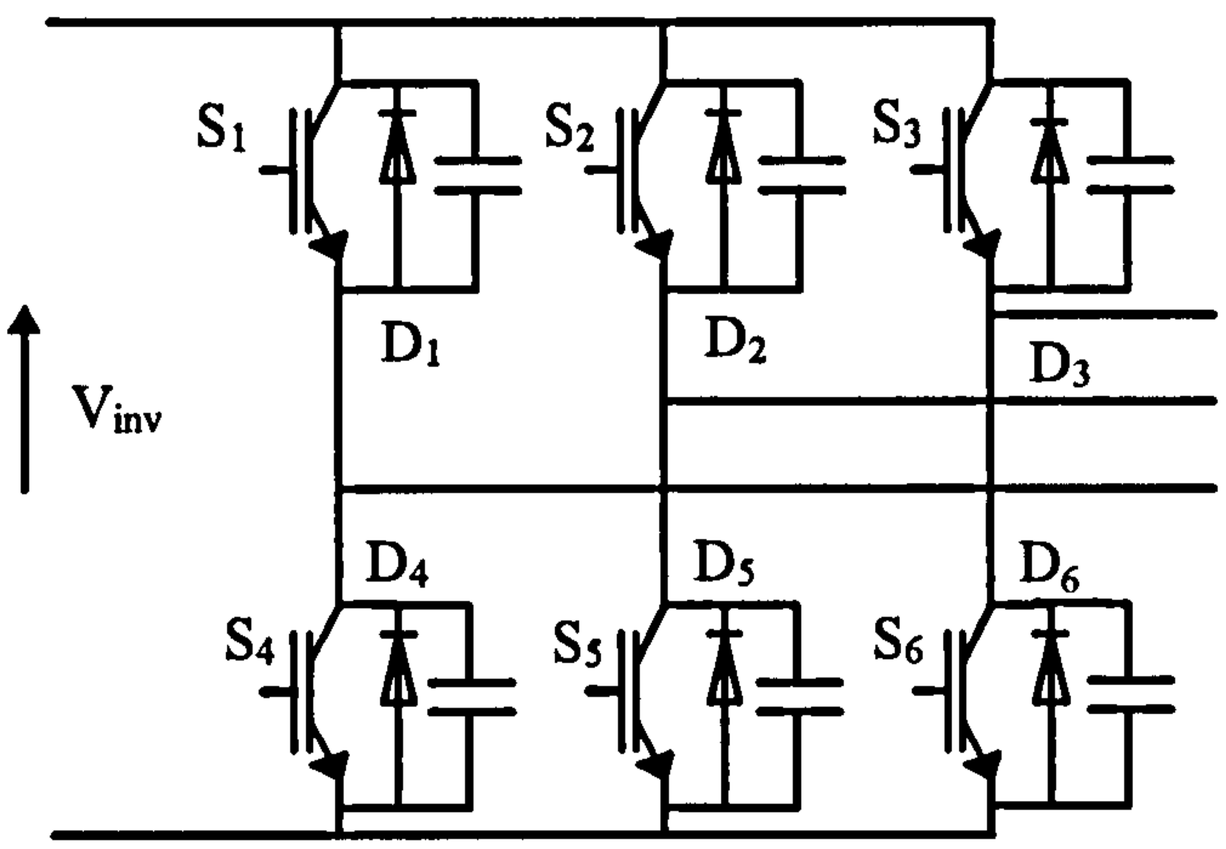
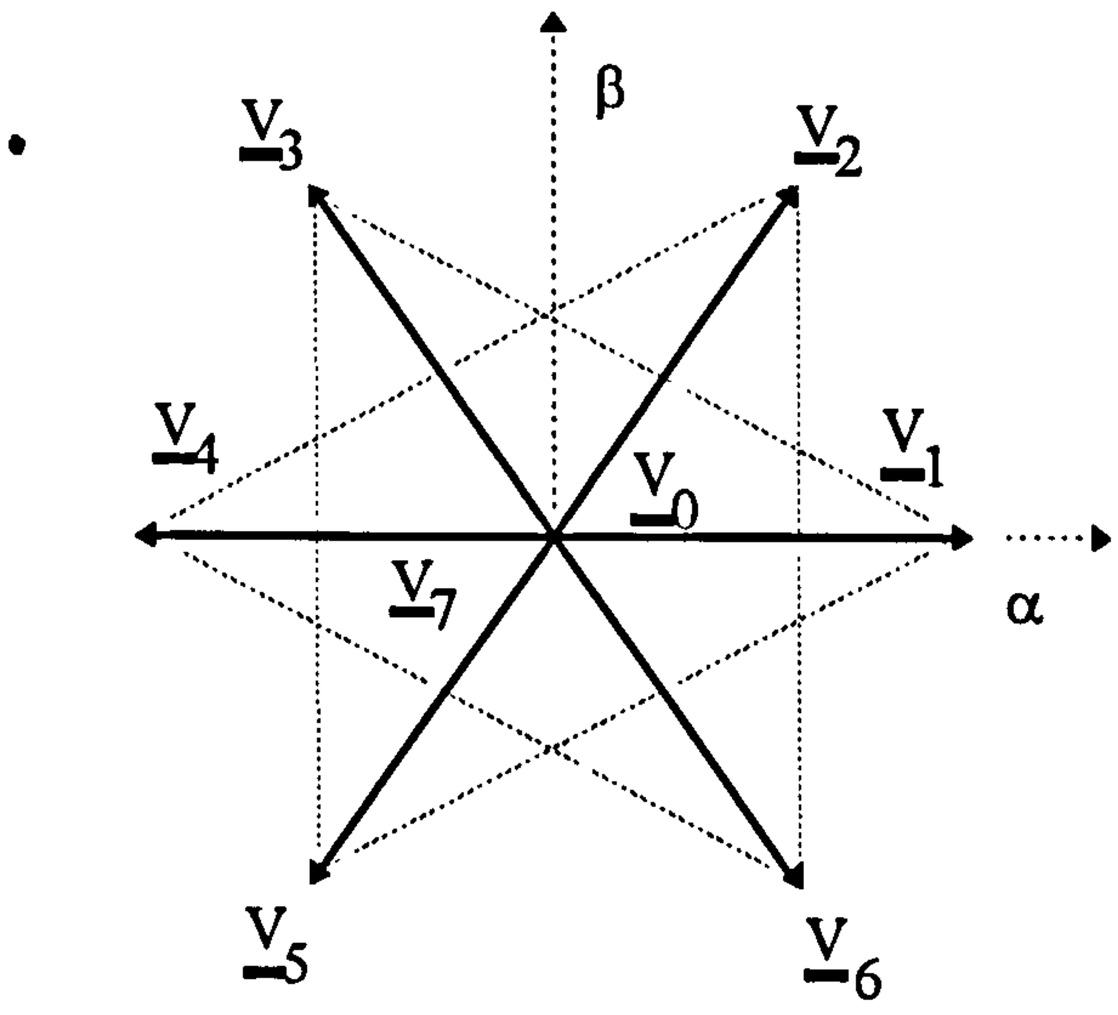


Figure 4.2.8: Normalised waveform of V_{out} (solid line), V_2 (solid line) and i_r (dashed line) over one pole commutation cycle of the basic ARPI

The analysed basic ARPI is controlled in such a way that a freewheeling current flows through the resonant inductor. Reference [4.10] describes a different control scheme of the basic ARPI without any freewheeling currents. The idea is to store energy in the inductor only when the switching status of the pole changes. Thus freewheeling losses are reduced. The operation mode is described as follows: Assume a positive load current is flowing through diode D_4 and all IGBTs S_1, S_2, S_3 and S_4 are off. The full dc-link voltage applies across capacitor C_2. The capacitor can not discharge because IGBT S_2 remains open. Now, the controller demands a change in pole status and turn-on both IGBTs S_1 and S_4 at the same time (S_1 is switched on under zero-voltage conditions because the dc-link voltage is applied across capacitor C_2 only). The inductor current ramps up and above the load current level the current in diode D_4 commutates to IGBT S_4 naturally. With both IGBTs conducting (S_1 and S_4) both are turned off at the same time and voltage resonance is initiated across the left side of the pole and the right side of the pole. Resonating elements are inductor L_r and all capacitors C_1, C_2, C_3 and C_4. At half of the resonant time diode D_2 and diode D_3 get forward biased and start conducting. At this time only IGBT S_3 is turned on and IGBT S_2 stays open. Thus the inductor current decreases linearly to zero and the voltage across capacitor C_2 is zero as well. To change the pole status to its initial state IGBT S_3 is switched and capacitor C_3 works as a snubber capacitor as discussed in section 3.3.2. In the same manner light load conditions are not controllable with this scheme.

Figure 4.1 shows two topologies called Delta-Configured Auxiliary Resonant Snubber Inverter (D-CRSI) [4.18] and Star-Configured Auxiliary Resonant Snubber Inverter (S-CRSI) [4.19]. Both topologies connect their auxiliary resonant branches between two output phases. Each auxiliary branch consists of a resonant inductor and a reverse blocking auxiliary switch. The D-CRSI uses antiparallel diodes to allow resonant current to flow in reverse direction, whereas the S-CRSI must block the negative voltage with a series diode. Both topologies are based on the principal to store energy in the auxiliary inductor and to use this to change the switching status of the two poles simultaneously. Although both topologies may operate with space vector control, the control can be very complicated because it requires sensing both load and resonant currents in the logic design [4.18]. Thus non-adjacent state space vector is applied. That means that during one inverter switching period one pole is unchanged and the other two poles changes their status. This control scheme is similar to the already discussed modified PWM control schemes applied on PRDCL topologies (mPWM, section 3.3.2). Figure 4.2.9 shows the switching diagram of a non-adjacent state space vector modulation.





forcing vectors		zero vectors	
$\underline{V}_1$	(100)	$\underline{V}_0$	(000)
$\underline{V}_2$	(110)	$\underline{V}_7$	(111)
$\underline{V}_3$	(010)		
$\underline{V}_4$	(011)		
$\underline{V}_5$	(001)		
$\underline{V}_6$	(101)		

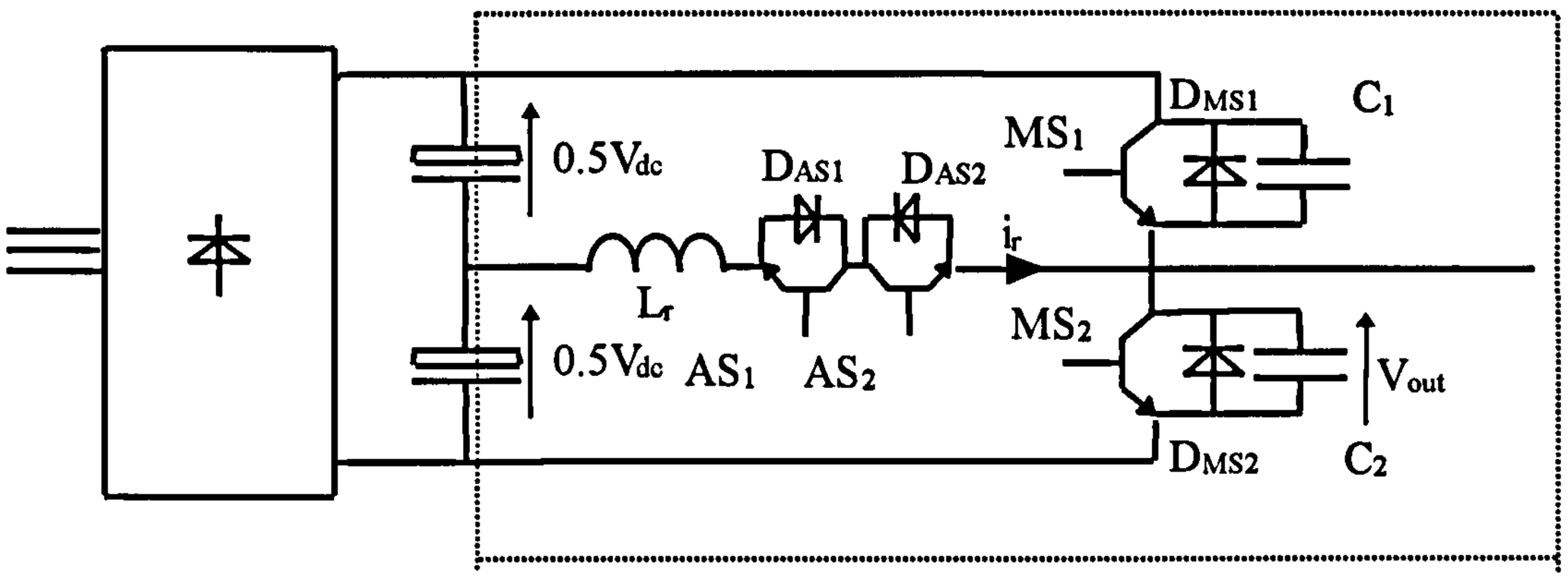
e.g. (010)=(S_1,off;S_2,on;S_3,off)

Figure 4.2.9: Non-adjacent space vector control

From an initial state of (100), i.e., switch S1 is on, and switches S2 and S3 are off, the allowable next states are (010), (001) or (011). This control scheme makes it difficult to apply the zero vectors (000) and (111).

4.2.2 Auxiliary Commutated Resonant Pole Inverter (ACPI)

Compared to the basic ARPI the ACPI makes use of the midpoint of the dc-link capacitors to store current in the inductor when commutation of the pole is needed. [4.12-4.14]. Most of the time the auxiliary switches are off. When a change in the pole status is demanded from the controller, one of the auxiliary switches is turned on under zero-current conditions allowing current to be stored in the resonant inductor. The amount of stored current depends on the commutation process of the pole. Less current is stored when the commutation process from the conducting IGBT to the opposite diode is needed and more current must be stored when the opposite commutation (Diode-IGBT) is commanded. The latter commutation is discussed first.



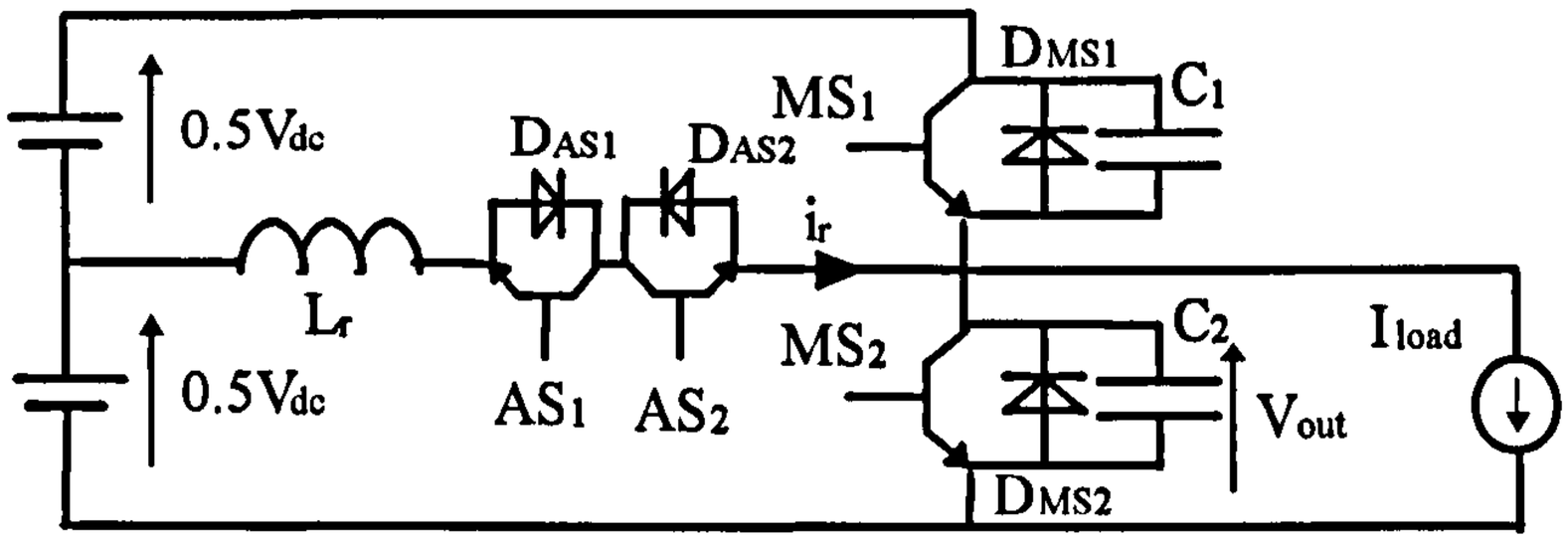


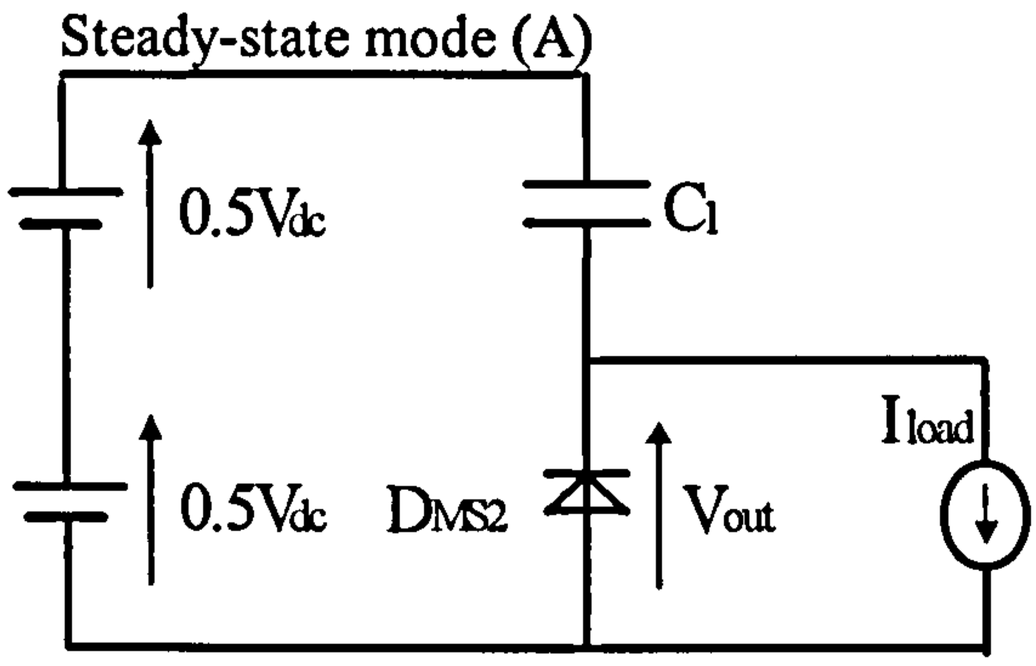
Figure 4.2.10: Schematic and equivalent circuit of one pole of the ACPI

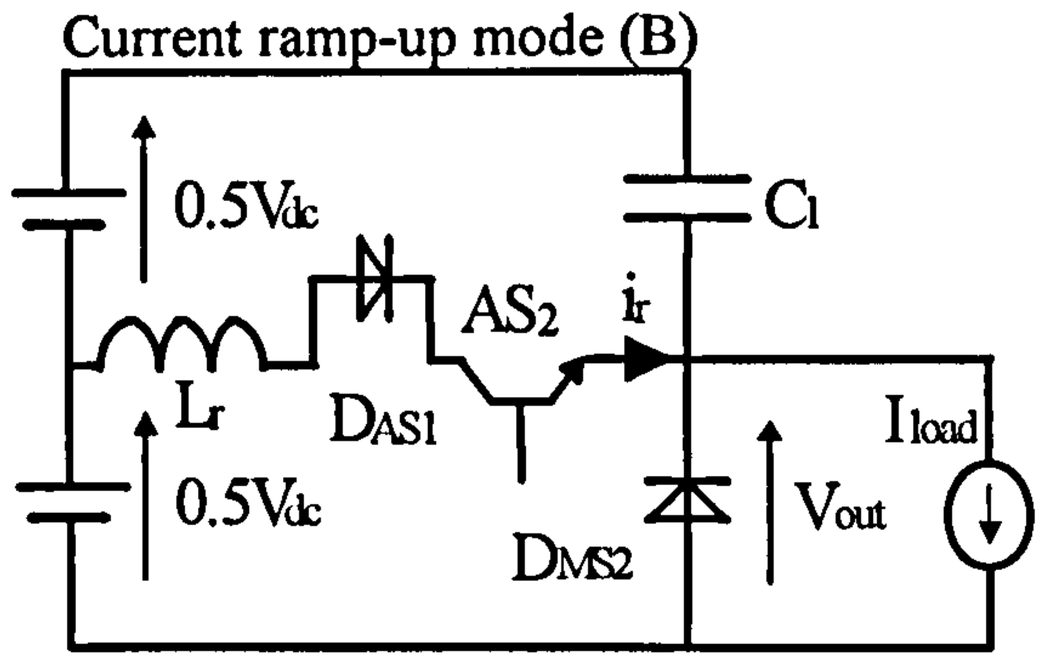
The operation modes are analysed with the help of Figures 4.2.11 to 4.2.19.

Commutation Diode-IGBT:

Steady-state mode (A): I_{load} is positive and the load current is flowing through diode D_{MS2} resulting in a clamped zero output phase voltage V_{out}. Both auxiliary devices are open and the antiparallel diode D_{AS2} prevents current flow through inductor L_r.

Current ramp-up mode (B): The controller commands to change the switching status of the pole. To do so the IGBT AS2 turns on first. The half of the dc-link voltage is applied across the inductor L_r and inductor current i_r ramps up. The current i_r reaches the load current level and diode D_{MS2} commutates to IGBT MS2 naturally.





$$V_{out}(t) = 0V \qquad (4.2.45)$$

$$i_r(t) = 0A \qquad (4.2.46)$$

$$V_{out}(t) = 0V \qquad (4.2.47)$$

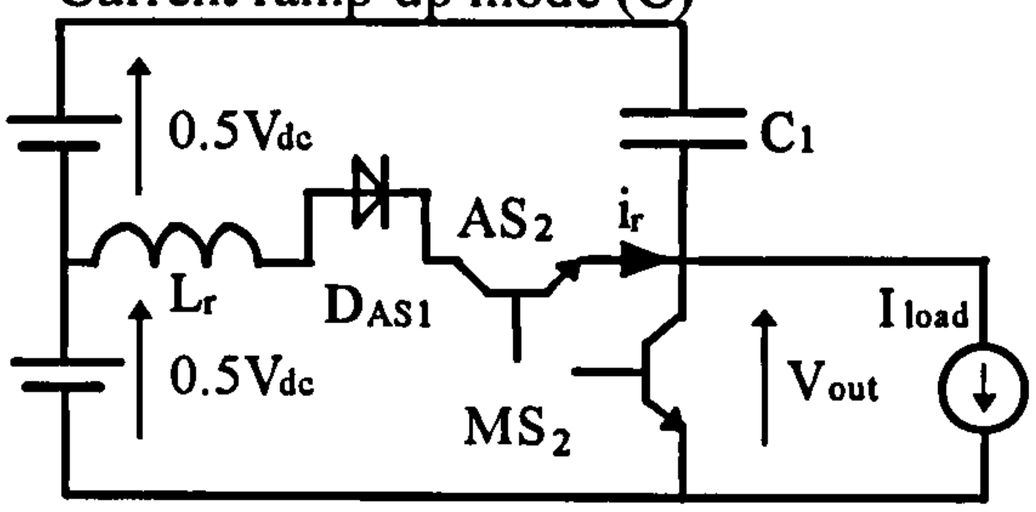
$$i_r(t) = \frac{1}{L_r}\int 0.5V_{dc}\,dt \qquad (4.2.48)$$

Figure 4.2.11: Operation modes A and B of the ACPI

Current ramp-up mode (C): The IGBT MS2 conducts and the half of the dc-link voltage applies still across inductor L_r resulting in a further increase of inductor current i_r.

Resonant mode (D): IGBT MS2 turns off and resonance takes place between L_r, C_1 and C_2.

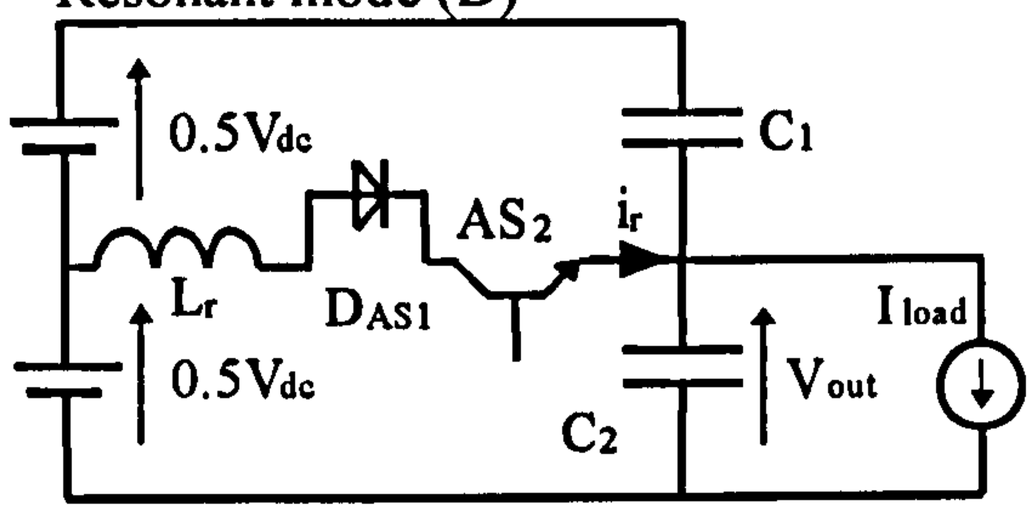
Current ramp-up mode (C)



$$V_{out}(t) = 0V \qquad (4.2.49)$$

$$i_r(t) = I_{load} + \frac{1}{L_r}\int 0.5V_{dc}\,dt \qquad (4.2.50)$$

Resonant mode (D)



$$V_{out}(t) = 0.5V_{dc}(1-\cos\omega_0 t) + \\ +I_{r1}Z_0\sin\omega_0 t \qquad (4.2.51)$$

$$i_r(t) = I_{r1} + \frac{1}{L_r}\int (0.5V_{dc} - V_{out}(t))dt \qquad (4.2.52)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_1 + C_2)}} \qquad (4.2.53)$$

$$Z_0 = \sqrt{\frac{L_r}{C_1 + C_2}} \qquad (4.2.54)$$

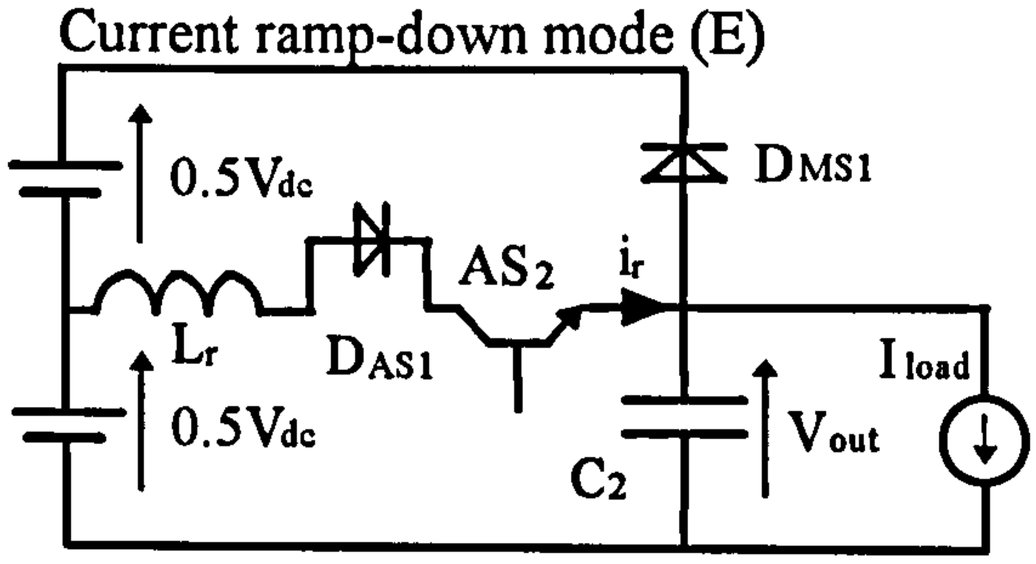
I_{r1} is the stored current in inductor L_r when IGBT MS2 turns off.

Figure 4.2.12: Operation modes C and D of the ACPI

Current ramp-down mode (E): With zero volt across diode D_{MS1} the diode gets forward biased and starts conducting. The resonant current i_r ramps down naturally, because the output phase voltage V_{out} is now equal the dc-link voltage and therefore a negative half dc-link voltage applies across the inductor L_r.

Current ramp-down mode (F): IGBT MS1 is switched on under zero voltage. The inductor current ramps down linearly to zero.

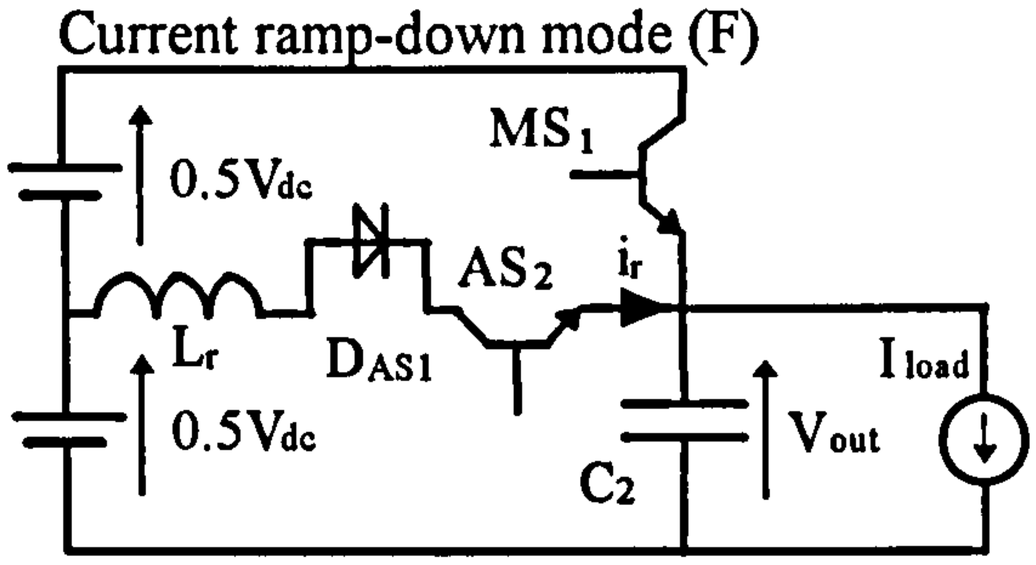
Current ramp-down mode (E)



$$V_{out}(t) = V_{dc} \qquad (4.2.55)$$

$$i_r(t) = I_{r1} - \frac{1}{L_r}\int 0.5V_{dc}\,dt \qquad (4.2.56)$$

Current ramp-down mode (F)



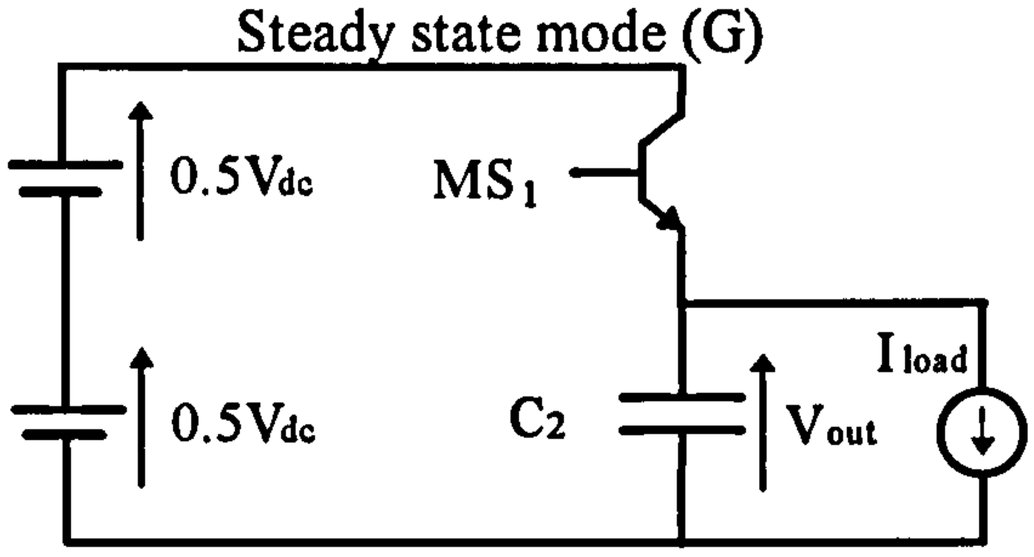
$$V_{out}(t) = V_{dc} \qquad (4.2.57)$$

$$i_r(t) = I_{load} - \frac{1}{L_r}\int 0.5V_{dc}\,dt \qquad (4.2.58)$$

I_{r1} is the stored current in inductor L_r when IGBT MS2 turns off.

Figure 4.2.13: Operation modes E and F of the ACPI

Steady state mode (G): Once i_r reaches zero auxiliary IGBT AS2 switches off under zero current switching conditions. Diode D_{AS1} stops conducting and prevents the inductor current i_r from a natural backswing.



$$V_{out}(t) = V_{dc} \quad (4.2.59)$$

$$i_r(t) = 0A \quad (4.2.60)$$

Figure 4.2.14: Operation mode G of the ACPI

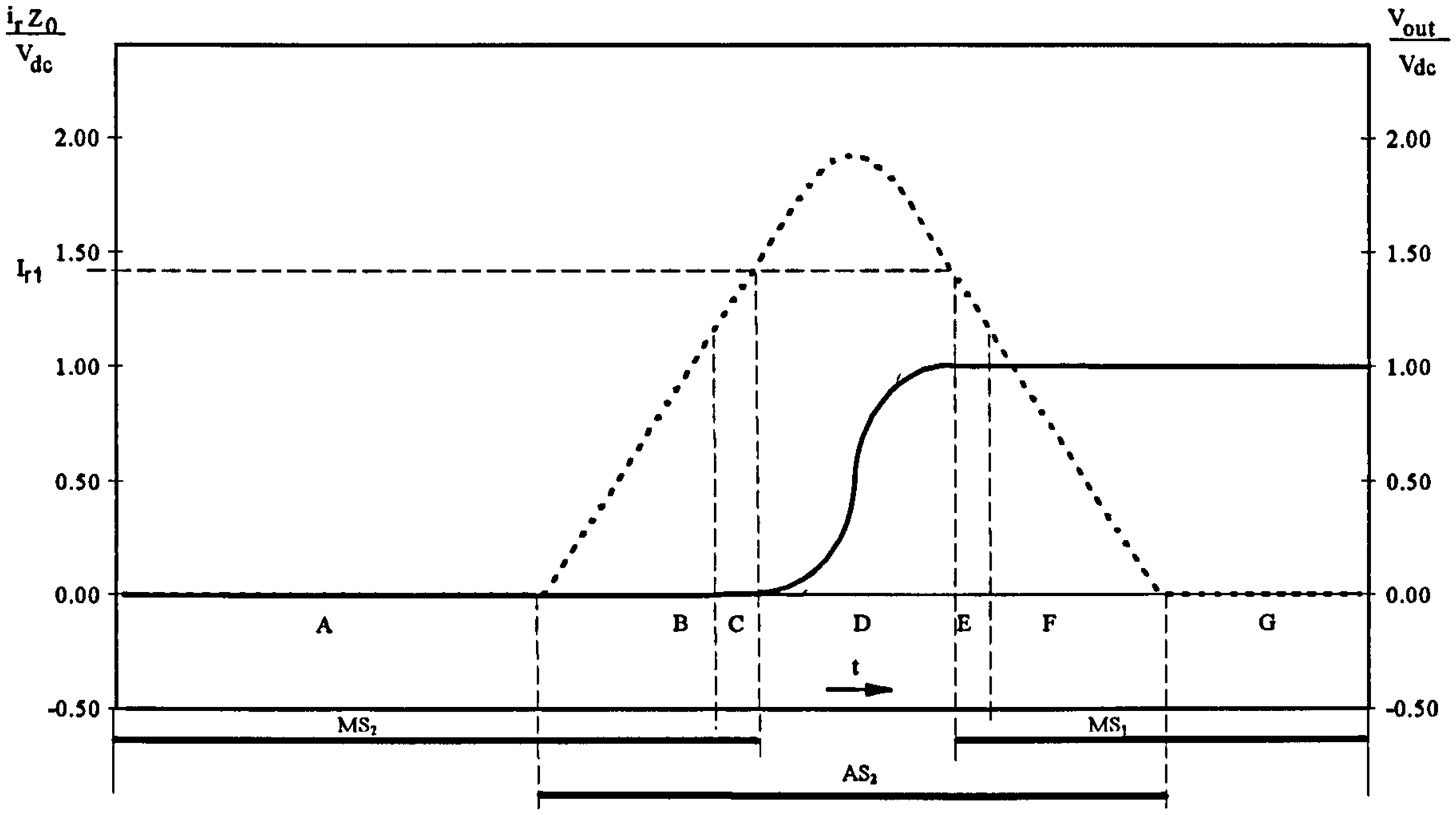


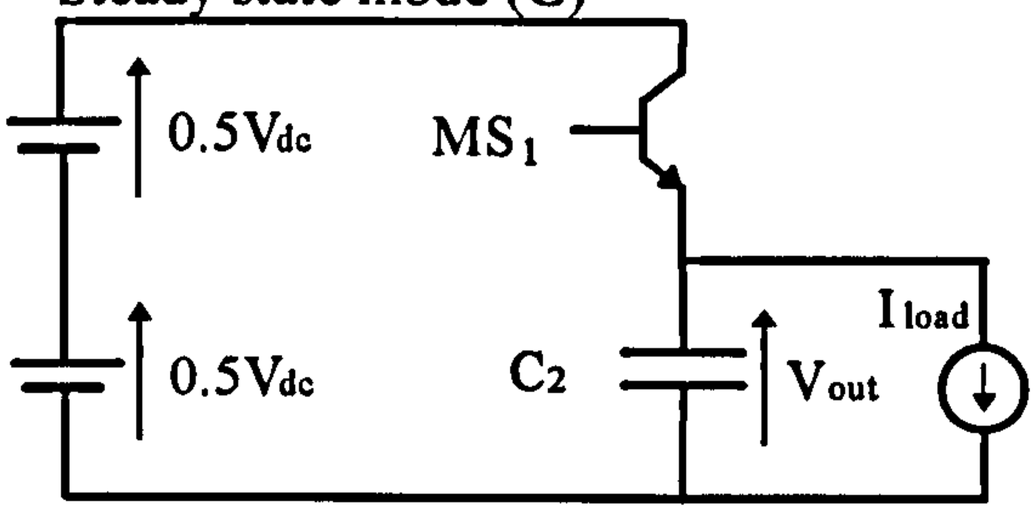
Figure 4.2.15: Normalised waveform of V_{out} (solid line) and i_r (dashed line) over the pole commutation process Diode-IGBT

Commutation IGBT-Diode

Steady state mode (G): IGBT MS1 conducts the load current and both auxiliary devices are off. Diode D_{AS1} withstands the voltage of $0.5V_{dc}$. Thus no current flows in inductor L_r. The output phase voltage is equal the dc-link voltage.

Ramp-up mode (H): The controller demands to change the switching status of the pole. Therefore IGBT AS1 is commanded to turn-on first. Thus the half of the dc-link voltage applies across the resonant inductor and the current i_r increases linearly.

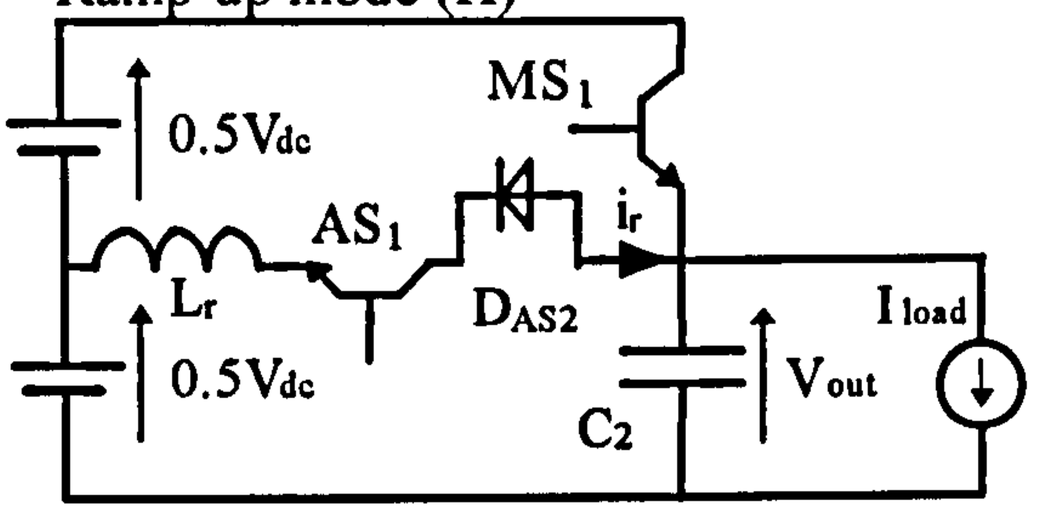
Steady state mode (G)



$$V_{out}(t) = V_{dc} \qquad (4.2.61)$$

$$i_r(t) = 0A \qquad (4.2.62)$$

Ramp-up mode (H)



$$V_{out}(t) = V_{dc} \qquad (4.2.63)$$

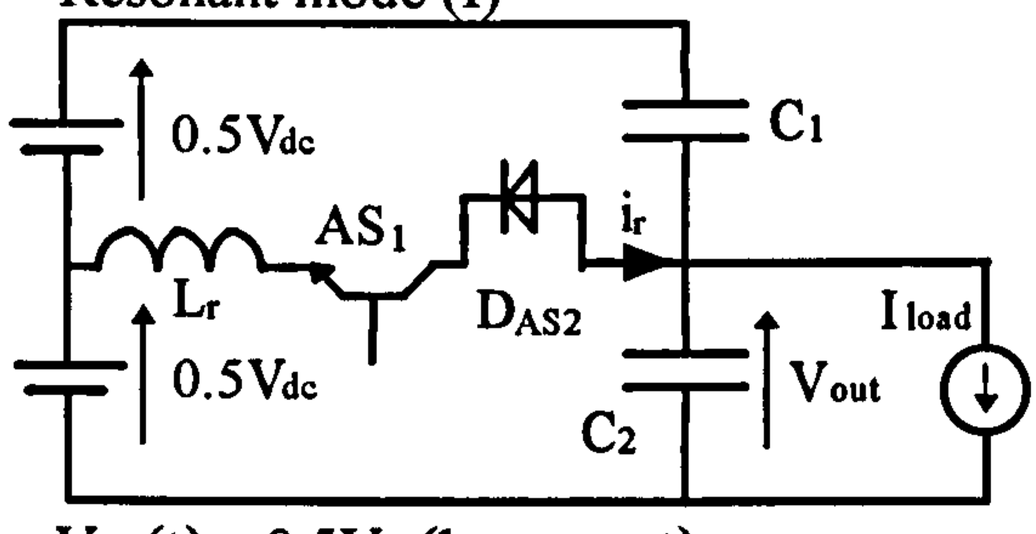
$$i_r(t) = \frac{1}{L_r}\int (0.5V_{dc} - V_{dc})dt \qquad (4.2.64)$$

Figure 4.2.16: Operation modes G and H of the ACPI

Resonant mode (I): Once current i_r reaches a defined current threshold (I_{r2}) that is smaller than the load current IGBT MS1 turns off resulting in a resonance oscillation between L_r, C_1 and C_2.

Ramp-down mode (J): The voltage V_{out} resonates to zero and diode D_{MS2} starts conducting clamping the output phase voltage V_{out} to zero volts. With diode D_{MS2} conducting IGBT MS2 can turned on under lossless manner. The current i_r decreases linearly to zero because the voltage across the inductor L_r changed its polarity during the resonant mode.

Resonant mode (I)



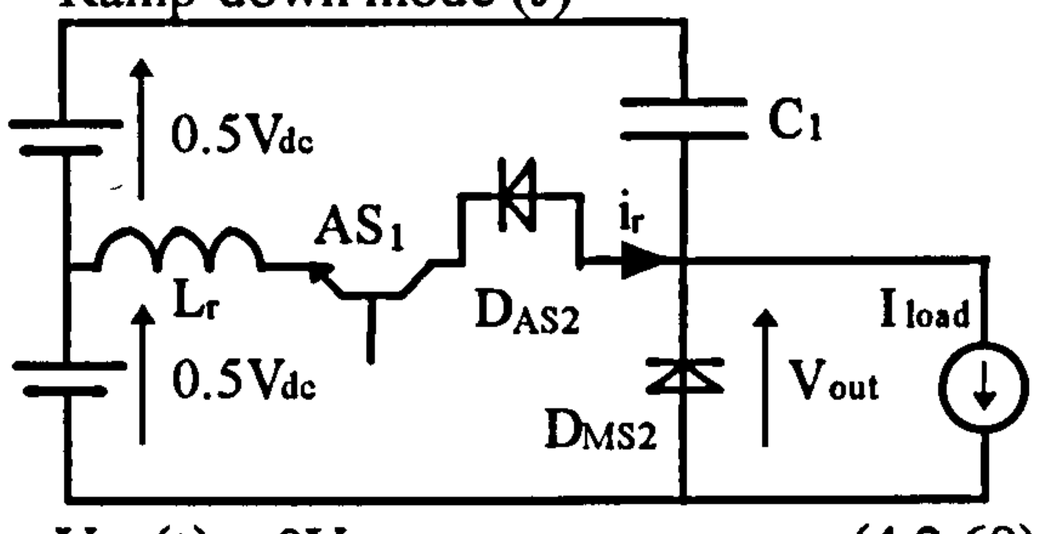
$$V_{out}(t) = 0.5V_{dc}(1+\cos\omega_0 t) - \\ - I_{r2}Z_0 \sin\omega_r t \qquad (4.2.65)$$

$$i_r(t) = I_{r2} - \frac{1}{L_r}\int (0.5V_{dc} - V_{out}(t))dt \qquad (4.2.66)$$

$$\omega_0 = \frac{1}{\sqrt{L_r(C_1 + C_2)}} \qquad (4.2.67)$$

$$Z_0 = \sqrt{\frac{L_r}{C_1 + C_2}} \qquad (4.2.68)$$

Ramp-down mode (J)



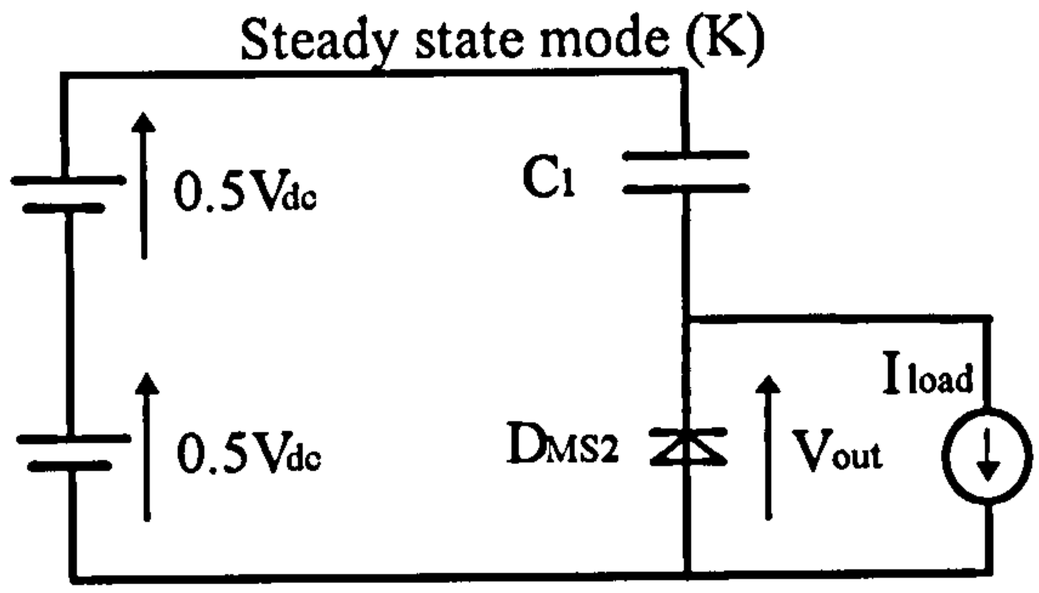
$$V_{out}(t) = 0V \qquad (4.2.69)$$

$$i_r(t) = I_{r2} - \frac{1}{L_r}\int (0.5V_{dc} - V_{dc})dt \qquad (4.2.70)$$

I_{r2} is a defined current level threshold.

Figure 4.2.17: Operation mode I and J of the ACPI

Steady state mode (K): IGBT AS1 is switched off under zero current conditions and diode D_{MS2} is carrying the full load current I_{load}.



$$V_{out}(t) = 0V \quad (4.2.71)$$

$$i_r(t) = 0A \quad (4.2.72)$$

Figure 4.2.18: Operation mode K of the ACPI

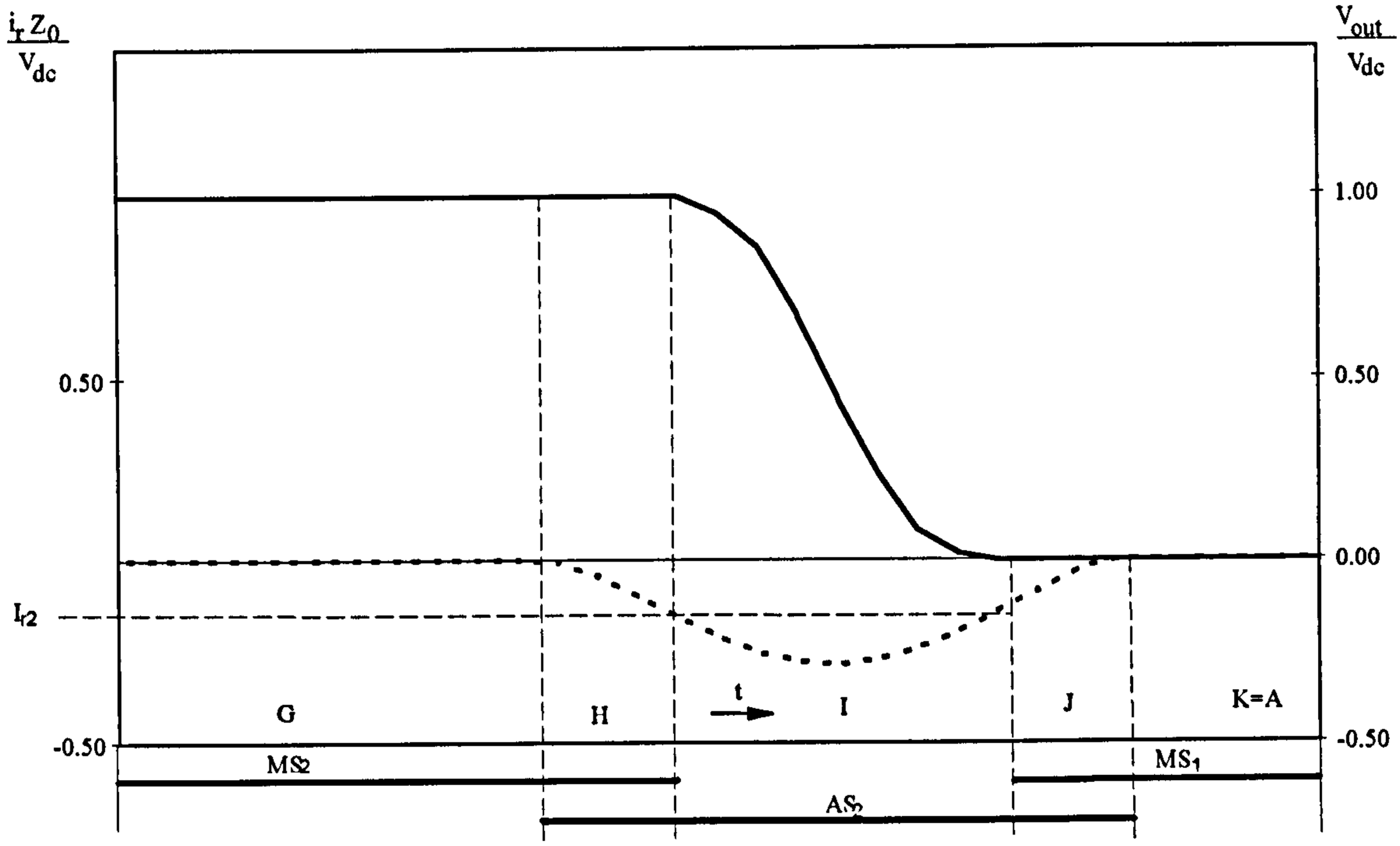


Figure 4.2.19: Normalised waveform of V_{out} (solid line) and i_r (dashed line) over one pole commutation process IGBT-Diode

Figure 4.1 shows that the number of auxiliary switching devices can be reduced to one, when using an IGBT in a diode bridge configuration. The advantage lays in cost reduction, but a sensor circuit must be integrated in the auxiliary path, providing zero current detection. This detector is needed to turn-off the device once the inductor current i_r reaches zero. That is because with the diode bridge configuration none of the diodes get reversed biased to stop the current i_r from further oscillation.

Chapter 5

ASSESSMENT OF CONVERTER TOPOLOGIES

Chapters 3 and 4 identified the major classes of softswitching converters. Selected topologies from each class were analysed in detail and key differences in component stresses, output performances and control complexity were investigated. Chapter 5 provides a comparative assessment of softswitching topologies for motor drives applications. Sections 5.1 and 5.2 describe advantages and disadvantages of the many sub-topologies published in the last twelve years. For a better understanding Appendix D shows the schematics of all topologies discussed in this chapter. Section 5.3 describes fundamental limitations of softswitching related to the physical behaviour of power diodes and IGBTs. Section 5.4 translates the outcome of section 5.3 into topology specific constraints on PWM modulation schemes and the resulting harmonic output spectrum. Section 5.5 considers each major class of topology in turn, identifying features such as devices stresses, additional losses, output waveforms fidelity, control complexity, number of additional components and cost. In addition, conclusions are drawn concerning the most appropriate softswitching topologies.

5.1 Comparison of Resonant DC-Link Inverters

The following comparison is based on the author's theoretical work, simulation results and statements published in various papers. In this section the switching status ZVS is used when zero voltage is applied across the switching device. This includes also the case when an antiparallel diode is connected with the switching device and the diode conducts the current. ZCS is used when zero current flows through the switching device.

5.1.1 Comparison of basic RDCL and clamp basic RDCL Topologies

The unclamped basic RDCL [5.1 and 5.2] (Figure 3.1.1) finds little application in practical circuits because of uncontrolled inverter leg voltage and the very high levels of resonant inductor current. Overshoot voltages higher than three times the dc-link voltage are reported in reference [5.2]. This overshoot happens at times when the inverter input current changes from maximum positive to maximum negative value. Another drawback is the use of a sophisticated controller to assure proper energy in the resonant components.

To alleviate the high voltage stress problems of basic RDCL converter topologies, the active and passive clamp basic RDCL were introduced [5.3-5.7] (Figure 3.2.1 and Figure 3.2.6). The voltage stress across the inverter switches depends on the clamp factor. Normally a clamp factor of 1.2 to 1.4 is applied to achieve a compromise between overvoltage stress and the time period of the resonant link cycle (equation 3.2.15).

Reference [5.8] summarises problems occurring when operating the active clamp basic RDCL topology. Firstly a per-cycle charge balance of the clamp capacitor is required to sustain link oscillation. That is, losses in the resonant components and the clamp switch must be anticipated and are compensated by storing sufficient initial current in the resonant inductor before the resonant cycle. The compensation technique tends to pump excessive charge into the clamp capacitor in order to ensure that the link voltage will return to zero. Unfortunately the excessive charge accumulation in the clamp capacitor causes the clamp voltage to increase. Thus a regulation loop is required to co-ordinate the conflict between sustaining link resonance and limiting the clamp voltage increase. The regulation requires a complicated control algorithm for the clamp switch, which relies on precise current sensing or current observer. The link resonance becomes difficult to maintain over all operating conditions. Secondly, the per-cycle clamp time is not constant and depends on the actual load current. Thus output harmonics vary.

In contrast to the active clamp circuit, the passive clamp basic RDCL does not require an additional switch to activate and deactivate the clamp mode. Main difficulty lies in realisation of the clamp transformer, particularly where a low clamp factor is required. Under these conditions the transformer clamp winding and clamp diode will experience a voltage stress of larger than the dc-link voltage. Thus, the clamp diode will typically consist of a number of series connected devices adding further to the complexity and cost of the circuit. In addition, the transformer leakage reactance will further increase voltage stress and may lead to increased EMI problems. A distributed co-axial winding in an integrated magnetic assembly that combines the resonant inductor and the clamp transformer could alleviate this problem [5.7].

Besides the discussed problems with basic, active clamp and passive clamp basic RDCLs, the topologies lack a true freewheeling state and the link is, therefore, in almost continuous resonance. As a result, DPM techniques must be employed to control this class of inverter. The relative high levels of low frequency harmonics so introduced (section 3.1.2) may adversely affect performance in some applications. A further concern is the continuous flow of current in the resonant inductor. Levels of current considerably in excess of highest per-phase load current mean that a conservative, and therefore bulky, design is necessary to avoid unacceptable conduction losses. Table 5.1.1 summarises the discussion above.

	UNCLAMPED	ACTIVE CLAMPED	PASSIVE CLAMPED
additional switches	0	1	0
other additional components	1L, 1C	1L, 2C	1C, 1T, 1D
control complexity of resonant circuit	high	very high	moderate
control type	DPM	DPM	DPM
switching status of inverter switches on/off	ZVS /ZVS	ZVS /ZVS	ZVS /ZVS
switching status of auxiliary switches on/off	---	ZVS/ZVS	---
max. voltage stress of inverter switch	$3V_{dc}$	kV_{dc}	kV_{dc}
max. voltage stress of auxiliary switch	---	$(k-1)V_{dc}$	---
current stress of inverter switches ?	yes	yes	yes
current stress of auxiliary switches ?	---	yes	---
need of snubber capacitor	no	no	no
comments	voltage stress unacceptable	difficulties in control of clamp voltage, clamp capacitor must be pre-charged	complicated transformer design

Table 5.1.1: Comparison of basic RDCL inverters (T: transformer, D: Diode)

5.1.2 Comparison of PRDCL Topologies

The earliest PRDCL topologies [5.9 and 5.10] used four additional switches to allow resonant transitions between dc-link capacitor and the inverter. Besides their high circuit complexity, one of the four switches suffers a voltage stress of at least twice the dc-link voltage and a current stress of at least twice the load current [5.11 and 5.12]. Because of the inherent repetitive notches in the inverter input voltage, the average supply voltage is reduced, which limits the output power when using conventional basic space vector control.

Reference [5.13] suggests splitting and transferring the resonant capacitor of circuits [5.8] and [5.9] from the input side to each inverter switching devices (section 3.3.1). The capacitors

have two functions: operation during resonant mode and operation during snubber mode, depending on the applied control scheme and directions of phase currents. The value of the 'resonant-snubber' capacitor is given in equation 3.3.1. The transfer of the capacitor allows the application of modified PWM control (mPWM) to limit the average voltage drop of the inverter input voltage. In addition all switches could be rated to the dc-link voltage. However, the impact on transition time when using snubber capacitors has been already discussed in section 3.3.3. It was found, that under light load conditions, the commutation time extends to unacceptable values. Another disadvantage of mPWM is the worse output harmonics as discussed in Chapter 3.

Based on topology [5.13] many topologies have been derived: for example topologies [5.11] and [5.14]. These PRDCL topologies were mainly motivated by the desire to optimise the circuit arrangement with the applied mPWM scheme. In each case the number of additional switches is always three. The topology proposed in reference [5.14] operates in a similar fashion to the ACPI discussed in section 4.2.2. The topology makes use of the split input capacitors, which introduces subtle charge balance problems. In order to realise softswitching for the full load range, the timing is also critical to control commutation energy [5.12].

Most of the PRDCLs mentioned so far store energy during the first half of the resonant mode in the commutation inductor. During the remainder of the converter cycle, the current freewheels in the inductor and produces conduction losses, especially when the modulation index is low [5.12]. References [5.15] and [5.16] use mixed capacitive and inductive storage elements to store the oscillation energy [5.15] thus avoiding freewheeling losses. In addition, both topologies use just two auxiliary switches. The main difference between the topologies is the use of a pre-charged resonant capacitor in topology [5.15] for energy transfer. This capacitor is relatively large and it seems to be difficult to balance the voltage across it. Both topologies suffer from the disadvantage of requiring mPWM techniques and therefore do not handle light load conditions.

To summarise, none of the PRDCL topologies is 'true' PWM controllable thus mPWM techniques must be applied. Some authors developed circuit specific mPWM control techniques (cs mPWM), but mPWM and cs mPWM are not satisfactory for drives applications (see section 3.3.3). In addition, the switch in the dc-link path, that is characteristic for PRDCLs, leads to constant high on-state losses, because most of the time the switch is on. The PRDCL is the only resonant dc-link topology that keeps the voltage stress across the inverter switches to the dc-link voltage level. Table 5.1.2 compares various PRDCL topologies.

	[5.10]	[5.9]	[5.13]	[5.12]	[5.15]	[5.16]
additional switches	4	4	3	3	2	2
other additional components	1L, 2C	1L, 2C	1L, 6C	1L, 1C	1L, 7C	1L, 7C, 1D
control complexity of resonant circuit	high	high	moderate	high	fairly high	moderate
control type	cs mPWM	cs mPWM	mPWM	cs mPWM	mPWM	mPWM
switching status of inverter on/off	ZVS /ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ ZVS	ZVS/ ZVS	ZVS/ZVS
switching status of additional switches on/off	3 ZVS/ ZVS, 1 ZCS/ZVS	3 ZVS/ ZVS, 1 ZCS/ZVS	1 ZVS/ ZVS, 2 ZCS/ZCS	3 ZVS/ ZVS	1 ZVS/ ZVS, 1 ZCS/ ZVS	1 ZVS/ ZVS, 1 ZCS/ZVS
max. voltage stress of inverter switch	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
max. voltage stress of auxiliary switch	2 V_{dc}	2 V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
current stress of inverter switches ?	yes	yes	yes	no	yes	yes
current stress of auxiliary switches ?	yes	yes	yes	no	yes	yes
need of snubber capacitors	no	no	yes	no	yes	yes
comments	improved control to [5.9]	many devices	problems at light load	also known ZVT	pre-charged capacitor	problems at light load

Table 5.1.2: Comparison of several PRDCL topologies (cs mPWM: circuit specific mPWM. ZVT: PRDCL topologies that applies zero voltage switching to IGBTs and diodes without increasing their voltage or current stresses are also known as (ZVT) zero voltage transition converter. The same applies for (ZCT) zero current transition converter)

5.1.3 Comparison of q-RDCL Topologies

The earliest active clamp q-RDCL topologies were derived from active clamp basic RDCL topologies and used 'resonant-snubber' capacitors. The clamp mode time of the active clamp basic RDCL was set to be rather large compared to the resonant mode time. This could be done by precise definition of the LC relation [5.17]. A longer duration of clamping time gives the opportunity to include a certain amount of PWM control [5.17]. Nevertheless, strictly speaking, these early topologies were not 'true' q-RDCLs, because the dc-link voltages still underwent continuous cycle by cycle resonant oscillation that was only interrupted by a long clamp mode. The large circulating currents present during the long clamp mode also led to significant inductor conduction losses.

Other early q-RDCL topologies [5.18] short the resonant inductor in the dc-link path by using a switch. During the time where no change in the inverter switching state is commanded, the dc-link voltage is applied across the input of the inverter. On opening the switch a resonant mode is activated between L and C. In this topology C is across the input of the inverter and every change in switching status of each switch must share this capacitor. In this configuration neither mPWM nor PWM can be applied[5.17].

As q-RDCL topologies have progressed, many circuits and control ideas have been published [5.19-5.22]. However, all topologies have one main drawback: an increase in the number of additional components and switches. For example, the topologies of references [5.17 and 5.18] use only one additional switch, whereas the topology of reference [5.21] uses four.

A somewhat different topology in the long list of q-RDCLs is proposed in reference [5.23] (Figure 3.4.1). Firstly only two additional switches are required. Secondly the clamp capacitor is pre-charged to over the dc-link voltage level. None of the other q-RDCLs use clamp capacitors that are pre-charged to a level above the dc-link voltage. Topology [5.23] is explained in detail in section 3.4.1. Unfortunately one of the auxiliary switches sees a high inrush current. This occurs because of a flow of charge from the clamp capacitor into the parasitic capacitances of the inverter devices. The inrush current leads to EMI problems and turn-on losses.

As already discussed for the active basic RDCL topologies, the largest difficulty in implementing the active clamp q-RDCL lies in maintaining the correct level of charge on the clamp capacitor. In general, active clamp techniques tend to pump excessive charge into the clamp capacitor in order to ensure that the link voltage will reach zero during resonant transition. As a result the clamp voltage will tend to increase without limit. Regulation of the clamp voltage seems to be very difficult, especially as switching frequencies are increased.

The development of the passive clamp q-RDCL has not been as dramatic as the development of the active clamp q-RDCL. Figure 3.4.6 shows the standard arrangement of a passive clamp q-RDCL. Although the control of the circuit is less complicated compared to an active clamp q-RDCL, a complicated transformer design is needed as discussed in section 5.1.2. Reference [5.24] describes an arrangement to reduce the number of switches from two to one. It replaces one of the switches in Figure 3.4.6 with an inductor. This additional inductor must be magnetically coupled with the transformer, adding further to its complexity.

	[5.18]	[5.17]	[5.21]	[5.23]	[5.8]	[5.24]
additional switches	1	1	4	2	2	1
other additional components	1L, 2C, 1D	1L, 7C	2L, 1C, 1VS, 1D	1L, 2C	1C, 1T	1C, 1T
control complexity of resonant circuit	high	high	complex	fairly high	moderate	moderate
control type	cs PWM	cs PWM	PWM	PWM	PWM	PWM
switching status of inverter on/off	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS
switching status of additional switches on/off	1 ZVS/ZVS	1 ZVS/ZVS	4 ZVS/ZVS	1 ZCS/ZVS, 1 ZVS/ZVS	2 ZCS/ZCS	1 ZCS/ZCS
max. voltage stress of inverter switch	kV_{dc}	kV_{dc}	kV_{dc}	kV_{dc}	kV_{dc}	kV_{dc}
max. voltage stress of auxiliary switch	$2V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}
current stress of inverter switches ?	yes	no	no	no	no	no
current stress of auxiliary switches ?	yes	yes	yes	yes	yes	yes
need snubber capacitors	no	yes	no	no	no	no
comments	also known as synchronised RDCL	clamp mode longer resonant mode	many devices	inrush-current during turn-on of one auxiliary device	difficult transformer design	very difficult transformer design

Table 5.1.3: Comparison of several q-RDCL topologies (VS: voltage source, T: transformer, D: Diode, cs PWM: circuit specific PWM)

Finally a comparison of the output harmonic spectra between active and passive clamp q-RDCL is shown in Figure 5.1.1. The comparison is done using PSPICE simulation. The simulation shows that the passive clamp q-RDCL, produces high distortions at low frequency. That is because the passive clamp q-RDCL has no charge control during resonant mode. The active clamp q-RDCL is able to control the charge balance using the clamp switch.

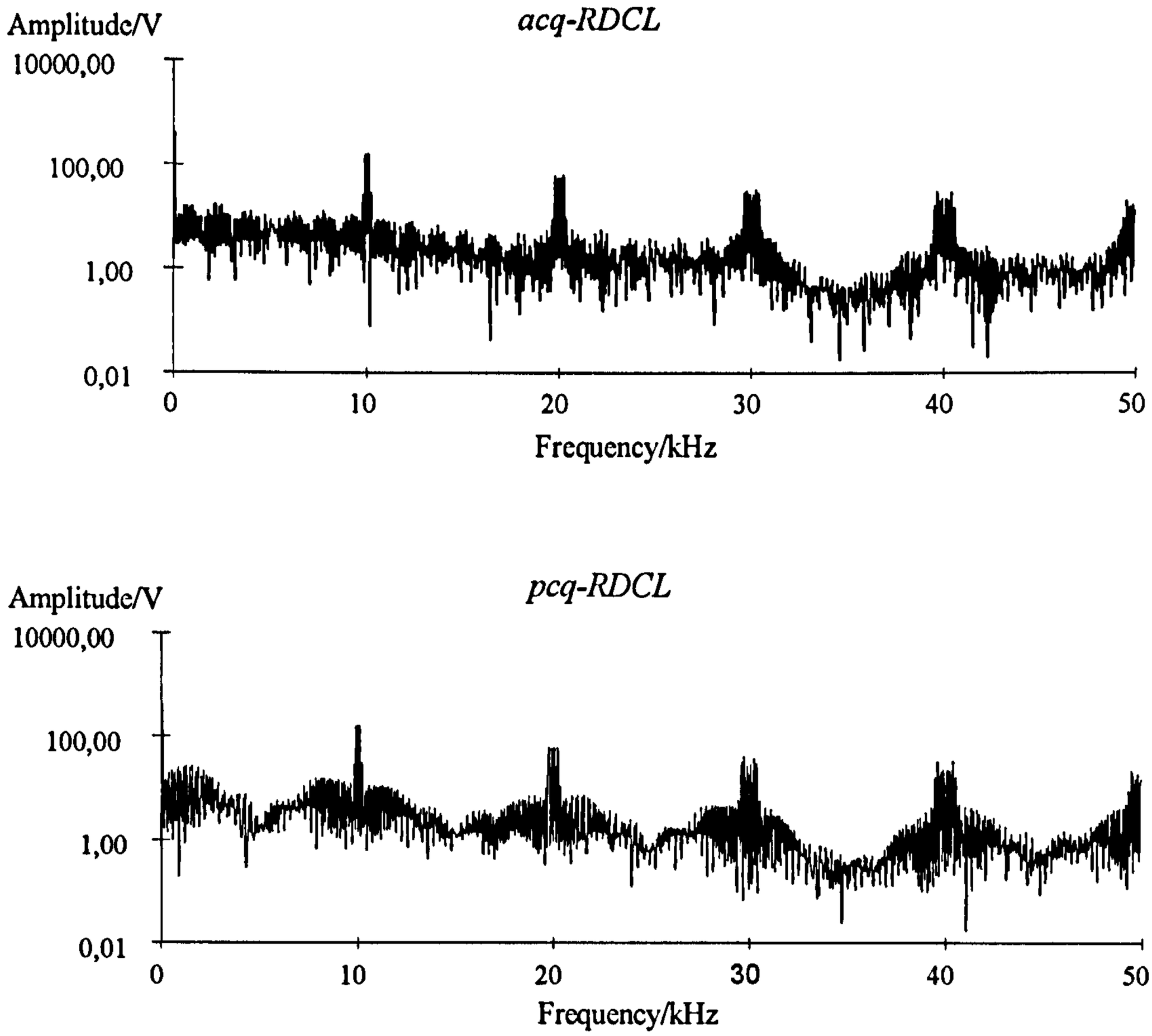


Figure 5.1.1: Output spectral performances of active and passive clamp q-RDCL (V_{dc}=600V, f_s=10kHz, f=50Hz, m_a=0,5)

5.2 Comparison of Pole Commutated Inverters

As in section 5.1 the comparison is based on the author's own theoretical work, simulation results and statements given from other authors.

5.2.1 Comparison of RPI Topologies

The constantly increasing or decreasing current of the resonant inductor of the basic RPI [5.25] (Figure 4.1) leads to very high inductor losses and strong limitations on the range of application of PWM control. As a consequence it is of little interests for drives applications.

The resonant inductor current of the ADPI [5.26] (Figure 4.1) flows continuously and has to be substantially larger than the load current to provide enough energy for the resonant mode and the freewheeling mode. High peak current (larger than 2.5*I_{load}) in the resonant inductor during the freewheeling mode causes significant overall losses. To limit this peak current the

capacitors parallel to the clamp diodes have to be set very large at the expense of the output voltage transition time degree of PWM controllability.

The TADPI [5.27] (Figure 4.1) reduces the inductor freewheeling time to around 30% compared to the ADPI topology (Figure 4.1.8). Careful design of the inductor is of great importance in keeping the overall losses down. These include the on-state losses of additional diodes and those of the transformer. PWM controllability is limited as for the ADPI.

	BASIC RPI	**ADPI**	**TADPI**	**N-LRPI**
additional switches	0	0	0	0
other additional components	3L, 3C	3L, 12C, 4D	2L, 15C, 3T, 12D	6L, 6C
control complexity for resonant circuit	moderate	fairly high	fairly high	high
control type	pseudo PWM	PWM	PWM	PWM
switching status of inverter on/off	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS
switching status of additional switches on/off	---	---	---	---
max. voltage stress of inverter switch	V_{dc}	V_{dc}	V_{dc}	V_{dc}
max. voltage stress of auxiliary switch	$2V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}
current stress of inverter switches ?	yes	yes	yes	yes
current stress of auxiliary switches ?	---	---	---	---
need freewheel current?	yes	yes	yes	yes
comments	for drives not suitable	high freewheeling current	many devices	need coupled saturation inductors

Table 5.2.1: Comparison of several RPI topologies (pseudo PWM: current ramps up and down. To limit excessive overcurrent, pole transition must be activated, even when no change from controller is commanded)

The N-LRPI (Figure 4.1) has a distinct advantage over other RPI topologies in that the installed switching power of the semiconductor is close to 1 pu. The first proposed topologies [5.28 and 5.29] needed an additional current source to maintain charge balance across the dc-

link capacitors. Later versions [5.30-5.32] eliminate the current source using an additional current feedback winding on the saturable inductor. However, the mode of operation of any N-LRPI requires that changes in duty ratio must be accompanied by changes in switching frequency [5.32]. Table 5.2.1 shows a comparison of the RPI topologies.

All RPIs suffer high losses during freewheeling mode and have limited PWM control capability. Furthermore, many RPI carry a large freewheeling current, particularly under light load conditions. Resonant inductor losses and dv/dt stress can be only reduced by limiting the PWM range.

5.2.2 Comparison of ARPI Topologies

The resonant transition times of the RPI topologies are relative long. Long transition times degrade PWM controllability. To bring PWM control one step closer, the basic ARPI can be used (Figure 4.1). Here the ARPI may be operated with [5.25] or without a freewheeling mode [5.33]. In both topologies the load current must be used to charge the device snubber capacitors during half of switching transitions. This produces variable transitions times and decreases the inductor current but limits performances at light load currents. The current stress of all switches proposed in reference [5.25] varies between I_{load} and $1.5*I_{load}$. Aside from academic interest in this topology one must conclude that a practical implementation is hindered by 6 additional devices rated to the same values as the main switches and the complex control structure. The topology in reference [5.33] uses auxiliary switches that are from smaller power range than the main switches. Nevertheless the number of devices and control complexity makes both circuits unattractive for drives applications.

The ACPI [5.34] (Figure 4.1) seems to offer a good compromise between voltage transition time and degree of PWM controllability. Firstly, no freewheeling current flows through the resonant pole inductor, giving much reduced losses. Secondly, a high degree of PWM control can be achieved without excessive device stress at higher inverter switching frequency. This circuit does, however, require a large number of active devices and has hitherto been discounted largely on cost grounds. An additional problem may arise under low frequency output conditions due to asymmetric charging/discharging of the split dc-link capacitance. This will cause the mid-point voltage to drift unless charge balance control is applied.

Attempts to eliminate the charge drift of the ACPI have resulted in the D-CRSI [5.35] and the S-CRSI [5.36] topologies (Figure 4.1). The D-CRSI has the advantages of avoidance of over-voltage ringing due to the junction capacitances of the diodes and parasitic components in the auxiliary circuit. It is, therefore, suitable for multiphase operation without circulating current

between off-state branch and its corresponding output load current [5.35]. However, the drawbacks for both topologies is that in each case two legs must change state simultaneously limiting the flexibility of any applied PWM control strategy.

	BASIC ARPI	ACPI	D-CRSI	S-CRSI
additional switches	6	6	6	6
other additional components	3L, 12C	3L, 6C	3L, 6C	3L, 6C, 1D
control complexity for resonant circuit	fairly high	moderate	high	high
control type	PWM	PWM	pseudo PWM	pseudo PWM
switching status of inverter on/off	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS	ZVS/ZVS
switching status of additional switches on/off	ZVS/ZVS	ZCS/ZCS	ZCS/ZCS	ZCS/ZCS
max. voltage stress of inverter switch	V_{dc}	V_{dc}	V_{dc}	V_{dc}
max. voltage stress of auxiliary switch	$2V_{dc}$	$0.5V_{dc}$	V_{dc}	V_{dc}
current stress of inverter switches ?	no	no	no	no
current stress of auxiliary switches ?	yes	yes	yes	yes
need freewheel current	both possible	no	no	no
comments	can be controlled with or without freewheeling current	all three phases must be connected to the same mid-point	non-adjacent space vector control	non-adjacent space vector control

Table 5.2.2: Comparison of several ARPI topologies (pseudo PWM: non-adjacent space vector control, Figure 4.2.9)

5.3 Switching Speed Limitations of PT and NPT IGBTs

In practical semiconductor switches, current and voltage transitions do not occur instantaneously. This situation is exacerbated in bipolar devices by the need to establish and remove quantities of stored charge (the well known forward and reverse recovery effects in diodes and voltage and current tailing effects in IGBTs are all examples of this phenomenon). In controlled devices, this manifests itself as a variable delay between the application of the

control signal and the demanded change in switch state. Clearly, any ZVS or ZCS scheme which requires a controlled switch to change state at the zero point will be sensitive to such delays. To avoid such problems, most softswitching implementations employ the uncontrolled characteristic of the diode for either the turn-on or turn-off transition. Consider, for example, the combination of IGBT and antiparallel diode. In ZCS applications, turn-on is achieved using the IGBT while turn-off is achieved by forcing the current to zero using an external circuit. The external circuit is arranged to provide the necessary current reversal between turn-on and turn-off and the IGBT is turned off in a zero current manner. For ZVS operation, turn-off is achieved using the IGBT while turn-on requires the diode to be forced into conduction first before turning on the IGBT. Again, the external circuit must ensure the required current reversal.

The operation of bipolar switching devices is also strongly influenced by the rate of change of applied voltage or current. In the case of diode commutation, the rate of change of current must be limited to prevent excess reverse recovery current. For example, when used as a series blocking device in a ZCS application (e.g. the auxiliary devices in an ACPI), the diode's recovery characteristics must be respected when choosing a suitable value for the ZCS inductor. It is also sensible to limit di/dt values in ZVS applications to avoid potential reverse recovery currents.

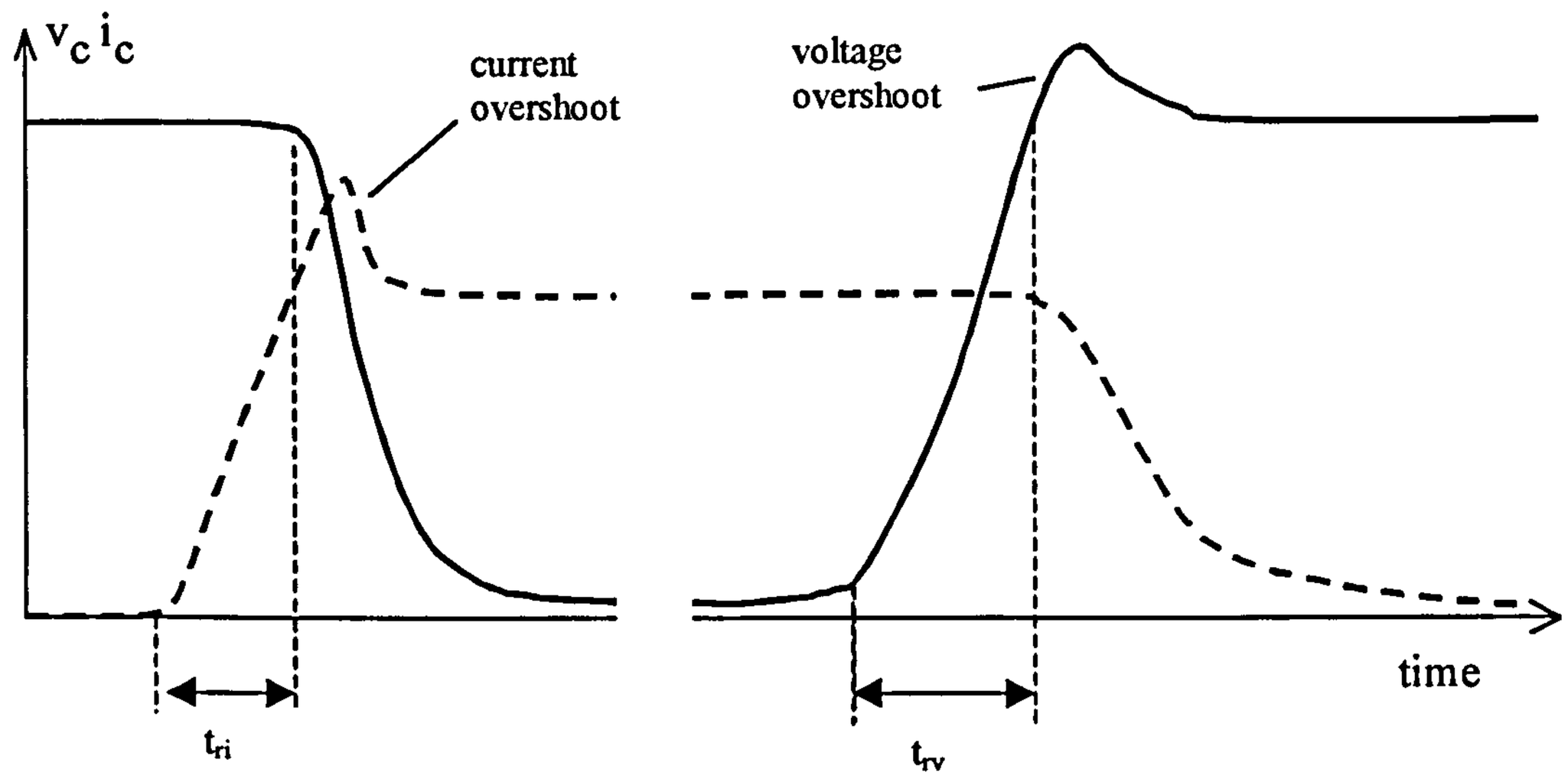


Figure 5.3.1: IGBT collector current (dash line) and collector voltage (solid line) waveforms for a hard switched inverter bridge leg under inductive load conditions. Current overshoot is due to diode reverse recovery, voltage overshoot is due to stray inductance and diode forward recovery

Under hard switched inductive load conditions, IGBTs suffer significant losses due to current tailing at turn-off and, to a lesser extent, voltage tailing at turn-on (Figure 5.3.1).

These losses are associated with the build up (turn-on) and decay (turn-off) of the stored charge in the wide base region of the device (Figure 5.3.2).

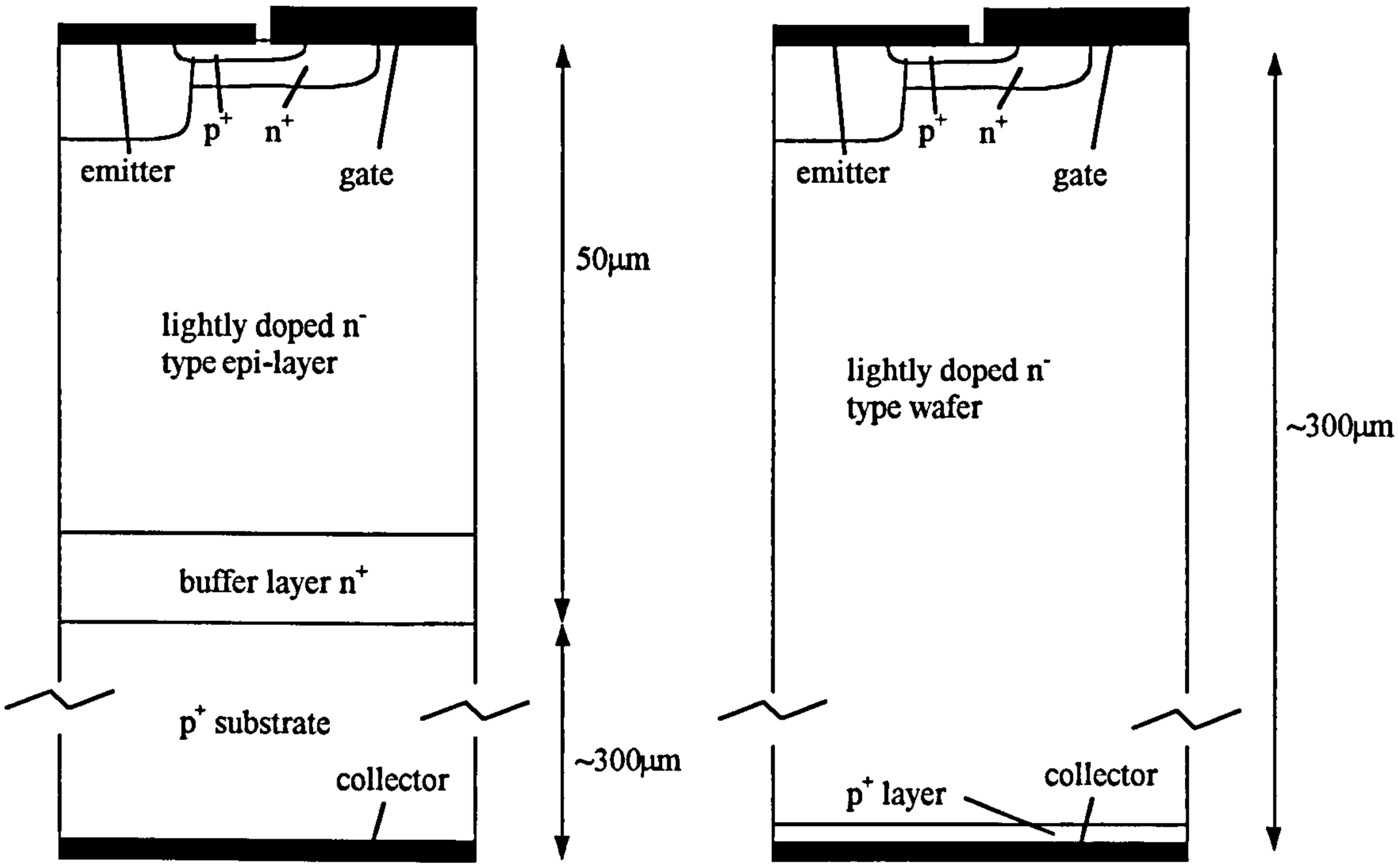


Figure 5.3.2: Punch through (PT) and non punch through (NPT) IGBT structures

To avoid voltage tailing losses in softswitching, di/dt values must be limited to ensure that the level of n-base charge tracks the current. In practical terms this means that the current rise time t_{ri} should be much greater than the n-base diffusion time t_{NB}:

$$t_{ri} >> t_{NB} \qquad (5.3.1)$$

Adequate conductivity modulation (i.e. sufficient levels of charge) can only be attained if the lifetime of carriers in the n-base, τ, is comparable with the n-base diffusion time [5.37]. Hence:

$$t_{ri} >> \tau \qquad (5.3.2)$$

During hard switched turn-off, n-base charge extraction occurs through a mixture of recombination and carrier sweep out during the turn-off dv/dt and recombination alone during the subsequent tail period. In softswitching, dv/dt driven carrier sweep and natural recombination act together throughout the turn-off process.

The effect of the charge sweep out term can be seen on many softswitching waveforms as a characteristic 'bump' in the collector current during the rise of collector voltage. To avoid the resulting switching losses it is necessary to make the softswitching voltage transition time, t_{rv}, much longer than the carrier lifetime.

$$t_{rv} >> \tau \tag{5.3.4}$$

It is clear that the carrier lifetime performs a central role in determining the limits to effective softswitching operation. The lifetime is, in turn, determined by the need to produce effective conductivity modulation in the base region of the diode or IGBT [5.37]:

$$\tau > \frac{w_{NB}^2}{4D_a} \tag{5.3.5}$$

where w_{NB} is the width of the n-base region and D_a is the ambi-polar diffusion coefficient. For typical punch-through (PT) epitaxial IGBT and pin diode structures, the n-base width can be estimated from the blocking voltage V_{BR}:

$$w_{NB} \approx \frac{V_{BR}}{E_C} \tag{5.3.6}$$

where E_C is the critical field in silicon (approx. 250kV/cm). Combining equation (5.3.5) and equation (5.3.6) shows that the high-level lifetime must vary as the square of the breakdown voltage. For example, a 1200V device could be expected to display a carrier lifetime of some 200ns. This in turn places a lower limit on softswitching transition times of around 600ns (3τ) for significant reduction in switching loss. For non-punch-through (NPT) IGBTs, the lifetime is determined by the thickness of the silicon wafer used in processing. For example, a typical wafer thickness of 300μm requires a lifetime of around 7.5μs. Even allowing for some increase in forward voltage drop it is unlikely that this lifetime could be reduced much below 2μs which is still a factor of 10 larger than in a 1200V PT structure. For hardswitching applications this is not a problem since the longer lifetime is compensated by a much reduced initial tail current, leading to comparable or even reduced switching loss [5.38]. Under softswitching conditions, however, the requirement for greatly increased transition times mean that NPT devices have limited application.

5.4 PWM Limitations of Softswitching Topologies

From the foregoing discussion, it is clear that the voltage and current transition times must exceed certain minimum values for the full benefits of softswitching to be realised. In addition, the voltage transition times should not be sensitive to changes in load current. These requirements effectively define maximum values for both the resonant frequency and resonant tank impedance:

$$\omega_0 = \frac{1}{\sqrt{LC}} < \frac{1}{V_{eff}} \left.\frac{dv}{dt}\right|_{max} \tag{5.4.1}$$

$$Z_0 = \sqrt{\frac{L}{C}} < \frac{V_{eff}}{I_{load,max}} \tag{5.4.2}$$

V_{eff} is the effective voltage amplitude of the resonant pulse and is determined by the converter topology and level of boost current. In general it should be slightly greater than the dc

reservoir voltage, V_{dc}, for RDCL topologies and slightly greater than $V_{dc}/2$ for the ACPI and related topologies. A further restriction might be placed on the maximum rate of change of current and hence the resonant inductor:

$$L > V_{dc}\left(\left.\frac{di}{dt}\right|_{max}\right)^{-1} \tag{5.4.3}$$

It has been shown that the various classes of converter topology exhibit different per-unit (pu.) transition times. For example, the active clamp q-RDCL with a clamp factor of 1.2 has a transition time of around 2.06 pu. while the ACPI displays an average transition time of just 0.5 pu. The minimum times for which a high ($t_{h,min}$) or low state ($t_{l,min}$) can be applied to the output of an inverter leg may then be estimated (Figure 5.3.3) and the PWM range available at a given switching frequency determined:

$$R_{PWM} = 1 - \frac{t_{h,min} + t_{l,min}}{T_s} = 1 - 2N_{pu}T_0 f_s \tag{5.4.4}$$

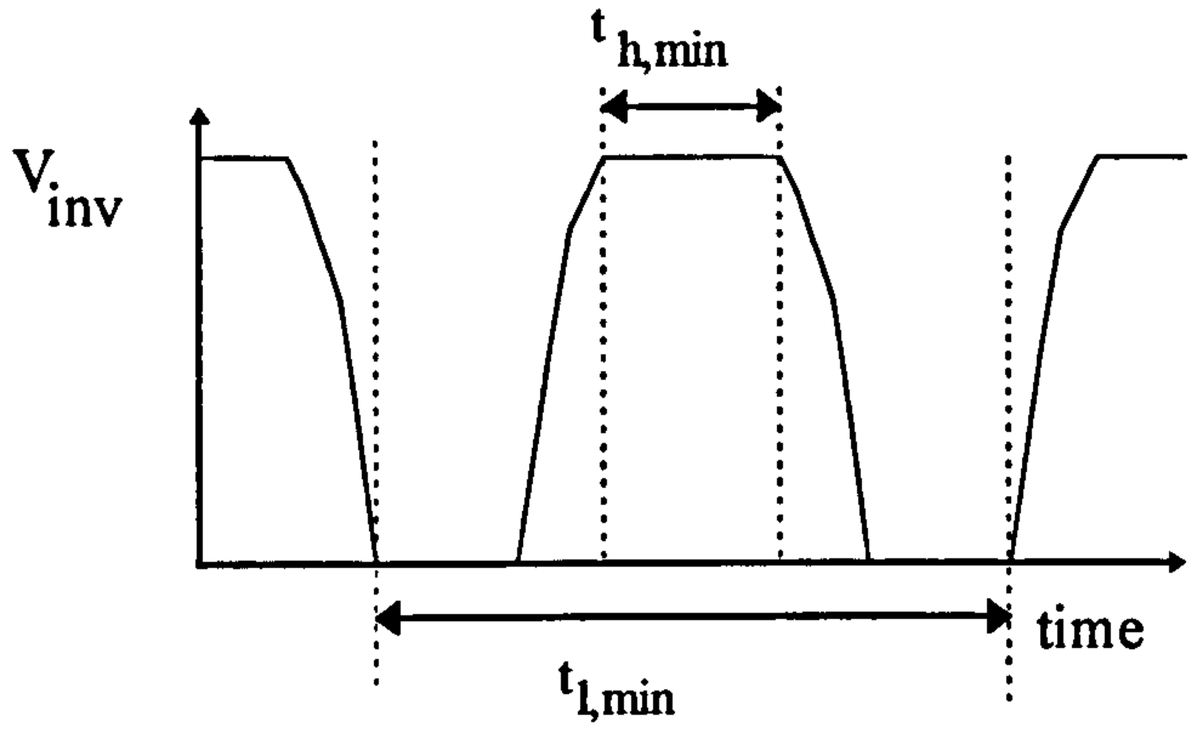


Figure 5.3.3: Inverter leg voltage for a RDCL inverter showing minimum high and low leg output state durations

For a given topology and dc reservoir voltage, the maximum resonant frequency compatible with a softswitching transition time of t_{ss} may be estimated:

$$\omega_0 V_{eff} < \frac{V_{dc}}{t_{ss}} \tag{5.4.5}$$

Substituting this limiting value into (5.4.4) yields:

$$R_{PWM} = 1 - 4\pi N_{pu} t_{ss} f_s \frac{V_{eff}}{V_{dc}} \tag{5.4.6}$$

The equivalent PWM range for a hard switched topology may be determined from the minimum pulse width time t_b:

$$R_{PWM} = 1 - 2t_b f_s \tag{5.4.7}$$

Equations (5.4.6) and (5.4.7) permit a comparative assessment of PWM control range to be made (Figure 5.3.4). It has been assumed that the minimum pulse width time can be well approximated by the minimum softswitching transition time.

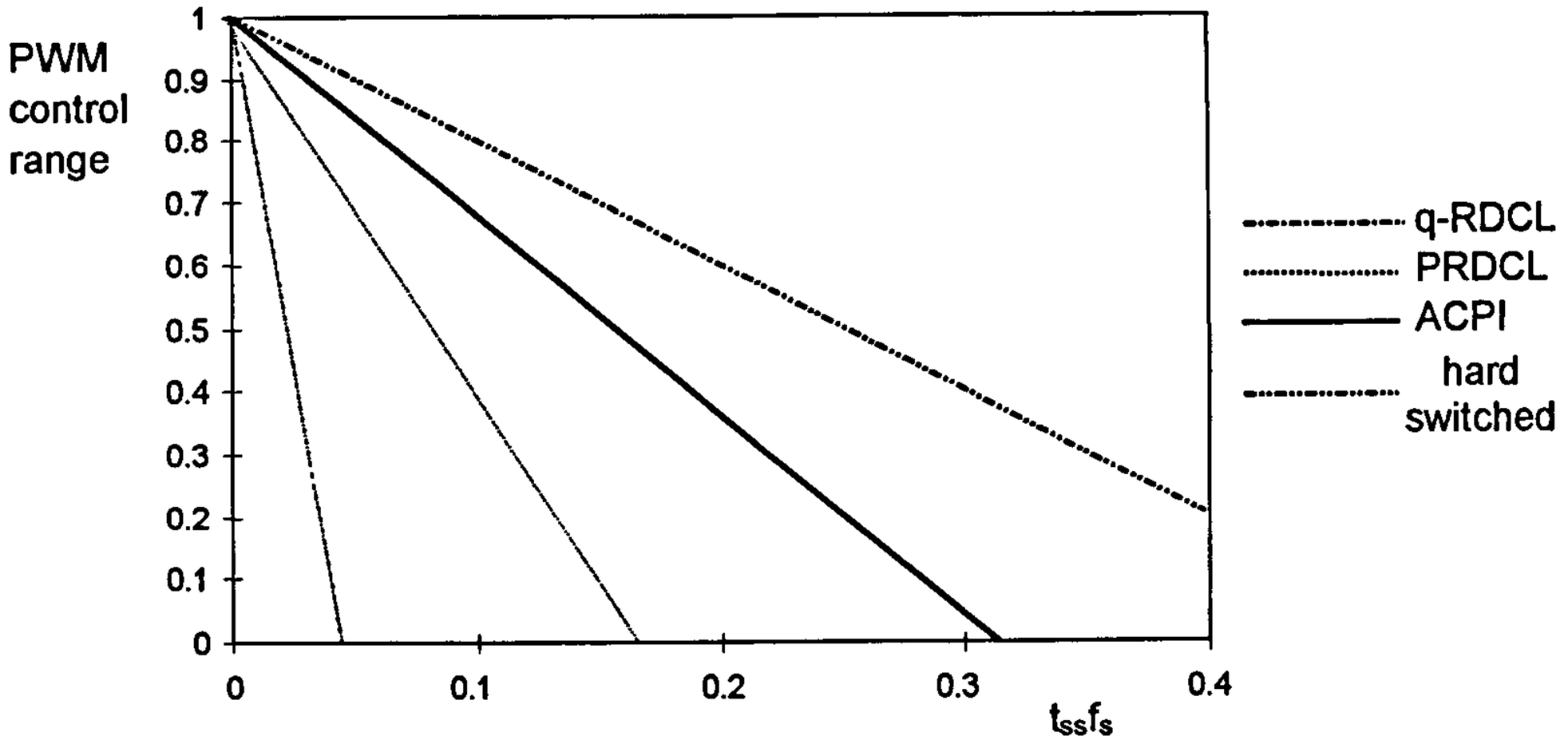


Figure 5.3.4: Basic space vector PWM control range as a function of normalised switching frequency. For RDCL topologies, control performance is also affected by the available PWM resolution - a control range of 2/3 corresponds to the onset of DPM operation

The above discussion of PWM range assumes that each leg may be considered independently. While this is true for PCI topologies, the common dc link of RDCL inverters implies a degree of coupling. Switching state transitions in different inverter legs must either occur during the same link transition or be separated by a time which is no shorter than the link transition time itself. It is, therefore, possible to define a resolution figure for RDCL topologies:

$$\Delta_{PWM} = 2\pi N_{pu} t_{ss} f_s \frac{V_{eff}}{V_{dc}} \qquad (5.4.8)$$

As the PWM frequency increased, both the PWM range and PWM resolution will be decreased until the link is in continuous resonance. In the case of basic space vector control, six link transitions are required in each PWM cycle. If the PWM frequency is increased to the point where the PWM resolution equals 1/6 (this corresponds to a PWM range of 2/3 in Figure 5.3.4), the inverter will be forced into a DPM control regime. It is also worth noting that the resonant link voltage is seen by all legs of the inverter at each transition. This not only increases the voltage distortion at the inverter output but effectively triples the number of voltage transitions seen by the motor windings. As many as half of these link transitions may be eliminated in certain topologies by placing individual snubber capacitors across the main bridge switches rather than utilising a single resonant capacitor. In this case, the load current is used to charge the snubber capacitance during IGBT turn-off. The voltage transition time is then dependent on the load current, leading to impracticable slow transitions under light load conditions. As the individual snubber capacitance is just one third of the capacitance seen during resonant transitions (equation 3.3.1), it is also necessary to ensure the highest load currents do not produce excessive device dv/dt. A technique to reduce the number of link transitions, involving modification of the basic space vector PWM strategy (mPWM), has

already been discussed. It has been shown, however, that this typically results in reduced output current quality and is, therefore, of limited application (section 3.3.3).

5.5 Overall Comparison of Converter Topologies

The basic RDCL, active clamp and passive clamp basic RDCL find little application in practical circuits because of the uncontrolled inverter leg voltage and the very high levels of resonant inductor current. DPM control techniques must be employed to control this class of converter.

PRDCLs show bad output harmonics performance because of the use of mPWM - a situation that becomes worse under light load conditions.

Q-RDCLs are a mixture between PRDCL and active or passive clamp basic circuit. This combination allows a high variety of topologies. However, when increasing inverter switching frequency the output performance of this topology becomes similar to a DPM controlled active or passive clamp basic RDCL, for given LC values. Changing the LC values (making them smaller) allows a higher PWM range but dv/dt stress increases, ultimately approaching the values seen in hardswitching. In addition, all q-RDCL employ a pre-charged capacitor with the attendant problem of maintaining the charge constant at high converter switching frequency.

RPI topologies suffer from high losses during freewheeling mode and have limited PWM control capability. Furthermore, they carry a large freewheeling current, which introduces additional losses that are particularly noticeable under light load conditions. Resonant inductor losses and dv/dt stress can only be reduced by using either additional switches or by limiting the range of PWM control. In addition retaining high PWM resolution at high switching frequency demands increased output dv/dt stress. Of all ARPI variants discussed in the thesis, the ACPI seems to be the most promising offering a high degree of PWM control without excessive device stress at high frequency.

Table 5.5.1 provides a comparison of the resulting softswitching topologies and the hard switched topology according to a variety of performance metrics.

	Q-RDCL	PRDCL	ACPI	HARD SWITCHED
additional components	+	+	++	0
relative PWM range: equation 5.5.1	0,08	0,32	0,63	1,0
limited PWM resolution?	Yes	Yes	No	No
inverter switching frequency	+	+	++	0
reduced overall switching losses	+	+	+	0
additional conduction losses	++	++	+	0
overall efficiency	+	+	++	0
output voltage distortion	++	++	0	+
output dv/dt control	+	+	+	0
current output harmonics	+	+	0	+
size and weight	0	0	0	0
initial cost	+	+	++	0

Table 5.5.1: Performance comparison of some common softswitching voltage source inverter topologies (+: high, ++: very high)

The PWM control performance figures are derived from the PWM range defined in equation (5.4.6):

$$\eta_s = \frac{V_{dc}}{2\pi N_{pu} V_{eff}} \tag{5.5.1}$$

All figures assume a common dc reservoir voltage level, identical switching transition times and make use of the best, theoretical per-unit transition times. Of the soft switched topologies, it is clear that the ACPI performs best while active clamp q-RDCL topologies are at distinct disadvantage. Identical switching transitions mean that switching losses and levels of output dv/dt are reduced to similar levels in all considered soft switched topologies. The reduction in softswitching loss must, of course, be considered against the losses in the resonant tank and any auxiliary switches. In the case of RDCL topologies, additional conduction losses occur as the result of either an inductor or switch in series with the main power path while additional output voltage distortion arises because of limited PWM resolution.

It should be noted that the PWM control range and therefore the PWM control performance effectively determines the ranges of output voltage available from the converter. Using Figure 5.3.4 the voltage is therefore a function of transition time and inverter switching frequency. The transition time is determined for both, hard and soft switched converter, by the physical limitations due to switching behaviour of the devices or the LC values. The transition time of the ACPI has to be set lower than that of the hard switched converter to limit dv/dt stress (e.g. transition time of ACPI is twice as long as for a hard switched converter). To allow the ACPI

the same PWM control range the switching frequency must be higher than that of the hard switched converter (e.g. more than twice). As will shown in Chapter 7 an increase of switching frequency of the ACPI is attainable, because of its low losses.

In the final reckoning, performance benefits must be weighed against the additional cost. The ACPI variant may have a brighter future if a sufficient large number of components can be integrated into a single power module, additional control hardware could be limited and number of sensors reduced. Regrettably semiconductor industry have not yet offered modules that allow integration of the switching arrangement of ACPI in one module. In addition power semiconductors have been optimised for hardswitching. Optimisation for soft switched operation could yield reductions in silicon area. Finally further reduction in cost is possible once the number of sensors needed for the ACPI can be reduced. The following chapter describes a control method that reduces the number of sensors and limit the control hardware.

Chapter 6

EXPERIMENTAL ARRANGEMENTS

This chapter describes the arrangement of an electric drive system. Chapter 6 is sub-divided into five sections. Section 6.1 describes in general the experimental set-up of the converter test circuit. Section 6.2 analyses the power converter technology. In addition this section analyses a novel scheme for sensorless control of the ACPI, that has not been published elsewhere. The hardware set-up of the controller is discussed in section 6.3. The load configuration and test equipment are described in section 6.4 and 6.5 respectively. More detailed circuit diagrams are given in Appendix B for the power converters and their additional electrical and electronic circuits. Also Appendix B includes the hardware set-up of the controller and the software code.

6.1 Experimental Arrangements of the Drive Set-up

An electric drive system for induction motors comprises of four main elements; the electrical power converter, the induction motor, the mechanical load and the control electronics. For experimental purposes the mechanical load and the induction motor can be simplified to an inductor-resistor load bank. This simplification is allowed when focusing on switching losses, overall efficiency or stress of the converter rather than on drive performances.

Each converter is connected between a 3-phase power supply and the 3-phase load bank. The load is represented by three inductors and three large resistors. Each output phase of the inverter is connected to an inductor connected in series with a resistor. The bulky resistance of the load bank allows around 20kW of power dissipation and all three resistor-inductor phases can be either star or delta connected. The converter is controlled by an electronic control system communicating with a PC. Figure 6.1.1 shows the experimental test circuit of the converters. During the developing process of the test bench the design philosophy behind the complete system was to produce a test bench that would be flexible (allowing quick rearrangements in the set-up), modular (easy exchanges of components) and test friendly (accessibility for measurements).

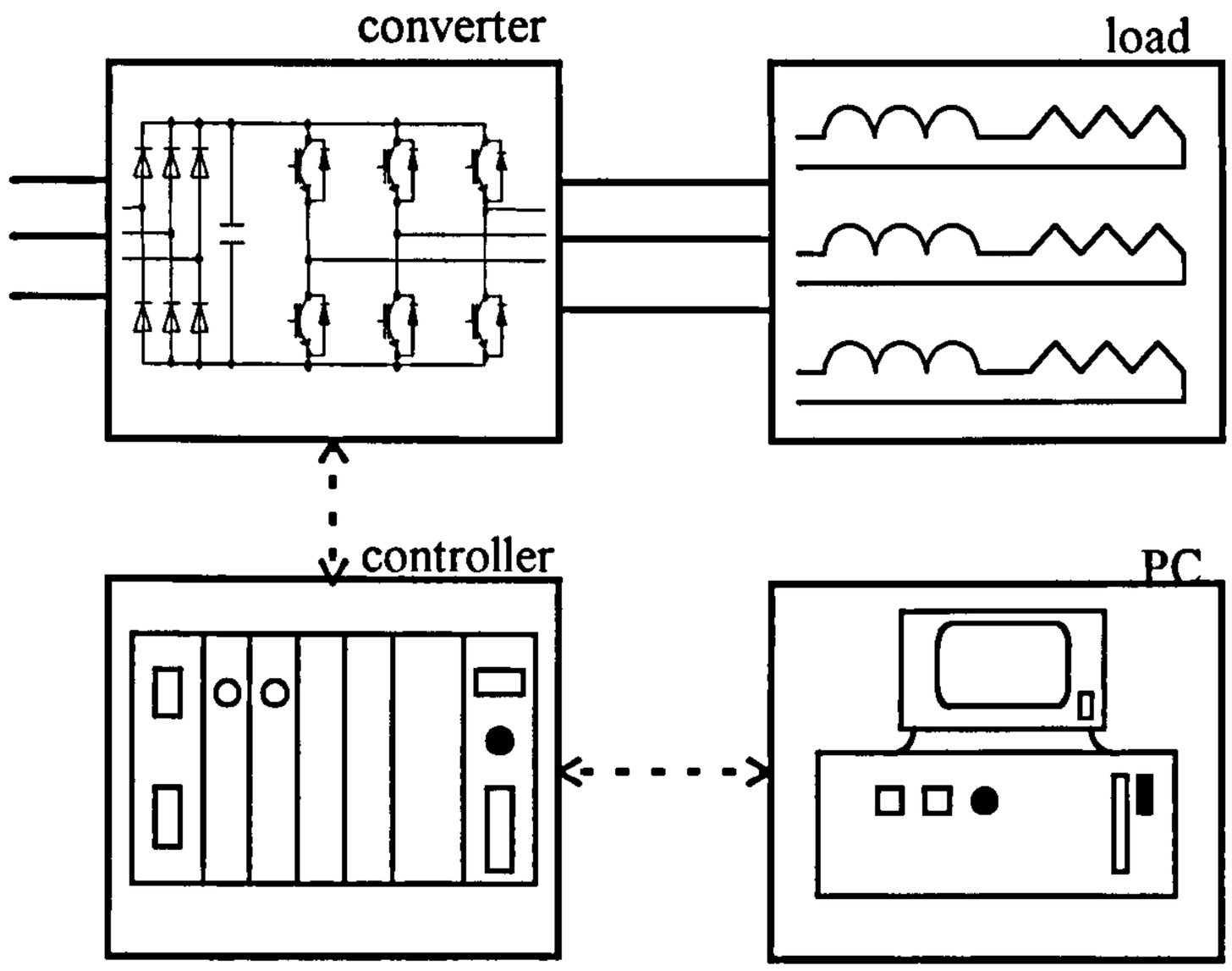


Figure 6.1.1: Arrangement of the converter test circuit

6.2 Power Converters

A 20kW hardswitching converter and a 20kW ACPI converter have been developed for comparative study. Figure 6.2.1 shows the general set-up of both converters. Each converter has four main elements; the input rectifier, dc-link filter, dc-link dump, and the inverter. It was decided to keep the arrangements of the rectifier, dc-link filter and dc-link dump when changing the inverter from the hardswitching configuration to the ACPI.

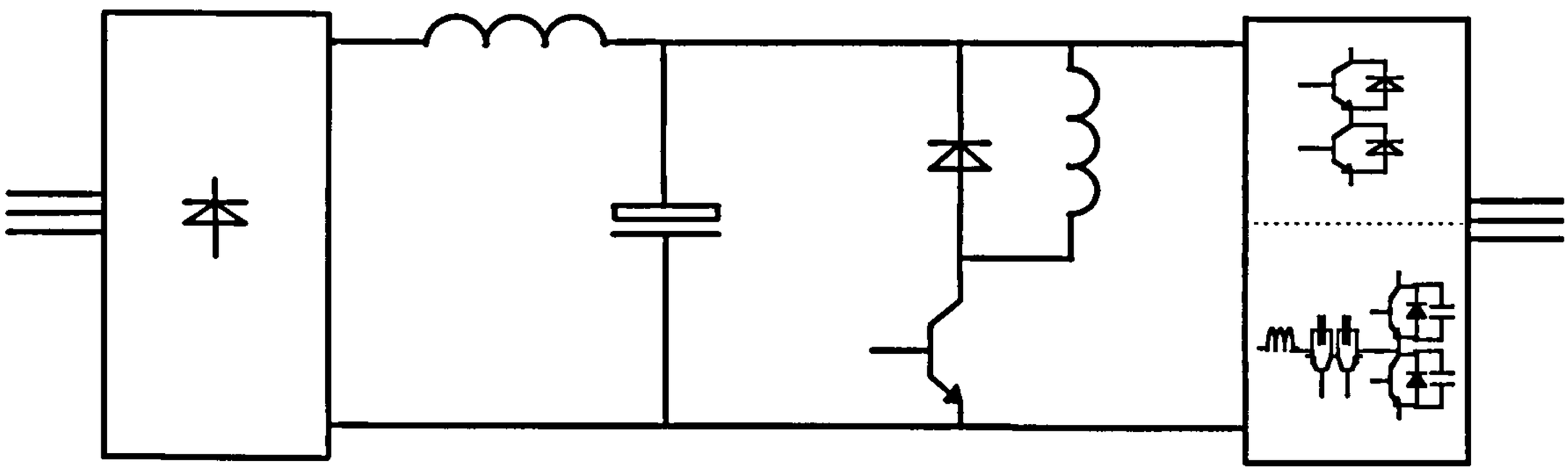


Figure 6.2.1: Converter arrangement

6.2.1 Input side

A simple diode rectifier bridge is used to rectify the three phase supplying dc-link voltage (Figure 6.2.1). The rated input voltage of 415V line to line allows an average dc-link voltage of around 560V. The rated power line current is 30A per phase. The choke

between dc-link capacitor and rectifier limits the inrush-current and in conjunction with the dc-link capacitor and the input line inductance it improves the current form factor. The dc-link capacitor and choke provide the dc-link filter, which reduces the voltage ripple from the output voltage of the rectifier. The main functions of the dc-link capacitor are to act as a energy storage reservoir, and to present a low supply impedance to the inverter bridge.

When connecting the converter with a motor a reverse power flow takes place when the motor acts as a generator or during the braking mode. With a diode bridge rectifier this energy can not be transferred into the main power supply. Thus energy has to be dumped into a resistor. This function is taken from the dump circuit. A hysteresis controller determines when to switch on or off the dump IGBT depending on the dc-link voltage level. However because of the inductor-resistor load bank reverse power flow can not be generated and the dump driver would never be active. Nevertheless it was decided to implement a dump circuit to allow induction motor drives for later research work in drives performance.

6.2.2 Output side

Hardswitching:

The load bank is connected to the poles of the inverter. Each pole includes one upper and one lower IGBT with anti-parallel diodes representing two switches (upper switch MS1 and lower switch MS2). For every pole low-saturation IGBT modules, including two switches from Toshiba with rated values of 1200V and 150A, have been used (MG150Q2YS11). The decision to use these Toshiba modules results in compromising between cost and performance. From the viewpoint of performance the device MG150Q2YS11 promises improved switching losses under zero-voltage conditions, because of its relative short and small tail currents. The device is manufactured from an epitaxial silicon structure that includes a small buffer layer doped with life time killers. That results in short and small tail currents [6.1]. Compared with homogeneous silicon structured devices such as the device BSM150GB123D from Siemens power loss reduction shows no strong improvement under zero-voltage switching [6.1]. In addition the Toshiba module is on average in price compared to its competitors (SEMIKRON SKM150GB123D: £247, Toshiba MG150Q2YS11: £173, Siemens BSM150GB120DN2: £135; all rated at 150A/1200V). The PT-IGBTs are controlled by the driver module IHD680AN from Concept. This driver allows isolation between low voltage side and high voltage side, voltage saturation protection and +/- 8A gate current. The hardswitching inverter was tested up to 20kW with a maximum frequency of 20kHz.

A sinusoidal PWM control scheme was implemented in the controller with a maximum modulation index of 1. The robust IGBTs made the use of snubber circuits unnecessary.

ACPI:

Each pole uses the same IGBT modules and drivers as used in the hardswitching inverter. The additional auxiliary path includes two ultra fast IGBT modules from International Rectifier (IRGPC50KD2) driven by IHD680AN Concept drivers (AS_1 and AS_2 in Figure 6.2.2). The IR modules are very fast in turning on and turning off. The maximum impulse current is 100A. This value is needed when the resonant peak current ramps up to around 80A at maximum load current. Alternative topologies are possible for implementing the auxiliary switch. Reference [6.2] discusses the use of one switch combined with four diodes in a bridge configuration (Figure 4.1 in Chapter 4). Although saving on one active device driver, this solution needs a current detection circuit to ensure turn-off at zero current during the resonant mode. The zero-current switching operation of the auxiliary switches permits the use of thyristor like devices. References [6.3 and 6.4] use MCTs whilst [6.5] uses two antiparallel thyristors. At present, MCTs are limited in their current handling capability and available thyristors have long recovery times. For these reasons individual IGBT co-packs, including ultra fast antiparallel diodes were utilised. The size of the resonant inductor and resonant capacitors depends on overall efficiency demands, PWM controllability and output spectral performance. During test runs a resonant inductor of 5.7µH was used in combination with two values of capacitance (20nF and 67nF) for comparative purposes. A detailed discussion on how resonant inductor and resonant capacitor influence the performance of the ACPI is given in Appendix C and Chapter 7. A more detailed discussion of auxiliary switches in this topology is given in reference [6.2].

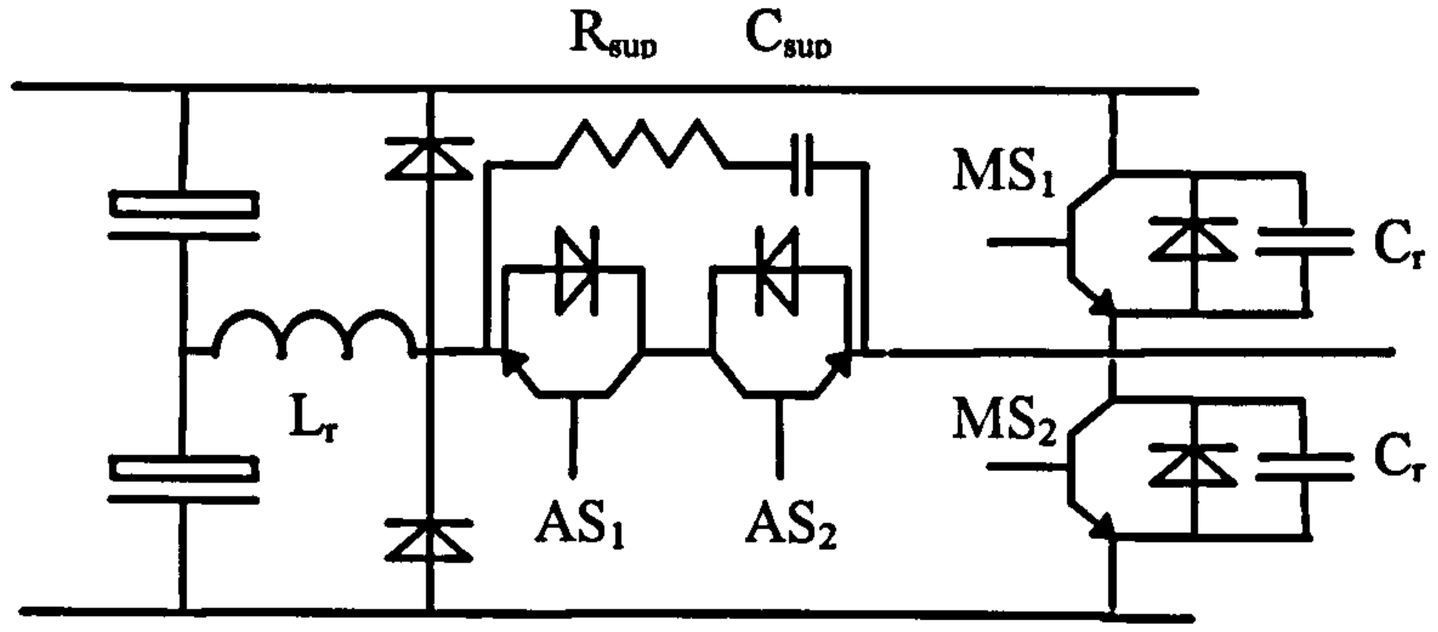


Figure 6.2.2: Pole of the ACPI

Besides the discussed switches and passive components the ACPI need further additional components. Two free-wheeling diodes are needed to allow to turn-off the auxiliary devices at any time even when still carrying the resonant current. In this case the diodes clamp the potential to the upper or lower rail, and provide a current path for the stored

current in the inductor. Thus the inverter can be turned off at any switching status without damaging the auxiliary devices. The RC combination in parallel to the auxiliary switches is needed to suppress voltage oscillation across the auxiliary devices during turn-off. Once the conducting auxiliary device turns off resonance occurs between the junction-capacitance of the diode and the inductor. The values of resistor R_{sup} and capacitor C_{sup} can be calculated from the following equations:

$$\frac{V_{dc}}{2} = I_{r,max} * R_{sup} \tag{6.2.1}$$

$$\frac{V_{dc}}{2} = I_{r,max} * Z_0 = I_{r,max} * \sqrt{\frac{L_r}{C_{sup}}} \tag{6.2.2}$$

$$P_{sup} = 0.5 * L_r * I_{r,max}^2 * f_{s,aux} + C * \left(\frac{V_{dc}}{2}\right)^2 * f_{s,aux} \tag{6.2.3}$$

$I_{r,max}$ is the maximum reverse recovery current, P_{sup} the power losses in the resistor and $f_{s,aux}$ the switching frequency of the auxiliary circuit.

Figure 6.2.3 shows the voltage oscillation across the auxiliary devices during turn-off device AS2 without any RC-snubber.

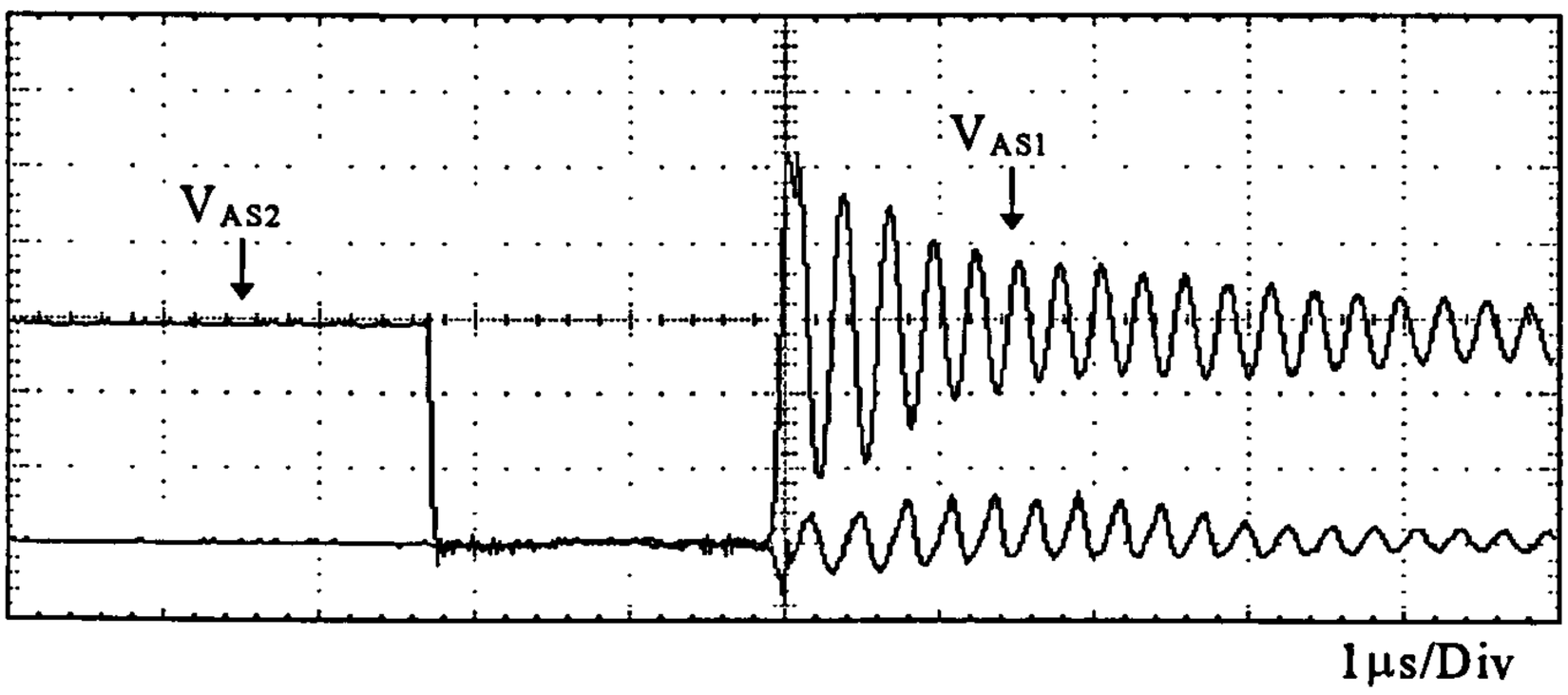


Figure 6.2.3: Voltage oscillation across the auxiliary devices during turn-off process without RC snubber

Figure 6.2.4 shows the turn-off performance using the snubber R_{sup}=39Ω, C_{sup}=10nF. The picture shows a strong reduction of the oscillation. Under consideration of a maximum reverse recovery current of $I_{r,max}$=20A and a frequency of the auxiliary circuit of $f_{s,aux}$=20kHz, equation 6.2.3 leads to losses at P_{sup} =15.68W. These losses are far too high.

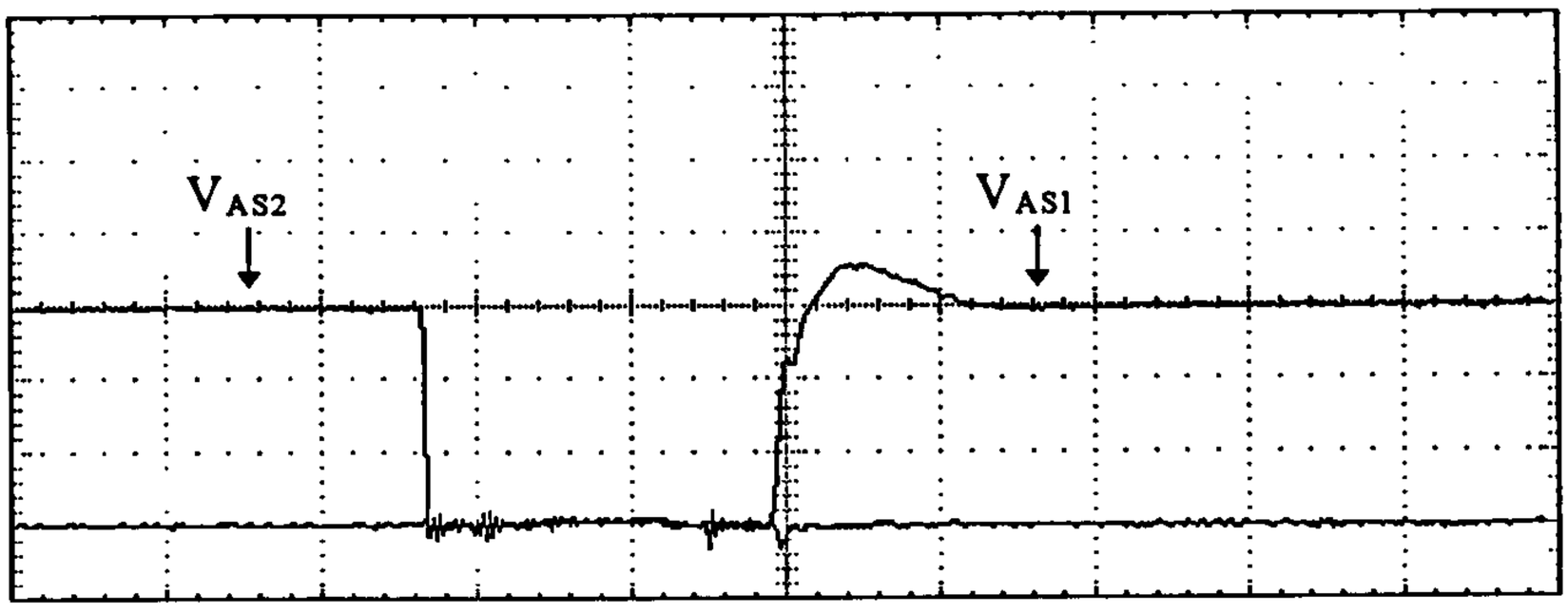


Figure 6.2.4: Reduced voltage oscillation across the auxiliary devices during turn-off process with RC snubber (R=39Ω, C=10nF)

A decrease in capacitance leads to less voltage peak reduction but lower losses. The snubber R=100Ω, C=1nF was seen to satisfy both voltage overshoot and losses (P_{sup}=1.57W, Figure 6.2.5).

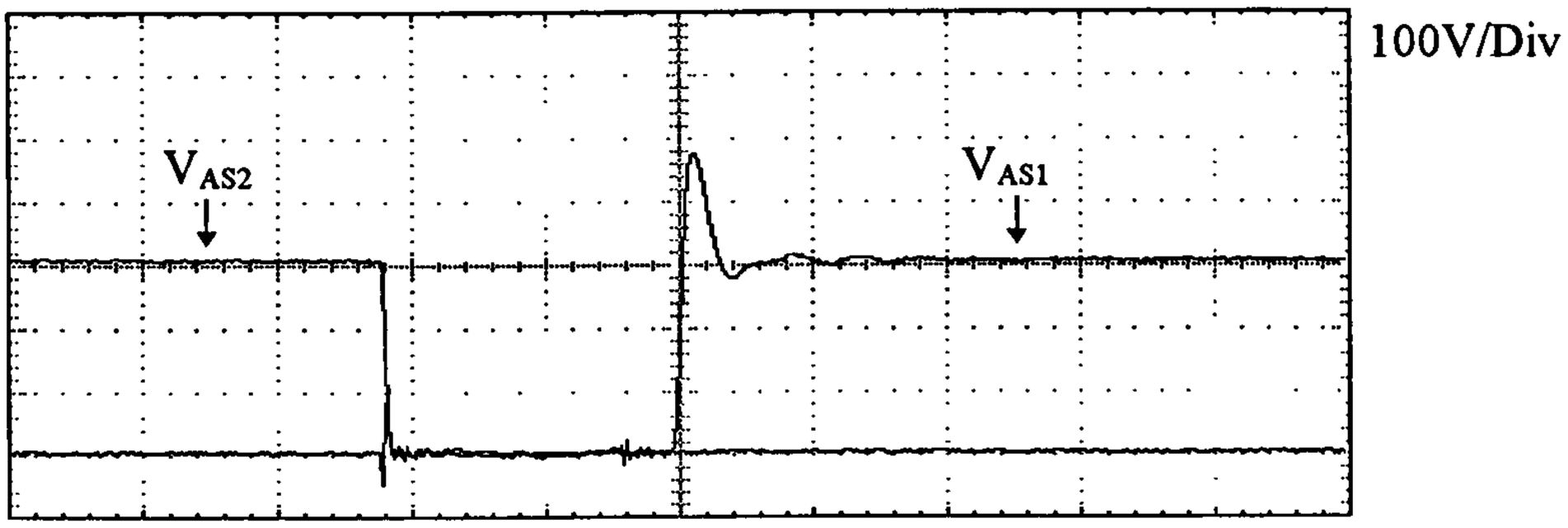


Figure 6.2.5: Reduced voltage oscillation across the auxiliary devices during turn-off process with RC snubber (R=100Ω, C=1nF)

6.2.3 Control of the ACPI -- Terminology and Definitions

So far only a few control schemes have been published describing the control of the ACPI. A discussion of these schemes follows in the next section, but for better understandings the terms: on-state time, current ramp-up mode and current ramp-down mode (section 4.2.2) are new defined. From now on the on-state time is called state-time. The current ramp-up modes B and C (Figure 4.2.15) are summarised to one mode and described as ramp-mode. The same applies to the ramp-down modes E and F that are also called ramp mode. Modes H and J (Figure 4.2.19) are called boost mode respectively. Figure 6.2.6 shows again Figure 4.2.15 and Figure 4.2.19 but includes the new terminology.

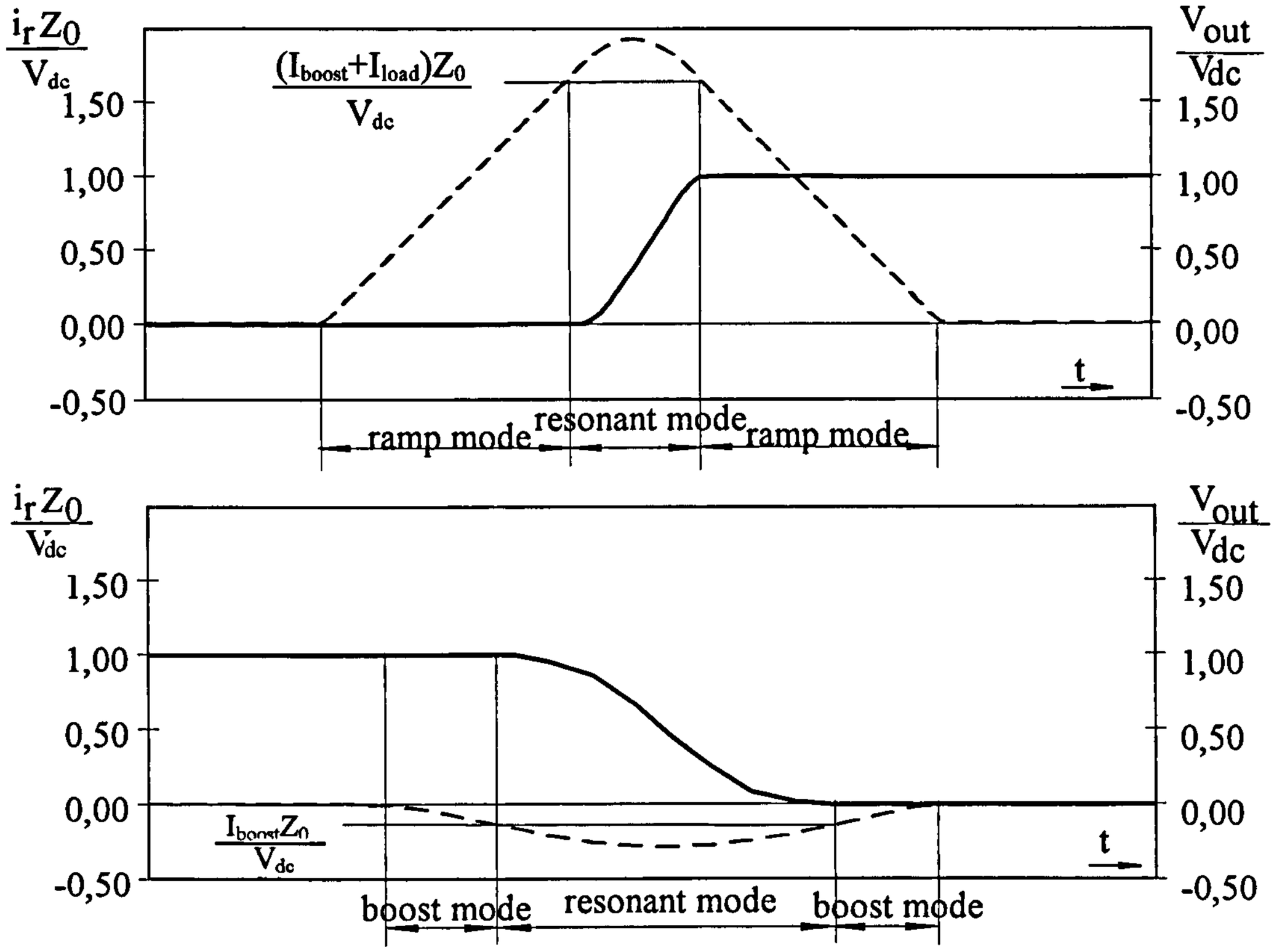


Figure 6.2.6: Switching waveforms of the ACPI (upper waveform Diode-IGBT commutation, lower waveform IGBT-Diode commutation)

The decision if boost mode or ramp mode applies is a function of load current level, its direction and the applied switching status (Table 6.2.1).

CONVERTER STATUS	BOOST MODE	RAMP MODE
I_{load}>0A ⊕ IGBT of MS_1 conducts	yes	no
I_{load}<0A ⊕ IGBT of MS_2 conducts	yes	no
I_{load}>0A ⊕ Diode of MS_2 conducts ⊕ I_{load}<I_{th}	yes	no
I_{load}<0A ⊕ Diode of MS_1 conducts ⊕ I_{load}>-I_{th}	yes	no
I_{load}>0A ⊕ Diode of MS_2 conducts ⊕ I_{load}>I_{th}	no	yes
I_{load}>0A ⊕ Diode of MS_2 conducts ⊕ I_{load}<-I_{th}	no	yes

Table 6.2.1: Converter stati that determine if the boost mode or the ramp mode is applied (I_{th} represents the threshold current level: $I_{th}=I_{boost}+I_{load}$ or $I_{th}=I_{boost}$)

6.2.4 Control of the ACPI – State of the Art

Reference [6.3] controls the ACPI by monitoring the current flow through every main switching device. Every diode and every IGBT has its own current sensor to detect if the device is conducting. Thus twelve sensors monitor the current flow through all main devices. Besides these sensors the ACPI is equipped with six additional current transducers and eight voltage transducers. Three current transducers are inserted into the auxiliary paths detecting zero current, the other three current sensors monitor the three phase currents. Six voltage transducers detect zero-volts across the six main devices, one voltage transducer measures the midpoint voltage and another voltage transducer the dc-link voltage. Reference [6.4] reduces the number of sensors. It eliminates the current sensor in the auxiliary path by a mixed analogue/digital controller which calculates the resonant current by integration. In addition reference [6.4] makes use of the inherent repeating switching status applied on the ACPI as shown in Figure 6.2.6 Reference [6.4] implemented a switching pattern following the switching status in a logic hardware configuration. The state time is calculated by a mixture of analogue/digital hardware using integrators and logic components. The number of sensors in reference [6.4] is reduced to current transducers for all three phases, zero-voltage detection sensors for each main device and a voltage transducer for dc-link voltage measurement. Reference [6.2] uses a completely digital solution of controlling the ACPI. The idea is to implement the switching pattern in a FPGA instead of using an analogue and digital circuitry. This state machine is connected to an EPROM. The EPROM is a look-up table for the FPGA. Once the FPGA applies a new switching pattern it reads the state time from the EPROM. The EPROM is fed with the latest update on the load current levels and the dc-link voltage. This information is used to select the right state time for the FPGA. However inserting an EPROM has two limitations: 1) When storing the information in an EPROM the information must be measured first for each pole and under all load conditions. Thus test runs of the ACPI are necessary or values must be calculated leading to less precision; 2) the fixed data in the EPROM allows limited flexibility during operation mode. The number of used sensors of the ACPI in reference [6.2] still remains the same as in reference [6.4] but works without any analogue integrators, which are known for off-set and drift problems. Also reference [6.2] modified the zero-voltage detection circuit from reference [6.4]. Instead of using a voltage divider with a comparator and reference voltage, reference [6.2] uses the gate drive of the driver circuit to detect zero voltage across the switching device. This information is feedback into the gate driver circuit that includes a second state machine for short circuit protection and start-up. Figure 6.2.7 shows the different control schemes.

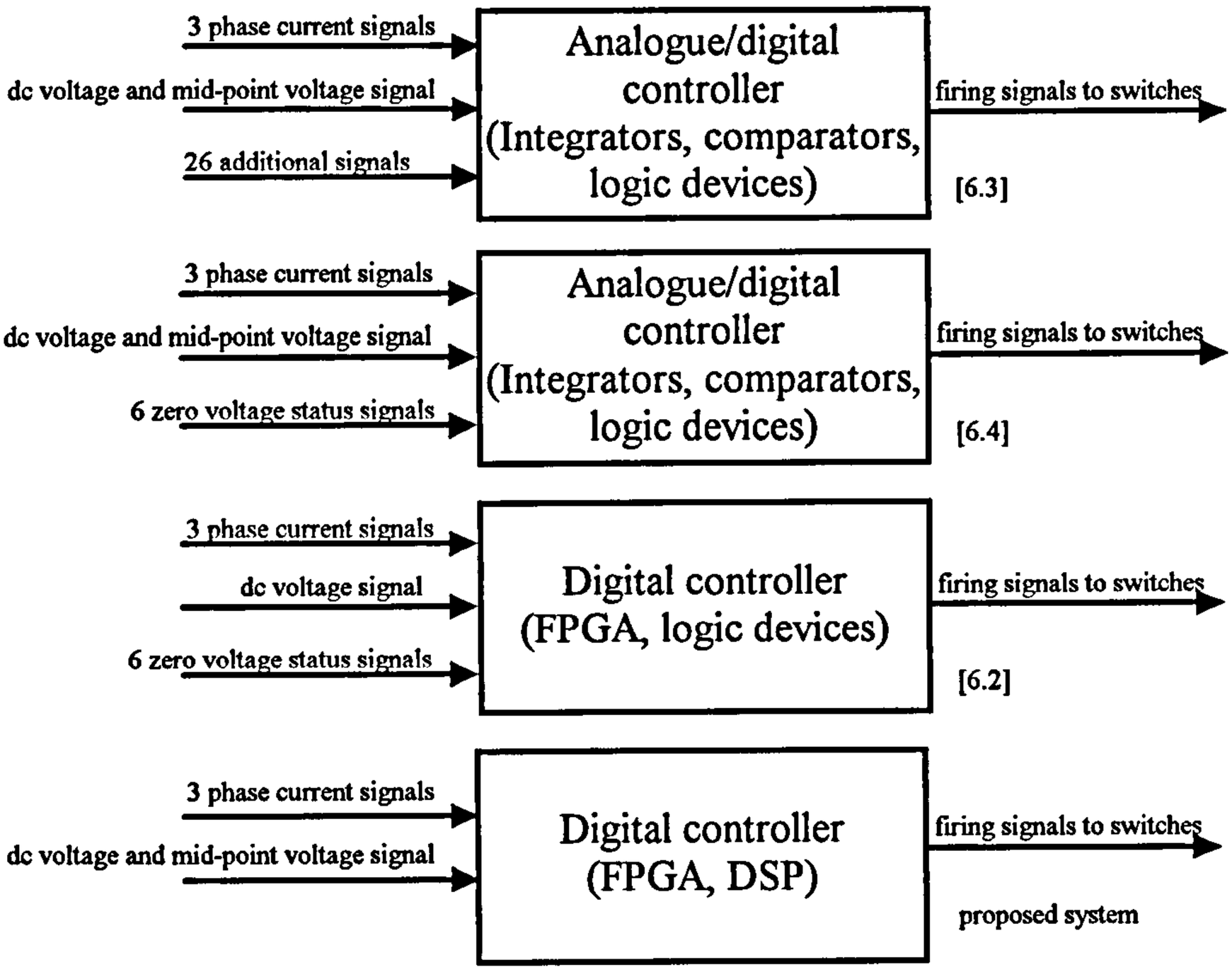


Figure 6.2.7: Control of the ACPI—State of the art

6.2.5 Proposed sensorless control of the ACPI

The proposed control scheme reduces the number of sensors and increases the accuracy of state time by on-line mathematically processing of the measured values for any load currents using a DSP chip. Cycle by cycle calculations are performed in a DSP to determine the optimum switching instants for both auxiliary and main devices without the need of an additional current sensor in the auxiliary path or monitoring the voltage across the main devices. Only the load current level and its direction have to be monitored. This information is taken from the phase current sensors that are already implemented in a conventional hardswitching converter drive system.

Figure 6.2.6 shows that during one commutation three state modes apply. The length of the state time is a function of various parameters that are discussed in the following example.

Assuming the load current is positive and diode of switch M_{S2} is conducting (Figure 6.2.2).

Status: $AS2_2${on}

To activate the resonant mode, one of the auxiliary devices is turned on first. The control signal that commands turn-on of the auxiliary device is generated from the PWM

controller (in our example the controller demands to turn-on the auxiliary switch AS_2). The status $AS_2\{on\}$ remains for a certain amount of time until the next status $MS_2\{off\}$ applies. The time between the different stati is a function of the direction of the load current and magnitude. In our example we assume that the load current is positive and therefore we call the state time t_{DIp} (DIp: commutation from Diode to IGBT under positive load current). The state time t_{DIp} applies until the inductor current reaches a defined threshold level. The threshold value can be mathematically expressed shown in Figure 6.2.6. Regrettably the measurements of the inductor current at the required speed is not acceptable, because there are no inexpensive standard components on the market. Thus the threshold level must be calculated. (A shunt as on-line measurement, may cause trouble since the whole control interface should be isolated from the power circuit).

An estimation needs the required data of the resonant inductance, dc-link voltage and the mid-point voltage. With these data the current in the resonant inductor can be expressed to:

$$i_r = \frac{1}{L_r}\int \Delta v dt \qquad (6.2.4)$$

$$\Delta v = V_{dc} - V_{mid} \qquad (6.2.5)$$

with Δv is the applied voltage across the resonant inductor. The dc-link voltage and midpoint voltage can be simply measured using voltage dividers.

Status: $MS_2\{off\}$

The DSP calculates the required state-time and sends a control signal to turn-off switch MS_2. This is precisely the time when the current reaches its defined level. The turn-off of the main device results in voltage resonance across both main switches. In our example the voltage across device MS_1 resonates towards zero, whereas the voltage across MS_2 resonates towards the dc-link voltage. Both reference [6.4] and reference [6.2], use zero-voltage detection circuits. The main IGBT turns on only when the measured voltage across the device is zero and an 'okay' signal from the controller reaches the IGBT driver. The 'okay' signal is calculated using equation:

$$t_r = \pi\sqrt{2L_rC_r} \qquad (6.2.6)$$

t_r is defined as time, where mathematically the voltage across the device MS_1 is zero. Appendix C shows that the influence of internal small resistance on the resonant time is negligible and variation in inductance and capacitance with temperature rise tolerable.

However the statement that the voltage reaches zero after time t_r collapses is only true at zero load condition. A change in the load results consequently in change of the voltage waveform. The voltage waveform can be expressed as (Appendix C):

$$V_{Diode-IGBT}(t) = \frac{V_{dc}}{2}(1-\cos\omega_0 t) + I_{boost} Z_0 \sin\omega_0 \quad (6.2.7)$$

$$V_{IGBT-Diode}(t) = V_{Diode-IGBT}(t) + I_{load} Z_o \sin\omega_0 t \quad (6.2.8)$$

where resonant impedance Z_0 and resonance frequency ω_0 are given in equations 4.2.54 and 4.2.53. It shows that the waveforms are a function of the load current and boost current. This relation is used in the proposed control scheme.

Figure 6.2.8 shows the theoretical voltage waveform under light load conditions and Figure 6.2.9 under high load conditions (with the values 5.7μH and 20nF) using equations (6.2.7 and 6.2.8).

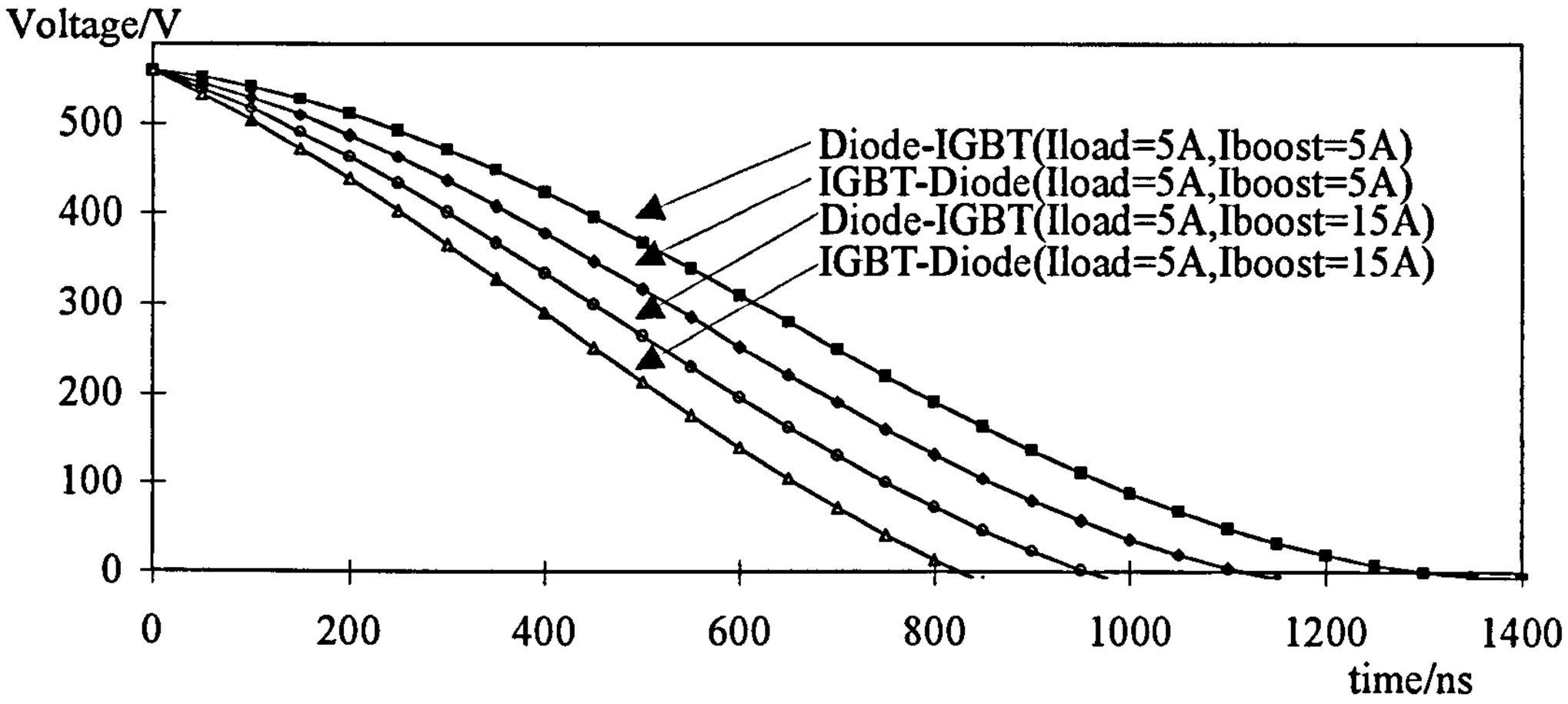


Figure 6.2.8: Voltage across IGBT vs. time at light load

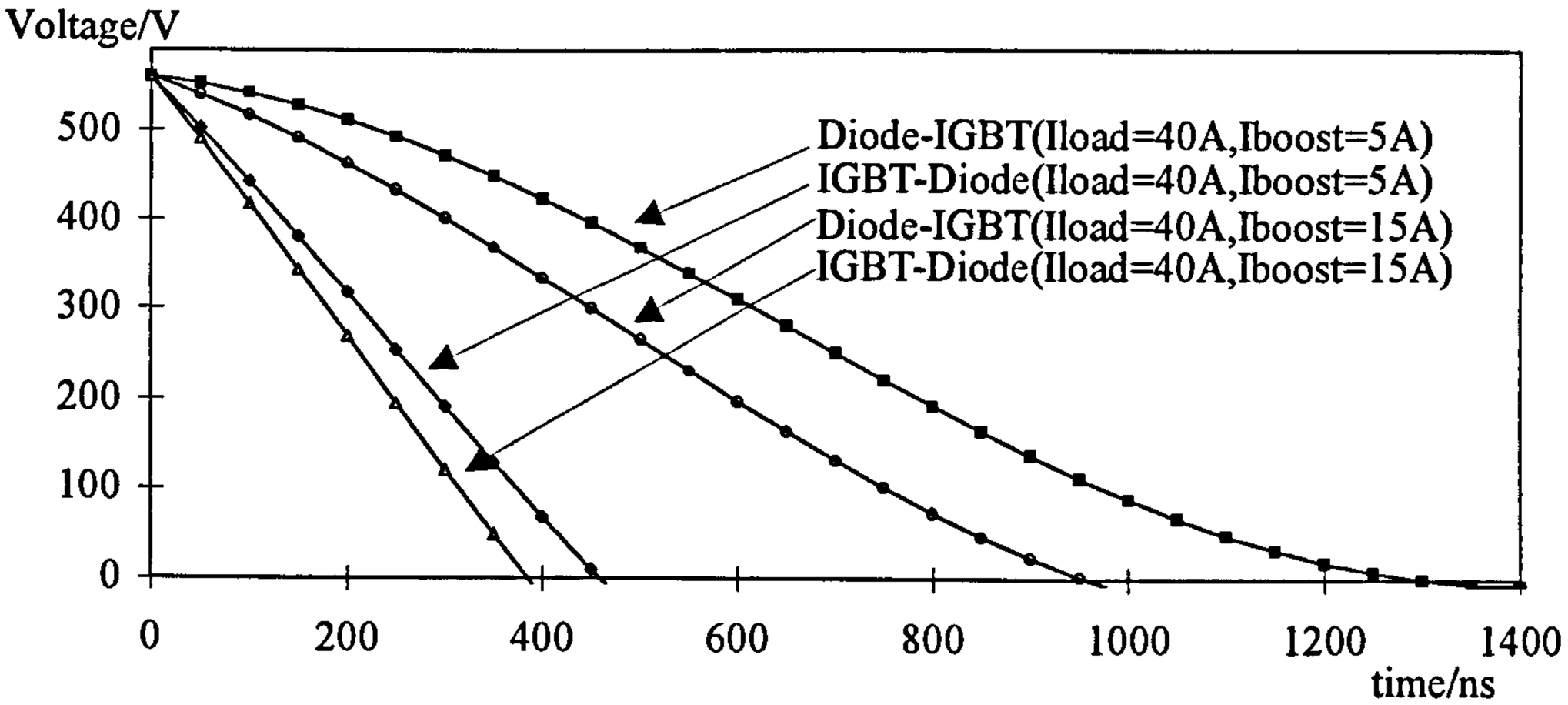


Figure 6.2.9: Voltage across IGBT vs. Time at high load

Once the voltage reaches zero the antiparallel diode starts conducting. During this time the IGBT (in our example MS_1) must turn-on allowing softswitching. The commutation process IGBT-Diode is from less interest, because the diode still conducts once the commutation process has completed (diode picks up the load current). Thus the

controller must take care only not to turn-on the IGBT too early. At the worst case scenario (boost current of 15A and maximum load current of 40A) the earliest turn-on impulse is 400ns (Figure 6.2.9). This is easy to implement in a DSP controller. During the commutation Diode-IGBT the timing of the firing impulse must be set with more accuracy. That is, because the diode conducts only for long where the voltage is zero (Figure 6.2.8 and 6.2.9). Consequently a longer 'zero' time increases the chance of successful softswitching during the turn-on process.

Figure 6.2.8 and Figure 6.2.9 show clearly that with a higher boost current (15A) the conduction time of the diode is longer compared to the conduction time using a 5A boost current even under all load conditions (note, the times where the voltage waveforms crosses the time axis and 1400ns is equal the diode conduction time). Care must be taken when increasing the boost level to a very high value. Firstly the losses in the auxiliary circuit increases and secondly the dv/dt stress across the main devices increases (Figure 6.2.9). It was seen that 15A boost current satisfy both having a relative long diode conduction time and small losses in the auxiliary path (Appendix C). With a 15A boost current a state time t_{reso} of 1.2µs can be used without losing any zero-voltage switching performances under all load conditions.

Note, that Figure 6.2.8 and Figure 6.2.9 show an instantaneous turn-off process of the IGBT MS_2. With the flexibility of a DSP controller the turn-off delay can be included when changing the offset of the variable. In addition other time delays can be taken into account such as time delay between controller and driver or propagation delay time of the driver.

Status: MS_1{on}

Once the main IGBT turns on (after 1.2µs), the current in the resonant inductor decreases linearly until it reaches zero. Again sensorless control is applied to turn off the auxiliary switch (our example AS_2). That is because during the commutation process of the pole the current in the auxiliary circuit is flowing in one direction only, but the applied voltage across the diode changes with the commutation. Thus the conducting auxiliary diode gets reversed biased and stops the current flow in the opposite direction.

Status: AS_2{off}

With AS_2 off the circuit remains in the steady-state mode until the PWM controller demands a new change in the pole.

The four discussed switching stati can be summarised to one switching sequence (sequence 1 in Figure 6.2.10). The same applies for the commutation process IGBT-Diode (Figure 6.2.10).

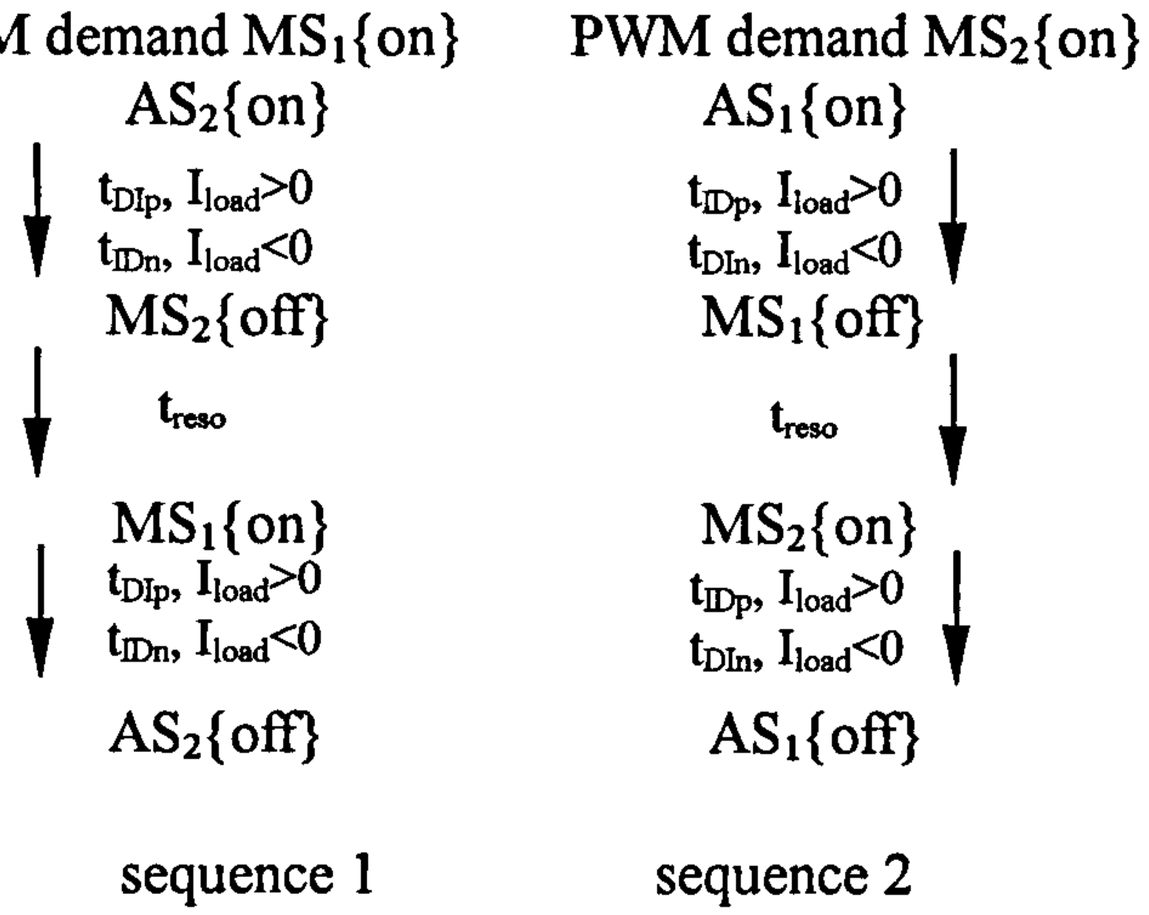


Figure 6.2.10: Switching stati of one pole at different load conditions

The state time of each switching state is a function of the load current, the dc-link voltage and the midpoint voltage (except for the resonant mode). These times can be calculated to (equations 6.2.9 to 6.2.13):

IGBT-Diode, positive load current

$$t_{IDp} = \frac{L_r\left(-I_{boost}\right)}{-\left(V_{dc} - V_{mid}\right)} \tag{6.2.9}$$

IGBT-Diode, negative load current

$$t_{IDn} = \frac{L_r I_{boost}}{V_{mid}} \tag{6.2.10}$$

Diode-IGBT, positive load current

$$t_{DIp} = \frac{L_r\left(I_{load} + I_{boost}\right)}{V_{mid}} \tag{6.2.11}$$

Diode-IGBT, negative load current

$$t_{DIn} = \frac{L_r\left(-I_{load} - I_{boost}\right)}{-\left(V_{dc} - V_{mid}\right)} \tag{6.2.12}$$

resonant mode is set to:

$$t_{reso} = 1{,}2\,\mu s \tag{6.2.13}$$

Knowing the sequence and the direction of the load current the DSP uses always the right equation and calculates the different state times.

It has to make sure, that long lifetime and temperature variation do not effect the results of the calculations. This is discussed in the following section.

6.2.6 Performance of Novel Control Scheme vs. Parameter Variations

When calculating the state time, one has to be certain that temperature variation will not affect the performance of the sensorless control scheme. For example changes in temperature will affect component values and semiconductor parameters such as switching times.

The ramp mode and the boost mode can be described with similar equations thus the effect of parameter changes is the same. The effect of change of the inductance value during temperature rise can be expressed with the introduction of the overall temperature coefficient of the core given in data books. Using an iron powder core two individual temperature coefficients have to be considered. Firstly the temperature coefficient of the core permeability and secondly the temperature coefficient of the percent permeability versus both dc magnetising force and peak AC flux densities ranges [6.6]. With both values given from the manufacturer the state time can be plotted against temperature rise with the help of equation 6.2.4. Figure 6.2.11 shows the time vs. temperature change for the ramp mode and boost mode under worst-case conditions.

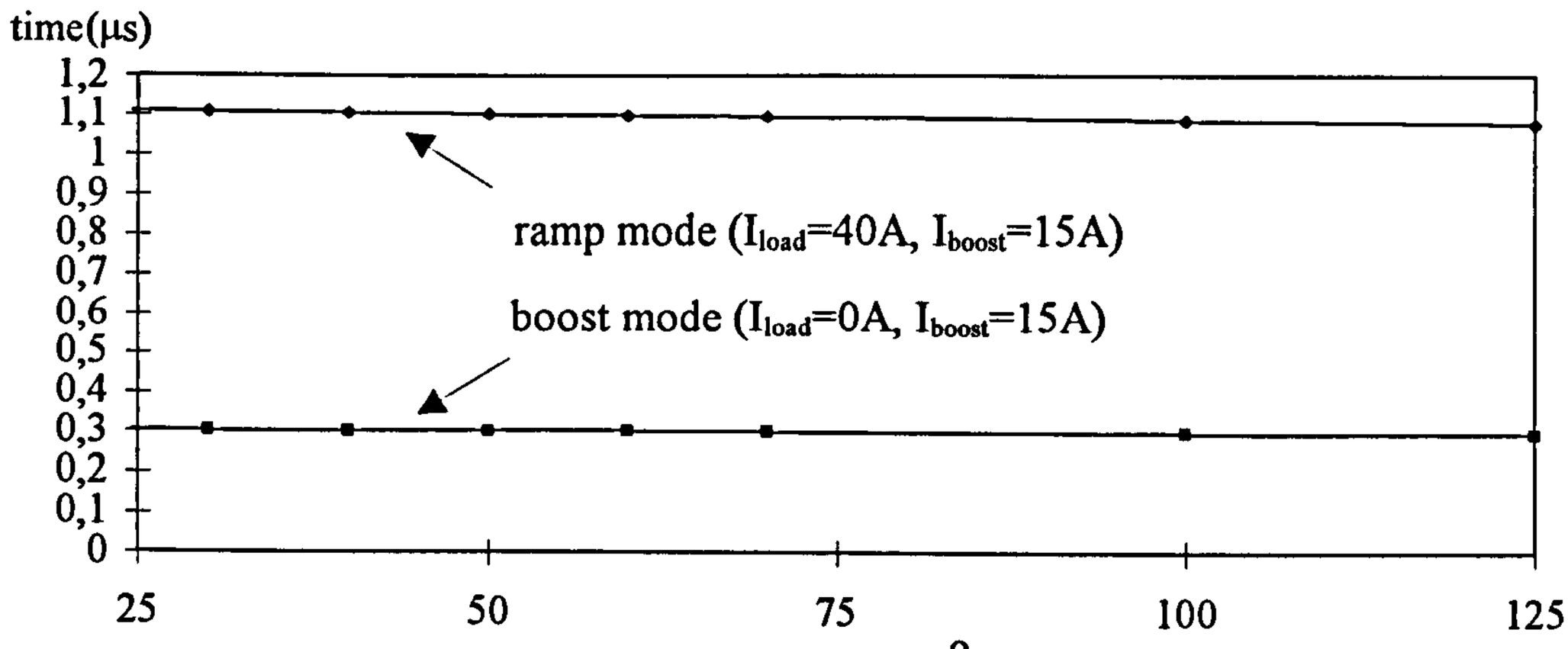


Figure 6.2.11: On-state time vs. temperature at different operation modes

With Figure 6.2.11 one can conclude that the error of the state time of ramp mode and boost mode is negligible. The same statement applies by change of value of the inductance during lifetime [6.4].

During the resonant mode the resonant time is only minor effected from change in temperature. Appendix C shows that the influence of internal small resistance on the resonant time is negligible and variation in inductance and capacitance with temperature rise tolerable.

6.2.7 Set Up of the Sensorless Controller

The sequences with their individual switching stati are stored in an FPGA. A DSP communicates with a FPGA in which a sinusoidal PWM generator is implemented. The DSP calculates the actual state time for every switching status and sends the information to the FPGA. Thus it is important to keep the sequences in an order, because a wrong state time send to the FPGA would change the complete time scaling of both sequences. To do so, the interrupt that is responsible for the synchronisation of the controller system is used to synchronise the data transfer from DSP to FPGA. The maximum voltage of the triangle waveform is used to generate the interrupt signal (Figure 6.2.12). Once an interrupt occurs the DSP reads the actual phase currents, dc-link voltage and midpoint voltage. The DSP then calculates all needed time demands t_{DIp}, $t_{\Pi Dp}$ etc. in readiness for the resonant commutations 'sequence 1' and 'sequence 2'. In addition, it calculates the usual voltage and frequency demands determined by the control structure of the drive. At the end of the interrupt routine all calculated data are fed into the FPGA.

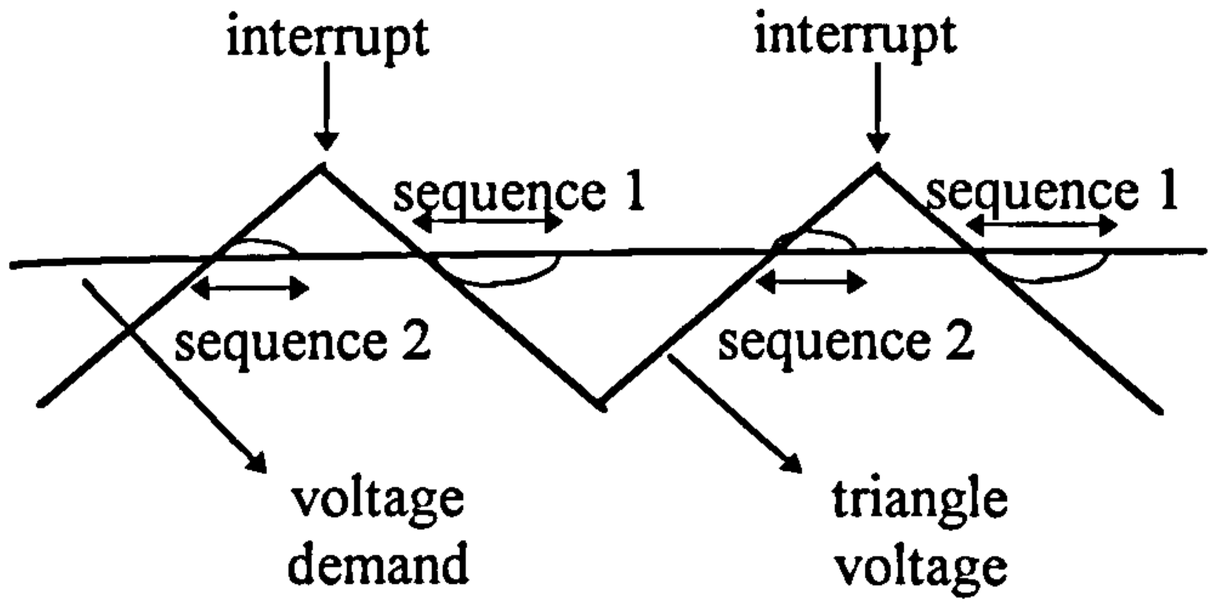
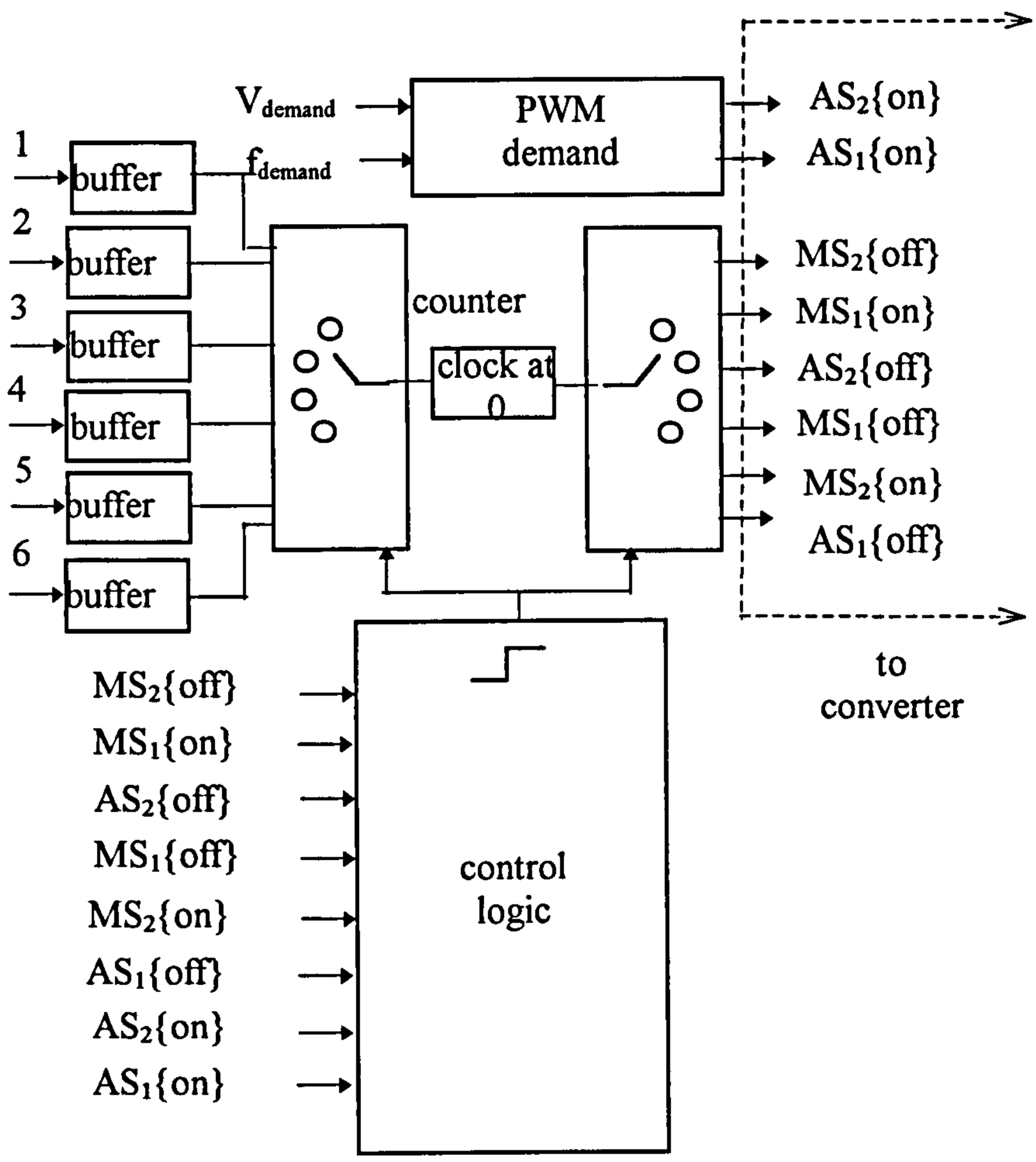


Figure 6.2.12: Order of sequences and interrupts

The FPGA (Figure 6.2.13) includes counters, multiplexers and logic gates. The data which carries the information of state times is stored in buffers. Voltage demand V_{demand} and frequency demand f_{demand} is also fed into the FPGA. From both values the FPGA generates the PWM pattern with its programmed sinusoidal PWM generator and the interrupt signal. The information is applied to one of the auxiliary switches and to the internal logic block. The logic block triggers a pre-set input selector. The input selector is only a channel to let the selected state time through a down counter. The down counter counts continuously with a frequency of 20MHz. Once the counter reaches zero

it feeds this information back to the control logic block that commands a new trigger signal to the input selector. In addition the converter triggers an output selector that commands the turn-on or tun off of one of the devices of one pole of the ACPI.



current direction	1	2	3	4	5	6
$I_{load}>0$	t_{DIp}	t_{reso}	t_{DIp}	t_{IDp}	t_{reso}	t_{IDp}
$I_{load}<0$	t_{IDn}	t_{reso}	t_{IDn}	t_{DIn}	t_{reso}	t_{DIn}

Figure 6.2.13: Simplified circuit of the FPGA

Using the described set-up the ACPI is sinusoidal PWM controlled and is running at a maximum switching frequency of 10kHz.

6.2.8 Other Circuits

Other circuits associated with the power converters are: a dc-link voltage divider for measurement of the dc-link voltage (the mid-point of the dc-link capacitors is measured

in case of the ACPI); Hall effect current transducer for phase current measurement; power switch gate drives circuit including the driver module IHD680AN; communication systems with the controller; protection circuits; auxiliary power supplies.

The phase current transducer uses a 50A Hall effect device with a bandwidth of DC to 150kHz. Gate drive circuits for the IGBT power switches allow 8A isolated gate pulses to flow into or out of the gate. The gate driver includes voltage saturation protection, provides output pins to indicate a fault and power supply under-voltage lockout. The driver card communicates with the controller via bi-directional transmission lines. Transceivers on the driver and the controller allows interface free transmissions of data. Circuits for safety and protection have been designed. Protection circuits are overvoltage protection and undervoltage protection of the dc-link voltage, overcurrent protection of the output current, input current limitation and over-temperature protection of the IGBTs. The overvoltage prohibits the dc-link voltage to overrate the maximum voltage of the dc-link capacitors. Undervoltage protection eliminates the case of generating an inrush current during a short circuit of the dc-link. Overcurrent protection of the phase current is necessary to exclude the case of slow overheating of the devices or man failure. Current temperature sensors are mounted on heatsinks, monitoring the heatsink temperature. At a maximum of 110°C a fault is recognised to shut down the gate drives and disconnect the rectifier from the supply board. An auxiliary power supply provides power for all individual built-in systems of the converter. The auxiliary power supply is split into two independent voltage sources allowing safe shut down of the complete converter system in case one auxiliary power supply fails.

6.3 Control Electronics

Figure 6.3.1 shows the general arrangement of the control equipment. Most of the control circuits are mounted in a 19'' rack cabinet, with connections to the PC and the power converter.

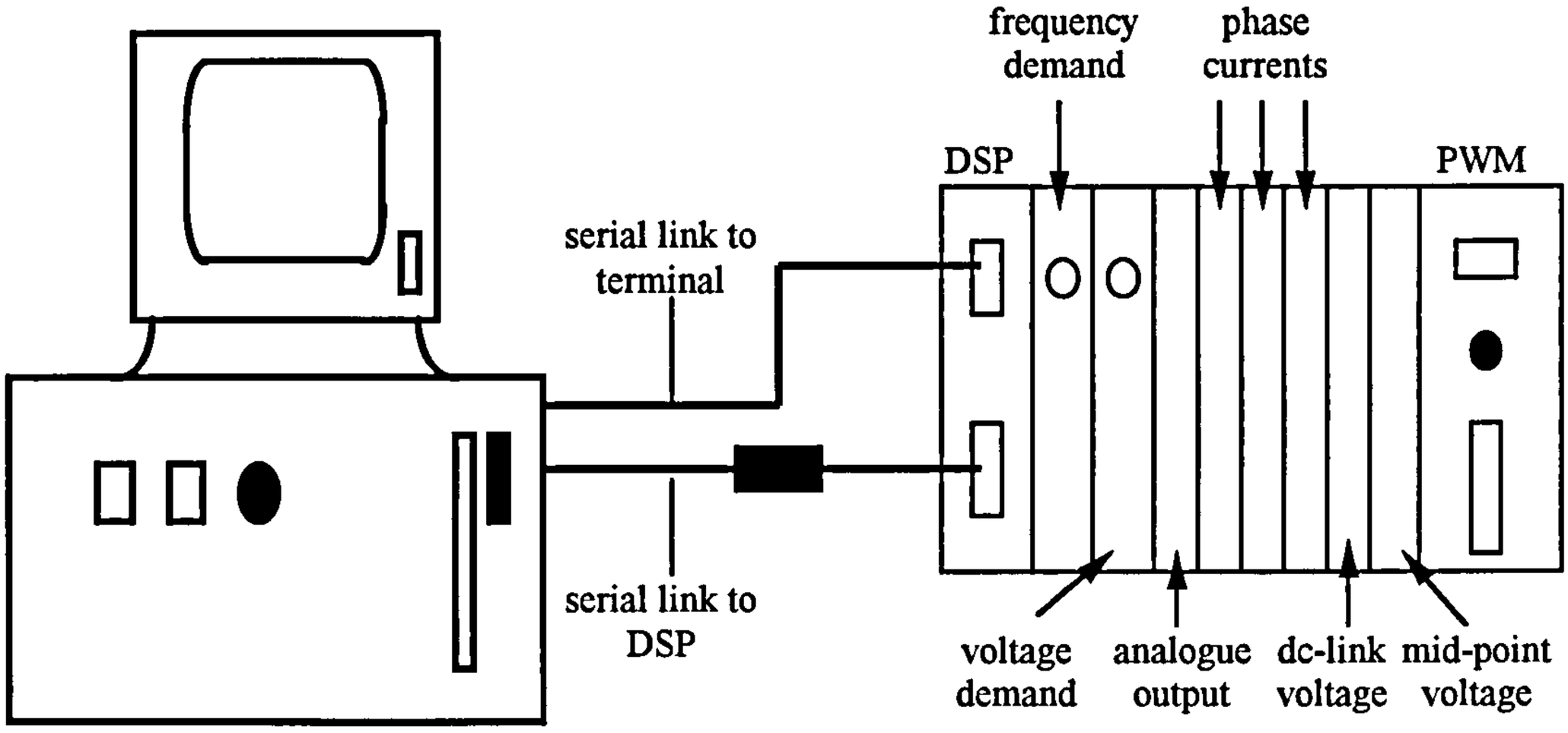


Figure 6.3.1: Arrangement of the controller

In this arrangement the PC acts as a file store and allows programs to be written, compiled, and downloaded to the control electronics. Another serial connection permits the actual values of program variables to be loaded into the PC terminal in quasi-real time.

The rack includes several cards for several functions (Figure 6.3.1 and 6.3.2). The main card is the DSP card based on Texas Instruments TMS320C31 operating at 40MHz. The 32bit floating point DSP has a large address space with extensive addressing capabilities and is able to perform complex mathematical functions quickly and is capable of handling large look-up tables. The TMS320C31 is set around a common backplane, where the DSP control board is the bus master. The following cards are connected to the backplane: one PWM card, seven 10-bit analogue input cards and one 12-bit analogue output card. All cards are isolated from the backplane, hence all cards and the processor can be accessed at the full processor 40 MHz clock speed.

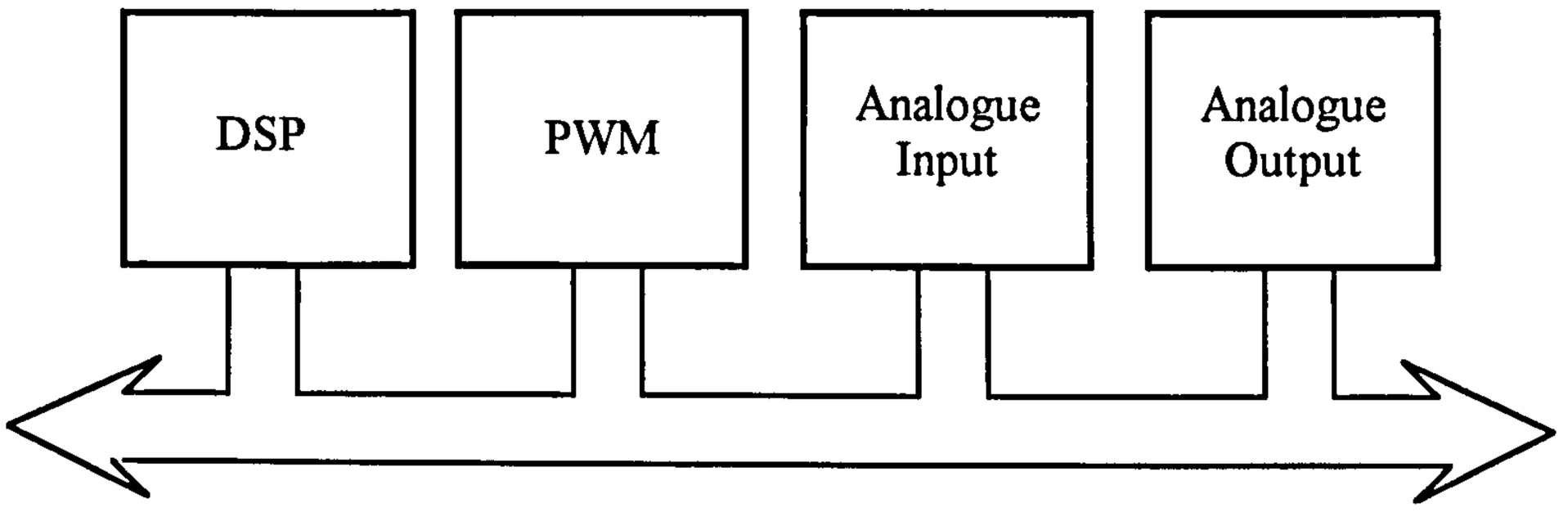


Figure 6.3.2: DSP drive backplane

The phase currents, dc-link voltage and midpoint voltage (using the ACPI) are inputs of the analogue cards. In addition voltage and frequency demands are manually controlled using control pins on the analogue cards.

The PWM card is capable of controlling six pairs of devices independently with PWM frequencies of at least 20kHz. The majority of the work is performed by a XILINX Field Programmable Gate Array (FPGA) which is configured by software held in a PROM at power up. All PWM control parameters are software programmable. These include for example, PWM frequency, dead times when running the hardswitching converter or boost times when running the ACPI. The PWM card holds the master clock of the whole controller and fires synchronised pulses to the DSP card. Besides the components FPGA and PROM other components such as output buffers and opto isolators are also included on the PWM card.

Due to the software basis of the system all measurable and inferred parameters can be output either via an analogue output card for display on scope or via a serial link connected to the computer. This software initialises the processor and enables a memory data buffer to be generated. The data buffer is connected with the DSP on board and enables the controller to communicate with the PC.

The DSP TMS320C31 is programmed in 'C' which enables more complex algorithms and data structures to be implemented with ease. Although implemented in 'C', some assembly language instructions are required for parts of initialisation and interrupt routines.

A software protection was implemented in the 'C' program. The protection monitors demand values for the PWM card. Values leading to a short-through in the pole, overvoltage, undervoltage or overcurrent govern to disable all the inverter power switches.

6.4 Load Configuration

The induction motor and the mechanical load are represented by using inductors and resistors. Figure 6.4.1 shows the load bank for one phase. The load is adjustable allowing to test the converters under various load conditions. The 20mH inductor is tapped at the middle allowing 5mH, 10mH or 20mH output impedance. Using star connection of all three phases the load bank can dissipate 20kW power without any fan-cooling system.

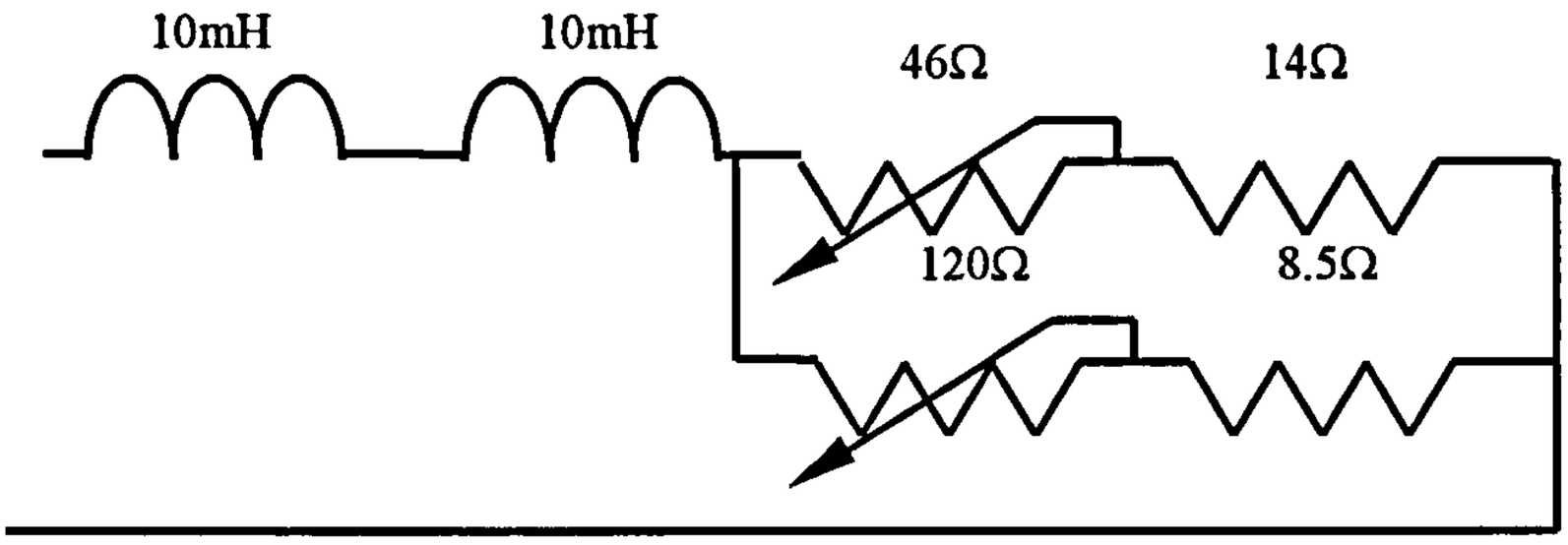


Figure 6.4.1: One phase of the load bank

6.5 Test Equipment

High voltage measurements were performed using differential voltage probes from UNIVERSAL PROBE. Current measurements were carried out using current probe and current amplifier set-ups from Tektronix. All the test equipment was tested, adjusted and offsets were recorded in case the need for later theoretical calculations. Cable lengths between probe and oscilloscope were adjusted to ensure equal propagation delays for both voltage and current measurement set-ups (This is crucial in case of recording losses across devices). Temperature measurements were made using thermocouples. It was made sure that voltage, current and temperature were measured at the same point at the converter when changing converter design from hardswitching to softswitching. In addition tests were only done when the ambient temperature was similar when comparing the temperature performance between hardswitching and ACPI. Measured data were captured with the help of the Tektronix oscilloscope, TDS744 (500Mhz, 2GS/s). In case of measuring losses or voltage output spectra this data has been prepared for Excel and Matlab programs allowing the data to be manipulated for off-set corrections or time delay corrections. Regrettably high accessibility for measurements on the converter results in relatively high stray inductance hence oscillations on the measured waveforms.

Chapter 7

MEASUREMENTS ON ACPI AND HARD SWITCHED CONVERTERS

Chapter 7 describes test results taken from the converters described in Chapter 6. Section 7.1 shows how to dimension the values L_r and C_r and how this affects the performance of the converter and influence current and voltage waveforms. Sections 7.2 to 7.4 show a variety of measured waveforms and results of calculations that have been based on the measurements. In addition, it describes and gives explanations for some phenomena that have been measured. Finally, section 7.5 summarises the results in the form of a table.

7.1 Impact of Resonant Inductor and Resonant Capacitor on ACPI Performances

The values of resonant inductors and resonant capacitors of the ACPI dictate the performances of the topology. The important values that describe the performance are commutation time ($t_{reso}+t_r$), resonant peak current (I_{peak}) and dv/dt stress across the main switches (dv/dt). The commutation time ($t_{reso}+t_r$) is a function of L_r and C_r (equations 4.2.48 and 4.2.53) and includes the resonant time (t_{reso}) and the current rise and current fall time (t_r) during ramp mode and boost mode. It is desirable to set the commutation time as short as possible to reach a high degree of PWM controllability. The resonant peak current (I_{peak}) is also a function of L_r and C_r (equations 4.2.48 and 4.2.54). A low maximum current is preferred to minimise current stress and not to over-dimension the auxiliary switches as that would increase the cost. Both commutation time and resonant peak current, must also be chosen with respect to low losses.

Equation 4.2.51 shows that the dv/dt stress across the main switches is dictated by L_r and C_r. From this equation the resonant time, resonant peak current and dv/dt stress can be expressed as a function of L_r and C_r. Figure 7.1.1 and Figure 7.1.2 show how L_r and C_r affect the values. The dv/dt stress must kept relatively low to increase the lifetime of the devices and reduce the stress across the motor isolation.

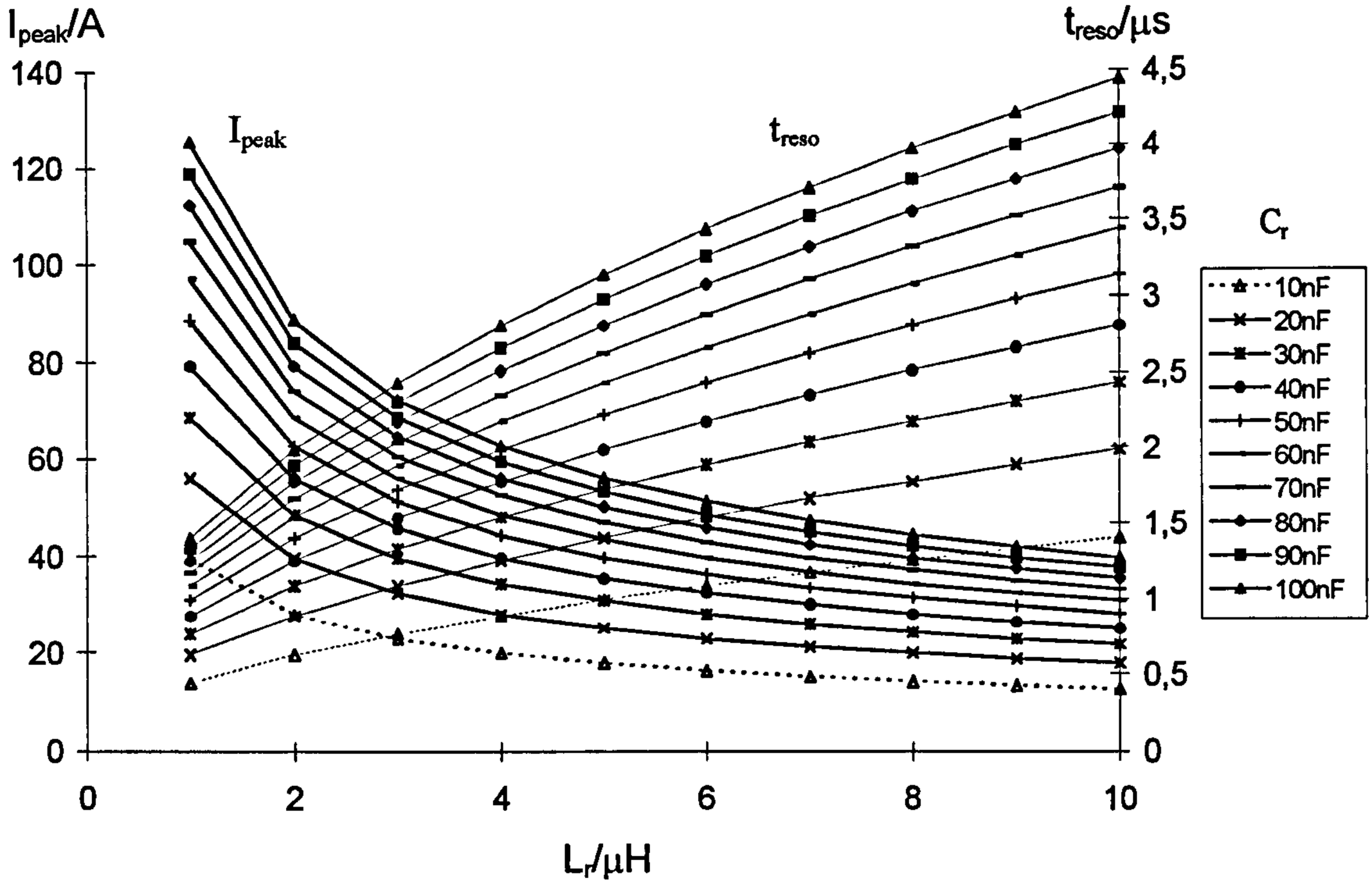


Figure 7.1.1: Resonant peak current I_{peak} and resonant time t_{reso} vs. L_r and C_r

Figure 7.1.1 shows that the peak current decreases with increasing inductance and the percentage increase of peak current is smaller at high capacitance values than at low capacitance values for one inductor size. The resonant time increases with larger inductance and the percentage increase of resonant time decreases with larger capacitance at constant inductance. Figure 7.1.1 helps to dimension resonant inductor and resonant capacitor. On one hand resonant time should be small in order to gain high PWM range. Thus a small inductance is needed. On the other hand the peak current should be kept small during resonant mode to minimise losses. Therefore the inductor chosen should be relatively large. From the design of the auxiliary switches, however, one can say that a smaller peak current is in favour for the devices because the ratio between peak current and rated current must be kept small to increase the lifetime of the devices. Most semiconductor manufacturers design IGBTs that withstand a pulse current of twice of the maximum rated current for a defined pulse length. When defining the maximum output current (42A) and boost current (15A) as rated current (57A) the resonant peak current should not overshoot 60A (Note that Figure 7.1.1 shows only the resonant peak current. The total maximum current that flows through the auxiliary path is 57A plus 60A equal 117A). Applying this result in Figure 7.1.1 one can say that the minimum inductance is around 5µH, considering that 100nF is the largest applied resonant capacitor.

The next step is the definition of value of the resonant capacitors. It is reasonable to set the commutation time of the ACPI similar to that of the dead time of its hard switched counterpart. In hardswitching topologies, 1.5µs to 2.5µs is usually applied in a power range of up to 100kW. Applying this time value and the defined inductor size in Figure 7.1.1, the resonant capacitors should be around 10nF to 30nF.

For the ACPI, 20nF resonant capacitors and a 5µH inductor are used for each pole. In reality, the self-designed inductor has an inductance of 5.7µH. In addition, later tests using 67nF capacitors have been used to compare the performance of the ACPI across a range of resonant capacitors.

Using the defined values of L_r and C_r the dv/dt stress must be considered. Figure 7.1.2 shows the dv/dt stress for various modes. The dv/dt stress applied during resonant mode and boost mode is small compared to the constant dv/dt stress of the snubber mode. The highest stress occurs during resonant mode and ramp mode. The dv/dt stress is, however, greatly reduced when compared to hardswitching as it is shown in the four following sections of this chapter.

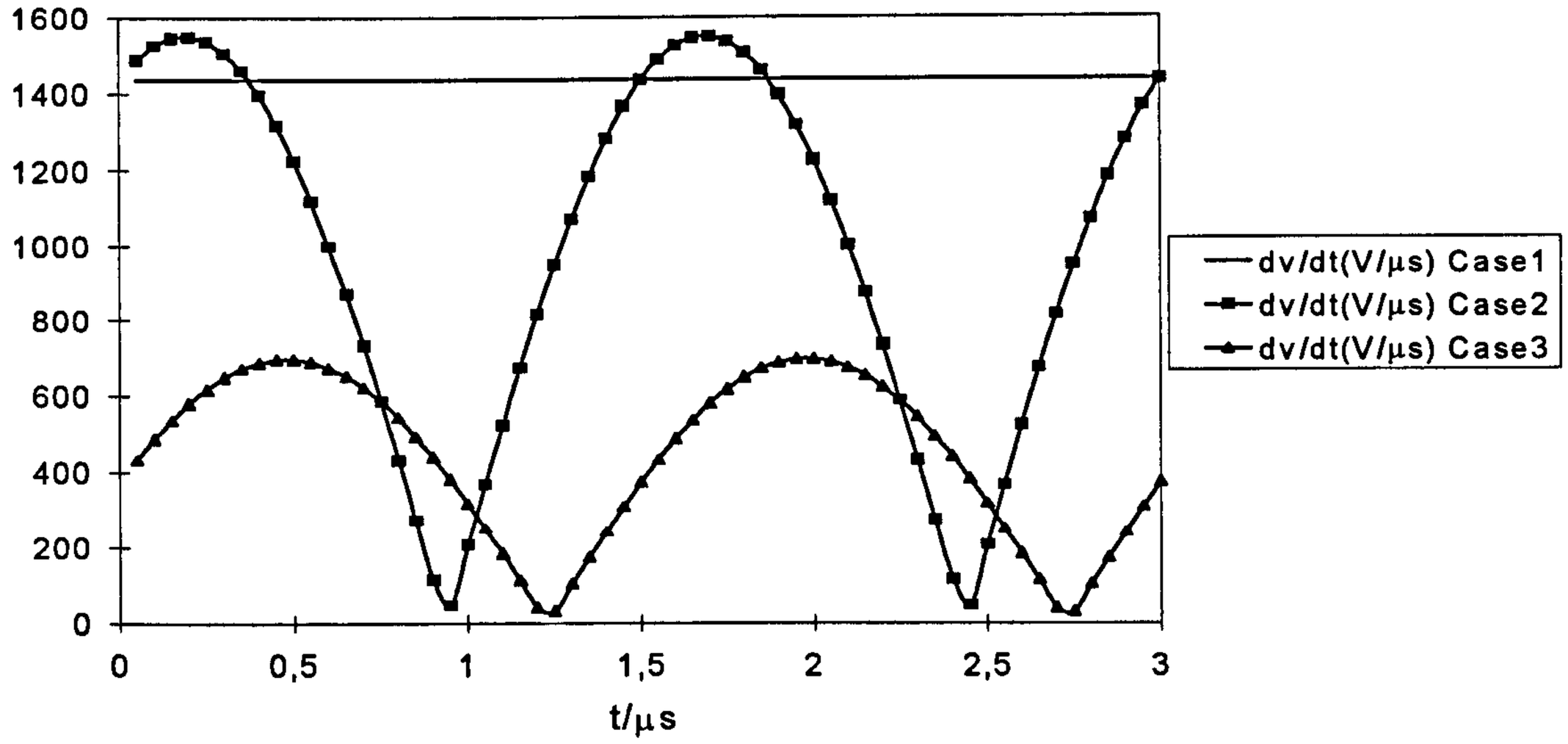


Figure 7.1.2: dv/dt stress for snubber mode (Case 1), resonant mode and ramp mode (Case 2) and resonant mode and boost mode (Case 3) vs. time (L_r=5,7µH, C_r=20nF, I_{boost}=15A, V_{dc}=560V)

Beside the dv/dt stress another kind of stress has to be considered. The di/dt stress of the auxiliary switches must be in an appropriate range. A high di/dt stress leads to damage on IGBT and diode. Figure 7.1.3 shows the relation between the maximum rise current I_{max} and ramp and boost time t_r at ramp mode and boost mode as a function of L_r. Firstly the maximum resonant current I_{max} is not a function of L_r or C_r, because the current level is defined from the

maximum load current (42A) and the boost current (15A). The time at ramp mode and boost mode is only a function of L_r (equation 4.2.48). This mode controls the current stress di/dt (the current stress during the resonant mode is negligible compared to the current stress during ramp mode and boost mode). Figure 7.1.3 shows that a larger inductor reduces the di/dt stress but increases the commutation time and therefore worsens the PWM control range.

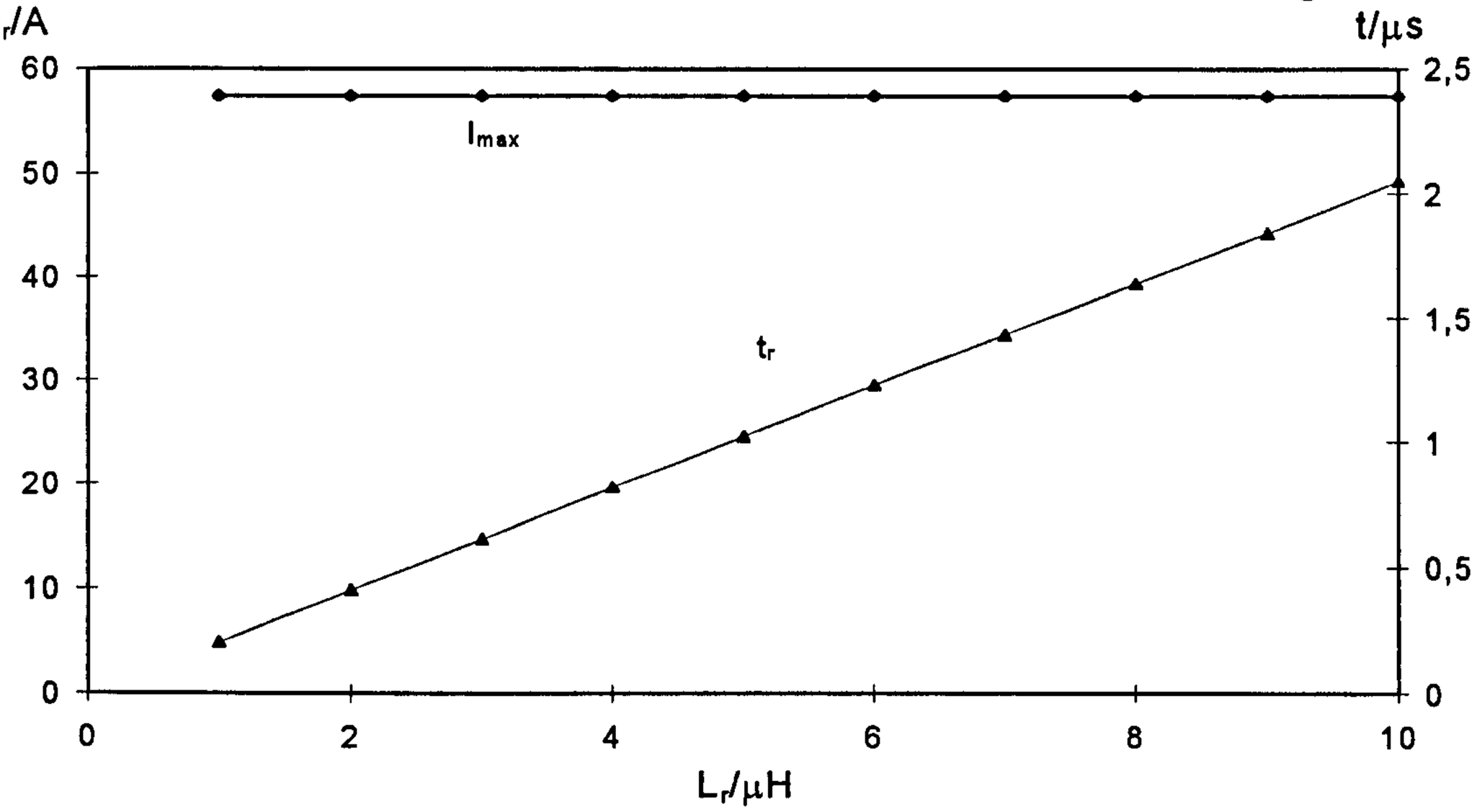


Figure 7.1.3: Maximum rise current I_{max} and rise time t_r during ramp mode and boost mode vs. L_r

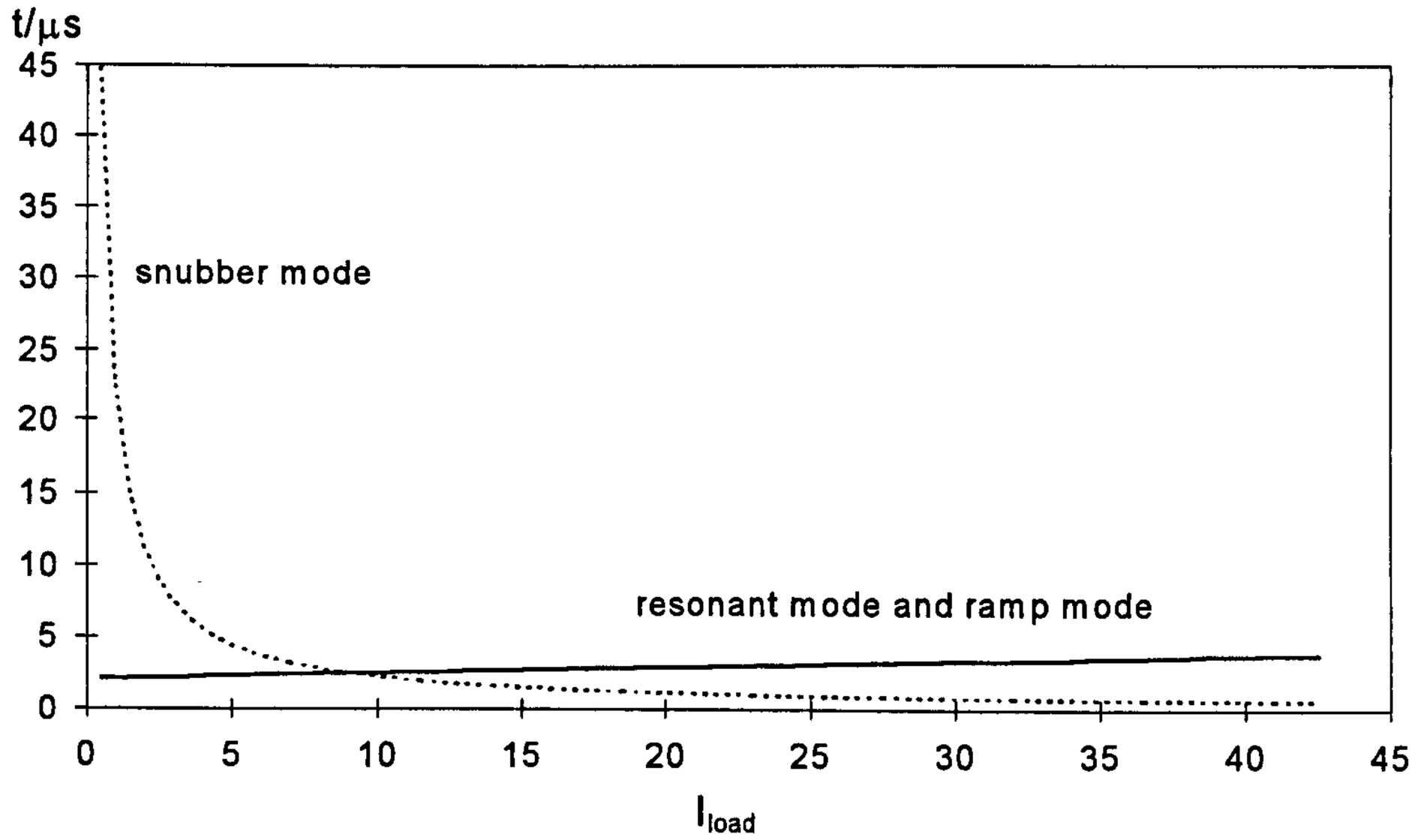


Figure 7.1.4: Commutation time of snubber mode compared to commutation time ($t_{reso}+t_r$) of resonant mode and ramp mode vs. load current

Figure 7.1.4 shows the differences in commutation time ($t_{reso}+t_r$) when applying resonant mode and ramp mode or snubber mode. At around 9A the commutation time of the snubber mode is

shorter. Nevertheless applying the snubber mode problems start to occur. When the ACPI is running under full load and with a low output frequency the midpoint dc-link voltage of the dc-link capacitors starts to drift. In general the midpoint voltage varies around the half of the dc-link voltage. That is because the charge in and out of the midpoint is a function of the amplitude and direction of the load current. Charge is referred and drawn from the midpoint during one output frequency cycle. In case of connecting all three poles to one pair of dc-link capacitors the symmetric output current waveforms show that the charge from in and out of the midpoint is equalised. When applying the snubber mode the amount of charge is unequal because during the snubber mode the auxiliary circuit is not activated. Therefore a shift of the midpoint potential occurs. Nevertheless, it has to be mentioned that the ACPI has midpoint shift problems even when applying resonant mode and ramp mode. With high output current and low frequency, as during motor start up, there may be a sustained time interval in which the charge resulting from ramp mode and resonant mode can not be compensated using 'normal' control techniques. Thus the control must be extended to handle this situation. The designed ACPI monitors the midpoint voltage. In case the voltage reaches a threshold the controller indicates a fault.

7.2 Measured Switching Waveforms at Main Switches

The following four sections show waveforms of voltage, current and losses, measured at the bottom device of one pole of the ACPI under various commutation processes and under the conditions of hardswitching and softswitching using 20nF and 67nF capacitors. The load current is set to around 50A.

7.2.1 Waveforms for commutation IGBT-Diode, bottom IGBT conducts and turns off

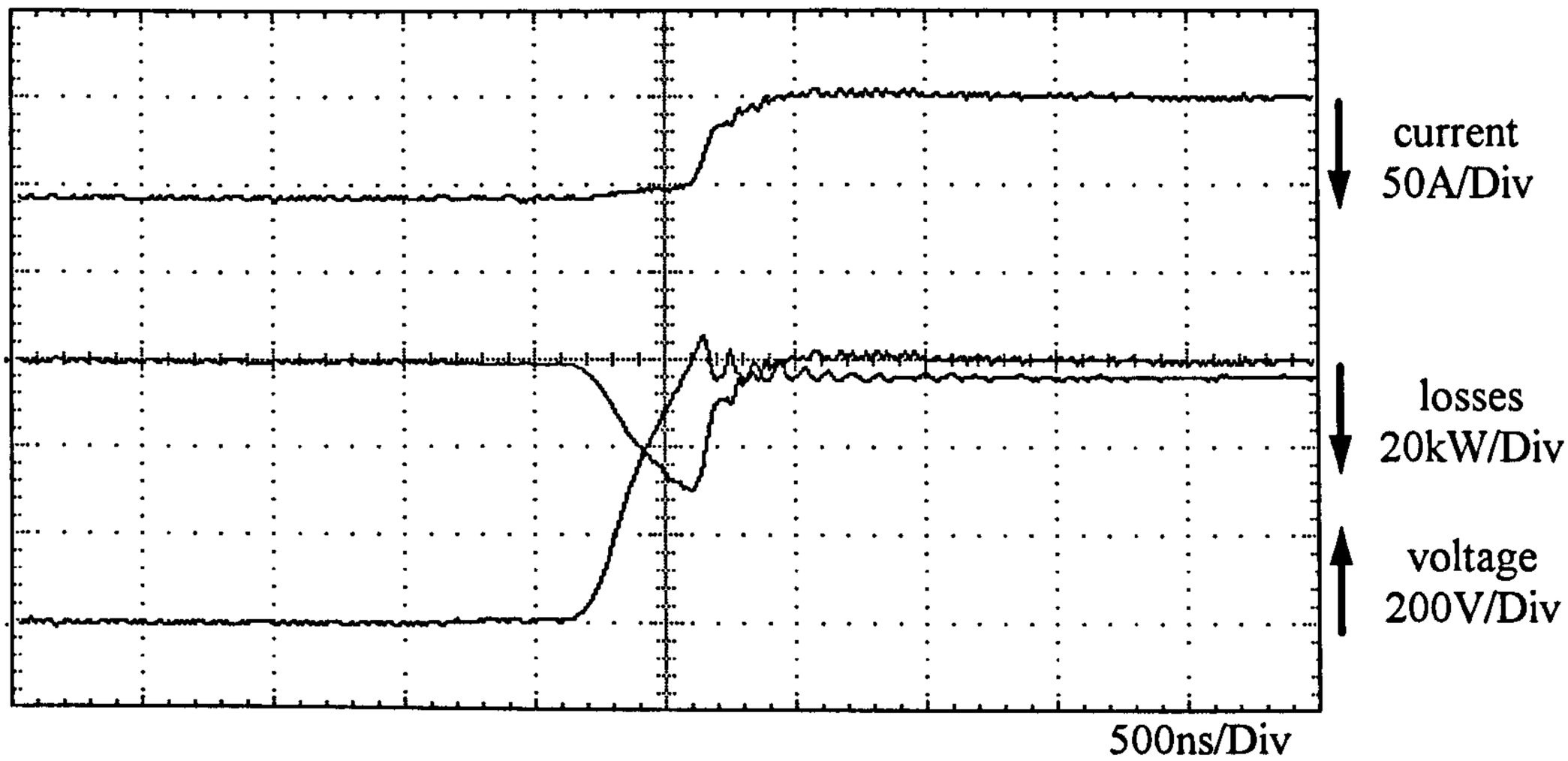


Figure 7.2.1: Turn-off waveforms under hardswitching conditions (IGBT-Diode)

Figure 7.2.1 shows the typical turn-off waveforms. The voltage rises up quickly towards the dc-link voltage level. Stray inductances in the converter design leads to overshoot in the voltage. Once the voltage reaches its maximum value, the current start to decrease. The long overlap time of voltage and current leads to high turn-off losses.

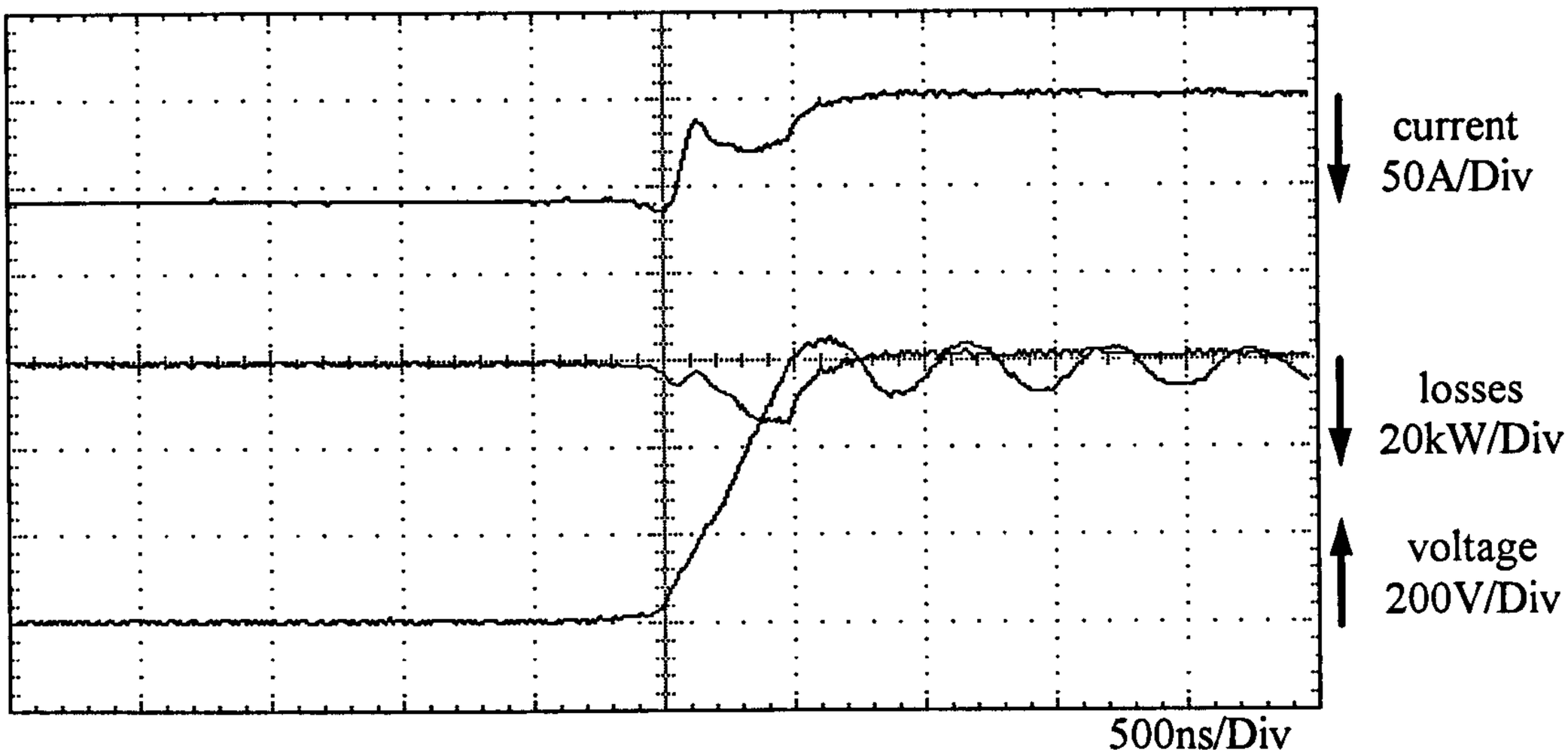


Figure 7.2.2: Turn-off waveforms under softswitching conditions (C_r=20nF, IGBT-Diode)

The voltage waveform looks similar to that of hardswitching, but the current waveform looks different (Figure 7.2.2). Firstly the current waveform shows a boost step before the resonant part takes place. This is the effect of the described boost mode. Secondly the tail current shows a 'bump' in its tail. This effect is characteristic for softswitching as it is described in Chapter 6. Both boost step and 'bump' lead to losses. However, the losses are greatly reduced compared to hardswitching, because the overlap time of current and voltage is shorter.

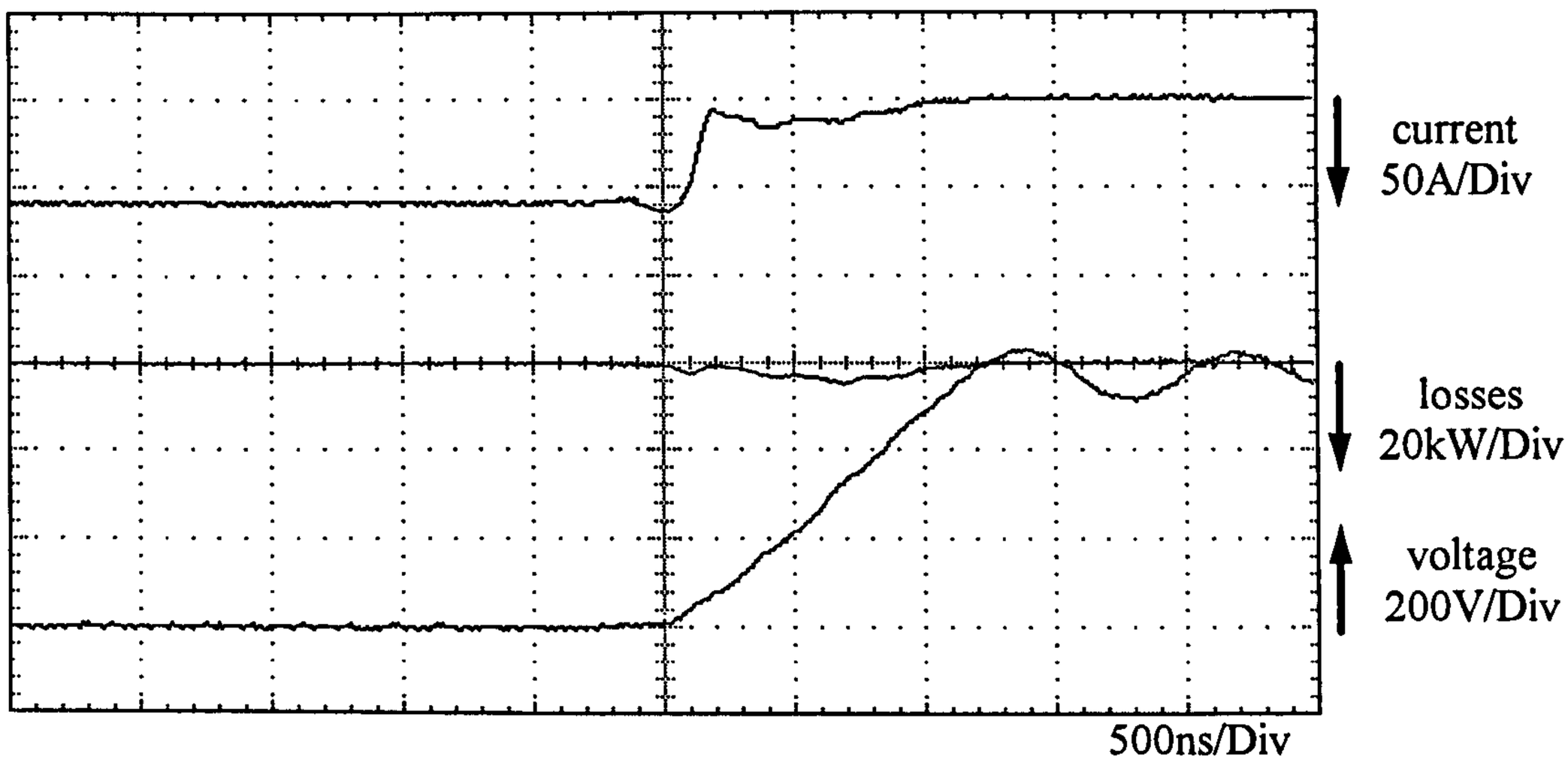


Figure 7.2.3: Turn-off waveforms under softswitching conditions (C_r=67nF, IGBT-Diode)

The voltage rise in Figure 7.2.3 is slower compared to Figure 7.2.2. That is because of the larger resonant capacitor. The 'bump' in the tail current is smaller in amplitude but longer. The losses are further reduced.

7.2.2 Waveforms for commutation Diode-IGBT, top diode conducts and bottom IGBT turns on

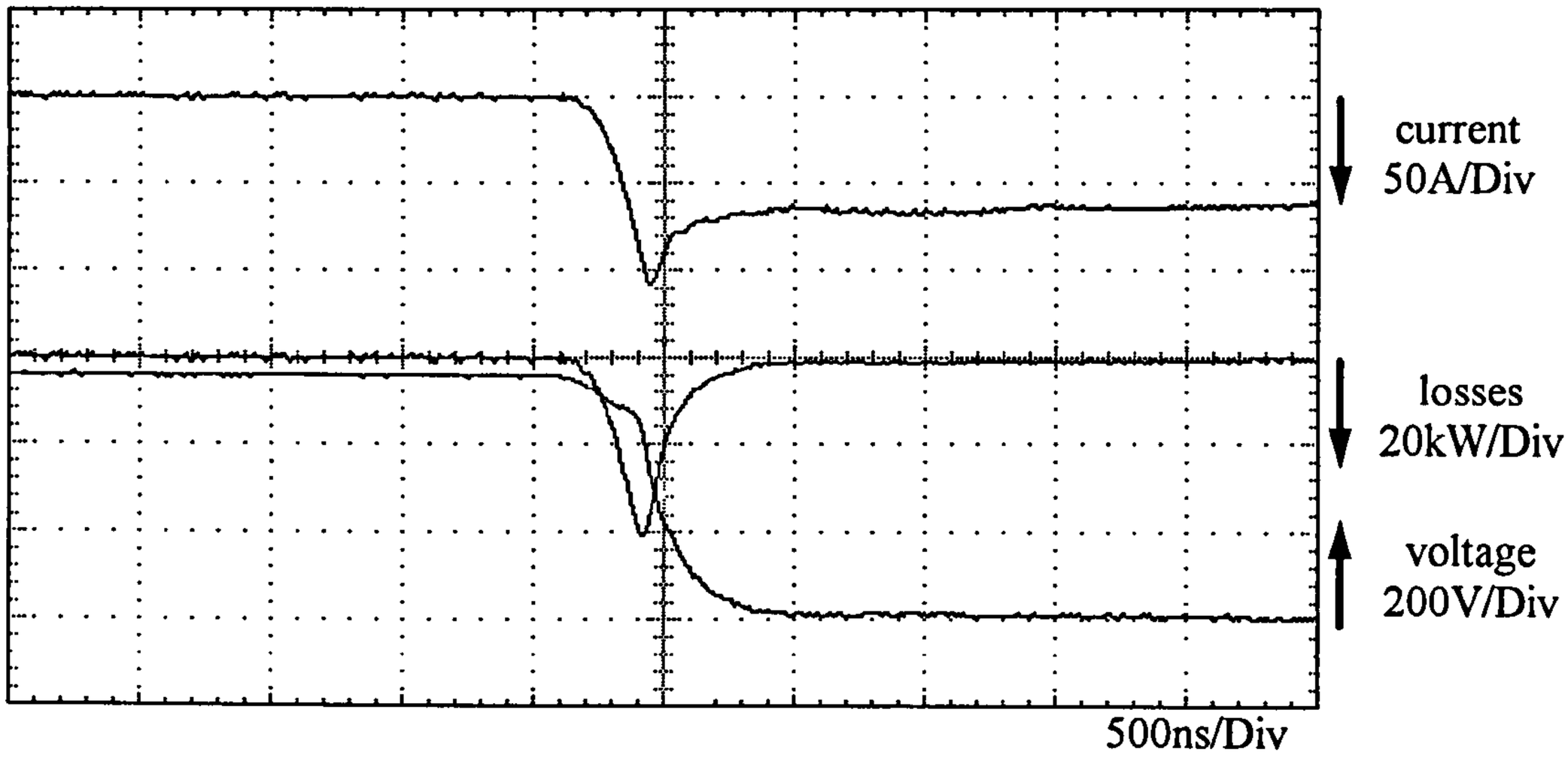


Figure 7.2.4: Turn-on waveforms under hardswitching conditions (Diode-IGBT)

Figure 7.2.4 shows the typical waveform of a hardswitching converter during commutation Diode-IGBT. The current peak is the result of the reverse recovery effect of the diode. Again losses are high.

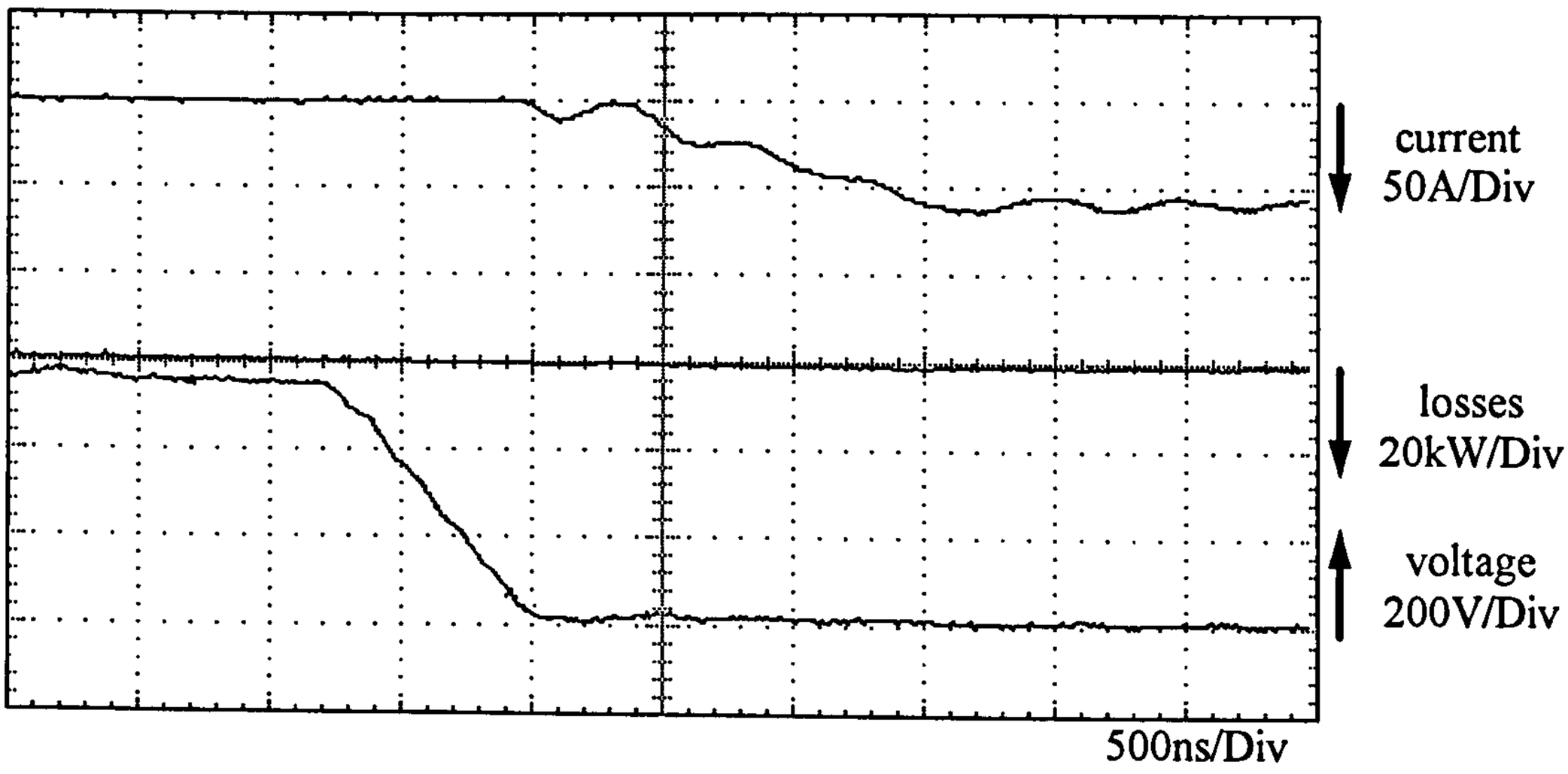


Figure 7.2.5: Turn-on waveforms under softswitching conditions (C_r=20nF, Diode-IGBT)

The waveform in softswitching mode looks totally different when compared with hardswitching. The voltage resonates to zero. Once the voltage is zero the current start to increase (Figure 7.2.5). The oscillation in the current resolves from the converter design. During the resonant mode the capacitors carry the load current. Thus no reverse recovery effect occurs during turn-on conditions. This results in reduced turn-on losses.

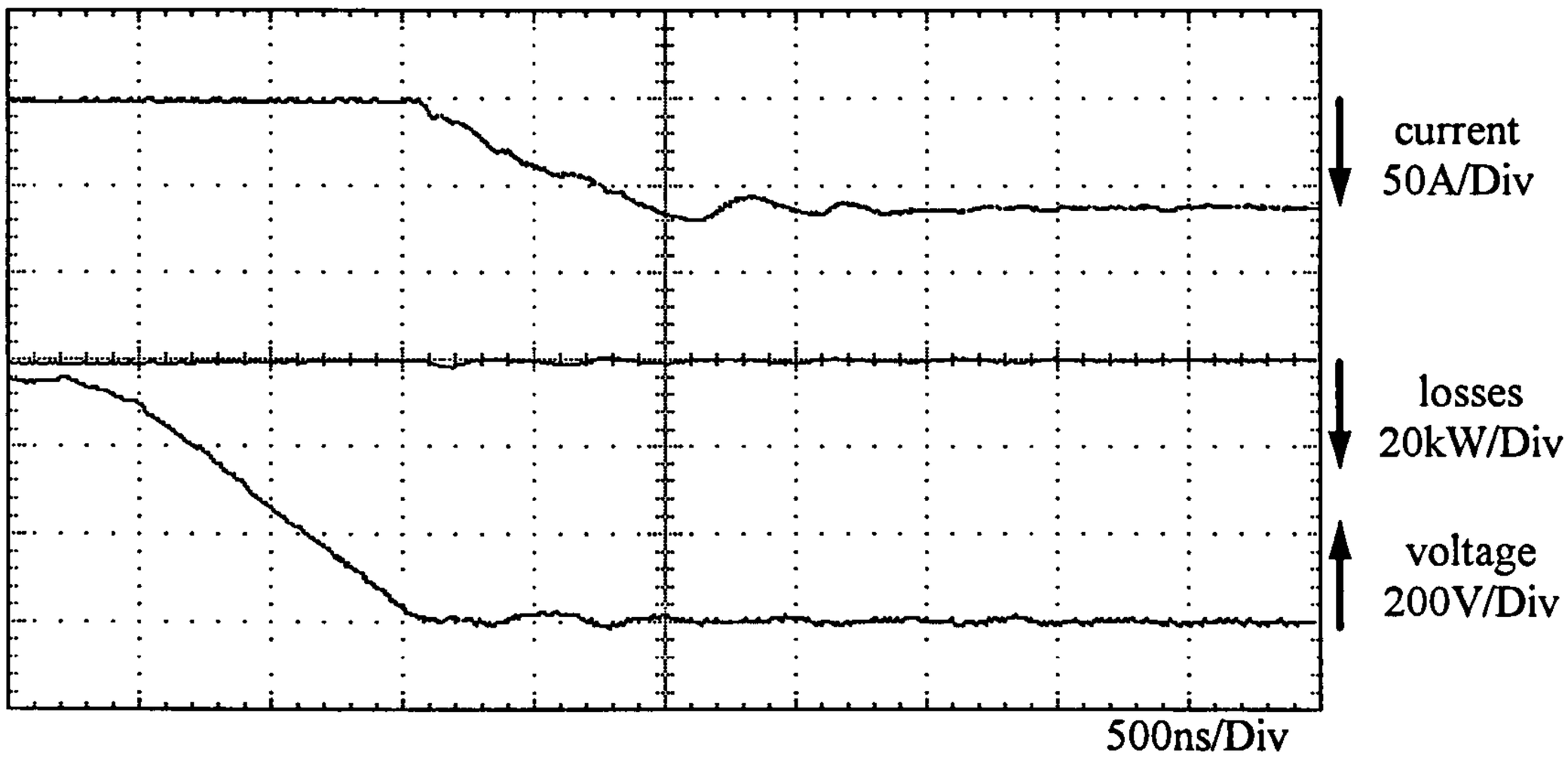


Figure 7.2.6: Turn-on waveforms under softswitching conditions (C_r=67nF, Diode-IGBT)

The dv/dt stress is lower compared with Figure 7.2.5. Again losses are low (Figure 7.2.6).

7.2.3 Waveforms for commutation Diode-IGBT, bottom diode conducts and top IGBT turns on

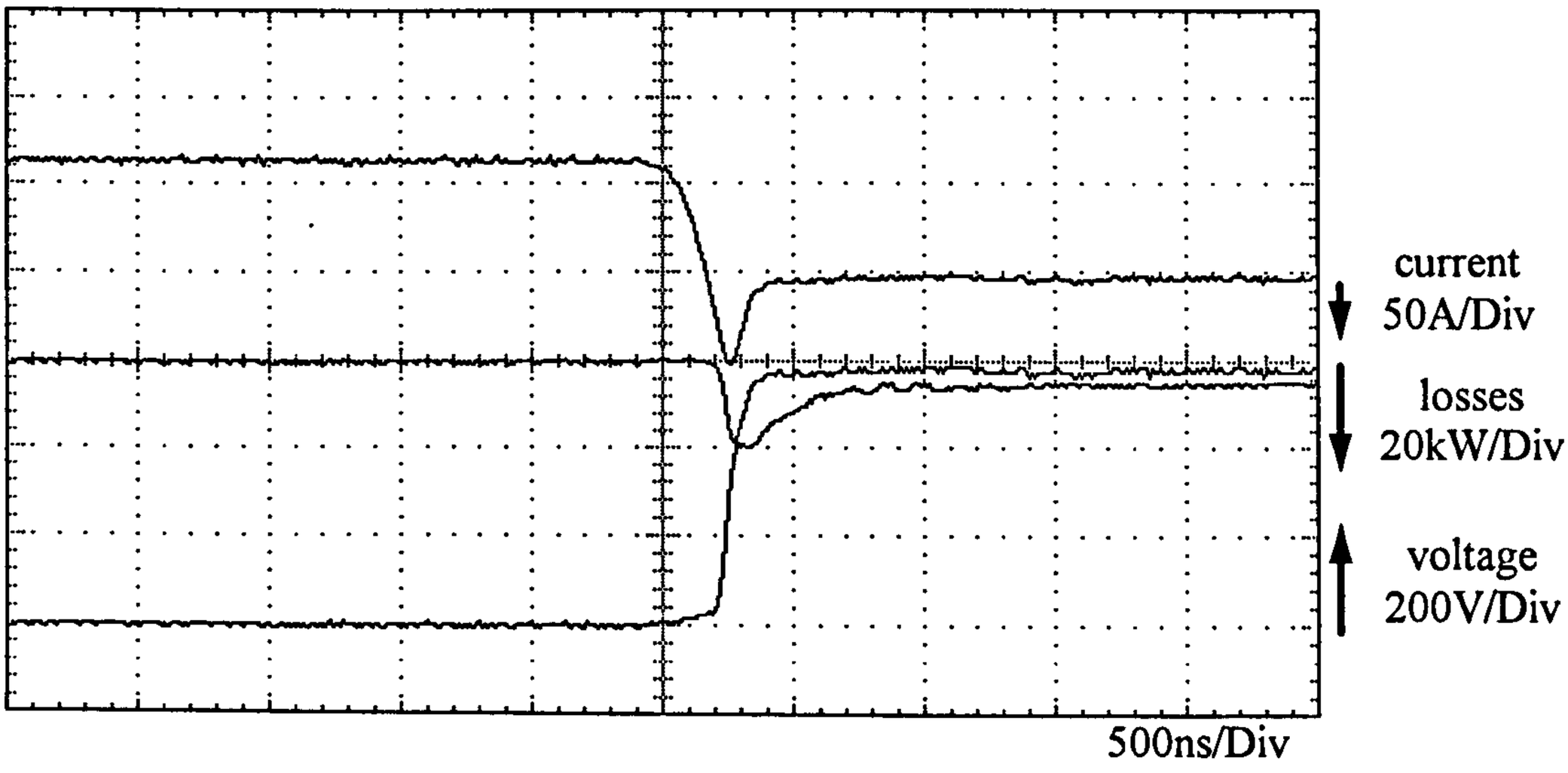


Figure 7.2.7: Turn-off waveforms (diode) under hardswitching conditions (Diode-IGBT)

Figure 7.2.7 shows again a peak in the current waveform. Again the stored charge of the conducting diode has to be removed. The losses in this commutation process are lower compared to the losses shown in Figure 7.2.4. That is because the switch is not conducting the load current during turn-off.

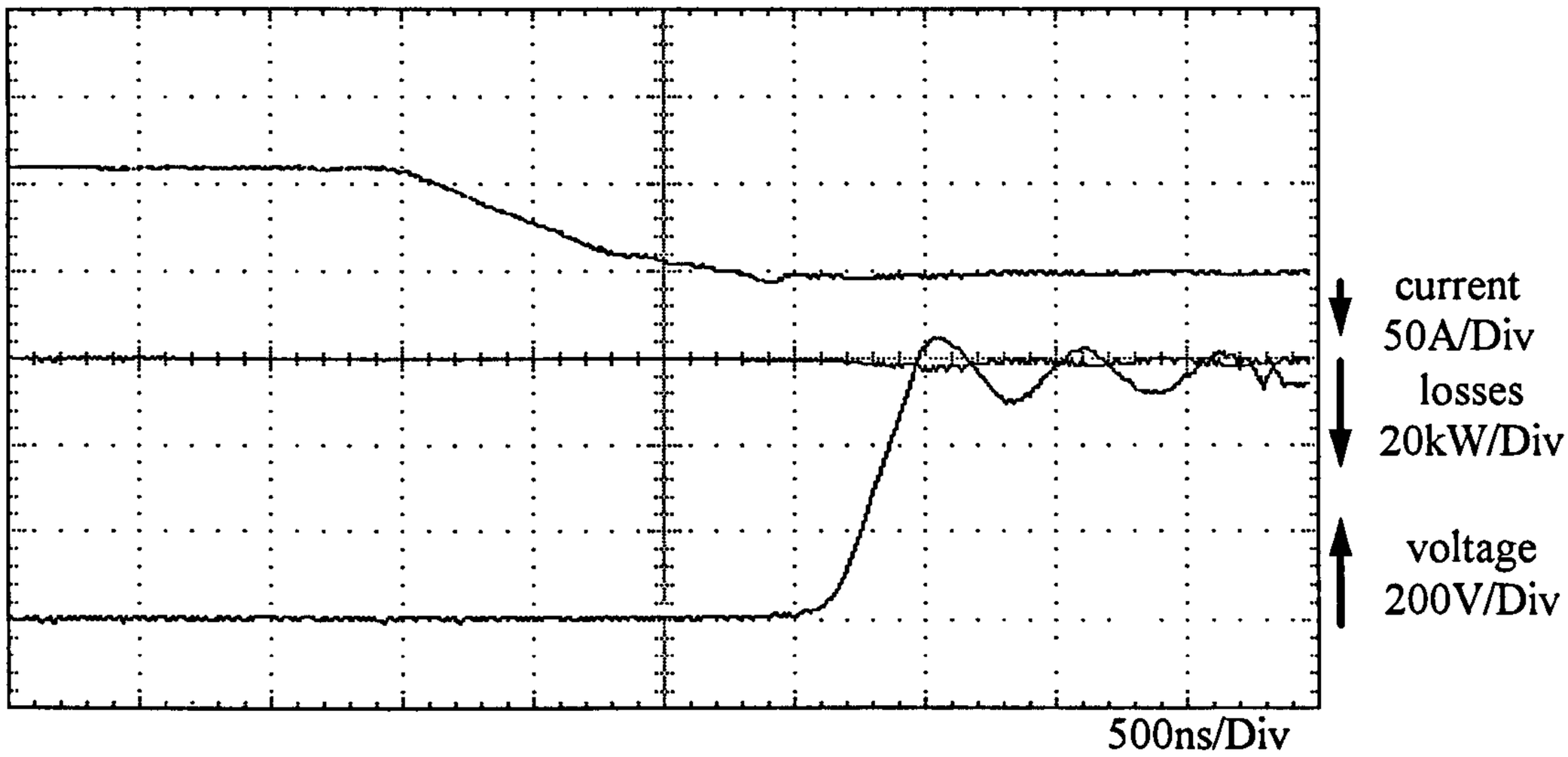


Figure 7.2.8: Turn-off waveforms (diode) under softswitching conditions (C_r=20nF, Diode-IGBT)

Figure 7.2.8 shows no peak current, because once the IGBT is turned off the resonant circuit is activated. The losses are greatly reduced compared to hardswitching.

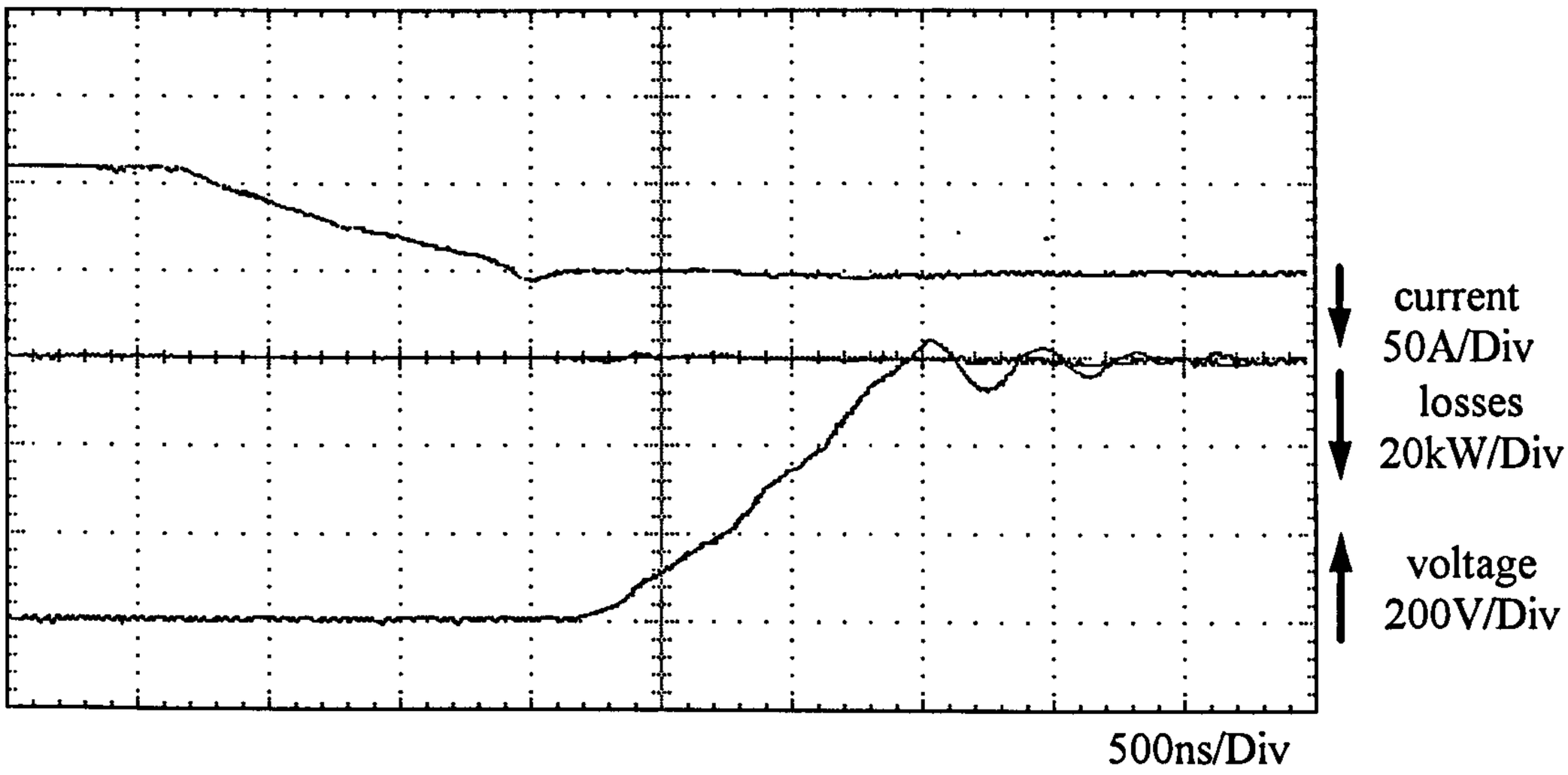


Figure 7.2.9: Turn-off waveforms (diode) under softswitching conditions (C_r=67nF, Diode-IGBT)

Again a large capacitor decreases dv/dt stress and losses, but increases the commutation time.

7.2.4 Waveforms for commutation IGBT-Diode, top IGBT conducts and turns off

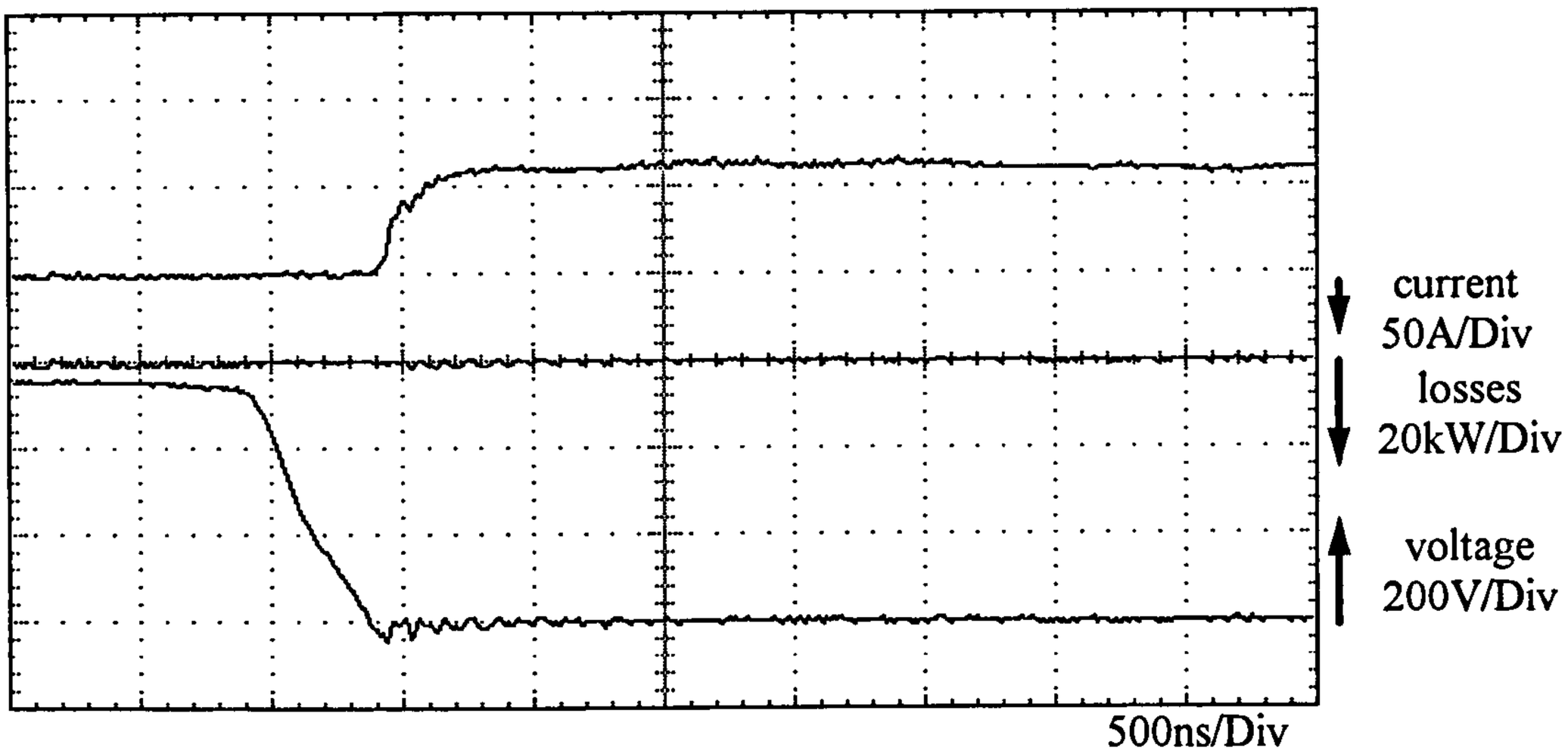


Figure 7.2.10: Turn-on waveforms (diode) under hardswitching conditions (IGBT-Diode)

The commutation process can be seen as softswitching in a hard switched converter. Virtually zero losses occur. Nevertheless high dv/dt stress remains.

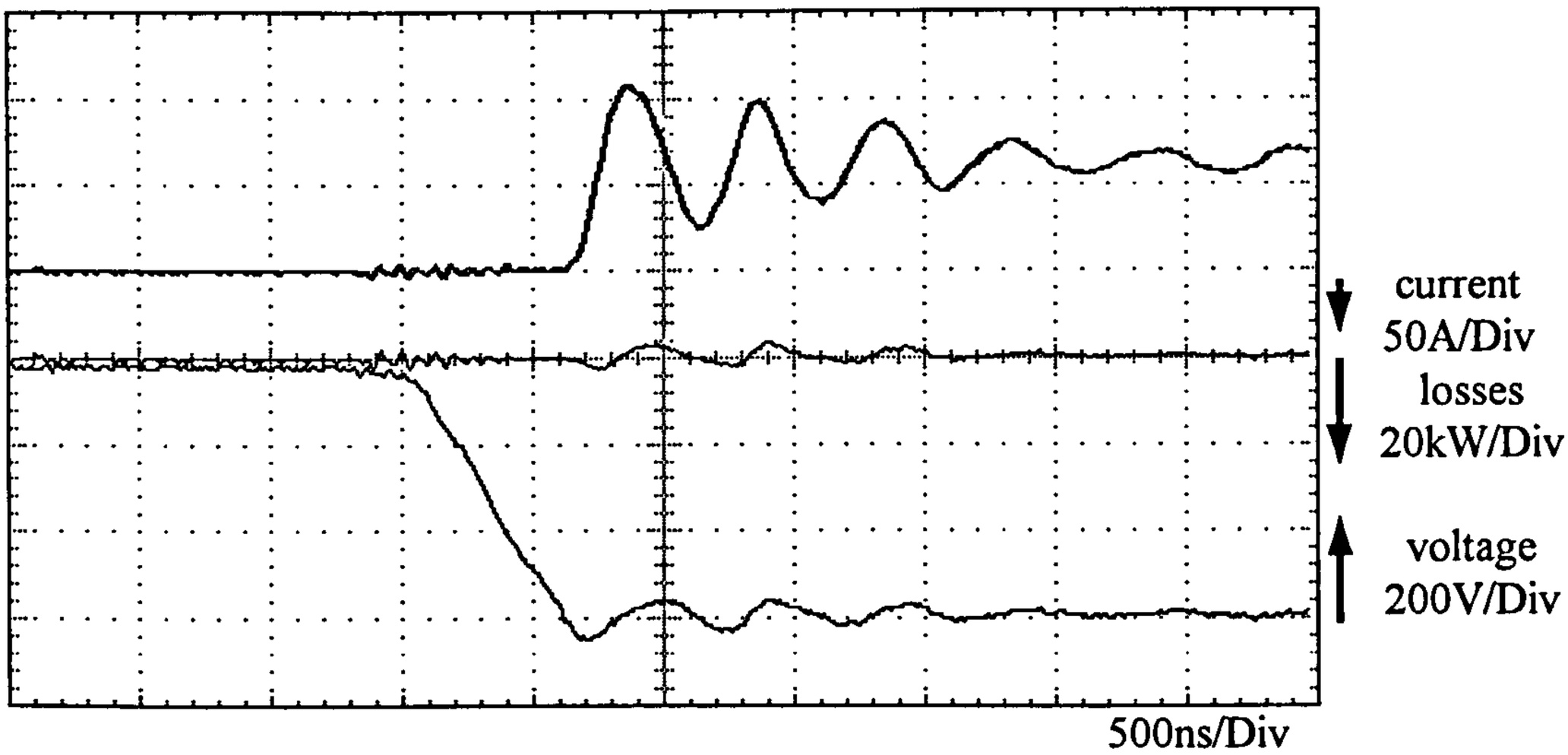


Figure 7.2.11: Turn-on waveforms (diode) under softswitching conditions (C_r=20nF, IGBT-Diode)

The current oscillation is characteristically for this commutation process. The oscillation results from a resonant circuit formed from the resonant inductor and the reverse recovery capacitance of the auxiliary diode. This oscillation leads to losses. To some extend the turn-on

losses of the main switches of the softswitching converter outweigh the turn-on losses of the main switches of the hard switched converter under this switching conditions.

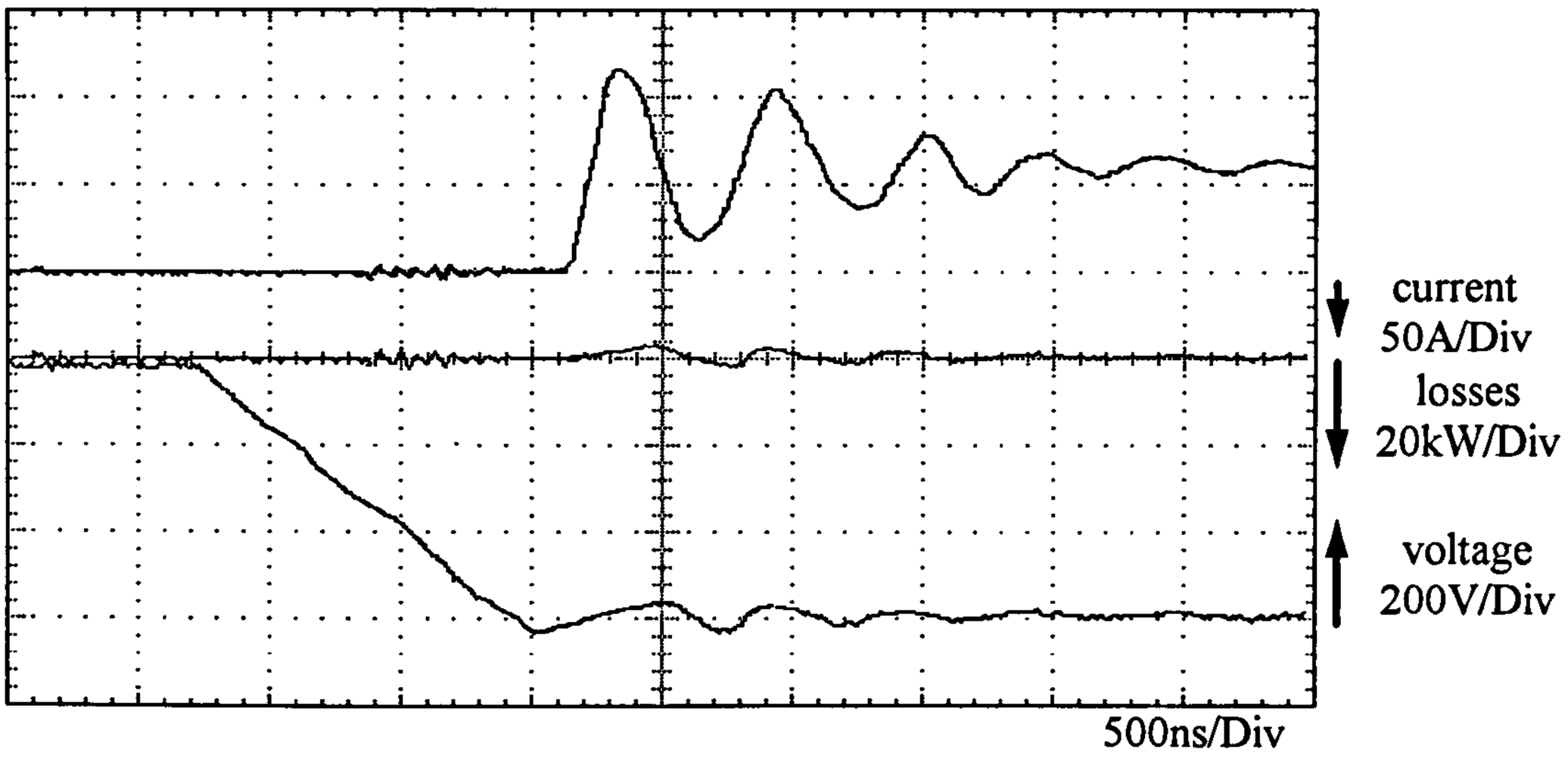


Figure 7.2.12: Turn-on waveforms (diode) under softswitching conditions (C_r=67nF, IGBT-Diode)

Using a larger capacitor has no effect on the oscillation (Figure 7.2.12).

7.2.5 Output Current Waveforms

Figure 7.2.13 shows the output phase current of the hardswitching converter at f_s=10kHz switching frequency, f_{out}=50Hz output frequency and 28A peak current.

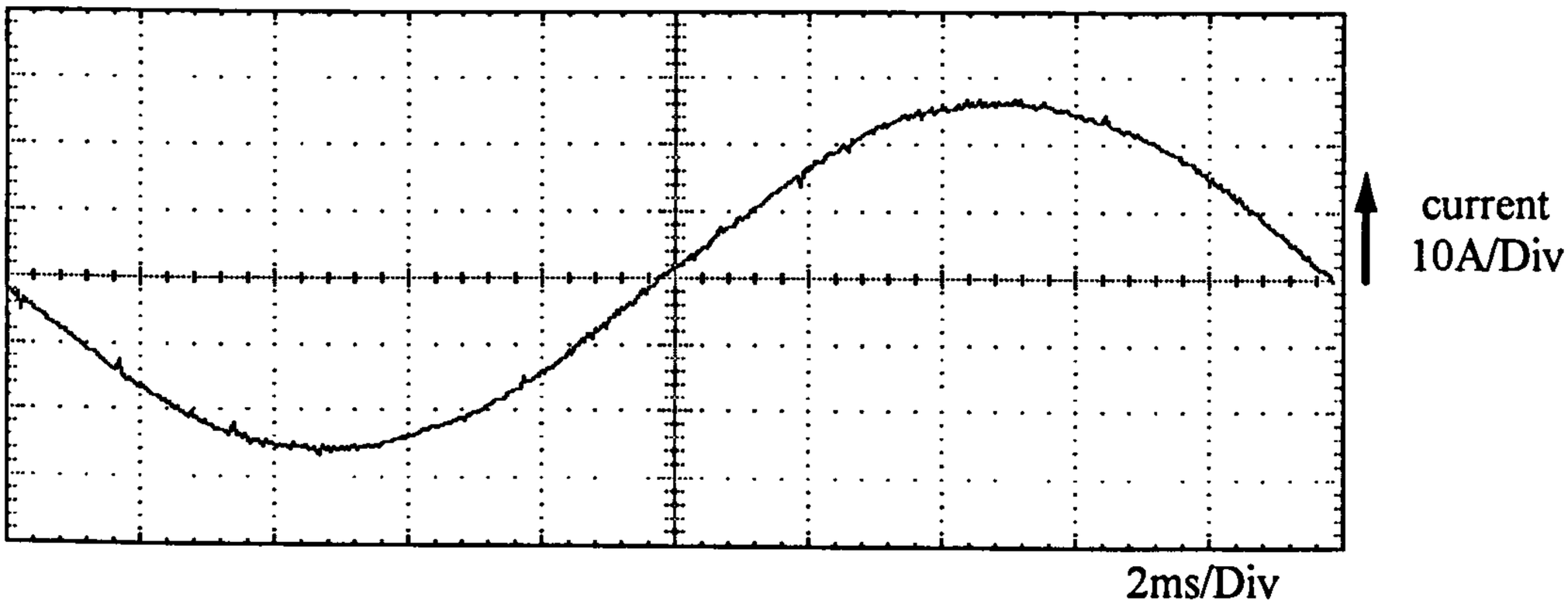


Figure 7.2.13: Phase output current of the hard switched converter (f_s=10kHz, f_{out}=50Hz, I_{load}=20A)

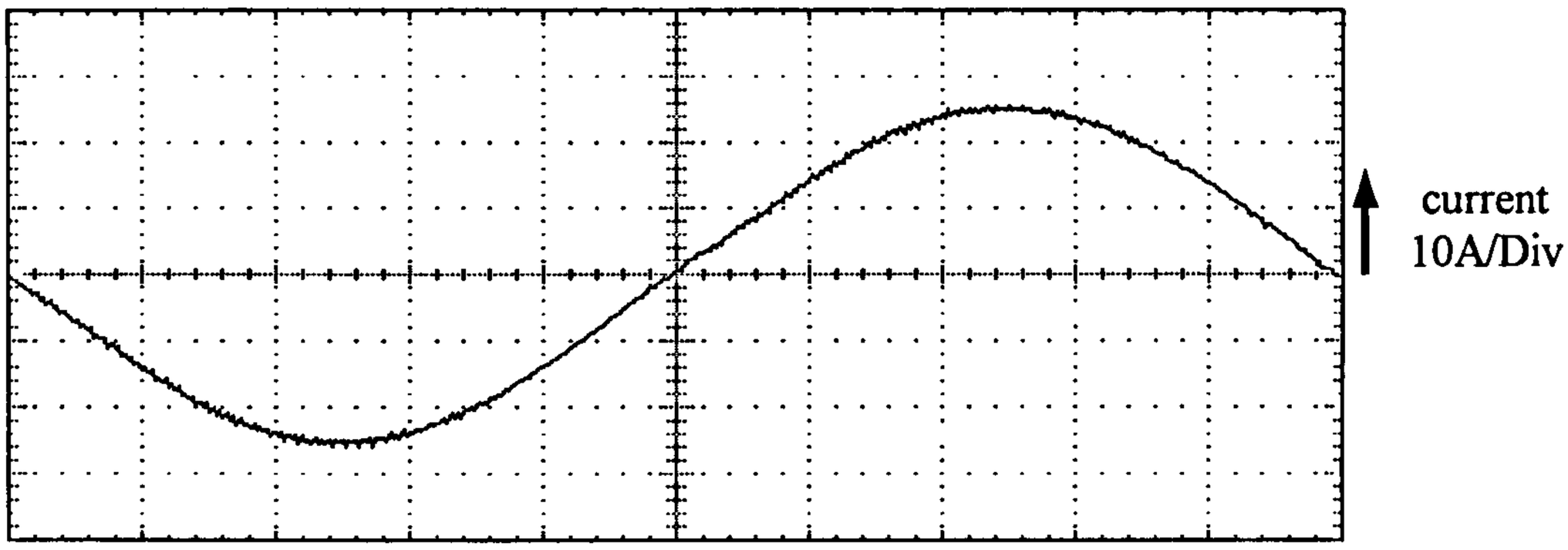


Figure 7.2.14: Phase output current of the ACPI (f_s=10kHz, f_{out}=50Hz, I_{load}=20A)

Figure 7.2.14 shows the phase output current of the ACPI under the same load conditions. Virtually no difference is seen between the current waveforms. However, section 7.4 investigates the current frequency spectra. Differences have been found in current harmonic distortions.

Figure 7.2.15 shows the output current waveform at a switching frequency of f_s=2.5kHz including the resonant current of the auxiliary circuit (f_s=2.5kHz, f_{out}=50Hz). The figure shows that the resonant peak current follows the amplitude and direction of the phase current. During the commutation IGBT-Diode the maximum current is constant to 15A, whereas during the commutation Diode-IGBT the current follows the amplitude of the output current.

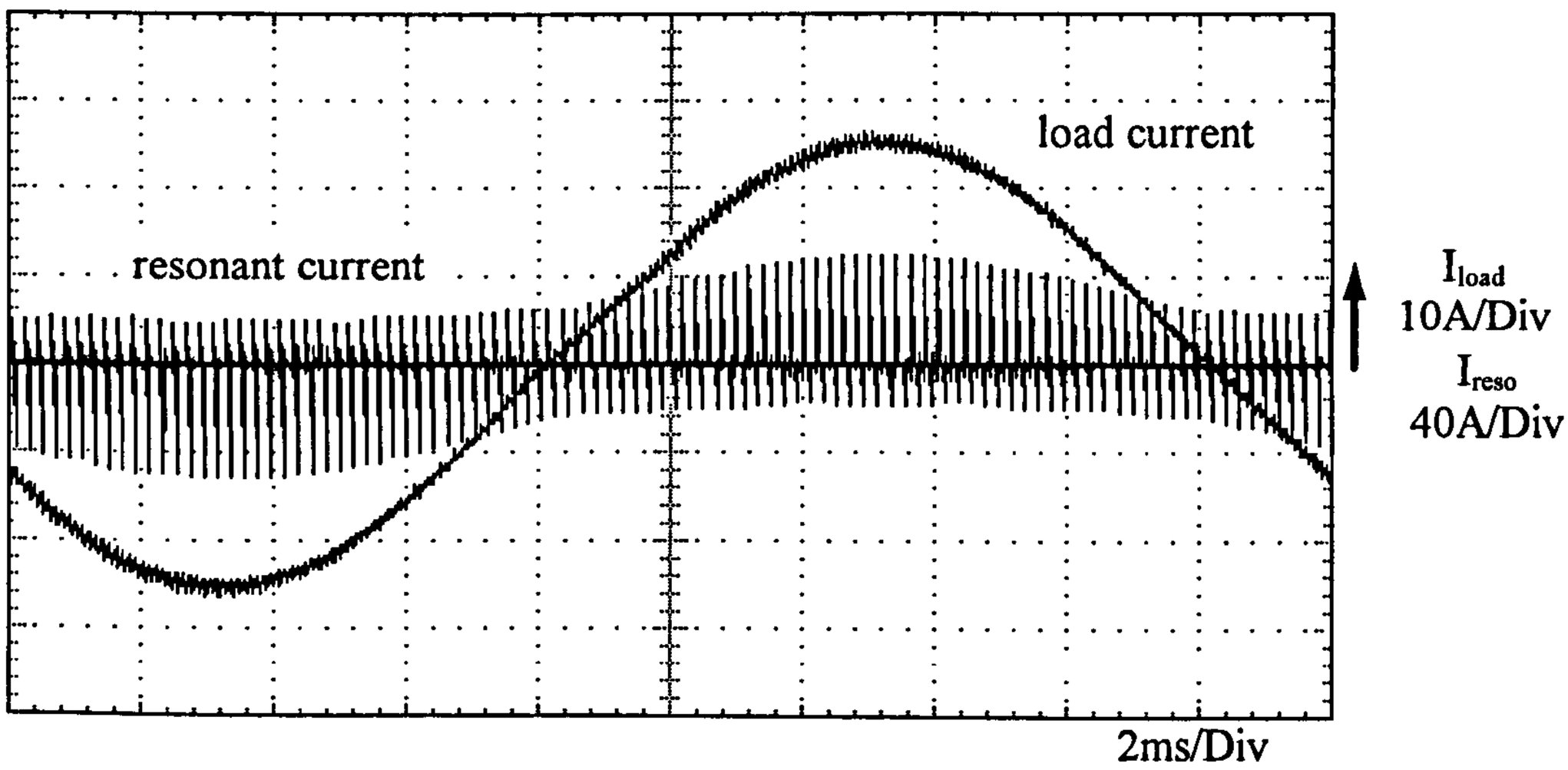


Figure 7.2.15: Phase output current and auxiliary current of the ACPI (f_s=2,5kHz, f_{out}=50Hz, I_{load}=20A. f_s=2,5kHz has been chosen to show the resonant pulses in detail over the whole output frequency)

7.2.6 Measured Waveforms at Auxiliary Switches

Figure 7.2.16 shows the current in the auxiliary path during one pole commutation period. When the auxiliary current reaches zero ampere the reverse recovery current of the auxiliary diode is activated. That leads to the overshoot in current as it can be seen in Figure 7.2.16. The current overshoots leads to losses, voltage oscillation across the auxiliary devices and current ringing as it is shown in Figure 7.2.11 and 7.2.12. The first resonant cycle represents the commutation IGBT-Diode, whereas the second cycle shows the commutation Diode-IGBT (load current 20A).

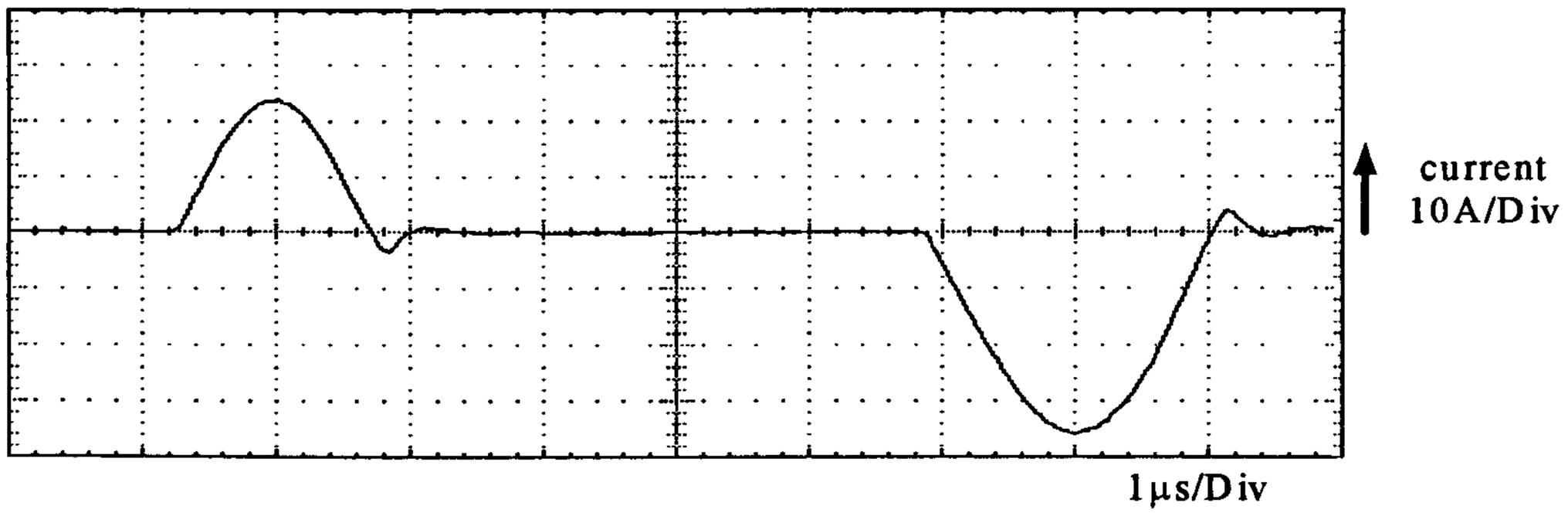


Figure 7.2.16: Auxiliary current of the ACPI (f_s=10kHz, I_{load}=20A)

Figure 7.2.17 shows voltage, current and losses waveforms across the auxiliary path in one modulation period. The highest losses occur in the inductor and not in the auxiliary switches. The conduction losses of the auxiliary switches are negligible, but the reverse recovery effect of the auxiliary diodes worsens the results.

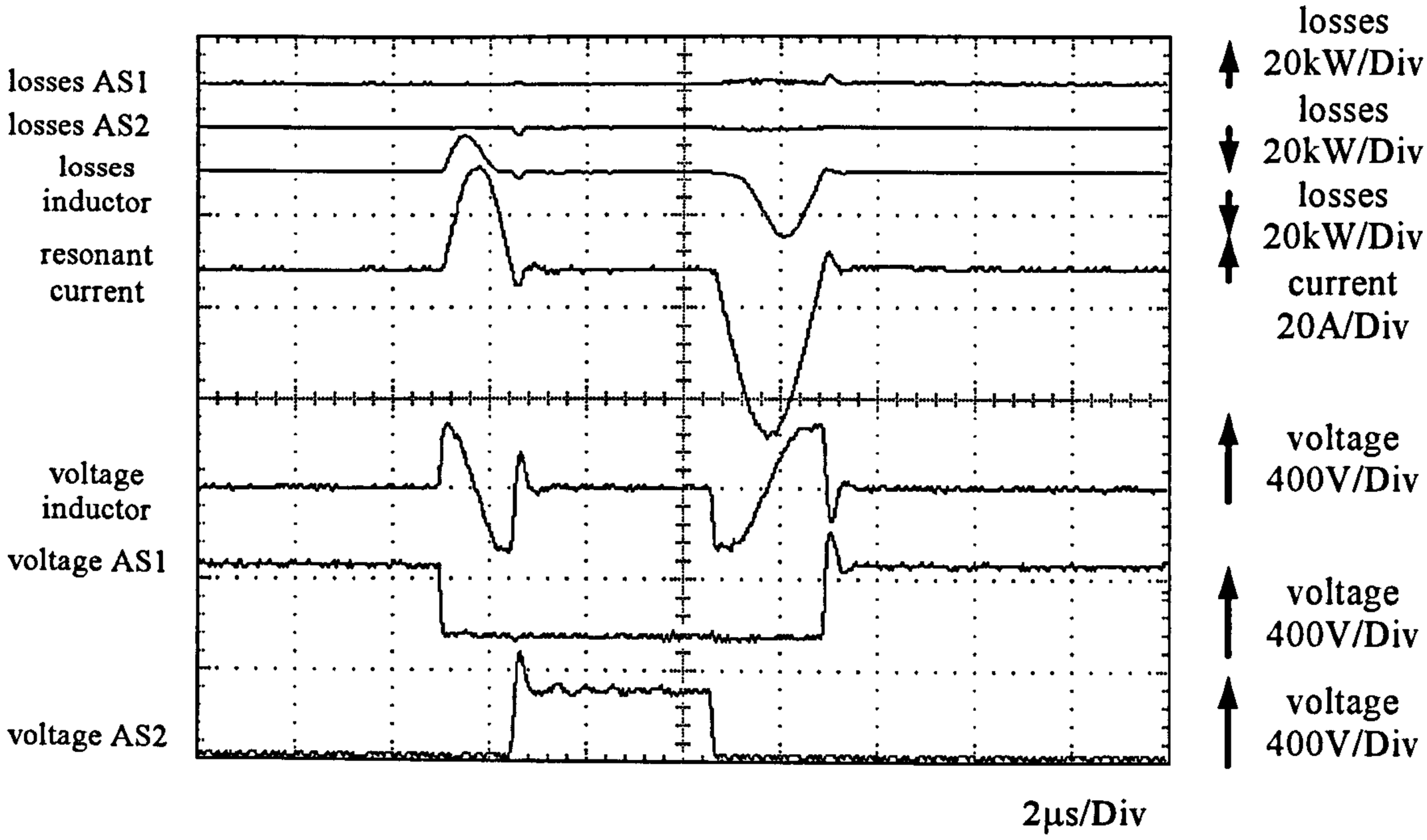


Figure 7.2.17: Comparison of waveforms measured at devices in the auxiliary path (I_{load}=20A)

Figure 7.2.18 shows the synchronisation of voltage waveform of the upper main switch and the current waveform of the auxiliary circuit during one turn-on and turn-off event of the upper switch. The waveform of losses represent the losses of the upper switch.

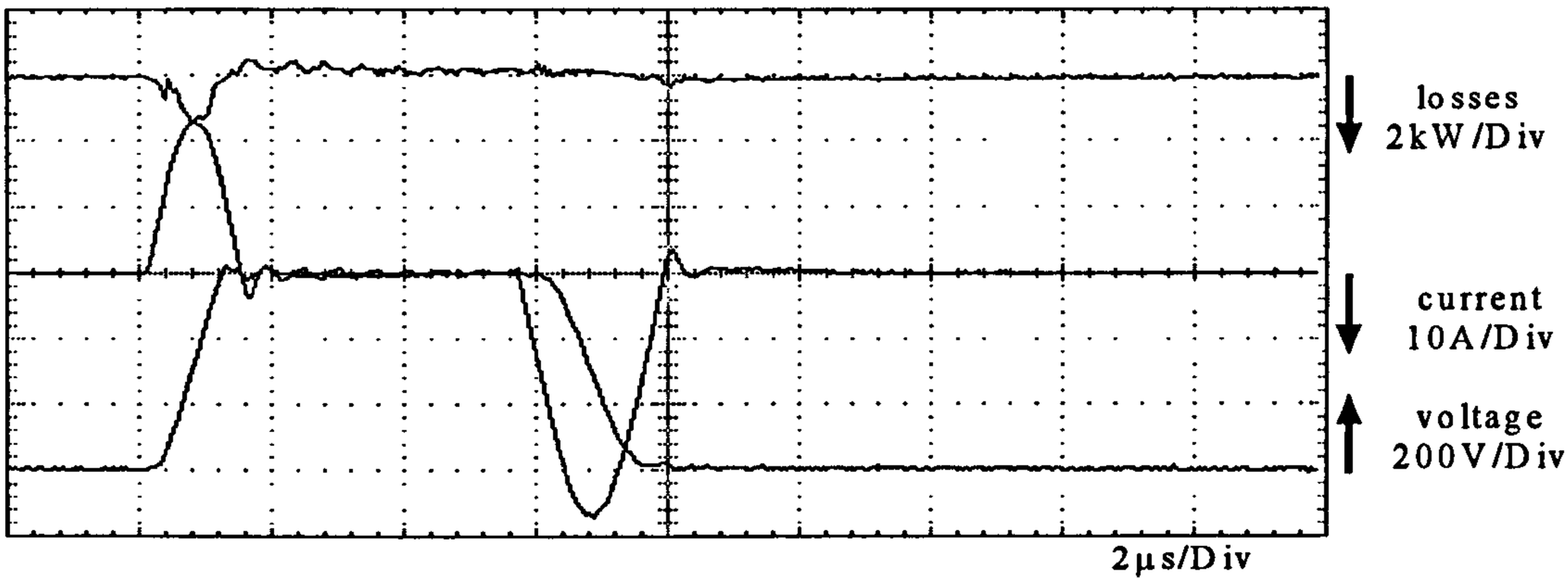


Figure 7.2.18: Synchronisation of the voltage across the main switch and the auxiliary current (f_s=10kHz, I_{load}=20A). Losses shown are for the main switch

Figures that show the synchronisation of voltage waveform of the main switches and the auxiliary current may be used to determine delay times resulting from the driver circuits or the devices itself.

7.3 Measured Switching Losses

The turn-on and turn-off losses of the hardswitching operating switch are shown in Figure 7.3.1. As already known turn-off losses are higher compared to turn-on losses. Both increase with the load current.

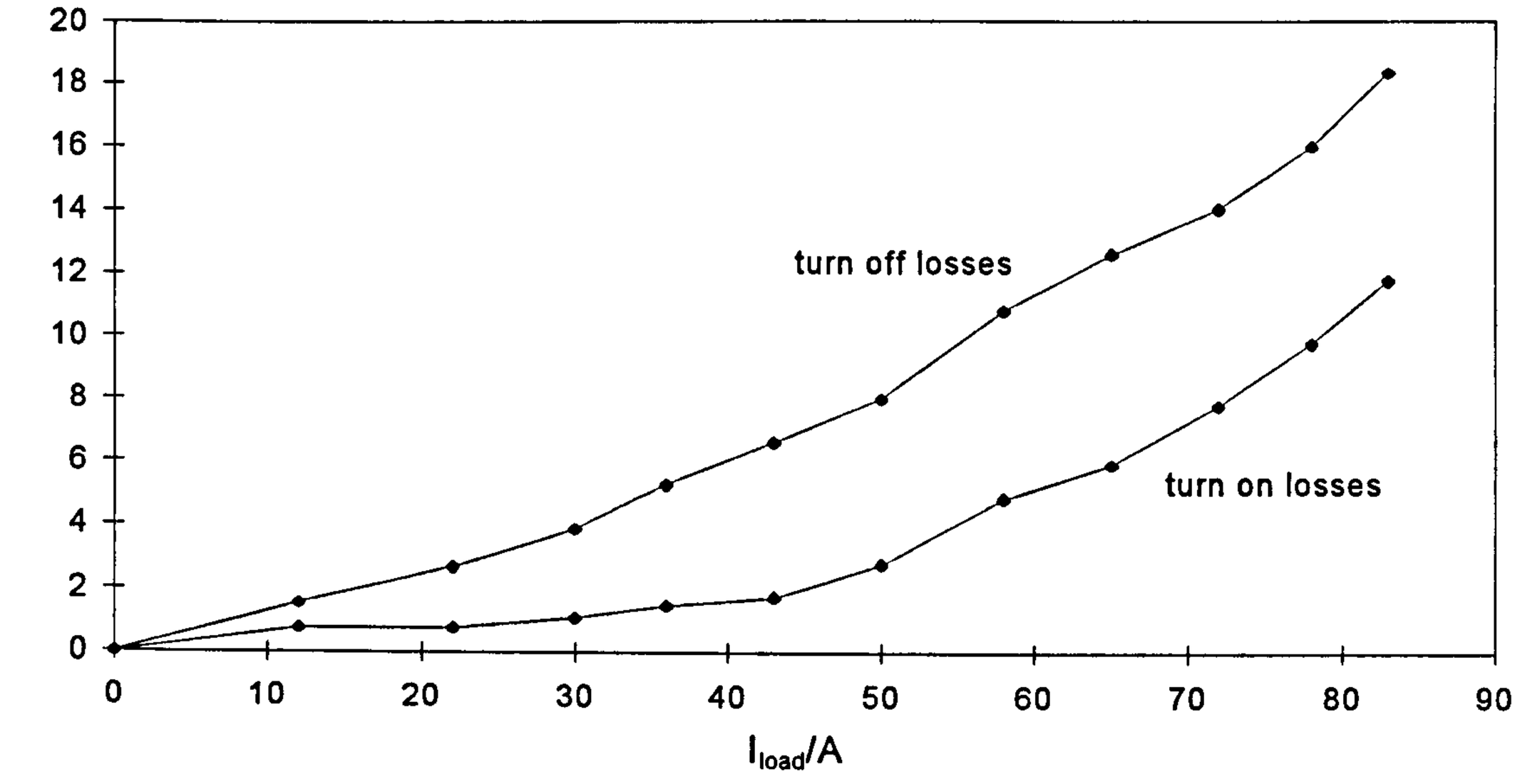


Figure 7.3.1: Turn-on and turn-off losses of the hardswitching converter

In comparison to the hardswitching losses Figure 7.3.2 shows the softswitching losses of the main switches using 20nF resonant capacitors. In average the turn-off losses are reduced to 50% and the turn-on losses by 66%. Again turn-off losses are higher than turn-on losses.

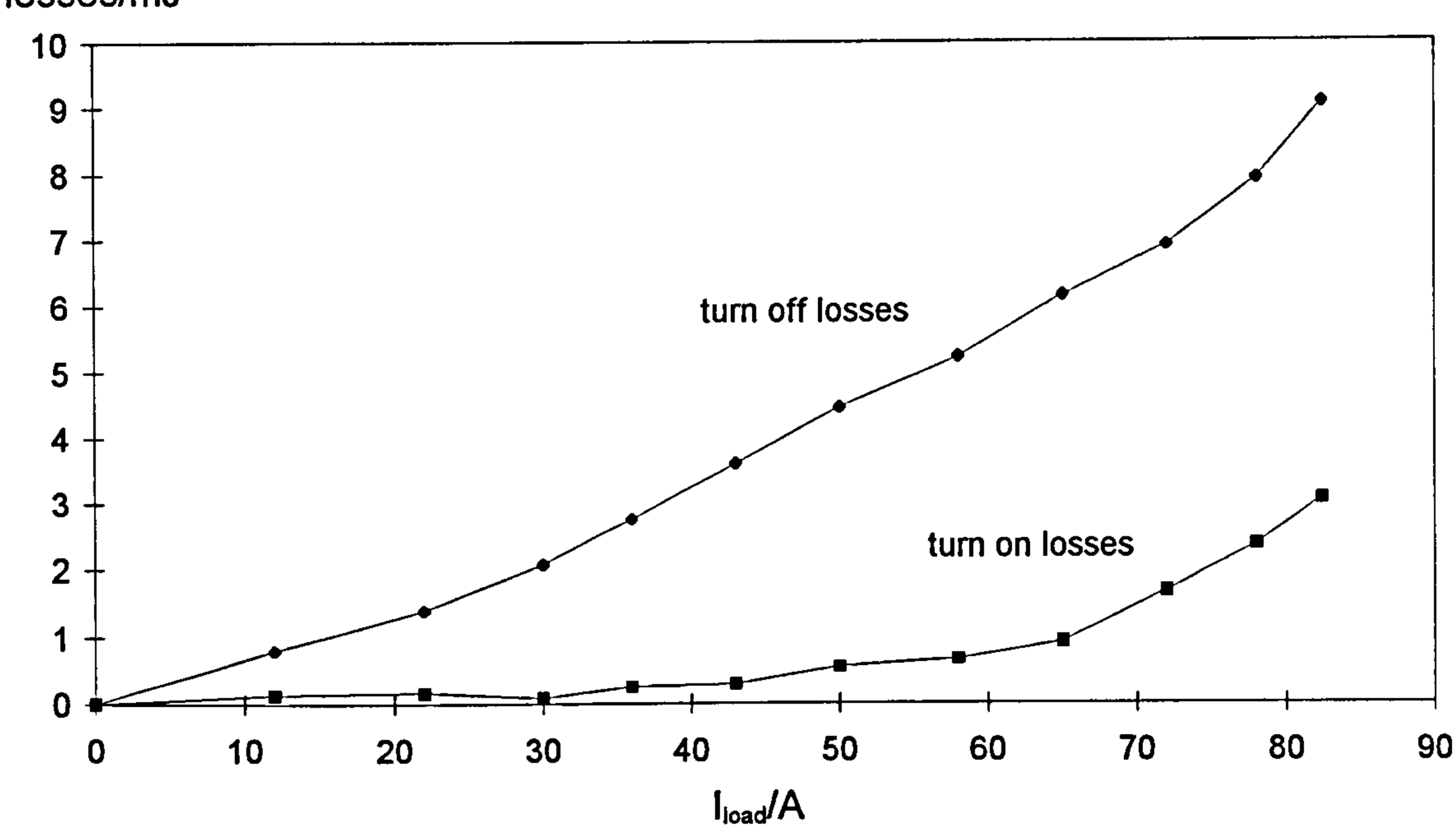


Figure 7.3.2: Turn-on and turn-off losses of the main switches of the ACPI

Beside the switching losses shown in Figure 7.3.2 the losses in the auxiliary circuit must be taken into account. Figure 7.3.3 shows the auxiliary losses when commutating from IGBT to diode and Figure 7.3.4 shows the auxiliary losses when commutating from diode to IGBT. Both figures include switching losses and conduction losses of the auxiliary IGBTs, the auxiliary diodes and the inductor. When comparing both figures one can see that the auxiliary losses occurring during the commutation Diode-IGBT are much higher than those occurring during the commutation IGBT-Diode.

Figure 7.3.3 shows that the inductor losses decrease with higher load current. This is because energy needed for pole commutation is diverted from the stored energy in the resonant inductor (resonant circuit) to the load current (snubber mode). This can be explained if it is realised that the resonant mode is basically a superposition of resonance (because of the resonant inductor and the resonant capacitors) and snubber effect (because of the resonant capacitors, which behave like snubber capacitors in this configuration (see Appendix C and section 3.3.3)). To achieve a resonant transition time that is relatively insensitive to load current levels a high resonant boost current is required. In this case the stored energy in the inductor controls the speed of commutation. At high load current the snubber effect dominates and commutation time is short. It is even possible for the load current to be so high that a

boost current is not needed for commutation. In this case the auxiliary device can turn-on at the same time as the main device turns off (direct resonant mode) [7.1].

Figure 7.3.3 shows also the losses of switch AS2 are higher than the losses of AS1 because conduction and switching losses of the IGBT of AS2 outweigh the conduction losses of the diode of AS1. Both losses are independent of load current because of the fixed boost current and resonant current.

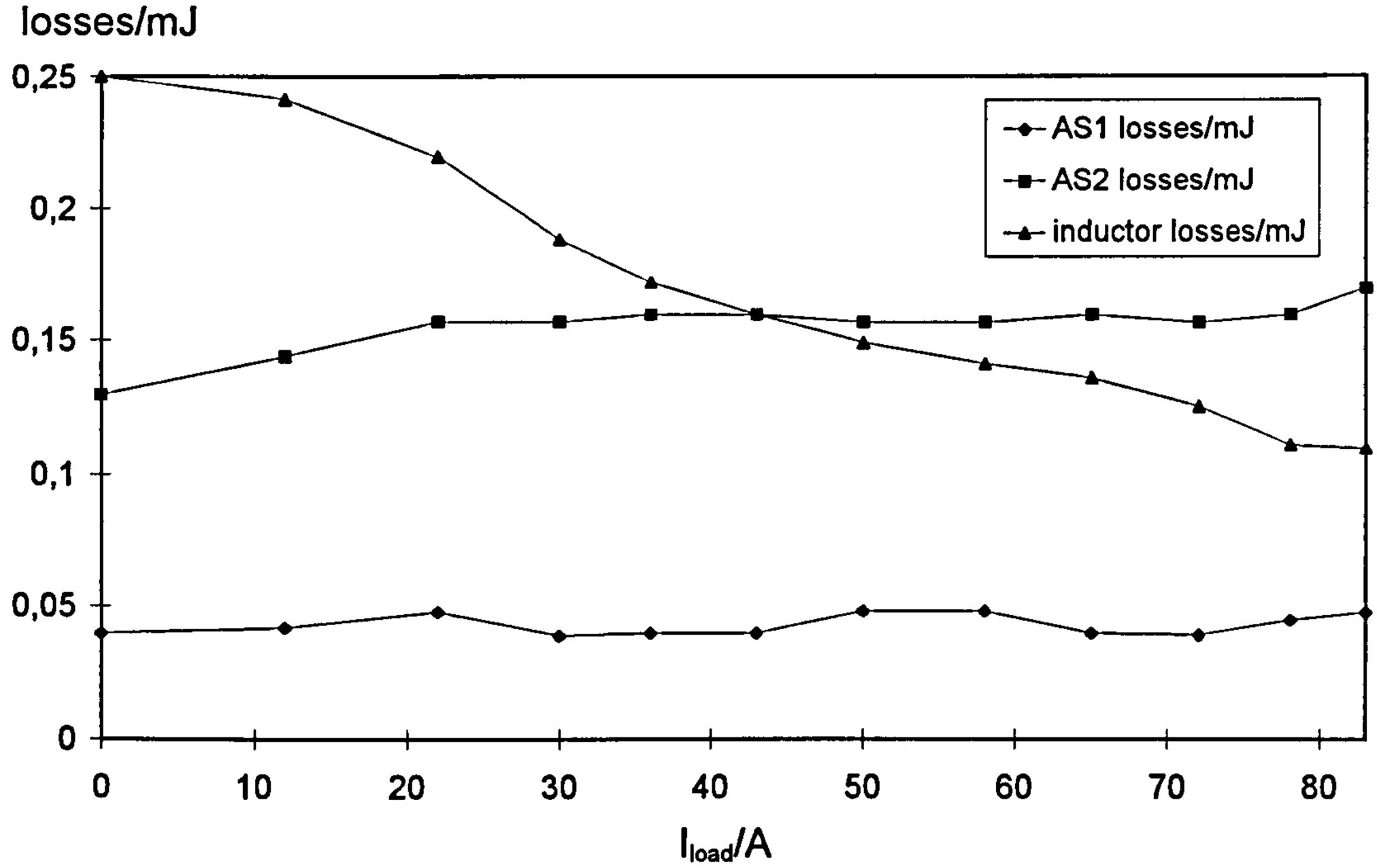


Figure 7.3.3: Losses in the auxiliary circuit during commutation IGBT-Diode

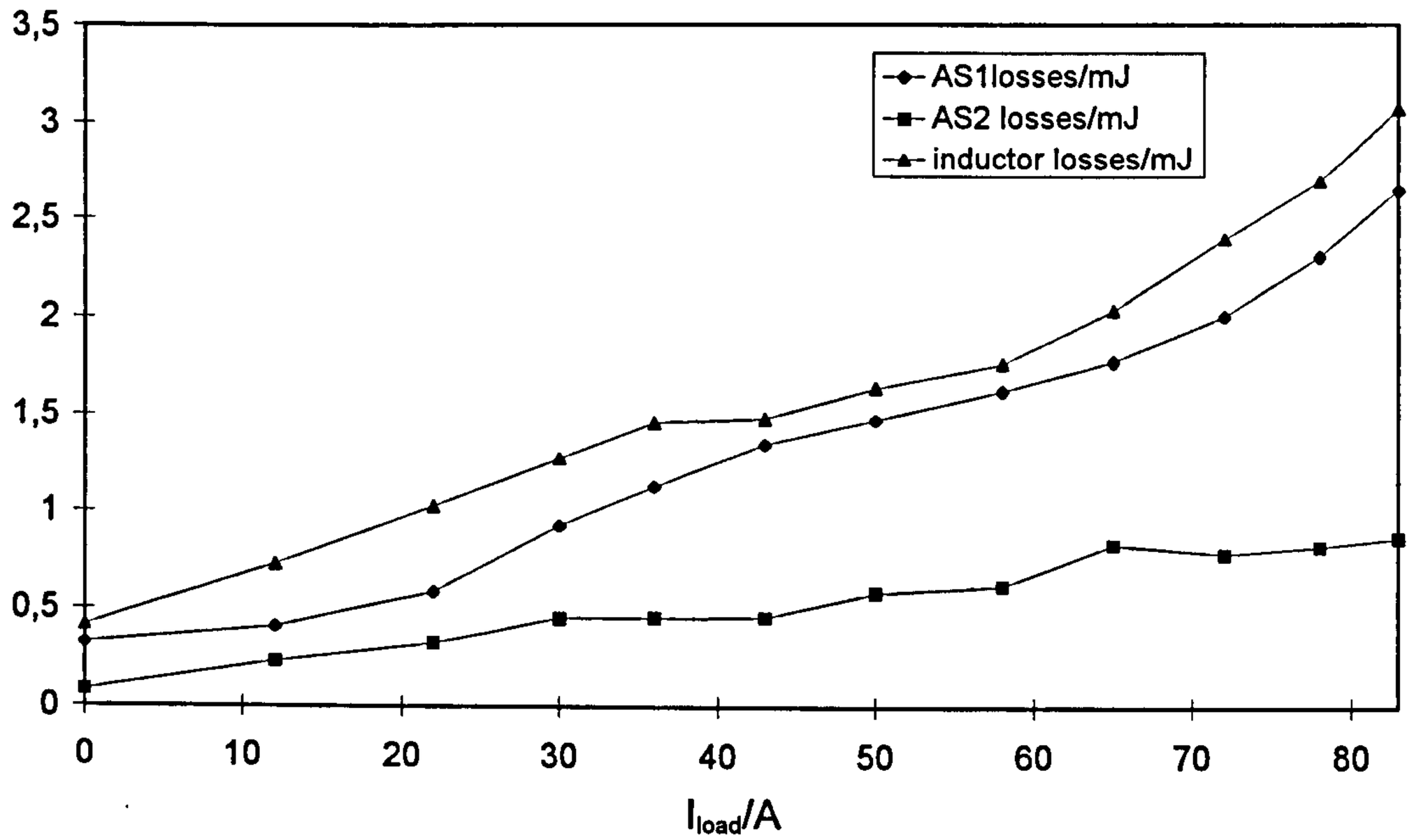


Figure 7.3.4: Losses in the auxiliary circuit during commutation Diode-IGBT

Figure 7.3.4 shows that the losses of the auxiliary switches and inductor losses increase with growing load current. The inductor losses dominates because both ramp and boost modes are active, resulting in a relatively high level of inductor current compared to the IGBT-Diode combination. The losses of switch AS1 are higher than the losses of AS2 because the IGBT of AS1 is switching and conducting, whereas only the diode from AS2 is conducting.

Figure 7.3.5 shows the superposition of the values given in Figure 7.3.3 and 7.3.4 and clearly demonstrates that the commutation process Diode-IGBT dominates.

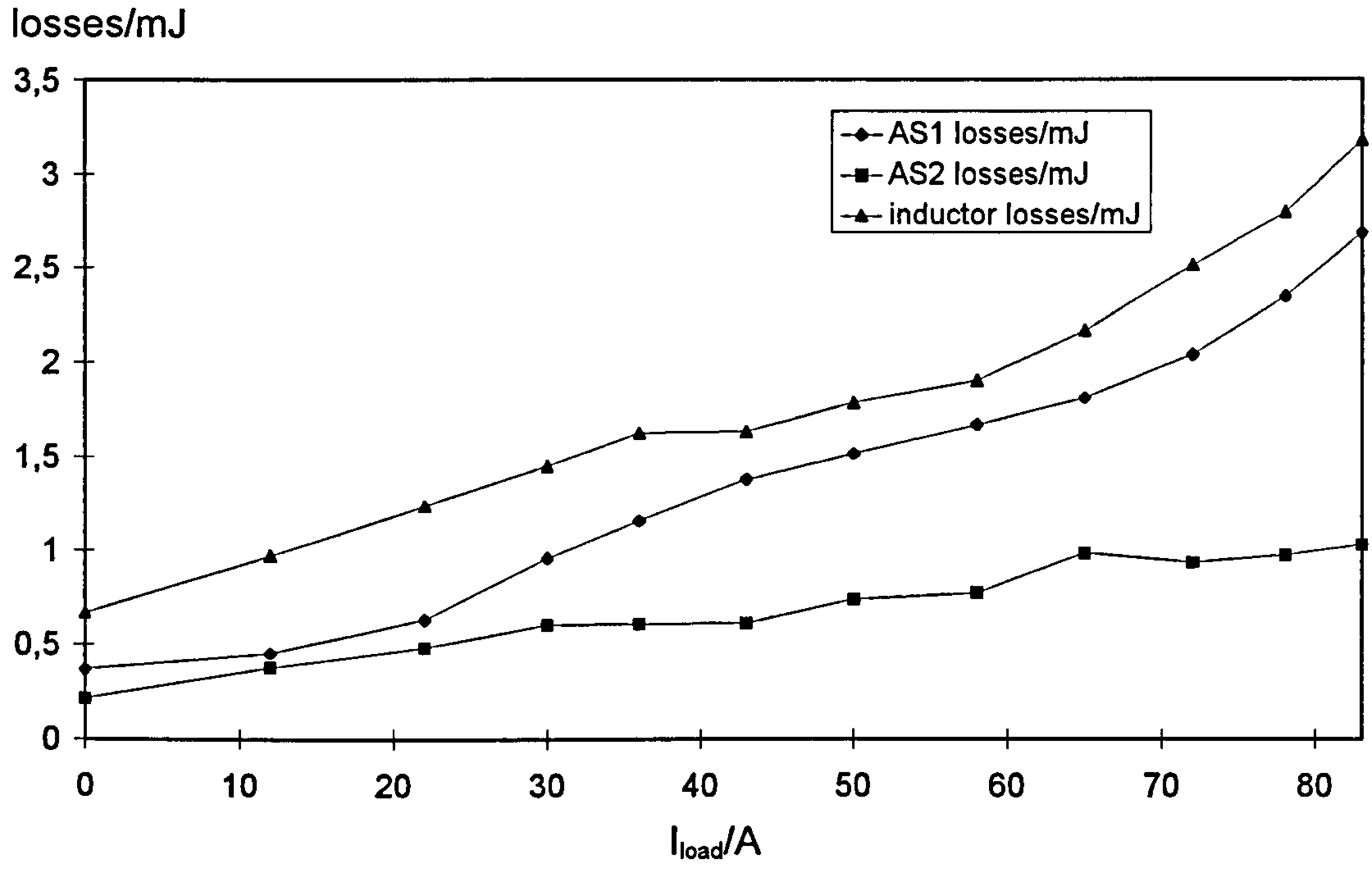


Figure 7.3.5: Overall losses of the auxiliary circuit in one modulation period

Finally Figure 7.3.6 shows the overall comparison of the losses and includes data on PWM control range (%PWM), dv/dt stress, resonant peak current and resonant time. At light load conditions the losses of the ACPI are higher compared to the hard switched converter, because of the additional auxiliary losses. With increasing load current the ACPI becomes more advantageous from the viewpoint of losses. A comparison between the ACPI with 20nF and 67nF resonant capacitors show little difference in the overall losses. This is largely due to the fact that reduced losses in the main switches are compensated by increased conduction losses in the auxiliary switches and resonant inductor. A higher value of inductance would enable reduced losses to be achieved at C=67nF at the expense of a further reduction in PWM controllability. Figure 7.3.6 shows in addition that the degree of PWM controllability decreases with larger resonant period but cuts down the dv/dt stress across the devices. The 20nF capacitor gives the same degree of PWM controllability as the hard switched converter, but reduces the dv/dt stress.

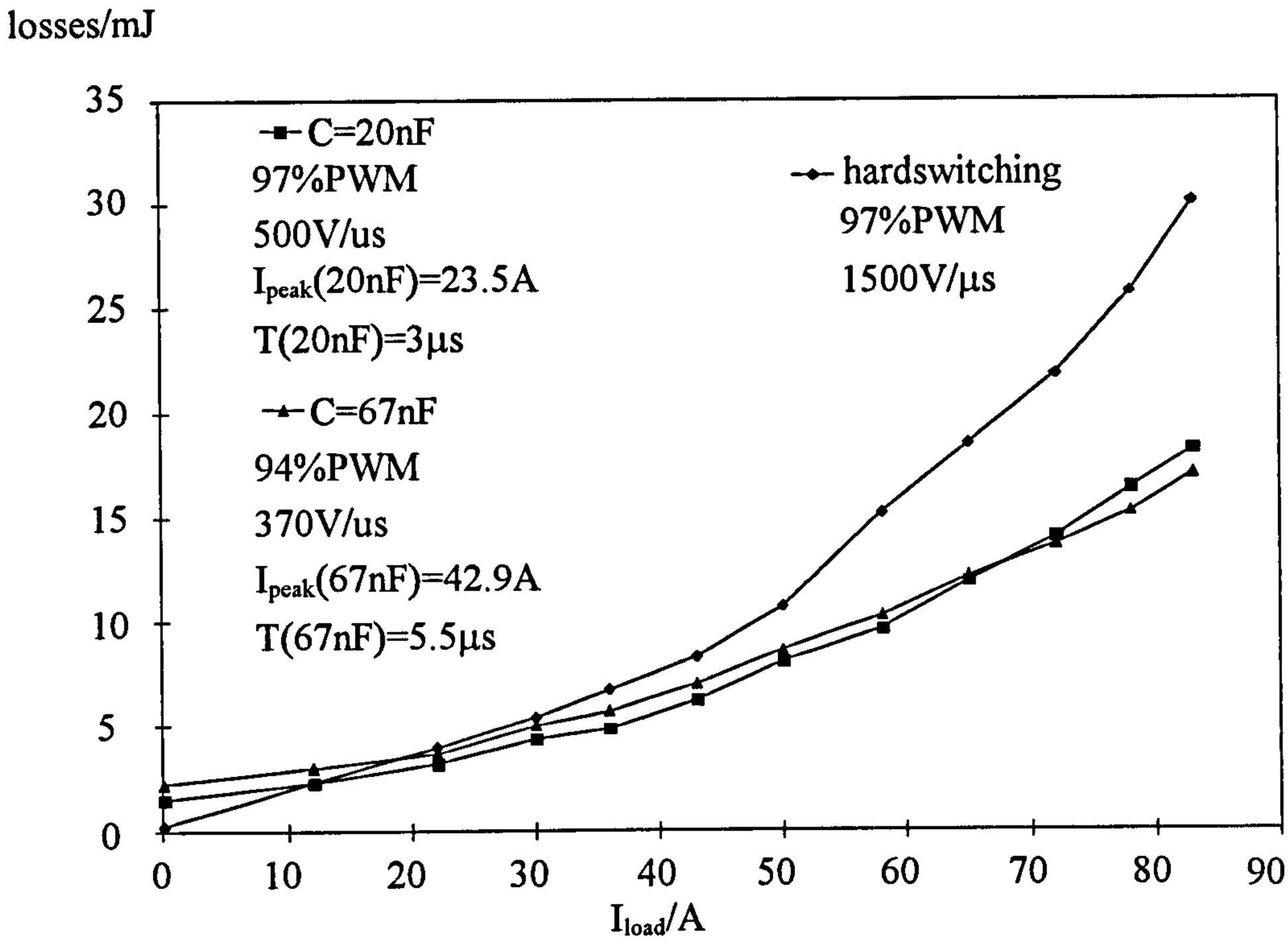


Figure 7.3.6: Overall losses of hard switched converter and ACPI in one modulation period

7.4 Measured and calculated Voltage and Current Output Spectra

Before starting to discuss the results of the output spectra it is important to describe the steps that lead to the results first.

200000 data points have been captured for each measurement of the output spectra. The output frequency was set to 50Hz. That is equal to a time period of 20ms. 200000 data points for 20ms results in a minimum time step of 100ns. Thus the turn-on and turn-off process of the switches could be monitored for both the hard switched converter and the ACPI. The maximum frequency range of the output spectra is defined by the Nyquist criteria. With a minimum time step of 100ns the maximum frequency is 5MHz. The minimum frequency of the output spectra is defined by the output frequency of the converter that was set to 50Hz. Unfortunately the oscilloscopes that have been used in the laboratory are not able to store 200000 data points. Thus the 20ms time period was sub divided into eight zones (Zone 1 represents the data from 0ms to 2.5ms, zone 2 represents the data from 2.5ms to 5ms etc.). Therefore each measurement captures 25000 data. The data from each zone was saved on a PC and once all eight measurements had been taken, the files were linked together creating one file representing 200000 data points.

The vertical resolution is set by an analogue-digital-converter and the acquisition mode. The oscilloscope uses an eight bit converter, which means that 256 levels represent the signal amplitude. These levels are distributed over 10.24 vertical divisions. Using 1V/Div sensitivity and the 200/1 divider of the differential voltage probe, the maximum voltage is given to +/- 1024V. In the high-resolution acquisition mode of the oscilloscope the vertical resolution is increased by frequently recording the measured data and comparing the data. The increase in resolution is given by the relation between the maximum sample rate of the oscilloscope (TDS 744: 2 GSamples/s) and the sample rate applied from the user (25000 data for 2.5ms => 10 MSamples/s). This leads to additional 200 levels per division or additional 2048 levels for 10.24 divisions. Therefore the vertical resolution in total is 2304 levels (256 levels plus 2048 levels) or 11.1699 bits.

If the discretisation error is assumed to be a Gaussian white noise source of amplitude equivalent to 1 discretisation level, the 'noise floor' of the Fast Fourier Transformation (FFT) may be estimated as follows:

$$\text{Noise voltage} \approx \sqrt{\frac{\left(\frac{\text{maximum peak to peak voltage}}{\text{maximum number of levels}}\right)^2}{\text{Nyquist frequency}}} \cdot \text{FFT bin width} \qquad (7.4.1)$$

$$\text{Noise voltage} \approx \sqrt{\frac{\left(\frac{2048\text{V}}{2304}\right)^2}{5\text{MHz}}} \cdot 50\text{Hz} = 2.81\text{mV}$$

The result show that the 'noise floor' is about 2.8mV in a 50Hz bin. As seen in this section, the voltages of all voltage spectra are mostly above this value. This leads to the conclusion, that the used method of measurement is sufficiently accurate for comparing frequency spectra, even at higher frequency.

During the measurements it was important not to change the trigger level of the oscilloscope and not to change the output frequency and load conditions. In addition care had to be taken when adjusting the set-up of the oscilloscope for a new measurement. Once all data were available in one file a FFT in Matlab was taken. The results have been plotted as Bode plot (x and y axis in logarithm format) and are shown in the following.

Figures 7.4.1 and 7.4.2 show the output voltage spectrum of the phase voltage of the hard switched converter (Figure 7.4.1) and the ACPI (Figure 7.4.2) in the frequency range 10Hz to 1MHz. The peak voltage of the carrier frequency (50Hz) for the hard switched converter is 270V. That results in a RMS voltage of $V_{ph,1,rms}$=191V. The peak voltage of the carrier frequency of the ACPI is 262V leading to $V_{ph,1,rms}$=185V RMS voltage at 50Hz. The RMS voltage for hard switched and ACPI can be calculated with the help of equation 7.4.2:

$$V_{RMS} = \sqrt{\frac{1}{T_s}\int v^2(t)dt} = \sqrt{\frac{\Delta t}{T_s}\sum_{\upsilon=1}^{K} v^2(\upsilon)} \qquad (7.4.2)$$

with Δt=100ns, T =20ms, K=200000 and v(υ) representing the collected data points. This results in $V_{ph,rms}$=235V for hard switched and 231V for the ACPI. Both Figures show not much differences in the maximum peak voltages at switching frequency and its multiple. Figure 7.4.2 shows in addition periodic voltage peaks in the output spectra commencing at 200kHz. These peaks result from the natural frequency of the auxiliary circuit.

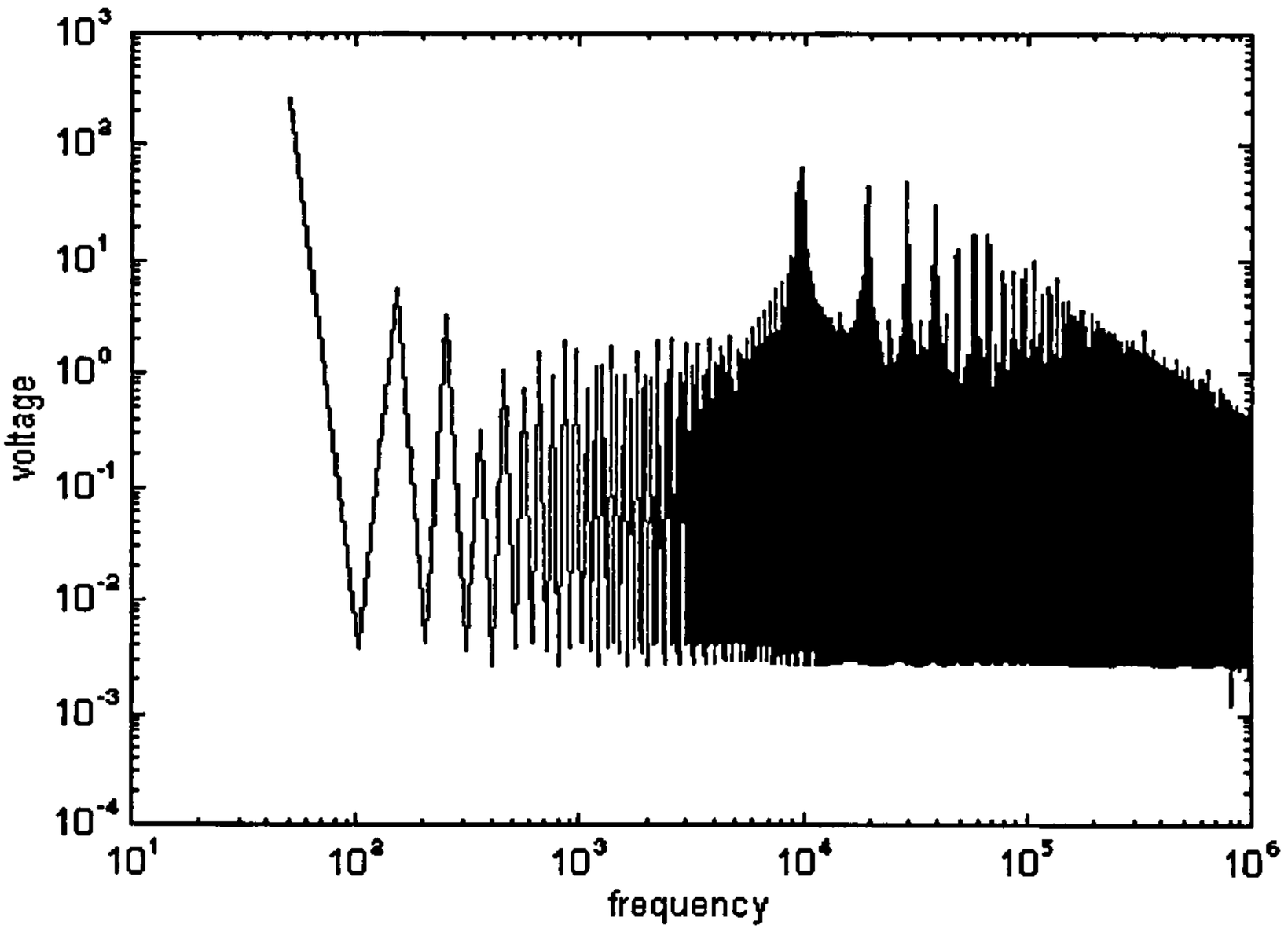


Figure 7.4.1: Phase output voltage spectrum (hardswitching converter)

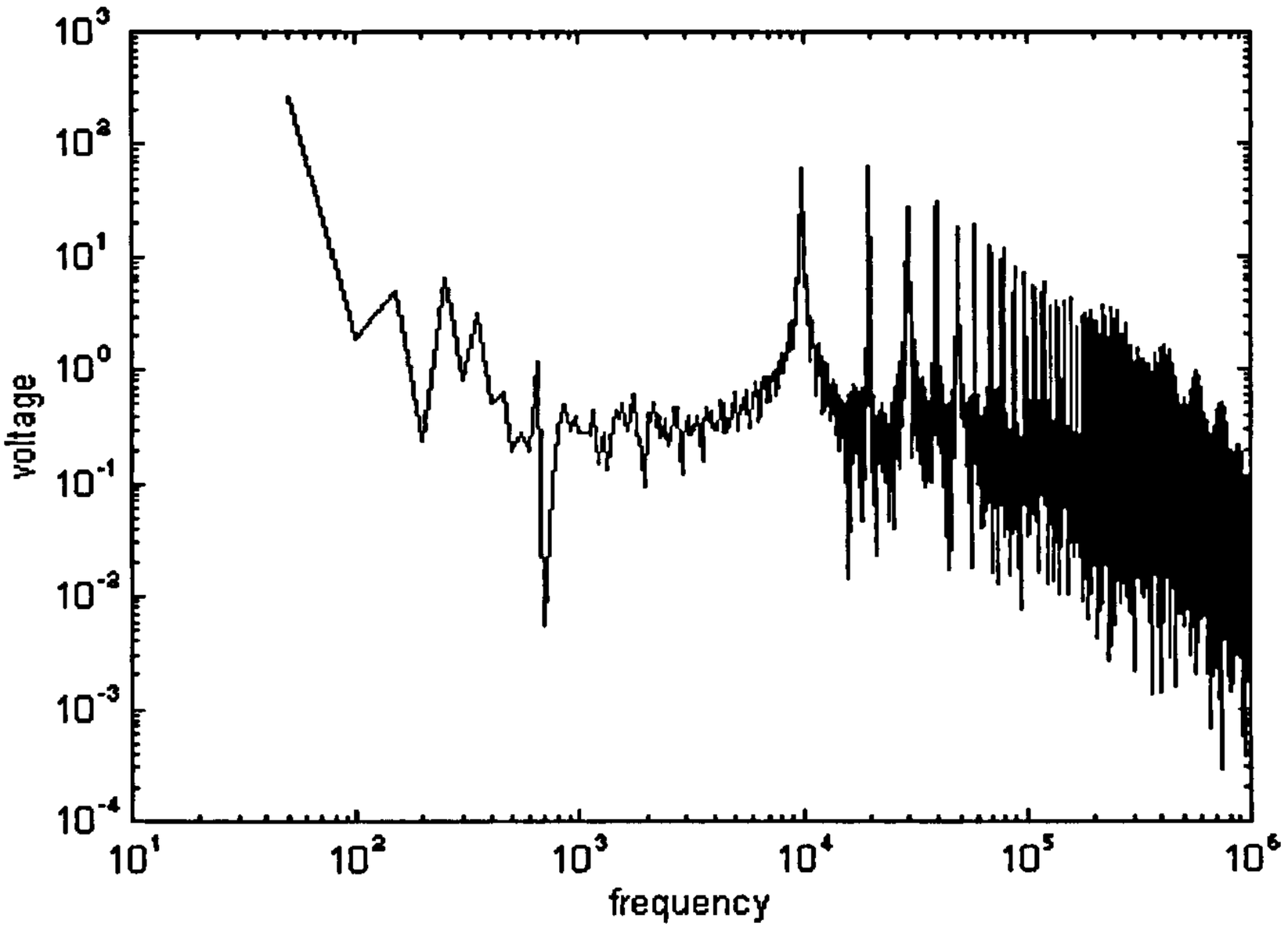


Figure 7.4.2: Phase output voltage spectrum (ACPI)

Figure 7.4.3 and Figure 7.4.4 show the output spectra of the line-to-line voltage. The RMS line-to-line voltages of the hardswitching converter is 401V and 321V at 50Hz, compared to 399V and 322V at 50Hz of the ACPI. Again the peak values at the multiple of the switching frequency are similar. Figure 7.4.4 shows the same periodical voltage peaks as Figure 7.4.2.

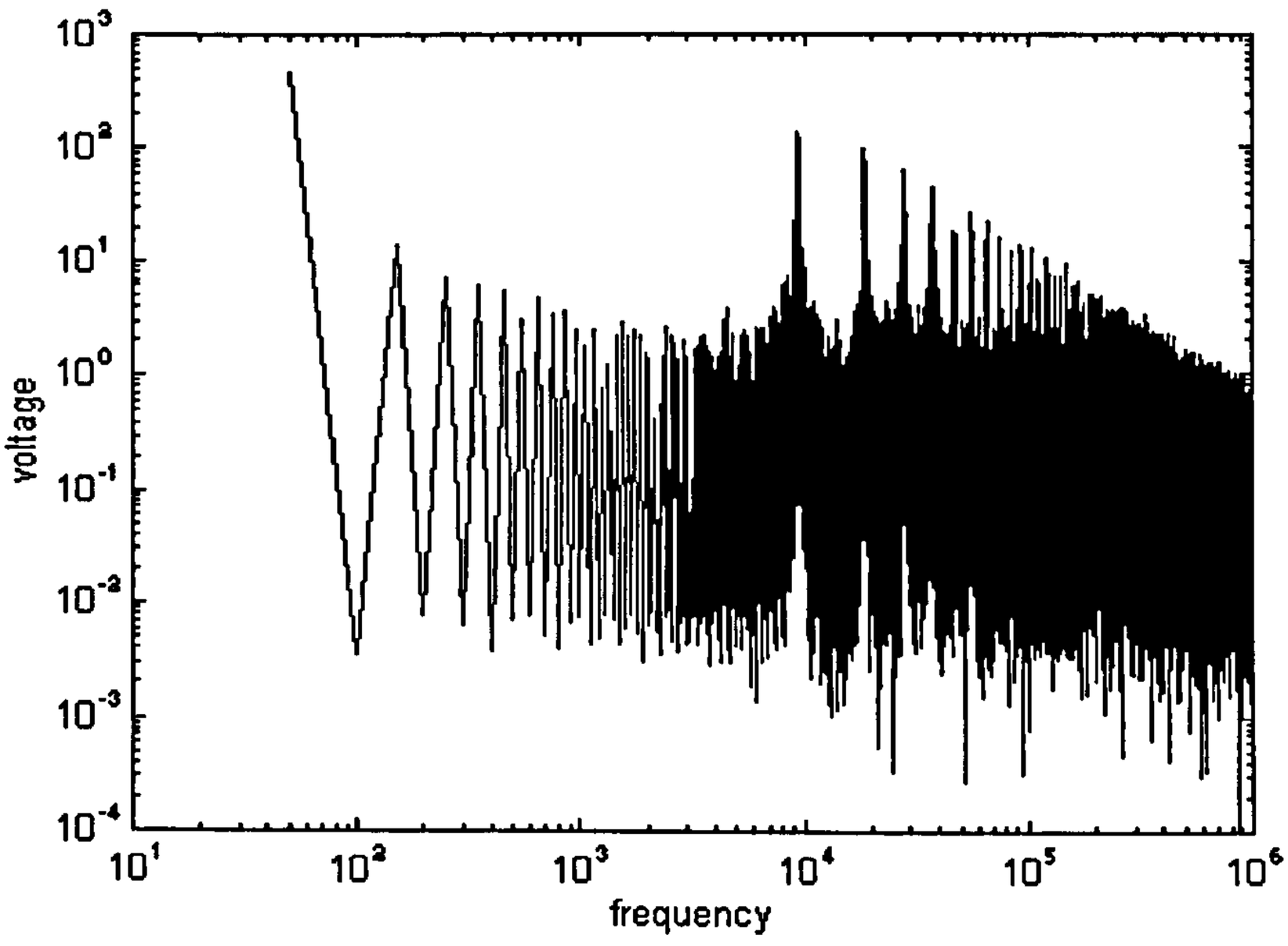


Figure 7.4.3: Line-to-line output voltage spectrum (hardswitching converter)

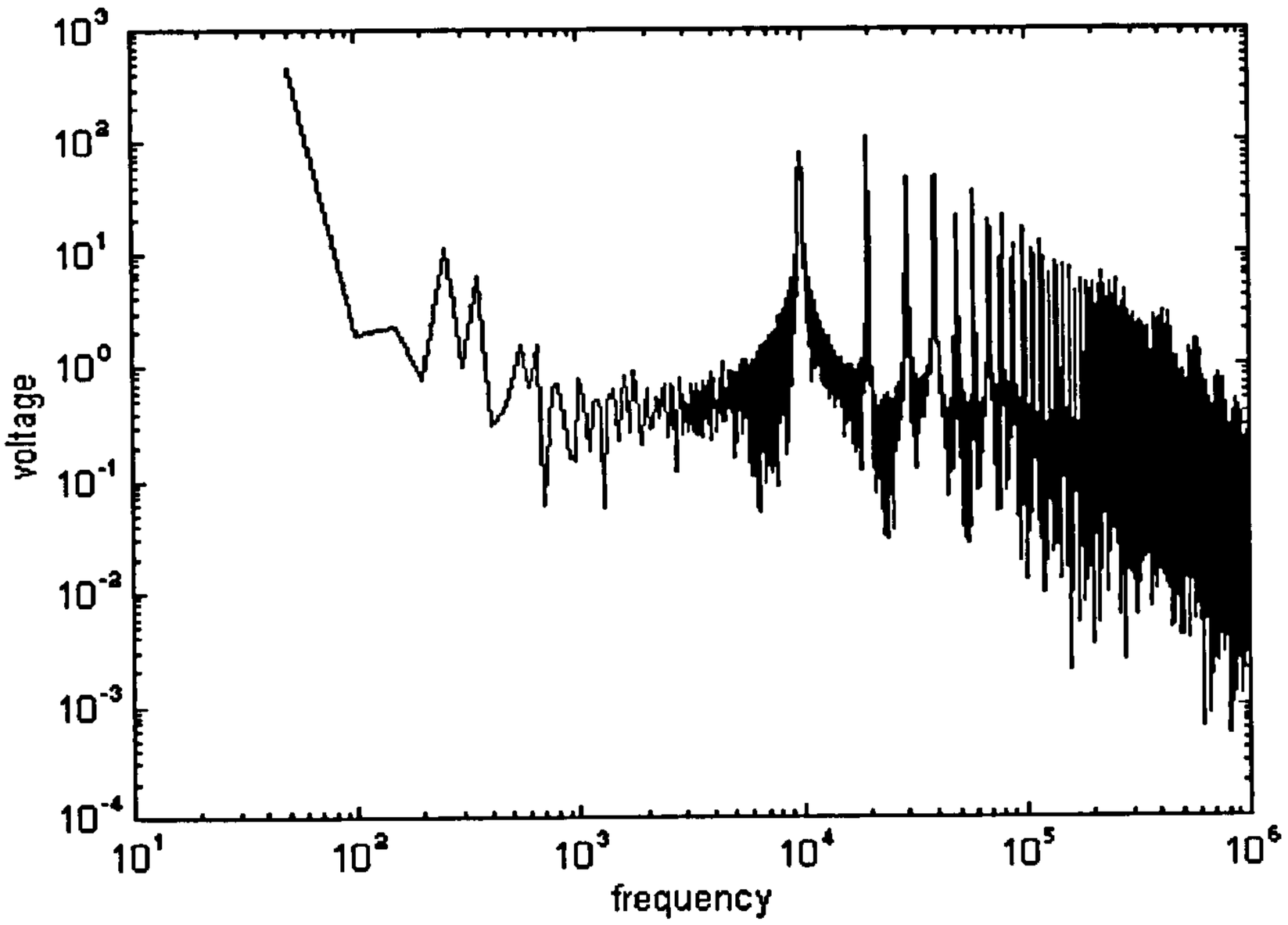


Figure 7.4.4: Line-to-line output voltage spectrum (ACPI)

Figures 7.4.5 and 7.4.6 show the output spectra of the phase output voltage in the frequency range between 1MHz and 5MHz. The figures show that the noise level of the ACPI is lower than that of the hardswitching converter. The maximum peak voltages of the hardswitching converter are not below 0.08V whereas the majority of peaks of the ACPI are below this value. In the frequency range between 1MHz and 2MHz the ACPI shows still the periodical voltage peaks. Above 2MHz the voltage level of these peaks get smaller and the effect disappears in the output spectra.

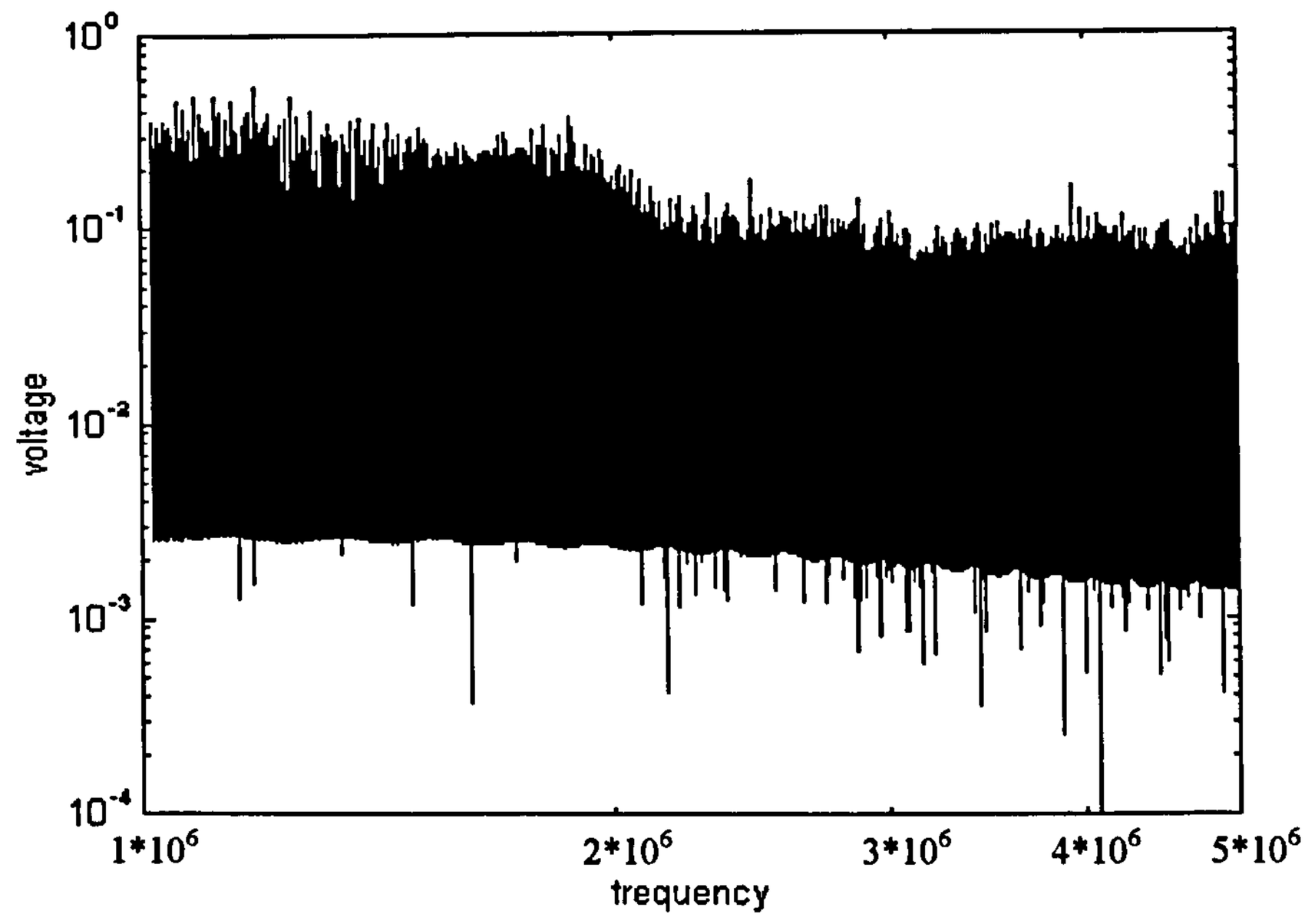


Figure 7.4.5: Phase output voltage spectrum (hardswitching converter, high frequency)

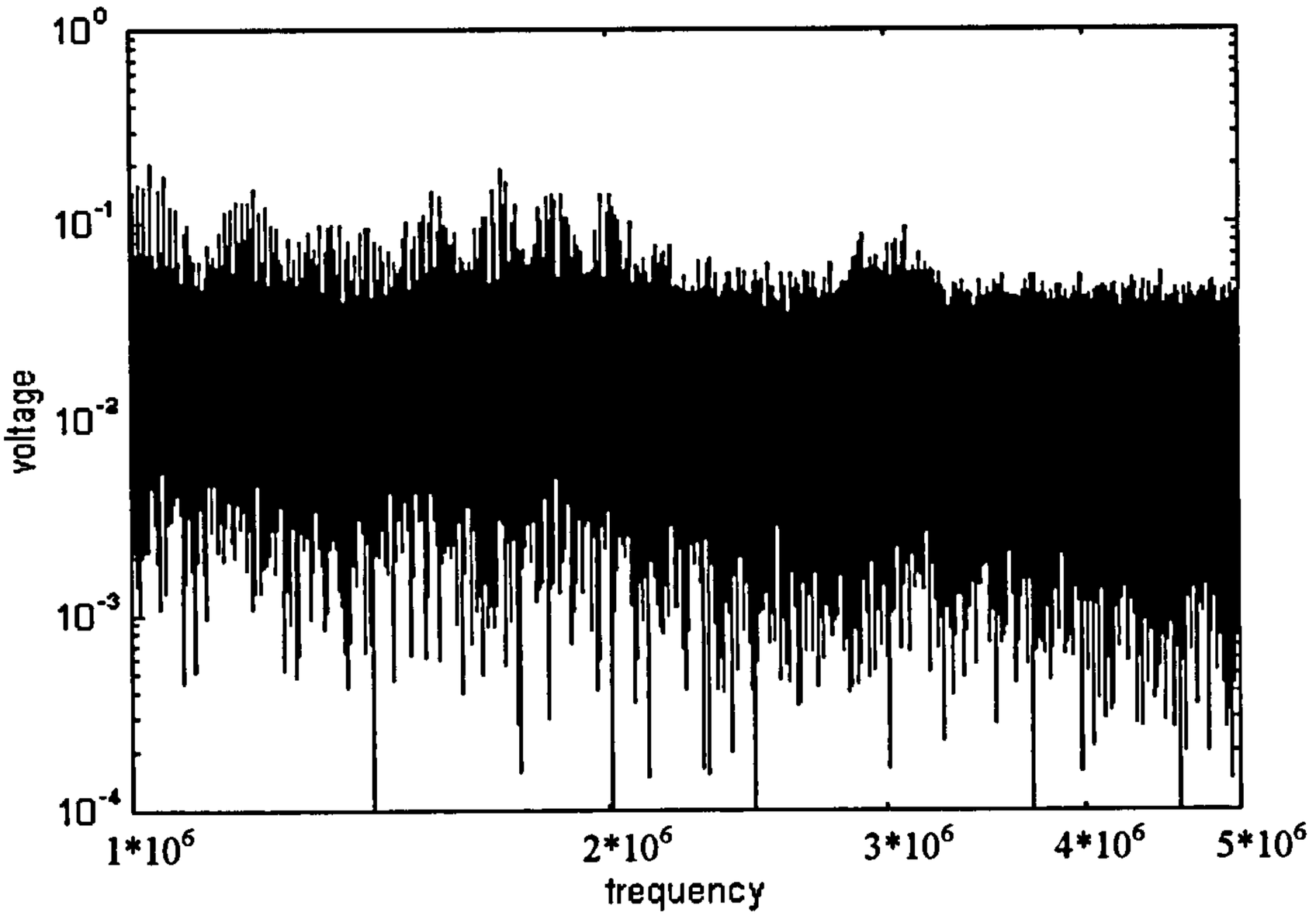


Figure 7.4.6: Phase output voltage spectrum (ACPI, high frequency)

The last two output voltage spectra are shown in Figure 7.4.7 and 7.4.8. Both spectra represent the line-to-line voltage in the frequency range from 1MHz to 5 MHz. Again most maximum peak values of the ACPI are lower when compared to the hard switched converter.

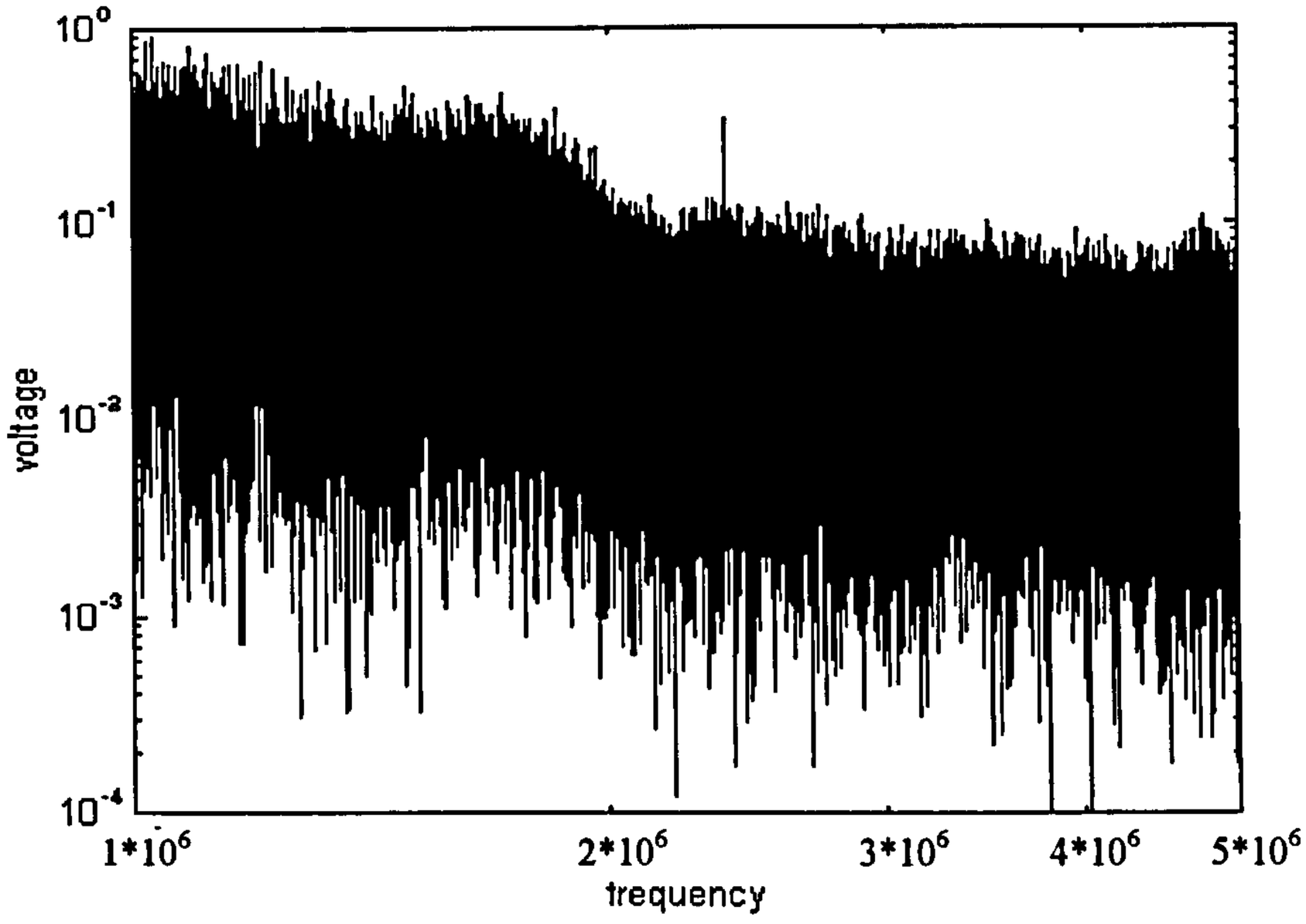


Figure 7.4.7: Line-to-line output voltage spectrum (hardswitching converter, high frequency)

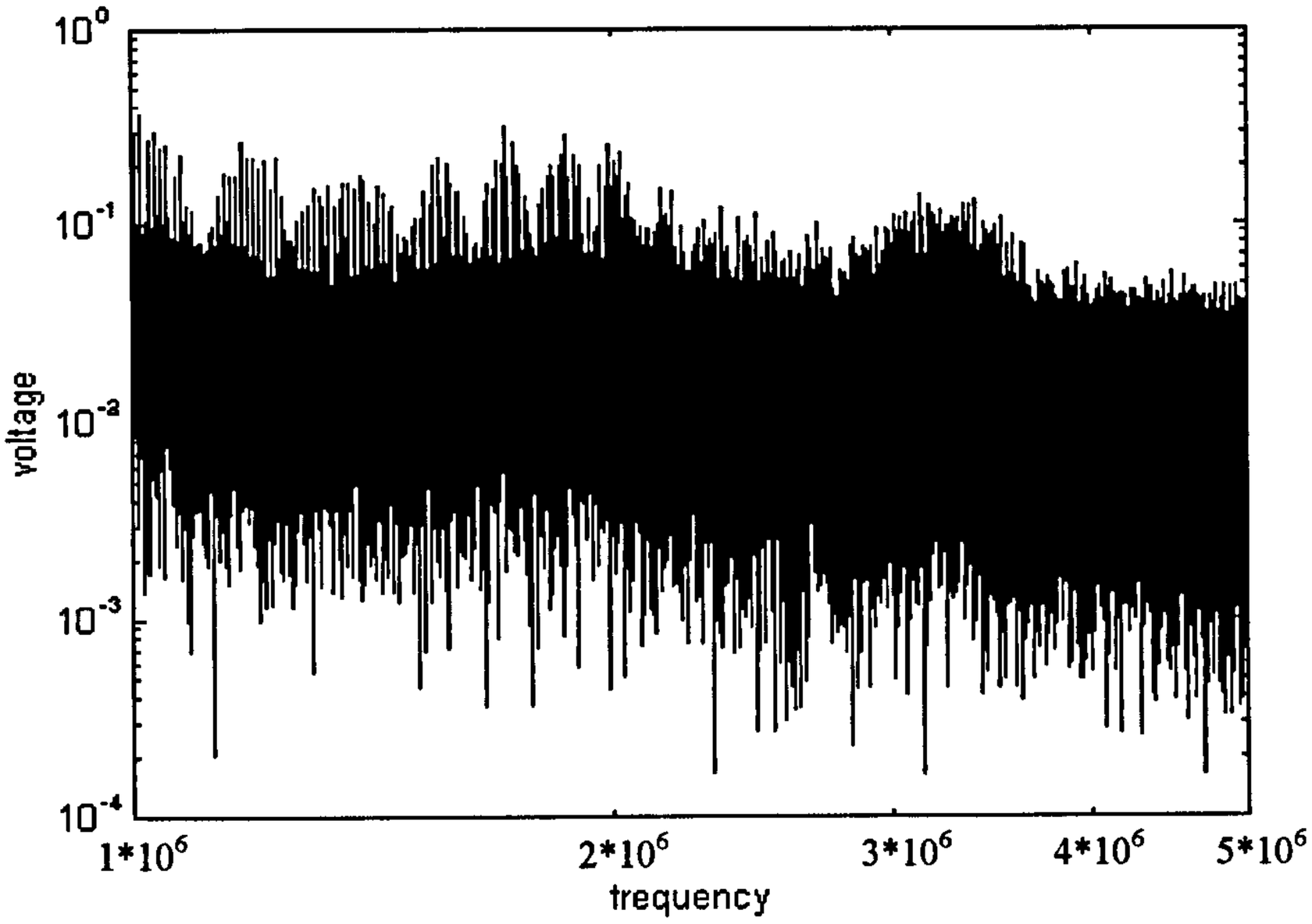


Figure 7.4.8: Line-to-line output voltage spectrum (ACPI, high frequency)

Figures 7.4.5 to 7.4.8 show a reduction in noise of the ACPI in the frequencies above 1MHz. Between 10Hz and 1MHz the output spectra looks similar. Therefore it is worth to calculate the unweighted total noise power using:

$$V_k = \sqrt{\sum_{\upsilon=n*f_1}^{k*n*f_1} v^2(\upsilon)} \qquad (7.4.3)$$

f_1 is the minimum frequency step in the output spectra (50Hz), n defines the starting point of the frequency range that likes to be investigated, k is the number of data of the investigated range. The total noise power can be used to approximate the noise energy that is stored in an investigated frequency range. The frequency range of the output spectra have been split in three parts. The frequency range 5Hz to 5kHz is captured on decade base (5Hz-50Hz, 50Hz-500Hz etc.), the frequency range 5kHz to 1MHz is captured on octave base (5kHz-10kHz, 10kHz-20kHz, 20kHz-40kHz, etc.) and the frequency range 1MHz to 5 MHz is captured on dual base (1MHz-2MHz, 2MHz-3MHz, etc.). This splitting leads to a moderate comparison of the power noise of both converters.

Figure 7.4.9 shows the total noise power of the line-to-line voltage of the hard switched and ACPI converter. As expected the noise power is lower at frequencies above 1MHz. From interest is that a reduction in noise power level starts already at around 160kHz for the ACPI. This result show that the additional voltage peaks generated from the auxiliary circuit and found in the output spectra (Figures 7.4.4 and 7.4.7) do not add substantial noise power. The ACPI shows also a reduction in noise power in the frequency range 100Hz-10kHz. Between 10kHz and 160kHz the noise of the hard switched converter is lower. That leads to the

assumption that the amplitudes of the multiple of the switching frequency (9.8kHz) and its sidebands must be higher for the ACPI than for the hard switched converter. Above around 160kHz the voltage level of the multiple of the switching frequency and its sidebands decrease.

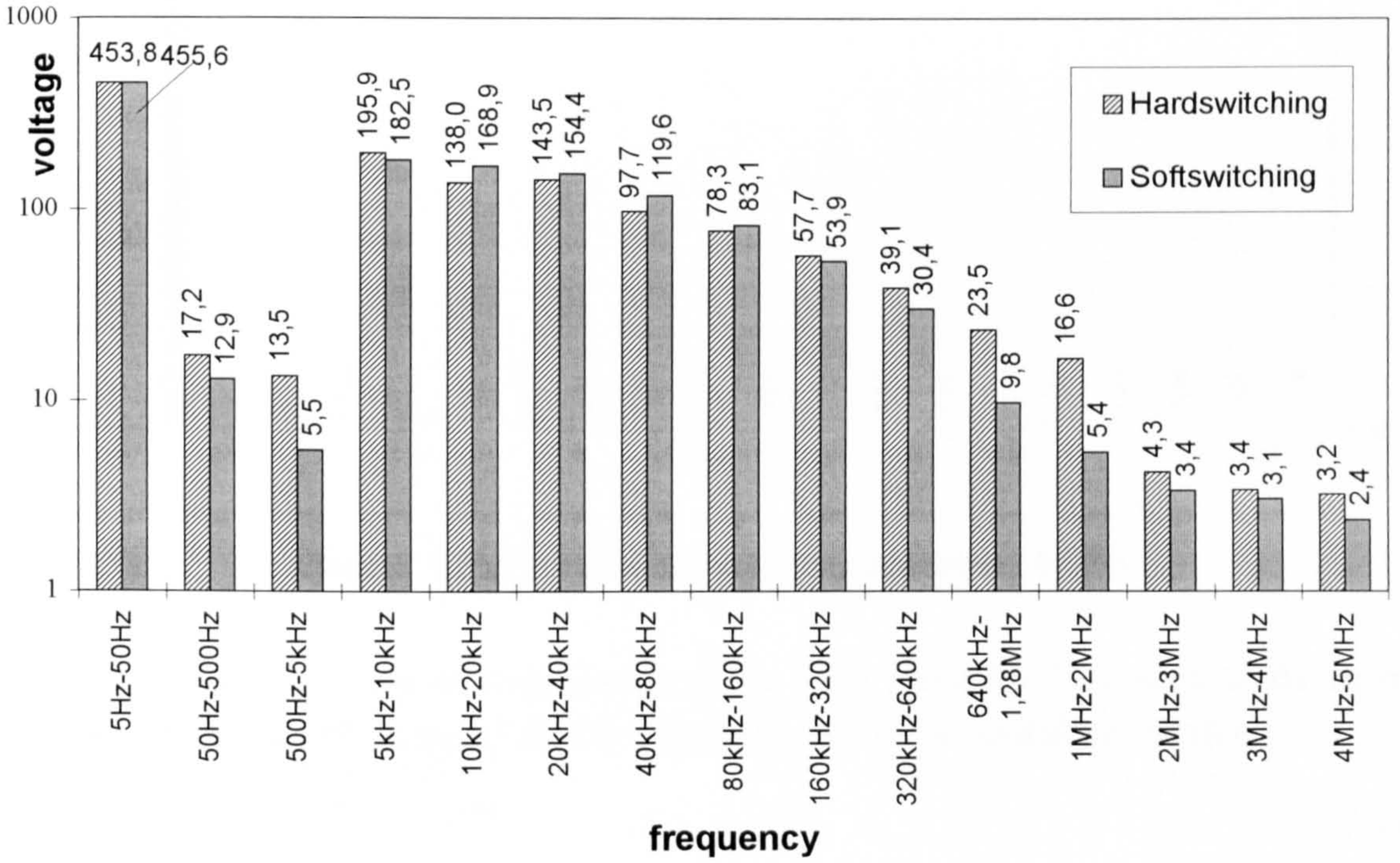


Figure 7.4.9: Total noise power of the line-to-line voltage of hard switched and ACPI converter (y axis in logarithm format, unit in volts; x axis describes different frequency ranges)

The current output spectra of the hardswitching converter and the ACPI is shown in Figure 7.4.10 and 7.4.11. When comparing the current harmonics the lower frequencies are of interest because low frequencies result in torque ripples.

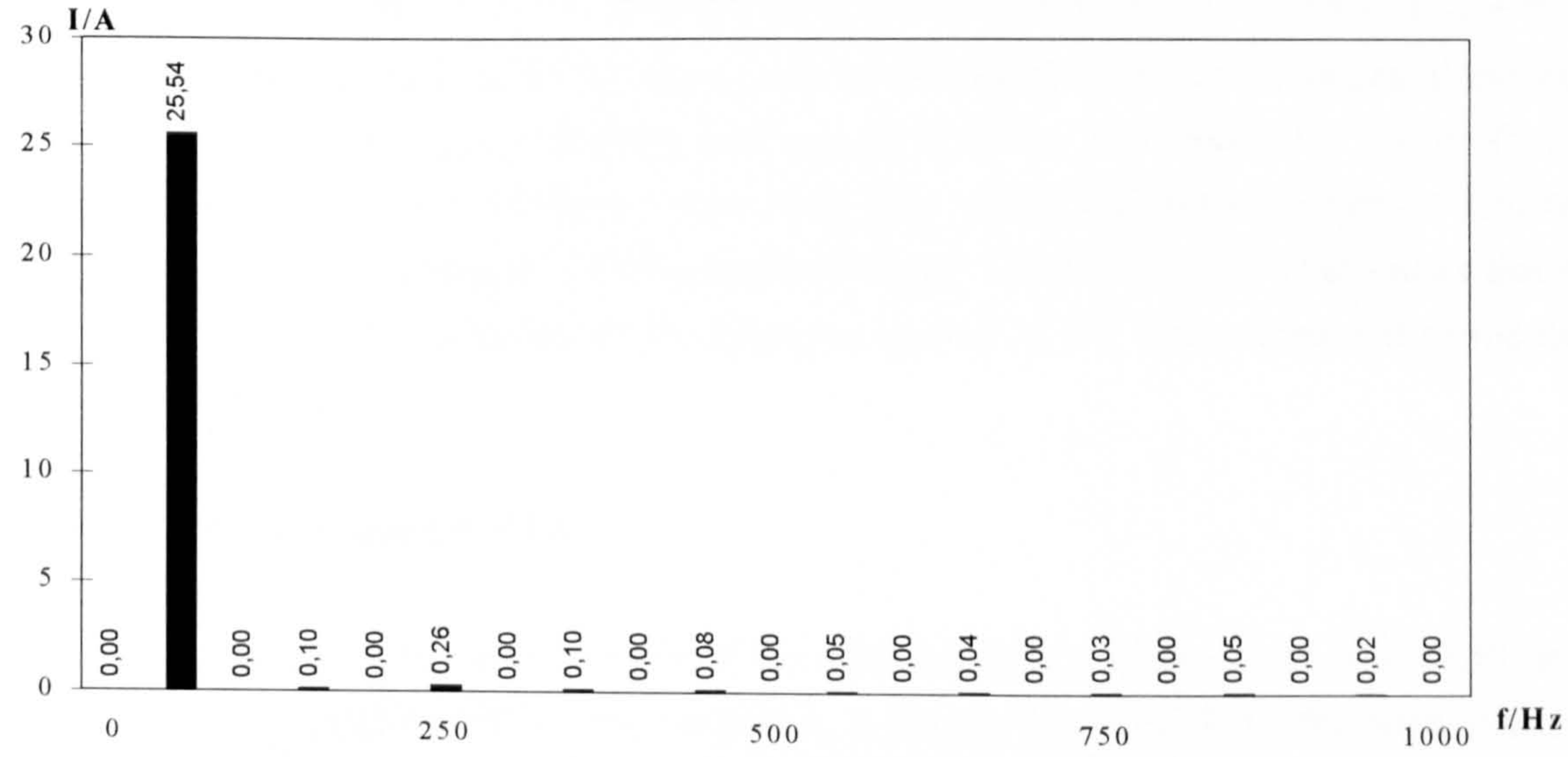


Figure 7.4.10: Phase output current spectrum (hardswitching converter)

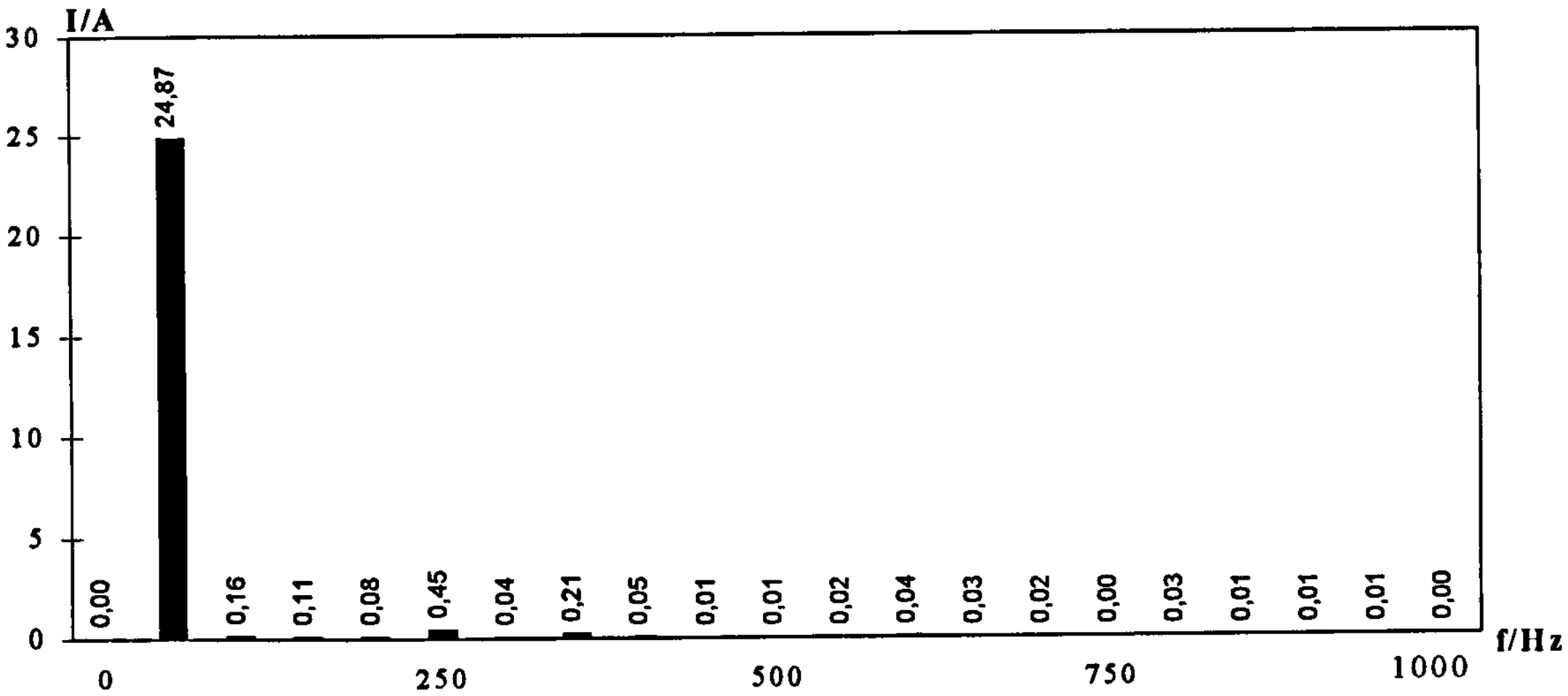


Figure 7.4.11: Phase output current spectrum (ACPI)

A useful indicator to compare both spectra is the Total Harmonic Distortion of the current (%THD$_i$). Reference [7.2] describes the equations needed to calculate %THD$_i$:

$$\%\mathrm{THD}_i = 100 \cdot \frac{\sqrt{I_{ph,rms}^2 - I_{ph,1,rms}^2}}{I_{ph,1,rms}} \tag{7.4.4}$$

$$I_{ph,1,rms} = \frac{\hat{I}_{ph,1}}{\sqrt{2}} \tag{7.4.5}$$

$$I_{ph,rms} = \sqrt{\frac{\Delta t}{T_s}\sum_{\upsilon=1}^{K} i^2(\upsilon)}\ I_{ph,rms} = \sqrt{\frac{\Delta t}{T_s}\sum_{\upsilon=1}^{K} i^2(\upsilon)} \tag{7.4.6}$$

Again 200000 data points have been captured over a time period of 20ms. Using Δt=100ns, K=200000, $\sum i^2 = 61807684{,}4A^2$ and T_s=20ms the RMS phase output current $I_{ph,rms}$ and the RMS phase output current at 50 Hz $I_{ph,1,rms}$ can be calculated. The current values of the hard switched converter are: $I_{ph,rms}$=18.064A and $I_{ph,1,rms}$=18,057A. The values for the ACPI are: $I_{ph,rms}$=17.594A and $I_{ph,1,rms}$=17.586A. From these four values and with the help of equation 7.4.4 %THD$_i$ can be calculated: 2.979% (hardswitching), 2.638% (ACPI). That shows that the current distortion of the designed ACPI decreases around 11.5% when compared to the hard switched converter.

7.5 Summary of measured Data

Table 7.5.1 compares the performances of the hardswitching converter with the ACPI at an output power of around 10kW. The reduction in losses, from 655W in the hard switched converter to 497W in the ACPI is clearly significant in terms of the power device cooling requirements. It is also significant that the total harmonic distortion content of the output

current and voltage is barely affected by softswitching control scheme (section 7.4). This demonstrates that the controller is effective in preserving the maximum degree of PWM control whilst reducing switching losses and output dv/dt.

	HARDSWITCHING	**SOFTSWITCHING**
load values (phase)	R=10,2Ω, L=10mH	R=10,2Ω, L=10mH
dc-link input power	10455W	9726W
output power	9800W	9229W
efficiency	93,73%	94.73%
converter supply frequency	50Hz	50Hz
output frequency	50Hz	50Hz
inverter switching frequency	9.8kHz	9.8kHz
RMS line-to-line input voltage	240V	240V
RMS phase output current	18.064A	17,594
RMS phase output current at 50Hz	18.057A	17,586
%THD$_i$	2.979%	2,638%
RMS phase output voltage	234,95V	230,59V
RMS phase output voltage at 50Hz	191.46V	185,4V
RMS line-to-line voltage	400.76V	399,13V
RMS line-to-line voltage at 50Hz	320.87V	322,12V
amplitude modulation index	0.98	0,95
max. commutation delay time	2μs	3,5μs
average output dv/dt	1500V/μs	500 V/μs

Table 7.5.1: Comparison of performances of ACPI (C_r=20nF) and hard switched converter

Chapter 8

CONCLUSIONS

The work presented in this thesis provides a comprehensive and critical assessment of novel converter topologies for controlling electrical machines with power ratings up to 100kW. A mixture of theoretical work, simulation and experimental work has been used to investigate all of the major classes of softswitching converter topology. For each class of topology, the mode of operation has been studied and fundamental performance limitations have been identified. The results of the studies have, for the first time, allowed a critical assessment and comparison of the many softswitching topologies to be presented in a coherent form. From this comparison one softswitching topology, the Auxiliary Commutated Resonant Pole Converter (ACPI), has been identified as the most promising novel topology. Experimental results from a 20kW ACPI, employing a unique sensorless DSP controller, have been presented and compared with results from an equivalent hard switched converter.

8.1 Overview of Novel Converter Topologies

A detailed survey of softswitching voltage source inverter topologies, suitable for induction motor drives applications, has been presented. Distinguishing operational features have been identified and used to construct a family tree encompassing all known softswitching converter types. Converter types which employ large number of devices (e.g. ac-link and direct AC-AC converter) have been identified as unattractive, because of the high initial cost.

Simple sub-topologies of the remaining softswitching dc-link topology, employing a minimum number of components are found towards the top of the family tree. Such converters operate in almost continuos resonance and are characterised by high peak current and voltage stress coupled with no PWM control. Derived topologies, employing auxiliary circuits, operate in a quasi-resonant mode and display PWM control. Here, the peak levels of resonant current are determined by the desire to render the resonant transitions insensitive to changes in switching state and load current.

The majority of topologies based on the resonant pole concept benefit from completely independent control over each leg. The use of three separate resonant circuits, each with its own circuitry does however, incur a severe cost penalty.

8.2 Assessment of Novel Softswitching Converter Topologies

For resonant dc-link schemes, only those converters which are PWM control compatible are likely to gain acceptance. Thus only PRDCL or q-RDCL topologies are seen to be attractive. The requirement to resonate the link voltage to zero at every inverter state transition depresses the average converter output voltage and limits the resolution of any applied PWM scheme for PRDCL topologies. To reduce the number of link transitions, resonant capacitors are placed across each switch, allowing a passive or "snubber" mode of operation. In this way, depending on the load current magnitude and direction, the resonant circuit does not always need to be activated. One drawback of using the snubber mode is that under light load conditions the commutation time increases unacceptably. Another suggestion for reducing the number of link transitions is the use of modified PWM control (mPWM), however the control schemes reduce output current quality. Q-RDCL topologies avoid the output voltage depression associated with PRDCL topologies by allowing the output voltage level to rise above the DC link level in a controlled manner. With this technique, the average output voltage is directly controlled by the switch duty ratio as it is in the hard switched converter. Finally, most of the PRDCL and q-RDCL topologies use pre-charged clamp capacitors, whose charge level can be difficult to control.

For all soft switched converters, it has been shown that the softswitching control fidelity is related to the ratio of the resonant transition time, to the characteristic carrier lifetime of the power semiconductor switches and, hence, to their voltage blocking capability. Regrettably, when conventional space-vector PWM control is employed, the finite transition period serves to limit not only the PWM range but also the PWM resolution. In addition, for PRDCL and q-RDCL topologies, the common resonant link means that all output phases see an increased number of voltage transitions with important consequences for output filter design or motor losses.

PCIs have the advantage of utilising a separate resonant circuit for each pole and do not suffer from the restricted PWM resolution and output voltage distortion encountered in RDCL designs. RPI topologies do, however, suffer from high resonant inductor losses and a limited PWM control range. The ARPI topology, on the other hand, uses a quasi-resonant technique to minimise inductor losses and displays an improved PWM control range. The largest PWM control range of all softswitching topologies is found in the ACPI topology. It does, however, have a high component count and is, therefore, relatively expensive when compared with hard switched converters.

The results of the assessment show the ACPI to be most promising topology, offering a high degree of PWM control without excessive device stress and the potential to operate at switching frequencies far above the normal hard switched limit without significant degradation of its control characteristics.

8.3 Improvement of the ACPI Topology

Compared to hard switched topologies, the ACPI topology seems to be unattractive because of its high initial cost. To bring down the cost two options are possible. Firstly a reduction in the number of sensors and secondly integration of some or all of the discrete devices into one or more power modules.

Work in this thesis has focused on reduction of sensors, with the help of a digital signal processor (DSP) and field programmable array (FPGA). Both devices are implemented in the controller, which requires only the load current and dc reservoir capacitor voltages as inputs. The cost of the control elements for the ACPI is thus reduced to a level comparable with that found in most state-of-the-art hard switched drives.

A performance comparison has been made with hard switched inverter at 10kW level (both converters are rated to 20kW). At this power level the results show reduced overall losses and reduction in output dv/dt stress over nearly the whole frequency spectrum without significant degradation in output current fidelity.

The lack of additional sensors and integration of control functions into the DSP provides a cost-attractive solution for drives systems, particularly where a DSP is already used to provide motor control functions. However, it is not clear that any savings in cooling cost would offset the additional hardware cost.

In the final reckoning, performance benefits and cost must be weighed with the application. The vast majority of motor drives operate at fundamental frequencies which rarely exceed a few hundred Hz and have relatively modest dynamic requirements. As such, they do not require very high PWM carrier frequencies. If the customer can put up with the acoustic noise and the output THD levels, the only remaining benefits from the ACPI are higher switching frequency and inherent control over output dv/dt. High speed drives or servo drives requiring enhanced dynamic performance, would clearly have more to gain from an increase in PWM carrier frequencies.

8.4 Further Work

Although the work outlined in this thesis has answered many questions and presented several topologies, there are still some questions which remain unanswered and avenues of research which deserve further investigation.

A clear economic incentive for the adoption of the ACPI topology could be provided by integration of the main switches, the auxiliary switches and even the resonant capacitors into a single power module. In addition, zero voltage switching of the main device permits a different optimisation of the device design. Higher device current densities can be achieved at the expense of a reduced (hard switched) turn-off safe operating area. Modified designs could be used to reduce either the total silicon area (device cost) or the on-state voltage (cooling cost).

It is likely, therefore, that the most significant advances in the ACPI and in novel converter technology will come from the power devices themselves. Thus, investigation of optimisation and integration of devices for resonant converters would be worthwhile.

Appendix A

SIMULATED WAVEFORMS

Appendix A shows simulated waveforms from various converter topologies. One has to bear in mind that only selected waveforms are given, because the high variety of collected waveforms would expand this appendix. This Appendix can be cross read with Chapter 3, 4 and 5. Section A.1 describes the simulation program that has been used and the simulation set-up. Section A.2 shows waveforms of RDCL topologies and section A.3 shows waveforms of PCI topologies.

A.1 Simulation Set-up

All discussed topologies were simulated in MicroSim/PSPICE. The PSPICE analysis program allows designing and simulating circuit designs containing both analogue and digital components. PSPICE starts a simulation by calculating the bias-point of the circuit. Thereby PSPICE sweeps sources, global parameters and model parameters through a range of values. The bias point is then calculated for each value of sweep. Thus for example, transfer functions of amplifiers or high and low thresholds of logic gates can be found. When PSPICE calculated the bias point it starts with the transient analysis. PSPICE maintains an internal time step which is continuously adjusted to maintain accuracy while not performing unnecessary steps. During periods of inactivity the internal time step increases. During active region, it decreases. Between two time steps PSPICE calculate voltage, current and other defined output parameters in the analogue and digital circuit. It is removing the time from the circuit producing a steady state circuit. In order to solve the circuit equations PSPICE uses an iterative algorithm following Newtown's iteration criteria.

Each resonant converter was simulated on a test circuit as shown in Figure A.1.1 for RDCL topologies and Figure A.1.2 for PCI topologies. Both test circuits use a voltage source and a diode at the input side. This combination is equivalent to an ideal three phase supply voltage and a diode bridge rectifier. As a consequence, a switch dump resistor is required to prevent excessive link voltage during periods of motor regeneration. In the simulation a simplified controlled dump resistor was used.

The inverter side was simplified by a single switch and a diode for the RDCL circuits. Turning on the device is thus equivalent to allow simultaneous conduction of both switches in an inverter leg. The inverter side of the PCI circuits do not include an additional switch, because

turning on both switches at the same time would mean a short circuit in the PCI topology. The performance of PCI circuits were simulated using one pole. Therefore only a load current had been directly connected to the inverter side.

The load current can be expressed either as a constant current source or a current step source depending on the converter topology. For the basic RDCL and the clamp basic RDCL it can be assumed that the inverter switching statues remains constant for several resonant cycles before the switching status changes. Thus an ordinary dc current source describes the load. A dc current source has been also used when simulating PCI topologies. Here the load inductance of each pole is much greater than the resonant inductance and therefore the load current can be assumed constant over several pole switching commutations. For PRDCL and quasi-RDCL topologies a current step source has been used. The dc-link voltage resonates mostly when the status of the inverter is changing. Thus it has to be taken into account the changing state of the inverter. In reality, the inverter input current consist of high frequency pulse widths which vary due to the applied modulation strategy. Reverse power flow was simulated by changing the sign of the dc current source or the step current source.

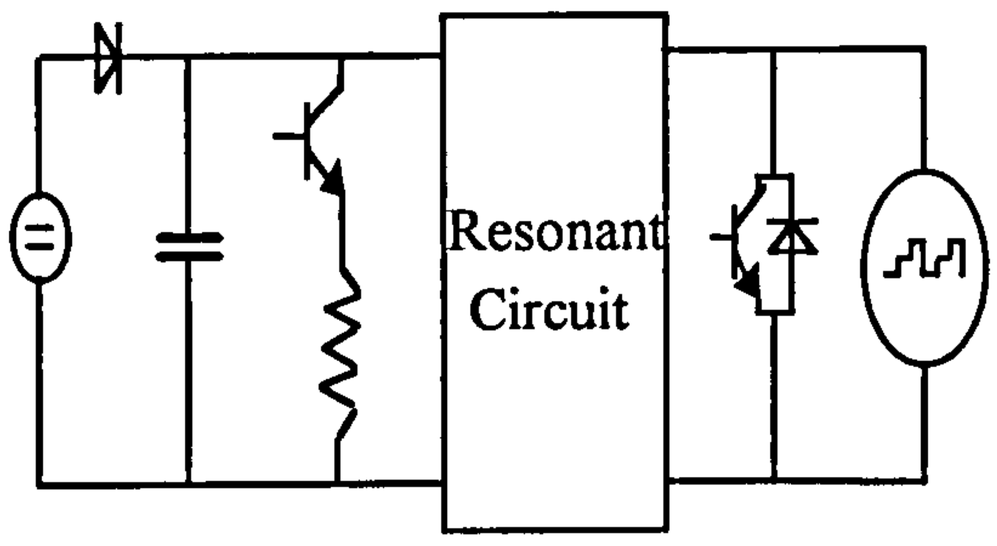


Figure A.1.1: Test circuit for resonant dc-link inverters

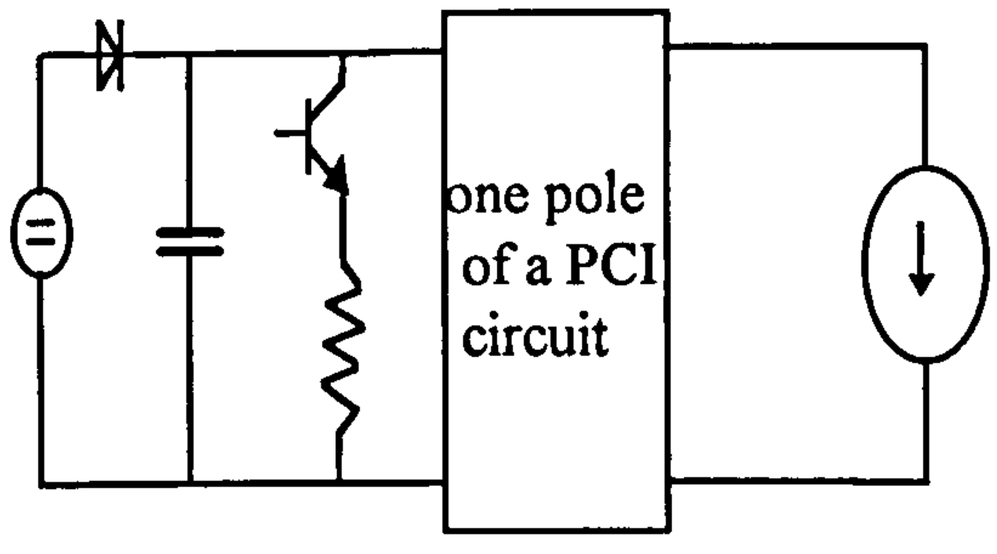


Figure A.1.2: Test circuit for pole commutated inverters

The model for each power semiconductor was simplified to a voltage controlled resistance with a low pass filter in series with the controlling voltage. This allowed reasonable on-state accuracy to be obtained with a minimal penalty on execution time. Accuracy during switching transitions was considered to be less important since all transistors took place at either zero voltage or zero current.

The control circuit for each converter was realised using a mixture of digital and analogue components as well as look-up tables. All capacitors, inductors and bus bars included a series resistance to model losses.

A.2 Resonant DC-Link Inverters

The simulated inverters were designed for a nominal power rating of 10kW. The dc-link voltage was set to 500V and a resonant dc-link frequency of 60kHz was chosen when PWM control was applied. The controller was programmed to ensure that zero voltage time for the main inverter switches was at least 1µs.

Basic RDCL: L_r=5µH, C_r=1µF, I_{load}=43A

Figure A.2.1 shows the simulated inverter input voltage. As discussed in Chapter 3 the voltage resonates up to a level of at least twice the dc-link voltage. The average resonant frequency is set to 66kHz.

Figure A.2.2 shows the resonating inductor current i_r. The maximum value of the current results from the impedance, the load current and the current boost mode level. During the boost mode the current increases linearly for the duration of short circuit of the inverter. This time is defined by the controller. With equation A.2.1 the current peak resulting from impedance and load configuration can be calculated to:

$$I_{peak} = \frac{V_{dc}}{\sqrt{\frac{L_r}{C_r}}} + I_{load} = \frac{500V}{\sqrt{\frac{5\mu H}{1\mu F}}} + 43A = 266A \qquad (A.2.1)$$

The controller adds additional currents between 4A to 14A. A simulated inductor resistance of 0.1Ω leads to instant losses at peak current of 7.8kW. This value shows that the basic RDCL topology tends to have high inductor losses.

Figure A.2.3 shows the simulated switching pattern of the switch S.

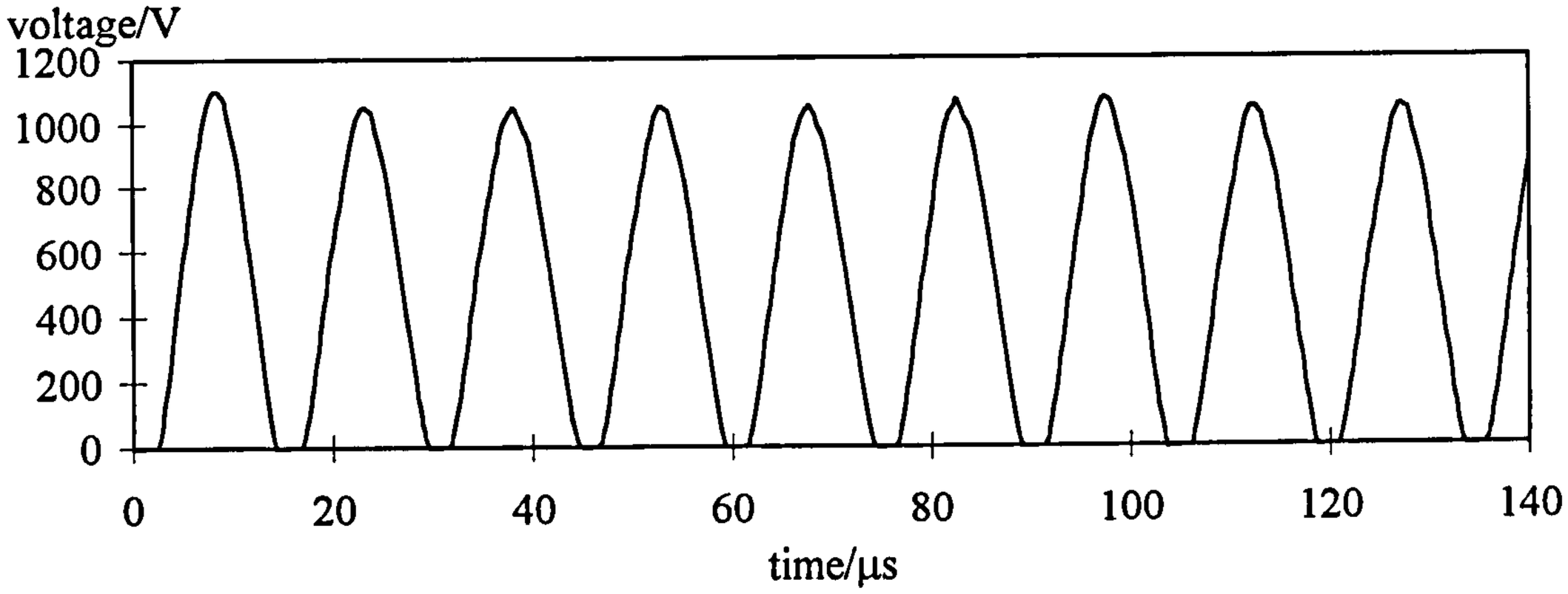


Figure A.2.1: Simulated inverter input voltage of the basic RDCL topology

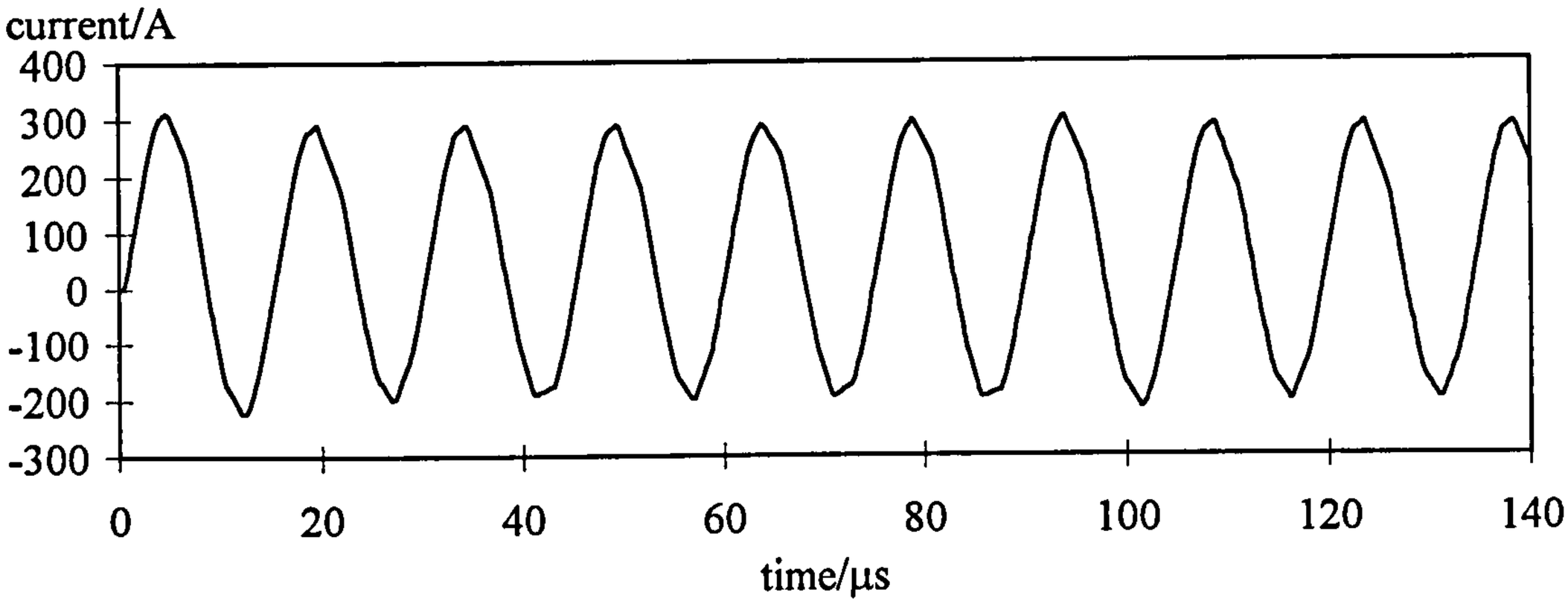


Figure A.2.2: Simulated resonant current of the basic RDCL topology

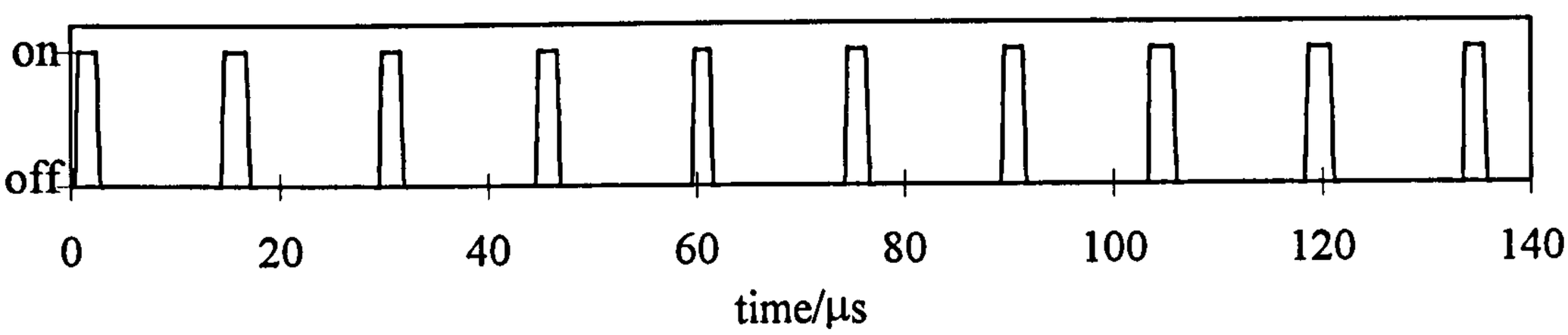


Figure A.2.3: Simulated switching pattern of switch S of the basic RDCL topology

Active clamp basic RDCL: L_r=5µH, C_r=1µF, C_{clamp}=100µF, V_{clamp}=280V, I_{load}=43A

Figure A.2.4 shows the inverter input voltage (voltage pulses) and the voltage across the clamp capacitor (dc voltage). With a dc-link voltage of 500V and a 280V pre-charged clamp capacitor the clamp voltage is around 750V. Thus the inverter input voltage is reduced to 25% compared to the basic RDCL circuit. In addition Figure A.2.4 shows that the voltage across the clamp capacitor is not constant. It varies slightly with every switching event. The change of this voltage (ramps up and down) is the result of two different charge operation modes (charging mode and discharging mode) that play an important role in the active clamp

technique. Once the inverter input voltage reaches the clamp voltage the diode is forward biased and starts conducting to charge the clamp capacitor (charging mode). At around half of the clamp time the clamp capacitor starts to discharge and current commutates from the clamp diode to the clamp IGBT (discharging mode). The charge across the capacitor is constantly monitored and the clamp IGBT must turn off when the charge balance across the clamp capacitor is equal zero. This is difficult to achieve from the point of view of sensors and controller.

Figure A.2.5 shows the resonant current. Again a simulated inductor resistance of 0.1Ω results in large instant inductor losses.

Figure A.2.6 shows the on and off state of switches S and, S_{clamp}.

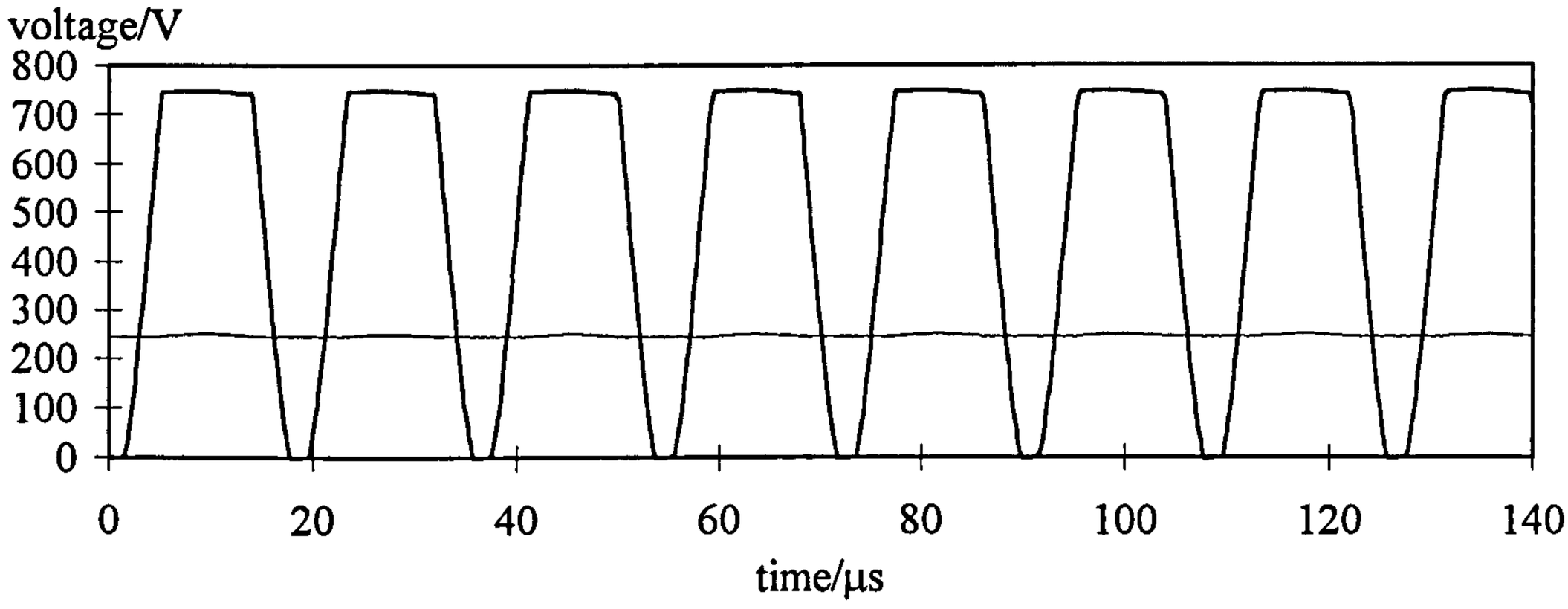


Figure A.2.4: Simulated inverter input voltage (pulse-line) and voltage across the clamp capacitor (dc-line) of the active clamp basic RDCL topology

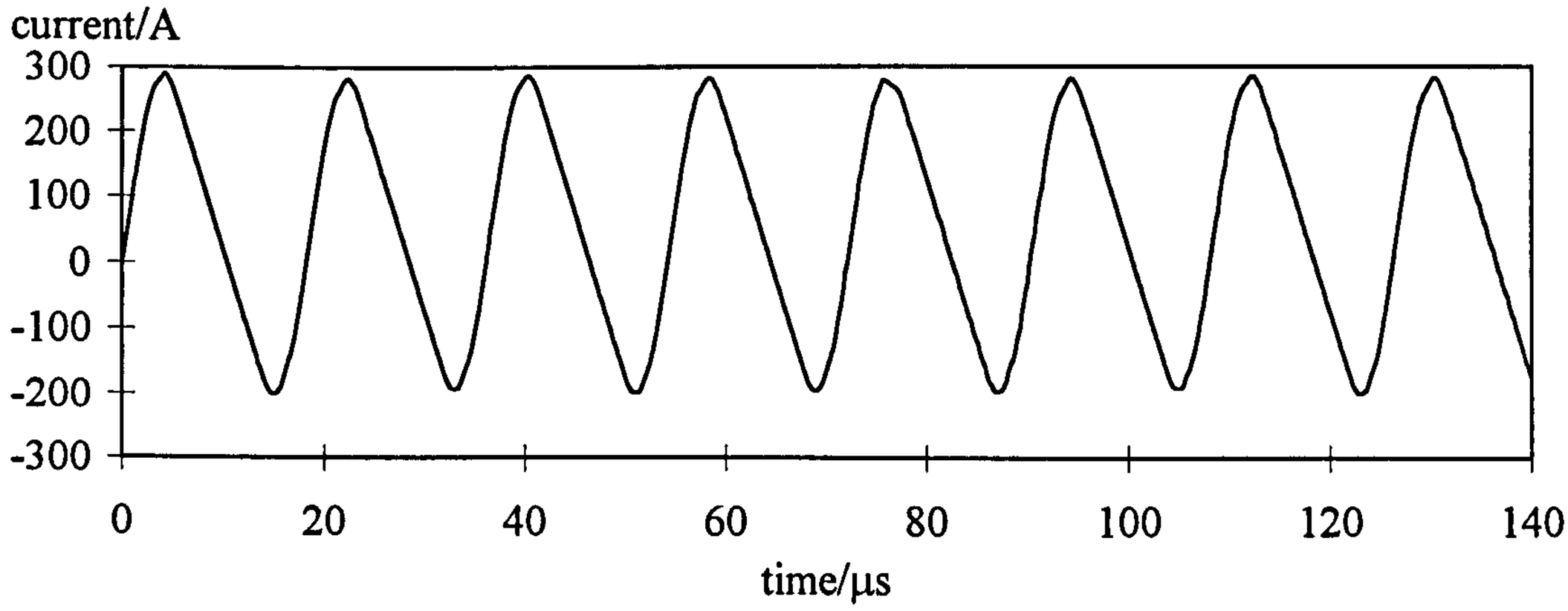


Figure A.2.5: Simulated resonant current of the active clamp basic RDCL topology

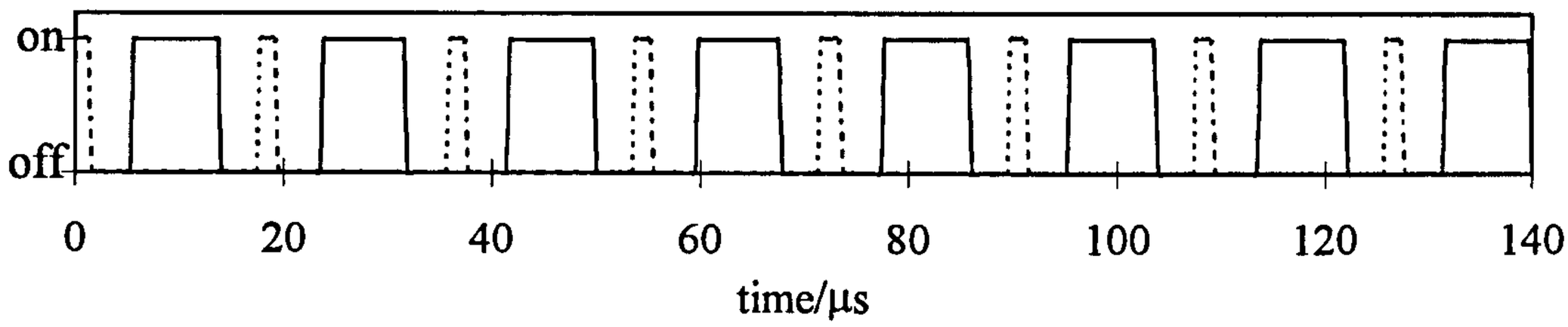


Figure A.2.6: Simulated switching pattern of switch S (dotted line) and switch S_{clamp} (solid line) of the active clamp basic RDCL topology

PRDCL: L_r=1.5µH, C_r=0.25µF, C_{snu}=33.6nF, I_{load}=(0A, 15A, 28A, 43A)

The simulated inverter input voltage is shown in Figure A.2.7. One can say firstly that the voltage is always clamped to the dc-link voltage and secondly the dc-link voltage includes voltage notches. This notches lead to supply voltage drop of the inverter and consequently to a reduction in the output power (Chapter 3).

Figure A.2.8 shows the simulated step load current. The steps 0A, 15A, 28A and 43A have been randomly chosen. This current must flow through the clamp switch S_{clamp} leading to high on-state losses as the following example shows: It is given: a device on-state voltage of 2.7V, 30A rms. load current, 1µs zero voltage on-state time and a switching frequency of 10kHz. In addition the modified PWM control scheme mPWM2 is applied (section 3.3.2) thus the resonant circuit is activated only once in one inverter switching period. Therefore the on-state losses can be calculated to (equation A.2.2):

$$P_{losses,on-state} = 2.7V*30A - 2.7V*30A*\frac{1\mu s}{100\mu s} = 80.19W \qquad (A.2.2)$$

Figure A.2.9 shows the resonant current flowing through the resonant inductor. In comparison to the basic RDCL and the clamp basic RDCL topology the current stress is drastically reduced.

Figures A.2.10 to A.2.12 show the switching pattern of switches S, S_{clamp} and S_r respectively.

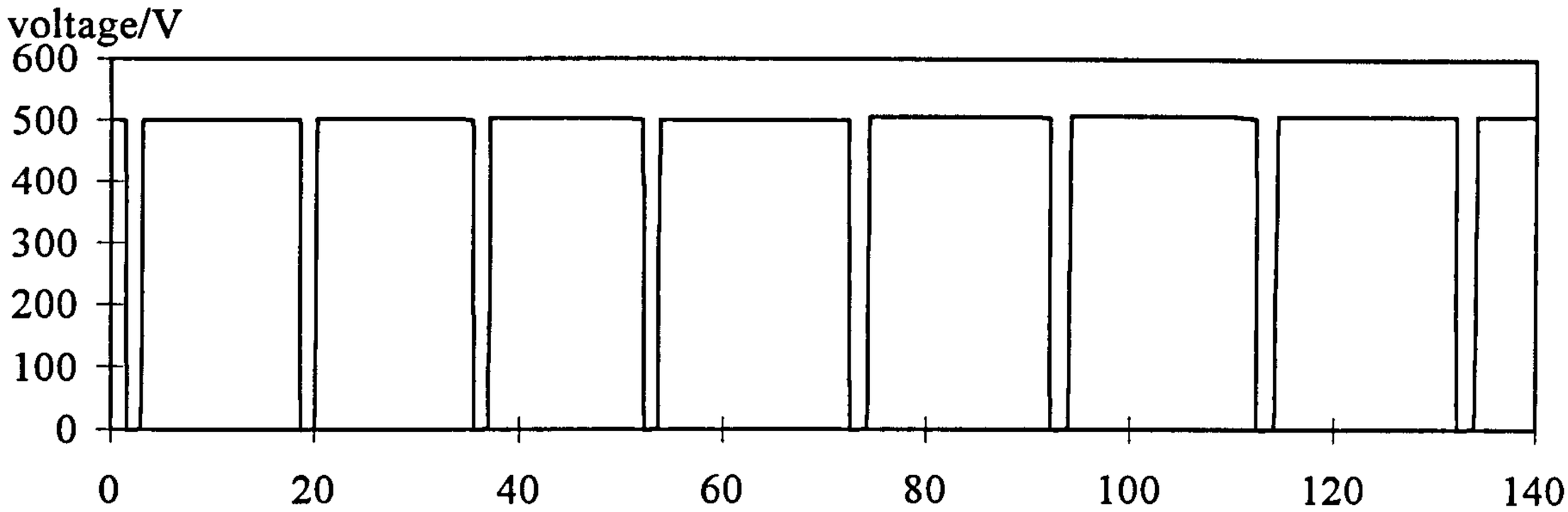


Figure A.2.7: Simulated inverter input voltage of the PRDCL topology

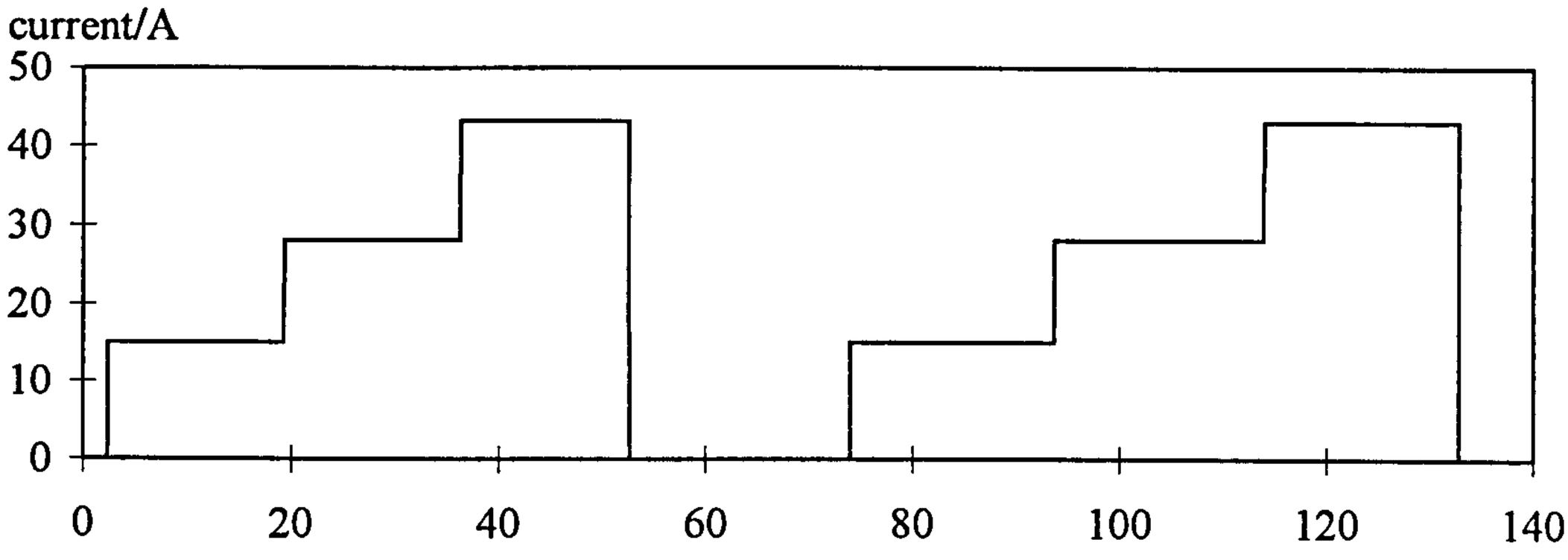


Figure A.2.8: Simulated step load current for the PRDCL topology

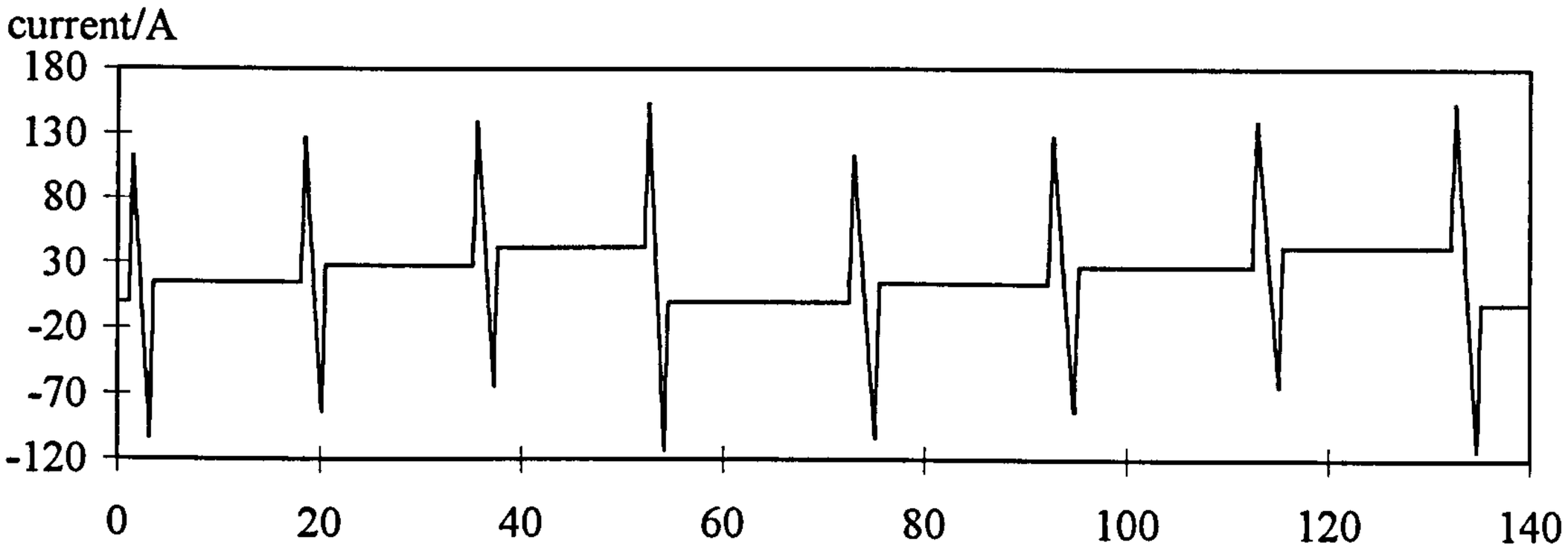


Figure A.2.9: Simulated resonant current of the PRDCL topology

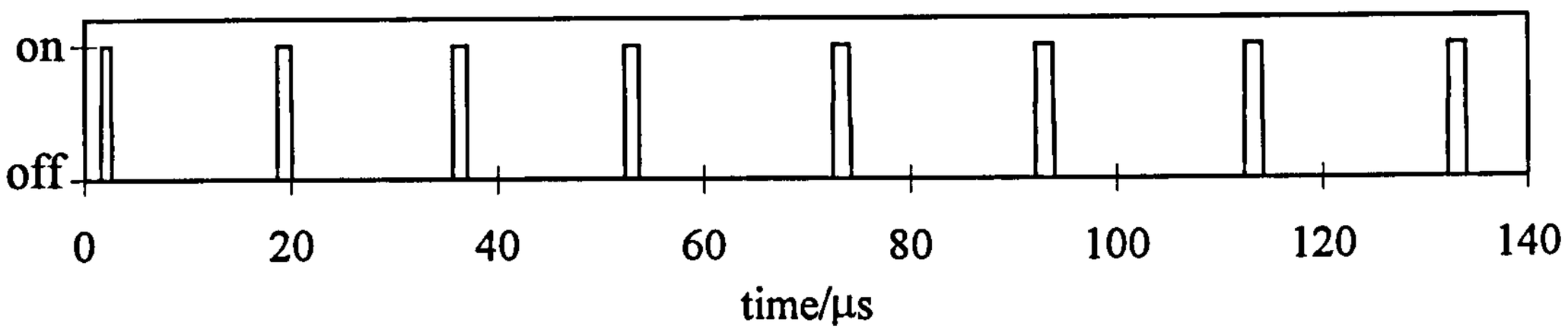


Figure A.2.10: Simulated switching pattern of switch S of the PRDCL topology

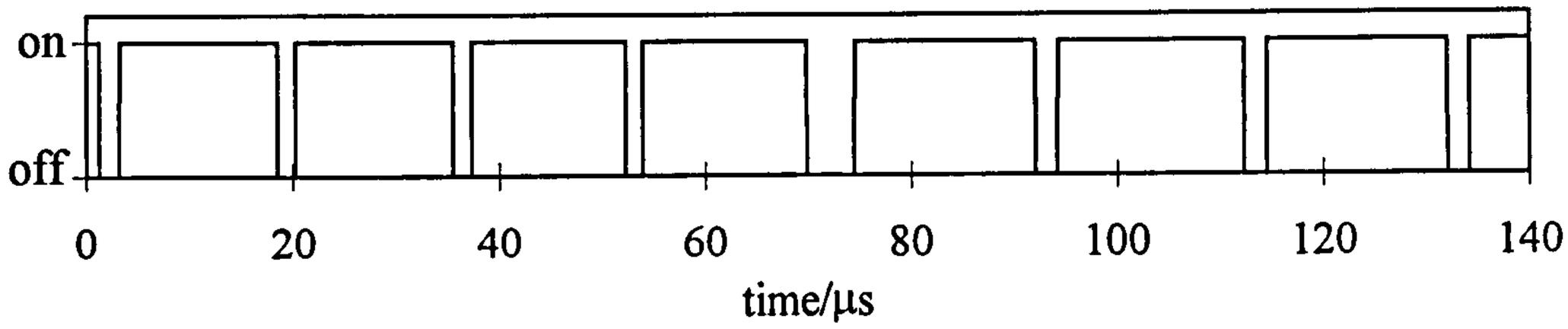


Figure A.2.11: Simulated switching pattern of switch S_{clamp} of the PRDCL topology

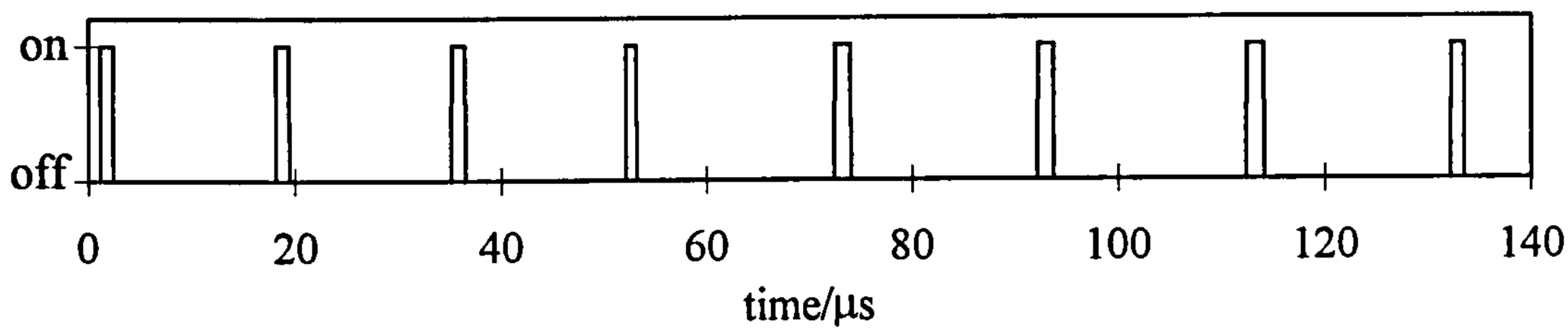


Figure A.2.12: Simulated switching pattern of switch S_r of the PRDCL topology

Active clamp q-RDCL: L_r=5μH, C_r=50nF, C_{clamp}=100μF, I_{load}=(0A, -15A, -28A, -43A)
The simulated waveforms shown for the active clamp q-RDCL result from reverse power flow conditions. Thus the load current is negative.

Figure A.2.13 shows the inverter input voltage V_{inv}. (When the inverter input voltage drops from the clamp value to its dc level a high frequency oscillation starts, accommodated from the interaction between the resonant inductor and the resonant capacitor during turn-off of S_{res} and S_{clamp}). As discussed in Chapter 3 the inverter input voltage is clamped and most of the time it stays at dc-link level.

Figure A.2.14 shows the simulated negative load current. At this point it has to be said that all simulated resonant inverters show no difference in performances, when testing the resonant inverter under forward power flow or reverse power flow. Figure A.2.15 shows how the resonant current follows the load current.

The switching patterns for S_{res}, S_{clamp} and S are given in Figures A.2.16, A.2.17 and A.2.18 respectively.

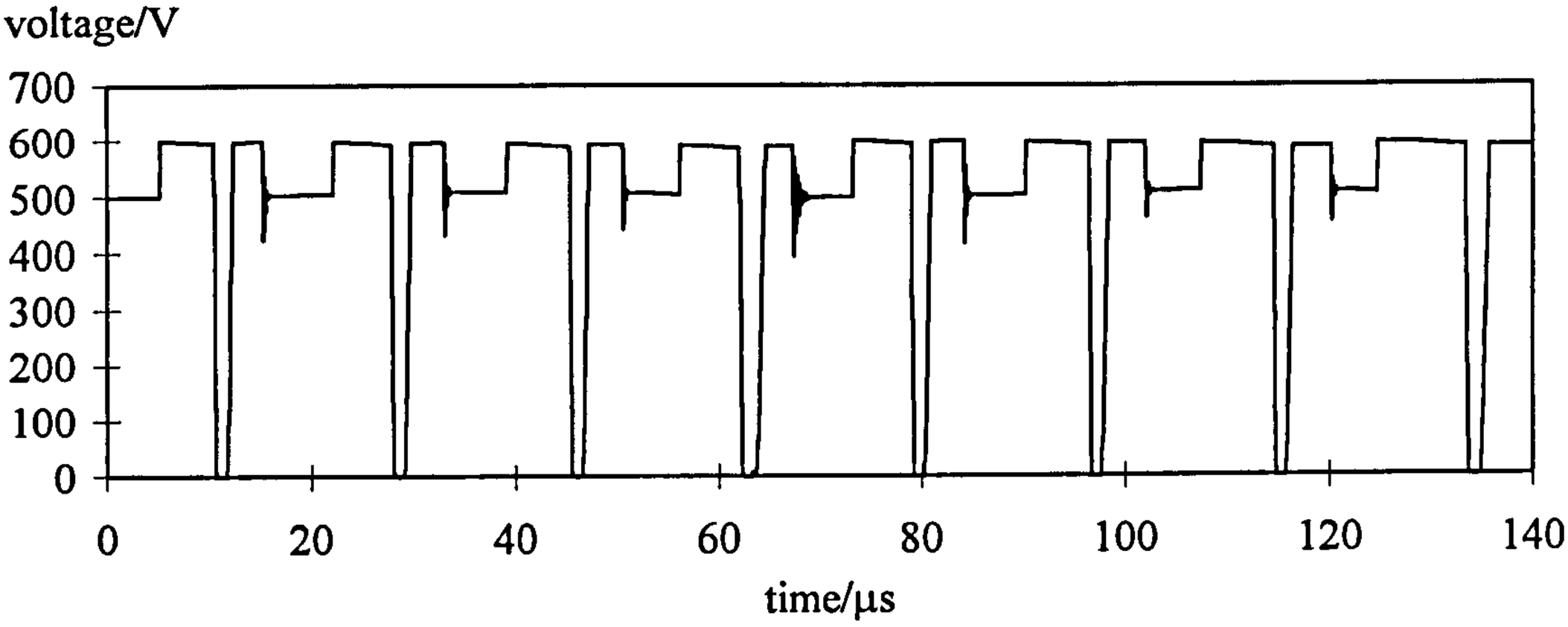


Figure A.2.13: Simulated inverter input voltage of the active clamp q-RDCL topology

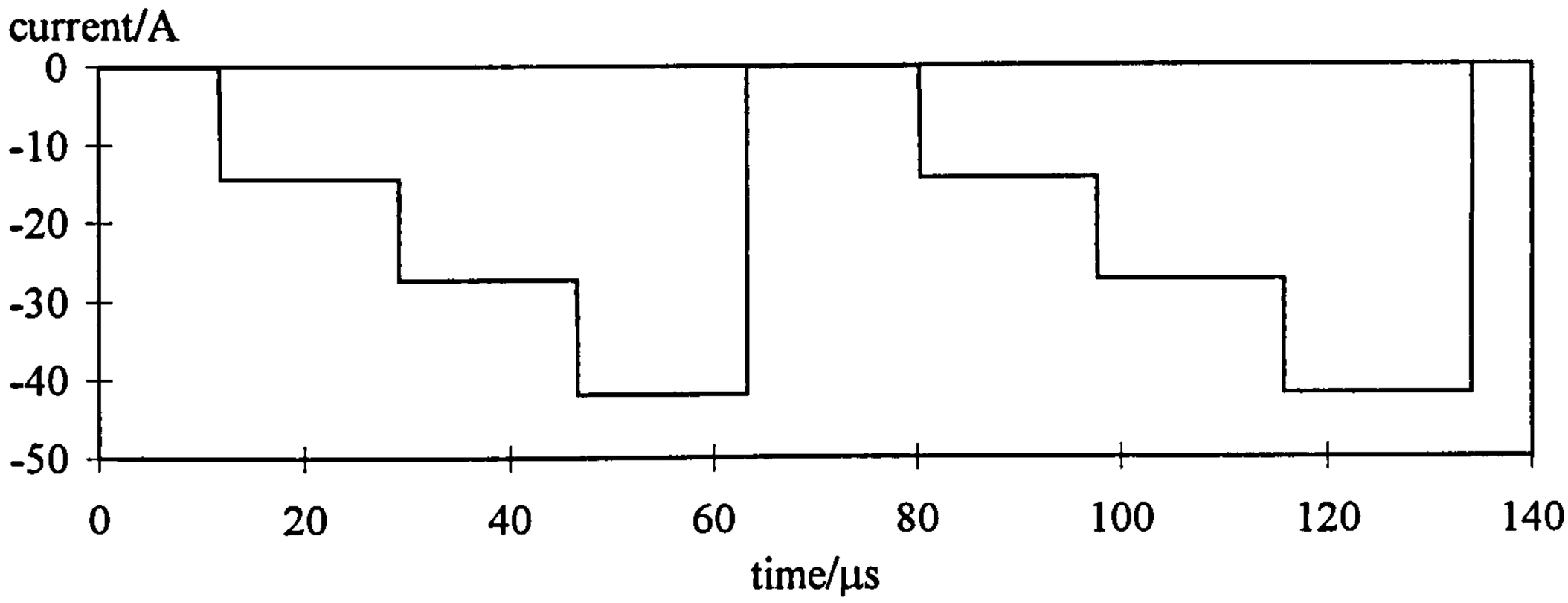


Figure A.2.14: Simulated step load current for the active clamp q-RDCL topology

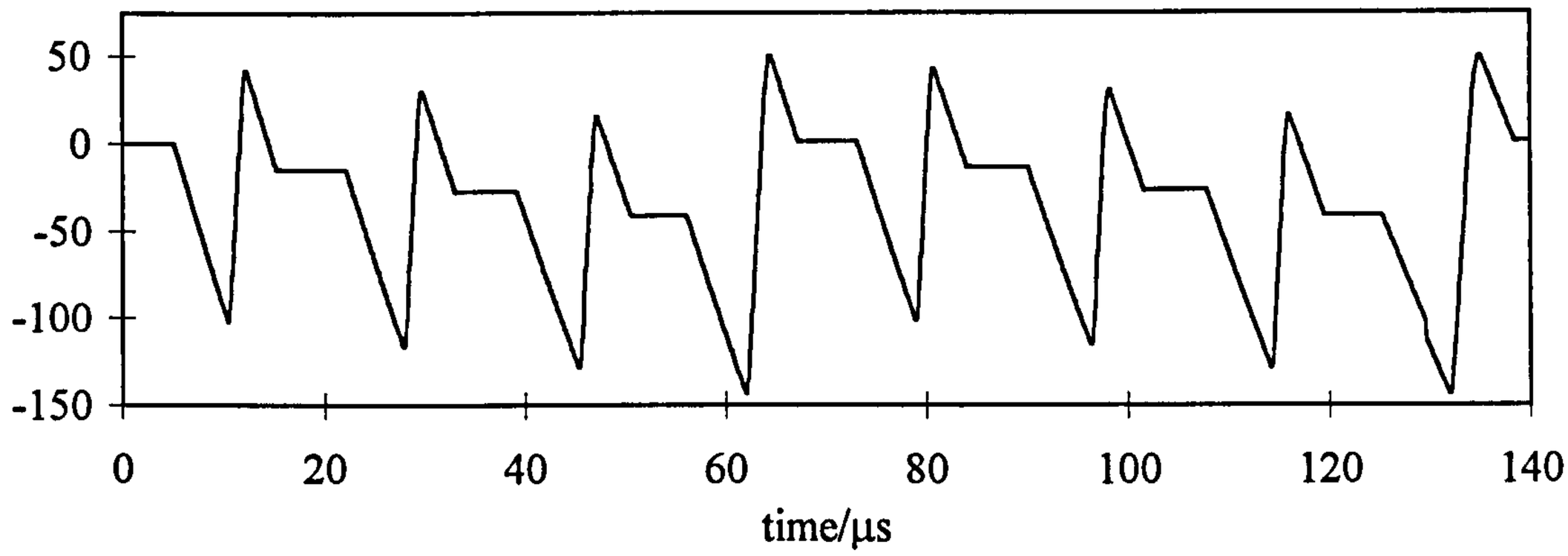


Figure A.2.15: Simulated resonant current of the active clamp q-RDCL topology

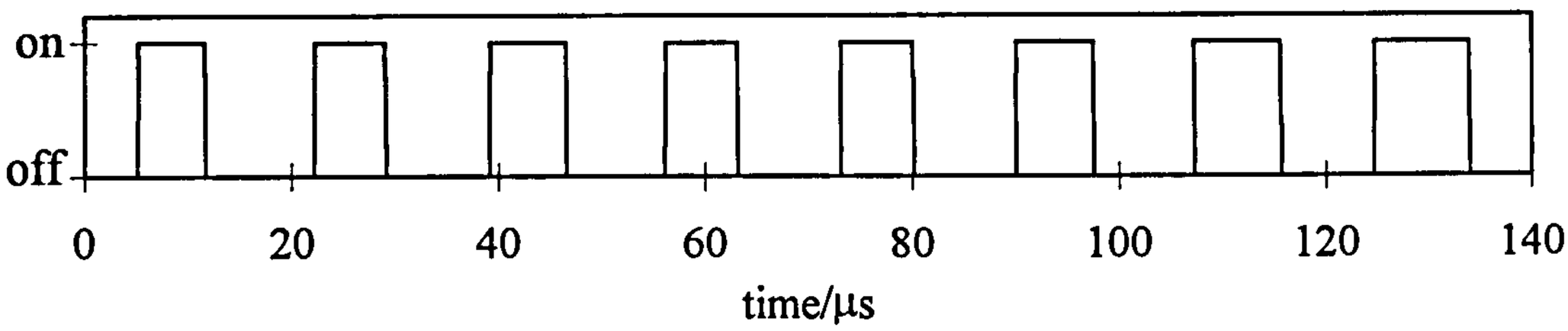


Figure A.2.16: Simulated switching pattern of switch S_r of the active clamp q-RDCL topology

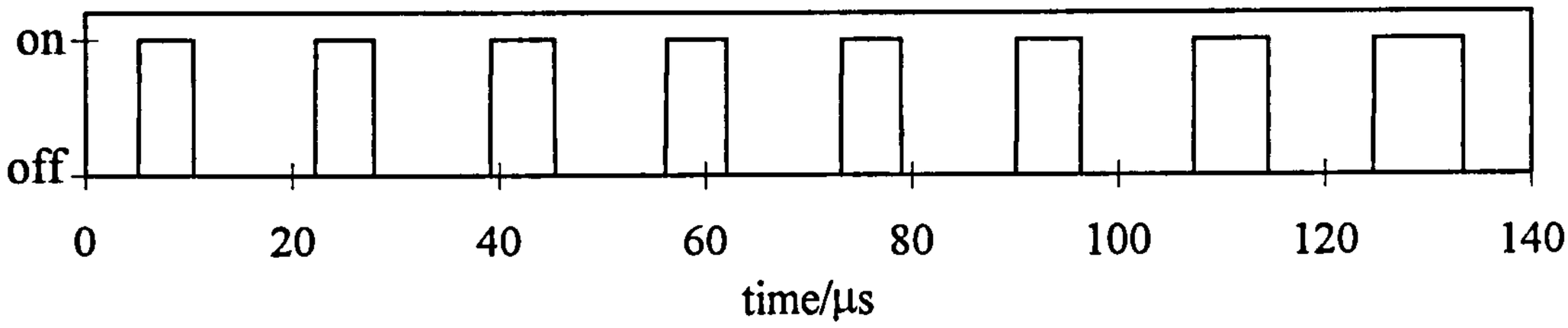


Figure A.2.17: Simulated switching pattern of switch S_{clamp} of the active clamp q-RDCL topology

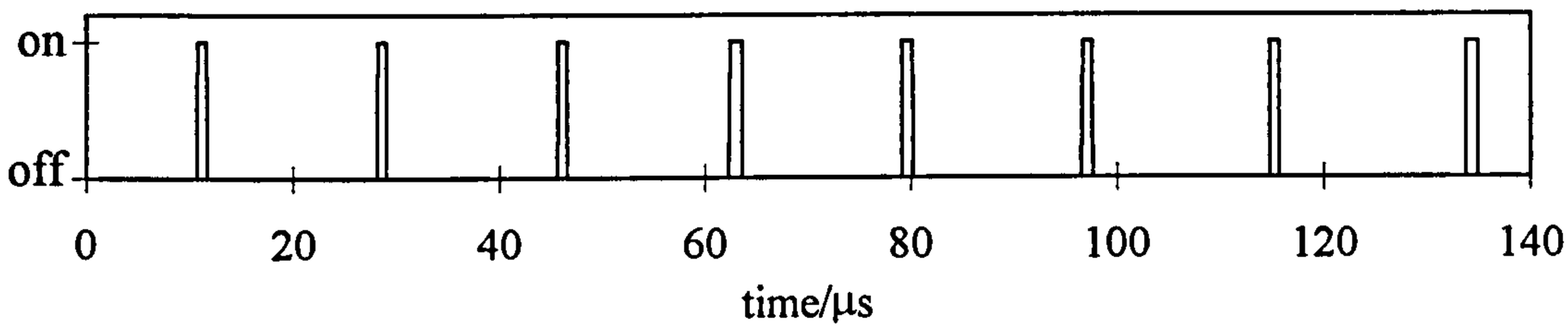


Figure A.2.18: Simulated switching pattern of switch S of the active clamp q-RDCL topology

Passive clamp q-RDCL: L_{r2}=5µH, C_r=50nF, C_{clamp}=100µF, $L_{r1}+L_{np}$=20µH, L_{ns}=320µH, coupling factor=0.99, I_{load}=(0A, 15A, 28A, 43A)

The inverter input voltage of the passive clamp RDCL topology is shown in Figure A.2.19. As discussed in section 3.4.2 the voltage tends to oscillate during the clamp mode because of the stray inductance of the transformer. A coupling factor of one would result in a constant inverter input voltage at clamp voltage level but a coupling factor of one is an unrealistic value from the viewpoint of the transformer design. The simulation waveform shows an additional oscillation once the clamp mode has finished. The inductor current flowing through $L_{r1}+L_{np}$ is somewhat higher than the load current once the clamp mode has stopped (Figure A.2.20). This charge unbalance results in a second unintentional oscillation between $L_{r1}+L_{np}$ and the resonant capacitor. Figure A.2.20 and Figure A.2.22 show the current in the primary winding and the secondary winding. When the inverter input current drops from the maximum value to zero (Figure A.2.20) the inductor $L_{r1}+L_{np}$ has stored such a large quantity of energy that the clamp mode remains constant until the next switching event (Figure A.2.19 and Figure A.2.22). Consequently a large current is flowing through the secondary winding. Figure A.2.21 shows

the current flowing through L_{r2}. Inductor L_{r2} stores only the needed energy for an successful resonant cycle. That explains the short resonant pulses of i_{r2}.

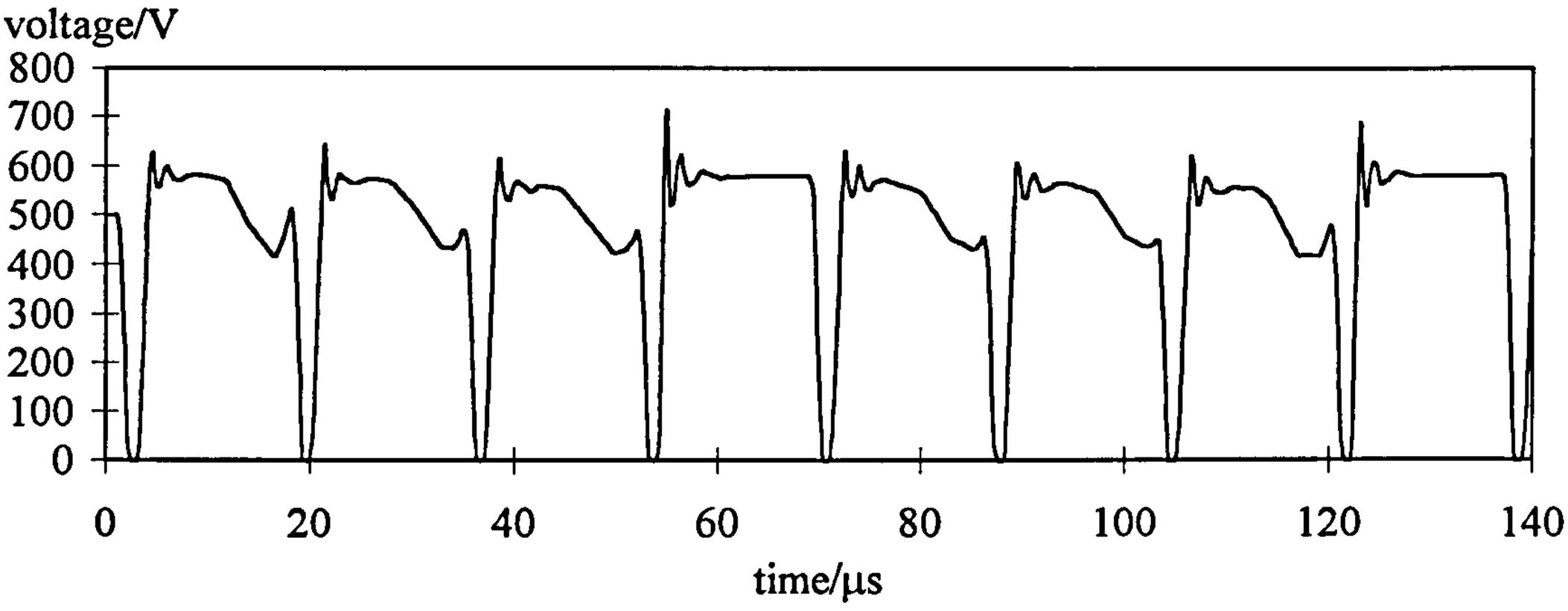


Figure A.2.19: Simulated inverter input voltage of the passive clamp q-RDCL topology

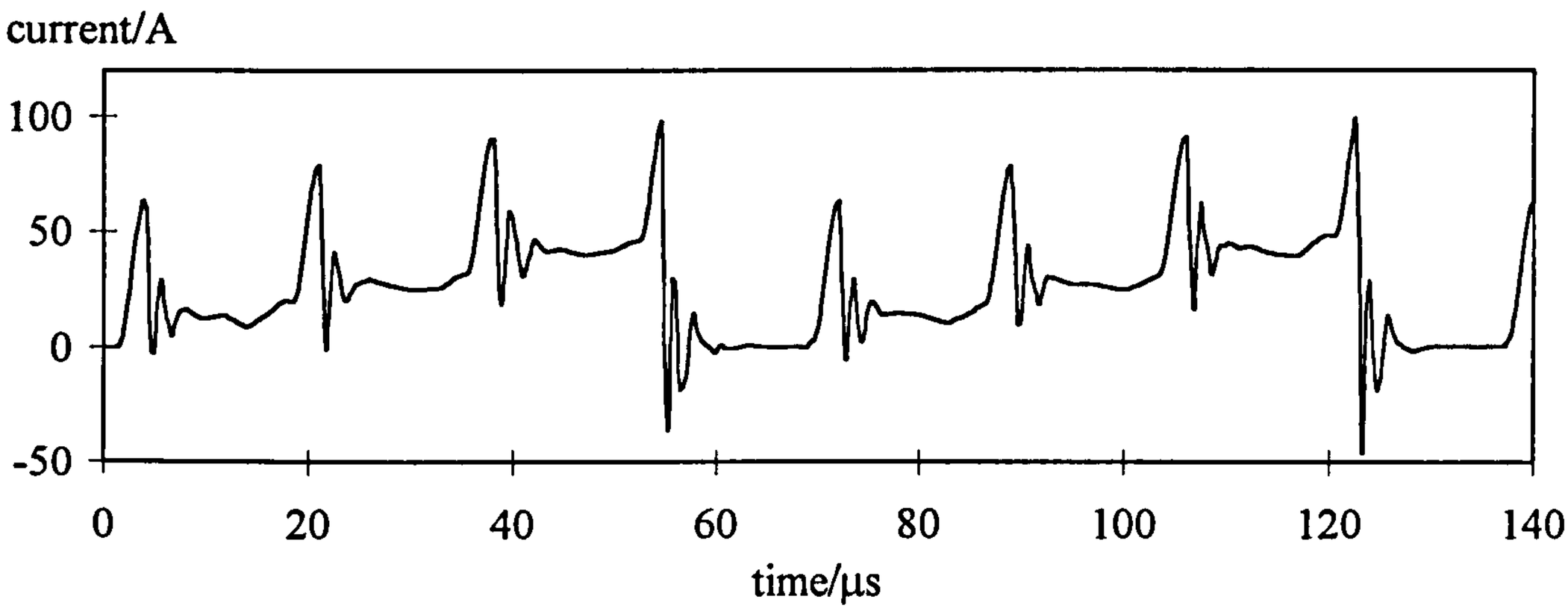


Figure A.2.20: Simulated resonant current i_r of the passive clamp q-RDCL topology

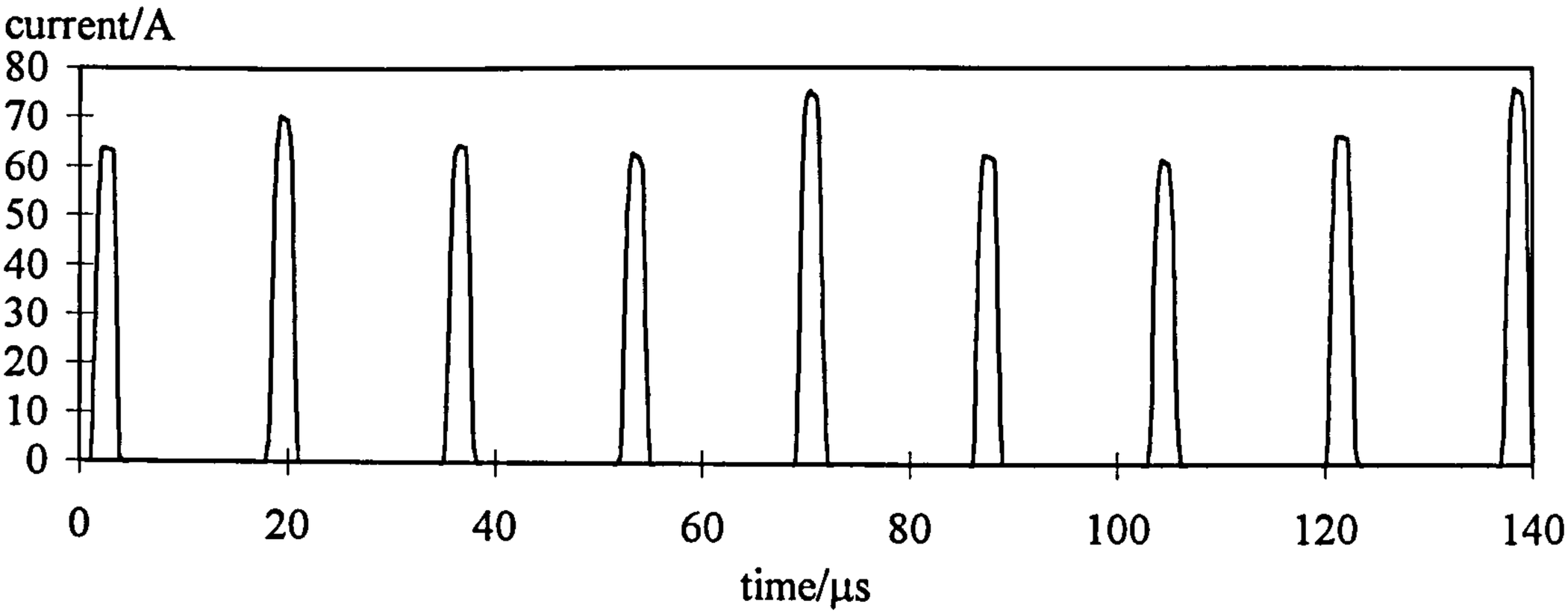


Figure A.2.21: Simulated inductor current L_{r2} of the passive clamp q-RDCL topology

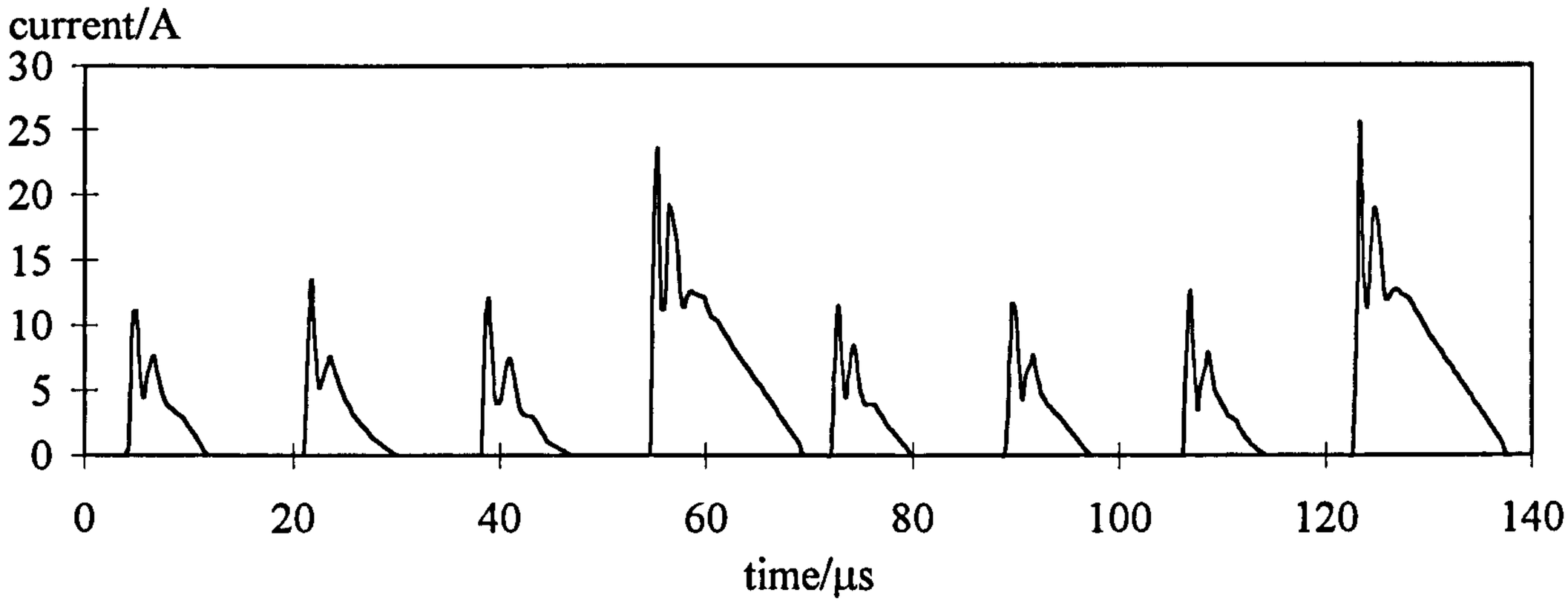


Figure A.2.22: Simulated current of the secondary winding of the transformer of the passive clamp q-RDCL topology

A.3 Pole Commutated Inverters

The simulated PCIs were supplied from a 560V dc voltage source. The load current was chosen to either +100A (motor mode) or -100A (generator mode) given a nominal power rating of 56kW for each pole. The inverter switching frequency was set to around 20kHz when PWM control was adopted. The controller was programmed to ensure that a amplitude modulation index of 0.5 was applied.

ADPI: L_r=19μH, C_{IGBT}=40nF, C_{DIODE}=1μF, I_{load}=100A

Figure A.3.1 shows the simulated phase output voltage. The large resonant inductor result in a low dv/dt stress across the switching devices that shortens the on-state time of the dc-link voltage across the device and shortens and limits the degree of PWM controllability.

Figure A.3.2 shows the inductor current that consists of two modes: freewheeling mode and resonant mode. During the freewheeling mode the inductor current is constant, whereas during the resonant mode the inductor current changes its polarity. As seen in Figure A.3.2, the freewheeling current is either +270A or -70A high. Considering a resistance of 0.1Ω of the inductor the freewheeling losses are very high.

The switching pattern of the lower switching IGBT is shown in Figure A.3.3.

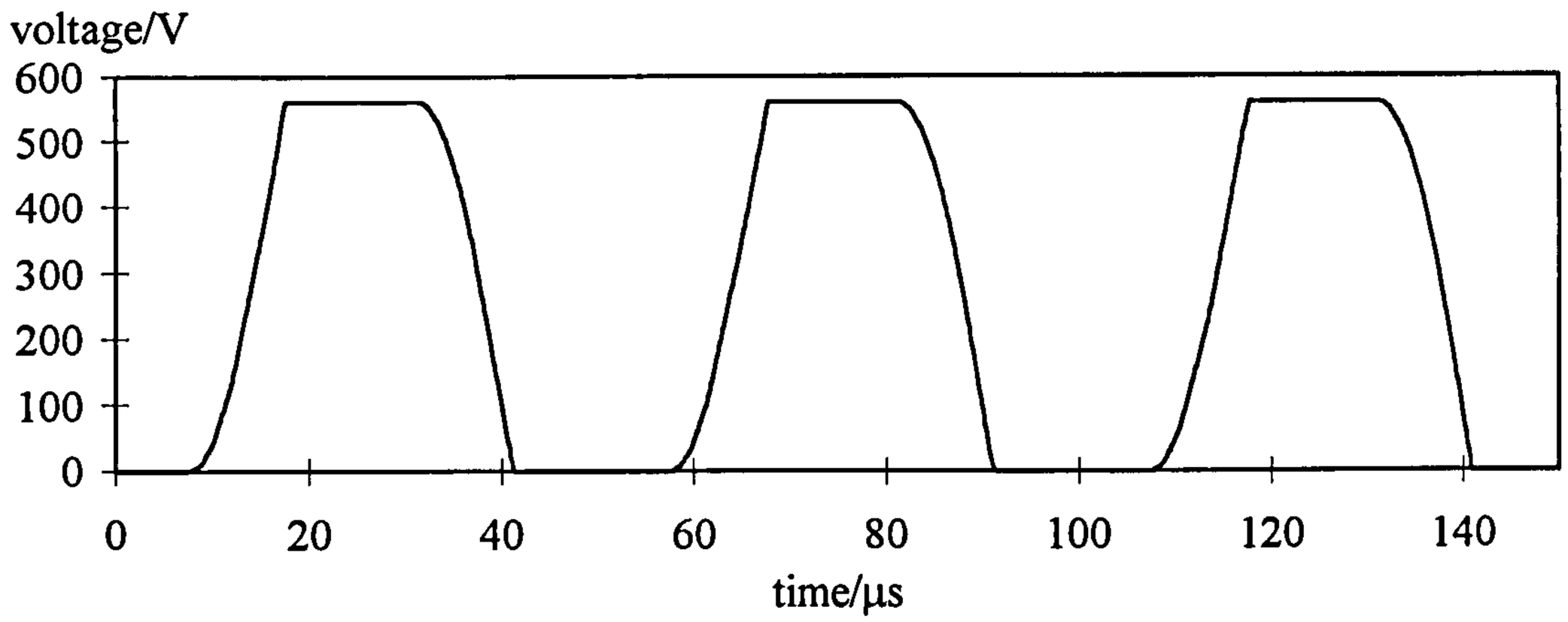


Figure A.3.1: Simulated phase output voltage V_{out} of the ADPI topology

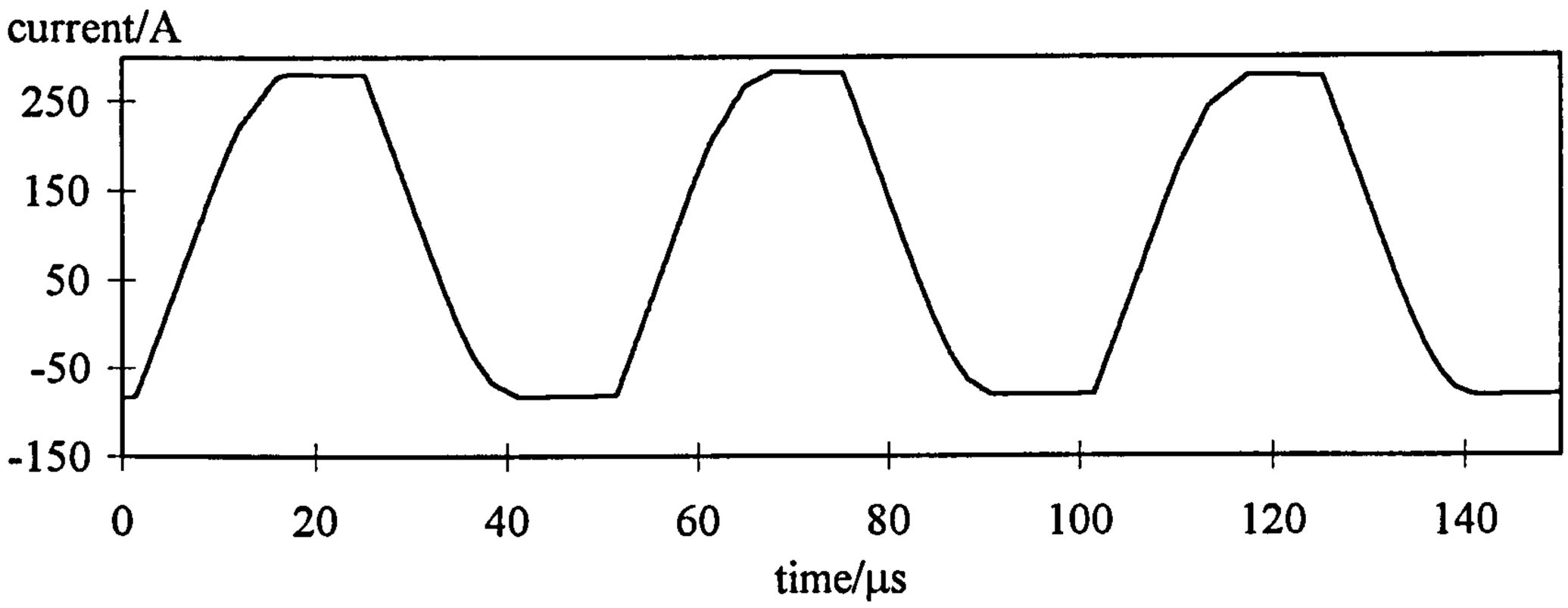


Figure A.3.2: Simulated inductor current i_r of the ADPI topology

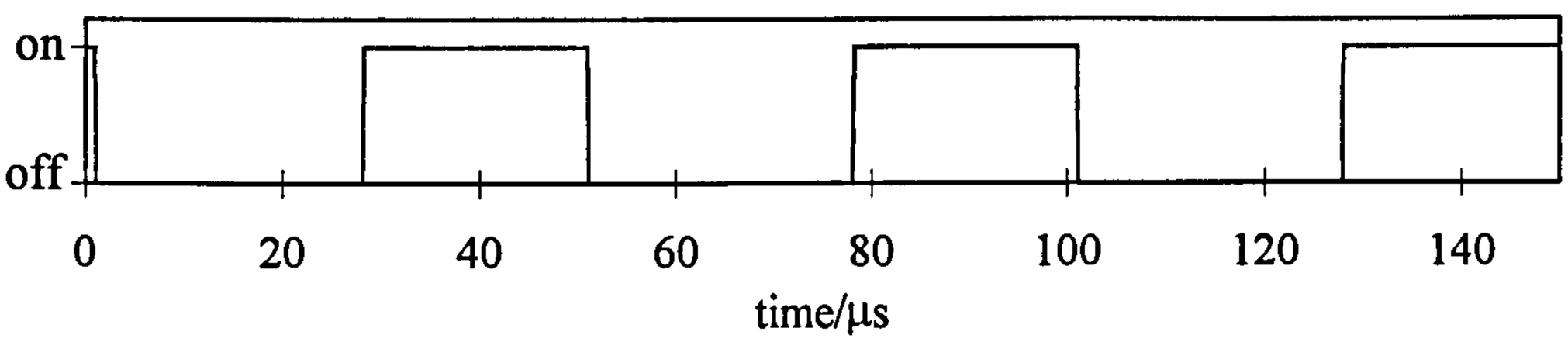


Figure A.3.3: Simulated switching pattern of switch S_2 of the ADPI topology

TADPI: L_r=8µH, C_{IGBT}=20nF, C_{DIODE}=150nF, $C_{transformer}$=800nF, $L_{primary}$=10mH, $L_{secondary}$=22.5mH, coupling factor=0.99, I_{load}=100A

Compared to the ADPI test circuit a smaller resonant inductor and a smaller snubber capacitor have been inserted for the TADPI. This results in higher dv/dt stress and longer on-state time of the dc-link (Figure A.3.4).

The transformer is connected with the output of the pole allowing a reduction of the freewheeling current compared to the ADPI. This benefit is achieved to the expense of heavy

transformers and additional devices. In this simulation the current is reduced to around +190A and -20A. This consequently leads to a reduction of the freewheeling losses (Figure A.3.5). Both topologies ADPI and TADPI must comply with equations A.3.1 and A.3.2:

$$\frac{V_{dc}}{Z_o} \geq I_{load} \qquad \text{(A.3.1)}$$

$$Z_0 = \sqrt{\frac{L_r}{2C_{DIODE}}} \qquad \text{(A.3.2)}$$

This equations show that for a given inductance L_r the capacitance C_{DIODE} must be large enough to cope with the maximum load current ($C_{DIODE} \sim I^2_{load}$). Under normal running conditions the capacitance might be chosen to a relative small value, but under start-up conditions a load current twice of that under normal running conditions or even more is required ($C_{DIODE} \sim 4I^2_{load}$). Thus the capacitors have to be dimensioned four times larger as for rated current values. That consequently leads to an increase in resonant time and therefore to scarifies the degree of PWM controllability.

Figure A.3.6 shows the control signal of the lower IGBT of the TADPI.

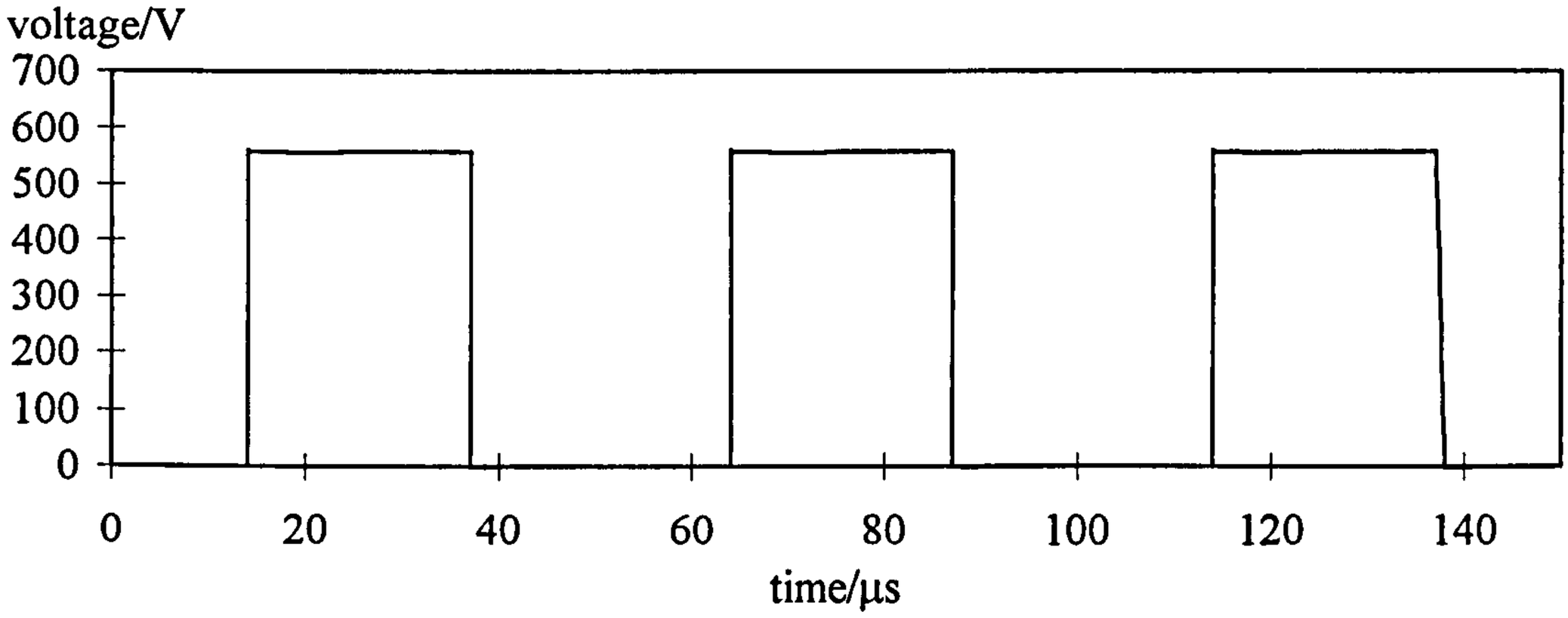


Figure A.3.4: Simulated phase output voltage V_{out} of the TADPI topology

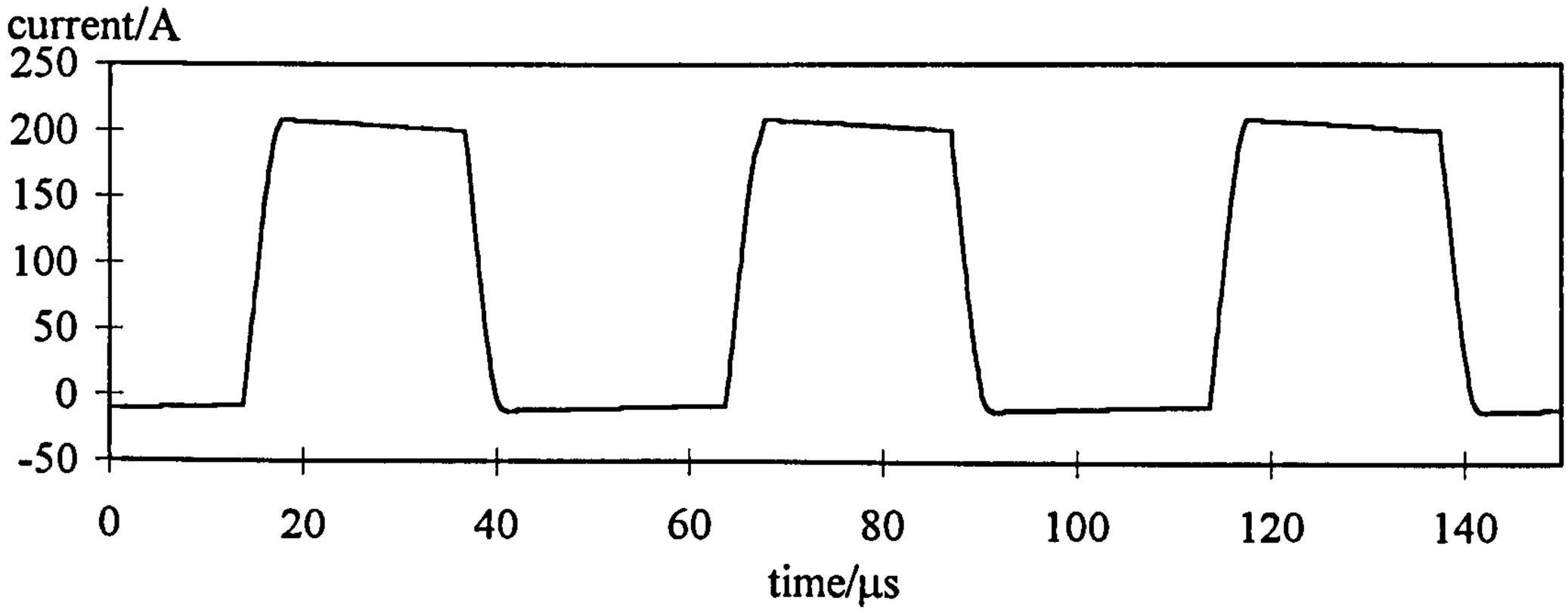


Figure A.3.5: Simulated inductor current i_r of the TADPI topology

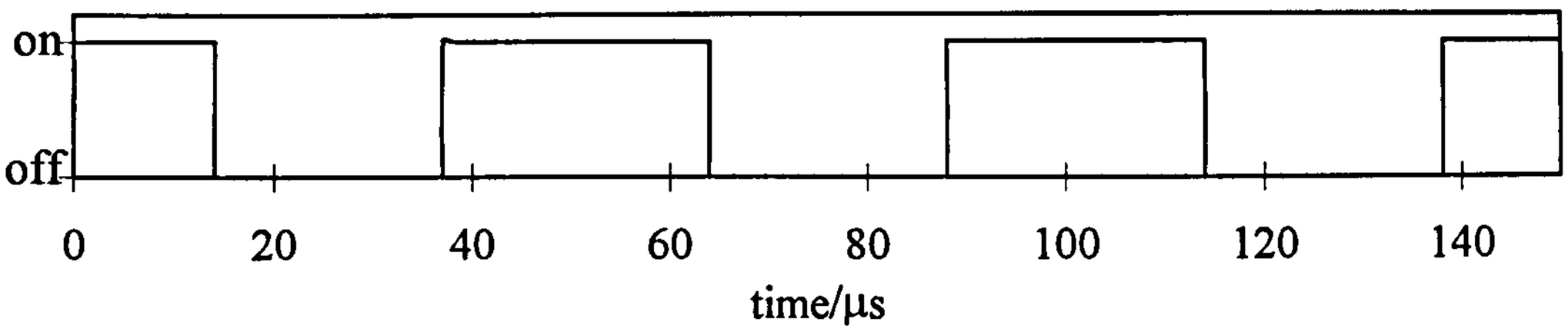


Figure A.3.6: Simulated switching pattern of S_2 of the TADPI topology

ARPI: L_r=60μH, all capacitors C=100nF, I_{load}=100A

The phase output voltage is shown in Figure A.3.7. Using the same capacitance for all four capacitors result in the same dv/dt stress across each device.

The freewheeling current is controllable and was limited to 20% overshoot of the load current during simulation (Figure A.3.8). The benefit of reducing the freewheeling current leads to the expense of the need of additional devices rated at the same power level as the main devices. Thus cost of the devices for the ARPI is twice of that of an hardswitching converter.

The switching patterns of all four devices is given in Figures A.3.9 to A.3.12.

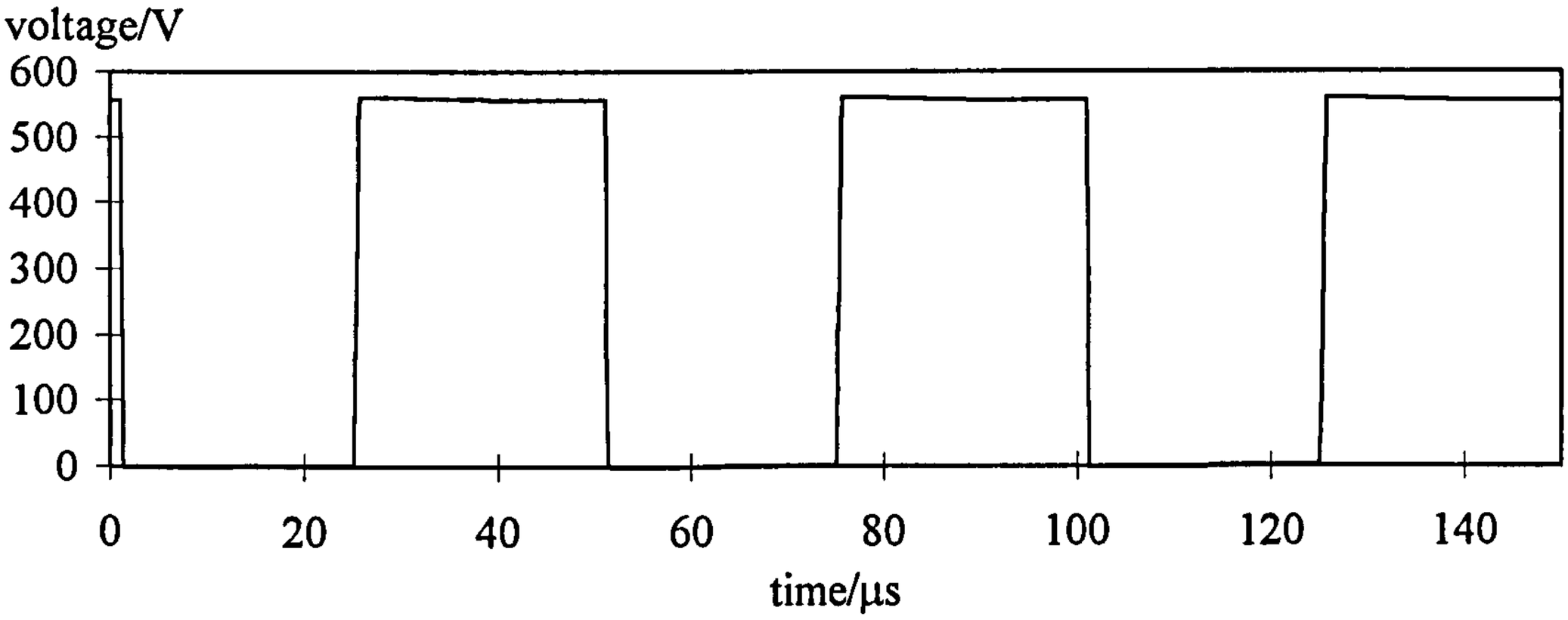


Figure A.3.7: Simulated phase output voltage V_{out} of the ARPI topology

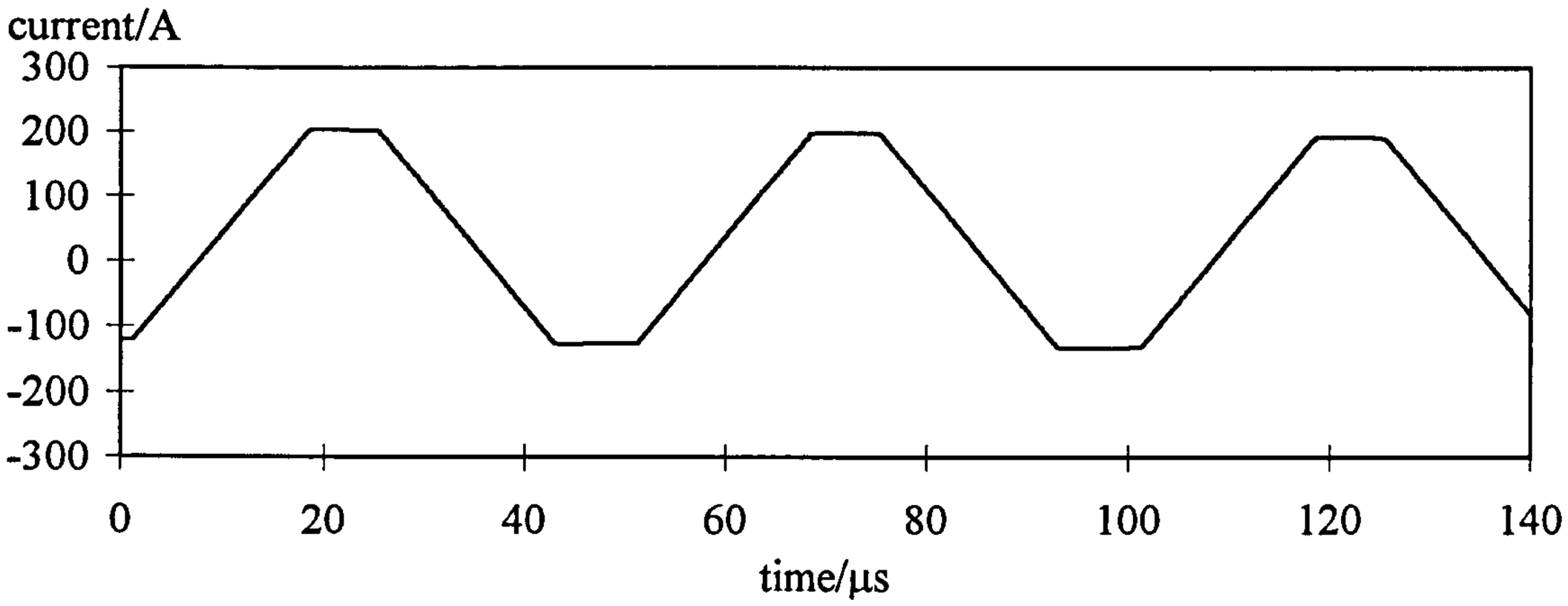


Figure A.3.8: Simulated inductor current i_r of the ARPI topology

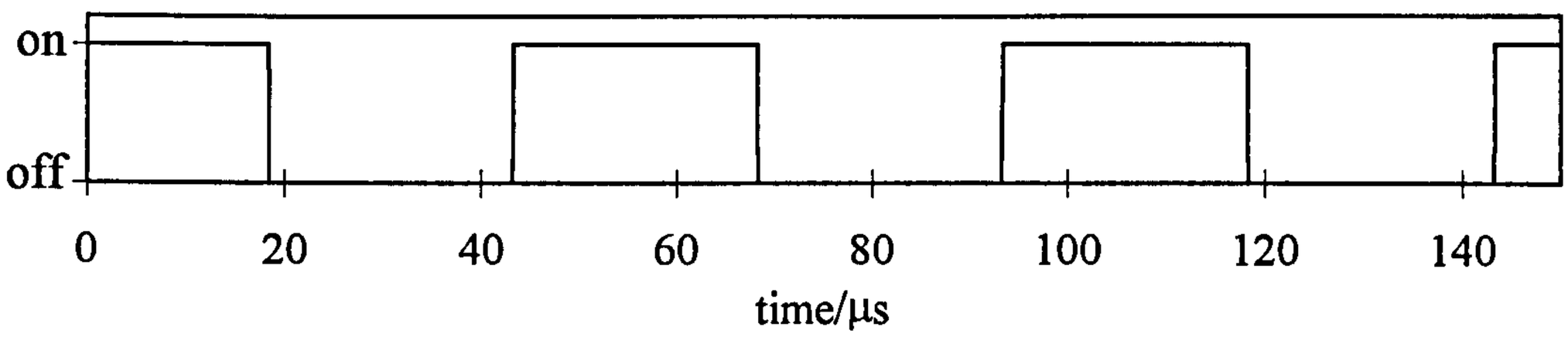


Figure A.3.9: Simulated switching pattern of switch S_1 of the ARPI topology

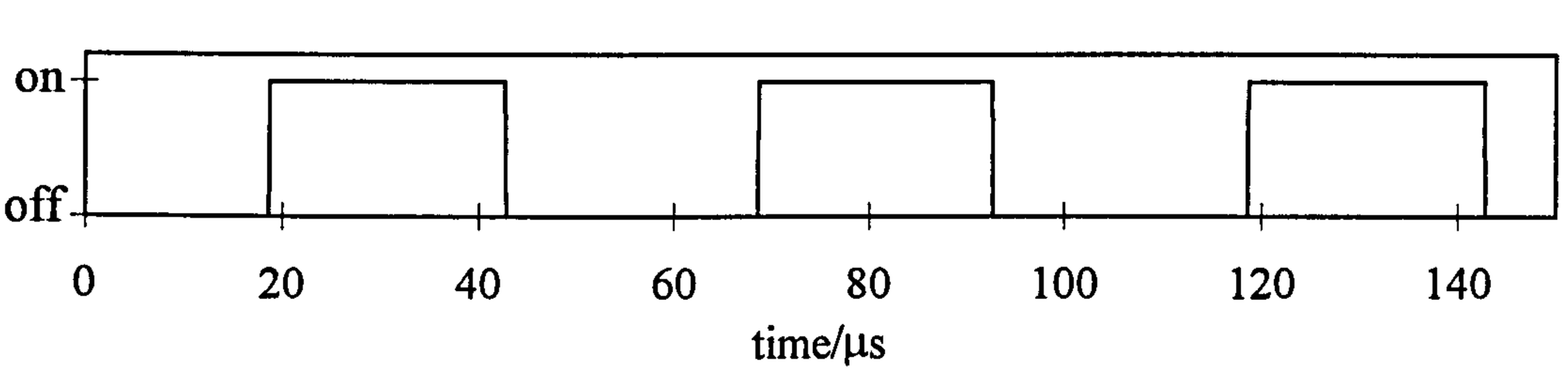


Figure A.3.10: Simulated switching pattern of switch S_2 of the ARPI topology

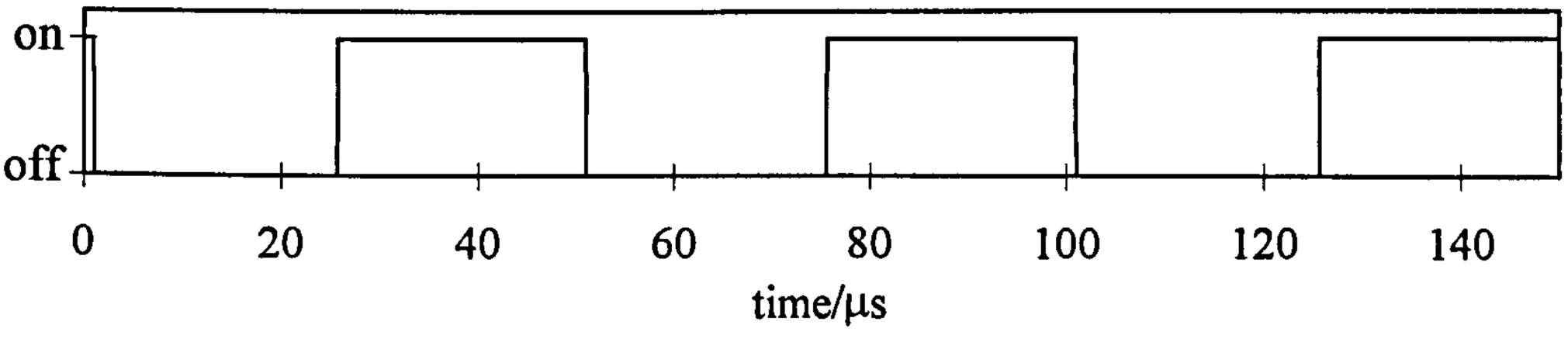


Figure A.3.11: Simulated switching pattern of switch S_3 of the ARPI topology

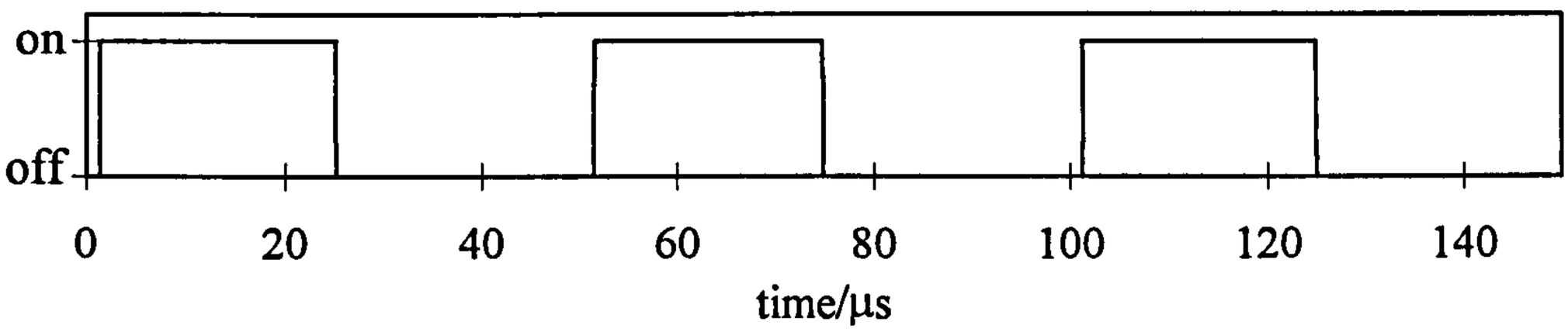


Figure A.3.12: Simulated switching pattern of switch S_4 of the ARPI topology

ACPI: L_r=5.7uH, C=67nF, I_{load}=100A

The ACPI is the only topology that makes use of the midpoint of the dc-link capacitors. Using the midpoint allows to apply three voltages on the output: dc-link voltage, half of the dc-link voltage and zero volts. The phase output voltage is shown in Figure A.3.13.

The current waveform looks completely different compared to the other ones (Figure A.3.14). No freewheeling current is needed. The ACPI was controlled without standard mode and direct resonant mode (Chapter 4). In case of a negative load current the large resonant current peaks of Figure A.3.14 would be in the negative direction and the small resonant current peaks in the positive one.

The switching pattern of the main switches are given in Figure A.3.15 and Figure A.3.16. Figure A.3.17 shows the switching pattern of both auxiliary switches. The on-state time of AS_2 is longer than the on-state time of AS_1. The overlap of the on-state times of AS_2 and MS_2 results in a ramp-up or ramp-down of the inductor current.

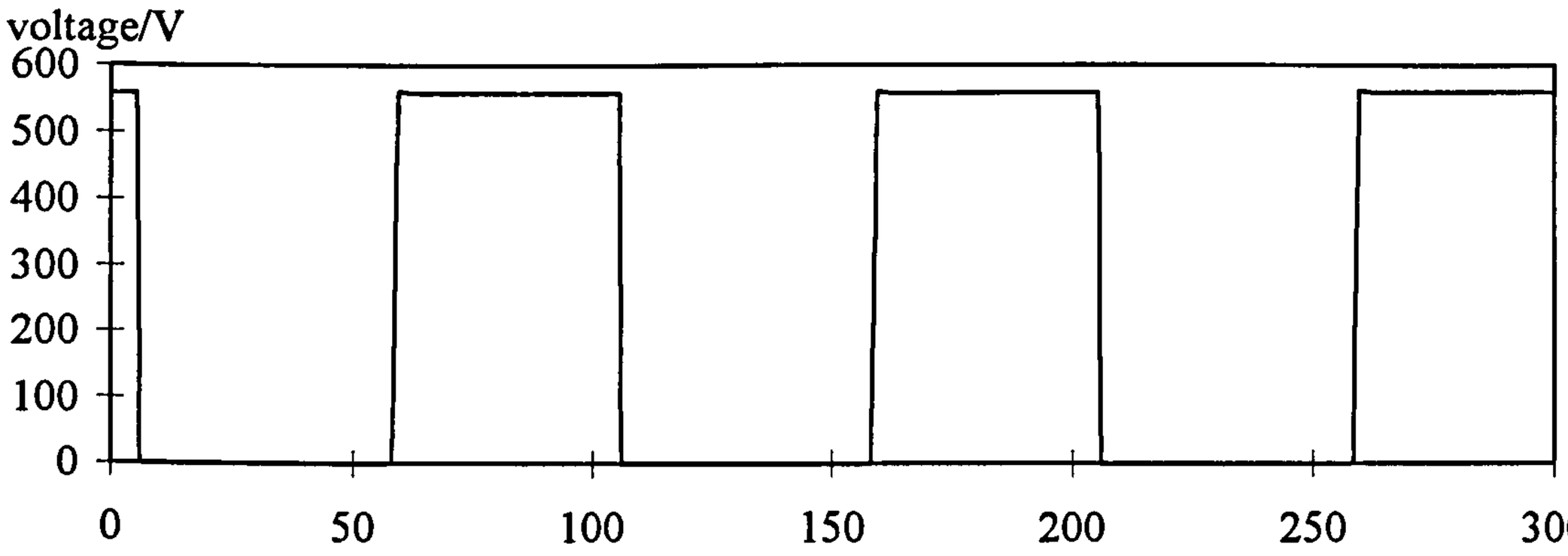


Figure A.3.13: Simulated phase output voltage V_{out} of the ACPI topology

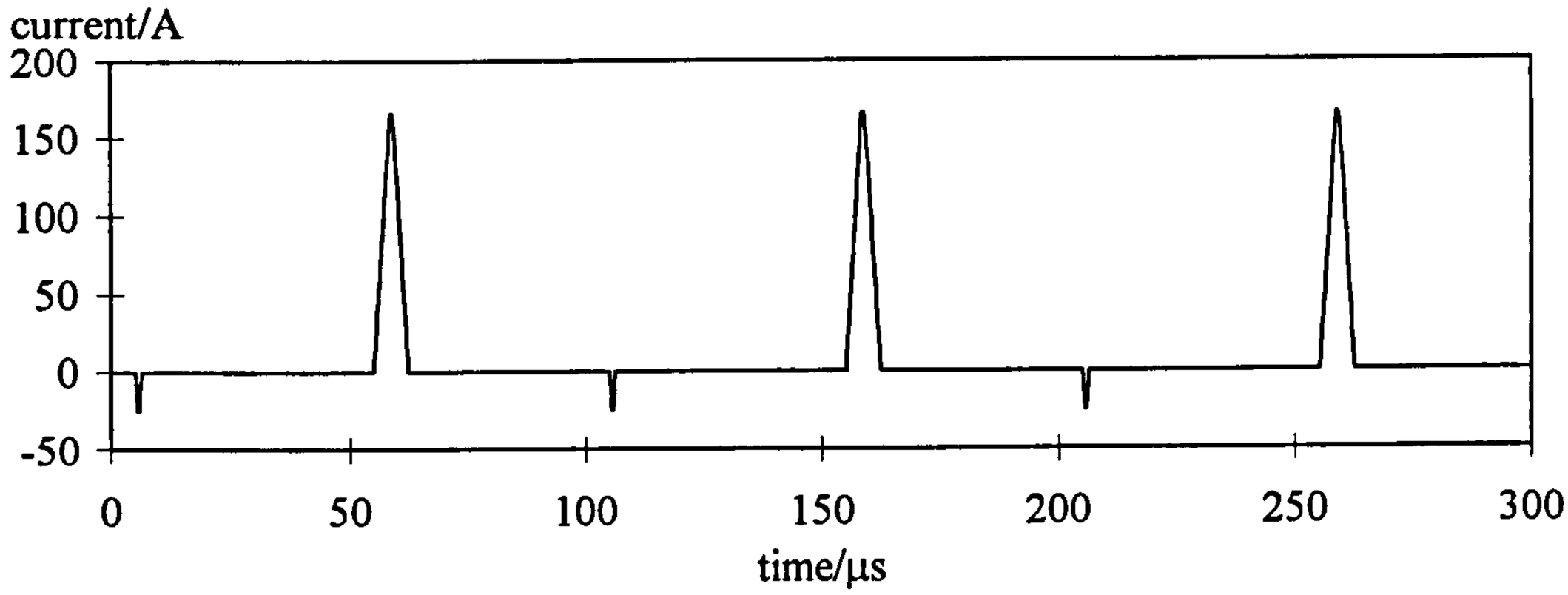


Figure A.3.14: Simulated inductor current i_r of the ACPI topology

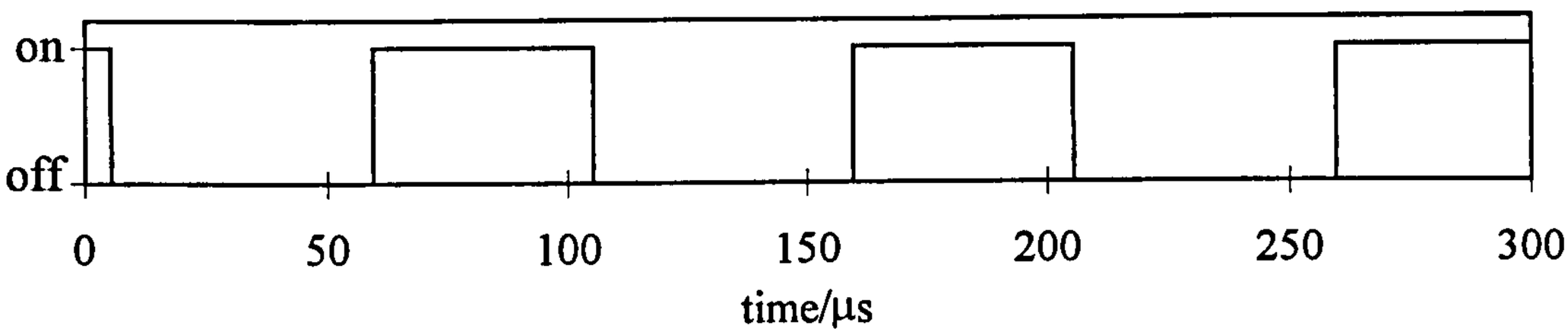


Figure A.3.15: Simulated switching pattern of main switch MS_1 of the ACPI topology

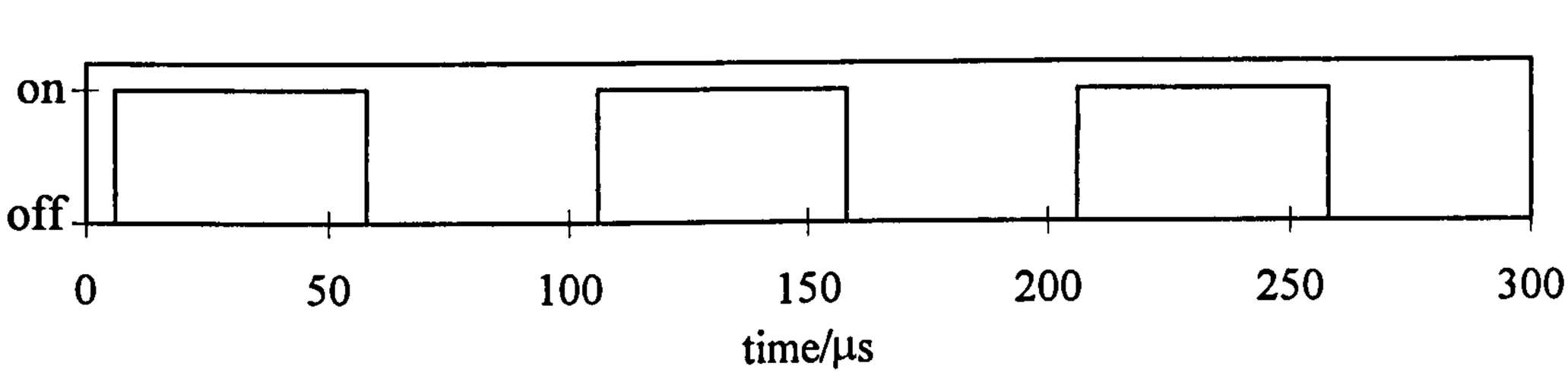


Figure A.3.16: Simulated switching pattern of main switch MS_2 of the ACPI topology

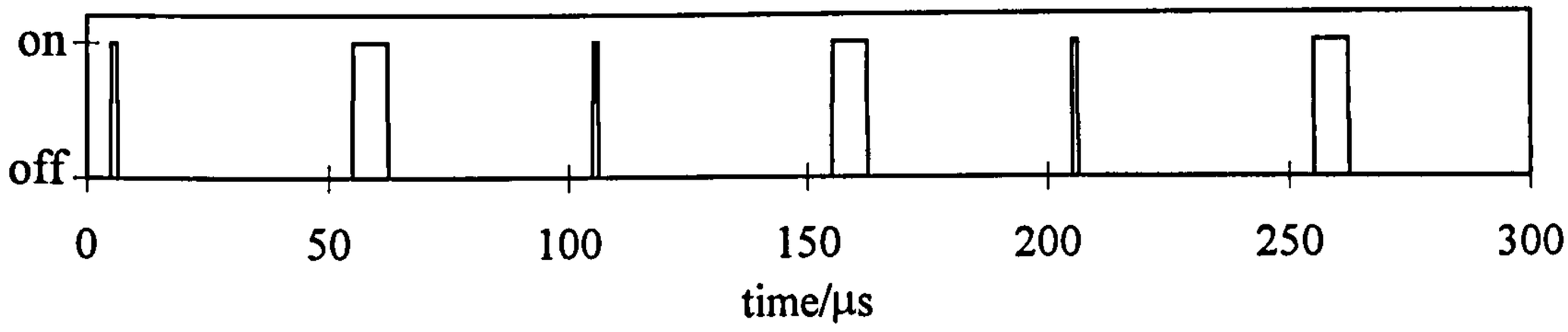


Figure A.3.17: Simulated switching pattern of auxiliary switch AS_1 (short pulse) and auxiliary switch AS_2 (long pulse) of the ACPI topology

Appendix B

ELECTRICAL AND ELECTRONIC CIRCUITS

Appendix B describes in detail the design of both power converters: hardswitching converter and the ACPI (Appendix B.1), the controller set-up (Appendix B.2), the used software and program given in pseudo code (Appendix B.3). In this Appendix the given circuit diagrams show only the function of the circuit and do not reflect the design of the circuit board. The same applies to the program which shows only the main structure.

B.1 Power Converter

The complete power converter is contained in a grounded metal box of the size (770mm*340mm*510mm). The metal box yields as electro-magnetic shield reducing emission and interference of electro-magnetic noise with its environment. The converter is earthed at one point only, because several ground connections with individual leads would increase the noise on the power supply lines resulting in ground fluctuations and voltage surges. All isolated metal objects inside the converter are connected to earth prohibiting floating potentials. Power is provided from a 3-phase power supply without neutral connection. The auxiliary power circuit is fed from a 240V single phase power supply.

B.1.1 Input side

The input side of the converter includes the rectifier, dc-link filter and dump circuit. The input rectifier and dc-link filter converts the ac supply voltage into a dc-voltage. As Figure B.1.1 shows, the rectifier is preceded with a contactor, fuses and an emergency stop. The contactor disconnects the input side of the converter with the ac power supply and is used as a main switch and emergency fault switch. In case the converter detects a fault signal the contactor disconnects the input of the rectifier with the output of the power supply. Likewise the emergency bottom disconnects both sides when manually activated. The fuses protect the rectifiers in the event of a short circuit across the dc-link. Using a 20kW three-phase power supply with fixed 415V line to line and 30A maximum rated current the rated current for fuses and diodes are given by the maximum rated phase current of the power supply. Thus, rated fuses of 32A (medium speed) and SEMIKRON diode bridge rectifiers (SKKD46/12) rated to 46A/1200V are in use. The

three phase rectifier is formed from three single phase bridge rectifiers. The diode bridge rectifier is mounted on a heatsink of 0.4°C/W. This value was calculated with the help of the data book from reference [B.1]. The dc-link inductor performs the functions: providing a second order filter with the dc-link capacitor and to help limit input supply current peaks during initial charging of the capacitors, whilst running. The dc-link filter has a cut off frequency of 43Hz, which gives 34dB attenuation at 300Hz, the fundamental ripple frequency. In consideration with the given rated voltage of an electrolytic capacitor, the allowed maximum ripple current and its capacitance, two in series electrolytic capacitors rated to 385V each and 18.5A ripple current at 100Hz are used in the converter design. Both capacitors have a capacitance of 6800μF. One has to be aware that a reduction in capacitance leads to an increase in the ripple voltage, and a reduction in stored energy and impedance, which is not preferred in drives application. Before activating the inverter switches of the converter the dc-link capacitors have to be pre-charged to around 560V, otherwise a substantial inrush current will flow into the capacitor, damaging the diode bridge rectifier. To limit the current a 220Ω resistor is connected in series with the choke inductor. Once the dc-voltage reaches its level the resistor is manually short circuited via a switch. In addition a second problem occurs when using dc-link capacitors. That is because, the full dc-link voltage still remains when switching off the converter system. To comply with safety aspects the capacitors have to be discharged, requiring resistors in parallel to be connected to the capacitors. The discharging process takes place with 10kΩ resistors given a discharging time of approximately 340s. The resistors are rated to 25W power dissipation. The function of the dump driver was already discussed in Chapter 6. Although no regenerating power is provided in the experimental set-up a dump driver was included allowing motor drive for future work. The dump circuit dissipates the energy in an external dump resistor. The size of the dump resistor and the dump IGBT is dependent on the generated power. The dump circuit has to be designed to carry at least the maximum transferred power during motor drive. Thus concluding that the dump resistor dissipates 20kW at 560V dc-link voltage with an average dump current of 36A. However not knowing the parameters of the machine and the mechanical load the dump IGBT is over dimensioned to twice of the calculated current of 36A. Thus without changing the dump circuit a range of freedom is given when choosing the motor and its application. The Toshiba module MG75Q2YS1 (75A/1200V) provides the dump IGBT. An IGBT module has the advantages of using the lower IGBT as dump IGBT and the upper antiparallel diode as free-wheel diode. A free-wheel diode is connected parallel to the resistor bank providing a current path for the stored current in the parasitic inductance of the resistor bank, during the turn off process of the lower IGBT. The module is mounted on a heatsink of 0.5°C/W with

respect to a 20kW load. The introduction of a snubber circuit parallel to the dump IGBT was seen as nonessential, but can easily be mounted across the module.

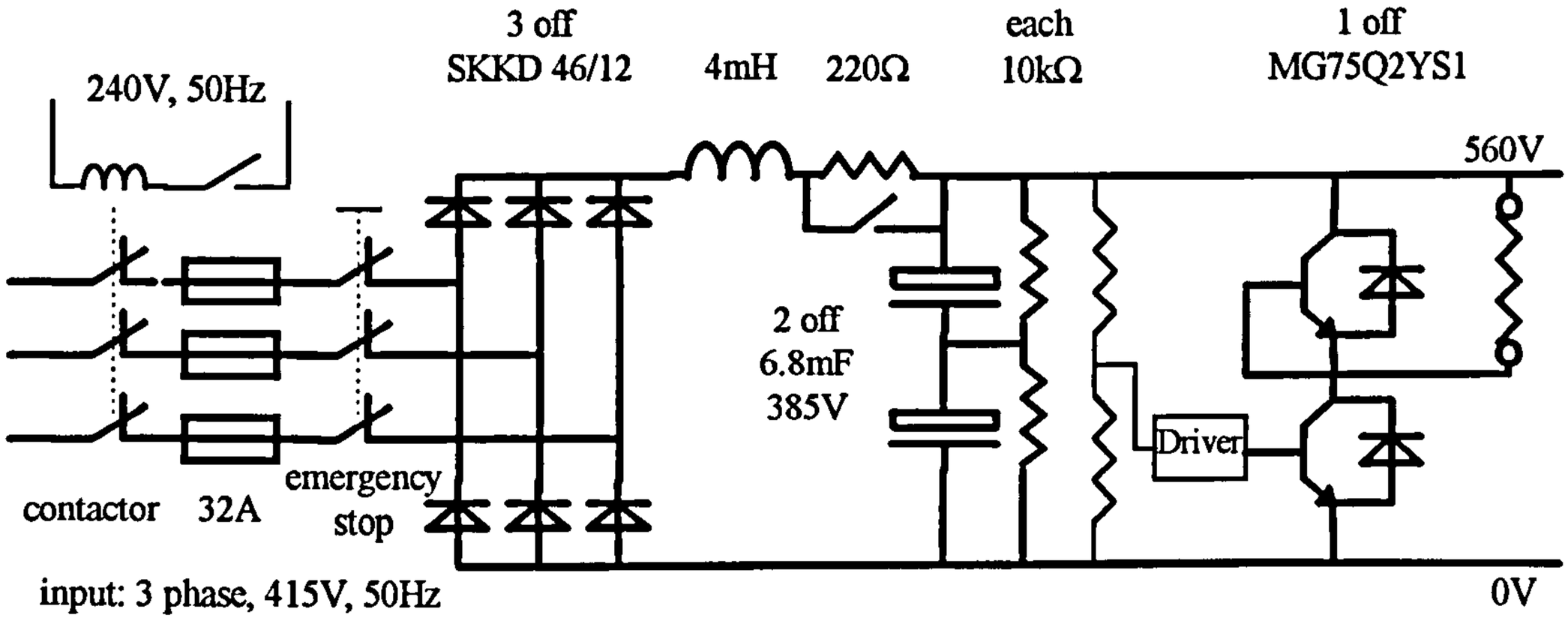


Figure B.1.1.: Input side

The supply voltage of the whole dump driver is isolated from the main auxiliary supply as seen from the electric circuit board in Figure B.1.2. The dc-link voltage is divided into a lower voltage amplitude allowing manipulation of the input voltage. The voltage is than compared with two different stabilised reference voltages. One comparator detects overvoltage at 700V and the other comparator detects undervoltage at 300V. In case an overvoltage is detected the dump driver switches on the dump IGBT. To turn off the dump IGBT the dc-link voltage must drop under 600V. In case the dc-link voltage drops below 300V an undervoltage fault signal appears. At 460V the undervoltage fault resets. An opto-coupler is used to drive the gate of the dump IGBT. The purpose of the opto-coupler is not to provide isolation but to allow to charge and discharge the input capacitance of the dump IGBT with a relative high current. In this case the opto-coupler provides an impulse current of 0.5A. The gate of the upper IGBT is short circuit with its emitter allowing a permanent turn-off of the upper IGBT.

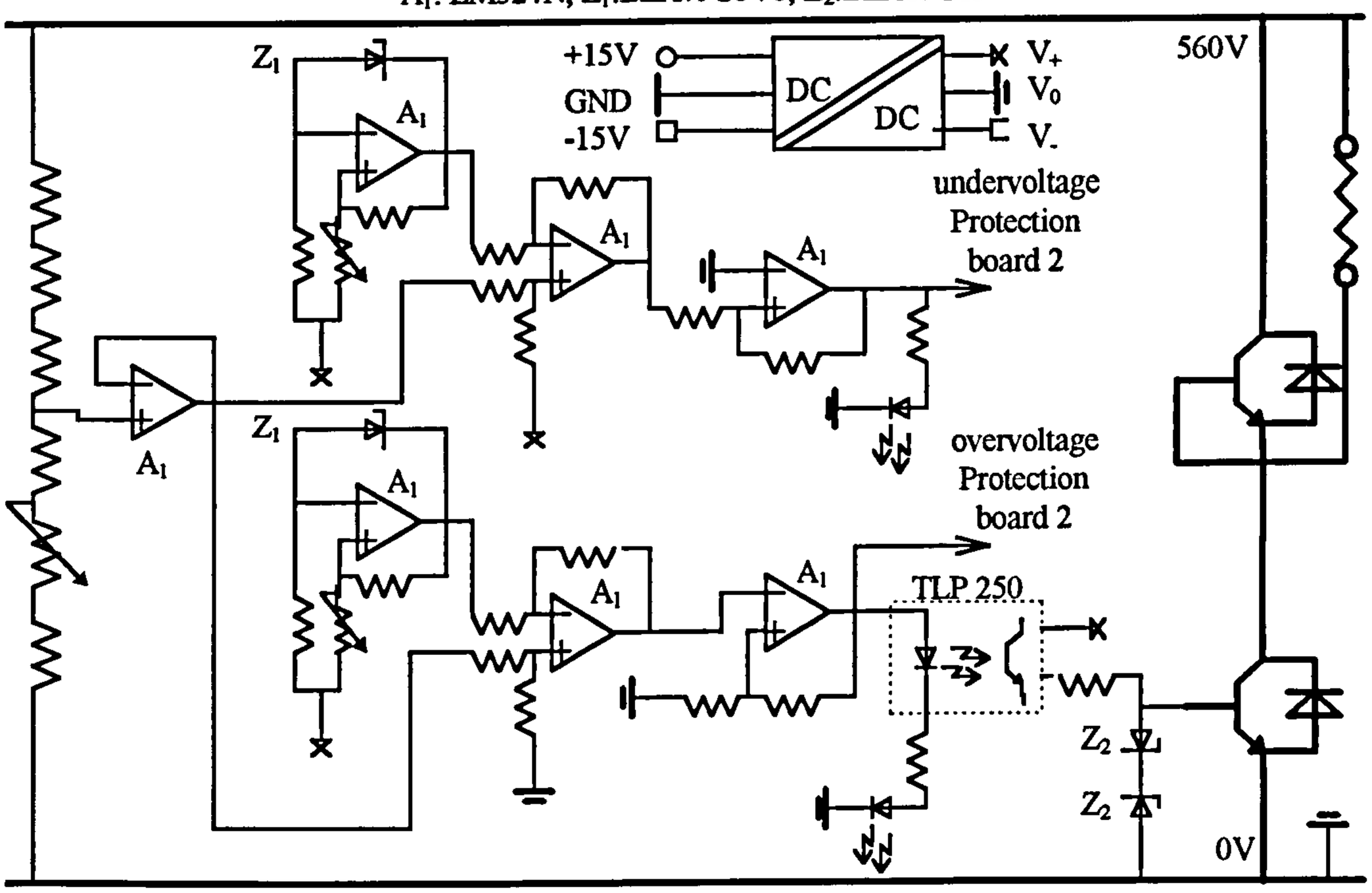


Figure B.1.2: Dump driver circuit

B.1.2 Drivers for main and auxiliary IGBTs

The driver requires isolation between the high voltage path and the low voltage path of the dc-link voltage and the auxiliary voltage. The low side of the driver is non-isolated to the auxiliary power supply, so the ground paths of the low side is earthed. The high side supply is transformer isolated and an impulse transformer is integrated in the used driver IHD680AN [B.2]. High and low side are supplied from a regulated 5V voltage regulator (L7805CP). Further requirements on drivers are noise immunity, internal undervoltage protection and protection in the event of power circuit fault. The driver IHD680AN from Concept provides a common mode immunity of 50kV/µs and makes it suitable for high speed power circuits. In case the auxiliary power supply drops to a certain voltage level a proper driver function is not guaranteed. Thus the driver shuts down and disengages the IGBT. The voltage saturation protection protects against unexpected high currents flowing through the device. In that case the driver starts to turn off the IGBT and all incoming signals are inhibited. This status remains in a pre-set inhibition time. The time is set by the user. In addition the driver flags back a fault signal to the low side. It was measured that a fault at the main IGBTs is detected at around 5µs and in case of the auxiliary IGBTs the detection time is 2µs. The driver is developed in such way, that an inhibition time of 20ms must pass before the driver allows again to transmit incoming signals. In addition it was chosen to use the fault signal of the low side as interrupt signal

for the PWM card. Consequently all IGBTs switch off when a fault signal is detected. In addition the contactor is commanded to disconnect the power lines between the rectifier and the power supply. The electric leads between driver cards, PWM card and protection board 2 are connected with transceivers MAX490. The slew-rate of the MAX490 is higher than of its counterparts and the MAX490 is equipped with circuitry allowing error free data transmission up to 25Mbps [B.3]. The Concept driver provides a maximum output current of +/- 8A allowing fast turn-on and turn-off of both main and auxiliary IGBT. This high charge current is needed when using control of IGBTs in resonant converters. Figure B.1.3 shows only one trail of the drive circuit. Two trails were combined in one circuit etched driver card controlling two IGBTs in one module (see Appendix E).

B_1:74HC04; Tr_1:MAX490; T_1:2N2222A; D_1:1N4007; D_2:1N4148; Z_1:BZX85C16; Z_2:BZX85C15;
Z_3:BZX79C4V7; Tr_1=Transceiver

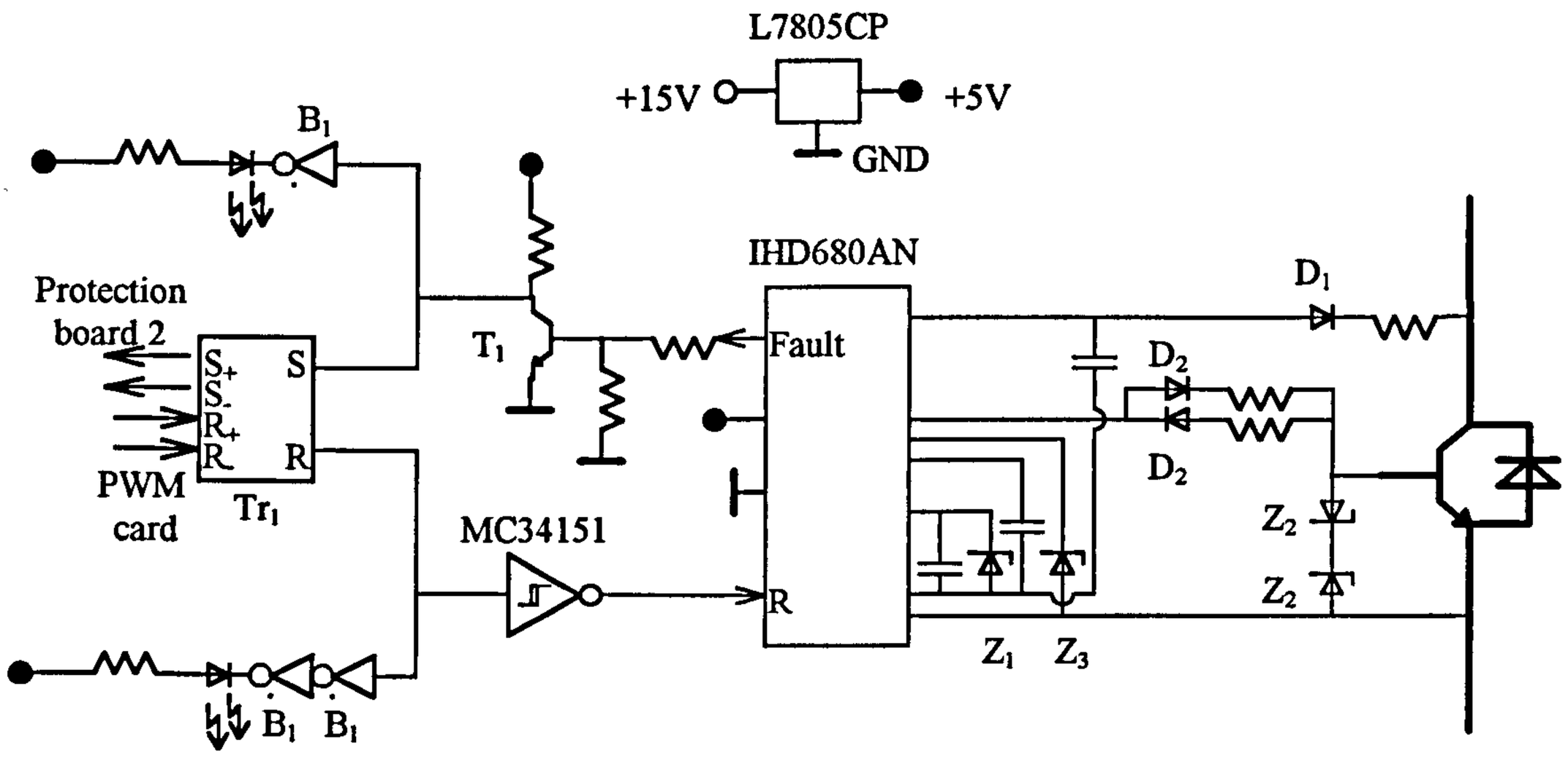


Figure B.1.3: Driver circuit for one IGBT

B.1.3 Phase Output Current

Phase current is measured using a Hall effect current transducer, LTA50P/SP1 (Figure B.1.4). This meets the basic phase current measurement targets of a peak current rating to 50A, bandwidth of DC to 150kHz, and isolation from the power circuit. A load resistor converts the output current into a voltage which is than multiplied by an amplifier OP470-6P. It was chosen for this relative expensive amplifier, because it offers very low input offset current, voltages for precision operation and low drift, sufficient gain bandwidth for the application and reduce errors due to ground noise and power

supply fluctuation. Because only five values are measured (three phase currents, dc-link voltage and mid-point voltage), accurate current measurements are vital. The amplified signal is filtered using a second order Butterworth filter. This filter limits the transmitted noise from the power phase line to the isolated current sensor circuit. Finally the output voltage is offset corrected using a potentiometer. The signal is than transferred to the analogue/digital card of the controller and to protection board 1. To allow accurate current measurements, the values of all resistors used in the phase current sensor circuit have a precision between 0.1% and 1%.

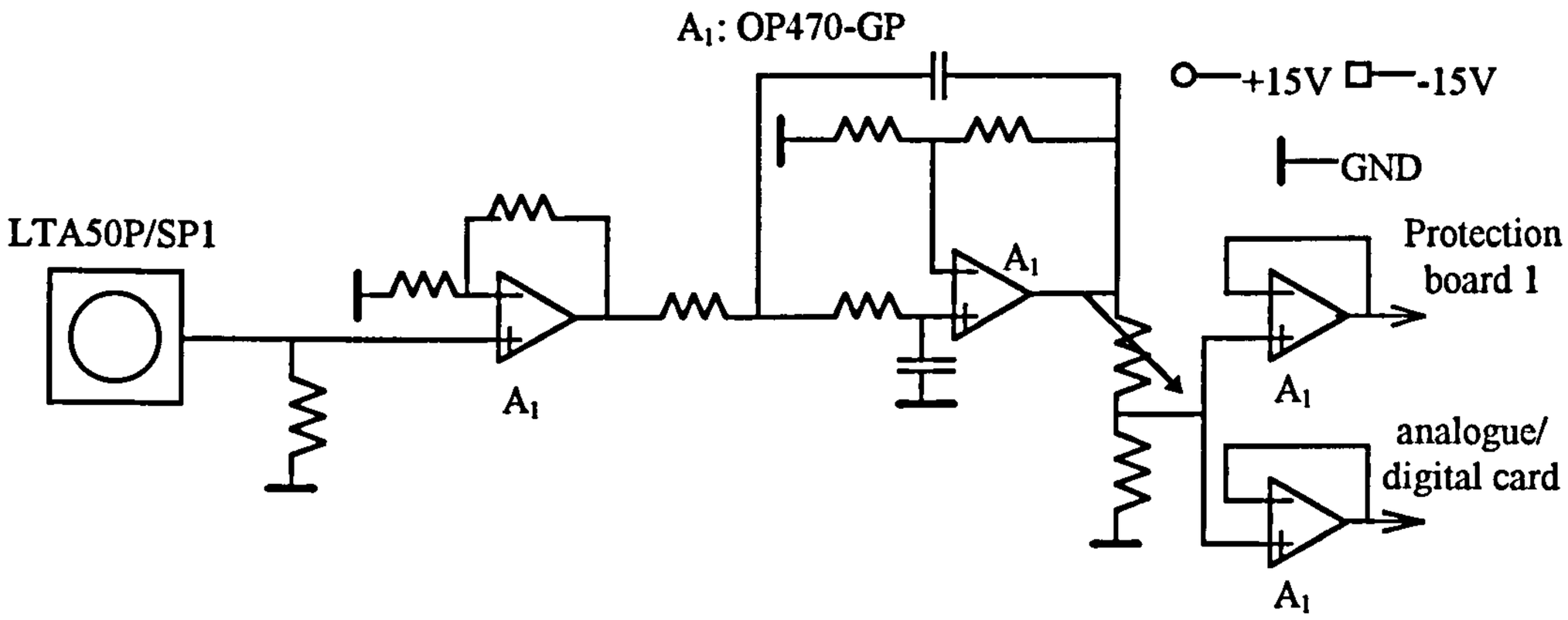


Figure B.1.4: 3 off phase current sensor circuits

B.1.4 Voltage Measurements

The dc-link voltage divider gives a 100:1 attenuation ratio so that the voltage can be safely read from the analogue/digital card of the controller (Figure B.1.5). The first stage divides the dc-link voltage down to a value determined by the quotient between the resistance among the non-inverted input of the amplifier and ground and the resistance among upper rail and lower rail of the dc-link. The second stage of the circuit adds this voltage together with a reference voltage. It was decided to set the reference voltage to 3V to be adequate to 300V dc-link voltage. That is equal the threshold voltage of the undervoltage protection. In addition a small range of reference values allow a higher resolution of the analogue/digital card of the controller. In the event that one of the top end resistors gets shorted or one of the bottom end resistors open circuit, the voltage rise up to either plus or minus of the maximum auxiliary supply voltage. The interrupt routine program reads this as undervoltage or overvoltage fault and turns-off the switching devices.

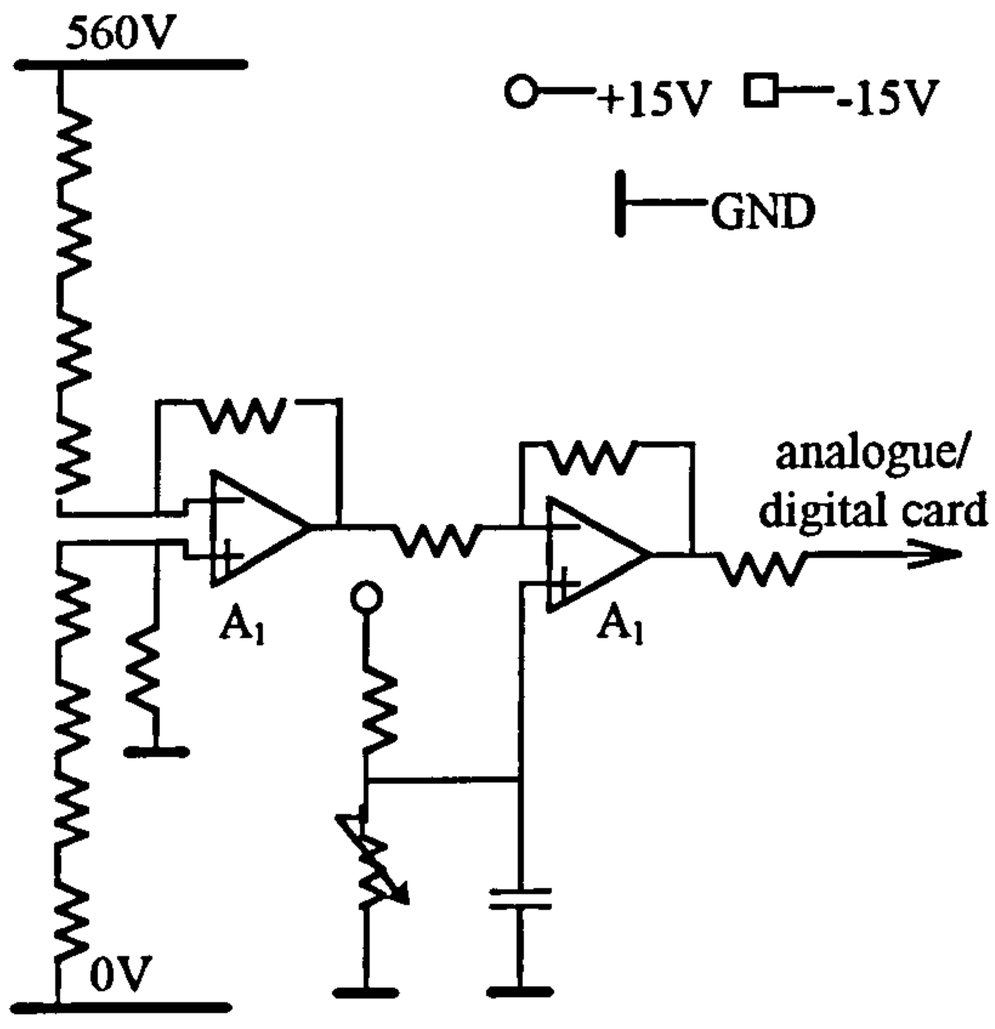


Figure B.1.5: DC-Link voltage measurements

B.1.5 Protection Board 1 (overcurrent and overtemperature)

Figure B.1.6 shows the circuit board of protection board 1. The measured current is compared with a hysteresis controller. The maximum current band of the controller is adjusted with trim potentiometers. If the phase current overshoots to +/- 50A than a fault is detected and the hysteresis controller triggers a delay-flip-flop (D-FF). The D-FF captures the fault and indicates that a fault occurred at this specific phase. The indication has to be manually reset. In case the heatsink temperature increases to over 110°C/Degree the resistor of the hysteresis thermostate changes immediately its resistance. Under 'cold' conditions the resistance is small and the base-emitter voltage is too low to turn-on transistor T_1. Under 'hot' conditions the resistance changes immediately once its reached the internal threshold temperature of the thermostate. The voltage skips and transistor T_1 turns-on. The conducting transistor is forward biased and a LED indicates the fault. The fault signal of the over temperature circuit or the over current circuit is send to protection board 2.

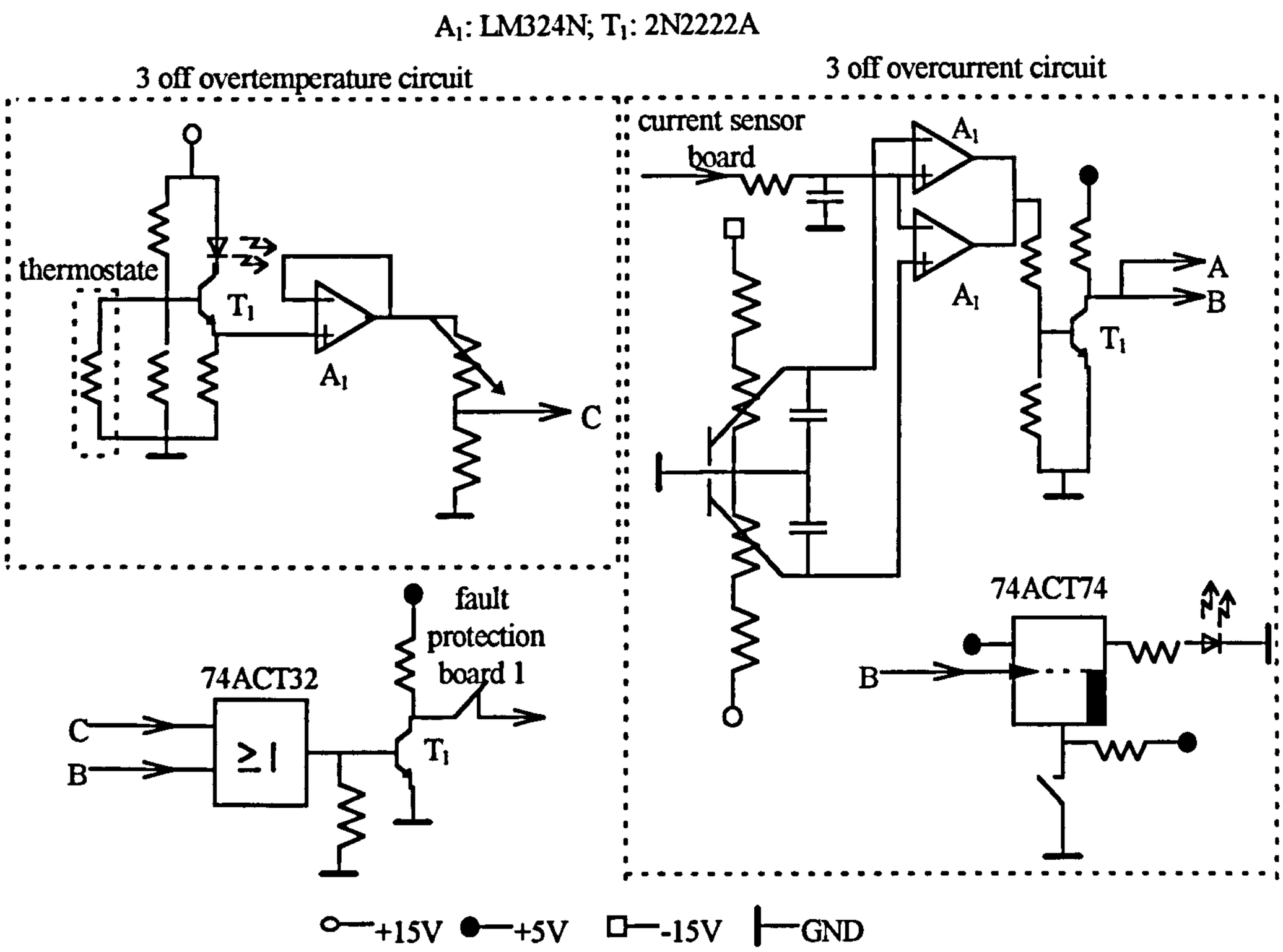


Figure B.1.6: Protection board 1

B.1.6 Protection Board 2

All fault signals gather together in protection board 2 (Figure B.1.7). The fault line from protection board 1, the undervoltage fault line and all fault lines of all twelve IGBT drivers are connected to a high speed or-gate 74ACT32. If only one fault is detected the contactor is commanded to switch off and the PWM card inhibits further data transmission. Faults send from the driver cards are captured and signalised, allowing to identify the faulty IGBT. The contactor still remains closed when only the overvoltage fault occurs. Is this the case only the devices are switched off. All D-FFs must be manually reseted before enabling control transmissions to the driver cards.

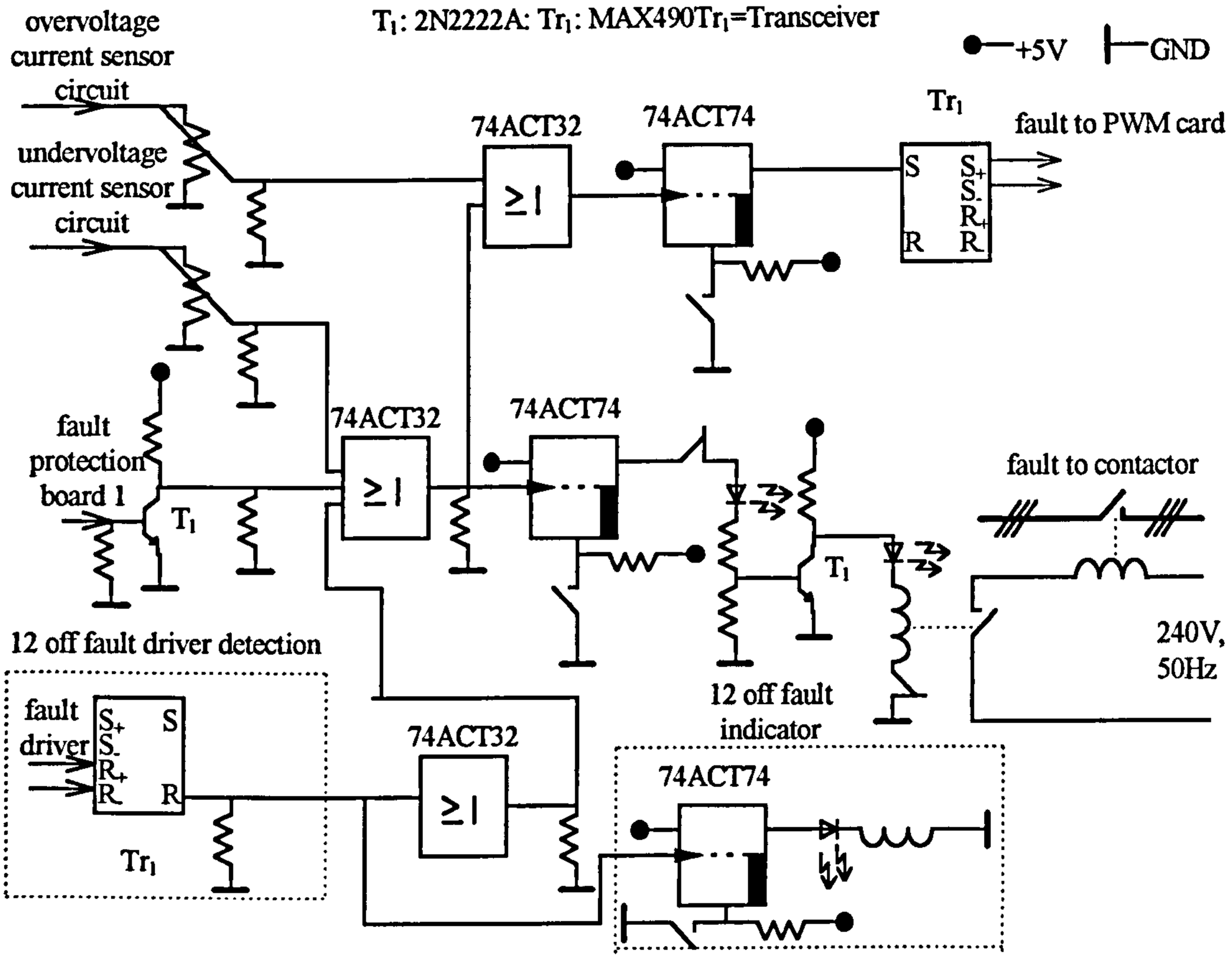


Figure B.1.7: Protection board 2

B.1.7 Auxiliary Power Supply

Two regulated voltage dc power supplies provide the total power of all circuits that have been discussed so far. The NFS40 power supply is a non-isolated AC-DC converter with a nominal power rating of 25W. The output voltage is +15V, -15V, +5V and GND. Two NFS40 supplies have been connected in parallel. This arrangement allows to provide the circuits with enough auxiliary power and protects the converter in case of an auxiliary power supply failure. In case one of the power supplies fails, the other power supply have to provide twice of the power. That results in a output voltage drop of the single NFS40. This drop is seen from the driver IHD680AN of the driver card. The internal undervoltage protection responses to switch off the IGBT and signals a fault signal.

B.1.8 Output side

The IGBT module Toshiba MG150Q2YS11 are integrated in each pole of the inverter bridge. This low saturation 3rd generation module is a compromise between cost and performance. In addition great power loss reduction is gained under zero-voltage

switching. This statement applies not for every device. An example is published in reference [B.4]. Their it was published that for example Siemens IGBTs, which have no doped lifetime killers, show no great improvement in turn-off loss reduction under zero-voltage conditions. It is concluded that NPT IGBTs (non-punch through) will have only a slight turn-off switching loss reduction with a capacitive snubber. The Toshiba module (150A, 1200V, 2.7V saturation voltage [B.5]) is a PT IGBT (punch through). Here the turn-off performance is better under ZVS (Chapter 5).

Each IGBT module is mounted on a heatsink with a thermal resistance of 0.4°C/W. Calculations on conduction and switching loss, of IGBT and diode using data sheets values show that under worst case conditions (switching 30A at 20kHz, with a dc-link voltage of 560V), results in losses requires fan cooling for heatsinks. However for a smaller duration of running time no fan cooling is required. In addition own estimations have shown that no fans are required when using the ACPI. Results of the loss calculations of the ACPI predicts that under proper zero-voltage and zero-current conditions the thermal resistance of the heatsink is sufficient when using the same heatsink for the ACPI, still during extend running duration.

Turn-off snubbers have not been used during test runs when the inverter was hardswitching. Likewise, no distributed snubbers across the dc-link were needed to suppress high frequency ringing.

Additional components needed for the ACPI are the IGBT modules of the auxiliary circuit, clamp diodes, resonant capacitors and the resonant inductor. In addition a small snubber circuit is implemented across the emitter of the first auxiliary switch and the emitter of the second auxiliary switch as seen in Figure B.1.8.

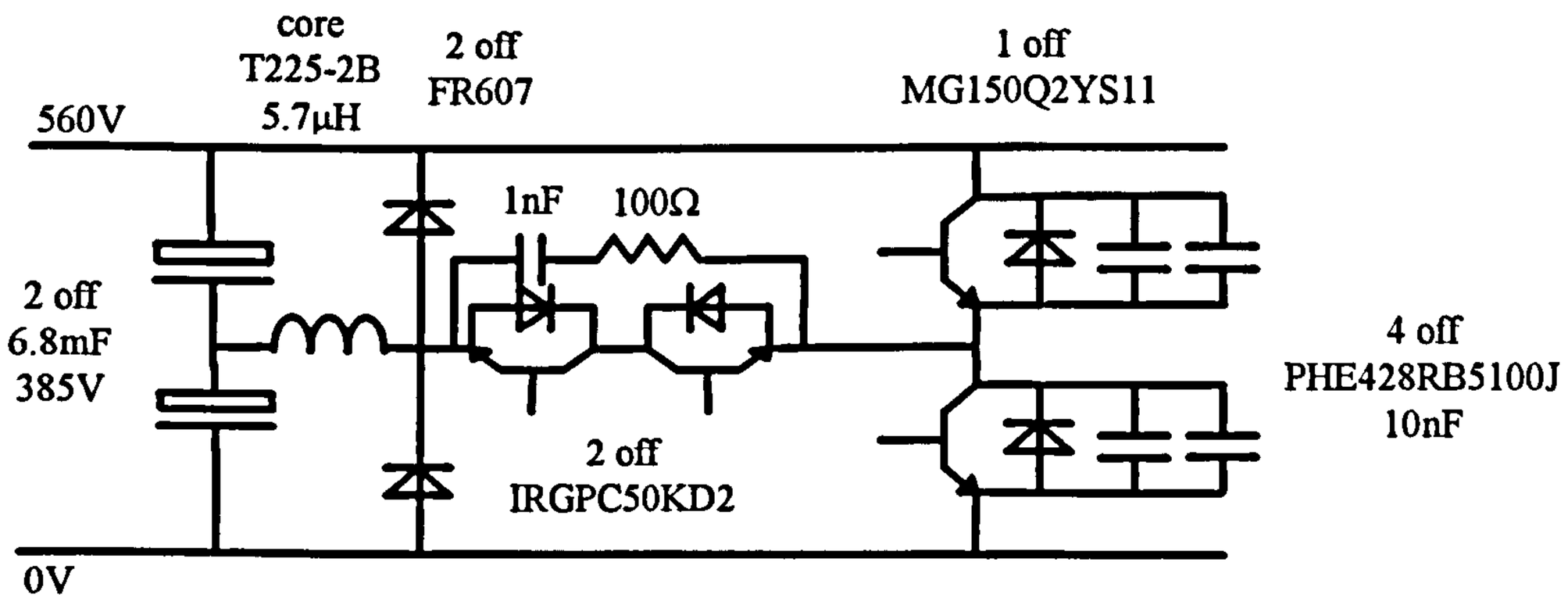


Figure B.1.8: Output side of the ACPI

The fast-recovery clamp diodes FR607 (6A/1000V) allow to turn-off the auxiliary devices in every converter status mode. Thus the stored current in the inductor can free-wheel via the diodes.

The auxiliary IGBT modules were chosen from International Rectifier (type IRGPC50KD2). This 600V, 52A device includes a ultra fast soft recovery antiparallel diode. Both, IGBT and diode, are rated to a maximum impulse current of 100A and are integrated in a TO247AC package. Two of theses modules are mounted on the heatsinks cooling the Toshiba modules. Thermally conductive isolator (Wart K177 material) provide thermal conduction and electric isolation between collector of the TO247AC housing and ground of the heatsink. To each Toshiba IGBT snubber capacitors are connected in parallel. In Chapter 7 it was shown the impact of the dv/dt stress under various resonant capacitors. During this test different Evox RIFA capacitors were used. This double metallized polypropylene capacitors (type PHE428RB5100J) withstand 1600V dc and 2500V/µs. Figure B.1.8 shows two 10nF resonant capacitors in parallel allowing an overall capacitance of 20nF. The resonant inductor was made of a litz wire winded around an iron powdered toroidal core from Micrometals. Ironpowder as core material is a cost-effective alternative to moly permalloy power or sendust [B.6]. The core permeability is given to $10\mu_0$ and the inductance rating (ratio between core cross section and square number of turns) to A_L=21.5 (nH/N^2). From reference [B.6] the inductance can be calculated to

$$L = N^2 * A_L \qquad \text{(B.1.1)}$$

(N comply with the number of turns)

The resonant current reaches peak values of 80A depending on the resonant capacitor and load. Thus during the whole resonant mode the inductance must stay constant otherwise resonance time and boosting time changes and therefore the estimated time values. In addition the magnetising current in the core has to stay outside the saturation. If the current reaches the saturation point the inductance becomes neglectable and no resonant transition occurs during the time where the current is outside the linear range of the B-H curve (saturation). The B-H curve of the resonant inductor was recorded (Figure B.1.9). The T225-2B is a 'soft' core material with a very small hysteresis band. In Figure B.1.9 the hysteresis waveform is averaged.

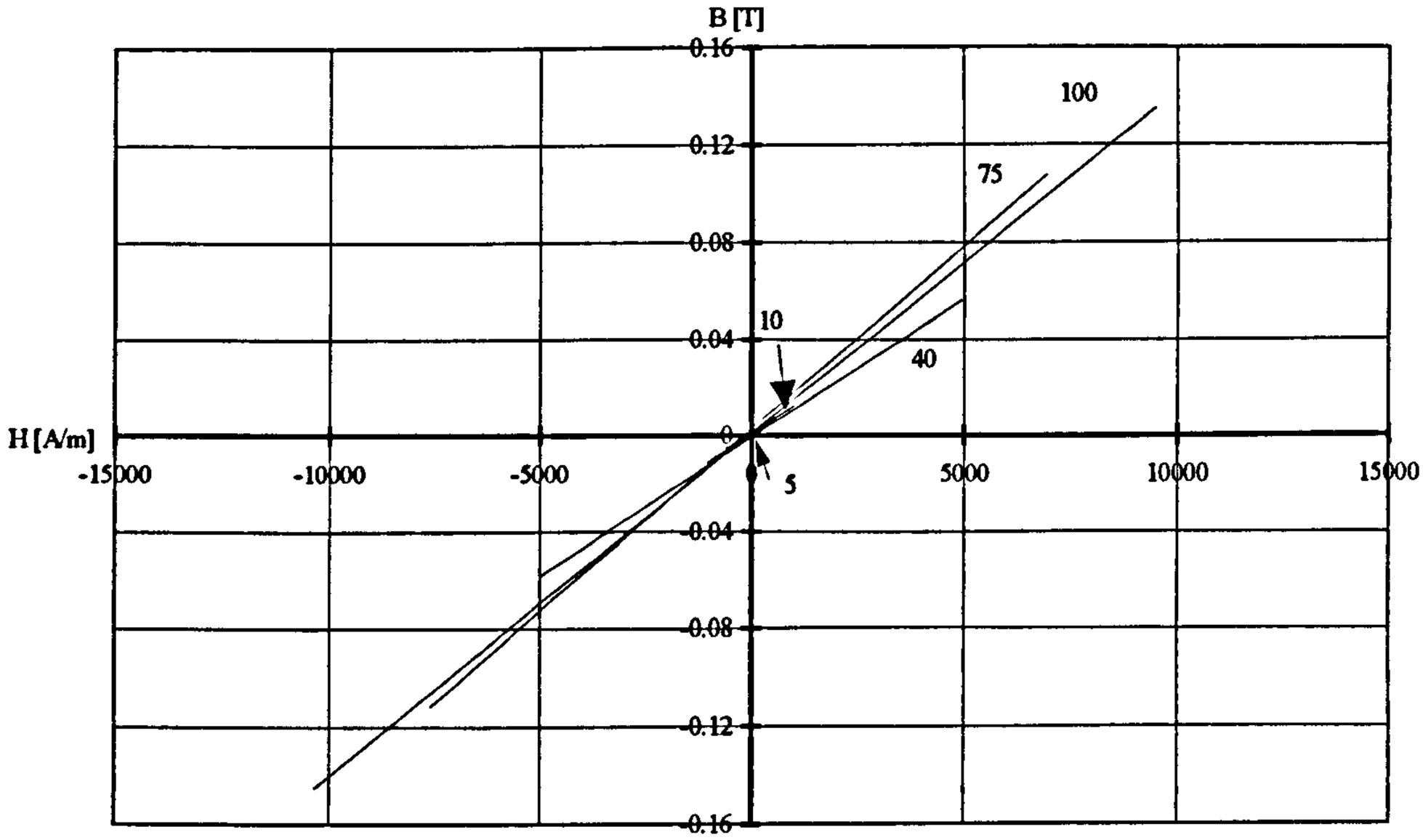


Figure B.1.9: Average B-H curve of the resonant inductor with the load current as parameter

Figure B.1.9 shows that no saturation occurs in the current range between +100A and -100A. The average B-H curve changes slightly with load current that results in change of the permeability and therefore in the inductance. The relative error of the inductance is between 1% and 5% with respect to the theoretical value.

As already discussed in Chapter 6 the RC combination across the auxiliary switches is needed to suppress the voltage ringing across both devices. The resistor is of value of 100Ω and the capacitor of 1nF.

B.2 Controller

It was decided, due to the experience and expertise present within the Electric Drives and Machines Group that the controller system should be based on the Texas Instrument DSP TMS320C3. In addition it was decided to take over circuit designs of the controller cards that have been optimised for drives control and that have already been developed in this Department. Rearrangements and upgrading of each circuit was made before use.

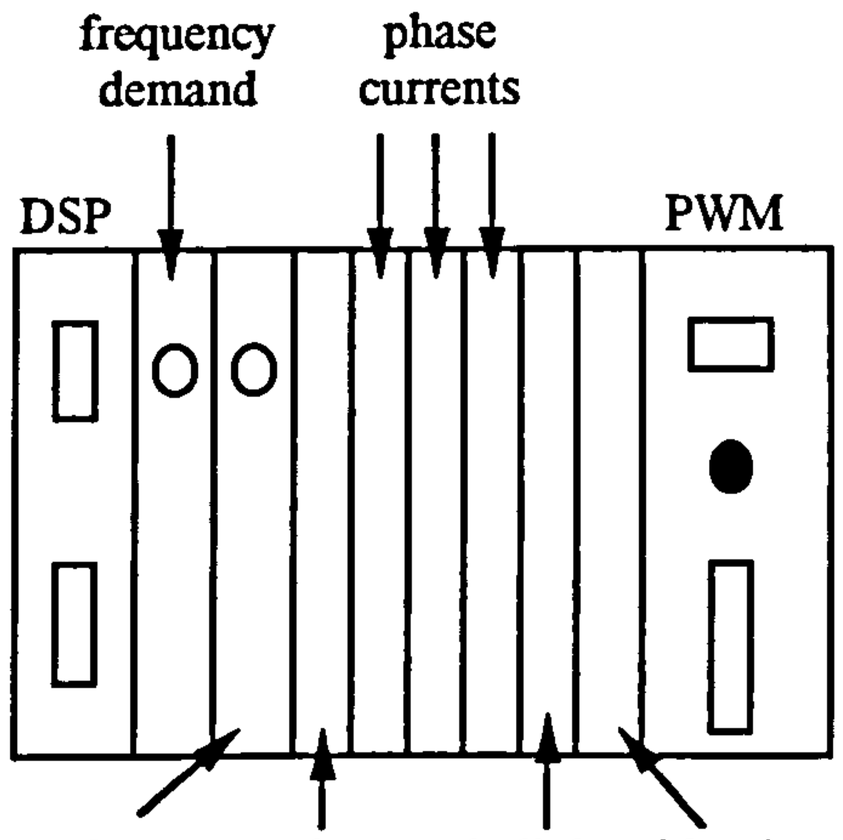


Figure B.2.1: Boards of the controller

Figure B.2.1 shows the controller including ten different controller cards fitted in a 3U 19'' rack with power supply and cooling fans. All cards are connected with a backplane (industrial standard) allowing to carry all required data, addresses, control and power lines. Card connection is provided with the DIN 41612 standard connectors. The DSP card includes a TMS320C31-40 processor clocked at 40MHz. The processor communicates with the PWM card which includes the FPGA XC3195APC84-5 from XILINX and the DSP is programmed from the emulator card TMS320C3X installed in the PC. In addition option is given to transfer data to the terminal of the PC with a serial link during idle processing time. Here phase current and dc-link voltage is monitored in quasi-real time. Two analogue cards define the demand values of frequency and voltage. Both are manually adjustable. The other five analogue/digital input cards convert the phase currents, the dc-link voltage and the midpoint voltage (ACPI only) into digital values readable for the processor. One digital/analogue output card allows to monitor one value under real-time condition on oscilloscope. The card was mostly used to monitor the demand output current of one phase.

B.2.1 DSP board

The Processor TMS320C31-40 (Version A) is a powerful processing chip from Texas Instruments. Highlights of the processor are: 60ns single-cycle instruction execution time, 33MFLOPS, 16 MIPS, flexible boot program loader, one serial port support 8/16/24/32 transfer and floating-point/integer multiplier [B.7]. In combination with the TMS320C3X XDS500 Emulator package from Texas Instrument and together with system memory on the DSP board the complete processing system is a very effective tool for drives applications. The package comes with a debugger that is able to trace the 'C'

code, compile and link it and debugger the code to the processor with the help of the XDS500 emulator (Version 2). The data transfers between TMS320C3X emulator PC board and processor is provided with a six wire high speed serial connection. Programs are loaded into DSP's RAM or into the external memory mounted on the DSP board. The static RAM (SRAM) chips on the DSP board have a memory of 32k*32 and use a 20ns access time. When this time is subtracted from the amount of time left in processor cycle (28ns with a clock of 40MHz) only 8ns is left, giving enough time for one F series logic gate needed for communication with the backplane. To communicate with the other cards the controller uses 16-bits data, 11-bits address, 4-bits handshake flags and three control bits: DSP clock (CLK), ADC clock (ADCC=interrupt) and DSP inhibition (INH) (Figure B.2.2). In addition the serial link port DSX0 is used to transfer data to the PC terminal and the time of the interrupt routine is monitored using an oscilloscope. All address lines are low except one which selects the area of memory. The four handshake bits are: activate backplane (LAS high when backplane is active), communication with input or output card (I/OF high when talking to input card), read-write (R/W high when reading) and strobe (STRB high when no data are read or write). Figure B.2.2 shows the interface between DSP and backplane. It shows that address and data lines are latched and buffered whereas handshake signals are only buffered.

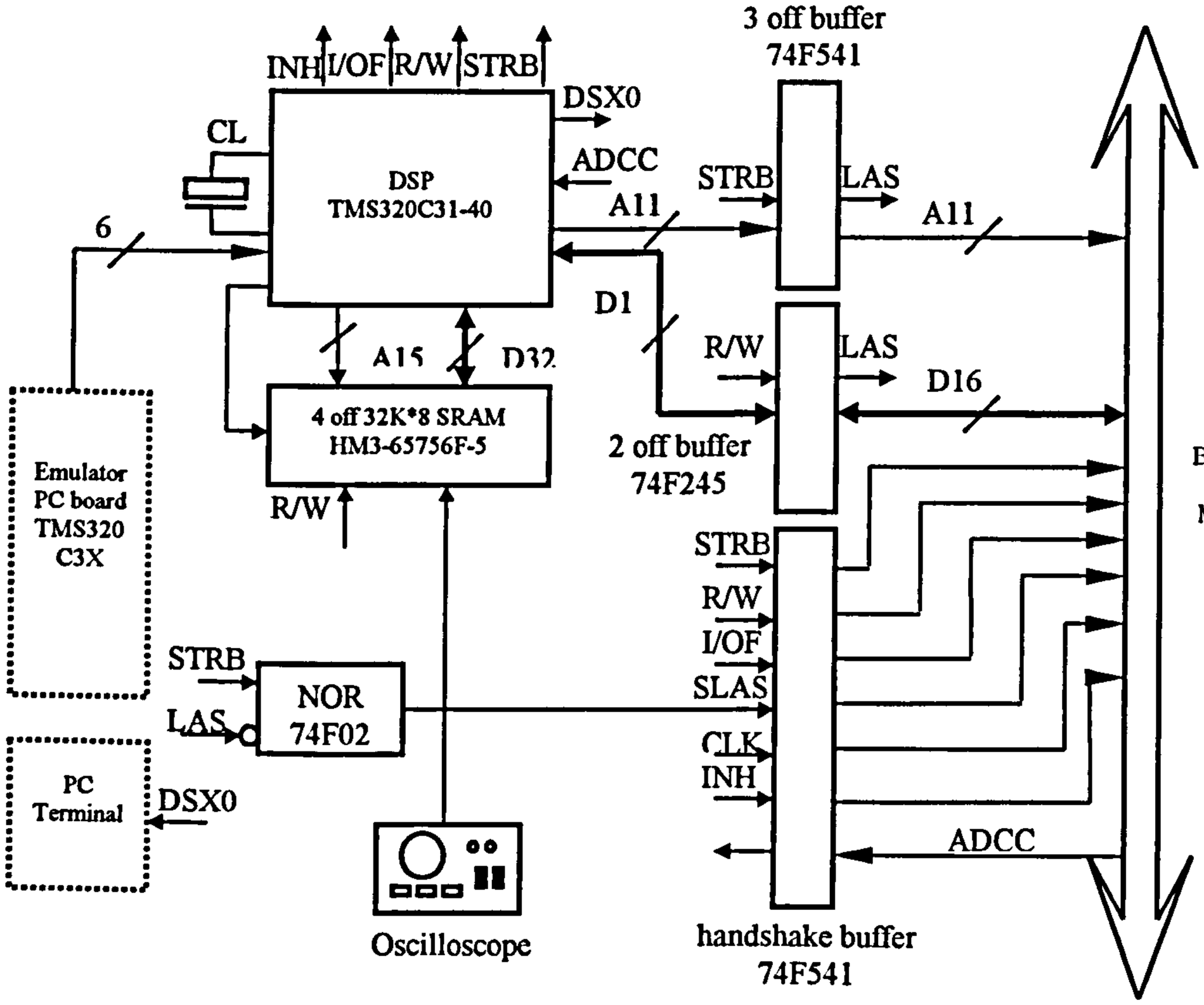


Figure B.2.2: Simplified schematic of the DSP board

B.2.2 PWM Board

The majority of work is performed by a XILINX FPGA XC3195APC84-5 which is configured by software held in a PROM (17128DPC). A crystal oscillator (20MHz) on the card clocks the FPGA with the PWM frequency being controlled by a divide down counter. The synchronisation signal is used as interrupt signal for the control system. The PWM output and control of the auxiliary switches is commanded by writing voltage references. Besides the FPGA and the PROM other components are used for interfacing, output buffer and opto isolation. Data buffering is incorporated on the input side to hold data for the FPGA to read while buffers on the output are necessary to supply enough current for the opto-couplers. External inhibits are provided to turn-off manually the IGBTs. All signals at the output of the FPGA are connected with transceivers 26LS31 allowing a successful transfer of data to the IGBT driver cards in a noisy electro-magnetic environment. Figure B.2.3 shows the schematic of the PWM board.

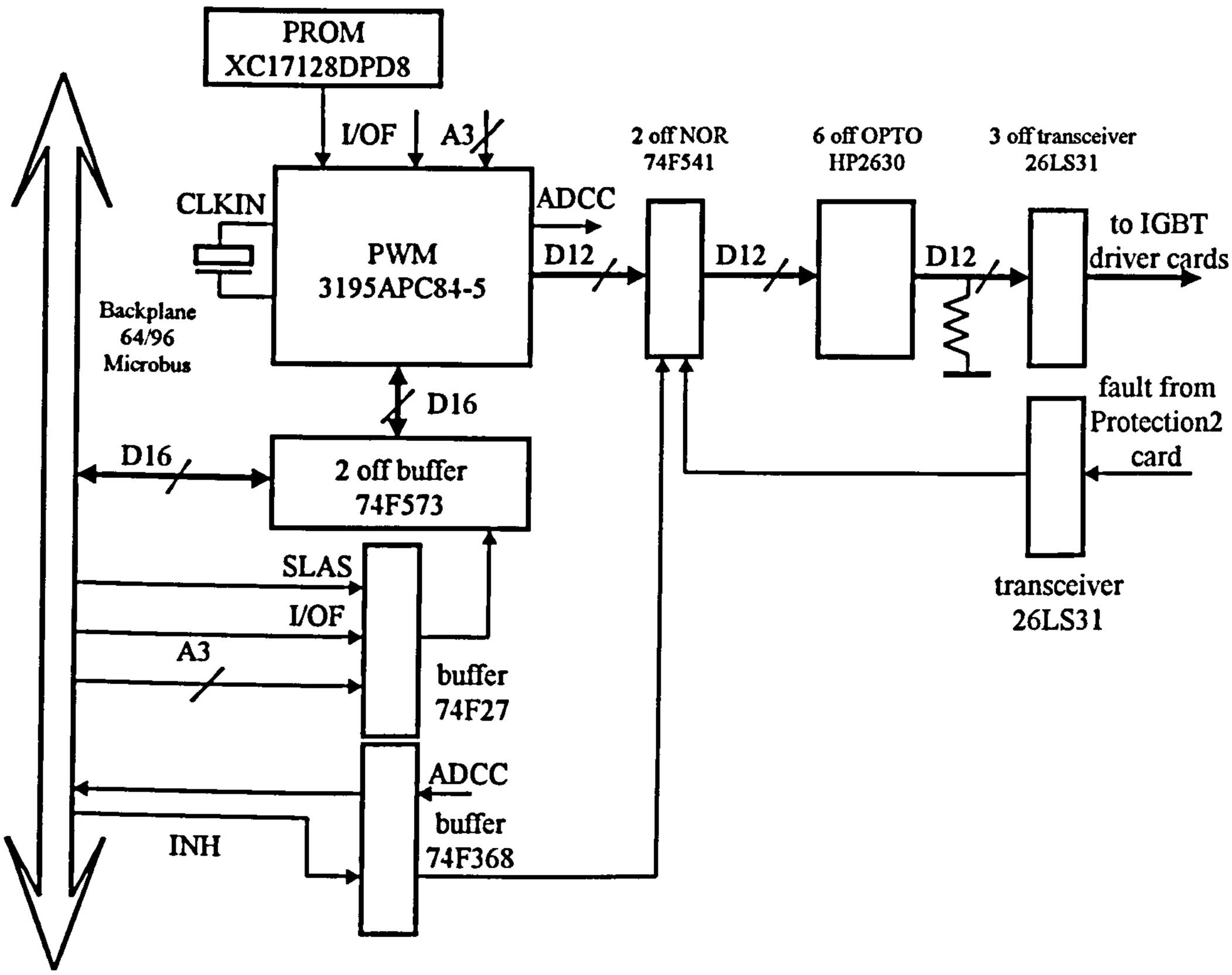


Figure B.2.3: PWM board

The software to the FPGA was developed using XILINX's Viewlogic software and its schematic is seen in Figure B.2.4. Figure B.2.4 shows that the voltage demand is

compared with an internal produced triangle signal. The output are signals that changes when the demand voltage value is larger or smaller than the triangle value. In case the demand voltage is larger than the triangle voltage, the auxiliary device AS2 must turn-on (SAS2 is high), in case the demand voltage is lower switch AS1 (SAS1) must turn on. The status of SAS1 and SAS2 and information about the modes, ramp time 1, reso time and ramp time 2, is feed into a statemachine. The statemachine reads data of the different modes that include the time delay specifications and applies the value into a down counter. The down counter counts until zero and changes the status of the Johnson Counter behind the down counter. A change in the Johnson Counter sets or resets the output flip flops in a pre-set order. This order can never change and once the Johnson Counter reaches the last state it is switched back to the top state. The decision which data must be loaded into the down counter depends on the status of the statemachine. In general a change in the statemachine activates the next mode of the following changes in the statemachine. Exceptions are the incoming signals SAS1 and SAS2.

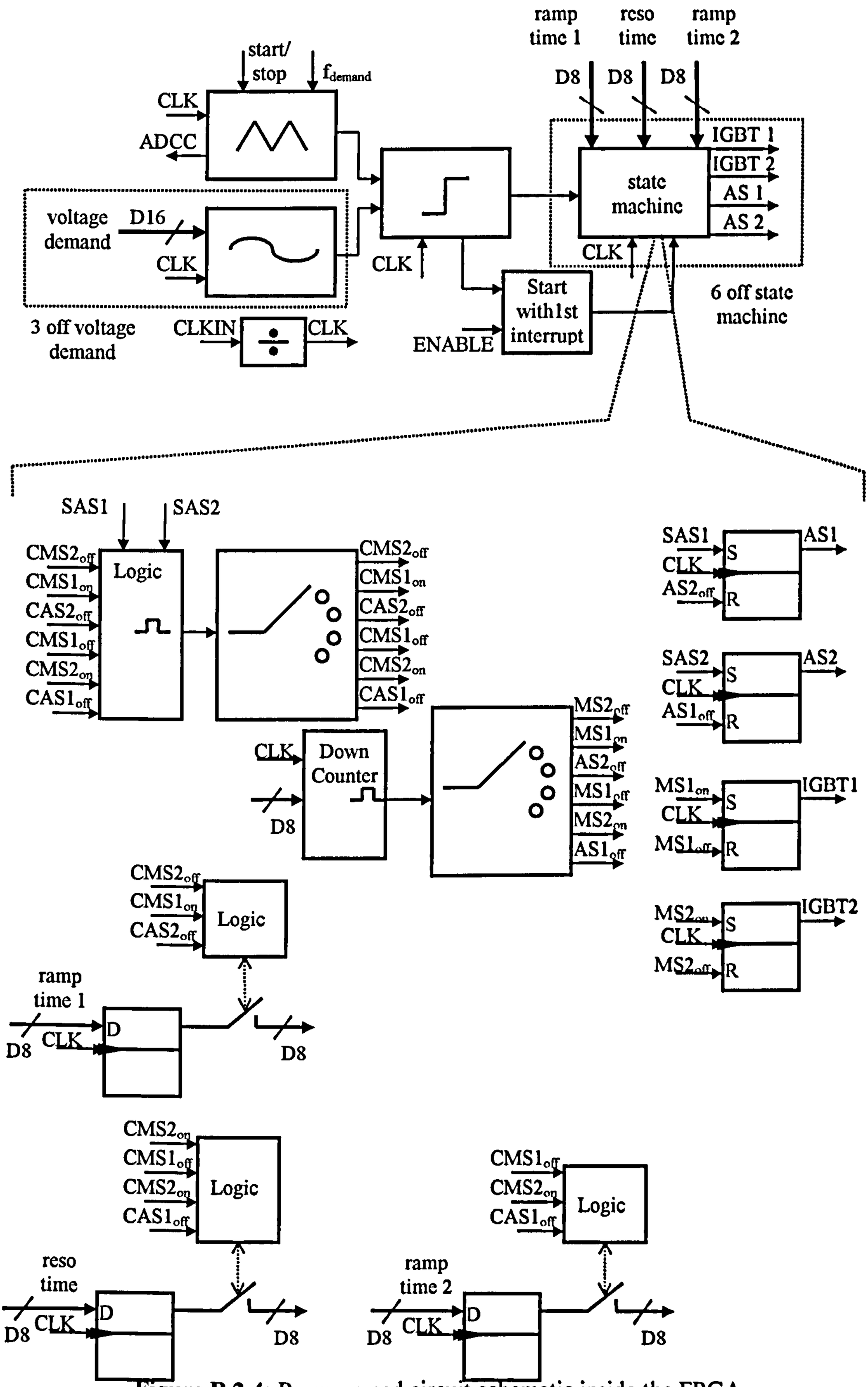


Figure B.2.4: Programmed circuit schematic inside the FPGA

B.2.3 Analogue/Digital Board

An overview of the analogue/digital card is shown in Figure B.2.5. The analogue signal is scaled in terms of gain and dc offset before going to the input pin of the ADC1061 10-bit flash converter capable of converting up to 600kHz. The ADC requires the signal at its input to vary from 0 to 5V, so the input signal must be scaled to achieve maximum resolution. When the data have been converted to its digital equivalent, the ready line on the ADC goes high. This ready line is used to latch data into a buffer, the output of which will always have the last converted data stored. The latch 10 bits of data then transmitted to opto isolators to backplane latch. Once the PWM board signals an interrupt the interrupt is deliberately delayed sampling the analogue/digital card from the DSP. That has the advantage to read the latest current value stored in the latch direct before the next interrupt occurs. Note that the clock (CLK) signal is also isolated before reaching the ADC. This, together with power supply isolation, ensures that the analogue circuit is isolated from the backplane, and hence other channels. The resulting bandwidth of the board is 600kHz.

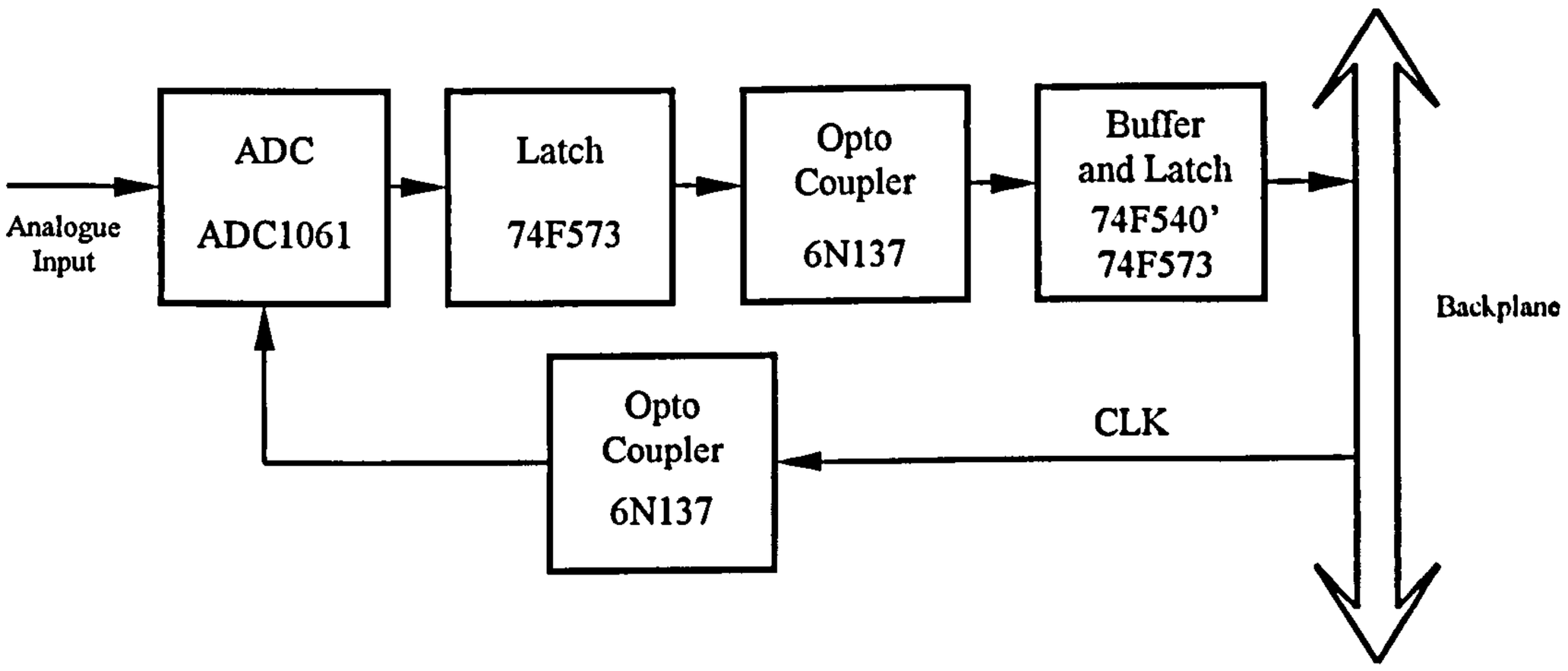


Figure B.2.5: Schematic of the analogue/digital card

B.2.4 Digital/Analogue Board

An overview of the analogue output card is shown in Figure B.2.6. Data is transferred to the digital to analogue converter via the opto-isolation and transfer latch. The bandwidth of this circuit is 500kHz. The analogue output card with the opto-isolation and isolation power supplies will also provide an analogue signal that is isolated from the system backplane and other channels. So this card has the capability of being able to inject analogue signal into a floating system.

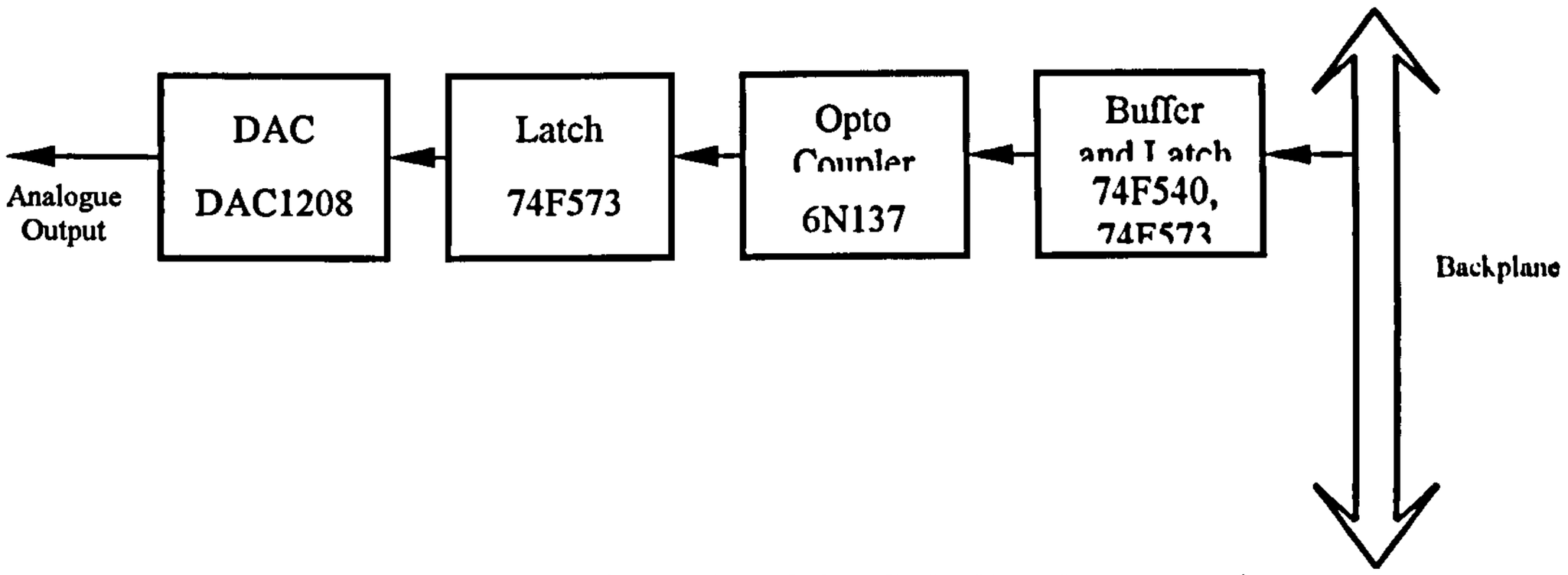


Figure B.2.6: Schematic of the digital/analogue card

B.3 Software

The DSP TMS320C31 operates all the required software tasks needed to control the converter except providing PWM signals that are calculated by the FPGA chip. The needed tasks are divided in two groups. One group is responsible for calculation of all data needed for the FPGA and the other group is responsible for protection and house keeping functions of the controller. The tasks in group one is summarised to:

-monitor front panel of demand frequency and demand voltage
-measure dc-link voltage and midpoint voltage (ACPI)
-measure phase currents
-calculate boost current depending on polarity of phase load current
-calculate voltage demands for PWM board
-calculate boost-time and resonant time for PWM board
-send voltage demands and required boost time and resonant time to PWM board
-send phase current demand to analogue output card

The tasks in group two are summarised to:

-switch off all IGBTs when dc-link voltage (and midpoint at ACPI) is too high
-switch off all IGBTs when dc-link voltage (and midpoint for ACPI) is too low
-switch off all IGBTs when phase current is to high
-switch off all IGBTs when calculated voltage demands, boost times or resonant times overshoots defined threshold
-switch off all IGBTs when time overlaps between resonant mode one and resonant mode two
-send required data to the PC terminal
-system timing including interrupt for ADC conversion and timing to read phase current
-house keeping

The 'C' language is the communication tool between user and DSP. Therefore all tasks was written in 'C' language. The program is structured into six different sections that are now briefly discussed:

Section-1:Header (Defining addresses and constant values)

This header allocates the global vectors to there physical addresses. In addition constant values are defined e.g., the number PI or the angel of 120^0 in radian. The last part of the header includes a look-up table of a sinusoidal waveform. The table stores calculated values in an one dimension array. 400 number presents one sinusoidal cycle.

Section-2: Header (Global values)

This section defines all global parameters and values. It allocates vectors to physical addresses and provides these vectors with comprehensible names. The last section of this header includes the set-up for the communication between the terminal of the PC and the DSP (e.g. baud rate, transmission length).

Section-3: Header (Serial Link)

The serial link allocates the transmitted data from the DSP into characters. Every data from the DSP has to be decoded into a character allowing to read the incoming data for the user. The first part converts data into characters corresponding with the keyboard. The second part describes the conversion of transmitted integer data into readable integer data and the last part defines special characters as bell or space.

Section-4: Header (background routine)

The background routine defines which data are monitored on screen. In addition it defines how to present the data (column, row) and how to label them. Once the program is running this header is responsible how the data appears on screen.

Section-5: Main program

The main programs starts by reading the headers. The next step is the initialisation of all defined global constants. Major global constants are inverter switching frequency, resonant time of each individual pole, maximum expected dc-link voltage (mid-point for ACPI) and maximum expected phase currents. The program sends a start signal to the FPGA to start initialisation of the PWM chip and to read interrupt time, the individual pole resonant times and pre-set times for the first boost mode. The program is than calculating the highest and lowest voltage demand values for the interrupt routine. Further it is eliminating dc-link voltage offset and phase current offsets. Once this routine finished the main program goes into an endless loop.

Section-6: Interrupt routine

The interrupt routine is activated every time when the PWM board sends an interrupt signal to the DSP. The routine is now given in a pseudo code. It is important that the length of the interrupt routine is less than the interrupt time, otherwise wrong data are

calculated. The length of the interrupt routine is measured with an oscilloscope (Figure B.2.2).

```
/* Interrupt Routine */
send start signal to DSP /*signal is needed to watch interrupt length*/
define local variables
start counter for timing ADC conversion for the following interrupt
read demand frequency and demand peak voltage
read all three phase currents
dc-link voltage correction
dc-link voltage to high?
        {
        yes: prepare output data to switch off IGBTs
        no: dc-link voltage to low?
                {
                yes: prepare output data to switch of IGBTs
                }
        }
calculate all three angles θ of the demand frequency /*θ, θ+120°, θ+240°*/
calculate three demand voltages as function from all three angles
repeat for all three phases
{
phase current to high?
        {
        yes: prepare output data to switch of IGBTs
        }
scale voltage demand
voltage demand<voaltage demand minimum?
        {
        yes: voltage demand=voltage demand minimum
        }
voltage demand>voltage demand maximum?
        {
        yes: voltage demand=voltage demand maximum
        }
}
calculate minimum boost time /* boost time is a function of the dc-link voltage */
repeat for all three phases
{
current positive?
        {
        yes: convert current in boost time
        current boost time<minimum boost time?
                {
                yes: current boost time=minimum boost time
                }
        boost time output=(current boost time, minimum boost time)
        }
        {
        no: convert current in boost time
        current boost time<minimum boost time?
                {
                yes: current boost time=minimum boost time
                }
        boost time output=(minimum boost time, current boost time)
        }
}
send demand voltage to analogue output card
send three demand voltage values to PWM card
send three boost time output values to PWM card
clear all flags
send signal: interrupt routine finished
end
```

Figure B.3.1: Interrupt routine

Once the program is written the debugger assembles the program. Before that two small assembler programs are activated. The first program defines the start addresses of the physical memory for the external interrupt flags, the global addresses for reset and interrupt routines and the start addresses of the serial port of transmit interrupt flag and receive interrupt flag. The second program describes how much space is given for each block that is provided from the assembler. A block defines values as stack, space for constant variables, space for the heap or space for global variables and initialisation. When both programs are cleared the interrupt routine program is ready to be assembled. Once the assembling was successful a called mapping program is written. The mapping program associates assembled program parts with the physical memory arrangements of the DSP and the external memory chips. Here for example the programmer may decide to use the DSP memory for the stack, because of the faster access speed and constant values may stored in the external memory. Finally the linker must be activated to achieve the desired memory map. The program is stored in the memory chips of the DSP board or in the internal memory of the DSP and can be monitored with the PC.

Appendix C

THEORETICAL WORK

This Appendix describes the voltage and current waveforms of the ACPI using mathematical tools such as Laplacian transformation and differential calculus (section C.1). In addition it shows the impact of temperature on voltage and current waveforms under various operation modes (section C.2 and section C.3). The results of section C.1 are used in Figure 6.2.8 and Figure 6.2.9. The results of Section C.2 are used in section 6.2.5 and results of section C.3 are used in Figure 6.2.11.

C.1 Mathematical Equations describing the Resonant Mode of the ACPI

This section describes the ACPI topology with the use of mathematical tools during the resonant mode and shows the mathematical deduction of the voltage across the top device. Figure 6.2.8 and 6.2.9 are based on these results which are discussed in this section. From Figure 4.2.10 the topology is drawn again (Figure C.1.1) except the switches have not been considered, because they are not relevant to the maths equations describing the ACPI.

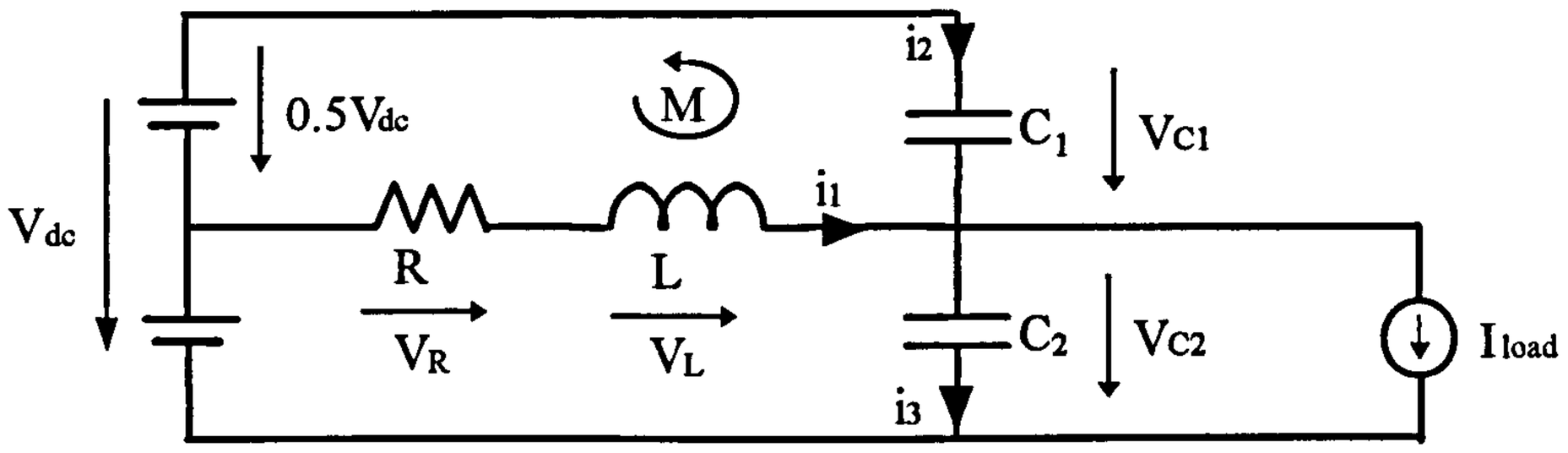


Figure C.1.1: One pole of the ACPI topology (C_1=C_2=C)

The inductance L combines the resonant inductance and stray inductances of the leads and housings of all modules used in this circuit. The capacitor C is the resonant capacitor. Voltage and current sources are assumed to be ideal and the resistor R represents all parasitic resistances in the upper part of the circuit (resistance of inductor, switches, diodes, dc-link capacitor and resonant capacitor).

With the help of Kirchhoff's second law the circuit equation of Figure C.1.1 is (M):

$$\frac{V_{dc}}{2} + V_R + V_L - V_{C1} = 0V \qquad \text{(C.1.1)}$$

The voltage drop V_R and V_L can be expressed as a function of i_1:

$$\frac{V_{dc}}{2} + i_1 R + L\frac{di_1}{dt} - V_{C1} = 0 \qquad \text{(C.1.2)}$$

All values in equation C.1.2 are known except the current i_1 and the unknown value V_{C1}. An equation for i_1 must be found to substitute the current from equation C.1.2. With the help of Kirchhoff's first law the current i_1 can be written as:

$$i_1 + i_2 = i_3 + I_{load} \qquad \text{(C.1.3)}$$

$$\rightarrow i_1 = i_3 - i_2 + I_{load} \qquad \text{(C.1.4)}$$

The currents i_1 and i_2 are a function of capacitance and voltage rising time or voltage falling time. This leads to:

$$\rightarrow i_1 = C\frac{dV_{C2}}{dt} - C\frac{dV_{C1}}{dt} + I_{load} \qquad \text{(C.1.5)}$$

Voltage V_{C2} is calculated as:

$$V_{C2} = V_{dc} - V_{C1} \qquad \text{(C.1.6)}$$

Substituting V_{C2} into equation C.1.5 yields:

$$\Rightarrow i_1 = -C\frac{dV_{C1}}{dt} - C\frac{dV_{C2}}{dt} + I_{load} \qquad \text{(C.1.7)}$$

and finally:

$$\rightarrow i_1 = -2C\frac{dV_{C1}}{dt} + I_{load} \qquad \text{(C.1.8)}$$

Equation C.1.8 expresses current i_1. This equation is now used for equation C.1.2 to substitute current i_1.

$$\Rightarrow \frac{V_{dc}}{2} - 2CR\frac{dV_{C1}}{dt} + RI_{load} - 2LC\frac{dV_{C1}^2}{d^2t} - V_{C1} = 0 \qquad \text{(C.1.9)}$$

This is a second degree differential equation with the parameters: dc-link voltage, resonant inductor, resonant capacitor, parasitic resistor and load current. The parameter load current can have two signs. Either a positive sign, in which case the current flows into the load or a negative sign, in which case the current flows into the pole. Thus, in the following, the two different cases have to be considered. To solve the equation the initial values must be found.

Case 1):

The phase output current flows from the pole into the load. The IGBT carries the load current and the boost current. The 'current ramp-up' mode (see section 4.2.2) has just finished and the resonant mode starts to take place. The voltage across capacitor C_1 is zero. The start conditions are given to

$I_{load}>0A$, $V_{C1}(0)=0V$, $i_1(0)=-I_b$, IGBT->Diode

Case 2)

The phase output current flows from the load to the pole. The IGBT carries the boost current. The 'current ramp-up mode' (see section 4.2.2) has just finished and the resonant mode starts to take place. The voltage across capacitor C_1 is zero. This can be summarised to

$I_{load}<0A$, $V_{C1}(0)=0V$, $i_1(0)=I_b+I_{load}$, Diode->IGBT

Case 1) is discussed at first followed by case 2).

Case 1)

Equation C.1.9 needs the initial values of V_{C1} and dV_{C1}/dt. Both can be expressed as:

$$V_{C1}(0)=0V \tag{C.1.10}$$

$$V_{C1}'(0)=\frac{dV_{C1}(0)}{dt}=\frac{i_1(0)-I_{load}}{-2C}=\frac{-I_b-I_{load}}{-2C}=\frac{I_b+I_{load}}{2C} \tag{C.1.11}$$

Using both of the above equations, equation C.1.9 can be written as:

$$\Rightarrow \frac{V_{dc}}{2}-2RC\frac{dV_{C1}}{dt}+RI_{load}-2LC\frac{dV_{C1}^2}{d^2t}-V_{C1}=0 \tag{C.1.12}$$

Laplacian transformation takes place and equation C.1.12 changes to:

$$0\longrightarrow\bullet \quad \frac{V_{dc}}{2s}-2RC\{sV_{C1}\}+\frac{RI_{load}}{s}-2LC\{s^2V_{C1}-V_{C1}'(0)\}-V_{C1}=0 \tag{C.1.13}$$

The following four equations calculates the voltage V_{C1}:

$$\rightarrow \frac{\frac{V_{dc}}{2}+RI_{load}}{s}-2RCV_{C1}s-2LCV_{C1}s^2+2LC\frac{I_b+I_{load}}{2C}-V_{C1}=0 \tag{C.1.14}$$

$$\rightarrow \frac{\frac{V_{dc}}{2}+RI_{load}}{s}+2LC\frac{I_b+I_{load}}{2C}=2RCV_{C1}s+2LCV_{C1}s^2+V_{C1} \tag{C.1.15}$$

$$\rightarrow V_{C1}=\frac{\frac{V_{dc}}{2}+RI_{load}}{s(2LCs^2+2RCs+1)}+2LC\frac{\frac{I_b+I_{load}}{2C}}{2LCs^2+2RCs+1} \tag{C.1.16}$$

$$\rightarrow V_{C1}=\frac{\frac{V_{dc}}{2}+RI_{load}}{s(2s^2+\frac{R}{L}s+\frac{1}{2LC})2LC}+\frac{\frac{I_b+I_{load}}{2C}}{s^2+\frac{R}{L}s+\frac{1}{2LC}} \tag{C.1.17}$$

With the help of the definition from the resonant angular frequency:

$$\omega_R^2=\frac{1}{2LC} \tag{C.1.18}$$

and the damping coefficient:

$$2\zeta\omega_R=\frac{R}{L} \tag{C.1.19}$$

$$\rightarrow \zeta = \frac{R}{2\omega_R L} \tag{C.1.20}$$

equation C.1.17. simplifies. The damping factor ζ can be expressed without the resonant angular frequency ω_R:

$$\Rightarrow \zeta = \frac{R}{2L}\sqrt{2LC} = R\sqrt{\frac{C}{2L}} < 1 \tag{C.1.21}$$

From that follows the relation:

$$\rightarrow R < \sqrt{\frac{2L}{C}} \tag{C.1.22}$$

For the designed ACPI converter the relation is true, because using the values L=5,7µH and C=60nF (stray inductances are neglectable) the parasitic resistor must be as small as:

$$R < \sqrt{\frac{2*5{,}7\mu H}{60nF}} = 13.78\Omega \tag{C.1.23}$$

The parasitic resistance of the converter is much lower than the value given in equation C.1.23 (approx. 500mΩ).

Substituting the expressions of resonant angular frequency and damping coefficient in equation C.1.17, the voltage V_{C1} is represented as:

$$\Rightarrow V_{C1} = \frac{\frac{V_{dc}}{2} + RI_{load}}{s(s^2 + 2\zeta\omega_R s + \omega_R^2)} * \omega_R^2 + \frac{I_b + I_{load}}{s^2 + 2\zeta\omega_R s + \omega_R^2} * \frac{1}{2C} \tag{C.1.24}$$

The second term of equation C.1.24 gets expand with $\omega_R{}^2$:

$$\rightarrow V_{C1} = \frac{\frac{V_{dc}}{2} + RI_{load}}{s(s^2 + 2\zeta\omega_R s + \omega_R^2)} * \omega_R^2 + \frac{(I_b + I_{load})\omega_R^2}{s^2 + 2\zeta\omega_R s + \omega_R^2} * \frac{1}{2C} * \frac{1}{\omega_R^2} \tag{C.1.25}$$

Now the inverse Laplacian transformation is used resulting in the final expression for the voltage V_{C1}: ●——0

$$\Rightarrow v_{C1}(t) = \left[\frac{V_{dc}}{2} + RI_{load}\right] * \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_R t} \sin\left(\omega_R\sqrt{1-\zeta^2}\,t + \Phi\right)\right] + \frac{I_b + I_{load}}{2C\omega_R} * \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_R t} * \sin\left(\omega_R\sqrt{1-\zeta^2}\,t\right) \tag{C.1.26}$$

where,

$$\Phi = \arccos\zeta \tag{C.1.27}$$

and

$$\zeta < 1 \tag{C.1.28}$$

as already discussed in equation C.1.21.

Case 2)

Equation C.1.9 needs the initial values of V_{C1} and dV_{C1}/dt. Both can be expressed as:

$$V_{C1}(0)=0V \tag{C.1.29}$$

$$V'_{C1}(0)=\frac{dV_{C1}(0)}{dt}=\frac{i_1(0)-I_{load}}{-2C}=\frac{+I_b+I_{load}-I_{load}}{-2C}=\frac{I_b}{2C} \tag{C.1.30}$$

Using both of the above equations, equation C.1.9 can be written as:

$$\Rightarrow\frac{V_{dc}}{2}-2RC\frac{dV_{C1}}{dt}+RI_{load}-2LC\frac{dV_{C1}^2}{d^2t}-V_{C1}=0 \tag{C.1.31}$$

Laplacian transformation takes place and equation C.1.31 changes to:

$$0\longrightarrow\bullet\ \frac{V_{dc}}{2s}-2RC\{sV_{C1}\}+\frac{RI_{load}}{s}-2LC\{s^2V_{C1}-V'_{C1}(0)\}-V_{C1}=0 \tag{C.1.32}$$

The following four equations calculates the voltage V_{C1}:

$$\rightarrow\frac{\frac{V_{dc}}{2}+RI_{load}}{s}-2RCV_{C1}s-2LCV_{C1}s^2+2LC\frac{I_b}{2C}-V_{C1}=0 \tag{C.1.33}$$

$$\rightarrow\frac{\frac{V_{dc}}{2}+RI_{load}}{s}+2LC\frac{I_b}{2C}=2RCV_{C1}s+2LCV_{C1}s^2+V_{C1} \tag{C.1.34}$$

$$\rightarrow V_{C1}=\frac{\frac{V_{dc}}{2}+RI_{load}}{s(2LCs^2+2RCs+1)}+2LC\frac{\frac{I_b}{2C}}{2LCs^2+2RCs+1} \tag{C.1.35}$$

$$\rightarrow V_{C1}=\frac{\frac{V_{dc}}{2}+RI_{load}}{s(2s^2+\frac{R}{L}s+\frac{1}{2LC})2LC}+\frac{\frac{I_b}{2C}}{s^2+\frac{R}{L}s+\frac{1}{2LC}} \tag{C.1.36}$$

With the help of the definition from the resonant angular frequency:

$$\omega_R^2=\frac{1}{2LC} \tag{C.1.37}$$

and the damping coefficient:

$$2\zeta\omega_R=\frac{R}{L} \tag{C.1.38}$$

$$\rightarrow\zeta=\frac{R}{2\omega_R L} \tag{C.1.39}$$

equation C.1.36. simplifies. The damping factor ζ can be expressed without the resonant angular frequency ω_R:

$$\Rightarrow\zeta=\frac{R}{2L}\sqrt{2LC}=R\sqrt{\frac{C}{2L}}<1 \tag{C.1.40}$$

From that follows the relation:

$$\rightarrow R<\sqrt{\frac{2L}{C}} \tag{C.1.41}$$

For the designed ACPI converter the relation is true, because using the values L=5,7µH and C=60nF (stray inductances are neglectable) the parasitic resistor must be as small as:

$$R < \sqrt{\frac{2*5,7\mu H}{60nF}} = 13.78\Omega \qquad \text{(C.1.42)}$$

The parasitic resistance of the converter is much lower than the value given in equation C.1.23 (approx. 500mΩ).

Substituting the expressions of resonant angular frequency and damping coefficient in equation C.1.36, the voltage V_{C1} is represented as:

$$\Rightarrow V_{C1} = \frac{\frac{V_{dc}}{2} + RI_{load}}{s(s^2 + 2\zeta\omega_R s + \omega_R^2)} * \omega_R^2 + \frac{I_b}{s^2 + 2\zeta\omega_R s + \omega_R^2} * \frac{1}{2C} \qquad \text{(C.1.43)}$$

The second term of equation C.1.43 gets expand with ω_R^2:

$$\rightarrow V_{C1} = \frac{\frac{V_{dc}}{2} + RI_{load}}{s(s^2 + 2\zeta\omega_R s + \omega_R^2)} * \omega_R^2 + \frac{I_b\omega_R^2}{s^2 + 2\zeta\omega_R s + \omega_R^2} * \frac{1}{2C} * \frac{1}{\omega_R^2} \qquad \text{(C.1.44)}$$

Now the inverse Laplacian transformation is used resulting in the final expression for the voltage V_{C1}: ●——0

$$\Rightarrow v_{C1}(t) = \left[\frac{V_{dc}}{2} + RI_{load}\right] * \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_R t} \sin\left(\omega_R\sqrt{1-\zeta^2}\,t + \Phi\right)\right] + \frac{I_b}{2C\omega_R} * \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_R t} * \sin\left(\omega_R\sqrt{1-\zeta^2}\,t\right)$$

(C.1.45)

where,

$$\Phi = \arccos\zeta \qquad \text{(C.1.46)}$$

and

$$\zeta < 1 \qquad \text{(C.1.47)}$$

as already discussed using equation C.1.40.

As already mentioned in this section the parasitic resistance R is very low. R is a value of the design of the converter and the resistance of the ACPI was calculated to approx. 500mΩ. Thus the assumption is made that the resistance R is neglectable for the following calculations. In case R->0Ω the damping coefficient yields:

$$\zeta \approx 0 \qquad \text{(C.1.48)}$$

With equation C.1.48 the following three approximations can be made:

$$\Rightarrow 1 - \zeta^2 \approx 1 \qquad \text{(C.1.49)}$$

$$\Rightarrow \arccos\zeta \approx \arccos 0 = \frac{\pi}{2} \qquad \text{(C.1.50)}$$

$$\Rightarrow e^{-\zeta\omega_R t} = e^{-\frac{R}{2L}t} \approx 1 - \frac{\frac{R}{2L}}{1!} + \frac{\left(-\frac{R}{2L}\right)^2}{2!} + \frac{\left(-\frac{R}{2L}\right)^3}{3!} + \ldots \approx 1 \qquad \text{(C.1.51)}$$

Equation C.1.51 is based on the Taylor series expansion of Euler's formula.

With these three approximations the voltage term V_{C1} simplifies to:

Case 1)

$$\Rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \sin\left(\omega_R t + \frac{\pi}{2}\right)\right] + \frac{I_b + I_{load}}{2C\omega_R} * \sin\omega_R t \qquad \text{(C.1.52)}$$

Applying trigonometric rules leads to:

$$\rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \cos\omega_R t\right] + \frac{I_b + I_{load}}{2C\omega_R} * \sin\omega_R t \qquad \text{(C.1.53)}$$

Case 2)

$$\Rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \sin\left(\omega_R t + \frac{\pi}{2}\right)\right] + \frac{I_b}{2C\omega_R} * \sin\omega_R t \qquad \text{(C.1.54)}$$

Applying trigonometric rules leads to:

$$\rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \cos\omega_R t\right] + \frac{I_b}{2C\omega_R} * \sin\omega_R t \qquad \text{(C.1.55)}$$

Introducing the resonant impedance:

$$Z_R = \sqrt{\frac{L}{2C}} \qquad \text{(C.1.56)}$$

leads to the final results:

Case 1)

$$\Rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \cos\omega_R t\right] + \left(I_b + I_{load}\right) Z_R \sin\omega_R t \qquad \text{(C.1.57)}$$

Case 2)

$$\Rightarrow v_{C1}(t) = \frac{V_{dc}}{2} * \left[1 - \cos\omega_R t\right] + I_b Z_R \sin\omega_R t \neq f\left(I_{load}\right) \qquad \text{(C.1.58)}$$

Voltage V_{C1} of equation C.1.58 is not a function of the load current, where as the voltage of equation C.1.57 is load dependent. Both equation are equal to equations 6.2.7 and 6.2.8. Because of the similarity of both equations one can write:

$$\Rightarrow v_{C1}(t)\Big|_{IGBT->Diode} = v_{C1}(t)\Big|_{Diode->IGBT} + I_{load} Z_R \sin\omega_R t \qquad \text{(C.1.59)}$$

C.2 Impact of Temperature Drift during Resonant Mode

In section 6.2.6 the statement was given that during resonant mode the resonant time is only minutely influenced by temperature drift. Section C.2 proofs this statement.

The relative error of the on-state time during the resonant mode is given in equation C.2.1:

$$\text{rel.error} = \frac{\pi\sqrt{2LC} - \pi\sqrt{2L(T)C(T)}}{\pi\sqrt{2LC}} \tag{C.2.1}$$

The inductor in form of a core is a linear function of the permeability μ as shown in equation C.2.2:

$$L = \frac{\mu N^2 h}{2\pi} * \ln\frac{r_o}{r_i} \tag{C.2.2}$$

(N=number of turns, h=higth of core material, r_o=radius to the outer edge of the core, r_i=radius to the inner edge of the core)

Thus the relative error can be expressed as:

$$\text{rel.error} = \frac{\sqrt{\mu C} - \sqrt{\mu(T)C(T)}}{\sqrt{\mu C}} \tag{C.2.3}$$

The temperature dependency of the permeability and the temperature dependency of the resonant capacitors are given by the manufacturer. One 10nF polypropylene doubled metallized foil capacitor has a temperature coefficient (TK) of TK_C=-200ppm/^{0}C. Using 20nF capacitance for each resonant capacitor two 10nF capacitors have been paralleled. Thus during the resonant mode four capacitors are involved. Two 10nF capacitors in parallel at the top switch and two 10nF capacitors in parallel at the bottom switch. The total TK of that configuration have to be considered. In a series circuit the TK is given as:

$$TK_{series} = \frac{TK_1Z_1 + TK_2Z_2}{Z_1 + Z_2} \tag{C.2.4}$$

The TK in a parallel circuit is given as:

$$TK_{parallel} = \frac{TK_2Z_1 + TK_1Z_2}{Z_1 + Z_2} \tag{C.2.5}$$

The impedance Z of the capacitor C can be written as:

$$Z_C = \frac{1}{j\omega C} \tag{C.2.6}$$

In the ACPI converter it is Z_1=Z_2=Z_c and TK_1=TK_2=TK_c. Thus equations C.2.4 and C.2.5 simplifies to:

$$TK_{series} = TK_C \tag{C.2.7}$$

$$TK_{parallel} = TK_C \tag{C.2.8}$$

From equations C.2.7 and C.2.8 yields the total TK of the capacitor arrangement:

$$TK_{total} = TK_c \tag{C.2.9}$$

The temperature coefficient of the inductor TK_L is given to +95ppm/^{0}C. The temperature coefficient of percent permeability versus both DC magnetising force and peak AC flux densities ranges from -100 to -400ppm/^{0}C. The combination results in lower inductance of high temperature even under biased conditions (for reference please refer to section 6.2.6). The TK_C and TK_L values have been inserted into equation C.2.3:

$$\text{rel.error} = \frac{\sqrt{\mu C} - \sqrt{\mu\left[1+95\frac{\text{ppm}}{^0\text{C}}\Delta T - 400\frac{\text{ppm}}{^0\text{C}}\Delta T\right]C\left[1-200\frac{\text{ppm}}{^0\text{C}}\Delta T\right]}}{\sqrt{\mu C}} \qquad \text{(C.2.10)}$$

Equation C.2.10 can be simplified to:

$$\text{rel.error} = 1 - \sqrt{\left(1+95\frac{\text{ppm}}{^0\text{C}}\Delta T - 400\frac{\text{ppm}}{^0\text{C}}\Delta T\right)\left(1-200\frac{\text{ppm}}{^0\text{C}}\Delta T\right)} = \frac{T-T'}{T} \qquad \text{(C.2.11)}$$

Equation C.2.11 shows that the relative error is substitute by equation C.2.1. The resonant time T is given as:

$$T = \pi\sqrt{2LC} = 1.5\mu s \qquad \text{(C.2.12)}$$

This value is valid at the ambient temperature of 25^{0}C. Equation C.2.11 can be rewritten as:

$$T' = -\text{rel.error} * T + T = T(1 - \text{rel.error}) \qquad \text{(C.2.13)}$$

and finally:

$$T' = 1.5\mu s\sqrt{\left(1+95\frac{\text{ppm}}{^0\text{C}}\Delta T - 400\frac{\text{ppm}}{^0\text{C}}\Delta T\right)\left(1-200\frac{\text{ppm}}{^0\text{C}}\Delta T\right)} \qquad \text{(C.2.14)}$$

Figure C.2.1 shows the resonant time vs. temperature rise. The error is less than 40ns over 100 degree temperature rise.

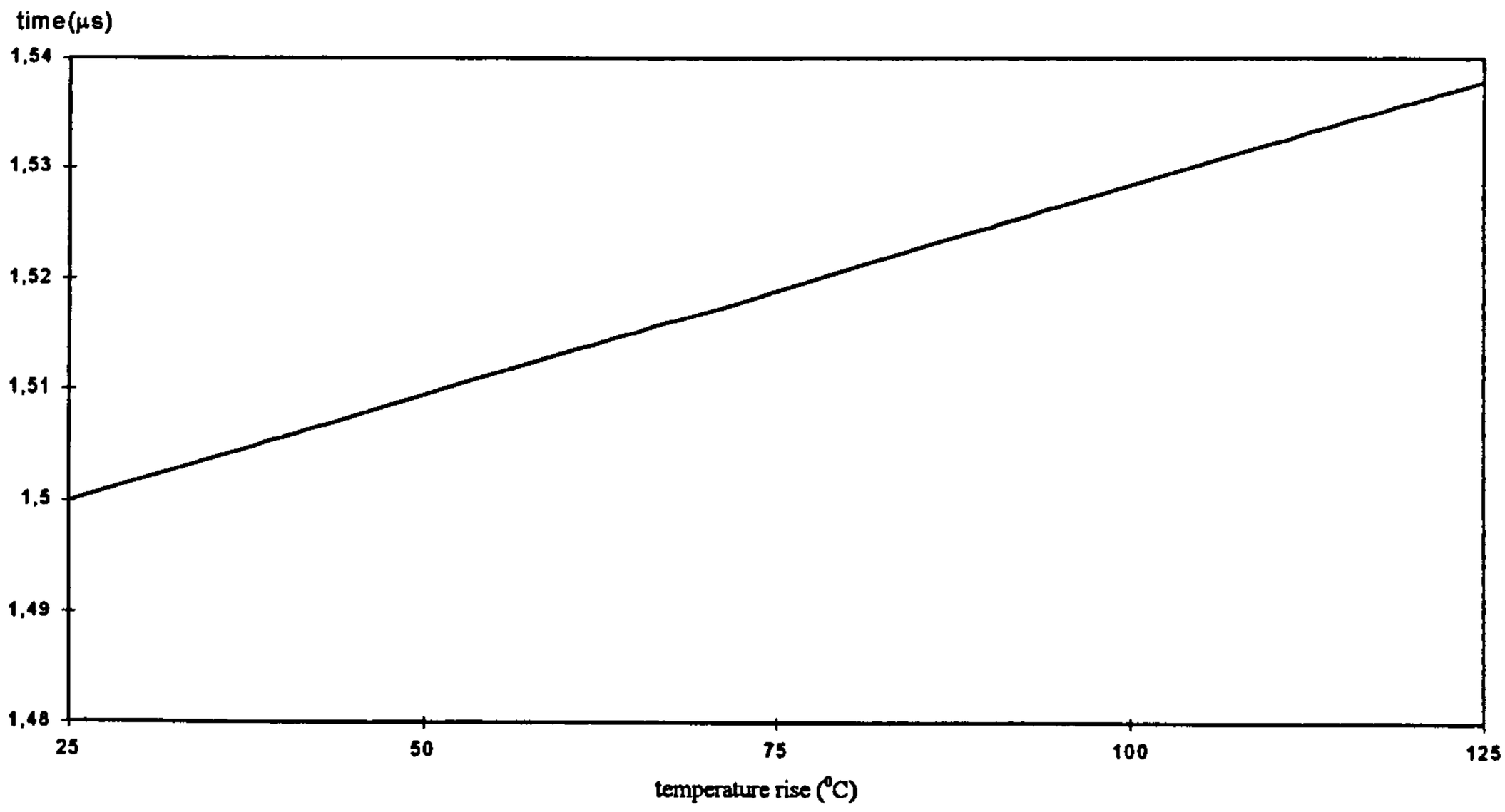


Figure C.2.1: Resonant time vs. temperature rise

C.3 Impact of Temperature Drift during Boost Mode and Ramp Mode

Figure 6.2.11 shows the on-state time vs. temperature rise at different modes (ramp-up mode and boost mode). Section C.3 describes the maths that leads to the plot of Figure 6.2.11. To start with the relative error of the ramp-up time is introduced:

$$\text{rel.error} = \frac{\Delta t - \Delta t(\Delta T)}{\Delta t} \tag{C.3.1}$$

Putting the known equations of an inductor with core shape (C.3.2 and C.3.3) into equation C.3.1:

$$u = L\frac{di}{dt} = L\frac{\Delta I}{\Delta t} \tag{C.3.2}$$

$$L = \frac{\mu N^2 h}{2\pi} * \ln\frac{r_o}{r_i} \tag{C.3.3}$$

(N=number of turns, h=higth of core material, r_o=radius of the outer edge of the core, r_i=radius of the inner edge of the core)

yields:

$$\text{rel.error} = \frac{L - L(\Delta T)}{L} = \frac{\mu - \mu(\Delta T)}{\mu} \tag{C.3.4}$$

Equation C.3.4 shows that the relative error is only a function of the permeability. The value of the permeability is given from the manufacturer (for reference refer to section 6.2.6 and section C.2). From that the relative error can be written as:

$$\text{rel.error} = \frac{\mu - \mu\left(1 + 95\frac{ppm}{^0C}\Delta T - 400\frac{ppm}{^0C}\Delta T\right)}{\mu} \tag{C.3.5}$$

and finally:

$$\text{rel.error} = 1 - \left[1 + 95\frac{ppm}{^0C}\Delta T - 400\frac{ppm}{^0C}\Delta T\right] \tag{C.3.6}$$

Equation C.3.1 includes the time $\Delta t(\Delta T)$ as a function of temperature. From that it is given:

$$\Delta t(\Delta T) = -\Delta t * \text{rel.error} + \Delta t = \Delta t(1 - \text{rel.error}) \tag{C.3.7}$$

where during ramp-up mode the time Δt at 25^0C is written as:

$$\Delta t = \frac{L}{v}\Delta i = \frac{5.7\mu H}{280V} * 55A = 1{,}1196\mu s \tag{C.3.8}$$

Substituting equation C.3.6 and equation C.3.8 into equation C.3.7 yields:

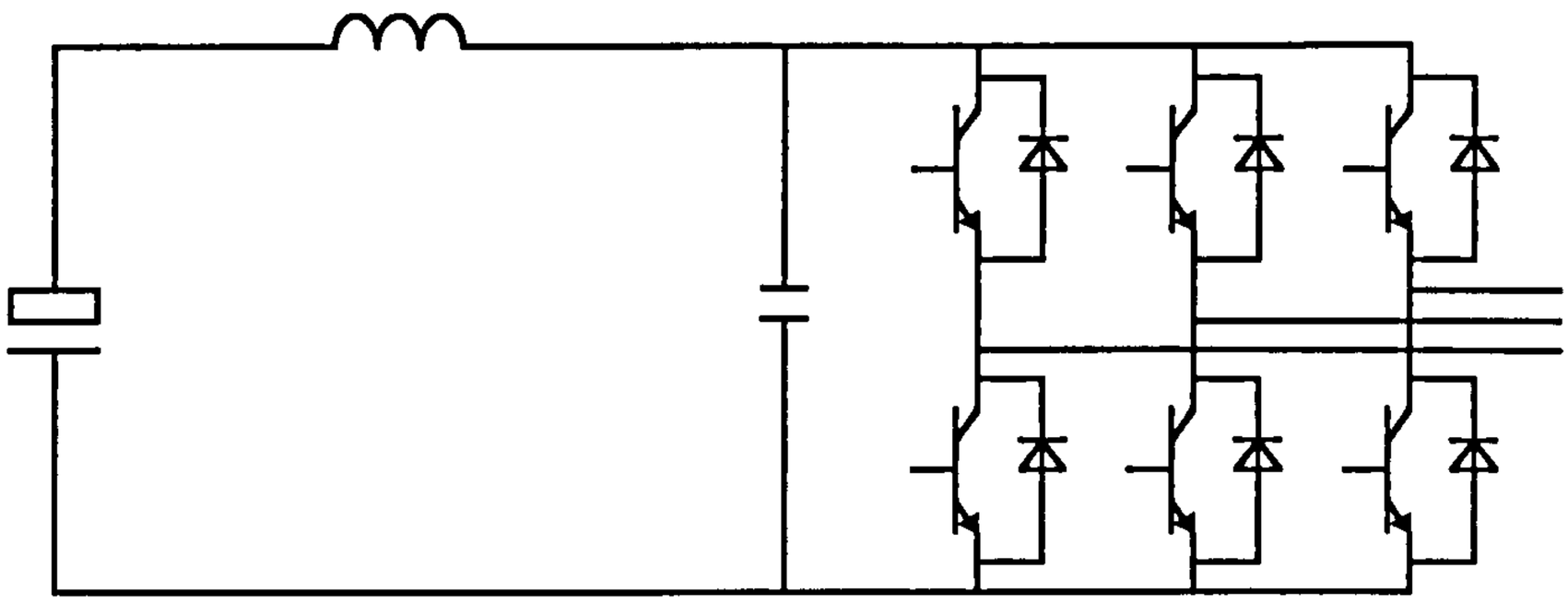
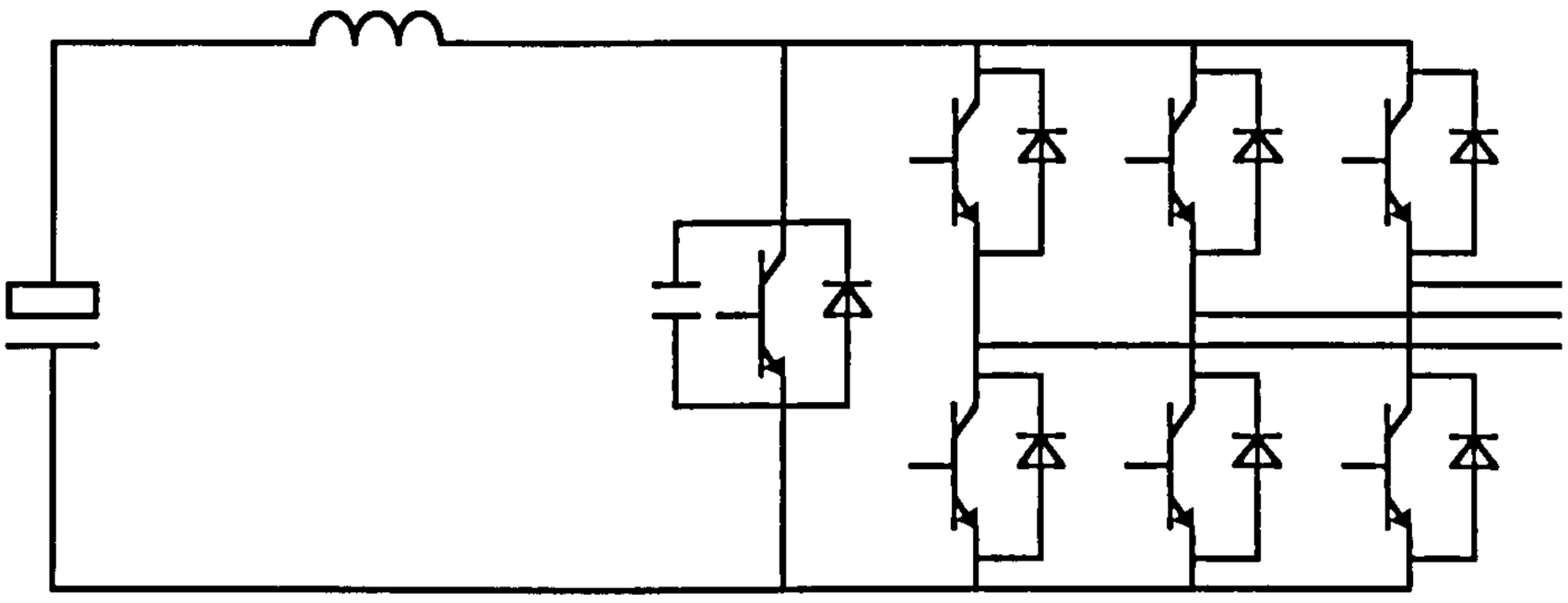
$$\Delta t(\Delta T) = \Delta t\left(1 - 95\frac{ppm}{^0C}\Delta T + 400\frac{ppm}{^0C}\Delta T\right) \tag{C.3.9}$$

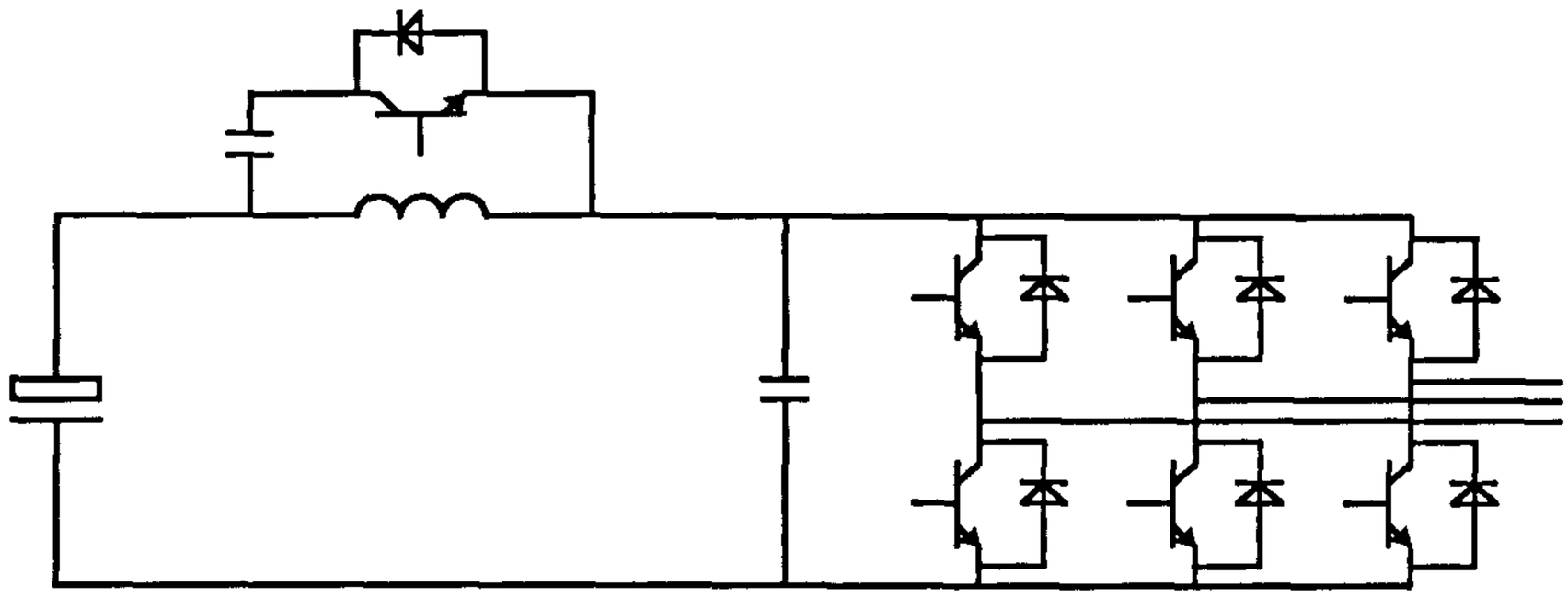
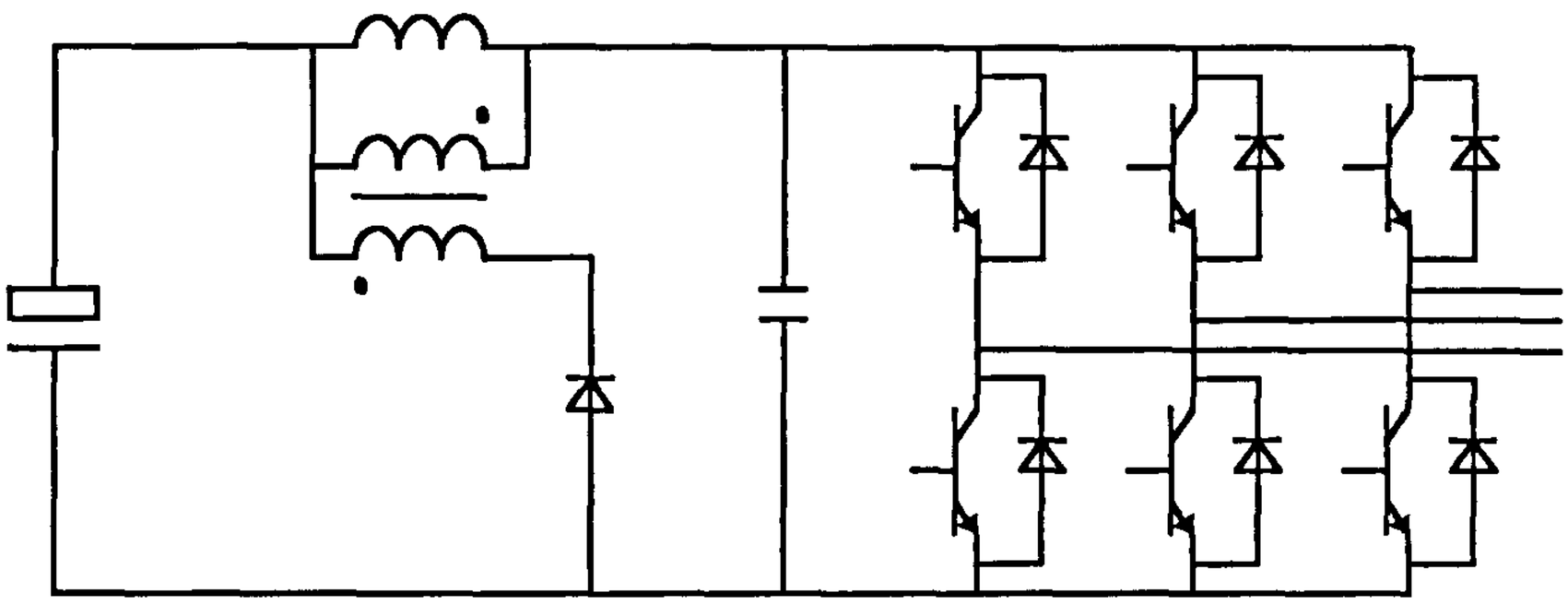
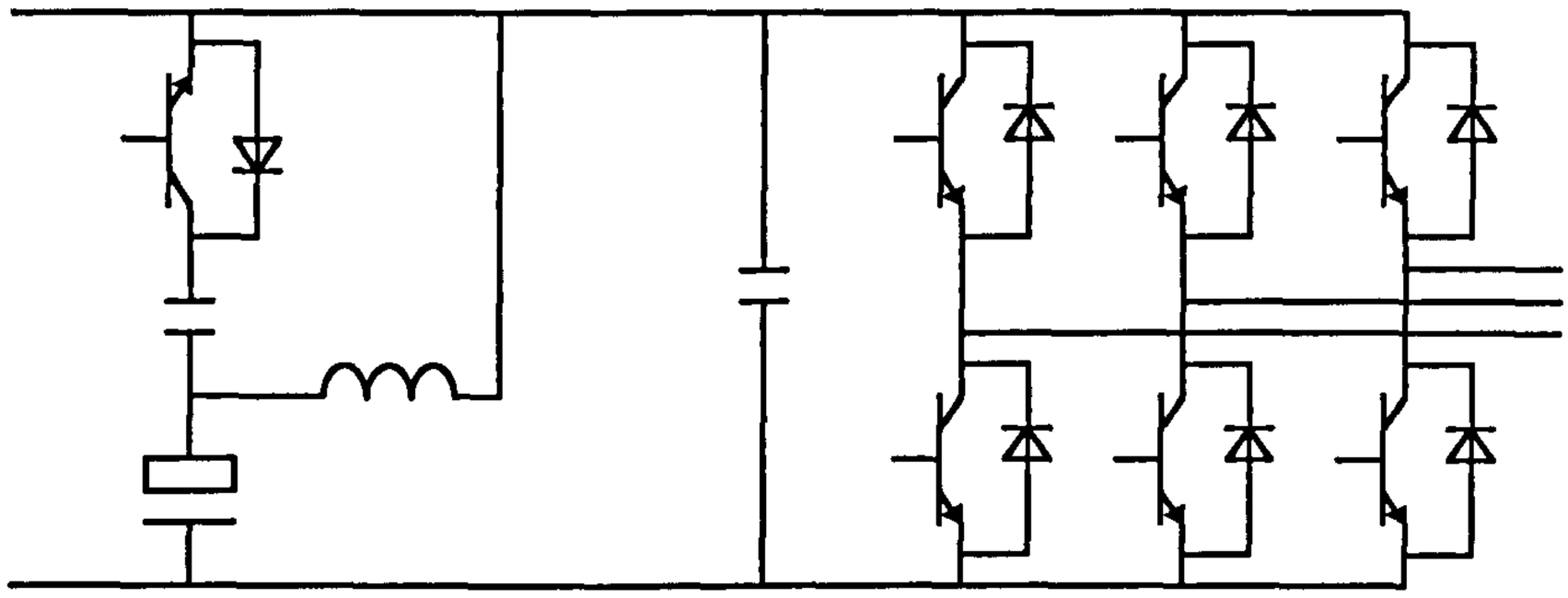
This equation has been used for Figure 6.2.11. Please note, that Δt at boost mode (0.3054µs) is different to Δt at ramp-up mode (1.1196µs).

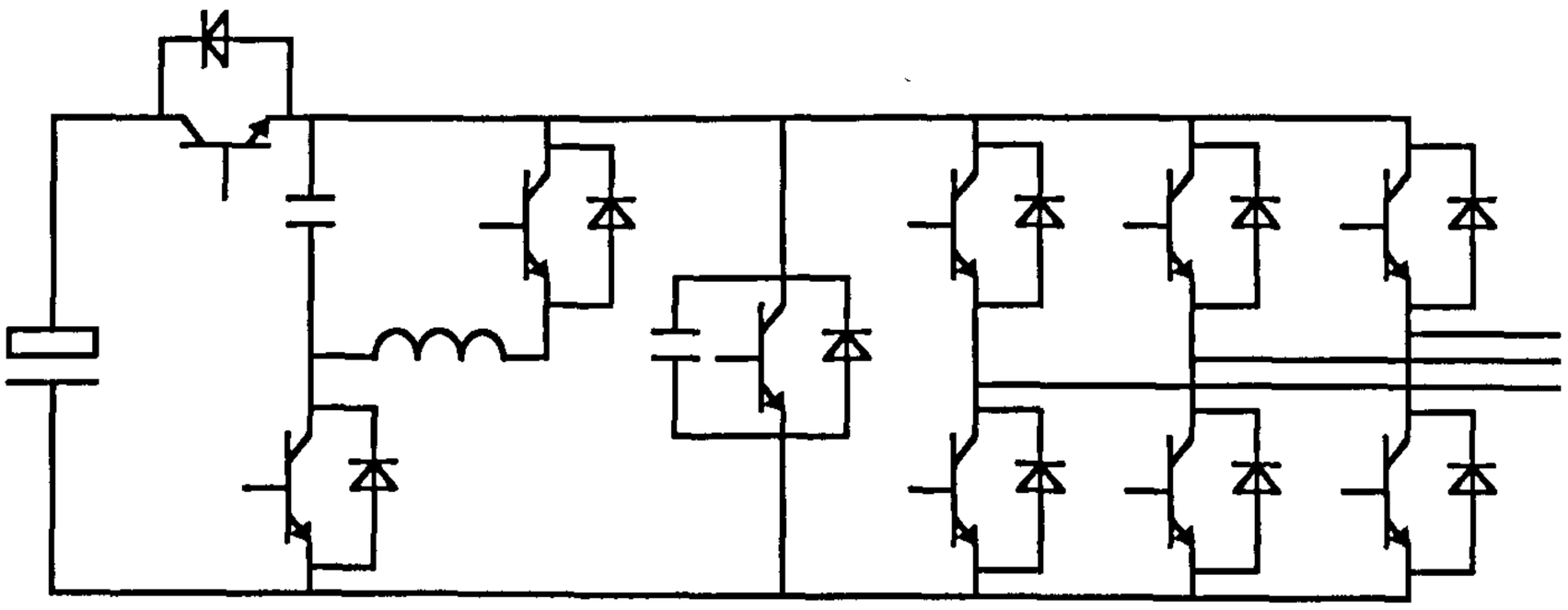
Appendix D

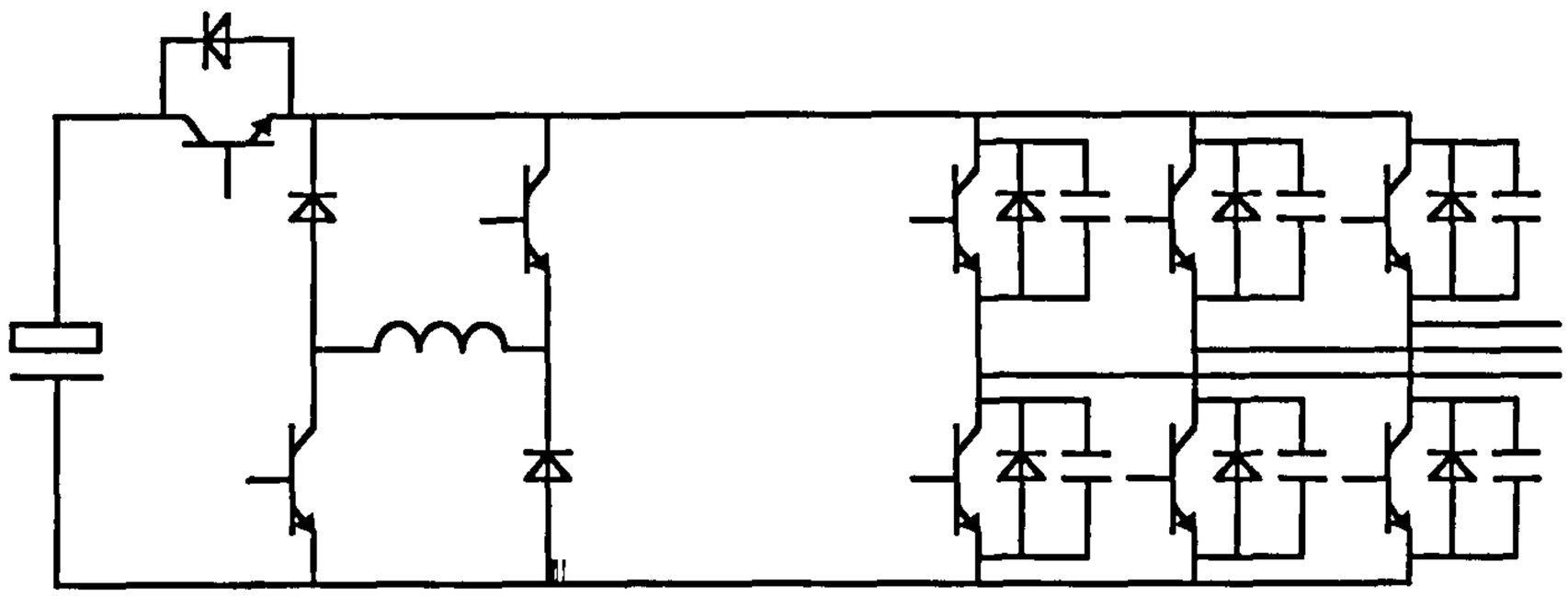
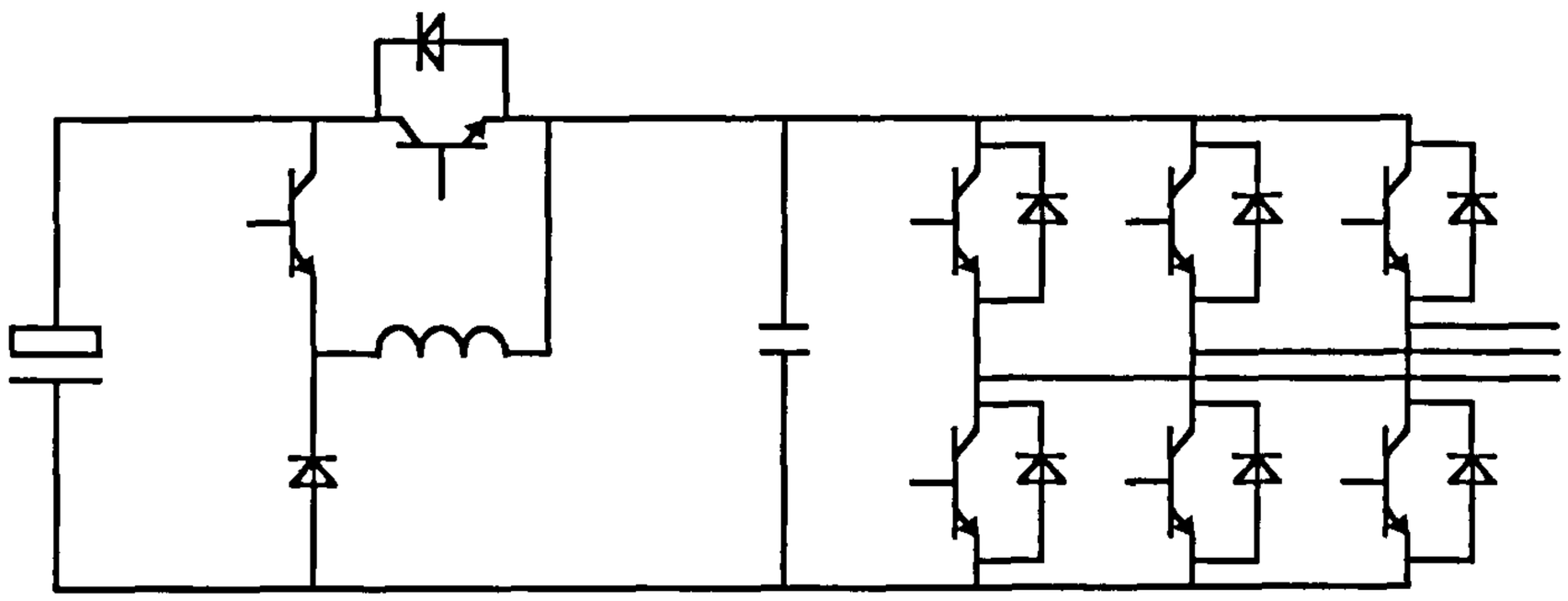
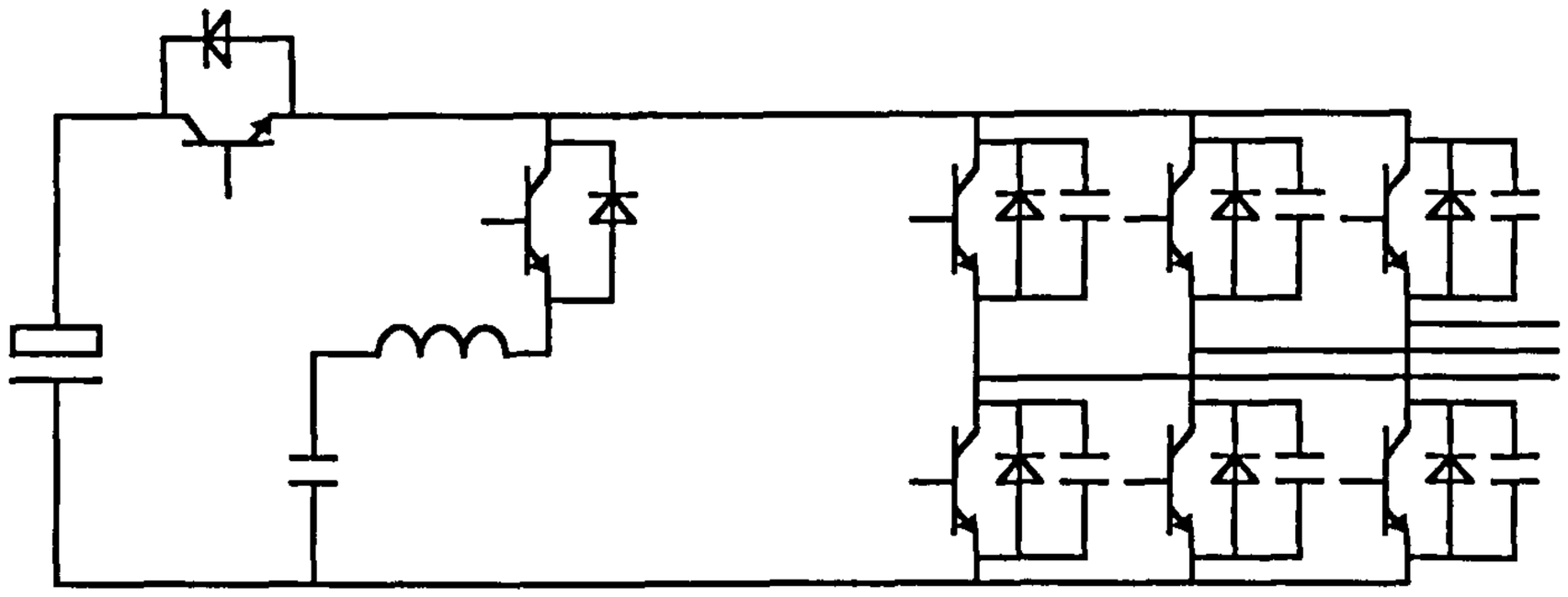
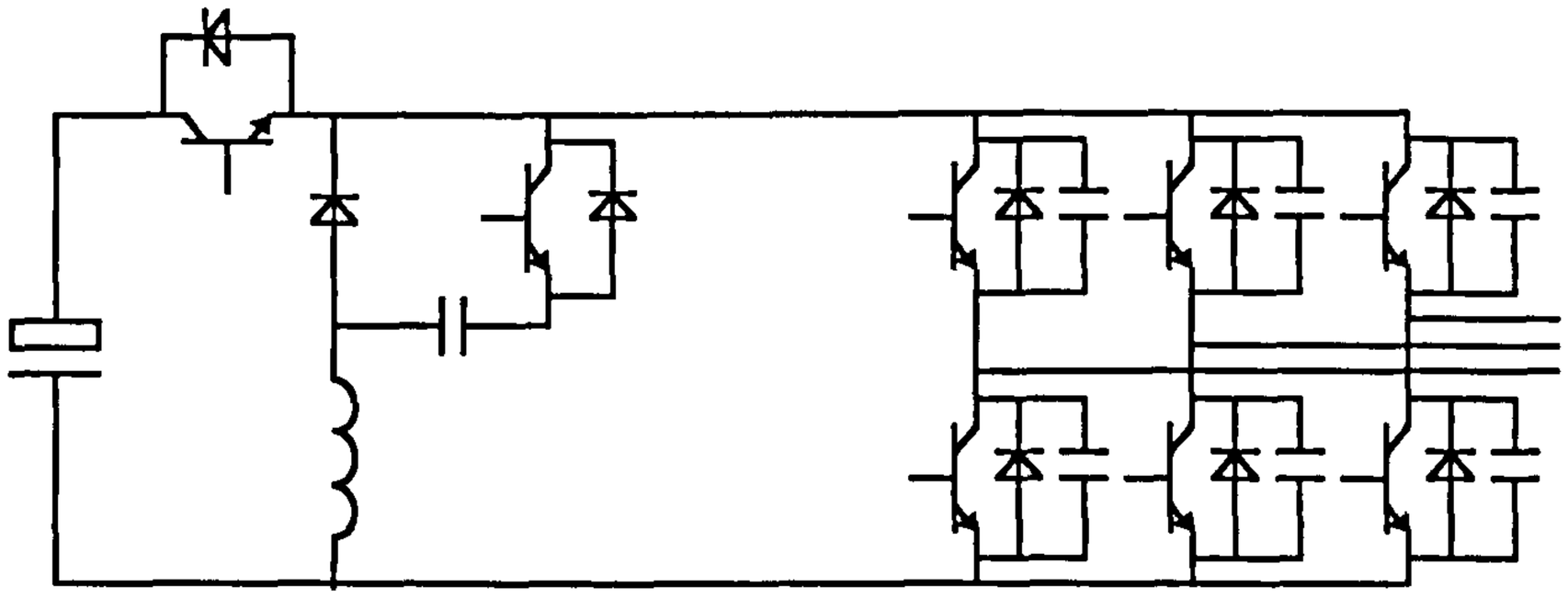
OVERVIEW OF SCHEMATICS OF SOFTSWITCHING TOPOLOGIES

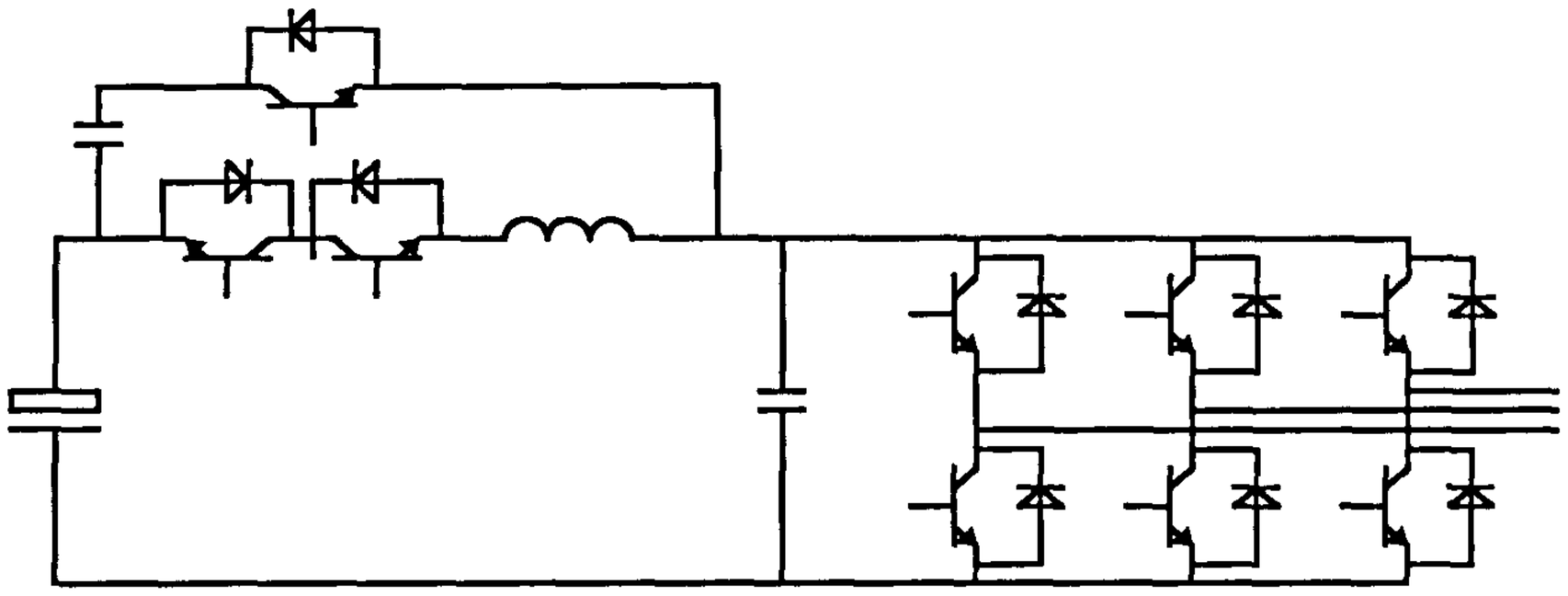
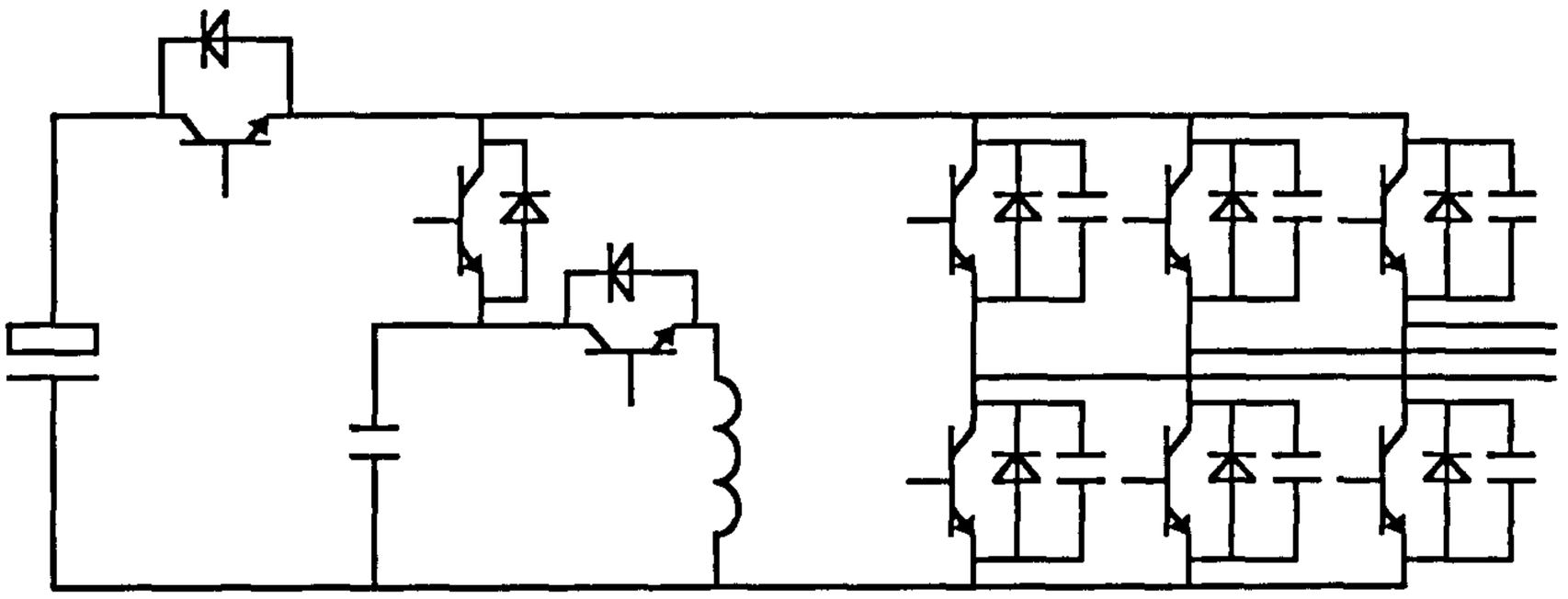
Appendix D includes one table (Table D.1). The table relates all discussed softswitching topologies with references that describe the operation mode of the topology. Some references are underlined to indicate that they are the same as the reference cited directly before them.

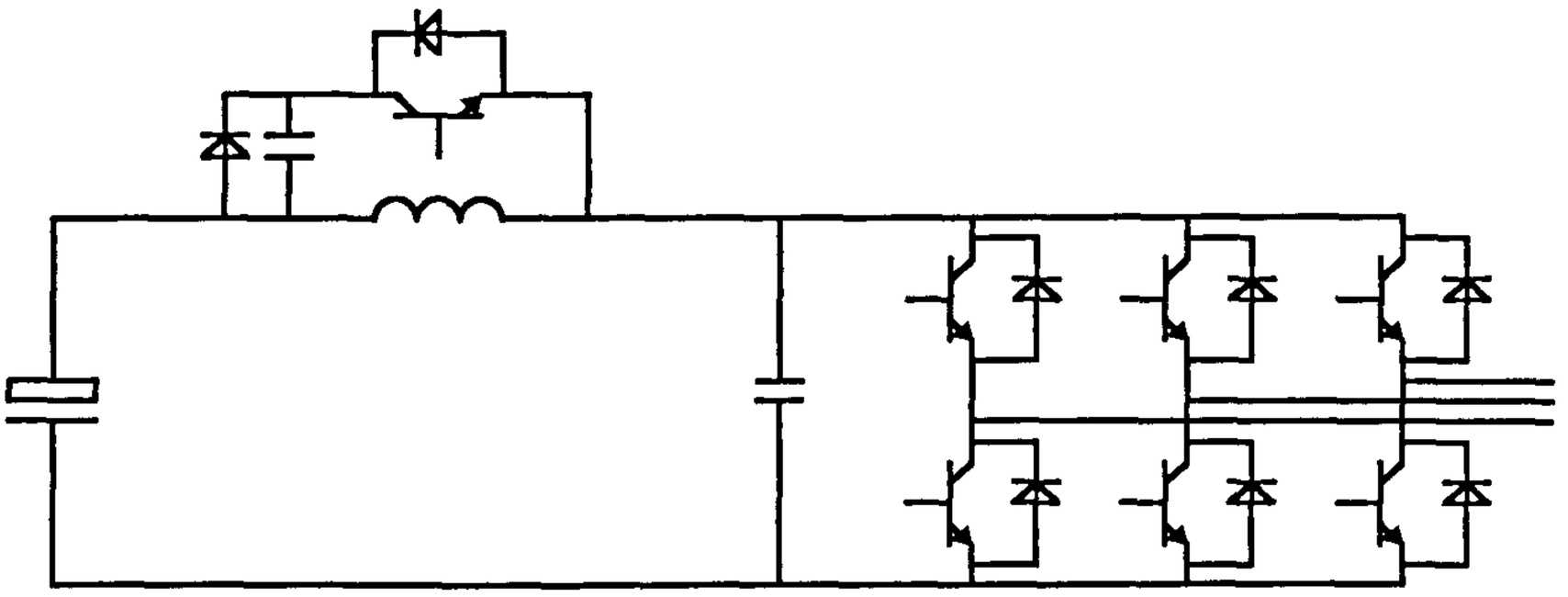
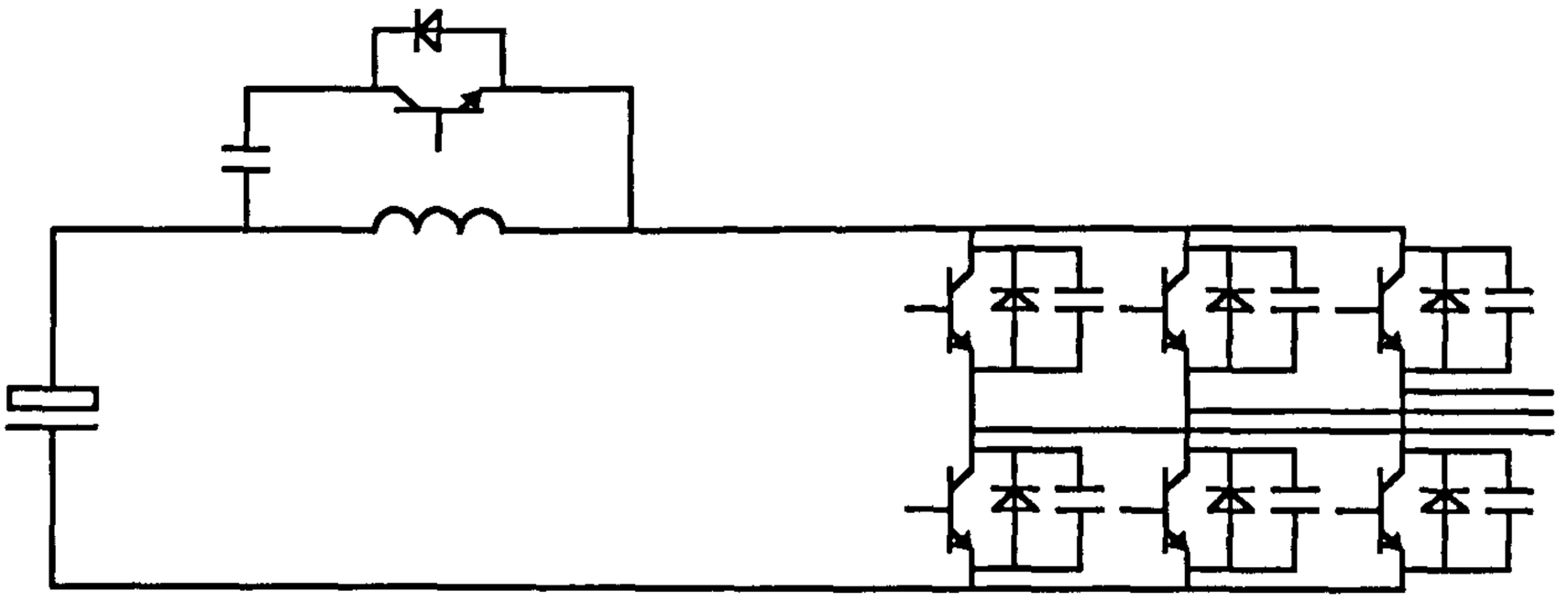
	TOPOLOGY
Reference	*basic RDCL*
[2.28], [3.1], [5.1]	
[3.2], [5.2]	

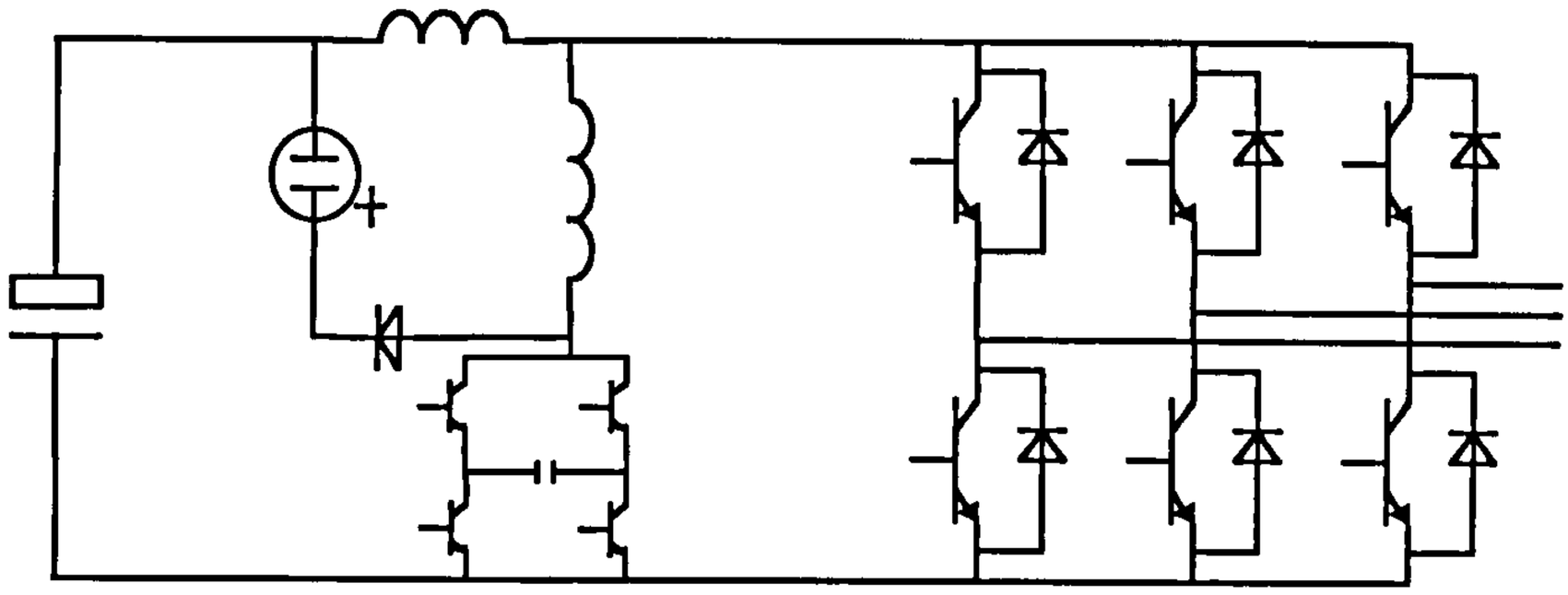
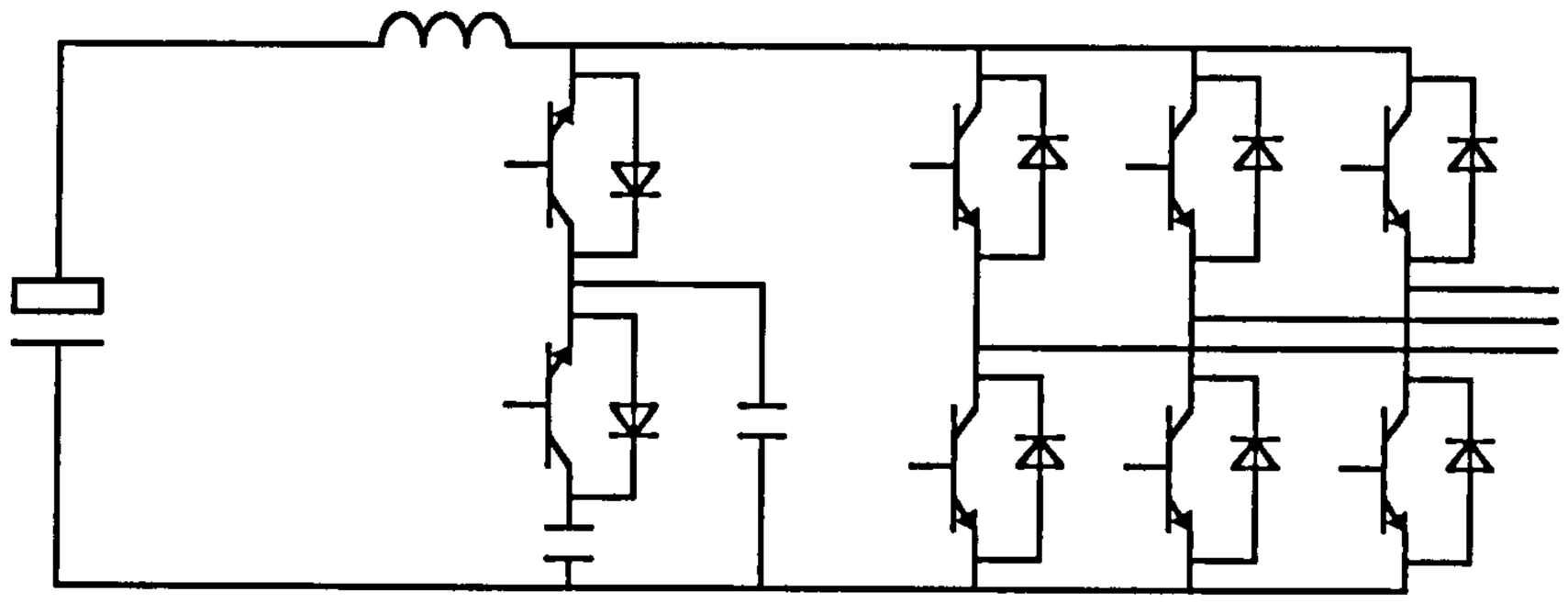
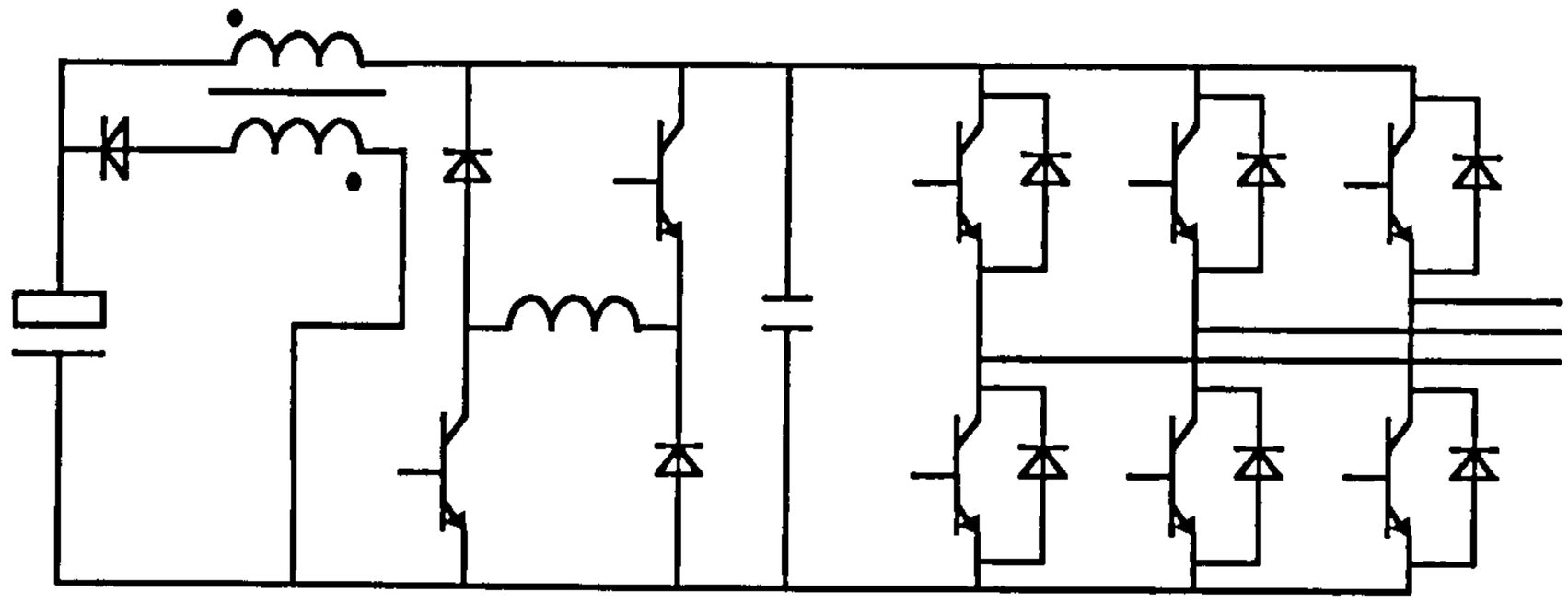
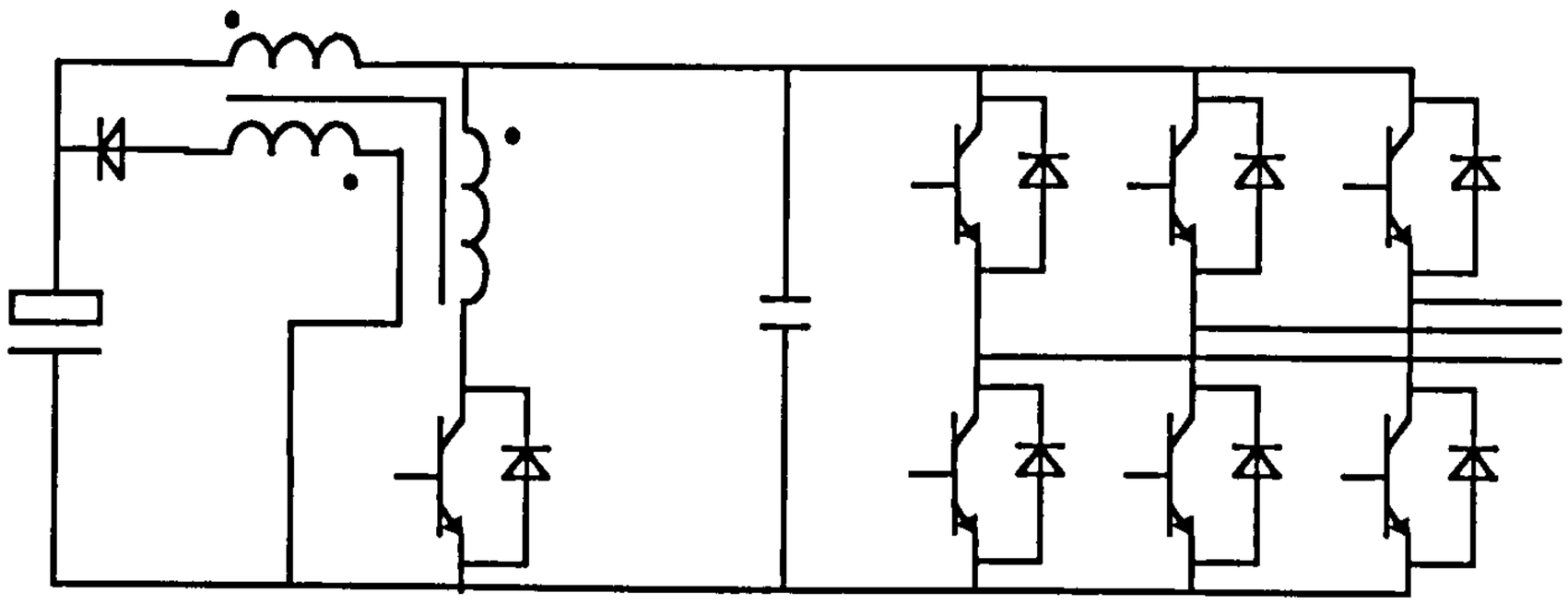
	clamp basic RDCL
[3.11], [5.3], [3.13], [5.5]	
[3.19], [5.6], [3.20], [5.7]	
[3.12], [5.4]	

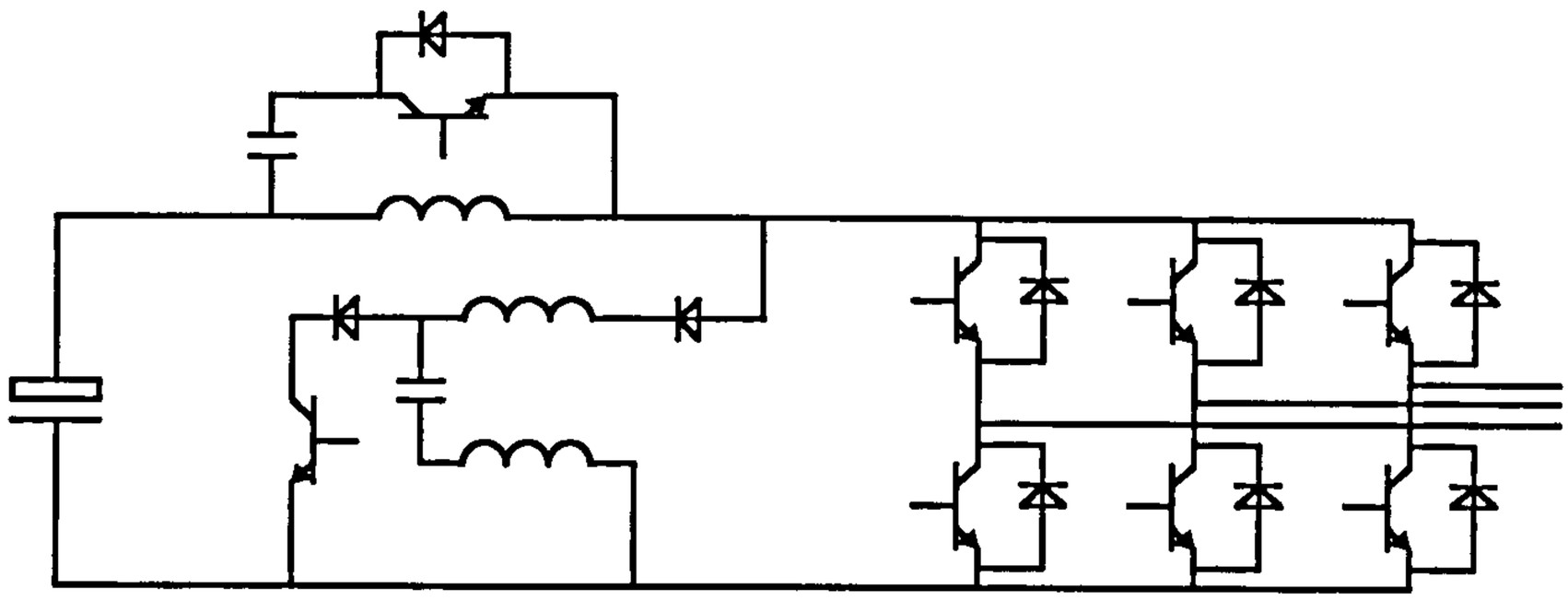
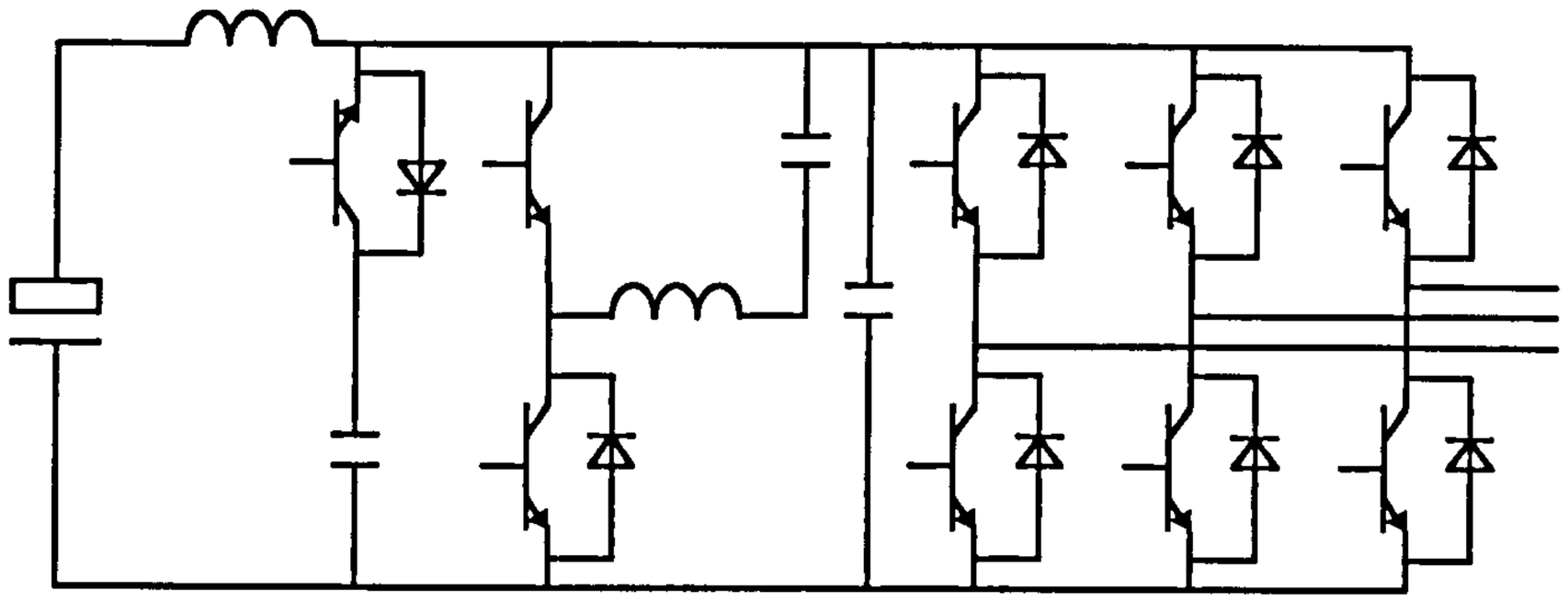
	PRDCL
[3.23], [5.10], [3.22], [5.9]	

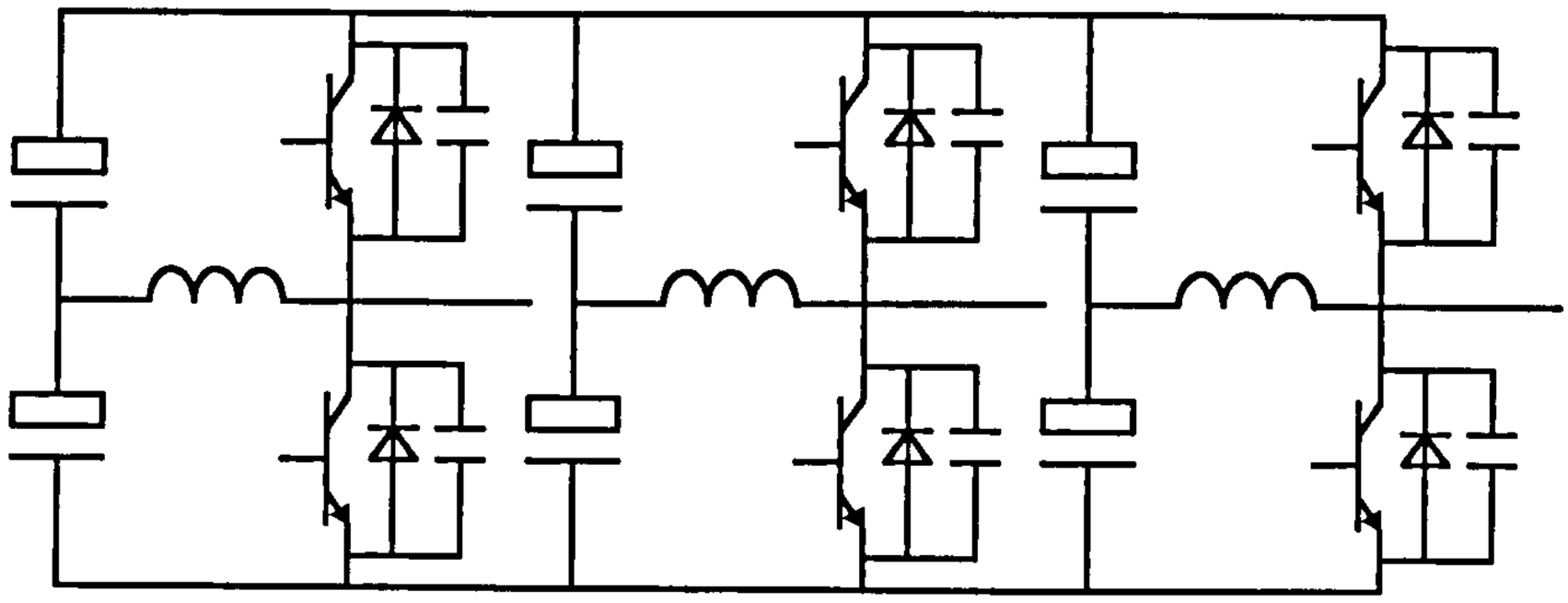
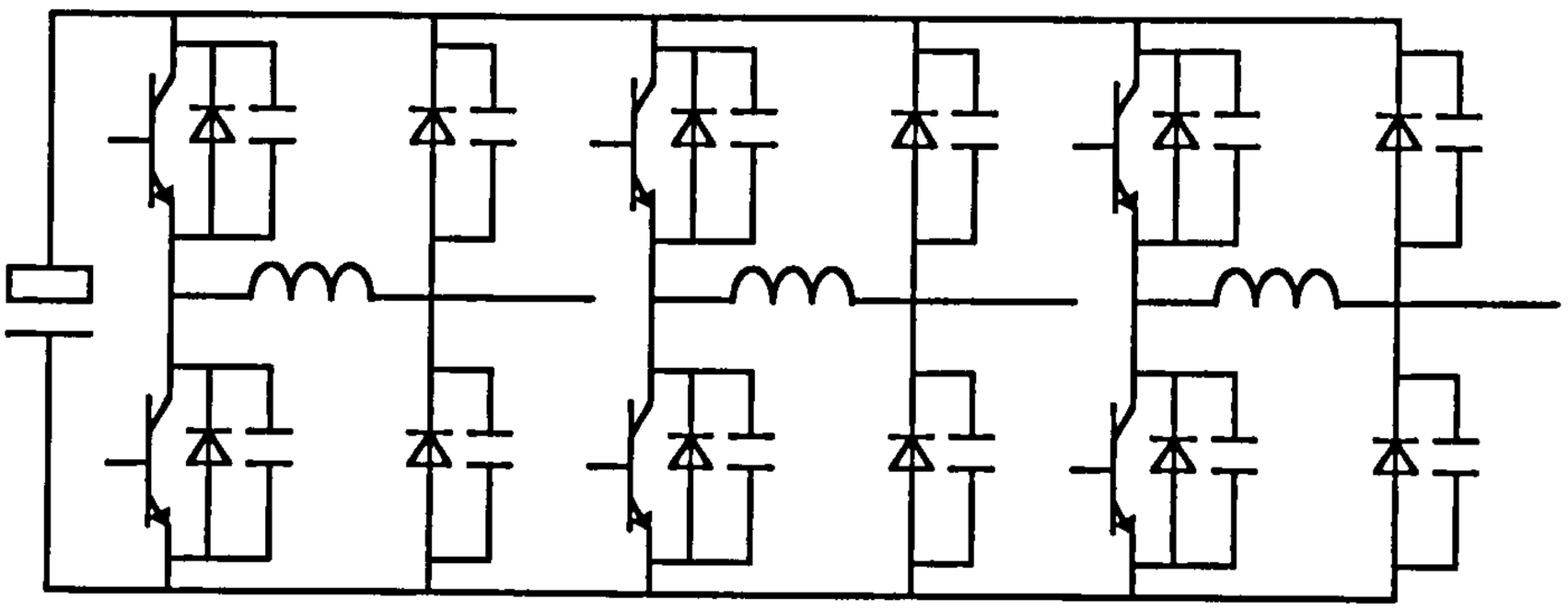
[2.31], [3.24], [5.13]	
[5.12]	
[3.26], [5.15]	
[3.27], [5.16]	

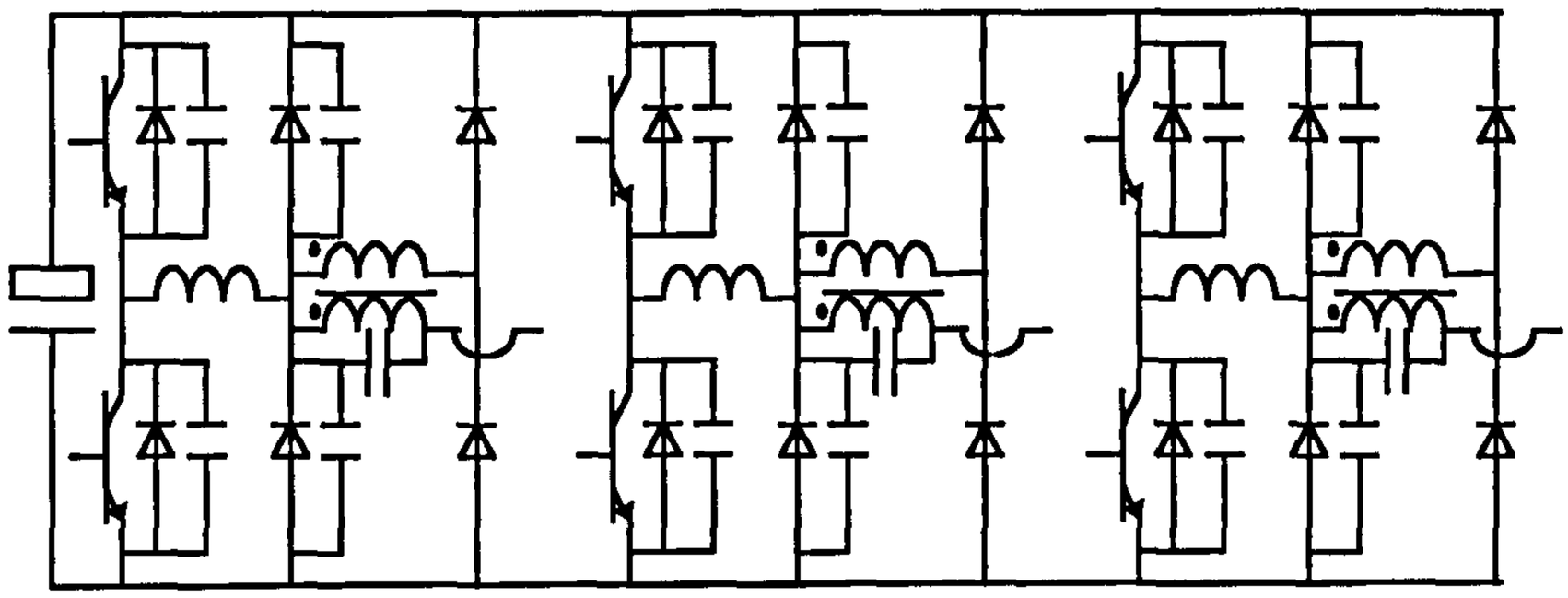
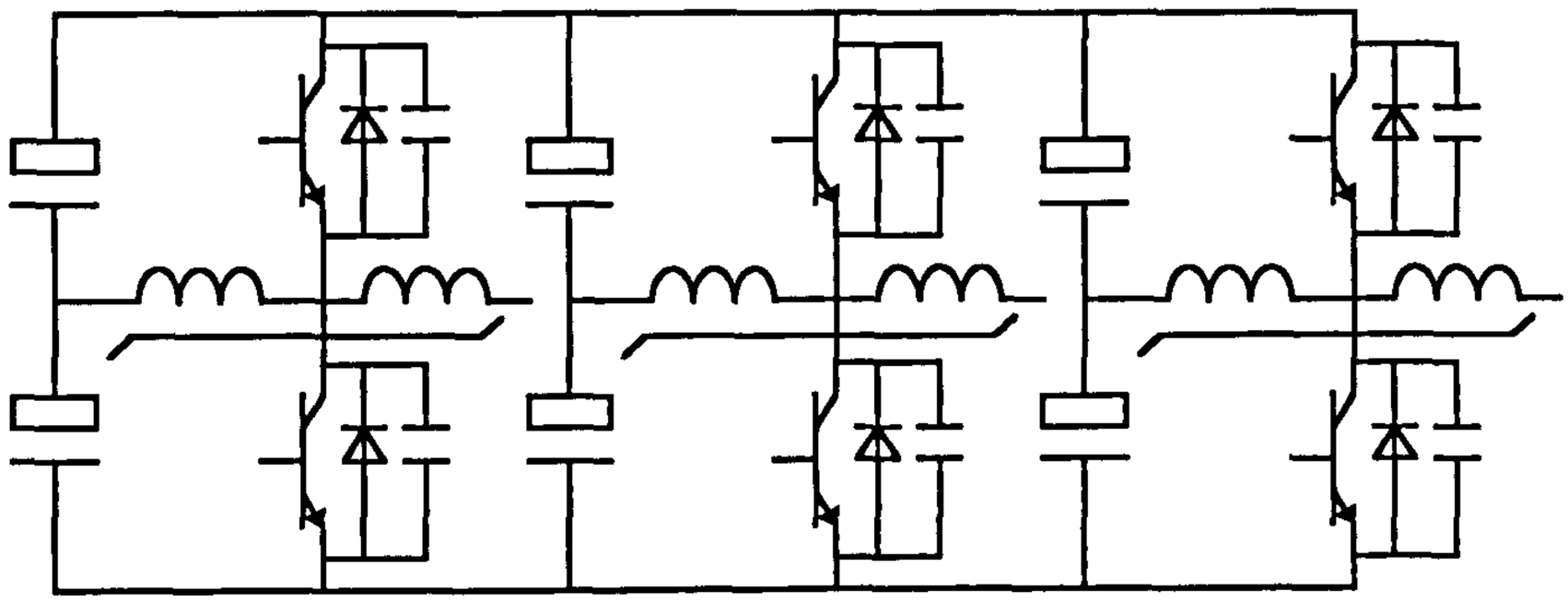
[3.29], [5.14]	
[3.25], [5.11]	

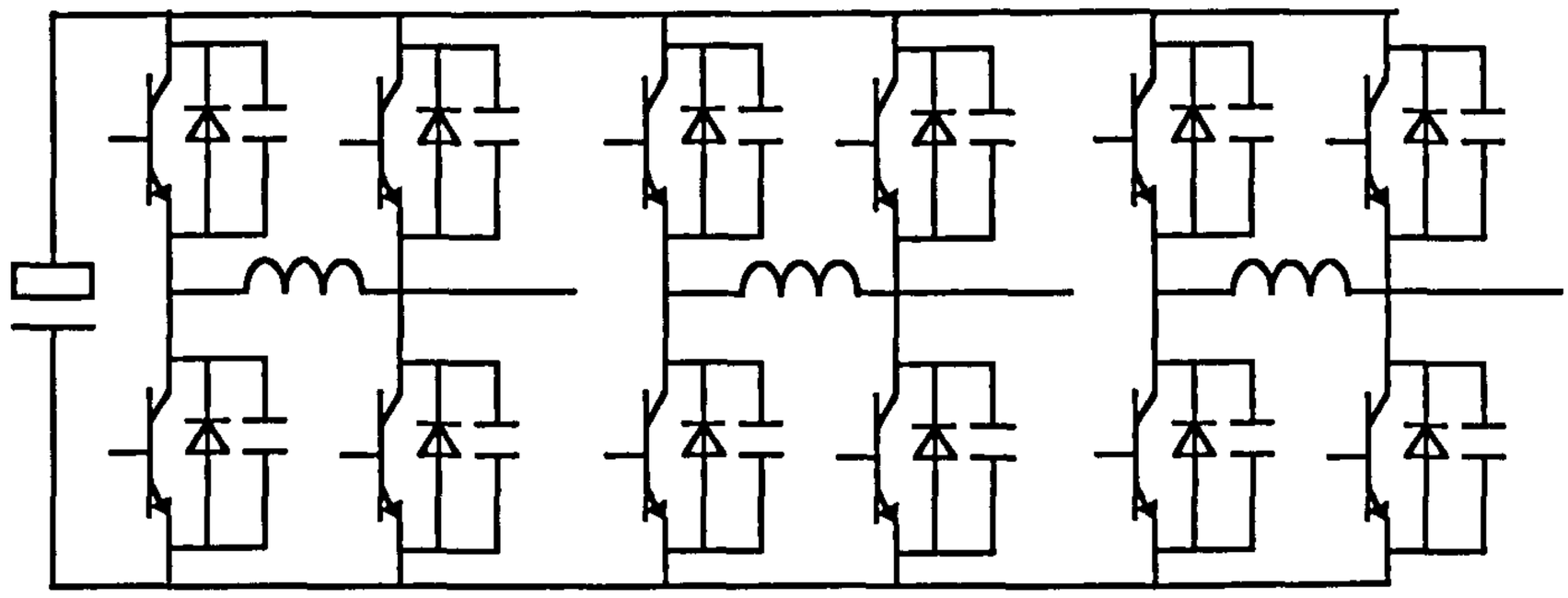
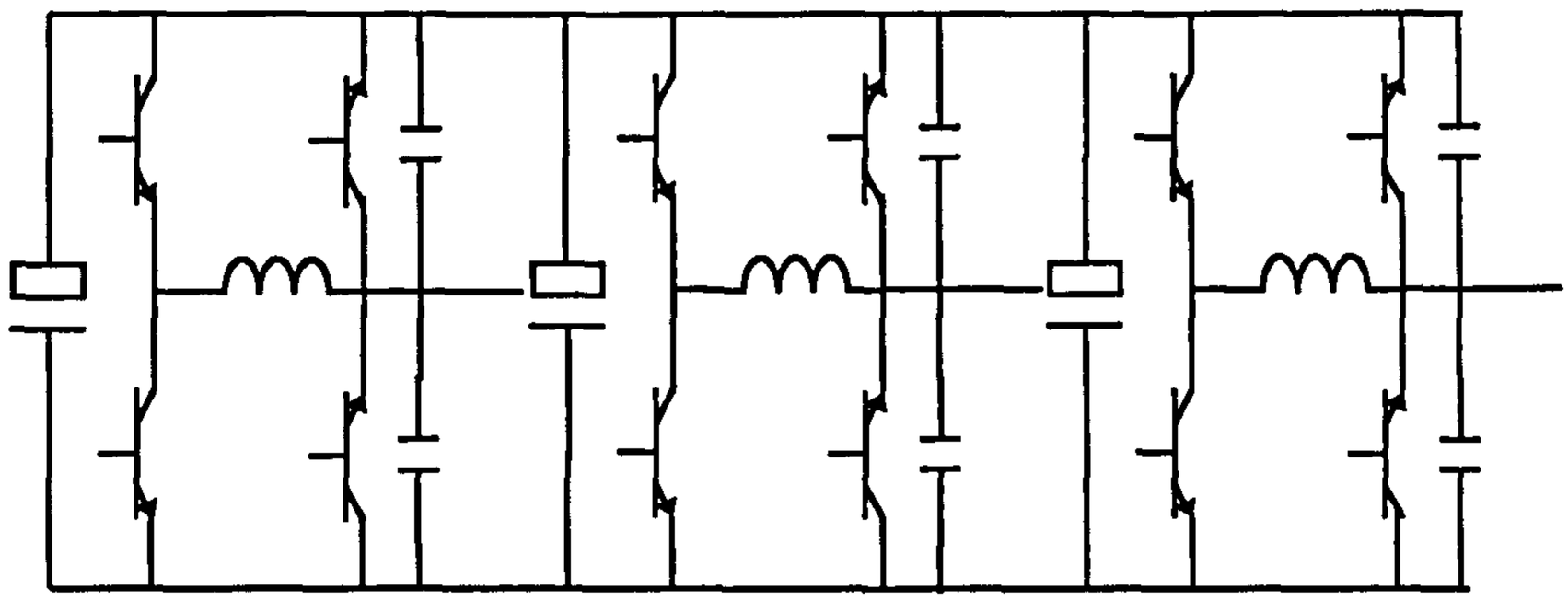
	q-RDCL
[2.29], [3.39], [5.18]	
[2.37], [3.38], [5.17]	

[2.34], [3.35], [5.21]	
[2.39], [3.41], [5.23]	
[2.38], [3.40], [5.8], [2.36]	
[2.35], [3.36], [5.24]	

[2.33], [3.34], [5.20]	
[3.42], [5.22]	

	RPI
[4.1], [5.25]	
[4.2], [5.26]	

[4.3], [5.27]	
[4.4], [5.30], [4.5], [5.29], [4.6], [5.31], [4.7], [5.28], [4.8], [5.32]	

	ARPI
[4.9], [5.25], [4.10], [5.33]	
[4.11]	

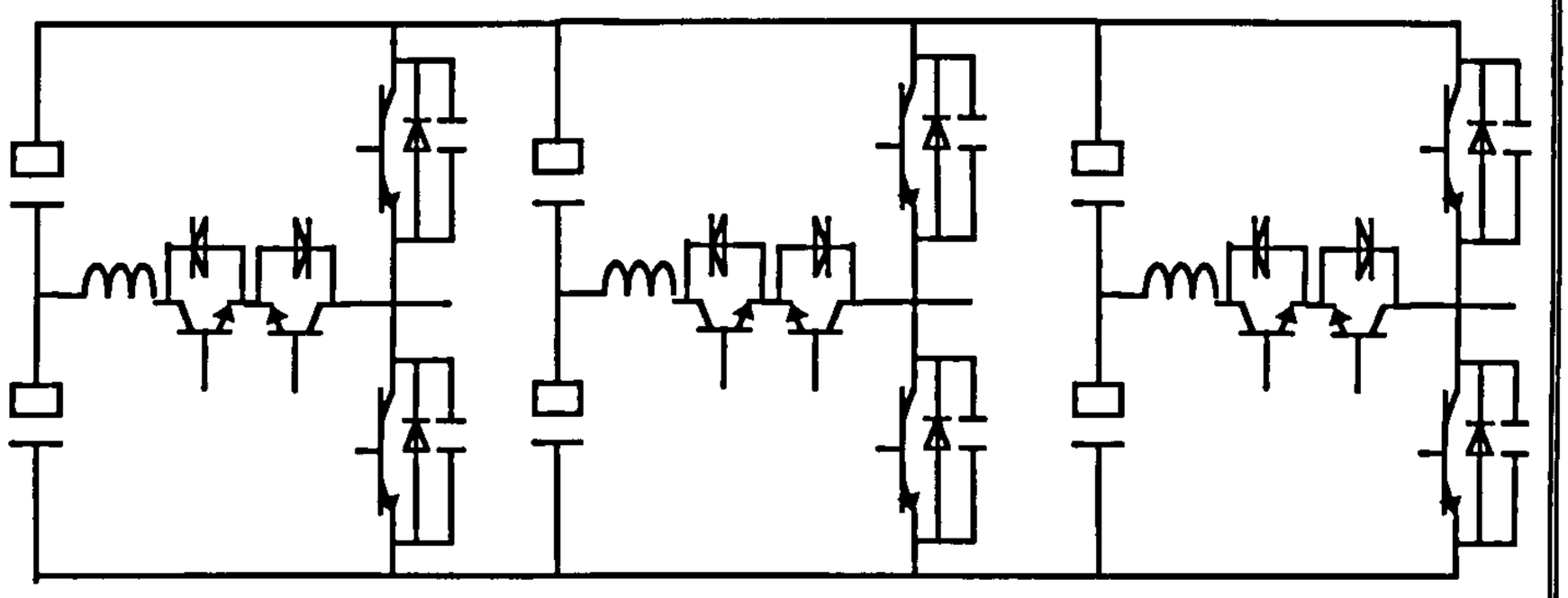
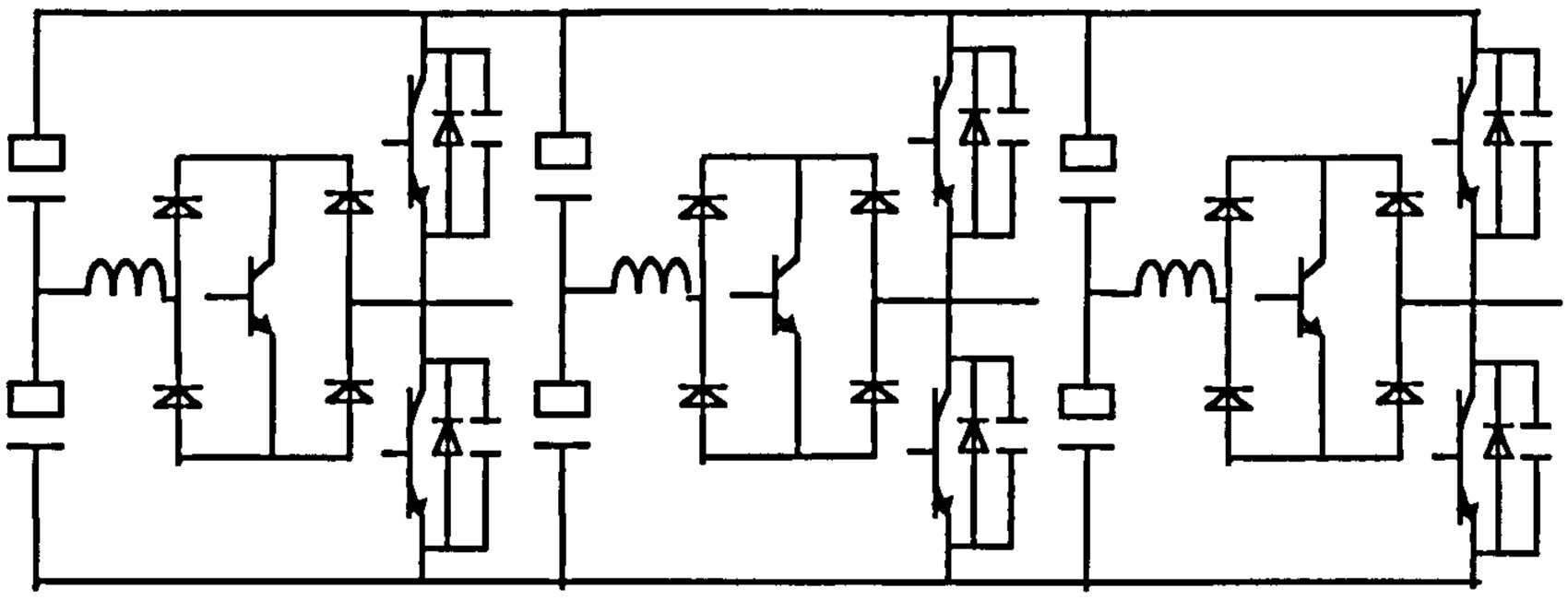
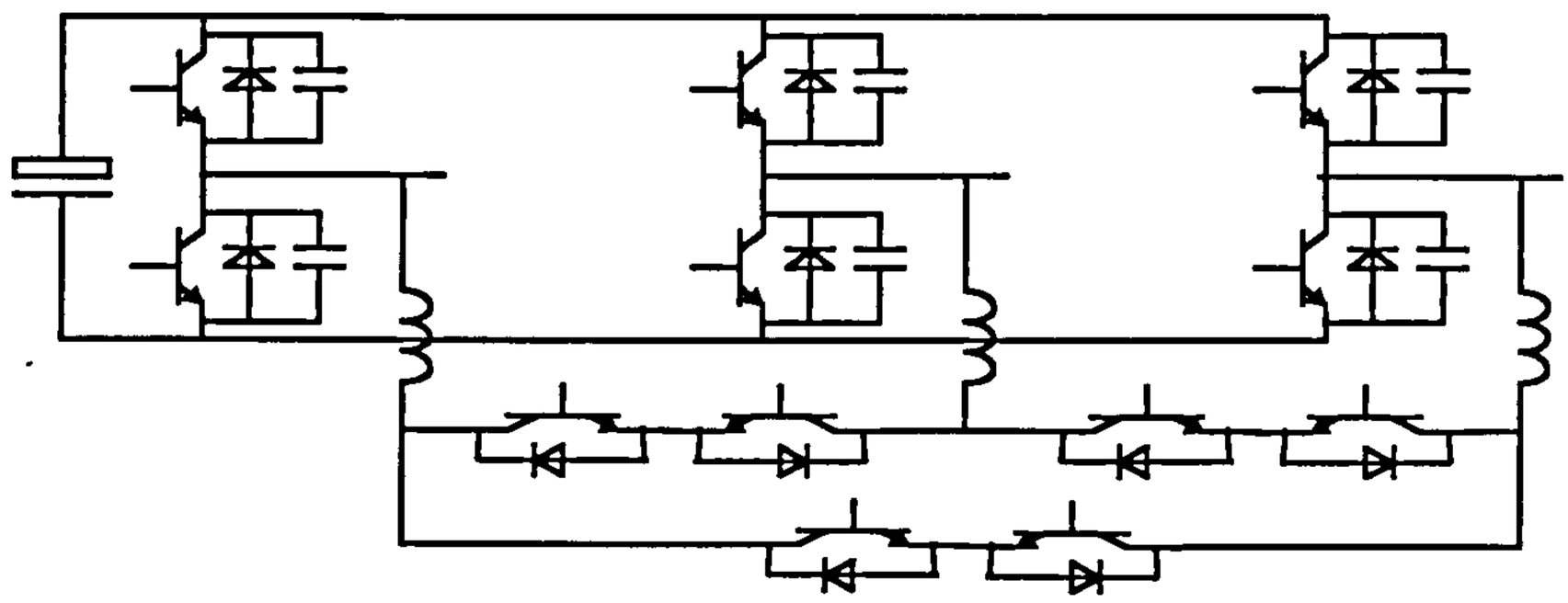
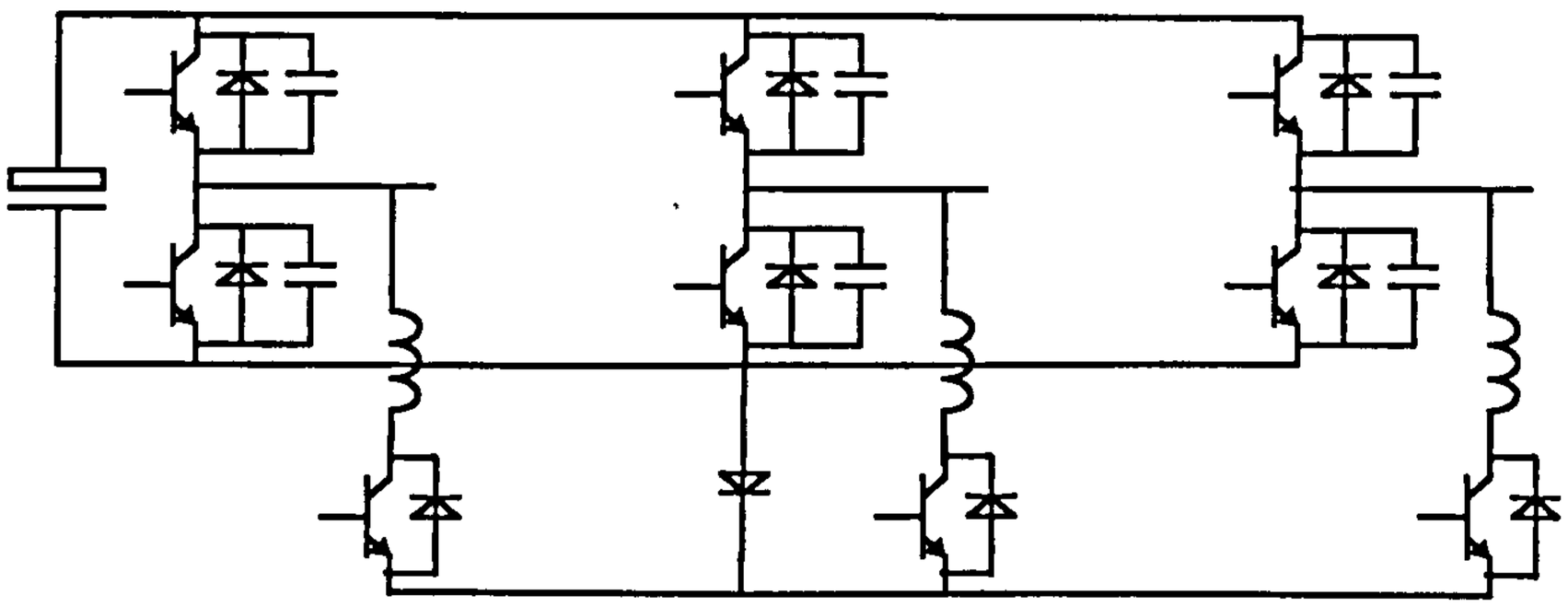
[4.12], [4.13], [2.30], [4.14], [5.34], [4.15], [4.16], [6.4], [4.17], [6.2], [7.1], [4.21], [4.22]	
[4.16], [6.4], [4.17], [6.2], [7.1]	
[4.18], [5.35]	
[4.19], [5.36]	

Table D.1: Overview of softswitching topologies discussed in this thesis.

Appendix E

A PICTORIAL EXPLANATION OF THE CONVERTER

The purpose of this appendix is to enable the visualisation of the converter and test arrangements described in this thesis. The appendix includes pictures coupled with a brief description of each.

Figure E.1: The picture shows the complete test arrangement and converter. Left: Resistor bank and load inductors, Middle background: Converter, Centre front: Measurement equipment, Right: PC and controller unit.

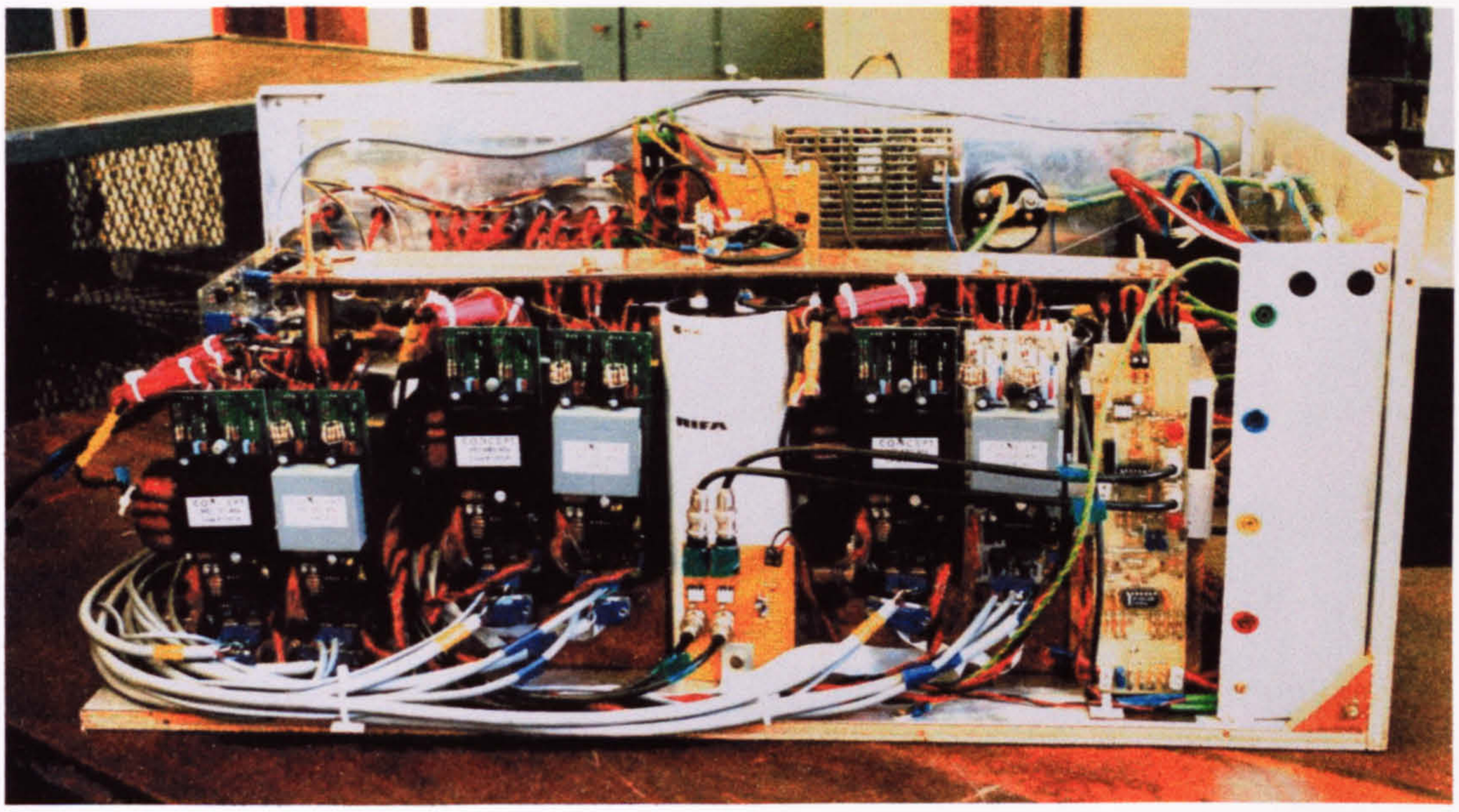


Figure E.2: The back of the converter. PCB cards that include the grey or black square devices are driver cards. The two left driver cards control the IGBTs on which have taken the most measurements. The centre of the picture shows one of the large dc-link electrolytic capacitors. The sandwich layer of the dc bus is mounted on the top of it. In the background one of the auxiliary power supplies is shown (golden mesh).

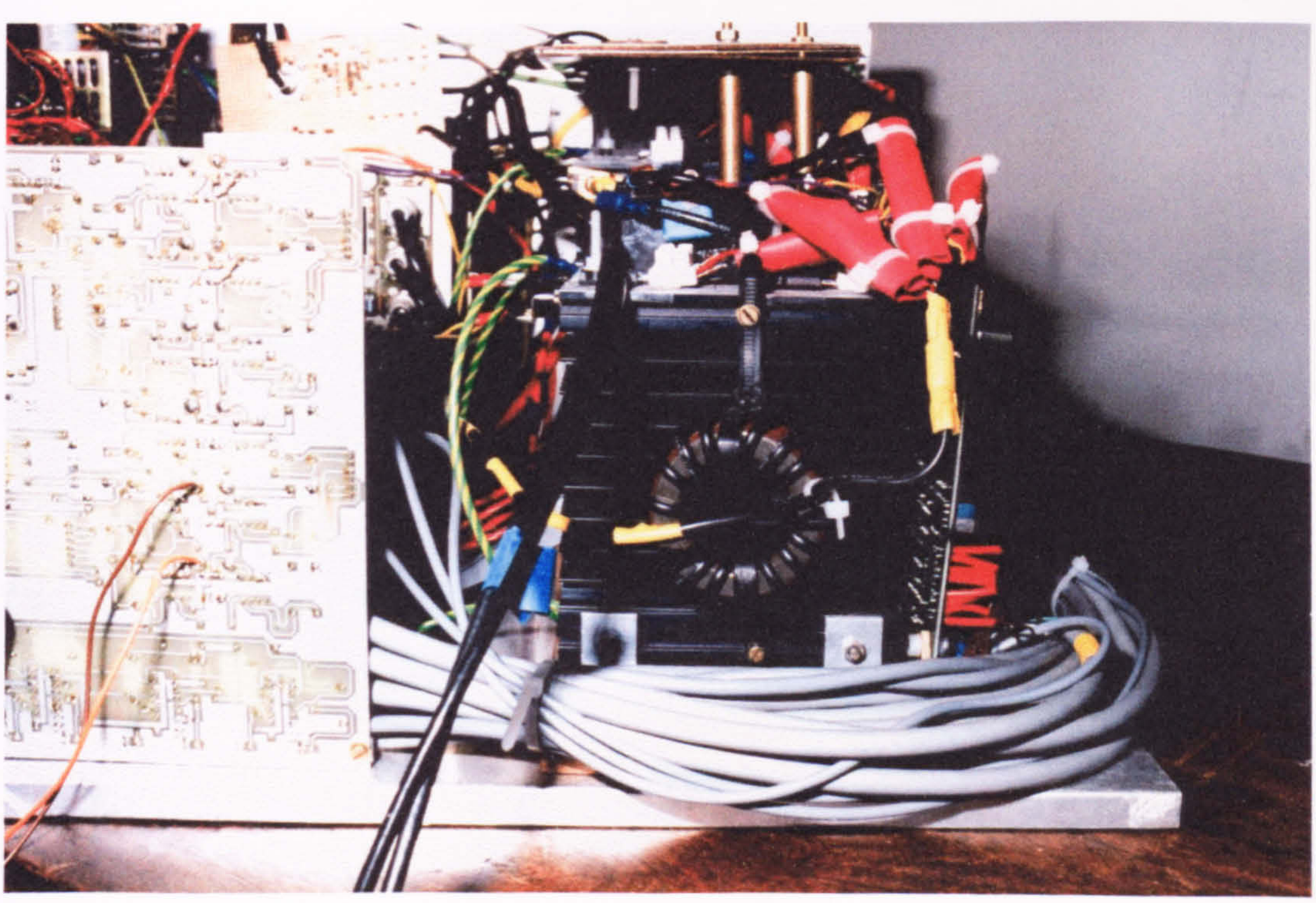


Figure E.3: Side view of the converter. The resonant inductor is screwed onto the heatsink. The two copper spacers connect electrically the dc bus bar and the main power module. Beside the left copper spacer one resonant capacitor is shown (blue).

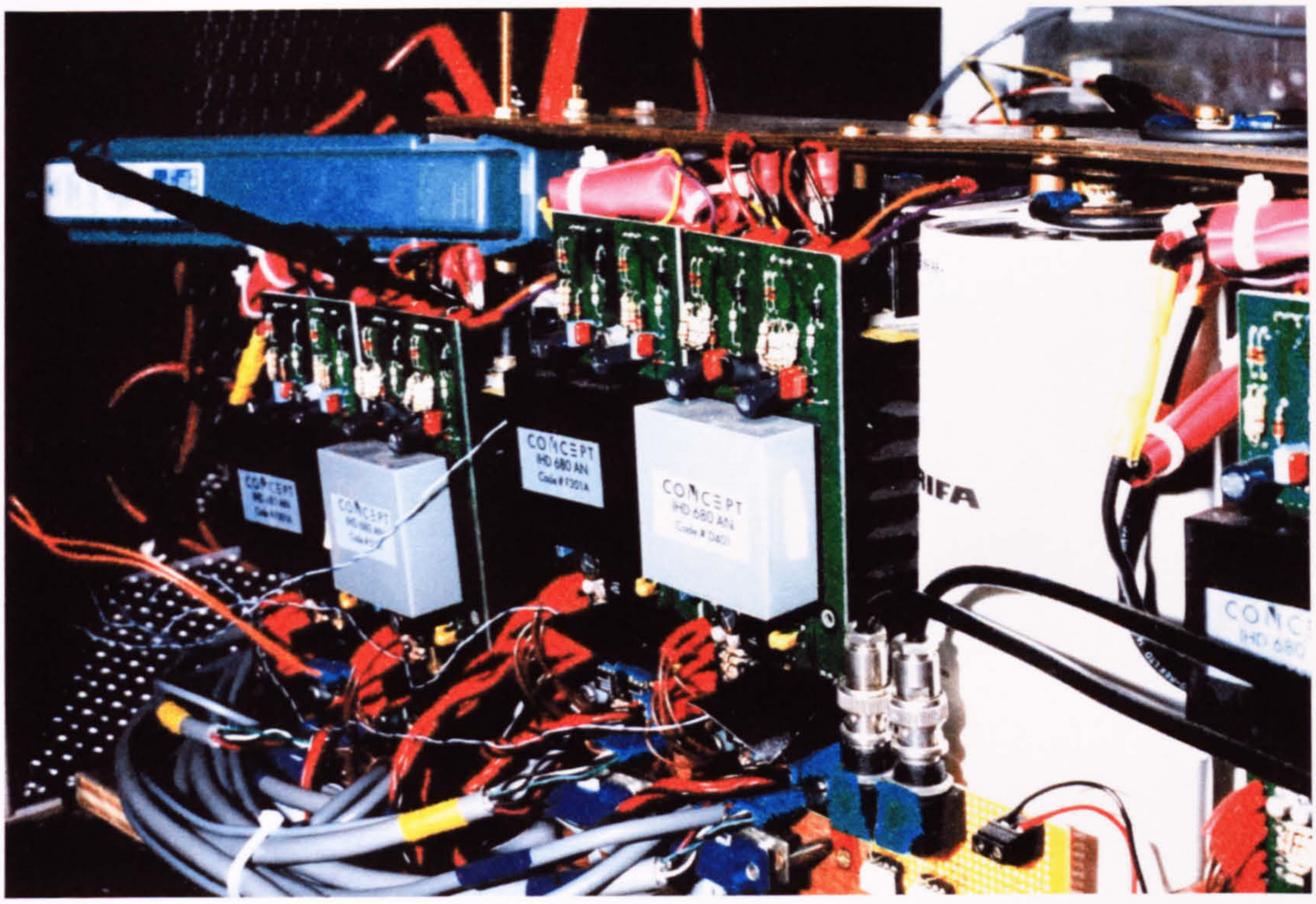


Figure E.4: The picture shows the arrangement and positioning of the test probes during test modes. The large blue probe is a current transducer and the black and red probes measure different voltage potentials.

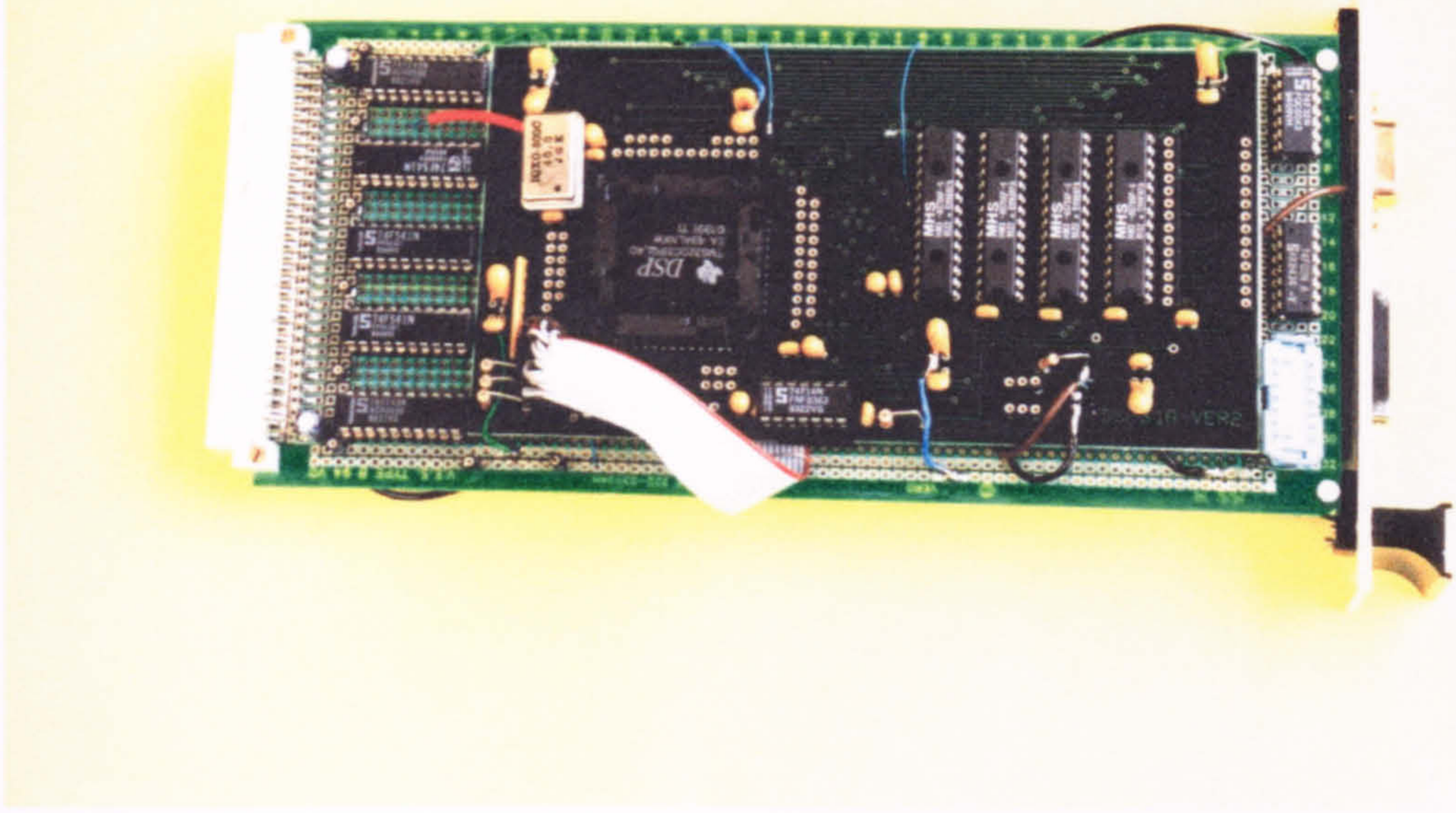


Figure E.5: DSP controller card. Left: ICs for communication to the backplane, Silver square: Quartz crystal for clocking the DSP, Centre: DSP itself, Right: Memory chips.

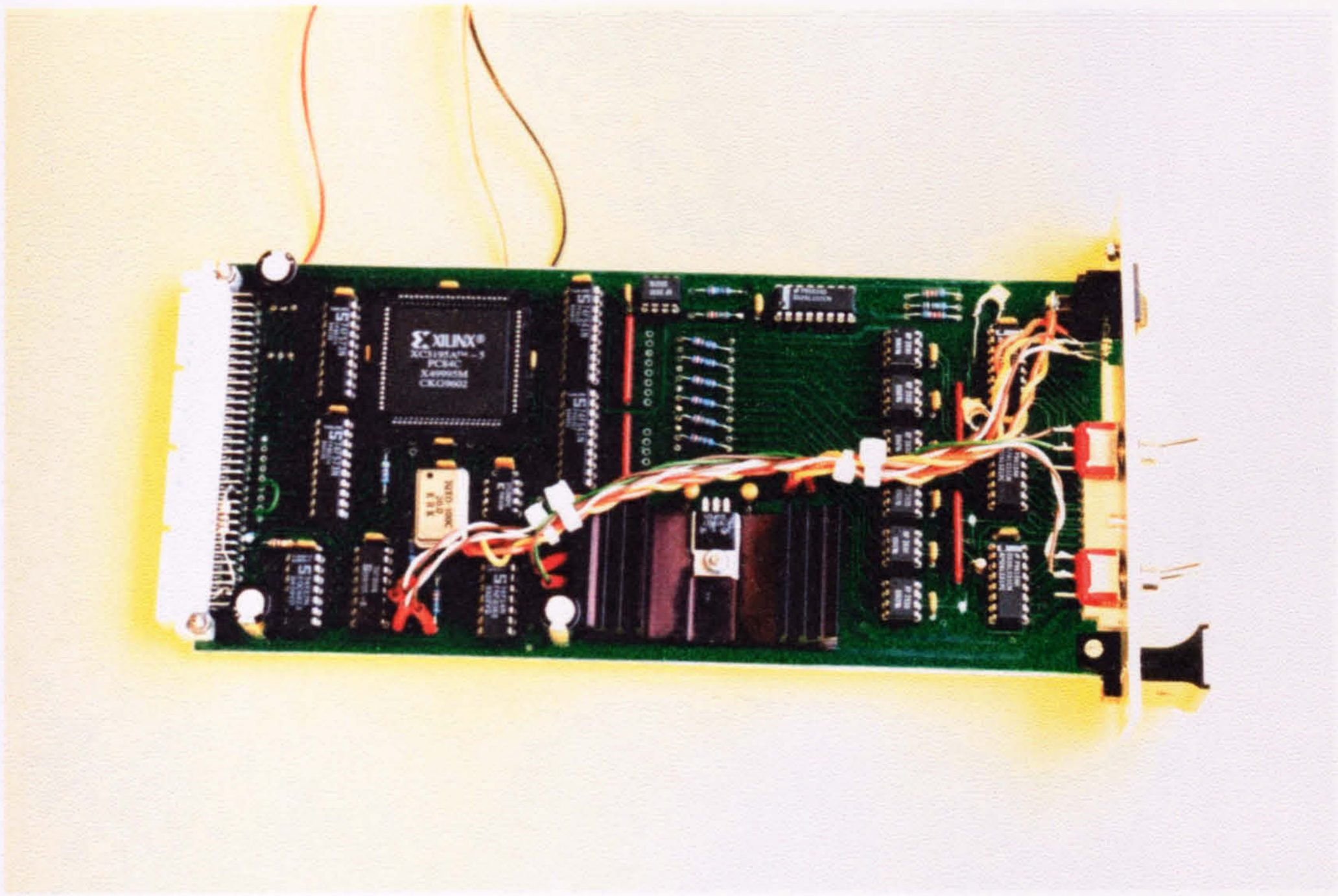


Figure E.6: FPGA card. Left from the heatsink: FPGA with communication devices for the backplane, quartz crystal and buffer ICs, Right from the heatsink: Opto-couplers and transreceiver units for electrical isolation and communication to the driver cards.

References

[1.1] Scharf A, Optimism in Industry, PCIM Europe Journal, No.6, p369 and 370, Building Blocks for Drives, p374, December 1996

[1.2] van Wyk JD, Power Electronic Converters for Motion Control, IEEE Proceedings, Vol.82, No.8, p1164-1193, August 1994

[1.3] Rissik H, Mercury-Arc Current Converters, London, UK: Pitman, 1935.

[1.4] Presser E, Der Selenengleichrichter, Elektrotechnische Zeitung, Vol.62, p3-16, 1932.

[1.5] Bose BK, Power Electronics—An Emerging Technology, IEEE Transaction on Industry Applications, Vol.36, No.3, p403-412, August 1989.

[1.6] Uhrig RE, Introduction to Artificial Neural Networks, IEEE PESC Conference Record, p33-37, 1995.

[1.7] Souse GCD, Bose BK, Fuzzy Logic Applications to Power Electronics and Drives – An Overview, IEEE PESC Conference Record, p57-62, 1995.

[1.8] van Wyk JD, Skudelny H-CH, Müller-Hellmann A, Power electronics, control of the electromechanical energy conversion process and some applications, IEE Proceedings, Vol. 133, Part B, No. 6, p369-399, 1986.

[1.9] Bose KB, Evaluation of Modern Power Semiconductor Devices and Future Trend of Converters, IEEE IAS Annual Meeting Conference Record, p790-797, 1989.

[1.10] Bose KB, Power Electronics—A Technology Review, IEEE Proceedings, Vol.80, No.8, p1303-1334, August 1992.

[1.11] Stockmeier T, Bayerer R, Sinerius D, Herr E, Thiemann U, Reliable, 1200A, 2500V IGBT modules for Traction Applications, IEE Colloquium on „IGBT propulsion drives“, London, Digest No: 1995/081, p3/1-3/13, 1995.

[1.12] Skudelny H-CH, Stromrichtertechnik, Hilfsblattsammlung zur Vorlesung Stromrichtertechnik WS 1991/1992, 1991.

[1.13] Brosch PF, Frequenzumrichter, Die Bibliothek der Technik Band 36, Verlag Moderne Industrie.

[1.14] Wang K, Lee FC, Hua G, Borojevic D, A comparative Study of Losses of IGBTs under Hardswitching, Zero-Voltage and Zero Current Switching,, IEEE PESC Conference Record, p1196-1204, 1994.

[1.15] Heumann K, Keller C, Sommer R, IEEE Behaviour of IGBT Modules in Zero-Voltage-Switch Applications, IEEE PESC Conference Record, p 19-25, 1992

[1.16] Heumann K, Keller C, Sommer R, Comparison of Stresses in IGBT Devices using the Quasi-Resonant Current Mode, EPE Firenze, Vol. 0, p209-214, 1991

[1.17] Forsyth AJ, Review of Resonant Techniques in Power Electronic Systems, IEE Power Engineering Journal, Vol.10, No.3, p110-120, June 1996.

[1.18] Schönung A, Stemmler H, Geregelter Drehstrom-Umkehrantrieb mit gesteuertem Umrichter nach dem Unterschwingungsverfahren, Brown Boveri Mittschrift 51, p555-577, 1964.

[1.19] Patel HS, Hoft RG, Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters, IEEE Transaction on Industry Applications, IA-9, No.3, p , (Part I) and IA-10, No 5 (Part II), p , 1973.

[1.20] Bowes SR, Clements RR, Computer aided Design of PWM Inverter Systems, IEE Proceedings B.1, p1-17, 1982.

[1.21] Eibel J, Jötten R, Control of a Three-Level Switching Inverter, Feeding a Three-Phase Machine by a Microprocessor, VDE Conference „Mikroelektronik in der Stromrichtertechnik und bei elektrischen Antrieben", Darmstadt, Proceedings paper, p217-222, 1982.

[1.22] Busse A, Holtz J, A digital Space Vector Modulator for the Control of a Three-Phase Power Converter, VDE Conference „Mikroelektronik in der Stromrichtertechnik und bei elektrischen Antrieben", Darmstadt, Proceedings paper, p189-195, 1982.

[1.23] van der Broeck HW, Skudelny H-CH, Stanke GV, Analysis and realization of a Pulse-width Modulator Based on Voltage Space Vectors, IEEE Transaction on Industry Applications, IA-24, No.1, p , 1988.

[1.24] Andersen ECH, Haun A, Influence of the Pulse-width Modulation Control Method on the Performance of Frequency Inverter Induction Motor Drives, ETEP, Vol.13, No.2, p151-161, March/April 1993.

[1.25] Depenbrock M, Direct Self-Control (DSC) of Inverter-Fed Induction Machine, IEEE Transactions on Power Electronics, Vol.3, No.4, p420-429, October 1988.

[1.26] Takahashi I, Noguchi T A New, Quick-Response and High-Efficiency Control strategy of an Induction Motor, IEEE Transactions on Industry Applications, Vol.22, No.5, p820-827, September/October 1986.

[1.27] Lüdtke I, Jayne MG, A Comparative Study of High Performance Speed Control Strategies for Voltage-Sourced PWM Inverter-Fed Induction Motor Drives, IEE Electrical Machine and Drives Conference, p343-348, September 1995.

[1.28] Frequenzumrichter ACS 600, ABB AC-Antriebe, Produktbroschüre, 1996.

[1.29] Kazmierkowski MP, Dzieniakowski MA, Review of Current regulation Techniques for three-Phase PWM Inverters, IEEE IECON, Vol.1, p567-575, 1994.

[1.30] McMurray W, Modulation of the Chopping frequency in DC Choppers and Inverters having Current Hysteresis Control, IEEE Transactions on Industry Applications, Vol.20, No.4, p763-768, 1984.

[2.1] Bose KB, Power Electronics—A Technology Review, IEEE Proceedings, Vol.80, No.8, p1303-1334, August 1992.

[2.2] Daniels AR, Slattery, DT New Power Convertor Technique employing Power Transistor, IEE Proceedings, Vol.125, No.2, p146-150, February 1978.

[2.3] Matsuo T, Bernet S, Colby RS, Lipo TA, Application of the Matrix Converter to Induction Motor Drives, IEEE IAS Annual Meeting Conference Record, p60-67, 1996.

[2.4] Wheeler PW, The Matrix Converter—Future possibilities, IEE Colloquium on „Update on new power electronic techniques", London, Digest No: 1997/091, p1/1-1/5, 1997.

[2.5] Mohan N, Undeland TM, Robbins WP, Power Electronics, Second Edition, Wiley, 1995.

[2.6] Schwarz FC, A Doublesided Cycloconverter, IEEE Transaction on Industrial Electronics, Vol.28, p282-291, 1981.

[2.7] Sul SK, Lipo TA, Design and Performance of a High-Frequency Link Induction Motor Drive operating at Unity Power Factor, IEEE Transaction on Industry Application, Vol.26, p434-440, May/June 1990.

[2.8] Newton C, Sumner M, Alexander T, Multi-Level Converters: A real Solution to High Voltage Drives?, IEE Colloquium on „Update on new power electronic techniques“, London, Digest No: 1997/091, p3/1-3/5, 1997.

[2.9] Tennakoon SB, Scheidecker D, Multi-Level Converters for Static Var Compensation, IEE Colloquium on „Update on new power electronic techniques“, London, Digest No: 1997/091, p4/1-4/6, 1997.

[2.10] Gjugyi L, Pelly B, Static Frequency Changers, Wiley, 1976.

[2.11] Alesina A, Venturini MGB, Analysis and Design of Optimum-Amplitude Nine-Switch Direct AC-AC Converters, IEEE Transaction on Power Electronics, Vol.4, No. 1, p101-112, January 1989.

[2.12] Bernet S, Bernet K, Lipo TA, The Auxiliary Resonant Commutated Pole Matrix Converter-A new Topology for High Power Applications, IEEE IAS Annual Meeting Conference Record, Vol.2, p 1242-1249, 1996.

[2.13] Huisman H, de Haan SWH, A DC to 3-Phase Series-Resonant Converter with low Harmonic Distortion, IEEE Transaction on Industry Electronics, Vol.32, No.2, p142-149, 1985.

[2.14] Schwarz FC, Klaassens JB, A Controllable 45-kW Current Source for DC Machines, IEEE Transaction on Industry Application, Vol.15, No.4, p437-444, 1979.

[2.15] Oruganti R, Lee FC, State-Plane Analysis of Parallel Resonant Converter, PESC Conference Record, p56-73, 1989.

[2.16] Finney SJ, Green TC, Williams BW, Review of Resonant Link Topologies for Inverters, IEE Proceedings-B, Vol.140, No.2, p103-114, March 1993.

[2.17] Klaasens JB, de Beer F, Three-Phase AC-to-AC Series-Resonant Power Converter with a reduced Number of Thyristors, IEEE PESC Conference Record, p376-384, 1989.

[2.18] van Wesenbeck,MPN, Klaasens JB, Controllable AC-AC Converter with Soft-Switching, EPE, p261-266, 1993.

[2.19] Bhowmik S, Spée R, A Guide to the Application-Oriented Selection of AC/AC Converter Topologies, IEEE Transaction on Power Electronics, Vol.8, No.2, p156-163, 1993.

[2.20] Lauw HK, Klaassens JB, Butler NG, Seely DB, Variable-Speed Generation with the Series-Resonant Converter, IEEE Transaction on Energy Conversion, Vol.3, No.4, p755-764, 1988.

[2.21] Drury W, PCIM Journal, March/April 1995.

[2.22] Barras PG, High Performance Switch Reluctance Drives, Thesis at Dept. Of Electrical Engineering, University of Newcastle upon Tyne, September 1995.

[2.23] Skudelny H-CH, Stromrichtertechnik, Hilfsblattsammlung zur Vorlesung Stromrichtertechnik WS 1991/1992, 1991.

[2.24] Siemens and John Wiley & Sohns, John, Wiley & Sons Verlag Electrical Engineering Handbook, New York, 1985

[2.25] Ziogas PD, Ranganathan VT, Stefanoviç VR, Four-Quadrant Current Regulated Converter with a High-Frequency Link, IEEE Transaction on Industry Application, Vol.18, No.5, p499-506, September/October 1982.

[2.26] Espelage PM, Bose BK, High Frequency Link Power Conversion, IEEE IAS Annual Meeting Conference Record, p802-808, 1975.

[2.27] Gyugyi L, Cibulka F, The High-Frequency Base Converter—A New Approach to Static High-Power Conversion, IEEE Transaction on Industry Application, Vol.15, No.4, p420-429, 1979.

[2.28] Divan DM, The Resonant DC Link Converter – A New Concept in Static Power Conversion, IEEE IAS Annual Meeting Conference Record, p648-656, 1986.

[2.29] Malesani L, Tenti P, Divan DM, Tiogo V, A Synchronized Resonant DC Link Converter for Soft-Switched PWM, IEEE IAS Annual Meeting Conference Record, p1037-1044, 1989.

[2.30] DeDoncker RW, Lyons JP, The Auxiliary Resonant Commutated Pole Converter, IEEE IAS Annual Meeting Conference Record, p1228-1235, 1990.

[2.31] Cho JG, Kim HS, Cho GH, Novel Softswitching PWM Converter using a New Parallel Resonant DC-Link, PESC Conference Record, p241-247, 1991.

[2.32] Taniguchi K, Yoshikawa T, Hirachi K, Tomokuni Y, A Quasi-Resonant PWM Converter with High Quality Input Waveforms and High Efficiency, PESC Conference Record, Vol.2, p1131-1136, 1994.

[2.33] Sikorski A, Citko T, Quasi-Resonant Parallel Dc-Link Circuit for High-Frequency DC-AC Inverters, EPE, p174-177, 1993.

[2.34] Bornhardt KE, Novel Soft-Switched GTO-Inverter Circuits, IEEE IAS Conference Proceedings, p1222-1227, 1990.

[2.35] Chen S, Lipo TA, Soft-Switched Inverter for Electric Vehicle Drives, IEEE IAS Annual Meeting Conference Record, p586-591, 1995.

[2.36] Chen S, Filho BJC, Lipo TA, Design and Implementation of a Passively Clamped Quasi Resonant DC Link Inverter, IEEE IAS Annual Meeting Conference Record, p2387-2392, 1995.

[2.37] Venkataramanan G, Divan D, Pulse Width Modulation with Resonant DC Link Converters, IEEE IAS Annual Meeting Conference Record, Vol.2, p984-990, 1990.

[2.38] Chen S, Lipo TA, A Passively Clamped Quasi Resonant DC Link Inverter, IEEE IAS Annual Meeting Conference Record, p841-848, 1994.

[2.39] Salame S, Tadros Y, Novel Softswitching Quasi Resonant 3-Phase IGBT Inverter, EPE, p2.095-2.099, 1995.

[3.1] Divan DM, The Resonant DC Link Converter – A New Concept in Static Power Conversion, IEEE IAS Annual Meeting Conference Record, p648-656, 1986.

[3.2] Lai J-S, Bose BK, An Improved Resonant DC Link Inverter for Induction Motor Drives, IEEE IAS Annual Meeting Conference Record, p742-748, 1988.

[3.3] Kheraluwala MH, Divan DM, Delta Modulation Strategies for Resonant Link Inverters, IEEE Transaction on Power Electronics, Vol.5, No.2, p220-228, April 1990.

[3.4] Lorenz RD, Divan DM, Dynamic Analysis & Experimental Evaluation of Delta Modulators for Field Oriented AC Machine Current Regulators, IEEE IAS Annual Meeting Conference Record, Atlanta, p196-201, 1987.

[3.5] Habetler TG, Divan DM, Performance Charactrization of a New Discrete Pulse Modulated Current Regulator, IEEE IAS Annual Meeting Conference Record, p395-405, 1988.

[3.6] Mertens A, Skudelny H-CH, Calculations on the Spectral Performance of Discrete Pulse Modulation Strategies, IEEE PESC Conference Record, p357-365, 1991.

[3.7] Finney SJ, Green TC, Williams BW, Spectral Characteristics of Resonant-Link Inverters, IEEE Transaction on Power Electronics, Vol.8, No.4, p562-570, October 1993.

[3.8] Kazmierkowski MP, Dzieniakowski MA, Review of Current regulation Techniques for three-Phase PWM Inverters, IEEE IECON, Vol.1, p567-575, 1994.

[3.9] Steele R, Delta Modulation Systems, London: Pentech, 1975.

[3.10] Dehmlow M, Heumann K, Sommer R, Resonant Inverter Systems for Drive Applications, EPE Journal, Vol.2, No.4, p225-232, 1992.

[3.11] Divan DM, Skibinski G, Zero-Switching-Loss Inverters for High-Power Applications, IEEE Transaction on Industry Applications, Vol.25, No.4, p634-643, July/August 1989.

[3.12] Kondo S, Yang SH, Takizawa S, Harashima F, Resonant DC Link Dual Converter System for Motor Drives, IEEE IAS Annual Meeting Conference Record, p789-794, 1991.

[3.13] Mertens A, Design of a 20KVA Resonant Dc Link IGBT Inverter on the Base of Experimental Device Evaluation, EPE, Firenze, Vol.4, p172-177, 1991.

[3.14] van Wyk JD, Present and Future Trends in Power Electronic Converters, EPE, Sevilla, Vol.0, p1-16, 1995.

[3.15] Fregien G, van Wyk JD, Non-Linear Capacitors in Snubber Circuits for GTO-Thyristors, IEEE PESC Conference Record, Milwaukee, p204-210, June 1989.

[3.16] Gluskin E, The use of Non-Linear Capacitors, International Journal of Electronics, Vol.58, No.1, p63-81, 1985.

[3.17] Harada K, Katsuki A, Fujiwara M, Nakajima H, Matsushita H, Resonant Converter Controlled by Variable Capacitance Devices, IEEE Transaction on Power Electronics, Vol.8, No.4, p404-410, October 1993.

[3.18] Takahashi I, Sato T, Takeda M, Applications of Nonlinear Impedance Circuit Composed of Diodes and Capacitors or Inductors, IEEE IAS Annual Meeting Conference Record, Vol.2, p757-762, 1993.

[3.19] Schülting L, A 100kVA Resonant DC Link Inverter with GTOs - Design Considerations and First Practical Experience -, IEEE IAS Annual Meeting Conference Record, p729-736, 1992.

[3.20] Skibinski GL, Divan DM, Design Integration of a 200kW GTO RDCL Converter, IEEE IAS Annual Meeting Conference Record, Vol.2, p1029-1040, 1993.

[3.21] Chen S, Filha JC, Lipo TA, Design and Implementation of a Passively Clamped Quasi Resonant DC-Link Inverter, IEEE IAS Annual Meeting Conference Record, p. 2387-2392, 1995.

[3.22] He J, Mohan N, Parallel Resonant DC Link Circuit—A Novel Zero Switching Loss Topology with Minimum Voltage Stresses, IEEE Transaction on Power Electronics, Vol.6, No.4, p687-694, October 1991.

[3.23] He J, Mohan N, Wold B, Zero-Voltage-Switching PWM Inverter for High-Frequency DC-AC Power Conversion, IEEE IAS Annual Meeting Conference Record, Seattle, p1215-1221, October 1990.

[3.24] Cho JG, Kim HS, Cho GH, Novel Softswitching PWM Converter using a New Parallel Resonant DC-Link, PESC Conference Record, p241-247, 1991.

[3.25] Krogemann M, Clare JC, Design and Analysis of a PWM Parallel Resonant DC-Link Inverter, EPE, Sevilla, Vol.2, p585-590, 1995.

[3.26] Malesani L, Tenti P, Tomasin P, Toigo V, High Efficiency Quasi-Resonant DC Link Three-Phase Power Inverter for Full-Range PWM, IEEE Transactions on Industry Applications, Vol.31, No. 1, p141-148, January/February 1995.

[3.27] Choi J-W, Sul S-K, Resonant Link Bidirectional Power Converter: Part I—Resonant Circuit, Transactions on Power Electronics, Vol.10, No.4, p479-484, July 1995.

[3.28] Choi J-W, Sul S-K, Resonant Link Bidirectional Power Converter: Part II—Application to Bidirectional AC Drive without Electrolytic Capacitor, Transactions on Power Electronics, Vol.10, No.4, p485-493, July 1995.

[3.29] Doncker RW, Lyons JP, The Auxiliary Quasi-Resonant DC Link Inverter, De IEEE PESC Conference Record, Cambridge MA, p248-253, June 1991.

[3.30] Jobing R, van der Merwe FS, Kamper MJ, Digital Implementation of Bus Clamped Space Vector Modulation, IEEE Transaction on Energy Conversion, Vol. 9, No.2, p344-348, June 1994.

[3.31] Handley PG, Boys JT, Practical real-time PWM Modulators: An Assessment, IEE Proceedings-B, Vol.139, No.2, p96-101, March 1992.

[3.32] Krogemann M, Clare JC, A Softswitching Parallel Quasi Resonant DC-Link Inverter with Modified Asynchronous Space Vector PWM, PEVD Conference Publication, No. 429, p.208-213, September 1996.

[3.33] Taniguchi K, Yoshikawa T, Hirachi K, Tomokuni Y, A Quasi-Resonant PWM Converter with High Quality Input Waveforms and High Efficiency, PESC Conference Record, Vol.2, p1131-1136, 1994.

[3.34] Sikorski A, Citko T, Quasi-Resonant Parallel Dc-Link Circuit for High-Frequency DC-AC Inverters, EPE, p174-177, 1993.

[3.35] Bornhardt KE, Novel Soft-Switched GTO-Inverter Circuits, IEEE IAS Conference Proceedings, p1222-1227, 1990.

[3.36] Chen S, Lipo TA, Soft-Switched Inverter for Electric Vehicle Drives, IEEE IAS Annual Meeting Conference Record, p586-591, 1995.

[3.37] Chen S, Filho BJC, Lipo TA, Design and Implementation of a Passively Clamped Quasi Resonant DC Link Inverter, IEEE IAS Annual Meeting Conference Record, p2387-2392, 1995.

[3.38] Venkataramanan G, Divan D, Pulse Width Modulation with Resonant DC Link Converters, IEEE IAS Annual Meeting Conference Record, Vol.2, p984-990, 1990.

[3.39] Malesani L, Tenti P, Divan DM, Tiogo V, A Synchronized Resonant DC Link Converter for Soft-Switched PWM, IEEE IAS Annual Meeting Conference Record, p1037-1044, 1989.

[3.40] Chen S, Lipo TA, A Passively Clamped Quasi Resonant DC Link Inverter, IEEE IAS Annual Meeting Conference Record, p841-848, 1994.

[3.41] Salame S, Tadros Y, Novel Softswitching Quasi Resonant 3-Phase IGBT Inverter, EPE, p2.095-2.099, 1995.

[3.42] Practical Evaluation of a Quasi-Resonant Circuit for Soft Switched-Inverters with Minimum Voltage Stress, EPE, Sevilla, Vol.2, p.652-657, 1995.

[4.1] Patterson OD, Divan DM, Pseudo-Resonant Full Bridge DC/DC Converter, IEEE PESC Conference Record, p424-430, 1987.

[4.2] Cheriti A, Al- Haddad K, Dessaint LA, Meynard TA, Mukhedkar D, A Rugged Soft Commutated PWM Inverter for AC Drives, IEEE PESC Conference Record, p656-666, 1990.

[4.3] Matsuo H, Iida K, Kurokawa F, Harada K, New Soft-Commutated PWM Inverter with AC Current Transformer, IEEE Proceeding of IECON, Vol.2, p1275-1280, 1993.

[4.4] Ferreira JA, Theron PC, van Wyk JD, van Ross A, Schoeman JJ, Matsemela K, The Nonlinear Resonant Inverter: A New Softswitching Topology, EPE, Firenze, Vol.4, p216-220,1991.

[4.5] Ferreira JA, van Ross A, van Wyk JD, A Hybrid Phase Arm Power Module with Non-Linear Resonant Tank, IEEE IAS Annual Meeting Conference Record, p1679-1685, 1990.

[4.6] Ferreira JA, Theron PC, van Wyk JD, Control of Nonlinear Resonant Pole Inverters, IEEE IAS Annual Meeting Conference Record, p834-839, 1991.

[4.7] Ferreira JA, van Ross A, van Wyk JD, A Generic Softswitching Converter Topology with a Parallel Nonlinear Network for High Power Application, IEEE PESC Conference Record, p298-304, 1990.

[4.8] Burgers KC, van Wyk JD, Case MJ, A High Performance Induction Motor Drive System based on a Non-Linear Resonant Pole Softswitching Inverter, IEEE IAS Annual Meeting Conference Record, p111-118, 1992.

[4.9] Divan DM, Venkataramanan G, De Doncker RW, Design Methodologies for Soft Switched Inverters, IEEE IAS Annual Meeting Conference Record, p758-766, 1988.

[4.10] Chan CC, Chau KT, Yao J, Chan DTW, A Novel Soft-Switching Inverter using Resonant Inductor Freewheeling, Proceedings of PEDS, p215-221, 1997.

[4.11] Kotsopoulos A, Holmes DG, A New Soft-Switched, Thyristor-Based, Regenerative, Quasi-resonant, Current Regulated Inverter suitable for High-Power Applications, IEEE IAS Annual Meeting Conference Record, p842-849, 1994.

[4.12] Bingen G, Utilisation de Transistors a Fort Courant et Tension Elevee, First European Conference on Power Electronics and Applications, Vol.1, p15-20, 1985.

[4.13] McMurray W, Resonant Snubbers with Auxiliary Switches, IEEE IAS Annual Meeting Conference Record, p829-834, 1989.

[4.14] DeDoncker RW, Lyons JP, The Auxiliary Resonant Commutated Pole Converter, IEEE IAS Annual Meeting Conference Record, p1228-1235, 1990.

[4.15] DeDoncker RW, Lyons JP, Control of Three Phase Power Supplies for Ultra Low THD, IEEE APEC, p622-629, 1991.

[4.16] Protiwa F-F, Koß J, A 20kVA Auxiliary resonant Commutated pole Converter--Design and Practical Experiences--, EPE, Sevilla, Vol.2, p111-116, 1995.

[4.17] Eckel H G, Sack L, Rascher K, FPGA based control of an ARCP-Inverter without additional Sensors, EPE, Trondheim, Vol.4, p385-390, 1997.

[4.18] Lai JS, Robert W, Young RW, George W, McKeever JW, Peng FZ, A Delta-Configured Auxiliary Resonant Snubber Inverter, IEEE Trans. On Industry Applications, Vol.32, No.3, p518-525, May/June 1996.

[4.19] Lai JS, Young RW, Ott GW, White CP, McKeever JW, A Novel Resonant Snubber Inverter, IEEE APEC, p797-803, March 1995.

[4.20] Lee Y-D, Set-up Circuits show the Behaviour of resonant Pole Converters, using PSpice, Thesis, Newcastle upon Tyne, Dept. of Electrical and Electronic Engineering, University of Newcastle upon Tyne, 1997.

[4.21] Iida K, Sakuma T, Mechi A, Matsuo H, Kurokawa F, The Influence of the Conducting Inductance in the Auxiliary Resonant Commutated Pole Inverter, IEEE PESC Conference Record, p1238-1245, 1997.

[4.22] Salberta FR, Mayer JS, Cooley RT, An Improved Control Strategy for a 50-kHz Auxiliary Resonant Commutated Pole Converter, IEEE PESC Conference Record, p1246-1252, 1997

[5.1] Divan DM, The Resonant DC Link Converter – A New Concept in Static Power Conversion, IEEE IAS Annual Meeting Conference Record, p648-656, 1986.

[5.2] Lai J-S, Bose BK, An Improved Resonant DC Link Inverter for Induction Motor Drives, IEEE IAS Annual Meeting Conference Record, p742-748, 1988.

[5.3] Divan DM, Skibinski G, Zero-Switching-Loss Inverters for High-Power Applications, IEEE Transaction on Industry Applications, Vol.25, No.4, p634-643, July/August 1989.

[5.4] Kondo S, Yang SH, Takizawa S, Harashima F, Resonant DC Link Dual Converter System for Motor Drives, IEEE IAS Annual Meeting Conference Record, p789-794, 1991.

[5.5] Mertens A, Design of a 20KVA Resonant Dc Link IGBT Inverter on the Base of Experimental Device Evaluation, EPE, Firenze, Vol.4, p172-177, 1991.

[5.6] Schülting L, A 100kVA Resonant DC Link Inverter with GTOs - Design Considerations and First Practical Experience -, IEEE IAS Annual Meeting Conference Record, p729-736, 1992.

[5.7] Skibinski GL, Divan DM, Design Integration of a 200kW GTO RDCL Converter, IEEE IAS Annual Meeting Conference Record, Vol.2, p1029-1040, 1993.

[5.8] Chen S, Lipo TA, A Passively Clamped Quasi Resonant DC Link Inverter, IEEE IAS Annual Meeting Conference Record, p841-848, 1994.

[5.9] He J, Mohan N, Parallel Resonant DC Link Circuit—A Novel Zero Switching Loss Topology with Minimum Voltage Stresses, IEEE Transaction on Power Electronics, Vol.6, No.4, p687-694, October 1991.

[5.10] He J, Mohan N, Wold B, Zero-Voltage-Switching PWM Inverter for High-Frequency DC-AC Power Conversion, IEEE IAS Annual Meeting Conference Record, Seattle, p1215-1221, October 1990.

[5.11] Krogemann M, Clare JC, Design and Analysis of a PWM Parallel Resonant DC-Link Inverter, EPE, Sevilla, Vol.2, p585-590, 1995.

[5.12] Wang K, Jiang Y, Dubovsky S, Hua G, Boroyevich D, Lee FC, Novel DC-Rail Soft-Switched Three-Phase Voltage-Source Inverters, IEEE IAS Annual Meeting Conference Record, p2610-2617, 1995.

[5.13] Cho JG, Kim HS, Cho GH, Novel Softswitching PWM Converter using a New Parallel Resonant DC-Link, PESC Conference Record, p241-247, 1991.

[5.14] De Doncker RW, Lyons JP, The Auxiliary Quasi-Resonant DC Link Inverter, IEEE PESC Conference Record, Cambridge MA, p248-253, June 1991.

[5.15] Malesani L, Tenti P, Tomasin P, Toigo V, High Efficiency Quasi-Resonant DC Link Three-Phase Power Inverter for Full-Range PWM, IEEE Transactions on Industry Applications, Vol.31, No. 1, p141-148, January/February 1995.

[5.16] Choi J-W, Sul S-K, Resonant Link Bidirectional Power Converter: Part I—Resonant Circuit, Transactions on Power Electronics, Vol.10, No.4, p479-484, July 1995.

[5.17] Venkataramanan G, Divan D, Pulse Width Modulation with Resonant DC Link Converters, IEEE IAS Annual Meeting Conference Record, Vol.2, p984-990, 1990.

[5.18] Malesani L, Tenti P, Divan DM, Tiogo V, A Synchronized Resonant DC Link Converter for Soft-Switched PWM, IEEE IAS Annual Meeting Conference Record, p1037-1044, 1989.

[5.19] Taniguchi K, Yoshikawa T, Hirachi K, Tomokuni Y, A Quasi-Resonant PWM Converter with High Quality Input Waveforms and High Efficiency, PESC Conference Record, Vol.2, p1131-1136, 1994.

[5.20] Sikorski A, Citko T, Quasi-Resonant Parallel Dc-Link Circuit for High-Frequency DC-AC Inverters, EPE, p174-177, 1993.

[5.21] Bornhardt KE, Novel Soft-Switched GTO-Inverter Circuits, IEEE IAS Conference Proceedings, p1222-1227, 1990.

[5.22] Hui SYR, Gogani E, Zhang J, Practical Evaluation of a Quasi-resonant Circuit for Soft-Switched Inverters with minimum voltage stress, Sevilla, Vol.2, p652-657, 1995. EPE,

[5.23] Salame S, Tadros Y, Novel Softswitching Quasi Resonant 3-Phase IGBT Inverter, EPE, p2.095-2.099, 1995.

[5.24] Chen S, Lipo TA, Soft-Switched Inverter for Electric Vehicle Drives, IEEE IAS Annual Meeting Conference Record, p586-591, 1995.

[5.25] Patterson OD, Divan DM, Pseudo-Resonant Full Bridge DC/DC Converter, IEEE PESC Conference Record, p424-430, 1987.

[5.26] Cheriti A, Al-Haddad K, Dessaint LA, Meynard TA, Mukhedkar D, A Rugged Soft Commutated PWM Inverter for AC Drives, IEEE PESC Conference Record, p656-666, 1990.

[5.27] Matsuo H, Iida K, Kurokawa F, Harada K, New Soft-Commutated PWM Inverter with AC Current Transformer, IEEE Proceeding of IECON, Vol.2, p1275-1280, 1993.

[5.28] Ferreira JA, van Ross A, van Wyk JD, A Generic Softswitching Converter Topology with a Parallel Nonlinear Network for High Power Application, IEEE PESC Conference Record, p298-304, 1990.

[5.29] Ferreira JA, van Ross A, van Wyk JD, A Hybrid Phase Arm Power Module with Non-Linear Resonant Tank, IEEE IAS Annual Meeting Conference Record, p1679-1685, 1990.

[5.30] Ferreira JA, Theron PC, van Wyk JD, van Ross A, Schoeman JJ, Matsemela K, The Nonlinear Resonant Inverter: A New Softswitching Topology, EPE, Firenze, Vol.4, p216-220,1991.

[5.31] Ferreira JA, Theron PC, van Wyk JD, Control of Nonlinear Resonant Pole Inverters, IEEE IAS Annual Meeting Conference Record, p834-839, 1991.

[5.32] Burgers KC, van Wyk JD, Case MJ, A High Performance Induction Motor Drive System based on a Non-Linear Resonant Pole Softswitching Inverter, IEEE IAS Annual Meeting Conference Record, p111-118, 1992.

[5.33] Chan CC, Chau KT, Yao J, Chan DTW, A Novel Soft-Switching Inverter using Resonant Inductor Freewheeling, Proceedings of PEDS, p215-221, 1997.

[5.34] DeDoncker RW, Lyons JP, The Auxiliary resonant Commutated pole Converter, IEEE IAS Annual Meeting Conference Record, p1228-1235, 1990.

[5.35] Lai JS, Robert W, Young RW, George W, McKeever JW, Peng FZ, A Delta-Configured Auxiliary Resonant Snubber Inverter, IEEE Trans. on Industry Applications, Vol.32, No.3, p518-525, May/June 1996.

[5.36] Lai JS Young RW, Ott GW, White CP, McKeever JW, Chen DS, A novel resonant Snubber inverter, Proceedings of IEEE Power Electronics Specialists Conference, p797-803, 1995.

[5.37] Gandhi SK, Semiconductor Power Devices, John Wiley and Sons Ltd., New York, 1977

[5.38] Petterteig A, Rogne T, IGBT Turn-off Losses - In Hardswitching and with a Capacitive Snubber, EPE, Firenze, Vol.0, p203-208, 1991.

[6.1] Petterteig A, Rogne T, IGBT Turn-off Losses - In Hardswitching and with a Capacitive Snubber, EPE, Firenze, Vol.0, p203-208, 1991.

[6.2] Eckel H-G, Sack L, Rascher K, FPGA Based Control of an ARCP-Inverter without Additional Sensors, EPE, Trondheim, Vol.4, p385-390.

[6.3] Dehmlow M, Vergleichende Betrachtung unterschiedlicher resonanter Umrichtertopologien, Dissertation, Technische Universität Berlin, April 1995.

[6.4] Protiwa F-F, Koß J, A 20kVA Auxiliary Resonant Commutated Pole Converter - Design and Practical Experiences -,EPE, Sevilla, Vol.2, p111-116, 1995.

[6.5] Beukes HJ, Enslin JHR, Speé R, Experimental Evaluation of AC/AC Converter Topologies in Utility Applications, PESC Conference Record, p517-522, 1995.

[6.6] Micrometals, INC (1995): „Power Conversion & Line Filter Applications“, Micrometal data book, Catalog 4, Issue H, June 1995.

[7.1] Eckel H-G, Sack L, Rascher K, FPGA Based Control of an ARCP-Inverter without Additional Sensors, EPE, Trondheim, Vol.4, p385-390.

[7.2] Mohan N, Undeland TM, Robbins WP, Power Electronics, Wiley, Second Edition, 1995.

[B.1] SEMIKRON International (1992): „Power Semiconductors 92/93“, SEMIKRON data book, No. 112189000, 1992.

[B.2] CT-Concept Technology Ltd Switzerland (1994): „Concept IHD 215/280/680“, CT data book, No. IHDDAT11, December 1994.

[B.3] MAXIM Integrated Products Ins. (1994): „MAXIM Integrated Products“, MAXIM data book, No. 19-0122 Rev.4, September 1994.

[B.4] Petterteig A, Rogne T, IGBT Turn-off Losses - In Hardswitching and with a Capacitive Snubber, EPE, Firenze, Vol.0, p203-208, 1991.

[B.5] Toshiba Co-operation (1992): „GTR Module (IGBT)“, Toshiba Semiconductor Group data book, No. 92-3CK, 1992.

[B.6] Micrometals, INC (1995): „Power Conversion & Line Filter Applications“, Micrometal data book, Catalogue 4, Issue H, June 1995.

[B.7] Texas Instrument Inc. (1994): „TMS320C3X User's Guide“, Texas Instrument data book, 2558539-9721 revision J, October 1994.

Publications by the Author

a) Pickert V, Johnson CM, An Assessment of Resonant Converters for Induction Motor Drives Applications up to 100kW, IEE PEVD Conference Publication, No. 429, p.214-220, September 1996

b) Pickert V, Johnson CM, Three-Phase Resonant Converters: An Overview, IEE Colloquium on „Update on new power electronic techniques“, London, Digest No: 1997/091, p2/1-2/6, 1997.

c) Pickert V, Johnson CM, DSP Controlled Auxiliary Resonant Commutated Pole Inverter without Switch Status Sensors, IEE PEVD Conference Publication, No: 456, p.650-655, September 1998

d) Pickert V, Johnson CM, Three Phase Soft Switching Voltage Source Converters for Motor Drives. Part 1: Overview and Analysis, forthcoming paper at IEE Proceedings, Electric Power Applications.

e) Johnson CM, Pickert V, Three Phase Soft Switching Voltage Source Converters for Motor Drives. Part 2: Fundamental Limitations and Critical Assessment, forthcoming paper at IEE Proceedings, Electric Power Applications.

f) V. Pickert, Comparison of modified Punch-Through and Non-Punch Through IGBTs for Soft Switching Topologies, digest at EPE 99