Battery Charging System Incorporating an Equalisation Circuit for Electric Vehicles

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A thesis submitted for the degree of Doctor of Philosophy

May, 2019

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Abstract

Hybrid electric vehicles (HEVs) and electric vehicles (EVs) are gaining in popularity mainly due to the fact that unlike combustion-powered vehicles, they do not pollute with greenhouse gases and toxic particles. Most HEVs and EVs are powered by lithium-ion battery packs which have high power density and longer cycle lives compared to other battery types. Each pack is made out of many battery cells in series connected and due to manufacturing tolerances and chemical processes in individual cells each cell has its own electric characteristics. In order to achieve a balanced voltage across all cells, a battery management system (BMS) must be employed to actively monitor and balance the cells voltage. On-board battery chargers are installed in HEVs/EVs to charge the lithium-ion battery pack from the grid. This charger converts AC grid voltage into a controllable DC output voltage, but it adds weight to the vehicle, reducing the overall efficiency of an HEV/EV and also increasing its cost.

The aim of researches in multi-functional power electronics is to design systems which perform several different functions at the same time. These systems promise cost and weight reductions since only one circuit is used to conduct different functions. An example is the electric drive in an HEV/EV. On one hand, it propels the car forward when driving, while on the other hand the battery can be charged via a modified electric motor and inverter topology. Thus, no additional on-board charger is required.

This thesis describes a new multi-functional circuit for HEVs/EVs which combines the functions of voltage equalisation with grid charging. Compared to a drive system, the proposed circuit does not rely on an electric motor to charge the battery. Various battery chargers and equalisation circuits are first compared. Then, the design of the proposed circuit is described and simulation results are presented for charging and voltage balancing. An experimental test rig was built and practical results have been captured and compared with simulation results for validation. The advantages and disadvantages of the proposed circuit are discussed at the end of the thesis.

Keywords- Multi-functional system, Battery charging, Voltage equalisation, Lithium-ion battery.

Acknowledgement

Working towards this point over the past four years has been an amazing experience for me. I've learned and gained more than I ever thought I could. Here I would like to say thanks to a few people without whom I would never made it here.

First and Foremost, I would like to express my deep thanks and sincere gratitude to my supervisors, Prof. Volker Pickert, and Dr. Simon Lambert. I am very grateful for their guidance and supports and encouragements to me about this work and more. Also, their expertise, patience, and enthusiasm have inspired me a lot in my future pursuits.

I had the good fortune to undertake my research in the UG lab with lovely people in EP group. I am grateful for all the supports I've received from academics and technical staff including electric and mechanical workshop teams.

I would like to express my appreciation to Dr. Haimeng Wu, Dr. Bing Ji for their valuable advice and assistance during my study. I am also grateful to Xiang Lu, Xu Deng, Boru Jia, Weichi Zhang, and all lovely friends and their families, for the company and all the wonderful memories in Newcastle.

My most profound thanks is to my parents, Xuedao Zhan and Huiping Li, for their full understanding and supports during my education in UK. Undertaking a PhD is a lot of work not only for me but also for them. The hard work and sacrifices of my parents made it possible for me to be here. For their great emotional and financial support, I am eternally grateful.

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Symbols

B	Battery cell
C	Capacitor
L	Inductor
Lm	Magnetic inductance
S	Switch
Np	Primary winding
Ns	Secondary winding
Bus	Bus in winding selector
Rcell	Resistance in battery model
V_{Lm}	Voltage across primary winding
V_{LS_1}	Voltage across top secondary winding
V_{LS_2}	Voltage across bottom secondary winding
i_{Lm}	Current in primary winding
I_{peak}	Peak current in primary winding
i_{LS}	Current in secondary winding
I_{LS_peak}	Peak current in secondary winding
T	Switching period
D	Duty cycle
Dc	Critical duty cycle
Vin	Input voltage
VBn	Cell voltage
Llk	Leakage inductance

C_{oss}	Output capacitance of S1
V_{DS}	Rated voltage of S1
V_{ds}	Voltage across S1
C_{sn}	Snubber capacitor
R_{sn}	Snubber resistor
D_{sn}	Snubber diode
id	Current through S1
isn	Current through Dsn
iD	Current through secondary winding
V_{sn}	Clamped voltage of snubber circuit
P_{sn}	Power dissipated in snubber circuit
ΔV_{sn}	Voltage ripple in V_{sn}
V_{ds_clamp}	Clamped voltage across S1
$P_{dead-time}$	Power loss in dead-time
ɧ	Circuit efficiency
φ	Phase angle between input voltage and current
$\cos\varphi$	Phase factor in PF
$\cos\theta$	Distortion factor in PF
K_v	Gain of input voltage
K_i	Gain of input current
K_p	Gain of proportional
K_I	Gain of integral
V_{ref}	Reference voltage

Abbreviations

AC	Alternating current
ADC	Analogue to digital converter
BMS	Battery management system
CC	Constant current
CCS	Code composer studio
CCS/Combo	Combined charging system
CC-CV	Constant-current-constant-voltage
CO_2	Carbon dioxide
CTC	Constant trickle current
CV	Constant voltage
DC	Direct current
DCM	Discontinuous conduction mode
DSC	Digital signal controller
DSP	Digital signal processor
EPRI	Electric Power Research Institute
ePWM	Enhanced pulse width modulator
ETM	Energy transmission medium
EV	Electric vehicle
EVSE	Electric vehicle supply equipment
FFT	Fast Fourier transform
GPIO	General purpose input and output
HEV	Hybrid electric vehicle
ICE	Internal combustion engine

IEEE	Institute of Electrical and Electronics Engineers
ISR	Interrupt service routine
IMF	Induced Magnetomotive Force
MMF	Magnetomotive force
MOSFET	Metal oxide surface field effect transistor
PF	Power factor
PFC	Power factor correction
PI	Proportional-integral
PSU	Power supply unit
PWM	Pulse width modulation
RCD	Resistor-capacitor-diode
SAE	Society of Automotive Engineers
SOC	State of charge
SPDT	Single-pole-double-throw
THD	Total harmonic distortion
V2G	Vehicle-to-grid
1P5S	One-primary-five-secondary

Chapter I Introduction

1.1 Background

Global warming due to the greenhouse effect has received more and more attention in recent years. Emissions of greenhouse gases, of which about eighty per cent is carbon dioxide (CO_2), are the leading cause of the greenhouse effect [1]. In the UK, CO_2 emissions from the transport sector accounted for 32 per cent of all carbon dioxide emissions in 2016, which is a 0.9 per cent increased from 2015 [2].

Compared to conventional oil-fuelled vehicles with internal combustion engines (ICEs), hybrid electric vehicles (HEVs) and electric vehicles (EVs) have the potential to reduce CO_2 emissions [3-5].

There are several potential components which have been used as energy source for HEVs/EVs, such as the lithium-ion battery, fuel cell and supercapacitor. As a traditional energy storage component, lithium-ion batteries have been used as energy sources for portable devices such as mobile phones and laptops for a long time. Compared to novel components such as supercapacitors, lithium-ion batteries have the main advantages of high energy density, good high-temperature performance and good safety performance [6-10]. They also benefit from their advanced recharge cycle and relatively low manufacturing cost. Supercapacitors may have considerably higher power density and charging/discharging speeds than lithium-ion batteries; however, their energy density is still low and their cost is high [6, 11, 12]. Fuel cells generate electricity from hydrogen applied to the anode and the air applied to the cathode. The advantages of fuel cells include high conversion efficiency, quiet operation, and very low emissions [6, 13]. However, fuel cells have some major issues including high price and on-board hydrogen storage which needs improved energy density and safety [14]. Above all, owing to their power and energy density and good cycle behaviour, lithium-ion batteries are chosen by most EV and HEV manufacturers. As the penetration of Li-ion powered vehicles across the world increases the scale of production, thus means that lithium-ion batteries will benefit from the maturity of production technology and higher volumes resulting in lower manufacturing costs [15, 16].

1.2 Battery systems in EVs

The voltage level for a single Lithium-ion battery cell is quite limited. For example, the nominal voltage of a Lithium-ion 19850 cell which is used by Tesla is only 3.8V. In most HEV/EV battery systems, the standard battery pack voltage is about 300V to 600V or higher [17, 18]. There is therefore a requirement for a large number of cells to be connected in series to form a battery pack with an adequate nominal voltage. With significant numbers of battery cells installed in a vehicle, a delicate charging system and battery management system (BMS) are required to guarantee the safety of both the vehicle and the passengers.

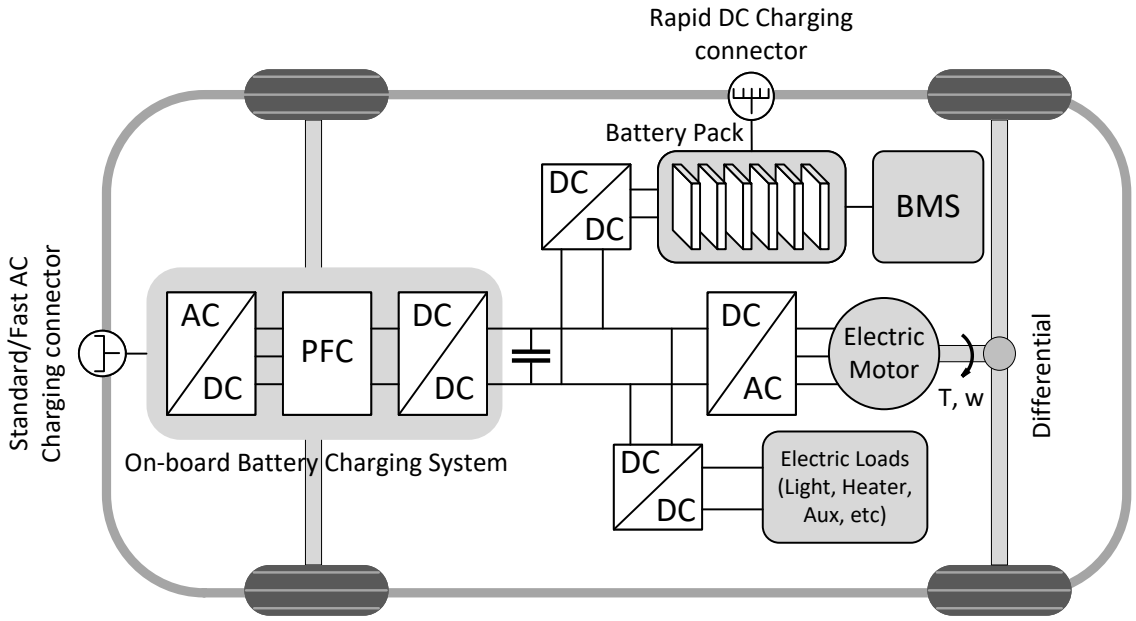


Figure 1- 1 – Diagram of a typical battery system in an EV.

Figure 1-1 illustrates a typical battery system in an EV, including battery charging and battery management [19-22]. EV chargers provide a DC charging voltage from an AC source, whether from a common socket outlet or from a purpose-built DC charging station. Therefore, blocks including AC/DC conversion and power conditioning control are needed to convert AC power to DC power, and a DC/DC converter is required to regulate the DC power to a suitable voltage for battery charging. Another DC/AC converter is involved in converting the DC power to AC again to drive the electric motor, and it is usually a bi-directional converter to allow energy flow from the motor to the battery during braking.

Three different charging power levels have been defined: Level 1 (standard) charging, Level 2 (fast) charging, and Level 3 (rapid) charging. Level 1 and Level 2 chargers can

deliver power up to 3kW and 22kW respectively, and both take AC power from the grid to charge the battery through an on-board charging system. Meanwhile Level 3 chargers supply very high power up to 120kW to achieve shorter charging times. With the very high power level, the charging circuit becomes very large and very expensive, and requiring heavy duty components. Hence, for Level 3 chargers, the functions of AC/DC conversion and power conditioning control take place in charging stations, fulfilled by off-board chargers.

The BMS is another system which is tightly integrated with the battery in an EV. It is responsible for monitoring the battery's operating conditions of voltage, current and temperature and controlling the charging/discharging rate to prolong battery life and guarantee its safety [23]. A typical BMS contains several different circuits to achieve the above functions, including measurement circuitry, a state of charge (SOC) calculator, equalisation circuits, and the thermal management circuits [23-25].

1.3 Voltage equalisation circuits

As a part of the BMS, the voltage equalisation circuit is a key element in maintaining the battery voltage within the normal range. Due to manufacturing tolerances and changes in battery chemistry due to ageing effects, each cell is unique in its electric performance. Therefore the charging and discharging profiles of all battery cells are not the same. When the series-connected cells are charged or discharged by the same current, each cell produces a different cell voltage across the stack due to their unique individual cell impedances. This is often termed an unbalanced state. The continued charging of mismatched cells in a pack can lead to the over-charging or over-discharging of cells, reducing the power-to-volume ratio of the battery system and, in the worst case, placing the whole system at risk of a catastrophic fault. Figure 1-2 shows a damaged lithium-ion battery and a damaged EV caused by a failure of a lithium-ion battery. Therefore, a method for voltage equalisation is necessary to guarantee safety and improve efficiency.

(a) (b)

Figure 1- 2 – Photographs of: (a) a damaged lithium-ion battery; (b) a damaged EV caused by battery failure.

A number of different circuits have been proposed in the literature to accomplish voltage equalisation [2-9] [26-31]. Based on different methods to deal with the management of energy in a battery pack, balancing circuits can be divided into two categories: dissipative and non-dissipative methods. In dissipative equalisation circuits, an energy absorbing unit such as a resistive load is switched into a parallel connection with the cell controlled by a micro-processor. This has the effect of discharging the cell's energy into the load and dissipating it as heat. This equalisation method has been widely used in low-power systems, due to the simple circuit structure and circuit control and its low cost. However, these circuits obviously exhibit low efficiency, since the energy extorted from higher voltage cells is wasted. Besides this, when the cell's stored energy is transformed into heat, the temperature in the battery pack must be carefully managed to avoid significant increases in temperature which could also lead to safety issues with the pack. Non-dissipative equalisation circuits have better performance in terms of energy efficiency. With the employment of an energy transfer medium such as converters and transformers, the energy in cells within a pack can be rearranged with less waste. Plenty of non-dissipative equalisation circuits have been proposed, and each circuit has its own advantages and drawbacks. Therefore, the choice of the equalisation circuit is often driven by the cost and specifications of applications.

1.4 Previous work on multi-functional design in EVs

Any non-dissipative equalisation circuit adds cost compared to a dissipative circuit. In order to attempt to reduce costs the concept of multi-functional design is explored in this thesis. The idea is that the power electronics associated with voltage balancing

could be modified in such a way as to be not only used for balancing the cell voltage but also for charging each cell directly from the grid. This way, the BMS will replace the AC/DC battery charger of an EV as shown in Figure 1-1. Thus a complete sub-system can be eliminated, reducing the weight and cost of an EV.

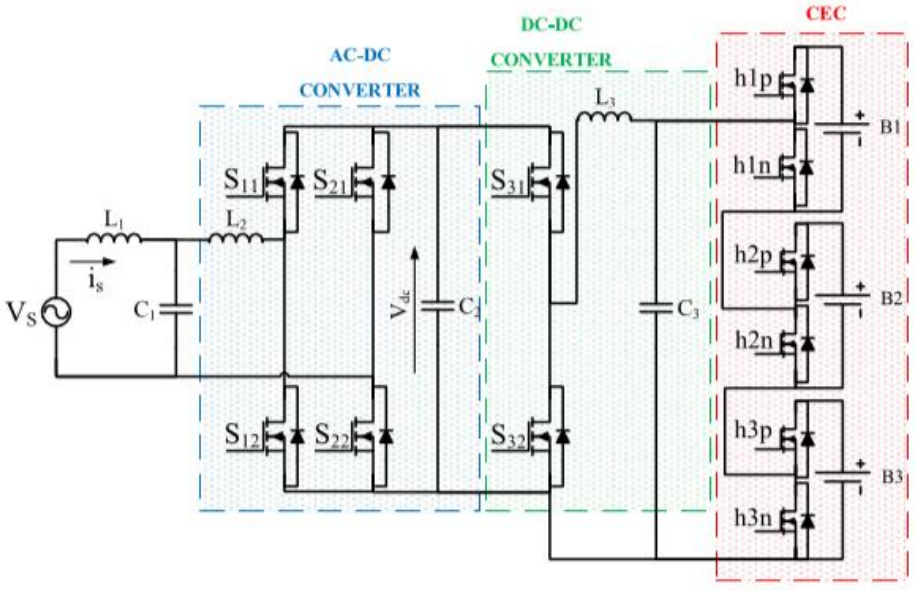


Figure 1- 3 – Bidirectional charger topology [26].

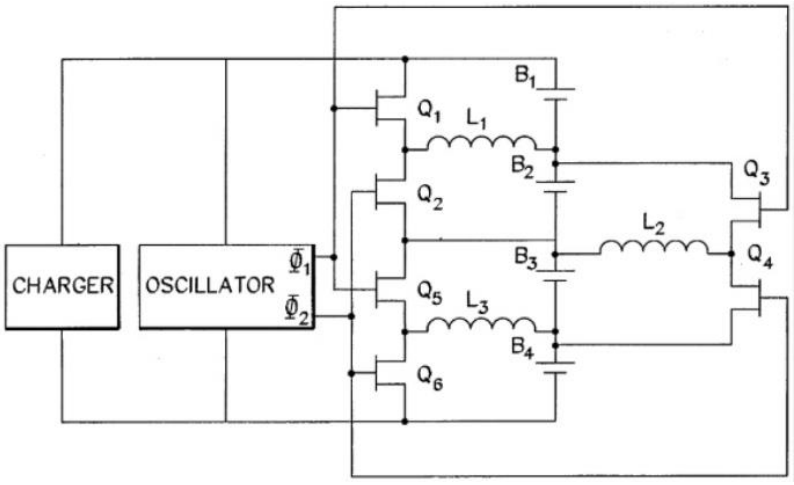


Figure 1- 4 – Non-dissipative battery charger equalizer topology [28].

A few attempts have been proposed to combine an additional function with the BMS. [32, 33] suggested a bi-directional battery charger with a modular integrated equalisation circuit in which the battery cells are connected to the grid via a full-bridge rectifier, a DC/DC converter and a group of switches. The circuit charges the cells by selecting those which have lower voltage and stops the charging of those which have reached the maximum cell voltage. Thus, rather than charging all cells with one current, each cell is charged individually from the grid. The proposed circuit is, however, only

able to balance the cell voltages when connected to the grid. Once the BMS is unplugged, the circuit is unable to achieve a balanced voltage across the cells. Another study proposes a battery charger that includes a voltage source and a non-dissipative shunt arrangement that can be customised to charge any number of batteries [34]. This non-dissipative shunt circuit includes a pair of transistors and an inductor for each pair of batteries, and they are connected as a buck-boost converter. Therefore, the circuit can be used to charge the battery as an EV charger when it is connected to the grid; meanwhile, it is capable of balancing cell voltages through the shunted buck-boost converters when the circuit is unplugged. However, the components involved in the proposed circuit are exactly the same as those when the charging circuit and the equalisation circuit are separate. In other words, this circuit does not achieve the aim of reducing the number of devices in the system.

1.5 Objectives

In a conventional EV, the battery charging and equalisation circuits are separate. Most chargers provide a charging voltage up to 600V, and components include the rectifier, power factor correction (PFC) circuit and isolated DC/DC. All of these components need to be designed to withstand this high voltage, which makes the battery charger bulky and costly. In order to achieve balanced voltage among a large number of battery cells, the size of the required equalisation circuit increases with the number of cells, as does the cost. Therefore, designing one circuit that combines both functions of charging and equalisation would save on number of components, weight and cost, which are important targets in the automotive industry.

The work in this thesis focuses on the design of a Level 1 battery charger incorporating a battery cell equalisation circuit for EVs. It aims to accomplish all of the functions of both battery charging and voltage equalisation using fewer devices. When the vehicle is static and connected to the grid, the proposed circuit is able to charge the traction battery just like conventional chargers do. When the vehicle is not connected to the grid, or is even on the road, the circuit operates like a conventional voltage equaliser. The design of such a circuit must therefore provide AC/DC conversion, grid power conditioning, isolation between the grid and the battery, and voltage equalisation.

To add a charging circuit to the voltage balancing circuit, the transformer-based balancing circuits are preferred, since the transformer structure can also provide the

isolation. The transformer-based balancing circuits can be divided into two types, one is based on flyback converter topology, while the other one is based on forward converter topology. Comparing these two types, the flyback converter topology has advantages such as smaller size and easier control. Besides, the flyback converter is more suitable for circuits with multiple outputs. However, the power of flyback converters are limited. The power level of a flyback converter is up to 200W, and it normally be used in low-power applications. As to the structure of the transformer, since in flyback converters, in order to prevent magnetic saturation, the core of the transformer needs to add an air-gap. It will increase the leakage inductance, reduce the circuit efficiency, and put more stress on the switching device. Besides, since the output voltage and current are pulsed, flyback converters are suitable for applications which highly require constant outputs.

1.6 Contribution to knowledge

The main original contributions of this research work are as follows:

- A detailed overview of published equalisation schemes is presented in this thesis, and a unique method is also firstly suggested for categorising these schemes to families based on different aspects including constituent components and energy transfer path, mode and sequence.
- An EV battery charger integrated with a multi-secondary windings transformer equalisation circuit is proposed in this thesis. The circuit has two standalone operational modes of grid charging or voltage balancing, which are alternated between using a pair of single-pole-double-throw (SPDT) switches.
- A multi-functional power electronic power converter is proposed for the first time which combines the full functions of grid battery charging with the full functions of battery equalisation with only one transformer in the circuit. Beside this, the proposed circuit is capable of achieving balanced voltage by selecting lower voltage cells during the charging process.
- A control strategy that includes PFC control and CC-CV charging control has been developed in this work. The control strategy demonstrates fast charging without compromising the PF when CC-CV charging is applied.

Some relevant outcomes from the research have been published in the following papers:

[1]. S. M. Lambert, V. Pickert, D. J. Atkinson and H. Zhan, "Transformer-Based Equalization Circuit Applied to n-Number of High Capacitance Cells," in *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1334-1343, Feb. 2016.

The author of this thesis made contribution in this article mainly focusing on the introduction part, where the commonly used equalisation circuit been summarised, and their advantages and disadvantages been discussed. Besides, a part of the proposed circuit in this thesis is learned from the circuit in this article.

[2]. Huaxia Zhan, Xin Xiang, S. M. Lambert, V. Pickert, Haimeng Wu and Xiang Lu, "A cascaded transformer-based equalisation converter for series connected battery cells," *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, 2016, pp. 1-6.

The author of this thesis participated in the whole process of the work, including design, modelling and simulation of the circuit, and the writing up of the paper. Even though that this equalisation circuit is not utilised as a part of the circuit in this thesis in the final, the research process became a valuable experience for the author to have a deeper understanding of both the battery voltage equalisation and the flyback converter.

1.7 Thesis overview

This thesis is divided into six chapters. Chapter I introduces the background of the project, including battery charging and battery voltage equalisation in EVs. The motivation and objectives of the study, and especially the design of a multi-functional battery system for an EV, as well as its contributions to knowledge.

In Chapter II a detailed overview is presented of both the battery charging system and the voltage equalisation circuit. It starts with the constant-current-constant-voltage (CC-CV) charging strategy for the lithium-ion battery. Then, EV chargers are introduced in terms of charging power levels with corresponding charging infrastructures, and different charging circuit schemes. This is followed by a thorough study of voltage equalisation circuits, including the factors which cause unbalanced voltage levels and the necessity for equalisation circuits for battery packs, and descriptions of existing equalisation schemes along with a summary of their advantages and limitations.

Chapter III presents the development of the proposed battery charging system incorporating an equalisation circuit. Each block of the circuit is described separately, including its design and function. There are five operational modes for the proposed circuit, two for battery charging from the grid, and three for voltage equalisation. The five operational modes are studied successively, where each mode is explained using an example of a possible combination of cells. This chapter also introduces the simulation model for the proposed circuit, and the simulation results obtained when the circuit operates under different modes with open-loop control.

A closed-loop controller for the proposed circuit is described in Chapter IV. The controller is capable of both PFC and CC-CV charging. This controller actually consists of two controllers, a PFC and CC controller and a PFC and CV controller. The choice of controller depends on the cell voltages in the pack. Simulation results are presented when the circuit operates with the two controllers.

Chapter V describes the experimental testing of the circuit. It starts with the design and implementation of the test system, including hardware and software implementation. Then, experimental results for the circuit operating as a battery charger and a voltage equaliser are presented. The experimental results are compared with the simulation results, and they prove that the proposed circuit is capable of either charging the battery or achieving balanced voltage within a battery pack.

Chapter VI summarizes the research work that was carried out in the project and discusses the advantages and disadvantages of the proposed battery charging system integrated with an equalisation circuit. The chapter ends with recommendations for future work to enhance the proposed technique.

Chapter II Charging and Equalisation for Lithium-ion Batteries

This chapter introduces background information concerning the development of a converter which achieves the aim of the project. Firstly, different charging strategies for lithium-ion batteries are explained. Then, battery charging systems which are currently used in EVs are described, including details of charging power levels and charging structures. Finally, an overview of existing battery equalisation circuits is presented covering their structure and operation, and a comparison based on the available literature.

2.1 Charging strategies for lithium-ion batteries

In order to provide optimal charging in terms of efficiency and charging time, various battery charging strategies have been developed, such as constant trickle current (CTC) charging, constant current (CC) charging, constant voltage (CV) charging, and constant current and constant voltage (CC-CV) charging, as discussed in [35-41].

CTC charging provides the battery with a very low but constant current. Therefore, the charging process can be very stable but extremely slow. The long charging time is the biggest disadvantage of this method. However, when a battery is charged from a very low initial voltage, for example under the pre-charge voltage threshold, the battery should be CTC charged for safety and reliability reasons until its voltage has risen to the pre-charge threshold value. Above the threshold, other charging strategies can be applied.

CC charges the battery with a constant current at levels well above those in CTC. CC allows a battery to be charged at high speed. One drawback of this method is that the battery can be easily overcharged due to the high charging current.

The CV charge strategy charges the battery with a constant voltage. Since the current is determined by the voltage difference between the battery and the charging source, the charging current level is driven by Ohm’s Law, and thus a higher current is applied to the battery at the beginning when the cell voltage is still low. Then the charging current declines slowly as the cell voltage increases. In the later stage of charging, the

charging speed becomes dramatically slower until the voltage difference is not sufficient to drive any further charging current.

Charging based on the CC-CV strategy is a combination of the previous three charging methods. CC-CV aims to charge battery cells in a more efficient way and to guarantee safety at the same time. The principal charging process of the CC-CV method is shown in Figure 2-1.

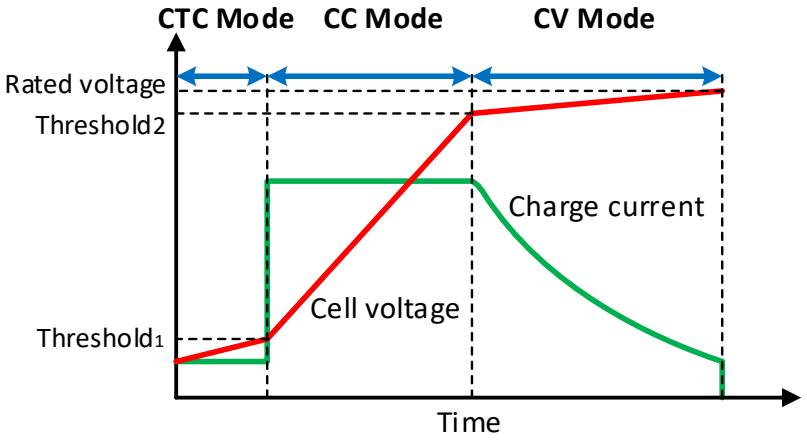


Figure 2- 1 – CC-CV charging method for battery cells.

At the beginning, the battery cell is charged in CTC mode by a small current when the cell voltage is under Threshold 1. After that, the charging process moves to CC mode during which the current is large enough to charge the battery at a higher speed and the cell voltage increases quickly. Once the cell voltage reaches Threshold 2, the charging switches to CV mode and thus the charging current starts to fall, as does the charging speed. The whole charging process ends when the cell voltage has reached its maximum value, which is normally defined by the manufacturer.

2.2 EV Battery chargers

An EV battery charger is in principle a rectifier circuit that converts AC voltage to DC voltage. The DC level is controlled and adapted to the voltage of the battery pack in an EV. According to the charging method, battery chargers can be categorised as using conductive and inductive charging. Conductive chargers have hard-wire contacts between the power supply and the vehicle, while inductive chargers use a varying magnetic field to transfer energy to the battery without any physical contact. A detailed comparative study of these methods has previously been published [42]. Inductive chargers provide galvanic isolation between electric vehicles and the power supply,

which makes the method safe for high power applications (in excess of 50kW). It also makes it possible for vehicles to be charged during motion by building charging strips into highways. However, the efficiency of magnetic energy transfer in inductive chargers is relatively low due to the loose coupling of coils; besides, the infrastructure costs of inductive chargers are much higher compared to conductive chargers [43]. Hence, in this project, conductive chargers have been taken into consideration and are introduced in the next section.

2.2.1 Charger power levels and infrastructure

The power level of a charger indicates its power, location, charging speed and infrastructure cost. According to the charging rate, conductive EV chargers can be classified into three categories, depending on the charging power level [44]. The categories are classified as Levels 1 to 3 and each level has its own electric vehicle supply equipment (EVSE).

EVSE is installed for the purpose of delivering energy from the grid to an EV, and consists of a residential or commercial charging stand, an attachment plug, a power outlet, a vehicle connector and some protection circuits [44]. Configurations of EVSEs vary depending on the power level, voltage, and frequency.

a) Level 1 Charging (Standard AC Charging)

The Level 1 category represent slow charger units found in both residential and commercial buildings with charging power up to 3kW. For this power level, EVs can receive power from a domestic single-phase socket outlet. Common EV plugs for Level 1 connected to power sockets are the three-pin NEMA 5-15P (US) or the three-pin BS1363 (UK), which are the same plugs as used on domestic appliances such as televisions and laptops. The other end of the EV cable connected to the vehicle possesses a connector which is either a five-pin SAE J1772 plug or a seven-pin IEC 62196 plug [45], as shown in Figure 2-2.

Level 1 charging requires approximately 6 hours to fully charge an EV such as the Nissan Leaf, for example, depending on the battery type and energy. Times between 6 to 8 hours are acceptable for EVs charged at home overnight, or in a car park during working hours. A Level 1 charger minimises the need to update the current power supply devices. The infrastructure cost per a residential Level 1 charger has been

estimated at approximately $800 in the US [46], including labour, material and permit costs.

b) Level 2 Charging (Fast AC Charging)

Level 2 charging is the primary charging method for both private and public facilities and provides charging power up to 22kW. It employs dedicated equipment and connections for a charging unit to provide higher levels of safety. A residential fast charger is typically mounted on a garage wall, with a tethered J1722 plug or IEC 62196 plug [45], whichever is compatible with the vehicle. Meanwhile some standing fast charging points can be found at workplaces or on-street locations which possess seven-pin socket outlets.

Fast charging will take approximately two to six hours to fully charge a vehicle. According to the Electric Power Research Institute (EPRI), most EV owners prefer to charge at home overnight, and therefore, Levels 1 and 2 chargers are the primary options. However, despite their higher infrastructure costs, Level 2 chargers are more popular in public sites due to their faster charging and standardized vehicle-to-charger connections [18]. The installation fee for a residential Level 2 charger is reported to be approximately $2,000 and about $1,800 for a commercial facility charger.

c) Level 3 Charging (Rapid DC Charging)

Level 3 charging is for commercial and public applications which can be installed in highway stations and refuelling points similar to commercial petrol stations. The charging unit requires dedicated equipment to operate with a three-phase circuit at 480V or higher, and the power output is normally up to 50kW (the Tesla supercharger has a maximum power output of 120kW [47].) Level 3 chargers contain an off-board charger to provide regulated AC-DC conversion. Therefore, the connection to the vehicle is direct DC. Level 3 charger units are typically equipped with tethered CHAdeMO plugs to connect to EVs with the corresponding socket [45]. However, certain EVs possess the Combined Charging System (CCS or Combo) socket which is compatible with either the tethered rapid DC charger plug or the tethered fast AC charger plug [44, 46].

A Level 3 charger can fully charge an EV within an hour due to its significantly higher power output. The high power output and infrastructure costs mean that Level 3 chargers are rarely feasible for private use. It is reported that the infrastructure costs

for a Level 3 charger are between $30,000 and $160,000, with extra costs for maintaining the charging station [44].

Figure 2-2 illustrates the charging equipment for all three levels of chargers, including the cords, plugs, and sockets mentioned above.

Figure 2- 2 – Electric vehicle supply equipment (EVSE) for three levels of chargers.

2.2.2 Power flow in EV chargers

There are two types of power flow in EV chargers: unidirectional and bidirectional power flow. In a unidirectional charger, energy can only flow from the grid to the vehicle, but cannot be injected back from the battery to the grid. These chargers typically use a diode bridge rectifier in conjunction with an input filter and a power factor correction circuit. EVs with bidirectional chargers can not only charge battery cells but also inject energy from the battery pack into the grid, which is referred to as the vehicle-to-grid (V2G) operation mode [48-52]. A typical bidirectional EV charger has two stages: an active bidirectional AC-DC converter connected to the grid which controls input power factor, followed by a bidirectional DC-DC converter to regulate the output voltage and current. While many studies have focused on bidirectional power chargers, their successful implementation requires extensive safety measures and more complicated controllers, since the power flowing in both directions need power factor corrections, and also the same phase angle is needed when injecting power into the grid [18, 44, 48, 52]. So far, all commercially available Level 1, 2 and 3 chargers are unidirectional. It is expected that only Level 2 chargers will become bidirectional, since the cost-

benefit ratio of a bidirectional Level 1 charger is too large and rapid charging (Level 3) only makes sense if the user wants to charge an EV battery as quickly as possible rather than extending the charging time by transferring energy back into the grid.

2.2.3 Structure of EV charging system

EV battery chargers can also be categorized as on-board or off-board chargers [18]. For Level 1 and Level 2 charging, since the power rating is limited, the system can be designed to be small and light enough to be installed on vehicles as on-board chargers. Meanwhile off-board chargers are less constrained by weight and space, and therefore Level 3 chargers are typically designed to be off-board [46].

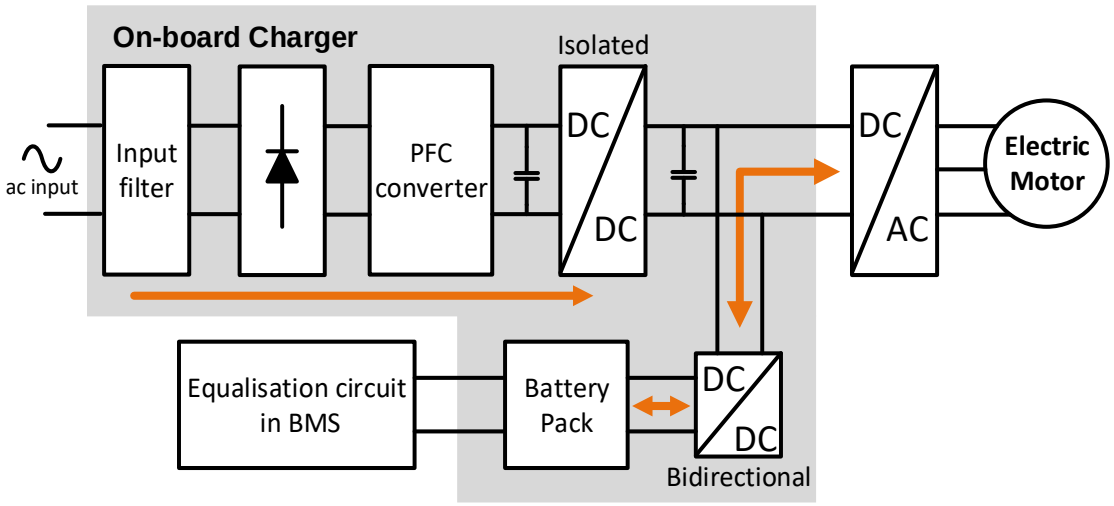


Figure 2- 3 – Block diagram of a typical EV battery charging system (Level 1 and 2).

Figure 2-3 presents a block diagram of a typical EV charging system for Level 1 and Level 2 charging [44]. The on-board charger mainly consists of an input filter, a rectifier, a PFC converter and an isolated DC-DC converter. The circuit is shown in detail in Figure 2-4. The input filter is to block interference signals from the grid to the system, which is necessary for most electric equipment connected to the grid. The rectifier converts AC input to DC, which is then regulated by the PFC converter which is responsible for achieving a good power factor. The isolated DC-DC converter provides galvanic isolation and control of the charging power. Isolation is required as the vehicle chassis ground and neutral of the grid should be kept separate.

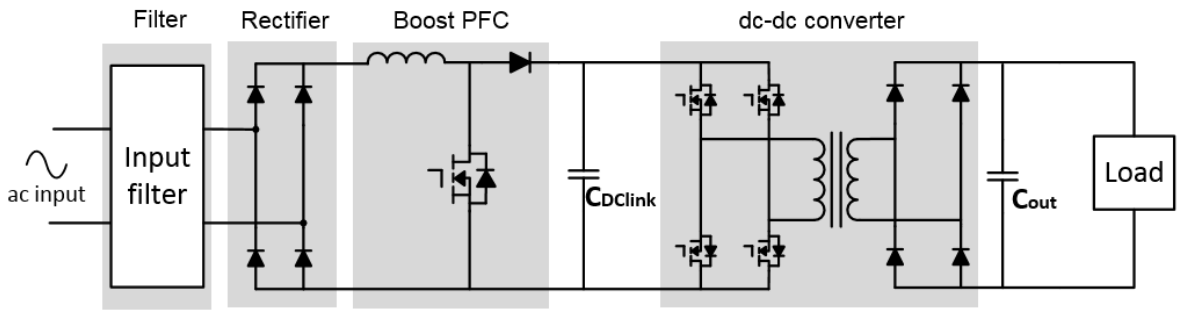


Figure 2- 4 – Typical Levels 1 and 2 charging circuit for an on-board EV charger.

2.2.4 Power factor correction (PFC) converters

According to IEEE and SAE standards, in EV chargers it must be ensured that the current is drawn with low distortion to minimize any impact of power quality, and with a high power factor to maximize the real power [44]. Thus, in order to improve the power factor in battery charging circuits, PFC circuits are embedded in most EV chargers. Although PFC can be implemented using different topologies, such as buck, buck-boost or Cuk converters, the boost converter is most commonly used in the PFC topologies employed in EV charging [53].

For applications such as EV battery chargers which require an isolated output along with input PFC, a two-stage conversion process typically includes a boost PFC followed by an isolated DC/DC converter, as depicted in Figure 2-5. Operation of the boost PFC converter helps to eliminate the distortion in the input current by compensating for the input voltage when it is lower than the voltage of capacitor C_B.

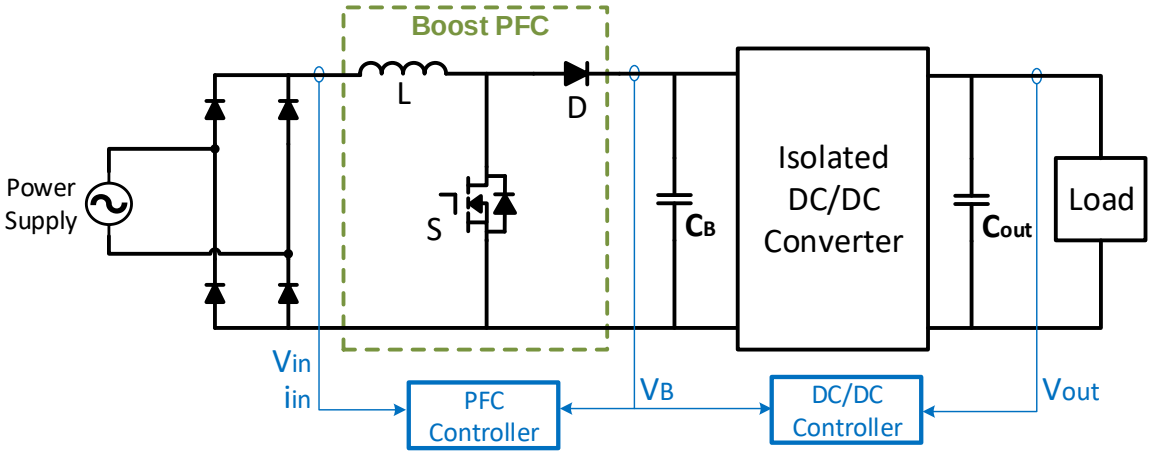


Figure 2- 5 – Typical two-stage boost PFC converter.

The two-stage PFC performs well in terms of achieving a high input power factor and low-frequency ripple in the output voltage, and therefore it suits many applications

beyond EV charging. However, the two-stage structure has low power density, and the overall efficiency of the two-stage topology is also low since power has to flow through two cascaded stages and each stage has to be designed at full output power, which means that the size and cost of the system increase [54]. In addition, each stage has its own controller, which makes the overall control of the charging more complicated.

By applying new circuit topologies which allow the merger of the PFC converter and the isolated DC/DC converter into one single conversion system, isolated single-stage PFC converters can be developed. In principle, these converters provide better efficiency and power density. The principles of this circuit are shown in Figure 2-6.

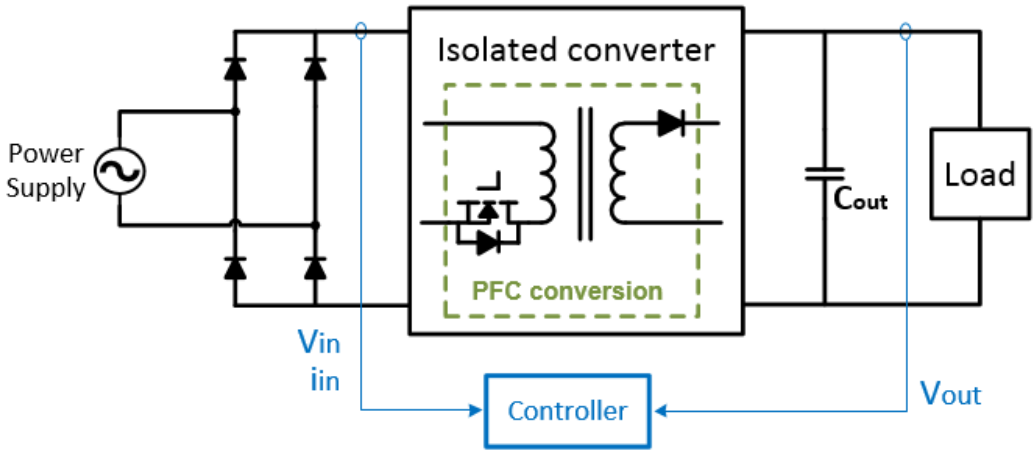


Figure 2- 6 – Principles of an isolated single-stage PFC converter.

Isolated single-stage PFC converters utilise auxiliary magnetic components and power switches to achieve PF correction. Extra power switches have been employed, but this increases the cost and control complexity of the circuit [55]. Other circuits have been developed with one forward converter to deliver the main output to the load, and another auxiliary flyback converter which regulates the output voltage and current [56, 57]. Single-stage PFC circuits with a flyback topology have also been proposed [54, 58, 59] in which extra devices such as inductors and transformer windings are needed as well.

2.3 Voltage equalisation for battery packs

Typically, the terminal voltage and energy capacity of a single lithium-ion battery cell are limited to about 4.2V and 3600mAh respectively [60]. Therefore, multiple cells are connected in series and parallel in EV traction batteries to meet the voltage and energy demands. In an EV battery system, the required bus voltage is in the range of 300-

600V, and the stored energy in the battery system determines the maximum endurance of the vehicle, where typical values are between 24kW to 66kW [17]. Hence, hundreds of batteries are usually assembled into one battery pack.

2.3.1 Unbalanced cells voltage

When a number of batteries are connected in series, they are charged and discharged at the same current rate. Ideally, the terminal voltage of each cell should be the same if they received the same initial voltage and charging/discharging speed. However, due to limitations in manufacturing technology, every single cell is unique. This means that in a battery pack, the internal characteristics of each cell are always slightly different from others even if they are produced in the same batch. Furthermore, cycling, elevated temperature and ageing decrease the performance of the battery cell over time.

The performance of a lithium-ion battery depends on ion movement between the positive and negative electrodes [61]. The ageing process begins at the moment the cell was produced, and results in declining cell capacity and increasing cell internal resistance [62, 63]. Figure 2-7 shows the degradation curve of a lithium-ion battery. Over 4500 cycles, the remaining capacity of the battery cell decreases from 100% to less than 80%.

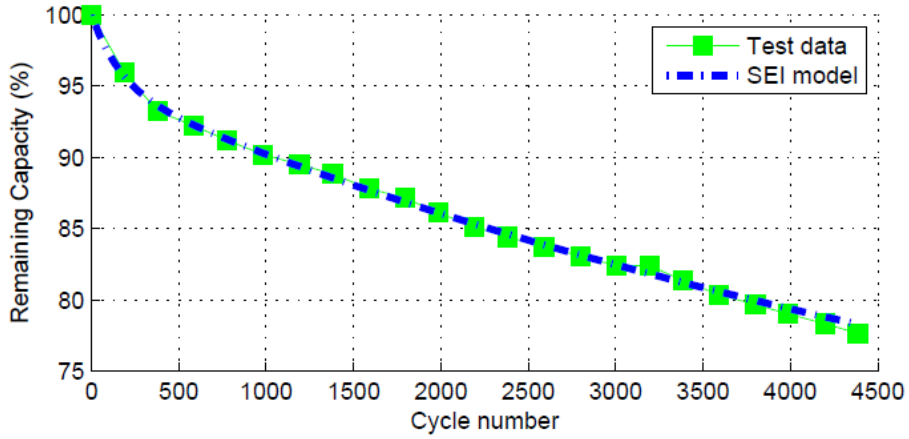
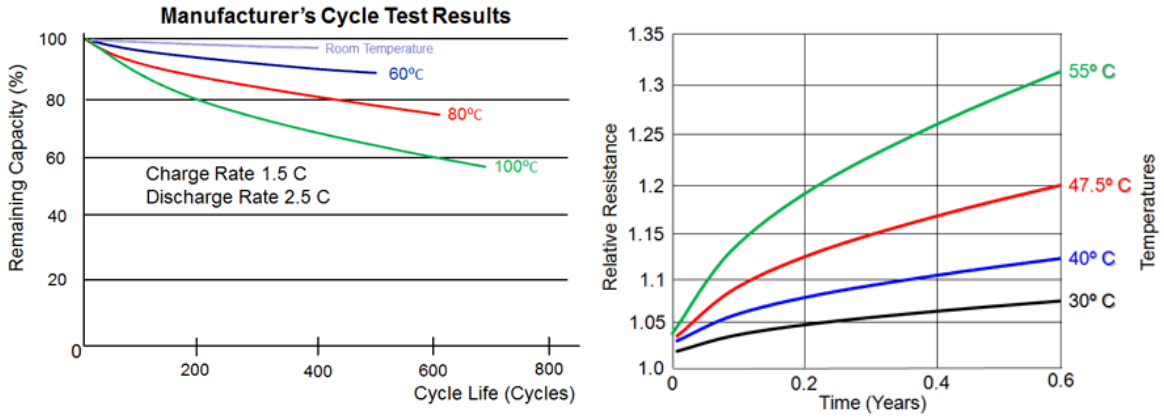


Figure 2- 7 – An example of degradation curve for a Lithium-ion battery (3.2V,1100mAh) [16].



(a) (b)

Figure 2- 8 – (a) Decreasing capacity with cycles and temperature; (b) increasing internal resistance with time and temperature [64].

Most batteries perform best at room temperature [61]. Figure 2-8 shows the changes of the remaining capacity and relative resistance of a lithium-ion battery over cycles or time under different testing temperature. It indicates that the high operation temperature will speeds up the degradation of a battery, causing the decreasing of the capacity, and the increasing of the internal resistance.

2.3.2 Necessity of equalisation circuits for battery packs

Due to the fact that each battery cell has its own unique characteristics as highlighted in section 2.3.1, each cell in a battery pack has a unique cell voltage. This unbalanced voltage causes two problems. Firstly, when the battery stack is being charged, the charging process stops once one cell has reached its maximum voltage level. This means that the battery stack carries less energy, since other cells with lower cell voltages have not been fully charged. Secondly, if a cell reaches a critical low voltage level that requires it to stop operating for safety reasons, the whole stack must halt its operation even though all other cells have higher cell voltages. Otherwise, there would be cells which over-charge or over-discharge in the stack. Repeatedly over-charging or over-discharging are extremely harmful to lithium-ion cells, as any damage is irreversible and will dramatically accelerate the ageing process of cells and can lead to their breakdown.

Furthermore, over-charging and over-discharging are not only dangerous to the cell but also to the battery pack. This is because the cell can short-circuit, which then causes a series of reactions via an avalanche effect in the battery pack, resulting in the failure of the whole system.

To avoid this situation, it should be ensured the voltage across every single lithium-ion battery is equal. The aim of equalisation circuits is to keep the voltage balanced across each cell in a battery pack. This can be accomplished in two ways. Either energy stored in the cell is bled into a resistor until the cell voltage reaches a specific level, or the energy from one cell is transferred to another cell to achieve a balanced voltage.

2.4 Overview of voltage equalisation circuits

Based on the different ways to deal with extra energy in cells, voltage equalisation for multi-cell battery packs can be divided into two categories: dissipative and non-dissipative methods. Typically a dissipative equalisation circuit uses an energy dissipating unit such as a resistor to absorb energy from a cell which has a higher voltage [65, 66]. A dissipative circuit is shown in Figure 2-9 and as shown, resistors will shunt to cells that have higher voltages by activating switches. Thus, these resistors consume energy from the battery cells by converting electric energy into heat until all cells have the same voltage. This method is also known as passive equalisation and it has been widely used typically in low power systems. Benefits include simple circuit structure and controlling and low manufacturing costs. However, passive equalisers show low energy efficiency since energy is wasted in heat, which can produce a temperature rise in the battery pack. Thus passive equalisation requires additional cooling efforts to manage any excess heat. In addition, the amount of current drawn by the shunt elements is not regulated. As a result, the cell voltages are not fully regulated [67].

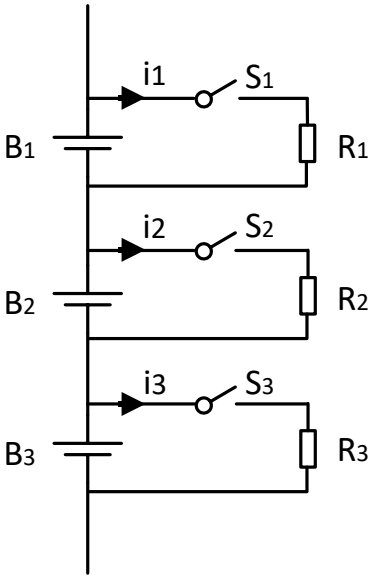


Figure 2- 9 – Dissipative voltage equalisation circuit

Compared to dissipative equalisation, non-dissipative equalisation circuits enhance energy efficiency by using electronic circuits to transfer energy from higher voltage cells to lower voltage ones; therefore, it is also known as active equalisation. This method aims to make better use of the electrical energy stored in battery cells at the expense of greater circuit complexity and higher fabricating costs. Active voltage balancing gains much more popularity in systems with higher power ratios.

There are several types of non-dissipative equalisation circuits according to the energy transmission medium (ETM) used, and they belong to families grouped either by constituent components or energy transfer method. Categorising by constituent components indicates the physical properties of the circuit, such as size, weight, component count, and cost. Meanwhile, grouping by energy transfer method describes the equalisation rate, modularity, and flexibility. Energy transfer methods are considered below in terms of three aspects: energy flow path, energy transfer sequence, and energy transfer mode.

2.4.1 Energy flow path

There are two types of energy flow path, which are illustrated in Figure 2-10. Assuming that battery cell *Bn* has the highest voltage and requires discharging, then two possible energy flow paths appear. Energy can either go to the adjacent cells *Bn-1* or *Bn+1*, or to any cells in the stack. These two energy flow paths are referred to as energy neighbour flow (Figure 2-10(a)) and energy global flow (Figure 2-10(b)).

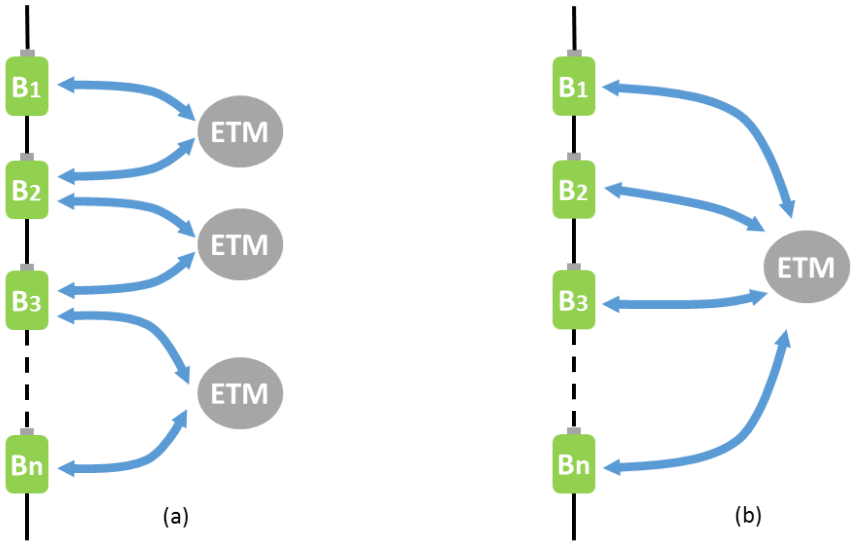


Figure 2- 10 – Energy flow paths: (a) neighbour flow; (b) global flow

The energy neighbour flow scheme is modular and the circuitry required is relatively easy to design. Also, due to its modularity, this scheme can be easily adapted for battery packs with no matter how many cells in. However, energy neighbour flow scheme become less attractive for applications with many cells. This is due to the poor efficiency caused by all of the conversion stages that are required to move energy from B_n to a target cell, in the worst case, from the top to the bottom. Also, energy rippling through the different stages results in a slow distribution speed.

Energy global flow schemes are considered to be a more desirable solution for applications with large battery stacks, since they transfer energy from B_n to a target cell far away using only one conversion step. This scheme is therefore more efficient.

2.4.2 Energy transfer sequence

Based on energy transfer sequence, equalisation circuits can be divided into two types: single and multiple equalisation schemes. This property is relevant to the equalisation rate and flexibility of circuits. Single equalisation schemes operate on the basis that only one equalisation event takes place in one time period. This is usually the case for energy global flow schemes. Multiple equalisation schemes offer the possibility that several equalisation processes can take place simultaneously. Normally, circuits based on the energy neighbour flow scheme operate as multiple equalisers, since equalisations in these schemes happen independently with isolated energy flow paths.

2.4.3 Energy transfer mode

There are three types of energy transfer mode: all-to-all, one-to-one, and one-to-all equalisation, as indicated in Figure 2-11. The choice is determined by the energy transmission medium that is used in the equalisation circuit. Usually, circuits using inductors or capacitors form one-to-one equalisation circuits and circuits with multi-winding transformers form one-to-all or all-to-all equalisation circuits.

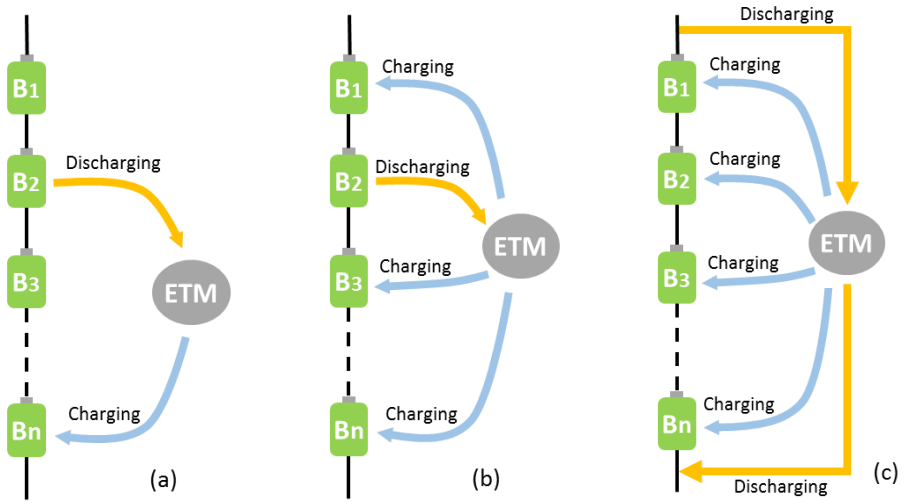


Figure 2- 11 – Energy transfer modes: (a) one-to-one equalisation; (b) one-to-all equalisation; (c) all-to-all equalisation.

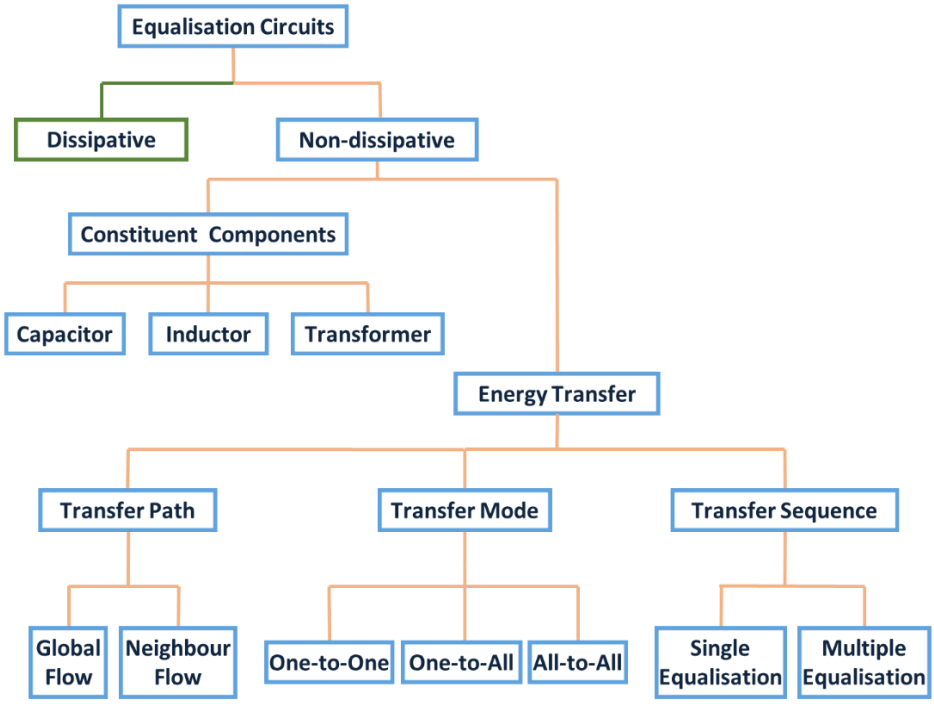


Figure 2- 12 – Taxonomy of equalisation circuit categories.

Figure 2-12 presents a taxonomy of equalisation circuits based on the discussion above. Details of each equalisation circuit scheme given in the next section are based on these categories.

2.5 Description of existing schemes

This section provides an overview of existing equalisation circuits from the point of view of their operational principles, taxonomic categories, and their advantages and disadvantages.

2.5.1 Switched capacitor equalisation scheme

It has been proposed in [68, 69] that voltage equalisation can be achieved using an auxiliary stack of capacitors paralleling battery cells via transistors. This scheme is shown in Figure 2-13. In this method, there are twice as many transistors as battery cells. They are grouped into upper switches *Sun* and lower switches *Sln* which are switched alternatively. The paralleled capacitor *Cn(n+1)* can be shunted to either the upper cell *Bn* or lower cell *Bn+1* according to the state of the switches.

When upper switches are gated on, the capacitors are connected to upper cells. Battery cells that have a higher voltage than their corresponding capacitor cells deliver energy to the capacitors. Once the lower switches are turned on, the capacitor cells are shifted to battery cells and release energy if a capacitor has a higher voltage than the battery cell. The inverse process can be used when energy is transferred from lower cells to upper cells. After a number of cycles of the process, the voltage of cells in the stack will be balanced.

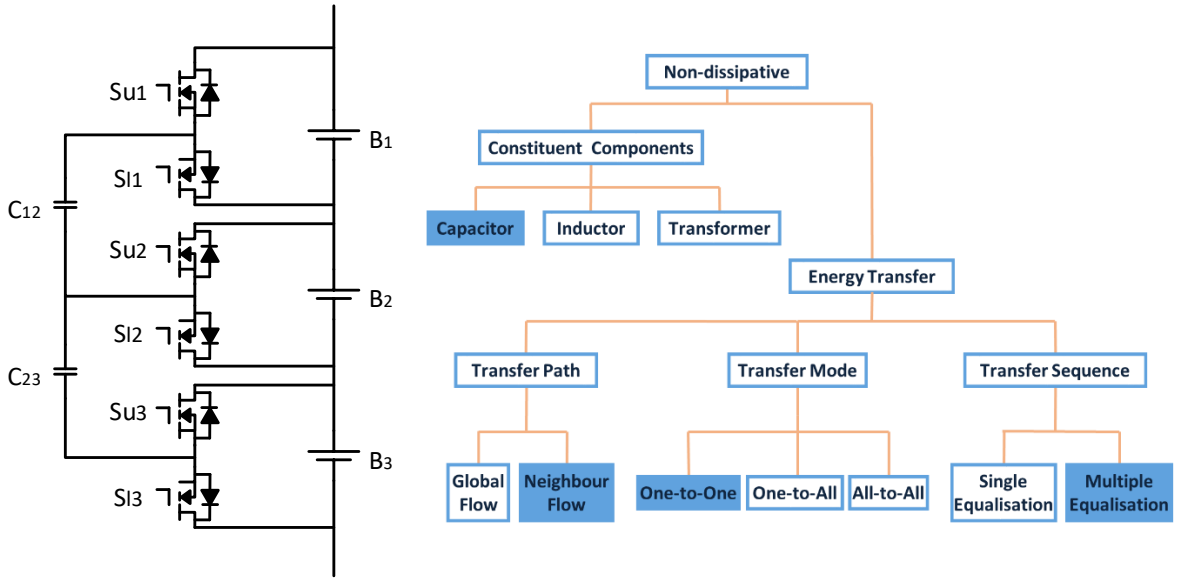


Figure 2- 13 – Switched capacitor equalisation circuit and taxonomic category.

Generally, equalisation circuits based on the switched capacitor are simple in implementation and controlling. For a battery string with N cells, the equalisation circuit requires 2N transistors, moreover, the voltage/current stress on transistors are low. It operates by open-loop control without monitoring the voltages of cells and can be used for low- and high-power applications [70]. The main disadvantage is the equalisation rate. When the voltage difference between adjacent cells is small, the balancing current between them is low, and so is the equalisation speed.

2.5.2 Flying capacitor equalisation scheme

Figure 2-14 shows the implementation of the flying capacitor equalisation circuit. Each cell in the stack is equipped with two pairs of bidirectional switches so that all cells can be connected to the flying capacitor by conducting its two corresponding switches. The basic idea of this scheme is to transfer energy from a higher voltage cell to the flying capacitor and then to deliver the energy to a lower voltage cell. The operation is repeated until the voltages of all battery cells are balanced.

The principle of operation of this circuit is simple. All cells in the stack are connected to the flying capacitor in turn, delivering or demanding energy from it. So, if a battery cell has a higher voltage than the capacitor, energy is delivered from the cell to the capacitor; otherwise, energy flows from the capacitor to the battery cell. By discharging cells with higher voltage and charging cells with lower voltage, balanced voltage will be achieved. This operating principle needs no voltage sensing or closed-loop control in the circuit; however, energy can only be transferred between two neighbouring cells at a time [66, 71].

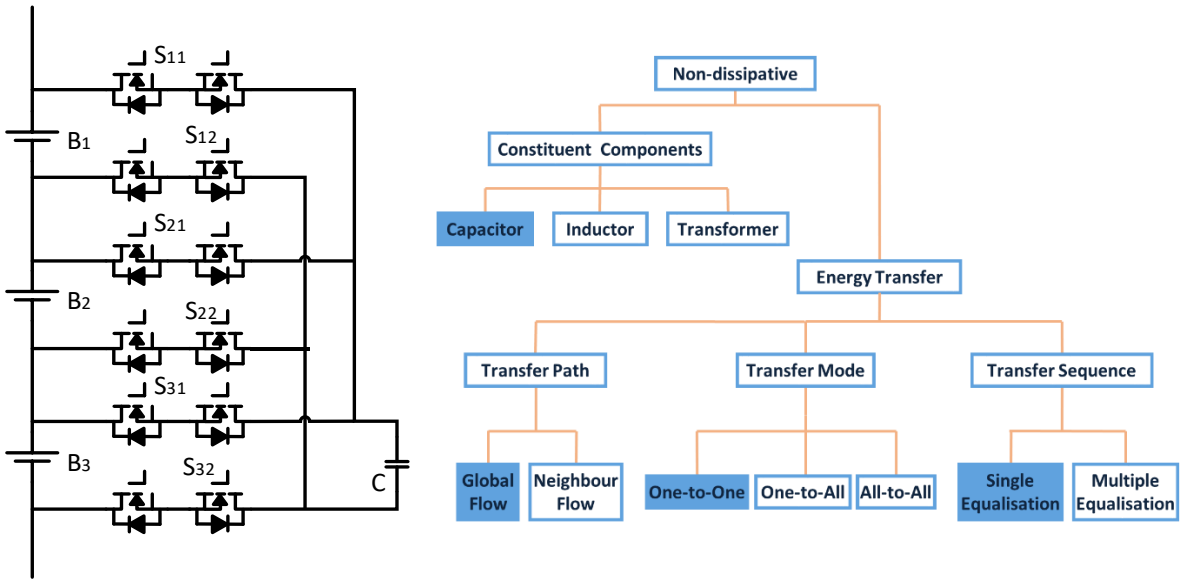


Figure 2- 14 – Flying capacitor equalisation circuit and taxonomic category

A variation of the control method has been proposed in which source and target cells can be selected intelligently [28, 72]. Assuming that *B1* has a higher voltage than *B2*, equalisation between them can be accomplished by switching *S11*, *S12* and *S21*, *S22* alternately, and in this way energy is transferred from *B1* to *B2* via the flying capacitor. Benefitting from global energy flow, this method dramatically reduces equalisation time, especially when the source and target cells are at opposite ends of the stack. However, additional controls and voltage sensors are required to detect and select cells.

Compared to the switched capacitor equalisation circuit, the flying capacitor equaliser has more flexible but complex control algorithm, and the number of required switches are doubled (4N switches for an N-cell pack) but with low stress. The power loss of the circuit are mainly the switching loss and conducting loss of the switches, hence, the circuit efficiency is relatively low.

Equalisation circuits based on capacitors have the drawback that the equalisation current is limited by the voltage difference between two cells. Therefore, they are not suitable for applications in which cells would need to be balanced rapidly. Equalisation schemes using inductors or transformers as the energy exchange medium have the design option to stipulate specific equalisation currents, and they can therefore be used for faster balancing. These schemes are discussed in the following sections.

2.5.3 Buck-boost converter equalisation scheme

In this scheme, each consecutive pair of battery cells has an associated bidirectional buck-boost converter, as shown in Figure 2-15 [73-77]. Thus, any cell in the stack except for the top and bottom cells is associated with two converters. This arrangement offers energy flow paths from one cell to either of its neighbours.

When *B1* is perceived to have a higher voltage than *B2*, then the first buck-boost converter is activated. *S1* and *S2* are switched alternately. Energy is firstly delivered from *B1* to inductor *L12*, where it is stored during *S1* is conducting. When *S1* is turned off and *S2* is turned on, the inductor *L12* continues to conduct and transfers energy to *B2*. This process will be repeated until *B1* and *B2* have balanced voltage.

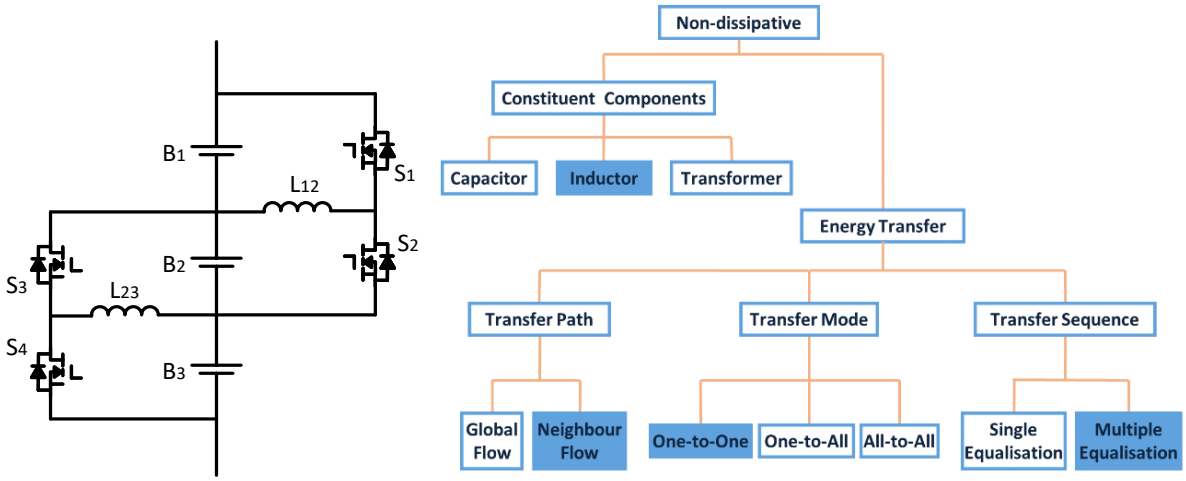


Figure 2- 15 – Buck-boost converter equalisation circuit and taxonomic category

Since the structure of the scheme only provides an energy flow path between adjacent cells, there is no direct path connecting non-consecutive cells. For example, to transfer energy from B_1 to B_3, energy must pass from B_1 to B_2, and then from B_2 to B_3. In this way, the equalization rate of the circuit is determined by the efficiency of each converter and the size of the stack. The longer the battery stack, the higher the number of cascaded steps take to transfer energy, and therefore the equalisation speed is lower. But due to the fact that the path between each pair of cells is isolated from others, and converters in the scheme are controlled independently, multiple equalisation procedures can take place simultaneously, and this helps to save equalisation time to some extent.

The other drawback of this scheme is that within a switching period T_s, the source cell is discharged only during DT_s (where D stands for duty cycle) and the target cell is charging in the rest of the duty cycle $(1-D)T_s$. The equalisation time and efficiency of this equalisation scheme are therefore limited [78].

The operation of this circuit requires voltage sensors to detect each cell, as well as a controller to deal with all of the buck-boost converters. This makes the circuit complicated and increases its cost. The circuit, however, has an important advantage of a high degree of modularity. Especially for high power applications with long battery stacks, modularity in the design of battery equalisation circuits is good for two reasons: it is easy to update the circuit when adding or subtracting cells from the stack; and the failure of a single converter will not affect other converters in the system, and it is far cheaper to replace one disabled part.

A variation of an equalisation scheme based on the buck-boost converter has been proposed in [79]. The circuit scheme is shown in Figure 2-16 where each cell in the stack has an associated buck-boost converter. Rather than separate units as in the conventional scheme (Figure 2-15), the converters are connected successively; however, the control for each transistor switch is still independent. The capacitor Cr is used as temporary energy storage, and the stored energy is redistributed back to the battery stack through an auxiliary buck-boost converter.

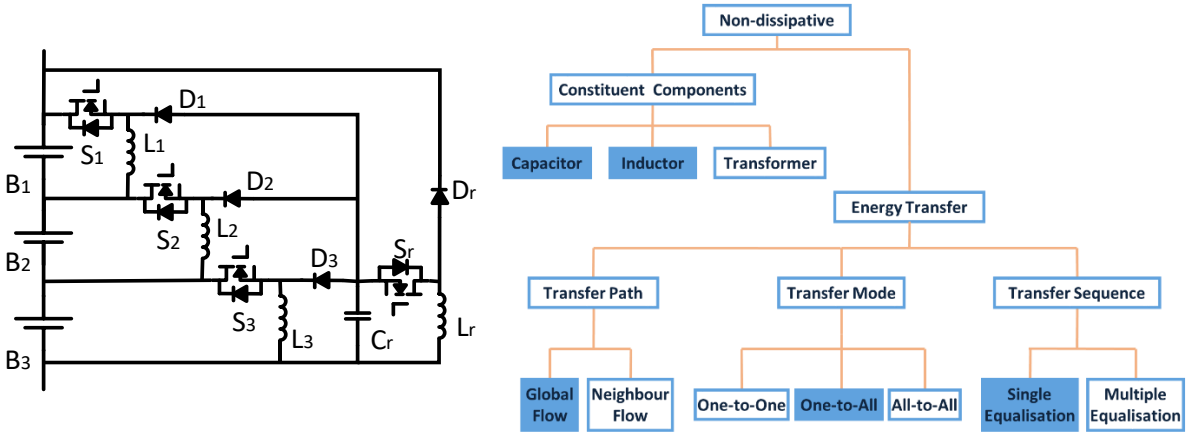


Figure 2- 16 – Successive buck-boost converter equalisation circuit and taxonomic category

When the cell B1 is detected to have the highest voltage, then the top converter is activated. During the conduction period of *S1*, current flows from the cell *B1* to the inductor *L1* and energy is stored. As soon as *S1* is turned off, the inductor continues to conduct and delivers energy to downstream cells *B2*, *B3*, etc., as well as to the capacitor *Cr*. By repeating this process, the extra energy in cell *B1* is distributed to the rest of the cells in the pack. However, since there is no cell under the bottom cell, if it has the highest voltage, the energy stored in the bottom inductor is transferred into the capacitor *Cr*, and then delivered back to the stack by the auxiliary buck-boost converter.

For the same number of cells, the successive buck-boost converter equaliser requires one more capacitor and two more inductors for energy temporary storage compared to the traditional scheme. Besides, the sequential connection of converters impairs the modularity of the circuit. However, it offers an energy transfer mode which the traditional circuit is not capable of, where one cell is discharged to charge all downstream cells. Therefore, the control strategy is simplified. During a single equalisation procedure, only one switch is controlled to discharge the source cell and there is no need to select target cells.

2.5.4 Cuk converter equalisation scheme

Figure 2-17 shows the scheme of an equalisation circuit based on the Cuk converter [78, 80, 81]. Instead of using buck-boost converters to exchange energy, this method employs Cuk converters. In this circuit, each pair of consecutive cells is associated with a bi-directional Cuk converter.

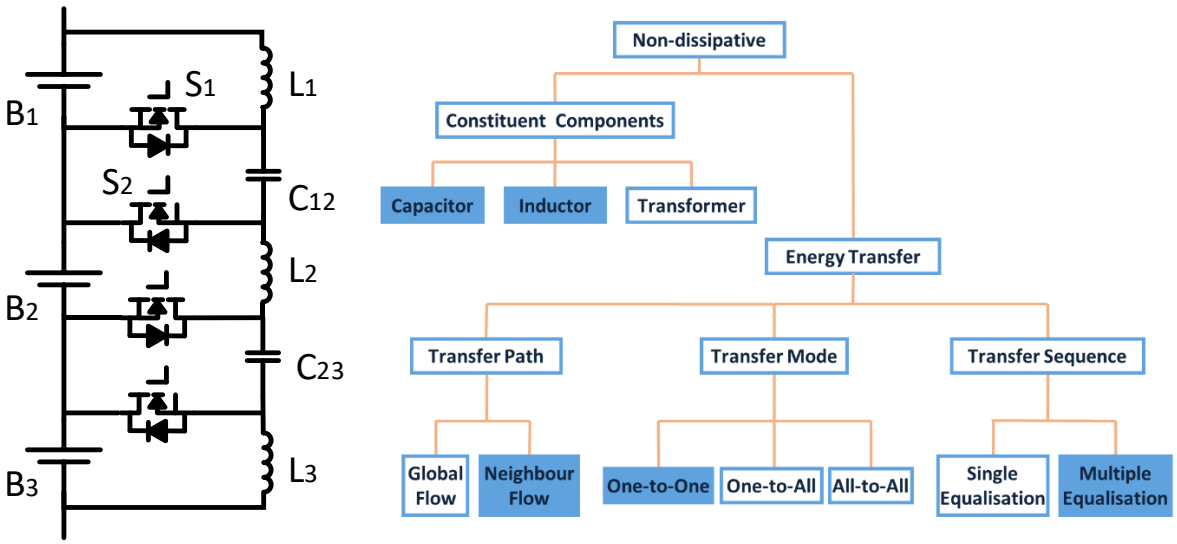


Figure 2- 17 – Cuk converter equalisation circuit and taxonomic category

During operation, both inductors and capacitors are involved in energy transfer. Considering that cell *B1* has a higher voltage than cell *B2*, two steps are necessary to obtain a balanced voltage. In the first step, *S1* is turned on and *S2* is turned off, and cell *B1* releases energy to inductor *L1* while capacitor *C12* is discharging and energy is collected by cell *B2* and inductor *L21*. In the second step, *S1* is turned off and *S2* starts to conduct. Cell *B1* and inductor *L1* are then discharging and *C12* collects energy. Simultaneously, inductor *L21* releases energy to cell *B2* via *S2*. This procedure can also operate backwards to transfer energy from *B2* to *B1* if the former has the higher voltage.

Although this circuit requires more components when compared with the buck-boost converter equalisation circuit, the discharging of source cells and charging of target cells are continuous in one switching period. Therefore, the equalisation speed is improved if the discharging and charging current is the same.

A modified scheme of a bus-based isolated Cuk converter equalisation scheme has been proposed [66, 82], and its circuit is presented in Figure 2-18. In this method, one terminal of a Cuk circuit is connected to a battery cell, and the other terminal is connected to the energy bus so that the cells are isolated from the energy bus.

With this arrangement, cells which have higher voltage release energy to the energy bus via the operation of the corresponding Cuk converters. Simultaneously, cells with lower voltage absorb energy from the bus. The energy bus provides flow paths between any pairs of cells in the stack. The effect of this is that the equalisation time is reduced and efficiency is improved.

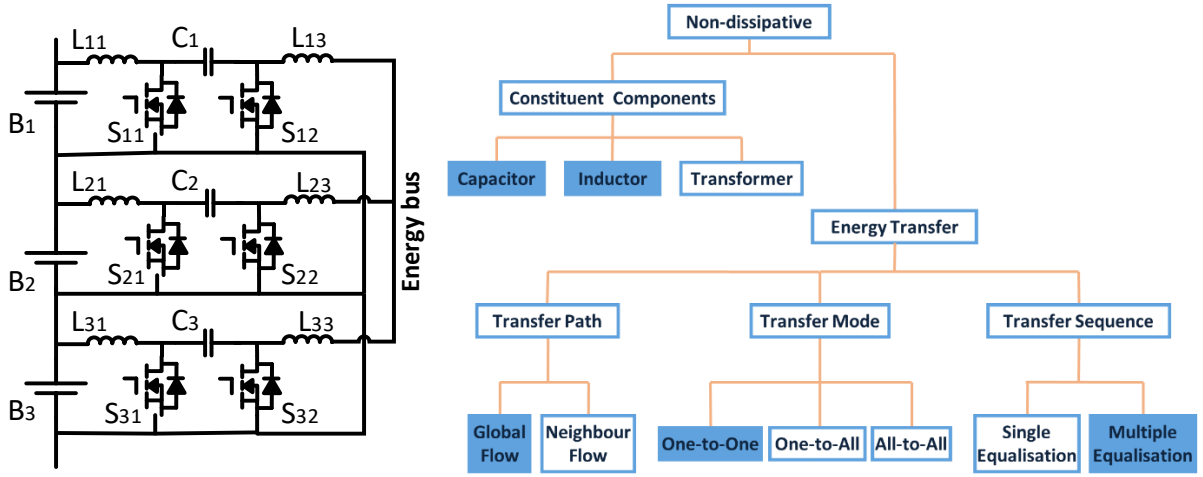


Figure 2- 18 – Bus-based isolated Cuk converter equalisation circuit with taxonomic category.

In general, inductor-based equalisation circuits including buck-boost, Cuk converters can realise bidirectional energy flow with high balancing efficiency and low stress, nevertheless, they often require a complex switch array and a precise control algorithm [83].

2.5.5 Multi-secondary winding transformer equalisation scheme

The equalisation circuit shown in Figure 2-19 utilises a transformer with distributed secondary windings to transfer energy from the stack to individual cells [29, 84-90]. The primary winding of the transformer is connected to two terminals of the battery stack with a transistor switch *S1*, while each secondary winding is shunted to a battery cell via a diode. Coils in the secondary side are reverse-coupled with the primary coil on a magnet core and therefore the transformer operates as a flyback converter. Moreover, secondary coils are designed with the same number of turns so that the voltages across them are identical when they are charging cells.

When an unbalanced voltage is detected, switch *S1* is gated on. Energy now flows from the battery stack to the transformer. The orientation of diodes between the cells and the transformer determines that no current flows in the secondary coils during this magnetising period, and therefore energy is stored in the transformer as a magnetic field. When *S1* is switched off, the inverted MMF is transferred to the secondary coils as a negative voltage allowing current to flow through the diodes to the battery cells. During the demagnetising period, the voltage of each secondary coil is equal and clamped to the lowest cell voltage in the stack. If a cell has a higher voltage than the coils, then there will be no current to charge the cell in the current equalisation process.

Hence, the lowest voltage cell is always getting charged first in this circuit. For example, if the initial voltages of cells *B1*, *B2* and *B3* are 3.0V, 3.5V and 3.7V respectively, then at the first stage of equalisation all three cells are discharged but only *B1* is charged and therefore the voltages of *B2* and *B3* fall but the voltage of *B1* increases until B1 and *B2* are balanced. The next stage is to discharge the stack and charge *B1* and *B2* until all cells have balanced voltage. Figure 2-20 shows the simulation results for cell voltage and the equalisation process based on the example above.

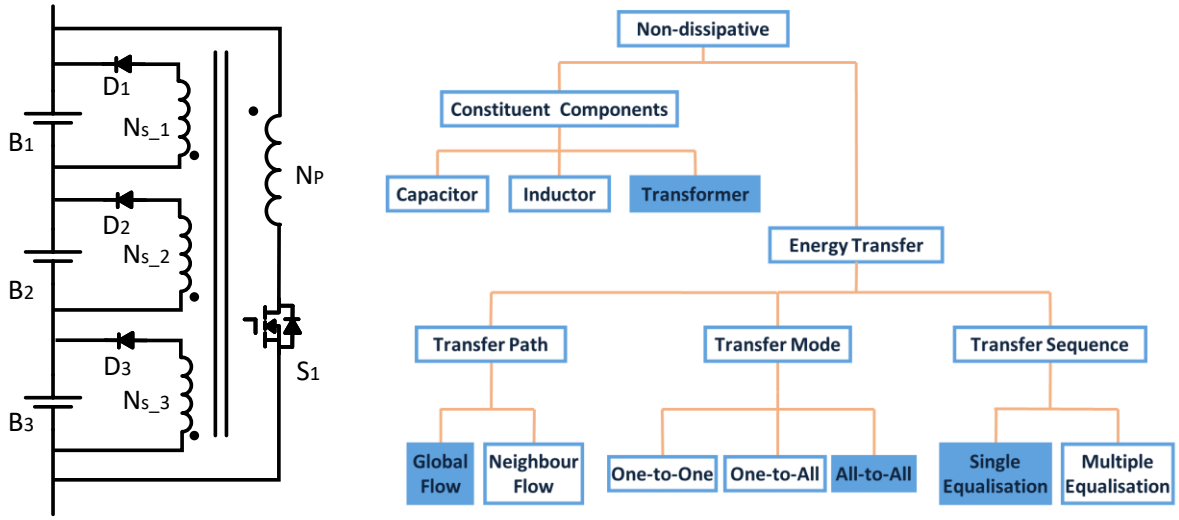


Figure 2- 19 – Multi-secondary windings transformer equalisation scheme and taxonomic category.

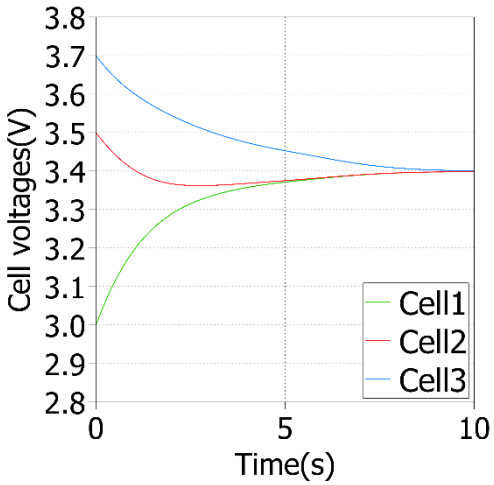


Figure 2- 20 – Voltage equalisation with multi-secondary winding transformer circuit.

The main advantage of this equalisation scheme is that it employs a self-regulating centralised converter. The control of this circuit is extremely simple, since there is only one transistor switch involved. The transistor is therefore required to support the voltage of the entire stack and the magnetising current.

The principle disadvantage of multi-winding transformer methods is that, irrespective of configuration, the transformer requires a discrete winding for every cell in the system. This reduces the modularity for the product of a given converter and makes the construction of the transformer extremely complex since all secondary windings must exhibit identical electromagnetic characteristics in order to properly perform a balancing operation. Achieving this is difficult when considering tens or more windings around a single transformer core, and the cost of developing such a bespoke arrangement and manufacturing it correctly to specification may be prohibitively costly.

2.5.6 Multi-primary winding transformer equalisation scheme

Another topology that is transformer-based is shown in Figure 2-21. In this configuration, energy flow paths between cells are provided by a transformer with distributed primary windings [29, 87, 91, 92].

Since the primary coils are forward-coupled in a magnet core, their polarities are the same, and they operate like a forward converter. This makes this scheme distinctive that in theory, there is no intermediate energy storage and energy is transferred between cells directly along the energy flow path. In a forward converter, coil Ns is used for the demagnetisation of the transformer when the switches are turned off.

This scheme offers a self-regulating equalisation method. When a difference in voltage is detected across one or more cells, the transistor associated with the cell which has the highest voltage is switched on. Energy is taken from the cell to the other ones, through the transformer and the respective diodes. During one conducting period, the voltages of all primary windings are clamped to the highest cell voltage. According to Ohm’s Law, the circuit which has a higher voltage difference gains higher current, which means that cells with lower voltage receive more energy than cells with higher voltage and thus the efficiency of the system is greatly increased.

The control of this scheme is relatively simple, since only the source cell needs to be selected in each switching period and then energy will flow from the source cell to the rest of the entire pack.

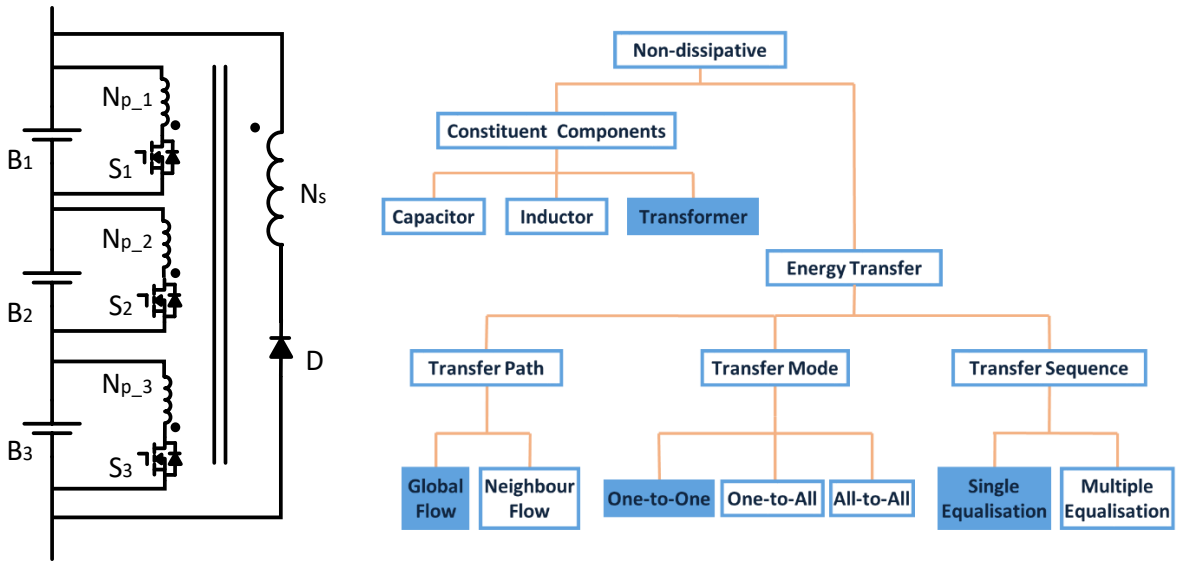


Figure 2- 21 - Multi-primary windings transformer equalisation scheme and taxonomic category.

In this circuit, the manufacture of the transformer is a big challenge, especially when the battery stack is longer. This scheme also has another drawback which is that the voltage difference between two cells has to be bigger than the forward bias voltage of the diode so that energy can flow. If the forward bias voltage of the diode is 0.5V and the voltage difference between two cells is less than 0.5V, no equalisation process can take place. However, for lithium-ion battery cells which are known to have limited voltage rates, the gap of 0.5V cannot be ignored if a balanced voltage is desired.

For multi-winding transformer based equalisation circuits, the nonideal characteristics the transformer can greatly impact the performance of these equalization schemes, including the balanced voltage and the efficiency. The main challenge is to realize a transformer structure with low and controlled parasitic and highly symmetrical transfer characteristics. These properties form the basis for realizing a fully symmetrical transformer-based equaliser. In addition, the transformer-based equalizers have poor expandability.

2.5.7 Switched transformer equalisation scheme

To avoid problems caused by multi-winding transformers, alternative configurations have been proposed in [66, 93] in which switched transformers are utilised. Their general topology is shown in Figure 2-22. The scheme is composed of three parts: a transformer with two reverse coupled windings N_1 and N_2; a multiplexor, including bidirectional switches S_1-S_4; and a selector comprising two bidirectional switches S_5

and *S6*. The multiplexor is used to select relevant cells and connect them to the transformer, while the selector determines which winding is involved.

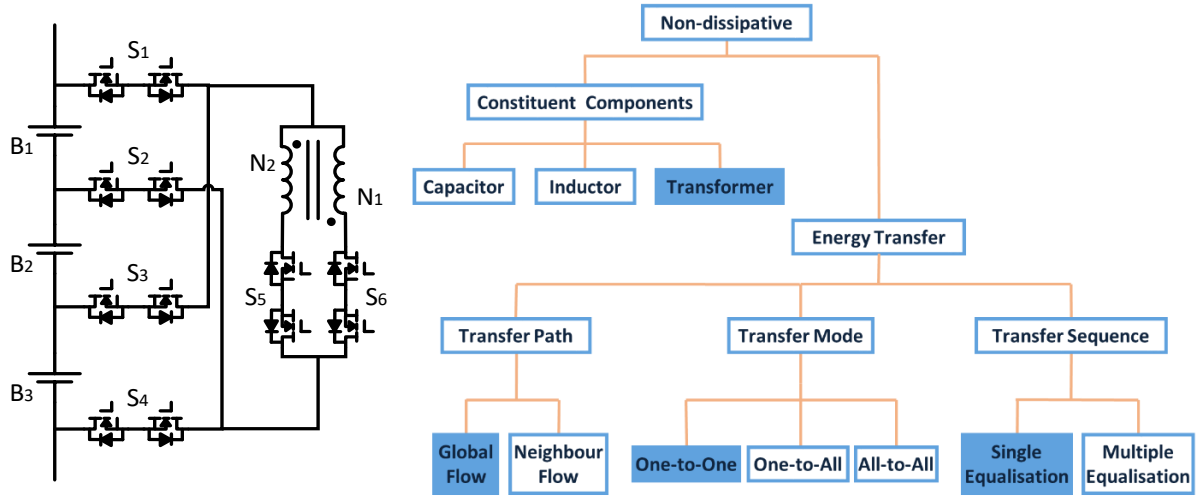


Figure 2- 22 – Switched transformer equalisation scheme and taxonomic category.

Assuming that cell *B1* has a higher voltage than *B3*, and winding *N1* is regarded as the primary winding, then transistors *S1*, *S2* and *S6* are turned on. During the conducting period, energy flows from *B1* to the transformer. As soon as those transistors are turned off, switches *S3*, *S4* and *S5* are closed to provide a flow path for energy from the transformer to the target cell *B3*.

This scheme uses a transformer with two windings instead of a multi-winding transformer, which makes the scheme more attractive for applications with long battery stacks. However, it requires more transistors and control is more complicated since the source and target cells are selected before every single switching period.

2.6 Summary

This chapter presents an overview of charging and equalisation techniques for lithium-ion batteries. Firstly, charging strategies for lithium-ion batteries are introduced and it is concluded that a fast and safe charging method is CC-CV charging. Secondly, charging systems for EVs have been reviewed, including charging power levels, the structures of charging systems and on-board charging circuits. This project focusses on Level 1 chargers for lithium-ion battery packs. Thus the design of the circuit proposed in Chapter III will be charged at a maximum of 3kW supplied from a single phase 240V grid. Thirdly, voltage equalisation circuits are studied, and a summary of the equalisation schemes is presented in Table 2-5.

Table 2- 1 – Summary of equalisation schemes

Equalisation scheme		Energy storage (consumption)	Control	Need for voltage sensing	Modularization	Cost
Dissipative	Resistor	Resistor	E	Y	E	LO
Non-dissipative	Switched capacitor	Capacitor	E	Y	M	LO
	Flying capacitor	Capacitor	C	Y	M	LO
	Buck-boost converter	Inductor	C	Y	E	M
	Cuk converter	Inductor & Capacitor	C	Y	E	M
	Multi-secondary transformer	Multi-winding transformer	E	N	H	VHI
	Multi-primary transformer	Multi-winding transformer	M	Y	H	VHI
	Switched transformer	Transformer	C	Y	E	HI

E: easy; M: moderate; C: complex; H: hard; Y: yes; N: no; LO: Low; HI: high; VH: very high.

Chapter III Development of Battery Charging System Incorporating an Equalisation Circuit

This chapter presents a new methodology for both battery charging and voltage balancing. So far, as described in Chapter II, both functions have been looked at separately. In this work, however, am attempt is made to combine both functions using one circuit rather than two. Thus a battery charger that incorporates voltage balancing is proposed. The need for and benefit of such a multi-functional unit is discussed first in this chapter. Then the proposed circuit for both charging the battery pack in EVs from the grid and achieving voltage balancing between battery cells is introduced. The main functions of the circuit can be divided into four parts and the structure and operation of each are introduced in section 3.2. There are five operational modes for the proposed circuit: two for charging batteries from the grid, and three for voltage equalisation between cells. The principal operation of each mode is described in detail in section 3.3. A simulation model of the circuit is developed and simulation results are presented in the last part of this chapter.

3.1 Design motivation

This project aims to propose multi-functionality for an active voltage balancing system that not only distributes charge between battery cells but is also able to charge batteries from the grid. Thus, a separated equalisation circuit, which is usually located in the battery management system (BMS), is not required.

Based on the results reported in Chapter II, priority will be given to non-dissipative equalisation circuits due to their efficiency. Transformer-based schemes have been shown to be most promising in order to achieve fast balancing and good efficiency. In the proposed circuit, the transformer plays a key role not only for voltage balancing, but also because it is required for the on-board charging of battery cells. Consequently, the transformer has two functions in the circuit: one is to support the voltage balancing across all battery cells, and the other is to provide electrical isolation between the grid and the battery pack for safety purposes.

Figure 3-1 shows an example of a principal circuit which is initially proposed in this study. The circuit has five battery cells *B1-B5* connected in series for simplicity. In this

circuit, each battery is connected to a secondary winding via a diode and all five windings form part of a distributed one-primary-five-secondary (1P5S) transformer. The primary winding of the transformer is connected in series with a transistor *S1* and a pair of single-pole-double-throw (SPDT) switches labelled *S2* and *S3*. The positions of the SPDTs decides the operating modes of the circuit which are as follows:

a) Charging mode. When *S2* and *S3* are in position 1, the primary winding of the transformer and *S1* are connected to the grid via a diode bridge rectifier. During the magnetising period, the transistor is gated on, and energy flows from the power supply to the transformer. Energy is not passed on to the secondary sides, as all diodes are reversed biased as long as *S1* is on. As soon as the transistor is gated off, the transformer begins to demagnetise, and diodes are forward biased. The energy stored in the transformer is now passed on to the battery cells. The equivalent circuit of this operating mode is shown in Figure 3-2(a).

b) Equalisation mode. With *S2* and *S3* in position 2, the circuit operates as a voltage equaliser. The primary winding of the transformer is now connected to the two terminals of the battery pack directly. In this way, during the magnetising period, the transformer absorbs energy from all cells and stores the energy until *S1* is gated off. When demagnetising, energy flows from the secondary windings of the transformer to the battery cells. The equivalent circuit of this operating mode is shown in Figure 3-2(b).

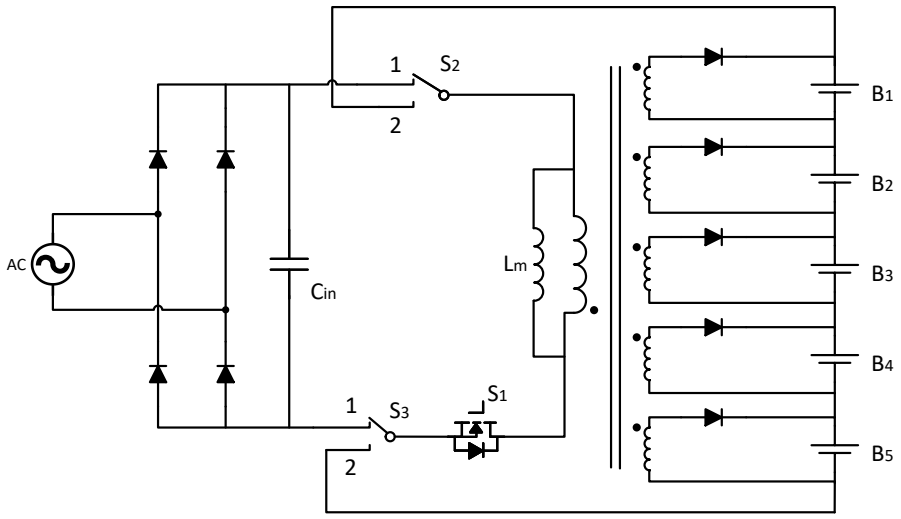
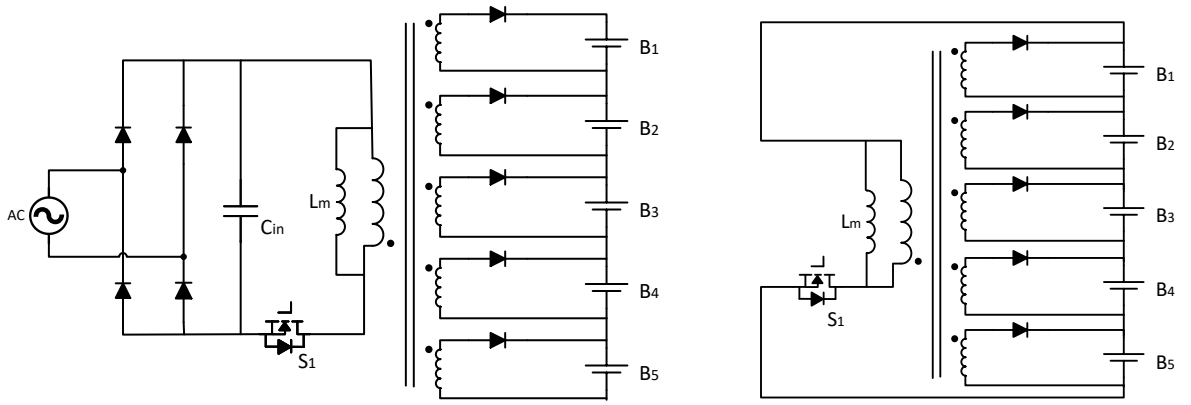


Figure 3- 1 – Principal circuit of a voltage balancing circuit based on multi-winding transformer with grid charging capability.



(a) (b)

Figure 3- 2 – Equivalent circuit of Figure 3-1 when operating for: (a) grid charging; (b) voltage balancing.

The circuit shown in Figure 3-2 operates as a flyback converter in both charging and equalisation modes. Therefore, this circuit maintains the advantages of a multi-secondary winding transformer equalisation circuit, as has been introduced in section 2.5.5. Also, the circuit is easy to control due to the fact that only one power switch is involved. During charging, when the numbers of turns in the secondary windings are equal, different charging/equalisation current to each cell based on its initial voltage can be arranged by the transformer.

The main weakness of the above circuit is the design and manufacturing of the multi-winding transformer, which becomes a great challenge particularly if the number of battery cells is high. Embedding taps into transformers is challenging and costly [94, 95] and the overall design becomes bulky. Also, the magnetic core of the transformer becomes large therefore the system is bigger in mass and volume as well [96-98].

The equalisation circuit which has been introduced in section 2.5.7 can solve the problem of a complicated transformer design, where a two-winding transformer is used. This makes it possible for a standard transformer to be used no matter how many cells are in the pack. Therefore, the proposed multi-functional circuit is based on the two-winding transformer concept.

3.2 Proposed circuit topology

This section introduces a novel topology that is able to balance voltages across battery cells and to charge these cells directly from the grid. As presented in Figure 3-3, the

circuit can be sub-divided into four parts: rectifier, isolated converter, winding selector and cell selector.

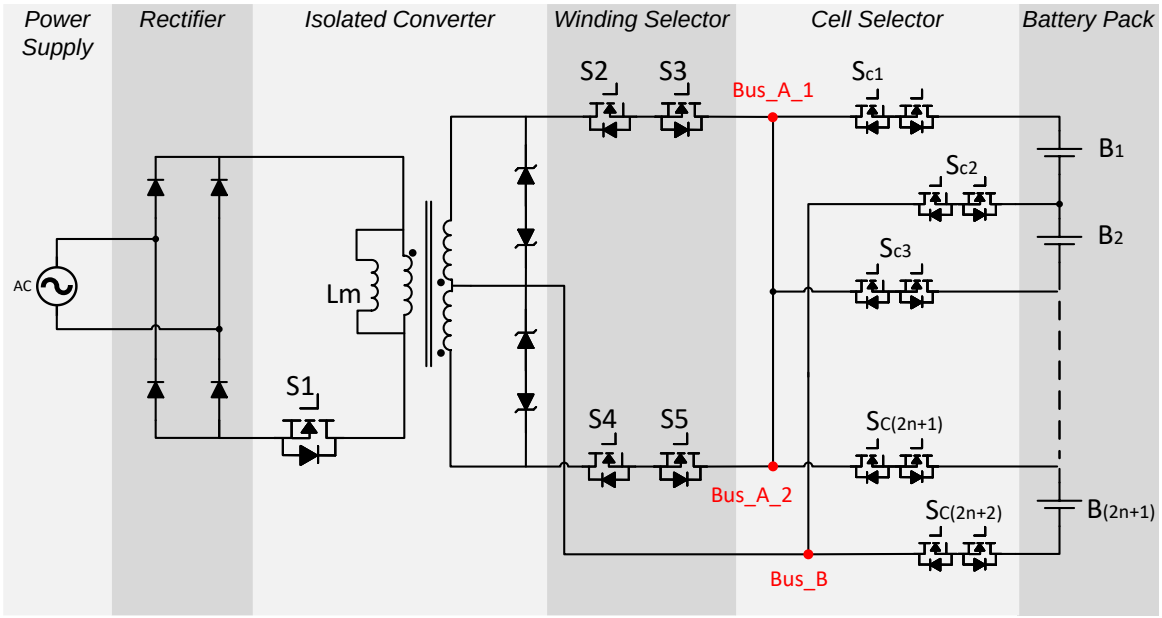


Figure 3- 3 – Proposed multi-functional battery charger integrated with voltage equalisation in (2N+1) battery cells.

To make the operational explanations easier, the proposed circuit is shown with five cells as in Figure 3-4, and this configuration is used in subsequent sections.

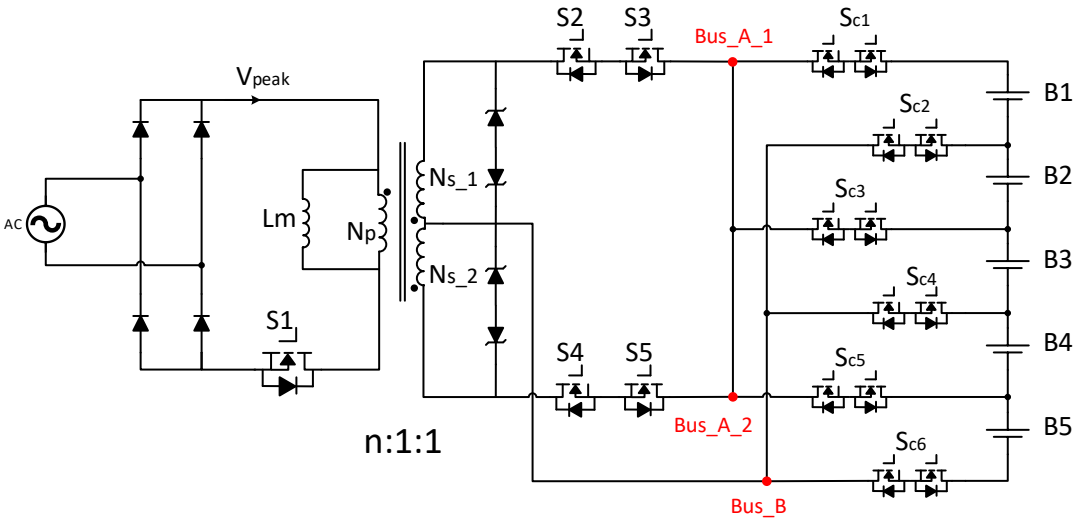


Figure 3- 4 – Proposed circuit with five cells.

3.2.1 Rectifier

For Level 1 unidirectional EV chargers, it is common to add a single-phase full-wave diode bridge rectifier to the grid in order to convert AC into a positive output voltage. However, in the proposed circuit, no capacitor is connected at the output of the rectifier, since a PFC circuit physically follows the rectifier directly. Thus the output voltage of

the rectifier swings with a frequency of 100Hz and the voltage varies from zero to a peak of 340V over 10ms.

3.2.2 Isolated converter

This part of the circuit consists of a three-winding transformer and a transistor that is connected in series to the primary winding. The input stage (primary winding and transistor) forms a PFC circuit and is used when charging the battery cells. The output stage (secondary windings) are used for two purposes: one is to form a flyback converter with the primary winding during battery charging and the other is to be used for voltage balancing which takes place when the EV is driving and is not connected to the grid. A schematic diagram of the transformer is shown in Figure 3-5. The primary winding and the two secondary windings are reverse-coupled on one magnetic core. Therefore, when power flows from the source to the batteries, irrespective of which secondary winding is involved during the de-magnetising period, the circuit always works as a flyback converter. Meanwhile, two windings in the secondary side are connected end-to-end. As indicated in Figure 3-5, while energy being transferred between two secondary windings during voltage equalisation, the transformer operates in flyback mode as well.

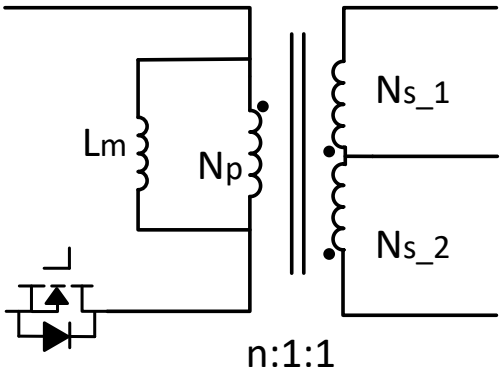


Figure 3- 5 – Schematic of transformer utilised in the proposed circuit.

The turns-ratio of the transformer is determined by the input and output voltages of the converter. The input voltage can be considered as the peak voltage of the AC power supply, and the output voltage is the sum of the rated voltages of all cells connected in series in the pack. For example, if there are N cells in the circuit, assuming these cells are identical with a rated voltage of *Vcell*, then the turns-ratio of primary and secondary windings of the transformer is calculated as follows:

$$n = N_p : N_{s\_1} : N_{s\_2} = \frac{V_{peak}}{N \times V_{cell}} : 1 : 1 \tag{3.1}$$

There are two pairs of Zener diodes parallel to the two secondary windings, the purpose of which is to protect the transistors in the winding selector and the cell selector.

3.2.3 Winding selector

The function of the winding selector is to change the fundamental operational mode of the circuit. The circuit is able to provide two different functions. One function is to charge the battery cells from the grid and the other is to balance the voltage levels across the battery cells. The first function of grid charging is used when the electric car is static, meaning that it is plugged into the grid. The second function of voltage balancing is used when the car is driving and cells must be continuously charged and discharged to achieve equal voltages across them.

In order to provide these two functions, the winding selector must be designed so that the current can flow in positive and negative directions, and it also must be designed so that the currents can be turned on and off. In addition, the circuit operates like a flyback converter, the principal operation of which requires a diode in the secondary side to block the current flowing during the magnetising period. Figure 3-6 shows the block diagram of the circuit when a battery cell is charging and discharging, including the directions of current flow.

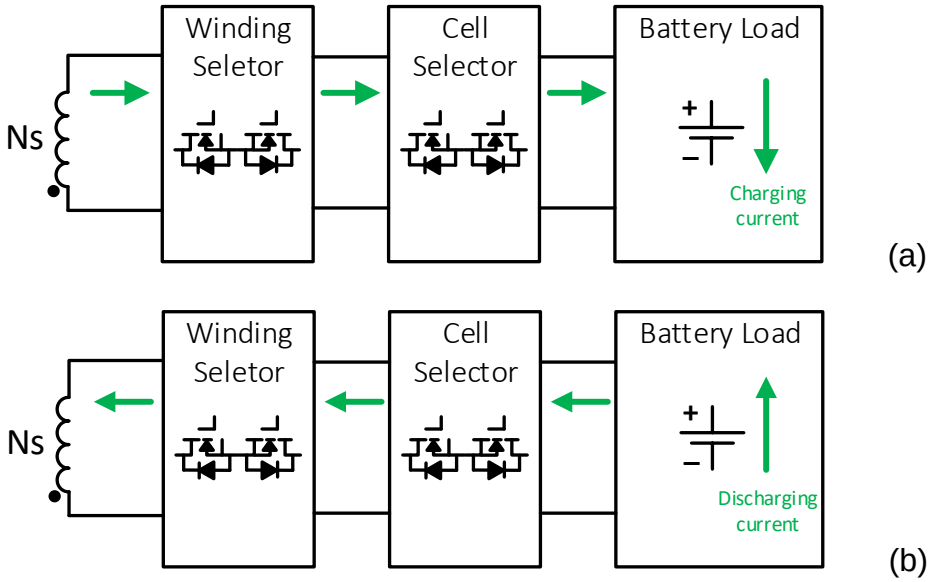


Figure 3- 6 – Block diagrams of the circuit with current directions when battery cell is: (a) charging; (b) discharging.

These two requirements result in the circuit shown in Figure 3-7. The winding selector comprises two secondary windings and four transistors. The two end-to-end connected

secondary windings form a transformer with three terminals. The top and bottom terminals are each connected to a pair of transistors and have been labelled as *Bus_A_1* and *Bus_A_2*. The midpoint of the transformer is the third terminal labelled *Bus_B.*

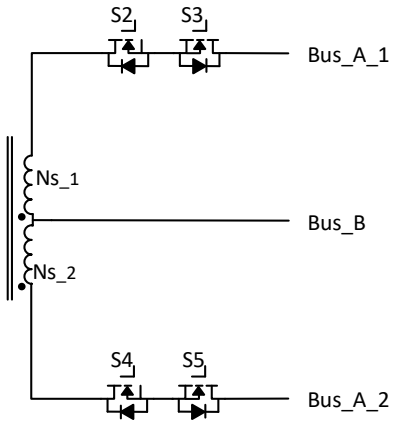


Figure 3- 7 – Secondary windings in the winding selector.

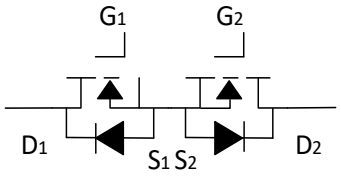


Figure 3- 8 – Bi-directional switch (gate, drain and source indicated).

The two anti-series connected transistors with their body diodes make up a bi-directional switch. MOSFETs have the advantages of having an intrinsic anti-parallel diode. In the winding selector, a pair of MOSFETs in one bi-directional switch are controlled independently. For example, as shown in Figure 3-8, when the left MOSFET is gated on and the right one is gated off, this bi-directional switch only allows current flow in one direction, as the opposite anti-parallel diodes D1 and D2 will block the opposing current flow.

This arrangement of the winding selector makes it possible that current can go through either of the windings and is under control in both directions. In total, this winding selector achieves four current flow modes, they are:

- Upper clockwise current: clockwise current flows through *S2* and the body diode of *S3*, then into *Bus_A_1*;
- Upper anti-clockwise current: anti-clockwise current from *Bus_A_1* goes through *S3* and the body diode of *S2*;
- Lower anti-clockwise current: anti-clockwise current flows through *S4* and the body diode of *S5*, then into *Bus_A_2*;
- Lower clockwise current: clockwise current flows through from *Bus_A_2* goes through *S5* and the body diode of *S4*.

The four current flowing modes are indicated in Figure 3-9.

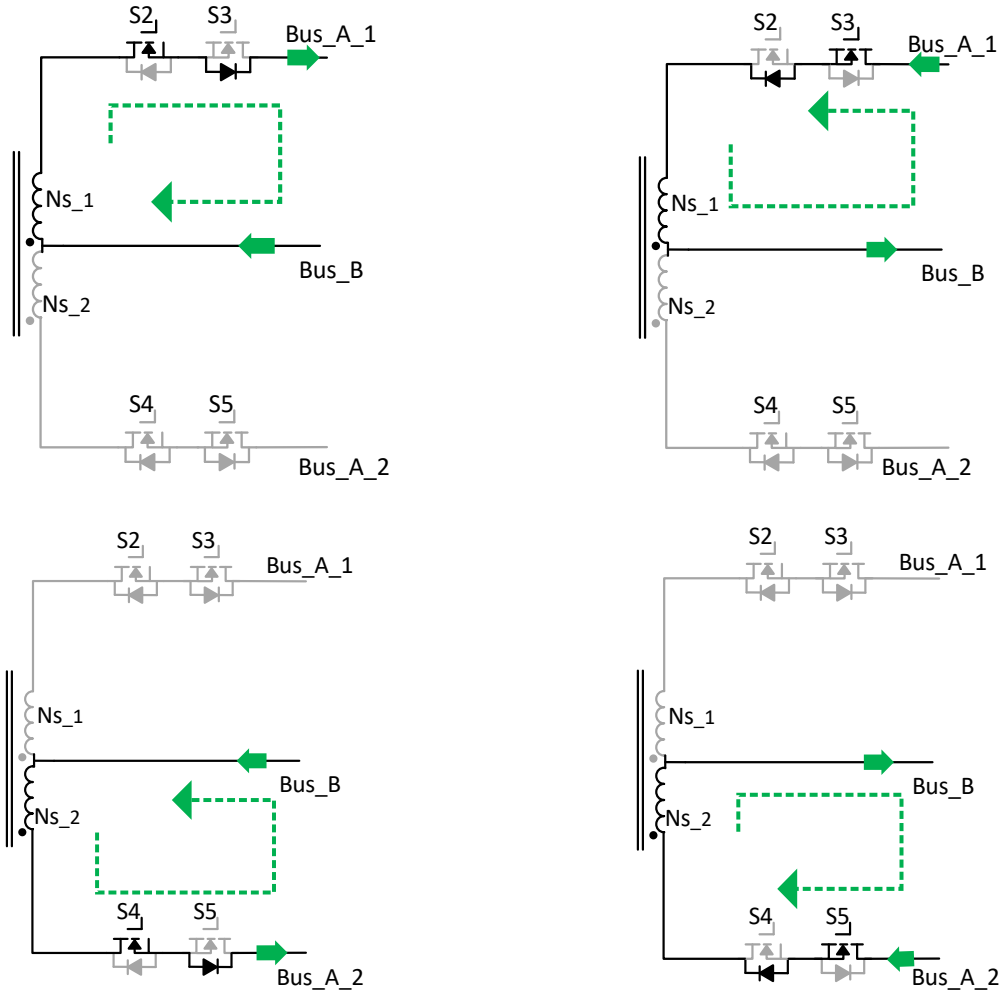


Figure 3- 9 – Four current flow modes in the winding selector.

It is worth mentioning that in Figure 3-9 the buses *Bus_A_1* and *Bus_A_2* are shown as two separated and isolated points. However, in the next section, these two buses are joined to become one bus labelled *Bus_A*.

3.2.4 Cell selector

This part of the circuit is designed to target the individual battery cells. In order to allow battery cells to be charged and discharged, the circuit must make sure that the current for each cell can go in and out. To allow bi-directional current flow a bi-directional switch to each pole of the battery cell is added, as shown in Figure 3-10. Alternatively, one bi-directional switch is connected to the positive pole of the battery and the other switch is connected to the negative pole of the battery. All switches connected to the negative poles of each battery cell are linked to form *Bus_B* (blue), and the same applies to all switches connected to the positive poles of the battery cells forming *Bus_A* (red), and *Bus_A* splits into *Bus_A_1* and *Bus_A_2*. With this structure, twice as many bi-directional switches as battery cells are required in the cell selector. For

example, if *B1* is the source cell, then switches *S11* and *S12* are gated on, and if *B2* is the target cell then switches *S21* and *S22* are on.

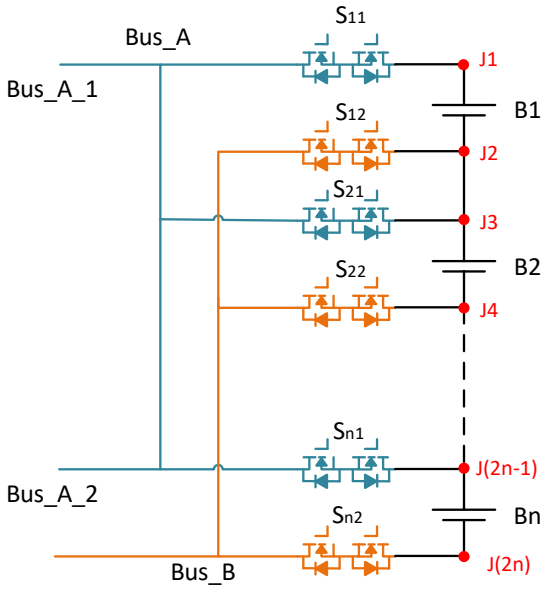


Figure 3- 10 – Cell selector with N cells.

An alternative to the circuit shown in Figure 3-10 is shown in Figure 3-11. In this circuit, the even number nodes are connected via bi-directional switches to *Bus_B* and the odd nodes are connected to *Bus_A*. The modified cell selector reduces the number of bi-directional switches required from 2N (Figure 3-10) to N+1, where N is the number of battery cells. The reduction in bi-directional switch numbers, however, comes at the expense of the circuit's operational flexibility. Unlike the previous design, where any combination of battery cells is possible for charge transfer via the winding selector, in the modified circuit charge transfer can only take place when the number of cells in a target string is odd. This makes sure that, when several consecutive cells are charging or discharging together, the top and bottom nodes of the string are connected to *Bus_A* and *Bus_B* separately. For example, *B1* can make itself a target by conducting *SC1* and *SC2*; *B1*, *B2* and *B3* together can also be a target by conducting *SC1* and *SC4*. However, a combination of *B1* and *B2* may never work because *SC1* and *SC3* are both connected to *Bus_A*, and thus there will be no closed loop in the cell selector.

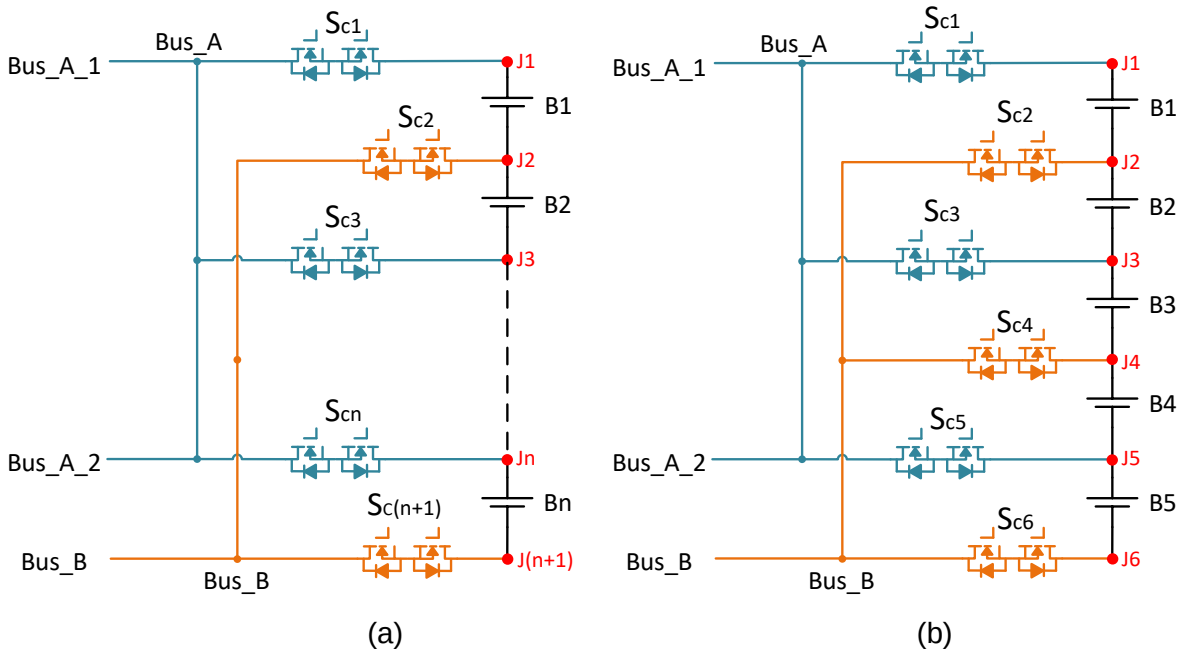


Figure 3- 11 – Modified cell selector with: (a) N cells; (b) five cells.

Table 3- 1 – Look-up table for switching states in a cell selector of five cells

	Switches						
Participant cell(s)		S_{C1}	S_{C2}	S_{C3}	S_{C4}	S_{C5}	S_{C6}
	B1	ON	ON	OFF	OFF	OFF	OFF
	B2	OFF	ON	ON	OFF	OFF	OFF
	B3	OFF	OFF	ON	ON	OFF	OFF
	B4	OFF	OFF	OFF	ON	ON	OFF
	B5	OFF	OFF	OFF	OFF	ON	ON
	B1-B3	ON	OFF	OFF	ON	OFF	OFF
	B2-B4	OFF	ON	OFF	OFF	ON	OFF
	B3-B5	OFF	OFF	ON	OFF	OFF	ON
	B1-B5	ON	OFF	OFF	OFF	OFF	ON

The limitation may appear to be a disadvantage. However, this disadvantage can be overcome by repeating charging or discharging processes. For instance, *B1* and *B2* cannot be charged simultaneously, but *B2* can be charged after B1. Besides, the controller of the cell selector circuit can choose if charging and discharging is taking place in individual cells only or in a string of cells. This flexibility allows for the statistical possibility that cells can be equalized without the use of a large number of bi-directional switches. Consequently, it was decided to use the modified cell selector for the final circuit. An example of activated switches correlating to single battery cells and cell combinations for the five battery cells *B1* to *B5* is shown in Table 3-1.

In the cell selector, the two MOSFETs forming pair of the bi-directional switches are controlled by a common control signal. This simplifies the gate drive circuit. It must be noted that the control of the MOSFETs in the winding selector must not to be combined. Each MOSFET in the winding selector should be controlled independently, whereas the MOSFETs in the cell selector are gated simultaneously with the same signal.

To summarize, in the proposed circuit, the cell selector is in charge of selecting and connecting cells (either individual battery cells or a string of battery cells) and the winding selector is in charge of the current direction for grid charging and voltage balancing modes. A detailed description of the circuit follows in the next section.

In the proposed circuit, cells are selectively connected to the coils. Compared to other multi-winding transformer based equalisation circuit, the proposed circuit shows better modularity that it is easy to update when adding or taking away cells from circuit, and a failure of a single switch would not lead to a failure of the whole circuit.

However, the voltage stress for the switching devices are high. For the main switch, it needs to stand for the input voltage, the Induced Magnetomotive Force (IMF) generated by the secondary side, and the voltage spike due to the leakage inductance. Stress for the secondary switches is less. However, rather than one switch is designed to connect one cell, secondary switches in the proposed circuit are requested to stand the voltage of a battery stack, depends on the operational mode and cells combination. For example, during charging the whole battery pack, switches in the winding selector and the top and bottom switches in the cell selector need to bear with the voltage of the whole battery pack.

3.3 Operating principles of the proposed circuit

It has been shown that the proposed circuit can operate as a grid charger or an equaliser, and the parts of the circuit play the same roles in both functions. The key component of the circuit is the transformer, which provides the required isolation during grid charging mode and provides the energy storage required for the voltage balancing mode. The winding selector determines how the current flows in the converter and the cell selector is responsible for the activation of the target cells that are involved in grid charging or voltage balancing. This section describes the operational modes of the proposed circuit for both grid charging and voltage equalisation. It is assumed that all components are ideal, and all MOSFETs are gated with a fixed duty cycle.

3.3.1 Mode 1: grid charging for odd numbered cells

The charging of battery cells operates in two periods, a magnetising period and a demagnetising period. For the purpose of simplicity, the operation is explained for one odd target cell *B1*. The principles work for all other odd cells. Furthermore, it is assumed that MOSFETs and transformers are ideal components with no loss and ideal coupling factors and that the battery cell is represented by an ideal capacitor and a parasitic resistor *Rcell*.

A. Magnetising period t_0 – t_1

This period starts when *S1* has been turned on. During this time, *S1* is gated on, *S2* in the winding selector is also *ON*, and so are S_{c1} and S_{c2} in the cell selector.

The AC input is converted to a rectified sinusoidal waveform V_{in} by the rectifier. Current flows from the grid into the primary winding of the transformer. Meanwhile, in the secondary side of the transformer, *S3* and *S4* are gated off and there is no current flow in either secondary winding. Therefore, energy is stored in the transformer during the magnetising period. Since the switching frequency of *S1* is much higher than the frequency of the input voltage V_{in}, the voltage across the primary winding can be considered as constant over one switching period. Assuming that the magnetic inductance of the primary winding is *Lm*, with a switching period *T* and fixed duty cycle *D*, the current that flows through the primary winding is:

$$i_{Lm(t)} = \frac{1}{L_m}\int_0^{DT} V_{in}\, dt \tag{3.2}$$

and the peak current in the primary winding at the end of the magnetising period is:

$$I_{peak} = \frac{1}{L_m} \cdot V_{in} \cdot DT \tag{3.3}$$

B. Demagnetising period t1 – t2

At the beginning of this period, *S1* is turned off. At this moment, the polarity of the three windings in the transformer is shown in Figure 3-12.

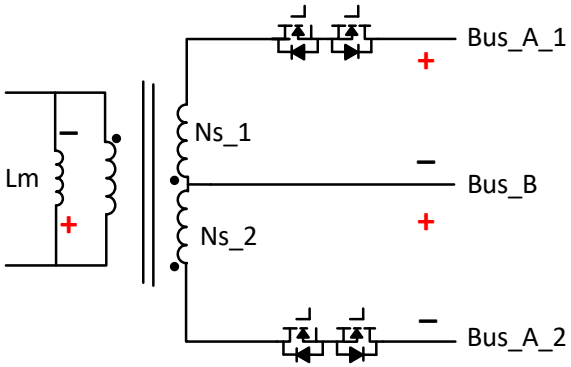


Figure 3- 12 – Polarity for transformer windings in the demagnetising period.

As discussed in section 3.2.3, cells in the battery pack are connected through the cell selector and the winding selector. For odd numbered cells, the positive poles of the battery cells are connected to *Bus_A*, and the negative poles are connected to *Bus_B*, as shown in Figure 3-13(a). While for even numbered cells, it is the exact opposite, as shown in Figure 3-13(b).

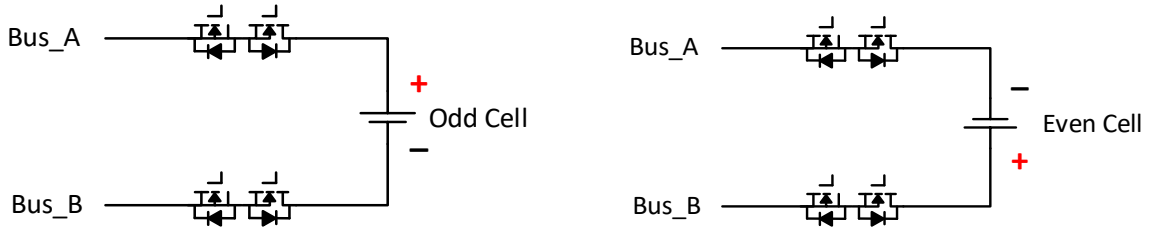


Figure 3- 13 – Polarity of a cell connected to the winding selector for: (a) odd cell; (b) even cell.

Hence, to charge *B1*, the winding selector needs to make sure that Bus_A has a positive output and Bus_B has a negative output. Consequently, *S2* must conduct during this operational mode.

Within this period, the energy stored in the transformer flows from the top secondary winding *Ns_1* to the target cell *B1* through *S2* and the antiparallel diode of *S3* in the winding selector, and Sc1 and Sc2 in the cell selector. The current is gradually decreasing from I_{peak}. In the event that the current reaches zero as the coil

magnetomotive force (MMF) has collapsed, B1 will not start to discharge because S3 in the winding selector is not turned on.

The equivalent circuits for the above operating mode are shown in Figure 3-14 and the idealised operation waveforms in Figure 3-15.

The above operation is based on the example of charging *B1* only. However, the operation can be applied to any odd battery cells, or battery strings starting with an odd numbered cell. Table 3-2 displays all switching states for all possible combinations of target cells within a five-cell pack. Table 3-2 lists the state of MOSFETs for all combinations of target cells for charging odd cells mode.

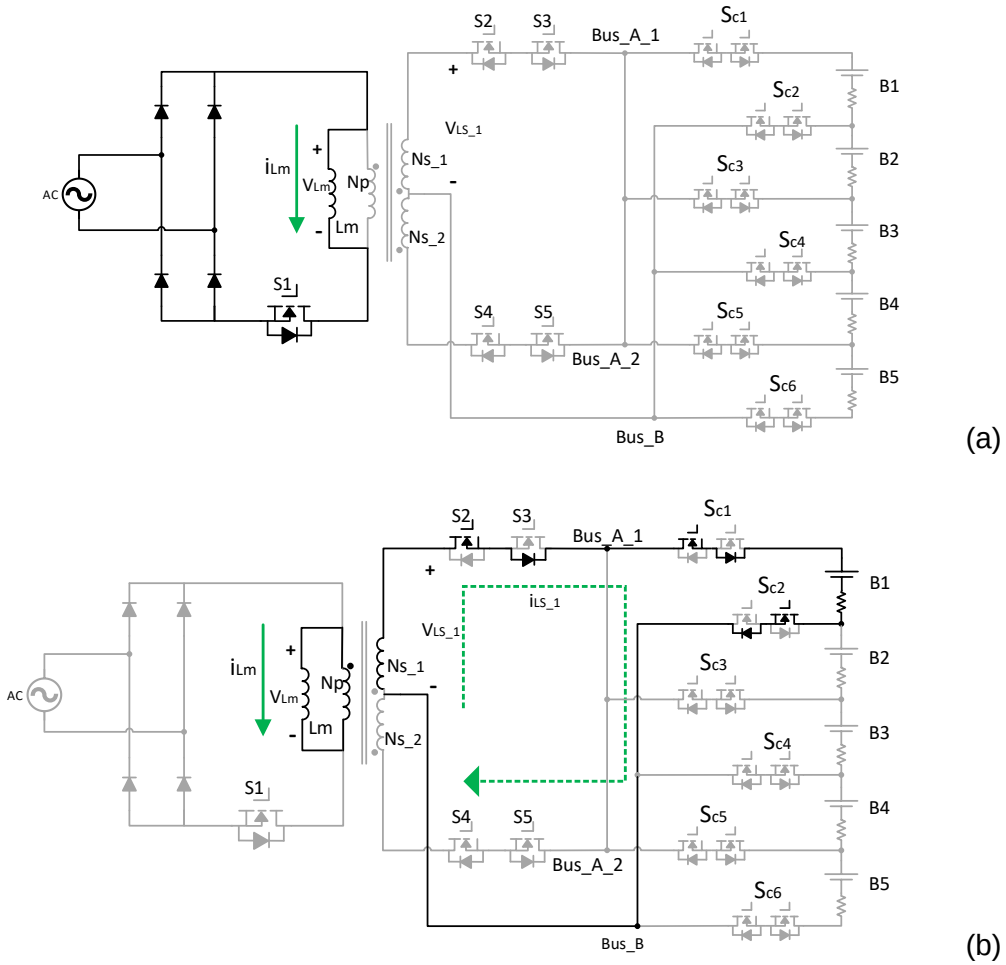


Figure 3- 14 – Equivalent circuits for charging B1 for: (a) magnetising period; (b) demagnetising period.

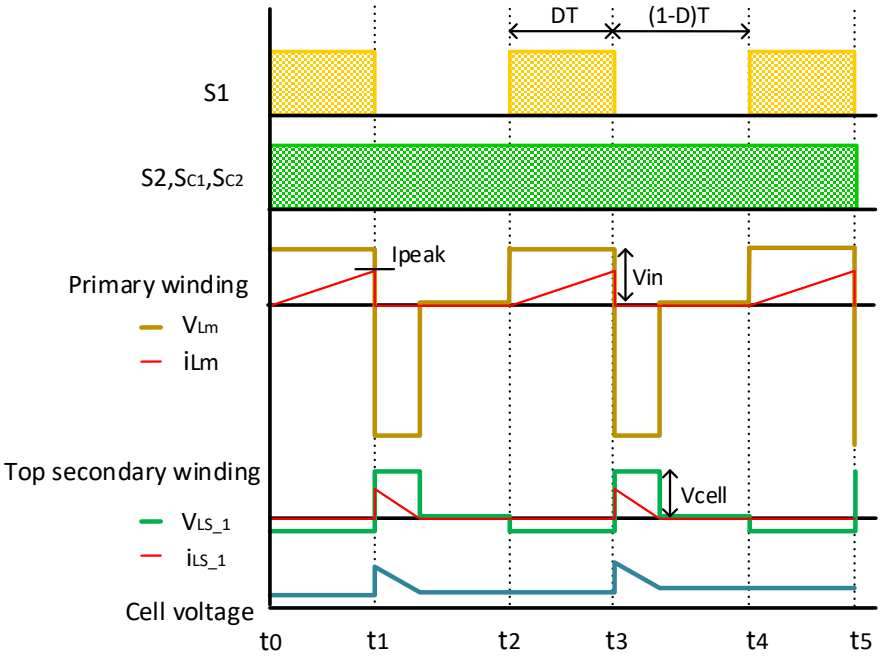


Figure 3- 15 – Predicted waveforms for the circuit when charging B1.

Table 3- 2 – MOSFET states for all cell-combinations when charging odd cells

		Switches										
		S1	S2	S3	S4	S5	Sc1	Sc2	Sc3	Sc4	Sc5	Sc6
Participant Cell(s)	B1	Pulse	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	B3	Pulse	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
	B5	Pulse	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
	B1-B3	Pulse	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
	B3-B5	Pulse	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
	B1-B5	Pulse	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON

3.3.2 Mode 2: grid charging for even numbered cells

The charging of even numbered cells operates in two periods, a magnetising period and a demagnetising period. For the purpose of simplicity, the operation is explained for one odd target cell *B2*.

A. Magnetising period $t_0 – t_1$

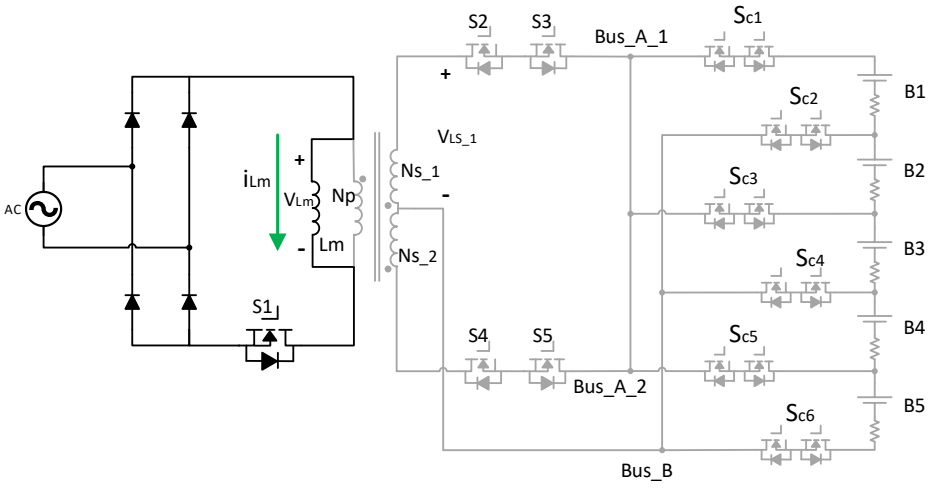
Since the proposed circuit still works as a charger, the circuit operates in the same way as in the magnetising period described for Mode 1.

B. Demagnetising period $t_1 – t_2$

As discussed above, when an even numbered cell is connected to the winding selector, the battery anodes must be connected to *Bus_B* and the cathodes to *Bus_A*, as shown in Figure 3-13. Therefore, to charge an even cell, *Bus_A* and *Bus_B* should be negative and positive respectively, which means that the bottom secondary coil *Ns_2* is requierd in this period. This time, *S5* in the winding selector is conducting.

The target cell is connected to the winding selector when the corresponding switches in the cell selector are conducting. For example, when *B2* is the target cell, then during the demagnetising period, *Sc2* and *Sc3* in the cell selector are conducting, and *S5* in the winding selector provides a closed loop path so that the energy stored in the transformer is released into the target cell *B2*.

The current paths for the scenario above for Mode 2 is shown in Figure 3-16 and the key waveforms are shown in Figure 3-17.



(a)

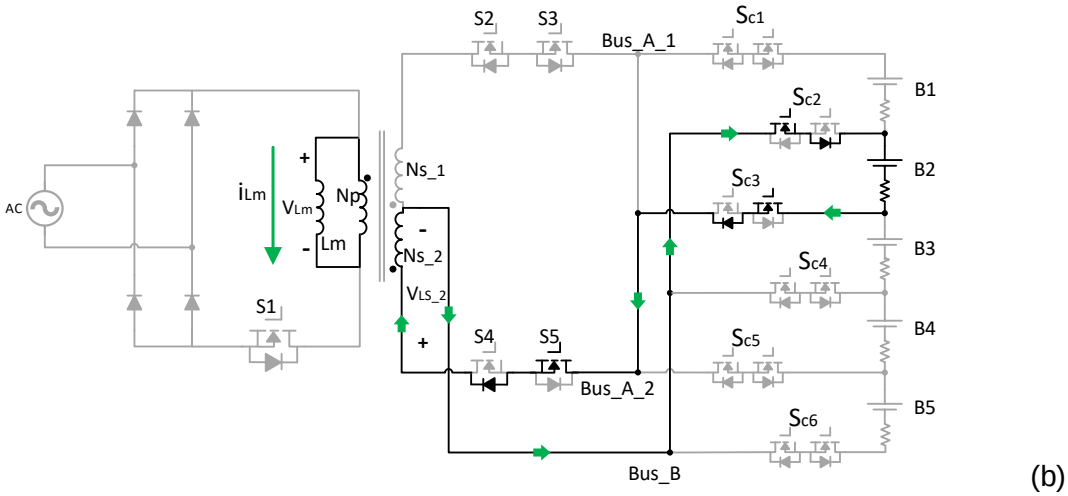


Figure 3- 16 – Equivalent circuit for charging B2 for: (a) magnetising period; (b) demagnetising period.

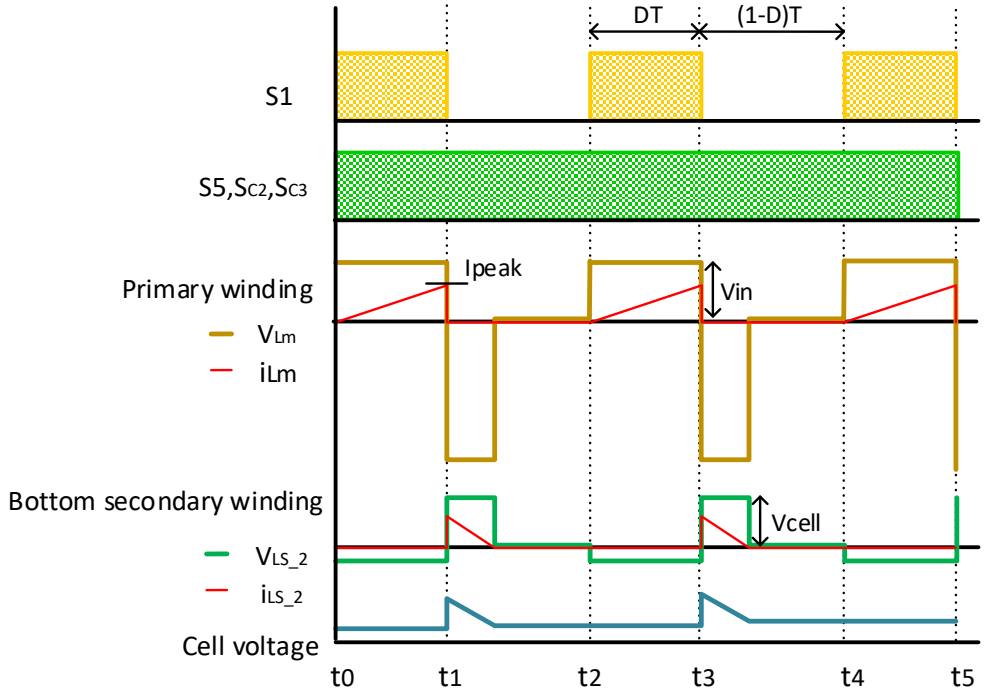


Figure 3- 17 – Predicted waveforms for the circuit when charging B2.

This operating mode can spread to all applications as long as the target cell string starts and ends with even cells. Taking a battery pack with five cells as an example, all combinations of target cells within a five-cell pack are displayed in Table 3-3, including the switching states of all MOSFETs.

Table 3- 3 – MOSFET states for all cell-combinations when charging even cells

		Switches										
		S1	S2	S3	S4	S5	S_{C1}	S_{C2}	S_{C3}	S_{C4}	S_{C5}	S_{C6}
Participant Cell(s)	B2	Pulse	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
	B4	Pulse	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
	B2-B4	Pulse	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF

3.3.3 Mode 3: equalisation from odd cells to odd cells

In the proposed circuit, voltage equalisation is achieved by energy transfer between cells within a battery pack, which means that the equalisation energy is supplied by a source cell (or cells) with higher voltage to a target cell (or cells) with lower voltage. Therefore, the grid and rectifier in the proposed circuit are not involved in this operating mode and therefore *S1* is gated off over the entire period which means that the primary winding of the transformer is always an open circuit.

In the following explanation, it is assumed that B1 has a higher initial voltage than B3. One equalisation cycle comprises three distinct periods: the magnetising, dead-time and demagnetising periods. The operating principles in each of these periods are described in detail as follows.

A. Magnetising period $t_0 – t_1$

This period is the time during which energy being transferred from the source battery B1 to the transformer. B1 is connected to the top secondary winding *Ns_1* through conducting MOSFETs S_{C1} and S_{C2} in the cell selector. Meanwhile, *S3* in the winding selector is turned on, and with the body diode of *S2* provides a path for a current flowing from *B1* to the secondary winding of the transformer. Other MOSFETs in the winding selector and the cell selector are OFF during this period, and thus energy from *B1* is transferred into the transformer. The equivalent circuit for this period is presented in Figure 3-18(a).

When the source battery *B1* is connected to coil *Ns_1*, the voltage of *B1*, V_{B1}, is applied across the coil and the current in the transformer rises. Usually, in a typical model of a transformer, magnetic inductors of secondary windings are referred to the primary side, to make the analysis and calculation easier and clearer. However, in the proposed circuit, coils on the secondary side of the transformer may be used as a primary winding in the magnetising period, and therefore a symbol of a magnetic inductor is added to a secondary coil when needed for circuit analysis. Due to the fact that the magnetising period is short, the voltage of *B1* can be regarded as constant during this time. Assuming that the magnetic inductor for the top secondary winding *Ns_1* is L_{s_1}, and the parasitic resistance of *B1* is R_{B1}, the relationship between the voltages across the coil is V_{Ls_1} and the magnetising current i_{Ls_1} can be expressed as:

$$V_{LS\_1} = L_{ms\_1} \frac{di_{Ls\_1}(t)}{dt} \tag{3.4}$$

$$V_{B1} = L_{ms\_1} \frac{di_{s\_1}(t)}{dt} + R_{B1} i_{Ls_1}(t) \tag{3.5}$$

B. Dead-time t1-t2

Theoretically, at the end of the magnetising period, the demagnetising period should start to ensure the maximum energy transfer between the battery cells. However, simultaneous switching for multiple MOSFETs is impossible in reality due to the fact that turn-on and turn-off times are required.

If the switching times of magnetising and demagnetising overlapped, then there is the risk that the batteries become short-circuited. For example, if S_{C3} is turned on before S_{C1} is turned off, *B1* and *B2* will be shorted via *Bus_A*. The very short overlap will likely cause damage to cells as well as MOSFETs. Consequently, a dead-time period must be added between the magnetising and the demagnetising periods for safety.

Turning off all MOSFETs results in disconnecting the transformer with its stored energy from the rest of the circuit. Consequently, a high voltage spike across all the windings will occur. This means that *S1*, which is connected to the grid, must have a high voltage rating, and therefore the generated voltage spike on the primary winding can be dealt with. The MOSFETS on the low voltage side, however, are selected for low voltage applications as the battery cell voltages are low. In order to protect all low voltage MOSFETs against overvoltage, two pairs of Zener diodes across the two secondary windings have been added, as shown in Figure 3-3. These anti-series connected Zener

diodes will clamp the voltage spike to a maximum value of *Vclamp*. The clamp voltage of the Zener diodes is selected to be slightly lower than the breakdown voltage of the MOSFETs

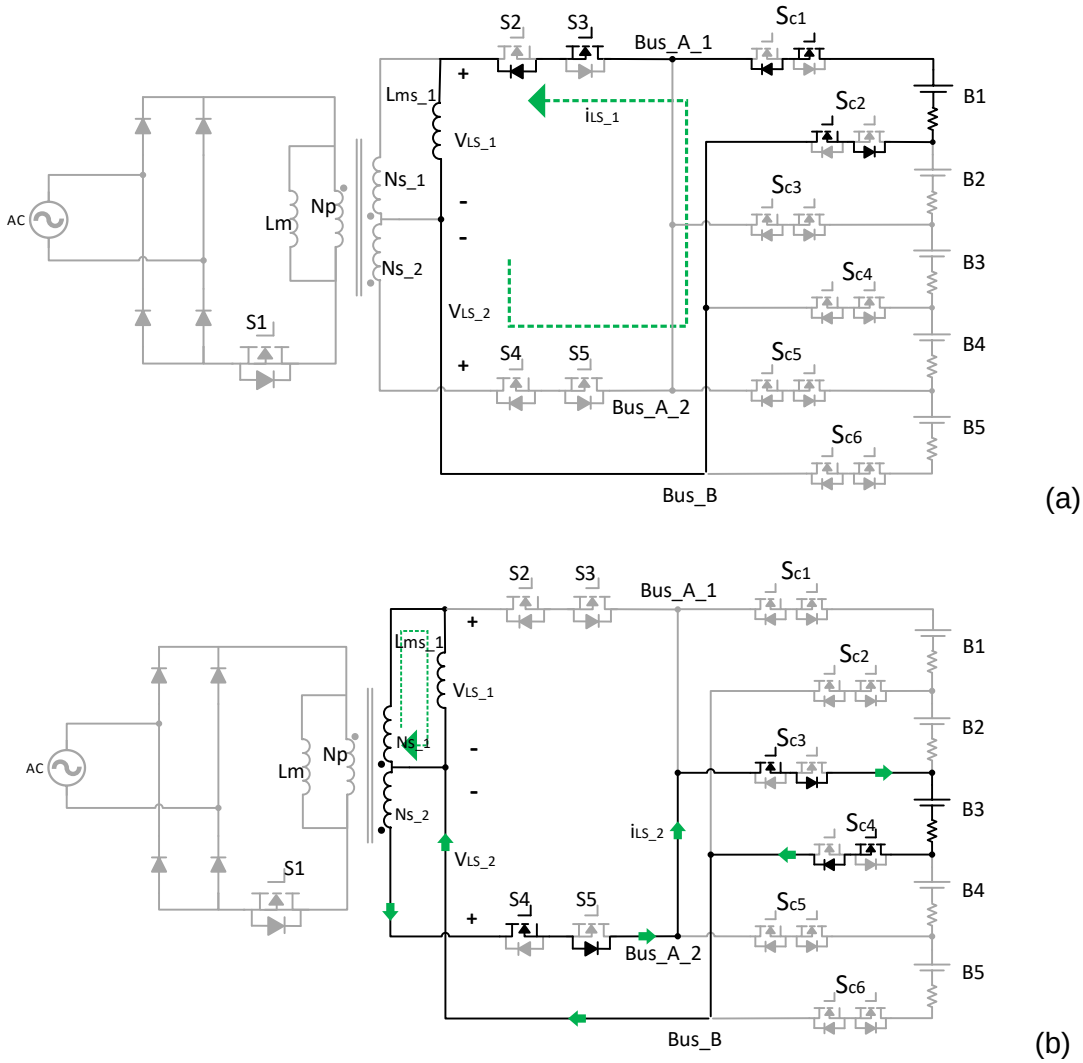


Figure 3- 18 – Equivalent circuits for equalisation from B1 to B3 for: (a) magnetising period; (b) demagnetising period.

The length of the dead-time period depends on the switching characteristics of the MOSFETs, which can be up to one per cent of the switching period. More details on dead-time are presented in Chapter V.

C. Demagnetising period $t_2 – t_3$

The energy kept in the transformer is now released to the target battery *B3*. *S4* in the winding selector and S_{C3}, S_{C4} in the cell selector are gated on so that a demagnetising current i_{LS_2} can flow from the bottom secondary winding through *S4* and the body diode of *S5*, and S_{C3} to the target cell. The peak value of i_{LS_2} occurs at the beginning of this period, and is smaller compared to the peak value of the magnetising current

due to the losses during the dead-time period. The current declines linearly during the demagnetising period until it reaches zero. The transistor *S5* in the winding selector is gated off which stops any current flowing from *B3* to the transformer or other cells. The equivalent circuit of this period is shown in Figure 3-18(b).

The predicted waveforms of coil voltages and currents are presented in Figure 3-19.

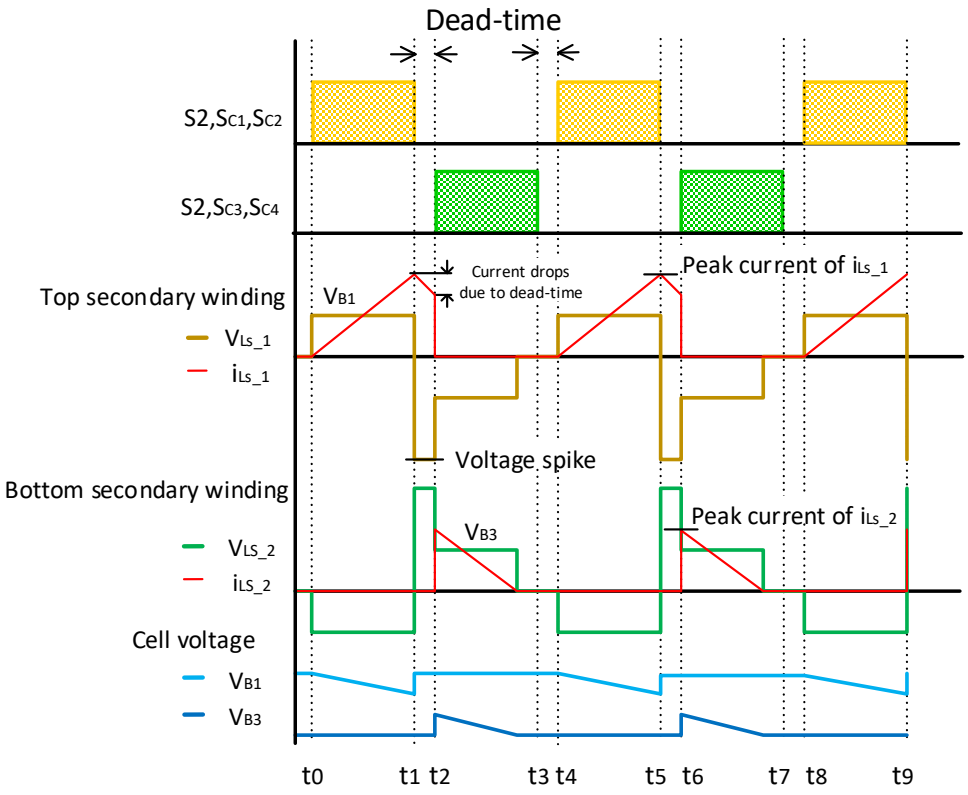


Figure 3- 19 – Predicted waveforms for the circuit when equalisation from B1 to B3.

It is important to make sure that the demagnetising current falls back to zero before the next magnetising period begins. Otherwise, the flux in the transformer will build up over every switching event, which will cause the saturation of the magnetic core. The duty cycle of the pulse signal determines whether or not the demagnetising current can go back to zero in time. Considering that all of the switches involved are ideal, the critical duty cycle can be calculated as:

$$I_{Ls\_1\_peak} = \frac{V_{B1} \times DT}{L_{ms\_1}} \tag{3.6}$$

$$V_{B3} = L_{ms\_1} \times \frac{I_{Ls\_1\_peak}}{(1-D)T} \tag{3.7}$$

Substituting $I_{Ls\_1\_peak}$ into equation (3.7), the critical value of D can be derived as:

$$D_c = \frac{V_{B3}}{V_{B1} + V_{B3}} = \frac{1}{\frac{V_{B1}}{V_{B3}} + 1} \tag{3.8}$$

Equation (3.8) indicates that the critical duty cycle is determined by the voltages of the source and target cells, and the bigger the voltage gap between them, the smaller the critical duty cycle. For example, the initial voltages of B1 and B3 are 4V and 2V respectively. The gap is 2V and the critical duty cycle can be calculated as $D_c = 2V/(2V + 4V) = 0.33$. After the voltage balancing has been operated for a while, the voltages of B1 and B3 reach 3.5V and 2.5V respectively. The voltage gap is reduced to 1V, and the critical duty cycle needs to be updated according to the new voltages as $D_c' = 2.5V/(3.5V + 2.5V) = 0.416$. The change in the duty cycle is because of the change in the demagnetising period. The rate of which the current falls in the demagnetising period is determined by the voltage across the winding, which is determined by the voltage of the target source B3. When B3 has lower voltage, the time it takes for the demagnetising current to drop to zero is longer, and thus the critical duty cycle is smaller.

Equation (3.8) can be used to design a duty cycle controller for battery equalisation. The controller generates pulse signals with fixed frequency but varying duty cycles depending on the voltages of the source and target cells. However, in practice, since there are some losses in the circuit, including dead-time losses, losses generated by leakage from the inductor, and the voltage drops of MOSFETs, the peak value of the demagnetising current is always smaller than $I_{Ls\_1\_peak}$. Therefore, it is also acceptable for the duty cycle to be set to 0.5 without taking V_{B1} and V_{B3} into consideration.

This operating mode has been explained for the transfer of energy from *B1* to *B3*. However, the model applies for voltage equalisation between all odd numbered cells (or strings that start with an odd cell). Possible combinations of source cells and target cells have been listed in Table 3-4 for a five-cell battery pack.

Table 3- 4 – MOSFET states for all cell-combinations for equalisation between odd cells

		Switches										
		S1	S2	S3	S4	S5	S_{C1}	S_{C2}	S_{C4}	S_{C4}	S_{C5}	S_{C6}
Participant Cells	B1	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	B3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
Participant Cells	B1	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
Participant Cells	B3	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
	B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
Participant Cells	B1-B3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
	B3-B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

3.3.4 Mode 4: equalisation from even cells to even cells

The operating principle of this mode is similar to that for Mode 3, since the winding and cell selectors have been designed with a symmetrical structure for individual cells. Hence, the following explanation is not as detailed as before, but the differences between them have been emphasized. As an example of this operating mode, voltage equalization occurs from *B2* to *B4*.

A. Magnetising period $t_0 – t_1$

In this period, the source cell *B2* is connected to the bottom coil *Ns_2*. Since an even numbered cell is connected to the transformer, the battery anode is connected to *Bus_B* and the battery cathode is connected to *Bus_A*. A magnetising current i_{Ls_2} flows from source cell *B2*, via the gated-on S_{C2} in the cell selector, to coil *Ns_2*. The

MOSFETs *S4* and *SC3* are also conducting to provide a return path for the current to B2. As in the operating principle of a flyback converter, during this period the energy is stored in the air-gap of the magnetic core. The polarity of the two secondary coils and the current flow path are indicated in Figure 3-20(a).

B. Deadtime t1-t2

A deadtime has been set between the magnetising period and the demagnetising period to protect the circuit from short circuit. Thus, all MOSFETs are off during this period.

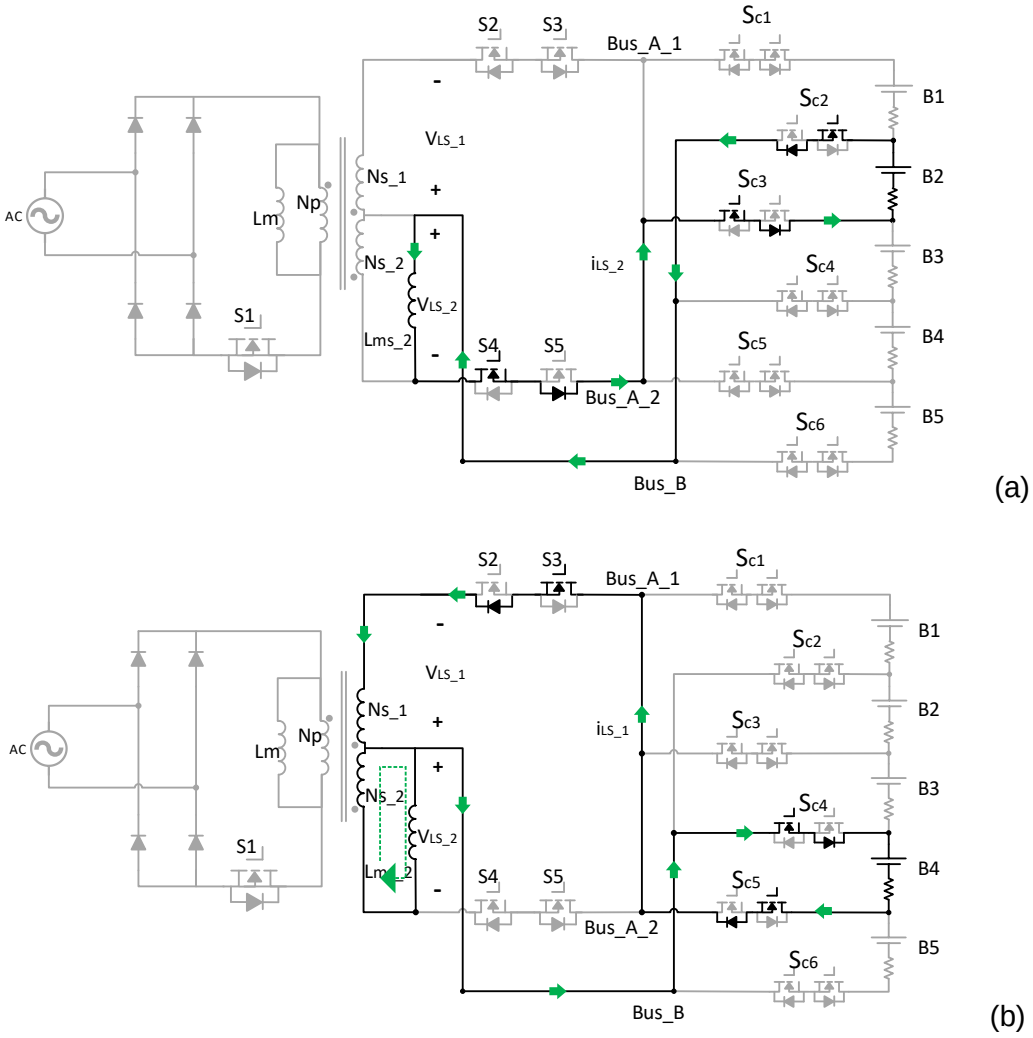


Figure 3- 20 – Equivalent circuits for equalisation from B2 to B4 for: (a) magnetising period; (b) demagnetising period.

C. Demagnetising period t2 – t3

The target battery cell *B4* is connected to the top secondary coil *Ns_1* by activating *SC4* and *SC5* in the cell selector and *S3* in the winding selector. Energy is released from the

transformer to *B4* before the next switching period starts. The current path for this period is shown in Figure 3-20(b).

The predicted voltage and current waveforms of the windings and the cells in this operating mode are shown in Figure 3-21. The discussion about calculating the critical duty cycle in the previous section (see Equation (3.8)) can also be applied to this operating mode as well.

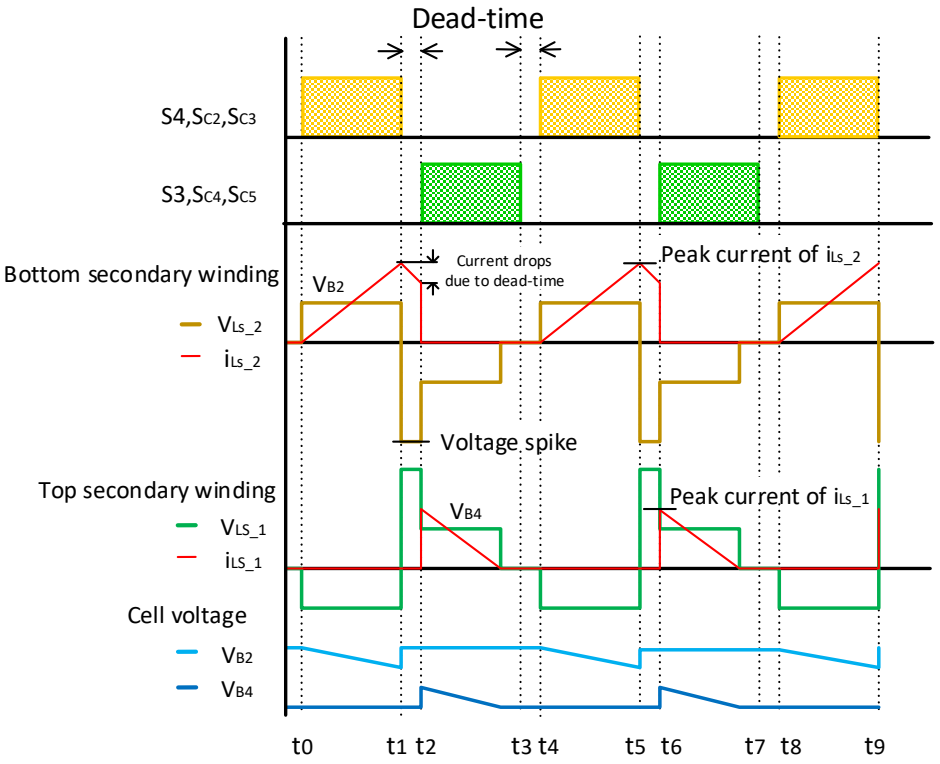


Figure 3- 21 – Predicted waveforms for the circuit when equalisation from B2 to B4.

This operating principle is suitable when the circuit is working to provide voltage equalisation between even numbered cells, or cell packs which start with an even cell. However, as explained above in section 3.2.4, irrespective of whether in battery charging or equalisation mode, the number of cells in the battery string involved has to be odd. Therefore, for a battery pack which contains of five cells, equalisation between *B2* and *B4* is the only possibility in this operating mode. Thus, Table 3-5 describes the states of the MOSFETs in the circuit when it is engaged in equalisation between *B2* and *B4*.

Table 3- 5 – MOSFETs states for all cell-combinations when equalisation between even cells

		Switches										
		S1	S2	S3	S4	S5	S_{C1}	S_{C2}	S_{C3}	S_{C4}	S_{C5}	S_{C6}
Participant Cells	B2	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
	B4	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF

When the circuit works in Modes 3 or 4, it operates like a multi-secondary winding transformer equalisation circuit, as introduced in section 2.5.5. However, when the equalization is between an odd cell and an even cell, the operating principle of the circuit will be similar to a buck-boost converter-based equaliser. Details of this case are explained in the following sections.

3.3.5 Mode 5: equalisation between odd cells and even cells

The explanation of this operating mode is based on an example of equalisation from *B1* to *B2*, assuming that *B1* has a higher initial voltage than *B2*. Since there is only one secondary coil involved, it is regarded as an inductor rather than a winding in a transformer. The balancing process in Mode 5 can be divided into 3 periods: the inductor charging period, the dead-time, and the inductor discharging period.

A. Inductor charging period t_0-t_1

During this time *B1* is connected to the top secondary winding N_{s_1} with S_{C1} and S_{C2} in the cell selector gated on. *S3* in the winding selector is also conducting, to provide a current flow path from *B1* to charge the transformer. Within this period, the coil plays a role as an inductive energy storage device. If the equivalent inductance of coil N_{s_1} is L_{ms_1}, and the inductor charging period lasts DT, then the peak value of this current i_{Ls_1} is:

$$I_{Ls\_1\_peak} = \frac{1}{L_{ms\_1}} \cdot V_{B1} \cdot DT \tag{3.9}$$

B. Dead-time t_1 – t_2

As discussed in section 3.3.3, any overlapping of the conducting of MOSFETs may have an impact on the battery cells and transistors. This is also true in this operating mode, hence, a dead-time is needed.

C. Inductor discharging period t2-t3

In the cell selector, *SC1* is gated off and *SC3* is gated on, and therefore the target cell *B2* is connected to the winding selector. *S3* continues conducting so that the energy stored in the winding *Ns_1* can be released to *B2*. This is the same as the principle that has been discussed in Mode 3, where the discharging current should fall to zero before the next period starts.

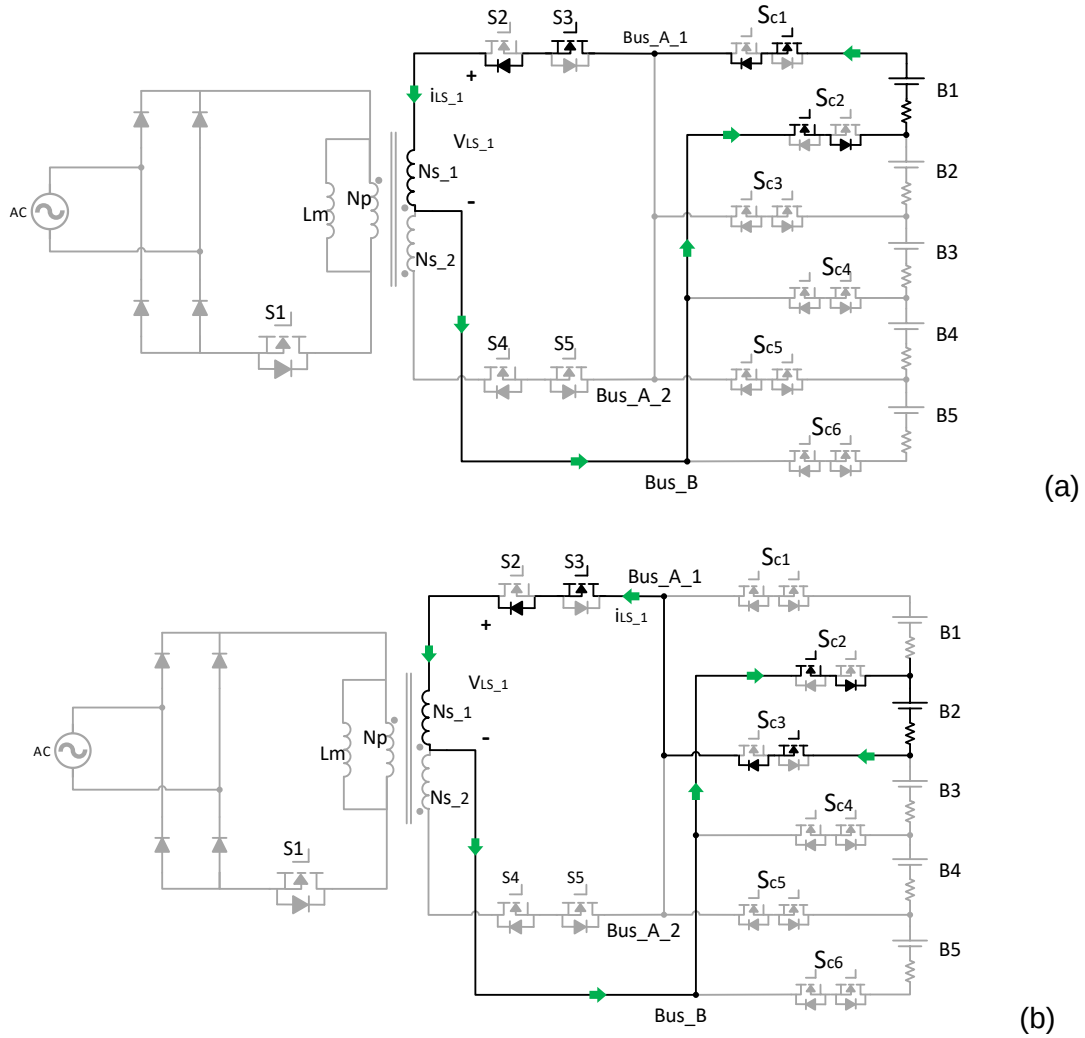


Figure 3- 22 – Equivalent circuits for equalisation from B1 to B2 for: (a) magnetising period; (b) demagnetising period.

The discussion about calculating the critical duty cycle in the last section (see Equation (3.8)) can also be applied to this operating mode as well. The current flow paths in the

inductor charging and discharging periods are shown in Figure3-22, along with the predicted key waveforms in Figure 3-23.

Table 3-6 shows the combination of participant cells in equalisation between odd and even cell mode for a battery pack of five cells. It also describes the states of the MOSFETs under each circumstance.

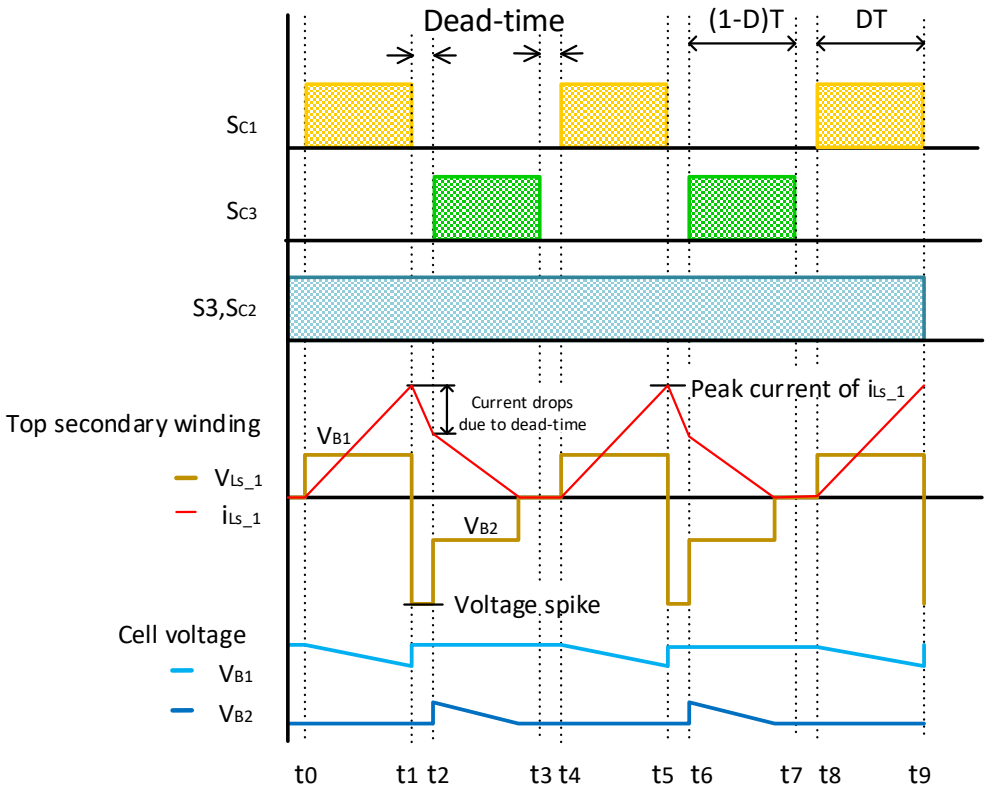


Figure 3- 23 – Predicted waveforms for the circuit when equalisation from B1 to B2.

Table 3- 6 – MOSFETs states for all cell-combinations when equalisation between odd cells and even cells

		Switches										
		S1	S2	S3	S4	S5	SC1	SC2	SC3	SC4	SC5	SC6
Participant Cells	B1	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	B2	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF

Participant Cells	B1	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	B4	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF
Participant Cells	B2	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
	B3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
Participant Cells	B2	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
	B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
Participant Cells	B3	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
	B4	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF
Participant Cells	B4	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
	B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
Participant Cells	B1-B3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
	B2-B4	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
Participant Cells	B2-B4	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
	B3-B5	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

In section 3.3, the operating principles of all modes have been demonstrated in detail. In summary, the proposed converter operates in five modes:

When the car is static and charging from the grid, two modes can take place:

1) Grid charging for an odd numbered cell, or a battery string starting with an odd numbered cell;
2) Grid charging for an even numbered cell, or a battery string starting with an even numbered cell;

When the car is not connected to the grid and voltage balancing between cells is required, three operational modes can be activated:

3) Equalization from an odd numbered cell to an odd numbered cell, or from a source string which starts with an odd numbered cell to a target string which starts with an odd numbered cell;
4) Equalization from an even numbered cell to an even numbered cell, or from a source string which starts with an even numbered cell to a target string which starts with an even numbered cell;
5) Equalization between an odd numbered cell and an even numbered cell, or between a source string which starts with an odd numbered cell and a target string which starts with an even numbered cell.

Compared to the conventional voltage balancing circuit, the proposed circuit requires more switching devices, which will increase the cost, as well as the difficulty of control. Not only the source cells and the target cells but also the involved winding need to be selected in every single equalisation period.

3.4 RCD snubber circuit design for flyback converter

Ideally, in a flyback converter, the drain-source voltage V_{ds} across the MOSFET is a square waveform alternating between zero and the supply voltage V_{in}. However, in practice, turning off the MOSFET causes a high voltage spike across the drain and the source of the MOSFET because of the leakage of inductance within the transformer. Figure 3-24 presents a flyback converter with parasitic components and waveforms when operating in discontinuous conduction mode (DCM). In Figure 3-24, L_{lk1} and L_{lk2} represent the leakage inductance for the primary and secondary windings of the transformer respectively. C_{oss} is the output capacitance of the MOSFET.

When the main switch is turned off, the current through the leakage inductor L_{lk1} is interrupted, resulting in a high-surge voltage occurring to the drain of the MOSFET which may damage the device. Besides, an oscillating occurs between L_{lk1} and C_{oss}, generating high frequency voltage and current ringing in i_d and V_{ds}, as shown in Figure-

24(b). Once the current in the secondary winding has fallen to zero, another resonance appears between the magnetic inductance *Lm* and *Coss* [99].

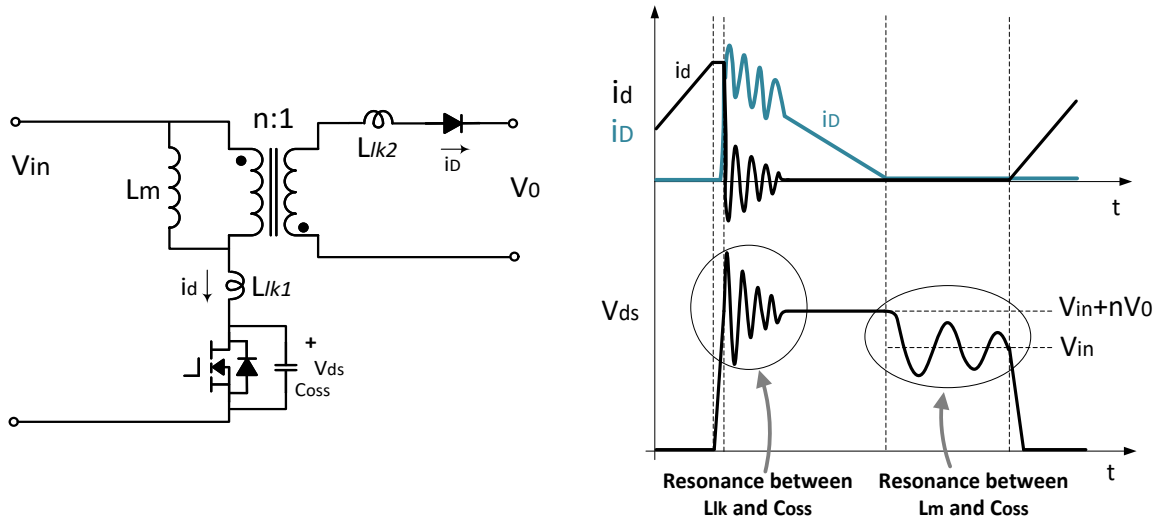


Figure 3- 24 – Flyback converter: (a) scheme with parasitic components; (b) DCM operation.

A snubber circuit on the primary winding of the flyback converter is used to absorb the energy that is stored in the leakage inductor, and to suppress the voltage spike so as to protect the MOSFET. The RCD snubber is a typical snubber circuit scheme, which consists of a snubber capacitor Csn, a snubber resistor Rsn, and a fast recovery snubber diode Dsn [89, 100-104]. Figure 3-25 (a) shows a flyback converter with a RCD snubber, with operating waveforms shown in Figure 3-25 (b).

When the MOSFET is turned off and the voltage across the MOSFET *Vds* exceeds *Vin+nV0*, the snubber diode *Dsn* conducts and a current *isn* flows from the primary winding to *Csn*. Assuming that the snubber capacitor is large enough so that the voltage of *Csn* is constant during a switching period, therefore the voltage across the leakage inductor becomes *Vsn-nV0*, where *nV0* is the reflected voltage across the primary winding. The time *ts* in Figure 3-25 (b) is obtained using Equation (3.10) in which *Ipeak* is the peak current in the primary winding when the MOSFET is gated on.

$$t_s = \frac{1}{V_{sn} - nV_0} \cdot L_{lk1} \cdot I_{peak} \tag{3.10}$$

And during time *ts*, the power dissipated by the snubber circuit is calculated as:

$$P_{sn} = V_{sn} \frac{I_{peak}}{2} t_s f_s = \frac{1}{2} L_{lk1} {I_{peak}}^2 \frac{V_{sn}}{V_{sn} - nV_0} f_s \tag{3.11}$$

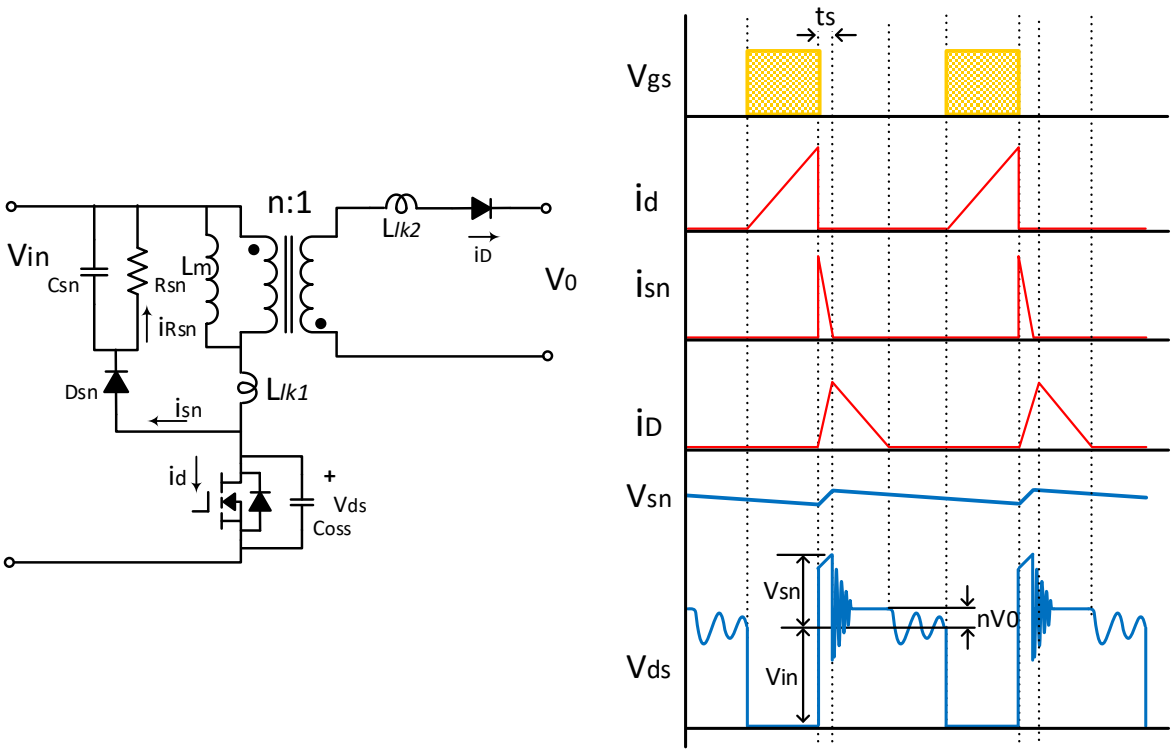


Figure 3- 25 – Flyback converter assembled with RCD snubber: (a) scheme with parasitic components; (b) DCM operation.

Vsn in the above equations stands for the clamped voltage. Usually, this clamped voltage could be set at 2 to 2.5 times of *nV0*, as long as with the maximum input *Vin_max*, *Vsn*+*Vin_max* is within the rated *VDS* of the MOSFET when considering a margin of voltage to protect the MOSFET as well; that is:

$$V_{sn} + V_{in\_max} < 0.8V_{DS} \tag{3.12}$$

Since the power *Psn* has eventually been consumed by the snubber resistor *Rsn*, the resistance of the snubber resistor is obtained by [99, 105]

$$R_{sn} = \frac{{V_{sn}}^2}{P_{sn}} = \frac{{V_{sn}}^2}{\frac{1}{2} L_{lk1} {I_{peak}}^2 \frac{V_{sn}}{V_{sn} - nV_0} f_s} \tag{3.13}$$

From Equation (3.11), it can be deduced that the dissipated power is inversely proportional to the clamped voltage *Vsn*, and meanwhile Equation (3.13) indicates that the value of snubber resistor *Rsn* is in direct proportion to *Vsn*. In other words, a larger snubber resistor will clamp the voltage across the MOSFET at a higher voltage level, and the power dissipation will be low; however, the MOSFET must withstand a higher voltage stress. On the other hand, a smaller snubber resistor will cause more power dissipation in the snubber circuit, but it will clamp the voltage over the MOSFET earlier and thus less voltage stress will ensure.

The value of the snubber capacitor is not crucial in determining the clamped voltage; however, it determines the voltage ripple of the snubber circuit voltage:

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s} \tag{3.14}$$

In general, voltage ripple of five to ten per cent is considered acceptable [99, 105]. Therefore, if the voltage ripple is 5% of the voltage, the value of the snubber capacitor can be expressed as:

$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn}} \cdot \frac{1}{R_{sn} f_s} = \frac{1}{0.05} \cdot \frac{1}{R_{sn} f_s} \tag{3.15}$$

Figure 3-26 presents the proposed circuit assembled with the RCD snubber circuit on the primary coil of the transformer.

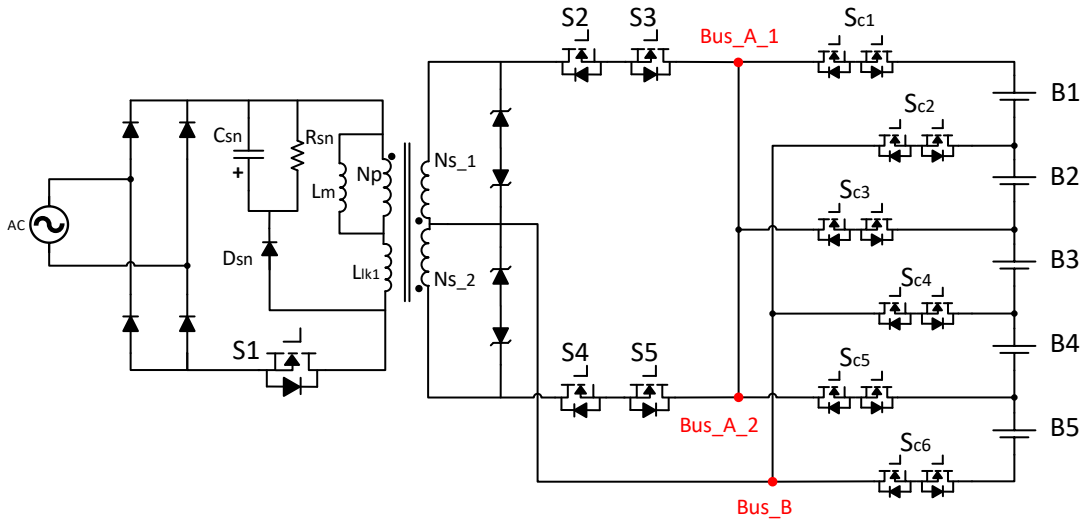


Figure 3- 26 – Proposed battery charging and equalisation circuit enhanced with RCD snubber.

It is worth noting that, when the circuit is operating in Modes 3, 4 and 5 (equalisation modes) with transistor *S1* off, the snubber circuit is causing energy dissipation due to the induced voltage from the secondary coils. For instance, during the magnetising period, in which energy is released from the battery *B1* to the coil *Ns_1*, the polarity of *Ns_1* and *Np* are reversed due to the back-coupling of the two coils. This arrangement causes the snubber diode *Dsn* to conduct as forward voltage is applied across this diode; hence, there is a current flowing through the snubber resistor *Rsn* with energy dissipation. However, due to the large value of *Rsn*, the level of energy dissipation on the snubber can be neglected. Details of the calculation of power dissipation are given later in this chapter.

So far, the structure of the proposed charging and equalisation circuit with an auxiliary RCD snubber circuit has been introduced, as well as the operational principles for the circuit. The following section shows the operation of the circuit with the help of simulation.

3.5 Development of the simulation model

This section introduces the network model used in the simulation which was built up based on the proposed circuit using the software PLECS. PLECS is the tool of choice for high-speed simulations of power electronic systems. With its comprehensive component library covers the electrical, as well as magnetic, thermal and mechanical aspects of power conversion systems and their control, PLECS facilitates the modelling and simulation of complete systems.

As the transformer is the key component in the proposed circuit, Figure 3-27 shows the transformer model used in the circuit, including its parasitic components. The turns-ratio between the primary winding and the two secondary windings is described in Equation (3.1).

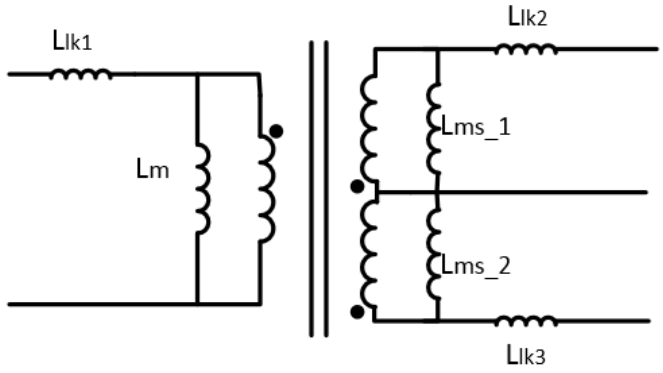


Figure 3- 27 – The transformer model.

In a standard equivalent model of a transformer, the magnetising and leakage inductors of the secondary windings are referred to the primary winding which makes the analysis and calculations easier. However, when the circuit operates as a voltage equaliser, the secondary windings can be utilised as a primary coil in the magnetising period. Therefore, in Figure 3-27, magnetic inductors for all the three windings in the transformer are displayed separately. The value of each magnetic inductor determines the peak current.

For a 1kW system with an input voltage of 230V, the input current can be worked out as $1kW/230V = 4.3A$. Assuming that the frequency and duty cycle of the pulse signal

to S1 are 20kHz and 0.4 respectively (to make sure that the converter operates in DCM), and since the current in the transformer increases linearly during the magnetising period, the maximum peak current in the primary winding in the transformer is:

$$I_{peak} = 2\frac{I_{rms}}{D} = 2 \times \frac{4.3A}{0.4} = 21.5A \tag{3.16}$$

With the desired value of the peak current, the magnetic inductor of the primary winding can be calculated:

$$L_m = \frac{V_{peak} \cdot DT}{I_{peak}} = \frac{230V \times \sqrt{2} \times 0.4 \times 50 \times 10^{-6}}{21.5A} = 302\mu H \tag{3.17}$$

To reduce energy losses in the transformer, the leakage inductance of each winding needs to be as small as possible [106, 107]. Leakage inductance can be reduced by improving the coupling factor between coils. In practice, applying the winding interleaving technique can reduce leakage inductance during transformer manufacture. In this simulation model, the magnetic inductors for two secondary windings are chosen based on the transformer used in the experimental test, and values of leakage inductance are selected to be 5% of the corresponding magnetic inductance. The parameters in the model of the transformer are listed in Table 3-7.

Table 3- 7 – Parameters of the transformer model

Parameters	Values
Turns-ratio	11:1:1
Lm	350 μH
Lms_1, Lms_2	4.2 μH
Llk1	17.5 μH
Llk2, Llk3	0.21 μH

The values of *Csn* and *Rsn* in the snubber circuit can be calculated using the equations described in section 3.4. At the full-load condition for charging five cells, the induced voltage across the primary winding, *nV0,* is $11 \times 4\text{V} \times 5 = 220\text{V}$. The clamped voltage

is set to be 2.5 times the induced voltage, and thus the voltage spike across the MOSFET can be calculated as:

$$V_{ds\_clamp} = V_{in\_max} + V_{sn} = \sqrt{2} \times 230V + 2.5 \times 220V = 875V \quad (3.18)$$

With the help of equations (3.13) and (3.15), the values of C_{sn} and R_{sn} can be calculated, and are set in the simulation at 2.6kΩ and 380pF respectively.

The battery model used in this simulation is composed of a series-connected capacitor and resistor, in which the capacitance of the capacitor stands for the battery capacity, while the resistor reflects the parasitic resistance of a battery. The capacitance in the battery model is set at 25F. A capacitance of this size has been chosen in order to observe changes in battery voltage within a reasonable simulation time. The parameters of the proposed circuit in the simulation model are presented in Table 3-8.

Table 3- 8 – Parameters of the proposed circuit in the simulation model

	Parameters	Values
Rectifier	Voltage drop per diode	0.55V
S1	Drain-to-source voltage, Vds	1200V
	On resistance, Ron	35mΩ
	Output capacitance, Coss	10nF
S2-S5, SC1-SC6	Drain-to-source voltage, Vds	40
	On resistance Ron	0.55mΩ
Transformer	See Table 3-7	
Zener diode	Zener voltage	33V
Battery	Capacitance	25F
	Parasitic resistance	0.011Ω
RCD snubber	Capacitor	15.56pF
	Resistor	64.82kΩ

3.6 Verification of simulations under open loop control

Simulations in this section are accomplished with PLECS, and the simulation results are displayed to assess the performance of the circuit.

3.6.1 Simulation of grid charging of battery cells

In this simulation, only one cell *B1* is charged. The initial voltage of B1 is 2.5V. *S1* is gated by a square wave signal with a duty cycle of 0.1. *S2* in the winding selector and *SC1* and *SC2* in the cell selector are all turned on throughout the time *B1* is charging. Figure 3-28 presents the gate drive signals applied to all MOSFETs involved, and the key voltage and current waveforms, as well as the voltage rise across *B1* during the simulation period of 2 seconds.

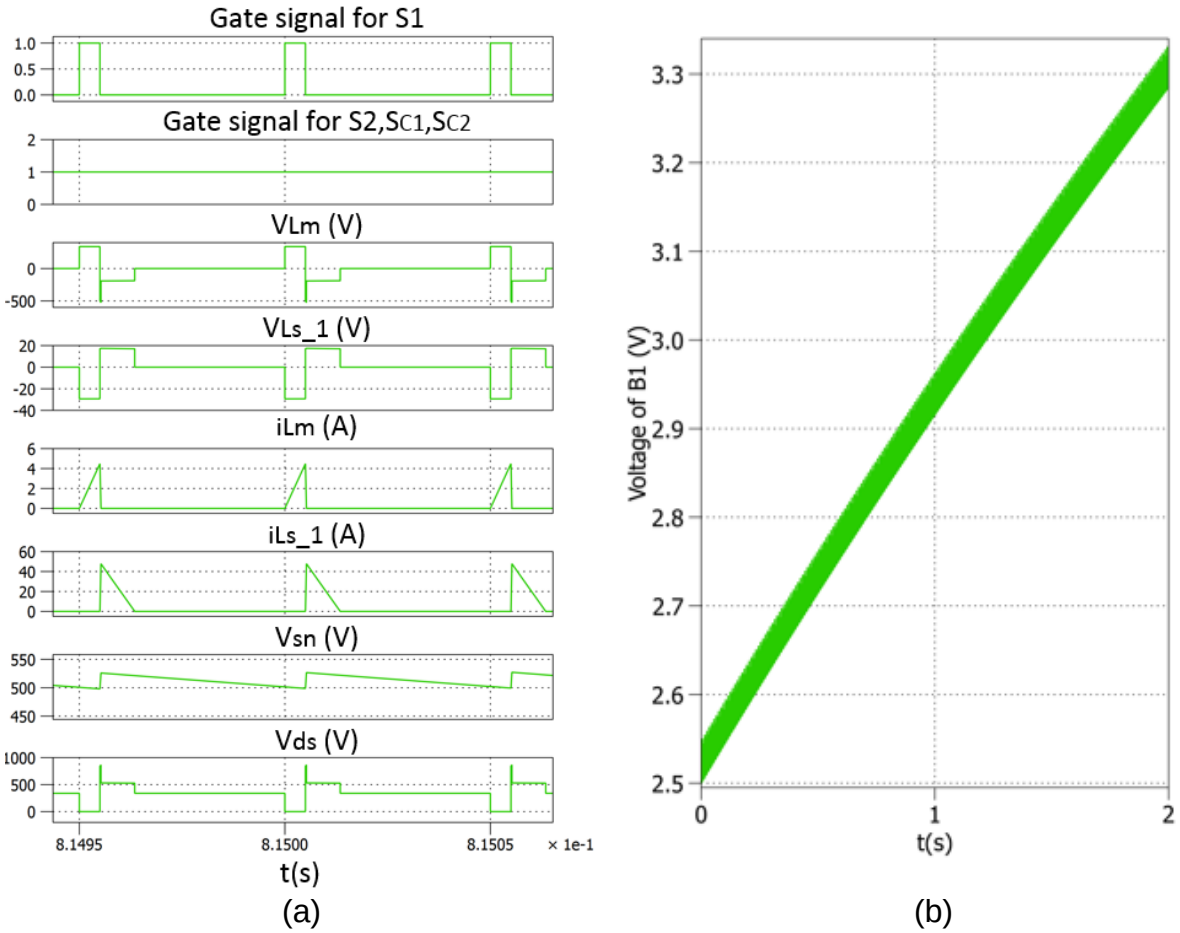


Figure 3- 28 – Simulation waveforms for the proposed circuit when charging B1.

The losses when the circuit operates in the grid charging mode is mainly the losses caused by the leakage inductance of the flyback converter. According to Equation (3.11), losses on the leakage inductance would be dissipated by the snubber resistance and the losses can be calculated.

$$P_{sn} = \frac{1}{2} L_{lk1} {I_{peak}}^2 \frac{V_{sn}}{V_{sn} - nV_0} f_s = 4.67W \quad (3.19)$$

Figure 3-28(b) shows that the voltage of cell B1 increased from 2.5V to 3.27V within 2 seconds. The output power of the circuit is calculated in equation (3.20). While, the input power of the circuit can be calculated based on the input voltage and current shown in Figure 3-28 (a), as in equation (3.21).

$$P_{out} = \frac{\frac{1}{2} C V_2^2 - \frac{1}{2} C V_0^2}{\mathrm{T}} = \frac{\frac{1}{2} \times 25F \times (3.28V^2 - 2.5V^2)}{2\mathrm{s}} = 44.42\mathrm{W} \quad (3.20)$$

$$P_{in} = V_{in} \cdot I_{in} = 230V \times 4.3A \times 0.5 \times 0.1 = 49.45W \quad (3.21)$$

The efficiency of the circuit can be worked out:

$$\eta_1 = \frac{P_{out}}{P_{in}} = 89.8\% \quad (3.22)$$

The charging current shown in Figure 3-28 is a pulsating current. Compared to traditional battery charging circuits that provide constant DC charging current, the proposed circuit essentially has only half time to charge, due to the magnetising and the de-magnetising processes. Therefore, the charging speed is relatively lower. However, the pulsating charging helps to slow down the increases of the battery impedance parameter values, and further contributes to extend the life span of batteries [108-111]. It is because that the relaxation times in between charge current pulses allows time for the Li^+ to successfully intercalate and helps to prevent dendrite formation [112]. Besides, pulse current can be controlled preciously by controlling the pulse duty cycle. Hence, it can be used when cells voltage reaches the threshold following the constant-current charging stage, thereby decreasing the total charge time for the rechargeable battery comparing to the constant-current-constant-voltage charging [113, 114]. However, pulse charging of lithium-ion batteries needs a preciously control system to calculated the pulse width and duty cycle based on the SOC of the cells, and it has not been deeply studied in this thesis.

Apart from charging battery cells, the proposed circuit is able to narrow the voltage gap within cells by charging individual battery cells that have a lower voltage than others. For example, in a battery pack with five cells, the initial voltage of cells *B1-B4* are 3.6V, 3.3V, 3.2V, 3.1V, and 2.5V respectively. The whole charging process can be divided into two parts. In the first part, the batteries in string *B1-B5* are charged. Since all cells

are connected in series, they are charged by the same current. Thus the voltage of all cells rises at the same rate. When B1 reaches the maximum voltage of 4V, that of B5 is only 3V at this point in time. To minimise the voltage gap between *B5* and the other four cells, the controller decides to charge only B5 in stage two. The cell selector switches are changed so that only B5 is charged, as shown in Figure 3-29, until the voltage of B5 is close to the other cell voltages. Figure 3-29 shows this charging example, with the states of the MOSFETs involved.

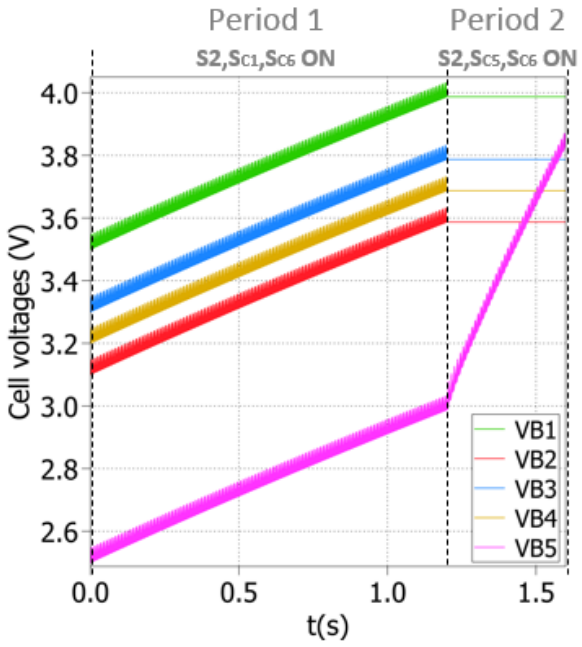


Figure 3- 29 – Cell voltages for B1-B5 when charging five cells in two steps.

3.6.2 Simulations of battery voltage equalisation

As described in section 3.3, the circuit operates as a flyback converter if both the source and target cells are either odd or even. The following example is for voltage equalisation with two odd numbered cells.

The initial voltages of cells *B1* and *B3* are 3.8V and 3.2V respectively. Since *B1* has a higher voltage than *B3*, energy must be transferred from *B1* to *B3*. In Figure 3-30 (a), the top two waveforms represent the gate signals for *S3*, *Sc1* and *Sc2*, and the gate signals for *S4*, *Sc3* and *Sc4*. The next two waveforms in this figure show the voltages across *Ns_1* and *Ns_2*, the currents through *Ns_1* and *Ns_2*, and the voltages across *B1* and *B3*. The final three waveforms present the voltage across the transformer and the snubber voltage and the current in the snubber resistor.

The waveform shows that the peak current during the magnetising period is higher than the peak value during the demagnetising period due to the dead-time period. In

this simulation model, a dead-time of 1μs has been added between the two groups of transistors that need to be switched. During this period, the voltage across the two coils is clamped at the Zener voltage. The current in *Ns_1* is reduced from the peak value of 12.1A to 8.7A during the dead-time. The power loss can be expressed as:

$$P_{dead-time} = \frac{1}{2} L_{s_1} (12.1^2 - 8.7^2) = 0.28 \times 10^{-3} W \tag{3.23}$$

When *S3*, *SC1* and *SC2* are turned on, the flyback voltage on the primary winding is calculated as:

$$V_{Lm} = nV_{B1} = 37.6V \tag{3.24}$$

Since the snubber capacitor is large enough, the voltage across the snubber circuit oscillates towards *VLm* with a small ripple, as does the current through the snubber resistor, and the current is obtained by:

$$i_{Rsn} = \frac{V_{Lm}}{R_{sn}} = 5.8 \times 10^{-4} A \tag{3.25}$$

Therefore, the power dissipation on the snubber resistor is estimated to be:

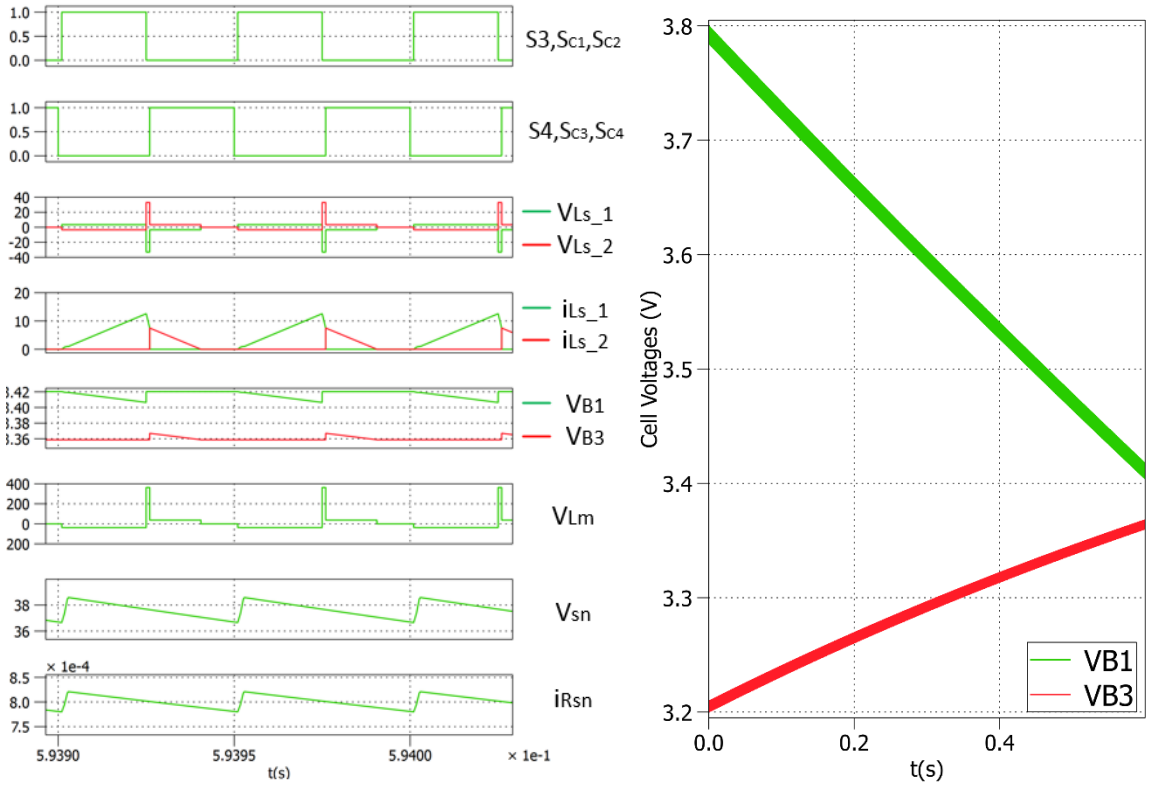
$$P_{sn} = {i_{Rsn}}^2 R_{sn} = 0.218W \tag{3.26}$$

During the dead-time, voltage over the secondary winding is clamped by the Zener diodes, therefore, the power dissipated by the Zener diodes is calculated as:

$$P_{zn} = \frac{V_{zn} I_{zn} t_{on}}{T} = \frac{33V \times 12.1A \times 1\mu s}{50\mu s} = 7.9W \tag{3.27}$$

After this voltage balancing, the voltage of source cell B1 is reduced from 3.8V to 3.42V, while, the voltage of target cell B3 is increased from 3.2V to 3.36V. The overall efficiency of the circuit can be understood as the ratio of the energy received by the target cell to the energy released by the source cell.

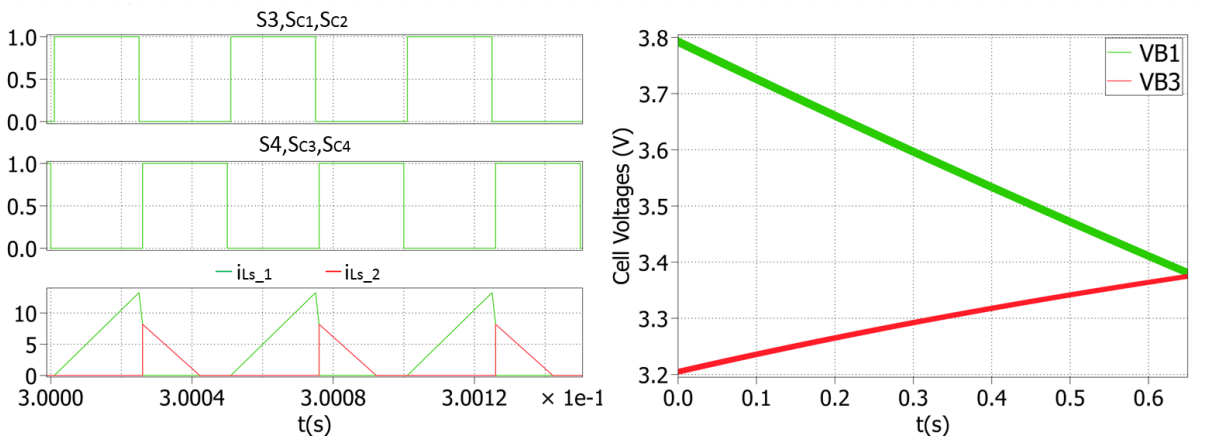
$$ɧ_2 = \frac{\frac{1}{2} \times C \times (3.36V^2 - 3.2V^2)}{\frac{1}{2} \times C \times (3.8V^2 - 3.42V^2)} = 38.25\% \tag{3.28}$$



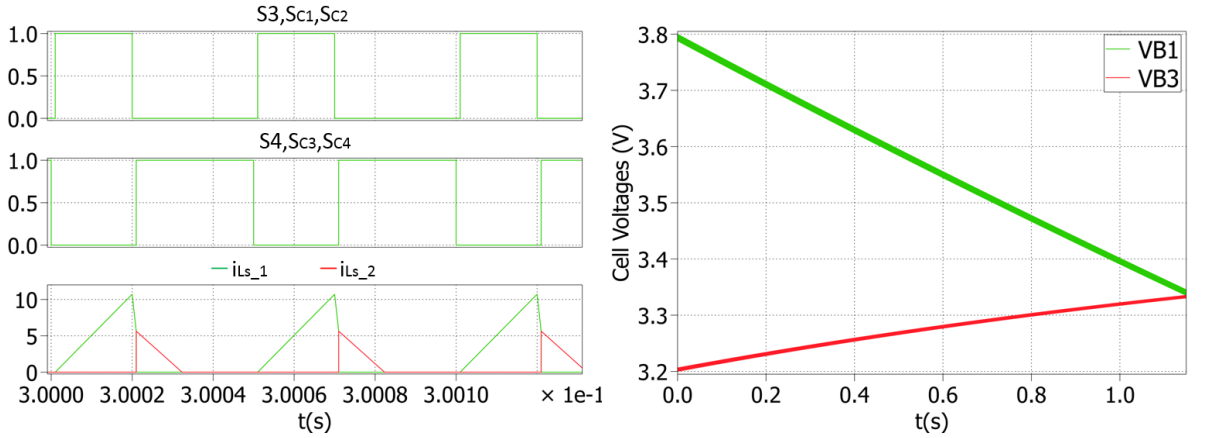
(a) (b)

Figure 3- 30 – Simulation waveforms for the proposed circuit when equalisation from B1 to B3.

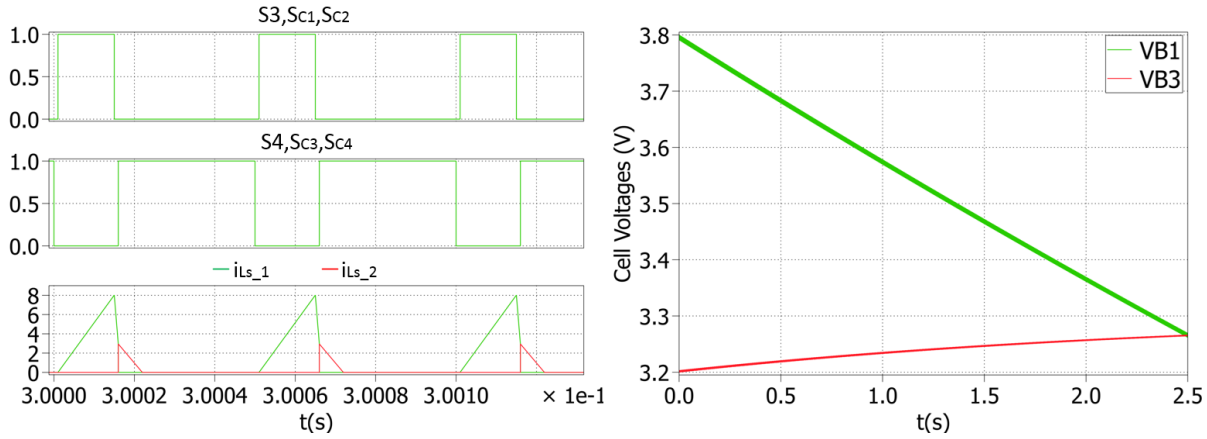
To explore the impact of the duty cycle on circuit performance, the circuit is simulated with different duty cycles. The duty cycle of signals for S3, Sc1 and Sc2 is reduced from 0.5 to 0.4 and then to 0.3. Figure 3-31 shows the current waveforms in both the magnetising and demagnetising periods and cell voltages when the circuit operates in different situations. As the duty cycle decreases, the magnetising period is reduced, as is the peak current of i_{LS_1}. Since the dead-time is unchanged, in these three simulations the peak current of i_{LS_2} is 5A less than the peak current of i_{LS_1}. It can be seen from the figure that with lower magnetising current, a greater the proportion of the 5A current is taken. This means that, when the duty cycle is decreased, the efficiency of energy transfer is reduced. The waveforms of cell voltages can also support this conclusion. When the duty cycle is 0.5, B1 and B3 reach a balanced voltage of 3.38V after 0.7s. Then when the duty cycle decreased to 0.4, it takes the two cells 1.1s to achieve a balanced voltage, which is 3.33V. And with a duty cycle of 0.3, the equalisation process takes 2.5s and ends with a balanced voltage of only 3.27V.



(a)



(b)

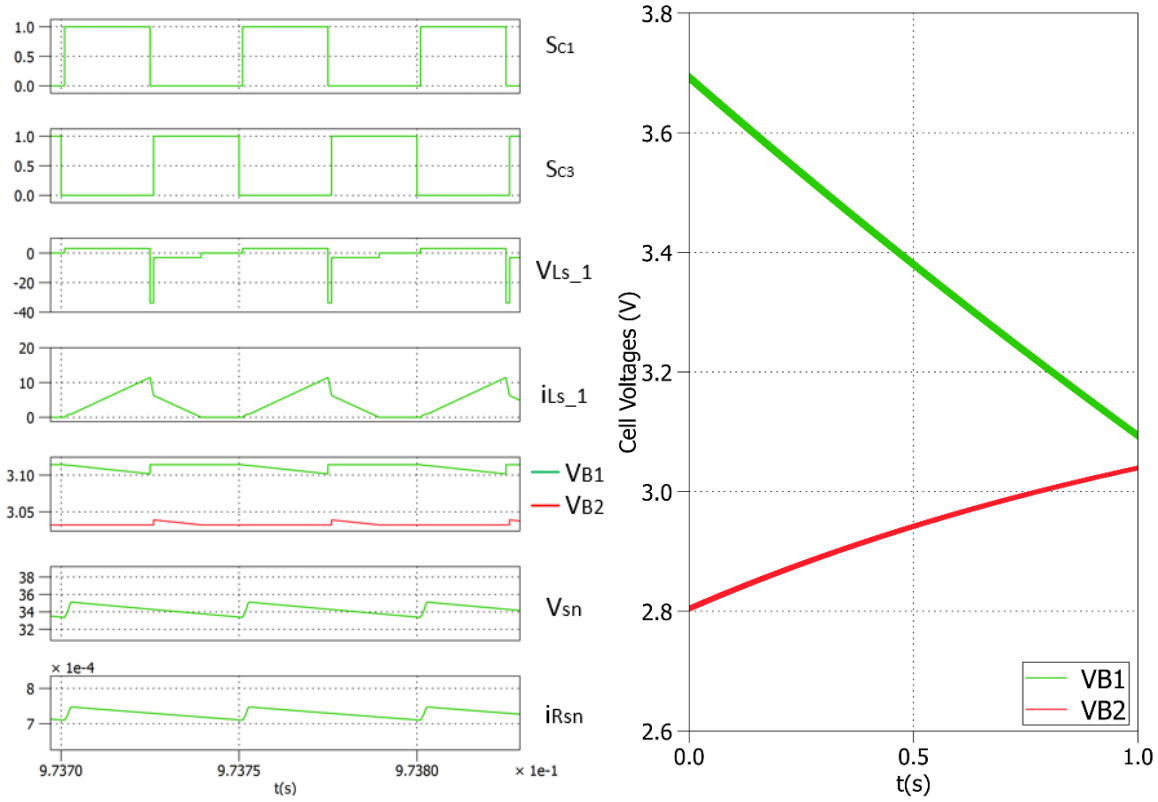


(c)

Figure 3- 31 – Equalisation from B1 to B3 with different duty cycles: (a) D=0.5; (b) D=0.4; (c) D=0.3.

When the voltage equalisation is between an odd numbered cell and an even numbered cell and the circuit operates in Mode 5, the circuit works as a buck-boost converter using only one secondary coil as an inductor. This situation has been simulated with an example of voltage balancing from B1 to B2, with initial voltages of 3.7V and 2.8V respectively. S3 and SC2 are turned on for the entire simulation period,

while SC1 and SC3 are controlled by a pair of complementary square wave signals with a duty cycle of 0.5 and a dead-time of 1 µs. Figure 3-32 shows the waveforms, including the gate drive signals for SC1 and SC3 in the first two figures, the voltage and current of the top secondary windings in the next two figures, the voltages across B1 and B3 in the fifth figure, and the voltage and current in the RCD circuit in the last two figures.



(a) (b)

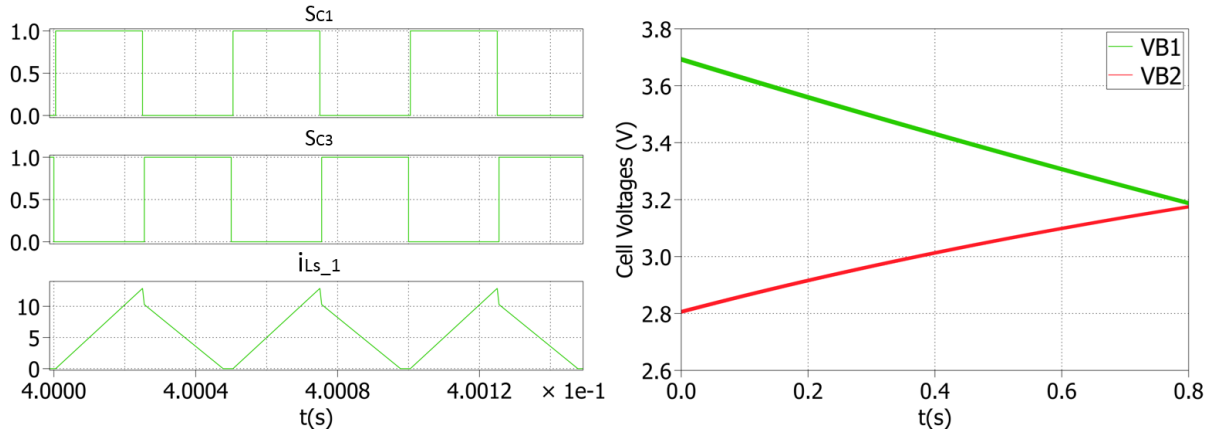
Figure 3- 32 – Simulation waveforms for the proposed circuit when equalisation from B1 to B2.

Calculate the circuit efficiency using the same method as in the previous simulation, the result is:

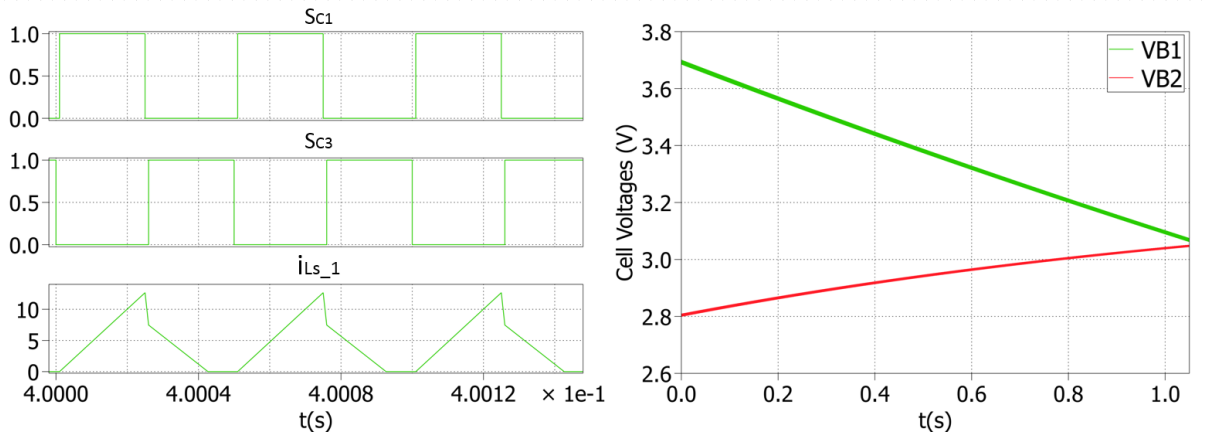
$$\eta_2 = \frac{\frac{1}{2} \times C \times (3.04V^2 - 2.8V^2)}{\frac{1}{2} \times C \times (3.7V^2 - 3.09V^2)} = 48.96\% \qquad (3.29)$$

Compared to the previous operational mode, the circuit has higher efficiency when the equalisation happens between an odd numbered cell and an even numbered cell. It is because in this operational mode, the circuit works as a buck-boost converter with only one winding involved, therefore, avoiding losses caused by the leakage inductance.

The circuit is then simulated with varying dead-times to demonstrate its impact on circuit performance. Figure 3-33 shows the current flowing in the winding N_{s_1} and the cell voltages when the circuit operates with dead-times of 0.5us, 1us, 1.5us and 2us. It can be seen from the current waveforms that the dead-time causes a drop in the current which is bigger when the dead-time is longer. The waveforms of cell voltages illustrate that both the equalisation speed and energy transfer efficiency are improved when the dead-time is shorter. With a dead-time of 0.5us, it takes B1 and B2 0.8s to reach a balanced voltage of 3.2V; however, when the dead-time is increased to 2us, the two cells consume 1.65s to get a balanced voltage, and the voltage drop in B1 is much greater than the voltage rise in B2.



(a)



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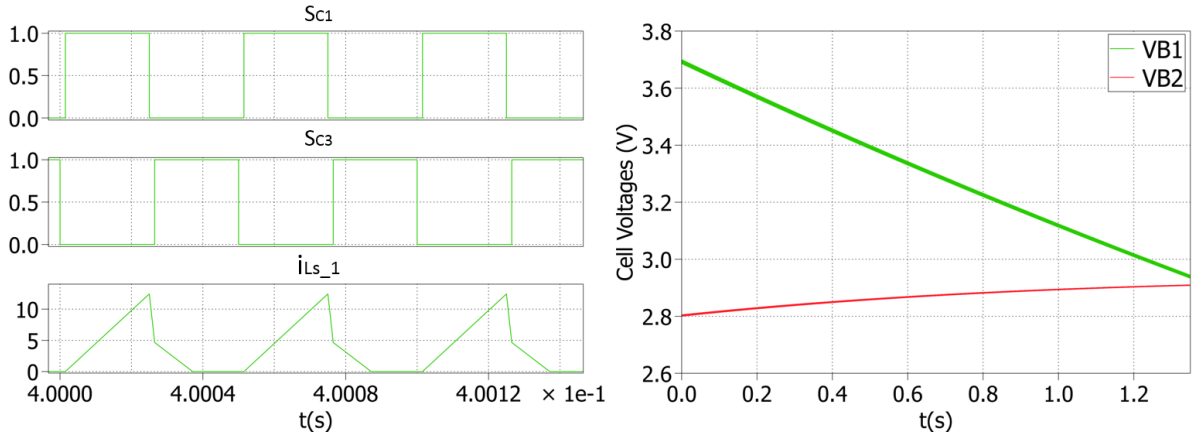

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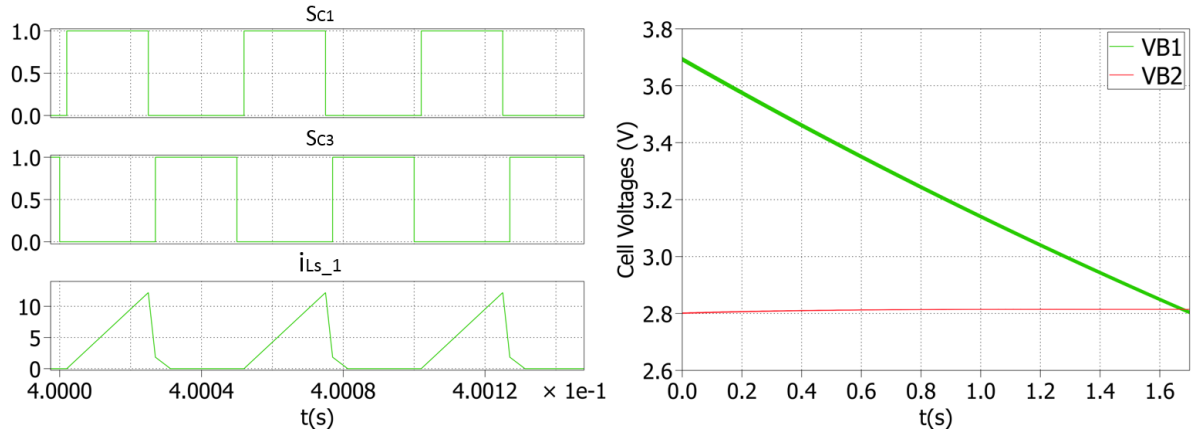


(d)

Figure 3- 33 – Equalisation from B1 to B2 with different dead-times: (a) dead-time = 0.5us; (b) dead-time = 1us; (c) dead-time = 1.5us; (d) dead-time = 2us.

It can be observed from the cell voltages waveforms, for example Figure 3-32(b), that as the voltage difference decreases, the voltage of the target cell increases at a lower rate. It is because that the charging current to the target cell is determined by the voltage difference, and will extend the equalisation time. Besides, the structure of the circuit determines that each cell is connected to a coil through four switches in the cell selector and another two switches in the winding selector, it makes the conducting losses and switching losses of transistors are higher than other kind of equalisation circuits.

3.7 Summary

A multi-functional voltage balancer circuit is proposed for an EV. The circuit combines the function of battery charging from the grid with the function of the voltage balancing of the battery cells. A three-coil transformer is the key component achieving these multiple functionalities.

The proposed circuit has five operational modes, two for grid charging and three for voltage balancing. When it is used for battery charging, or equalisation between odd cells or even cells (Mode 1 – Mode 4), the converter in the circuit operates in flyback mode. Meanwhile if the circuit is working for equalisation between odd cells and even cells (Mode 5), one coil of the transformer is utilised as an inductor in a buck-boost converter.

The proposed circuit has been simulated in PLECS to test the principles of operation. The circuit was tested under open-loop control and waveforms have been recorded to demonstrate the principles of operation. For battery grid charging, the efficiency of the simulated circuit is 89.8%. For voltage equalisations between odd cells or even cells, the circuit efficiency is 38.25%, the losses are mostly dissipated by the leakage inductance and the Zener diode. For voltage equalisations between odd cells and even cells, the circuit efficiency is relatively high as 48.96%, and reducing the dead-time could further improve the efficiency.

Chapter IV PFC & CC-CV Controller

This chapter presents a closed-loop control method for the proposed circuit which allows the circuit to realise functions including power factor correction (PFC) and constant-voltage-constant-current (CC-CV) charging during operation. Rather than being controlled by an open-loop control signal with a fixed duty cycle, the circuit will run more stably and produce a modulated output under the proposed control method.

4.1 Power factor (PF)

As introduced in section 2.1.2, EV chargers must guarantee that the charger unit produces a high power factor to maximize the real output power, and the charging current is drawn with low distortion to minimize the impact on power quality [115-117]. This section describes how the power factor of a circuit is defined and calculated.

The PF is defined as the ratio between the real and apparent power:

$$PF = \frac{Real\ Power\ (Watts)}{Apparent\ Power\ (VA)} \tag{4.1}$$

The PF indicates the effectiveness of a system in delivering pure real power from the source to the load. The ideal PF is 1, and this occurs if the system is purely resistive. In this case, the voltage and current are in phase and neither have AC distortion.

There are two reasons that cause a poor PF: a phase difference between voltage and current; or a high harmonic content in the current or voltage waveform resulting from a distorted current or voltage signal. If a system is composed of only resistive, capacitive and inductive elements and all are linear, then both the voltage and current are sinusoidal but not in phase. Figure 4-1 shows the impact of phase delay on the PF. In this figure, a lagging PF is shown where the phase of the current lags behind the phase of the voltage by a phase angle φ. The power factor of this system is equal to the cosine of the angle, $\cos\varphi$.

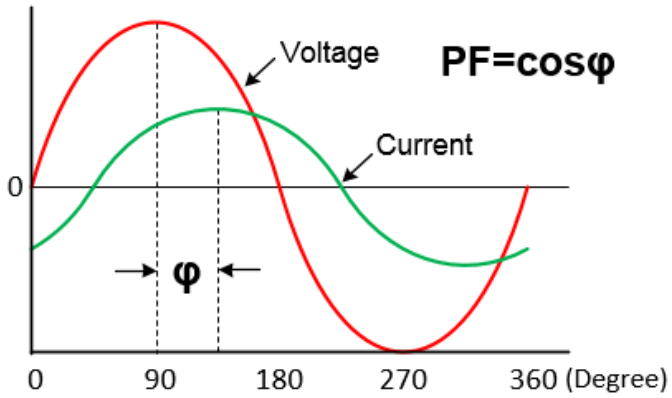


Figure 4- 1 – AC voltage and current with a lagging power factor in a linear system.

A distorted current waveform can be the result of a switched mode power converter or the result of other electronic devices influencing the current and voltage signals. These elements present a nonlinear impedance to the system and further cause distorted waveforms with high harmonics. For example, the input circuit shown in Figure 4-2 consists of a rectifier followed by a DC bus capacitor capable of sustaining the voltage of approximately the peak value of the input sine wave until the next peak comes along to recharge the capacitor. In this case, current is drawn from the input only when the input voltage is higher than that of the capacitor, and therefore the sine wave current is squeezed to current pulses. Figure 4-3 illustrates this situation.

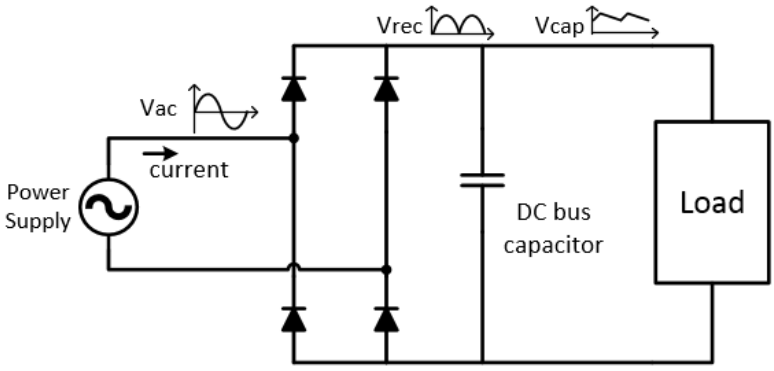


Figure 4- 2 – AC input circuit with a rectifier and a DC bus capacitor.

In Figure 4-3 the current and voltage are still in phase, despite the severe distortion of the current waveform. To calculate the power factor in these circumstances, the harmonic content of the current needs to be taken into consideration.

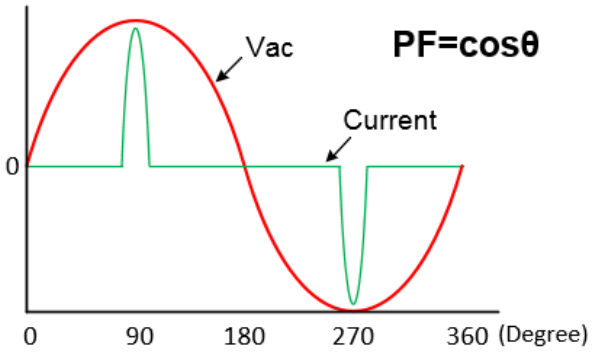


Figure 4- 3 – Input characteristics of an AC input circuit without PFC.

Figure 4-4 shows the harmonic content of the current shown in Figure 4-3. The fundamental harmonic at 50Hz has the highest amplitude; however, odd harmonics are indicated to have a significant amplitude as well. Since only the fundamental produces real power, while other harmonics only contribute to the apparent power, the PF drops below 1.0. The deviation is represented by the distortion factor of the current, $\cos\theta$. In systems where the current is distorted but still in phase with the voltage, the power factor is equal to the distortion factor of the current.

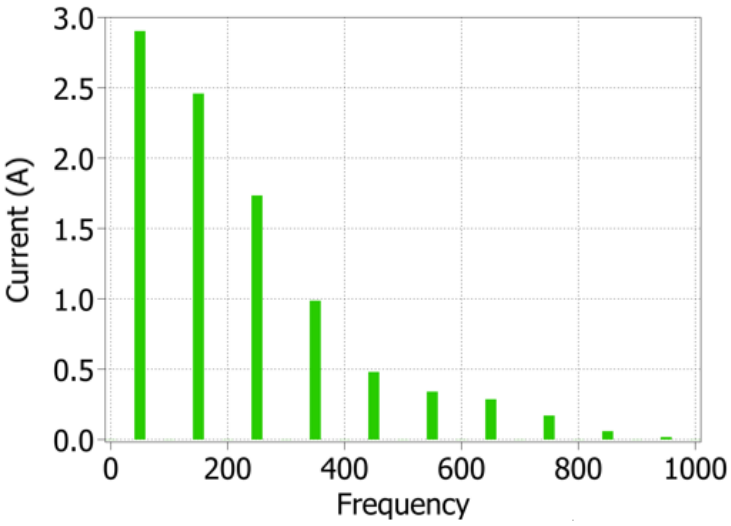


Figure 4- 4 – Harmonic content of the current waveform in figure 4-3.

The distortion factor of the current, as well as the power factor, can be expressed as:

$$PF = \cos\theta = \frac{1}{\sqrt{1+THD^2}} \tag{4.2}$$

in which,

$$THD(\%) = 100 \cdot \frac{\sqrt{\sum_{p=2}^{\infty} {I_p}^2}}{I_1} \tag{4.3}$$

THD stands for the total harmonic distortion, which is the quadratic sum of the unwanted harmonics over the fundamental giving the relative weight of the harmonic content with respect to the fundamental.

Generally, in a system, if the current no longer mimics the voltage as a sine wave and they are not in phase, then the power factor is given by:

$$PF = \cos\varphi \cdot \cos\theta \tag{4.4}$$

4.2 PFC control for the proposed circuit

This section introduces a PFC controller for the proposed circuit, including the block diagram of the PFC circuit and simulation results when the proposed circuit operates either with open-loop control or with PFC control.

4.2.1 PFC control circuit

When operating in charging mode, the proposed converter is connected to the grid and operates as a flyback converter. In order to achieve high PF, the circuit must have a PFC circuit. Due to the fact that the proposed circuit operates as a flyback converter, no additional components are required for PFC during charging mode and all of the control is embedded in the controller. Figure 4-5 shows the sensors that are required for the PFC in the proposed circuit.

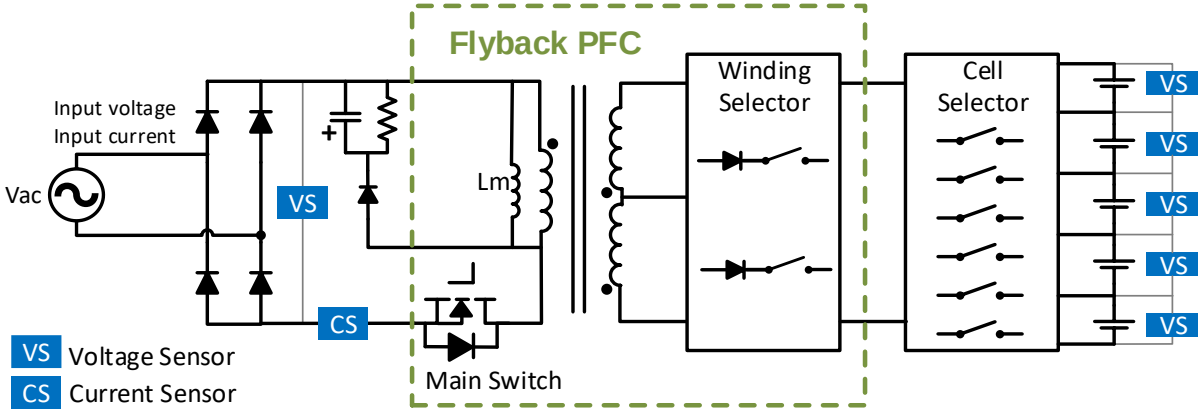


Figure 4- 5 – Proposed charging circuit with PFC.

Input voltage and current information is collected at the position between the rectifier and the primary side of the transformer. To allow the current to mimic the voltage as a half-sinusoidal wave, there is no input capacitor shunted at the output of the rectifier.

When the circuit operates under open loop-control, the main switch is gated by a pulse signal with a fixed duty cycle *D*. This means that the current ramp-up time in the primary

winding is fixed, regardless of the value of the input voltage. The AC power supply offers a sinusoidal input voltage $V_{in}\sin\omega t$, after the rectifier, and the voltage across the magnetic inductor is a half sine wave, with the value varying from zero to the maximum. As the output of the rectifier produces a pulsed half sine waveform with values varying from zero to the peak voltage of the AC input voltage, the voltage across the magnetic inductor *Lm* varies and consequently the peak current value during the magnetisation period can be expressed as:

$$I_{peak} = \frac{V_{in} \cdot |\sin \omega t|}{L_m} \cdot t_{on} = \frac{V_{in} \cdot |\sin \omega t|}{L_m} \cdot D \cdot T \tag{4.5}$$

Where, *ton* is the on-state time and *T* is the switching period. During the following demagnetizing period, the voltage across the primary winding is clamped by *nV0*, in which *V0* is the output voltage across the battery pack, and the current in the inductor starts to drop since the energy flows to the load. The time consumed Δt_f as the inductor current falls to zero is:

$$\Delta t_f = \frac{I_{peak} \cdot L_m}{nV_0} \tag{4.6}$$

Applying Equation (4.5) into (4.6), the demagnetization current also becomes a function of the duty cycle:

$$\Delta t_f = \frac{V_{in} \cdot |\sin \omega t|}{nV_0} \cdot D \cdot T \tag{4.7}$$

Therefore, the total time T' during which the inductor current rises from zero to the peak value and falls back to zero is:

$$T' = t_{on} + \Delta t_f = t_{on}\left(1 + \frac{V_{in} \cdot |\sin \omega t|}{nV_0}\right)$$

$$= DT\left(1 + \frac{V_{in} \cdot |\sin \omega t|}{nV_0}\right) \tag{4.8}$$

In order to avoid the saturation of the transformer, the magnetizing and demagnetizing processes must be completed before the end of a new switching event. Thus the following equation must be fulfilled:

$$DT\left(1 + \frac{V_{in} \cdot |\sin \omega t|}{nV_0}\right) < \mathrm{T} \tag{4.9}$$

Therefore,

$$\frac{V_{in} \cdot |\sin \omega t|}{nV_0} < \frac{1}{D} - 1 \quad (0 < D < 1) \tag{4.10}$$

When the proposed circuit charges the battery from the grid under open-loop control, the critical value of the duty cycle D can be calculated from Equation (4.10) based on the worst-case scenario, and that is when the input voltage is at its maximum value. An example of the circuit operating with a constant D which meets the description in the above equation is shown in Figure 4-6.

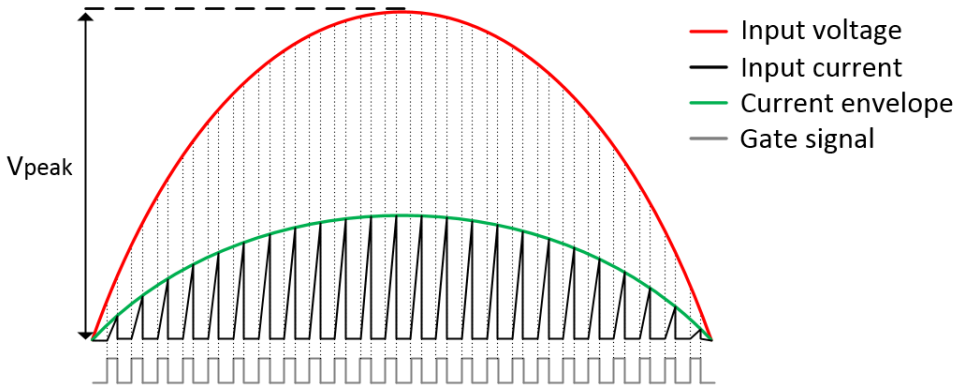


Figure 4- 6 – Waveforms when the circuit operates at a constant D within the range in equation (4.10).

Figure 4-7 shows the voltage and current waveforms when the duty cycle D exceeds the range described in equation (4.10). The transformer suffers saturation when the value of input voltage rises to a level so that the energy stored during the magnetizing period cannot be transferred to the load within the demagnetizing period. This causes a severe distortion around the centre area in the current wave when the input voltage is near the maximum.

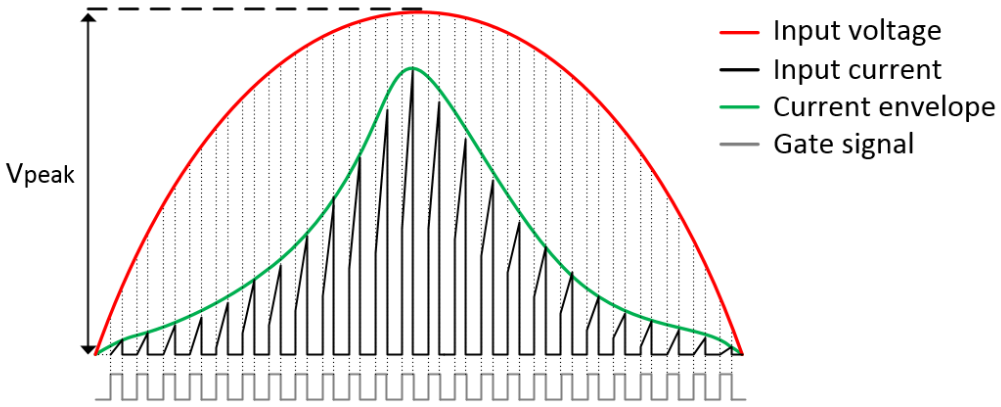


Figure 4- 7 – Waveforms when the circuit operates at a constant D exceeding the range in equation (4.10).

Due to the fact that the input voltage varies, the duty cycle can vary too and does not need to be constant. Consequently a varying duty cycle can be used to improve the input current distortion. Besides, Equation (4.10) indicates that the range of D that keeps the circuit operating with a good PF is determined by both the input voltage *Vin* and the load voltage *V0*. Due to the fact that, according to the descriptions in the last chapter, the target battery string can be different combinations of battery cells, the load voltage may change during the charging process. This means that a constant D may not satisfy all the situations when the target battery cells change. Thus a PFC control structure has been developed for the circuit.

The PFC controller is shown in Figure 4-8, including the required sensors. To collect necessary information during operation, except for the voltage and current sensors between the rectifier and transformer, each battery cell is shunted by a voltage sensor. The controller consists of three functional blocks: an outer voltage loop, an inner current loop, and a PWM modulator.

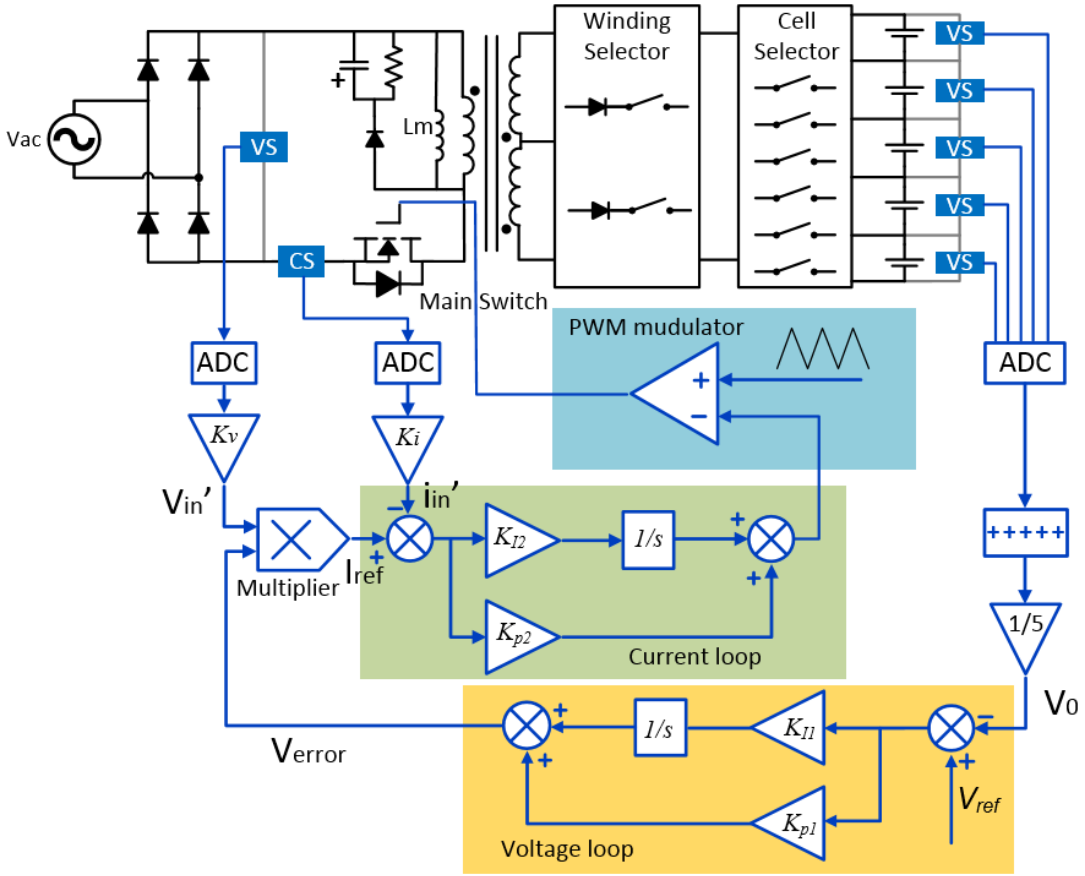


Figure 4- 8 – Schematic of the proposed PFC controller.

The voltages of each cell are detected and an average value V_0 is calculated as the output voltage of the system. Using the average voltage instead of the overall output voltage allows adaptation to the reference in the outer voltage loop. In this way, the reference can be set as the rated voltage of one battery cell no matter how many cells are charged. The average voltage is compared with the battery stack reference voltage *Vref* producing the error *Verror* which is PI controlled by the voltage loop. The voltage error is multiplied by the regulated input voltage V'_{in}. Thus information about the shape and the DC contents of the battery pack are generated and this is regarded as the current reference I_{ref}. In the inner current loop, I_{ref} is compared with the regulated current i'_{in} and the error is controlled by the current PI controller. The controlled signal is then fed into a PWM modulator. Within this block, the signal is compared to a fixed frequency triangle wave to generate a pulse wave with a modulated duty cycle. This pulse wave is utilised to drive the main switch in the circuit.

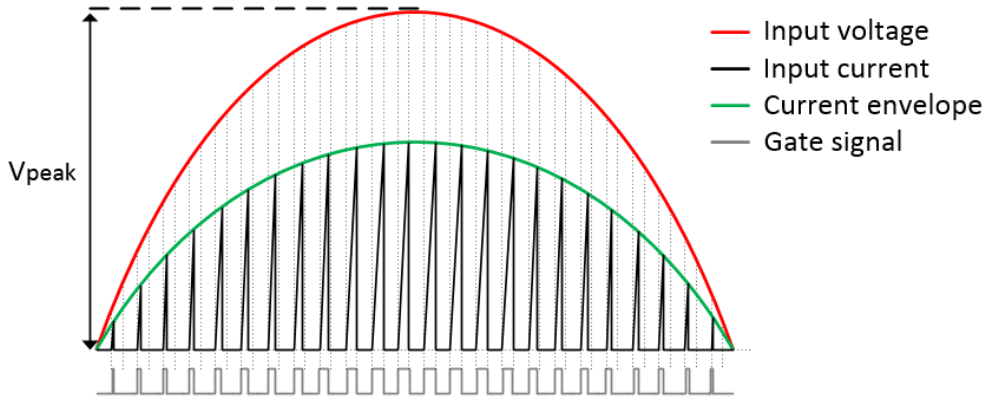


Figure 4- 9 – Waveforms when the circuit operates under PFC control.

Figure 4-9 indicates the key waveforms when the circuit operates under PFC control. The gate signal of the main switch maintains the fixed switching frequency since it is determined by the frequency of the triangle wave in the PWM modulator, while the duty cycle now varies with the value of the input voltage.

4.2.2 Circuit simulation with PFC controller

For the proposed charging circuit, whether or not a cell needs charging is determined by its terminal voltage. This means that the output voltage of the circuit is uncertain. Hence, a pulse signal with a fixed duty cycle cannot guarantee a high power factor in these circumstances. This section demonstrates how the circuit operates with and without the PFC controller with a changed load.

The simulation model used in this simulation is the same as that described previously in Chapter III. To show that the load has an impact on the PF, the load of the circuit is changed during the simulation from five cells to three cells. In the first stage of simulation, there are five cells in the target battery string and the circuit is gated continuously by a pulse signal with a duty cycle of 0.35.

The initial voltage of each cell is set at 4.0V; hence, when there are five cells in the load, the output voltage is $4.0\text{V} \times 5 = 20\text{V}$. These parameters are input into Equation (4.10):

$$0 < \frac{325V \cdot |\sin \omega t|}{20V \times 11} < 1.48 \tag{4.11}$$

$$\frac{1}{D} - 1 = \frac{1}{0.35} - 1 = 1.86 \tag{4.12}$$

With the maximum input voltage when $|\sin \omega t|$ =1, Equation (4.10) is fulfilled. Figure 4-10 shows the input voltage and current in this situation.

As soon as the load circuit switches to three cells, the output voltage of the circuit is reduced to $4.0\text{V} \times 3 = 12\text{V}$. Thus:

$$0 < \frac{325V \cdot |\sin \omega t|}{12V \times 11} < 2.46 \tag{4.13}$$

Comparing Equation (4.13) and (4.12), the new circuit no longer satisfies Equation (4.10) all of the time. From the waveform on the right hand side of Figure 4-10, it is obvious that the peak current reaches a very high value. Figure 4-11 shows the zoomed waveforms, indicating that the peak value of the input current is low for a period at the beginning of the half cycle and for a period at the end of the half cycle but increases dramatically in the period in between. This is because Equation (4.10) is satisfied during the periods at the beginning and end of the half cycle but not during the intervening period, which results in the saturation of the transformer. Beside this, there are phase lags between the voltage and current, where the phase difference is measured as 16.2°, and $\cos \varphi$ is 0.96.

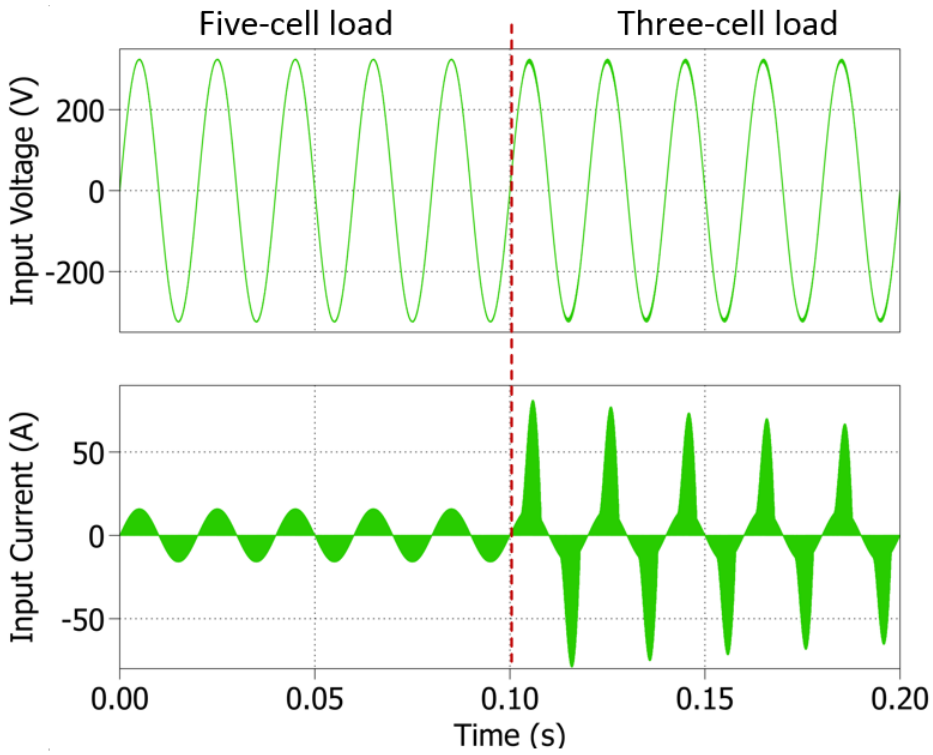


Figure 4- 10 – Simulation for fixed D=0.35 and load change from 5 to 3 cells.

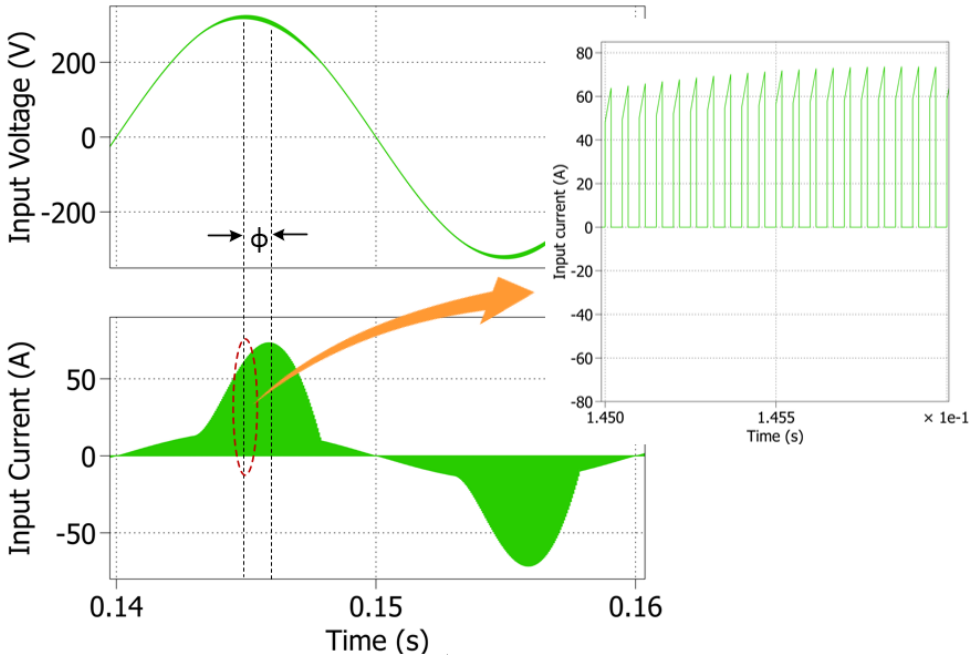
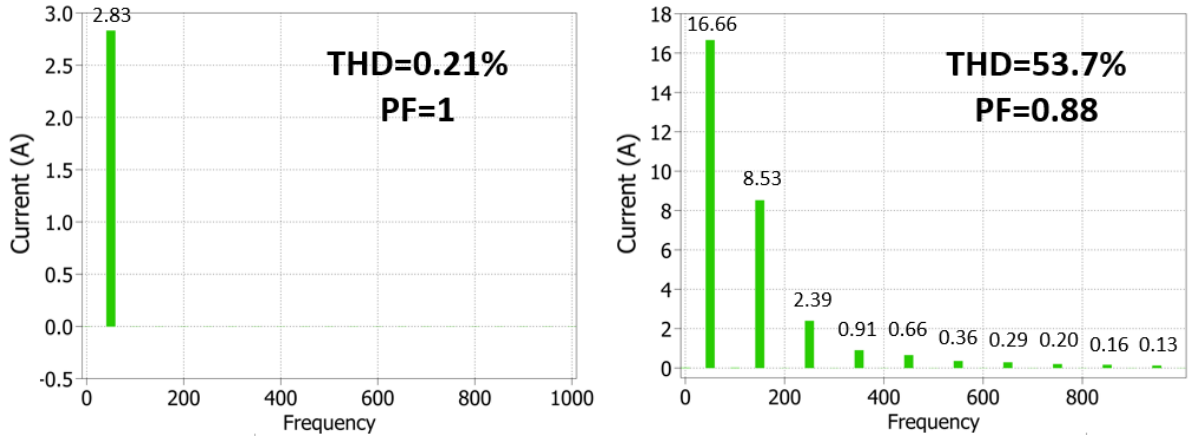


Figure 4- 11 – Zoomed waveforms in Figure 4-10.

A fast Fourier Transform (FFT) analysis applied to the input current produces the current harmonic spectrum. For the pulsed sine waves shown in Figure 4-11, the harmonics at the switching frequency and multiples of the switching frequency are large. The harmonic contents of the full frequency span re shown in Appendix A. However, the main purpose of the PFC controller is to eliminate low-frequency odd-

order harmonics, and hence the harmonic contents shown in this chapter contains harmonics within 1kHz, and the THD is calculated based on low frequency harmonics as well. Figure 4-12 shows the spectra for the five-cell load and the three-cell load. Charging five cells provides a high PF very close to 1 and a THD of only 0.21%, whereas charging three cells results in a PF value of 0.88 and THD of 53.7%.



(a) (b)

Figure 4- 12 – Harmonic content of the current waveforms in Figure 4-10 with the load of: (a) 5 cells; (b) 3 cells.

In order to deal with the change in the PF caused by load changes, the PFC controller was introduced earlier and is simulated here. The parameters of the controller are presented in Table 4-1 and the simulation results are shown in Figure 4-13.

Table 4- 1 – Simulation parameters in the PFC controller

Voltage Loop		Current Loop	
K_v	1/325	K_i	1/16
K_{p1}	1.25	K_{p2}	0.9
K_{I1}	0.8	K_{I2}	0.05
V_{ref}	4.5		

Figure 4-13 show that neither an excessive rise nor sharp current distortion in the current when the load is changing from five cells to three cells. The harmonic contents of the two sections of current has been studied and the results are shown in Figure 4-14.

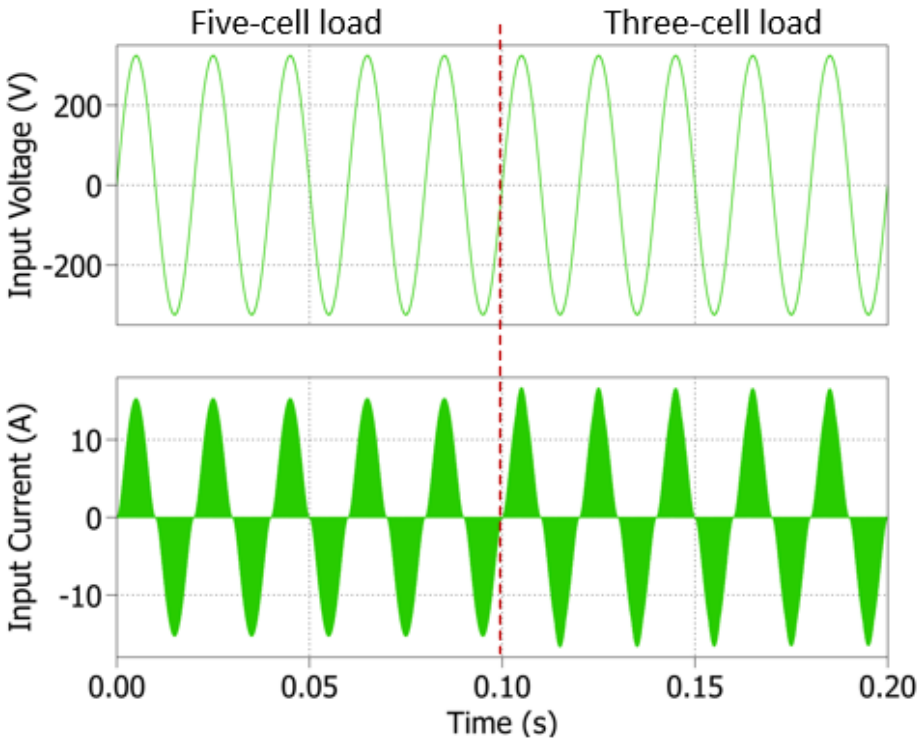


Figure 4- 13 – Simulation with PFC controller and the load change from 5 cells to 3 cells.

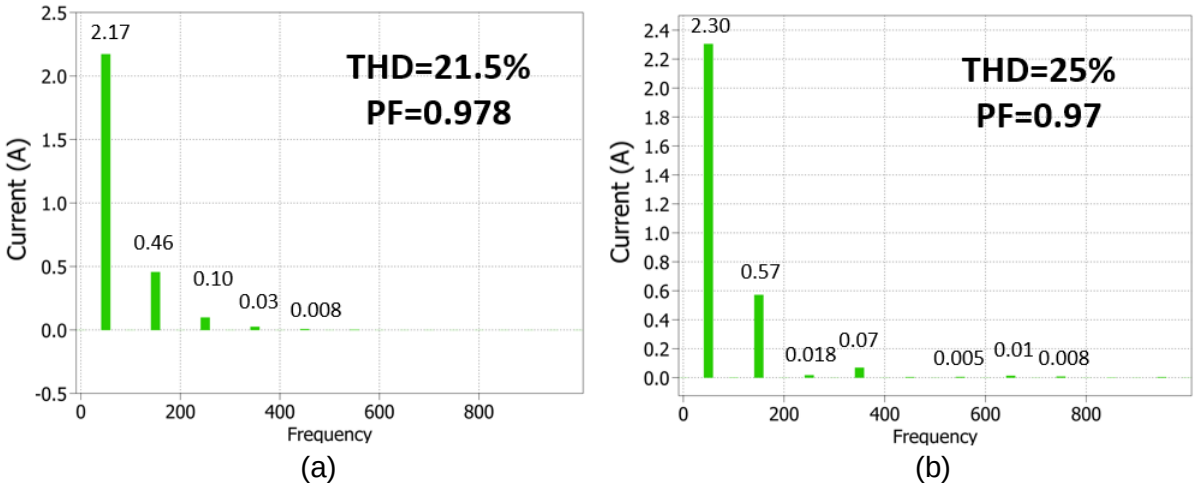


Figure 4- 14 – Harmonic content of the current waveforms in Figure 4-13 with the load of: (a) 5 cells; (b) 3 cells.

Comparing the PFC control with the fixed duty cycle control, the PF of the circuit is slightly decreased for the five-cell load from nearly 1 to 0.978 but significantly improved for the three-cell load from 0.84 to 0.97. This proves that the proposed control method contributes to maintain a good power factor when the circuit load changes.

4.3 PFC and CC-CV control

In Chapter II it was stated that the most efficient method to charge a lithium-ion battery is CC-CV charging. Therefore, the circuit must not only provide a good PF but also charge the battery cells according to CC-CV at the same time. This section describes the enhancement of the PFC controller introduced in Section 4.2 in order to achieve CC-CV control.

In the early stages of battery charging, when cell voltages are far below the maximum allowable cell voltage, charging with a large current helps to increase the charging speed and reduce charging time.

Figure 4-17 shows the diagram of the PFC and CC controller. There are two differences between this control circuit and the former one shown in Figure 4-10. Firstly, CC control means that the current flowing into the battery cells must be controlled but the battery voltage is not. As the relationship between the input and output current of the transformer is determined by the turns-ratio of the transformer, the current can be controlled either by the secondary side or the primary side of the transformer. Since the PFC controller already uses a current sensor on the primary side, the CC controller will make use of the same sensor. As CC directly controls the input current, which means that it also controls the battery current, it is theoretically independent from the voltage level across the battery. Consequently, the PFC and CC control does not require voltage information from the battery pack as feedback into the controller. Secondly, the voltage reference used in the outer current loop is the rectified voltage multiplied by K_{v1} rather than a constant value, in order that the reference and the input current keep the same shape.

With the outer loop regulating the current level and the inner loop regulating the current shape, this PFC and CC controller helps the circuit to produce a constant current output with a high power factor.

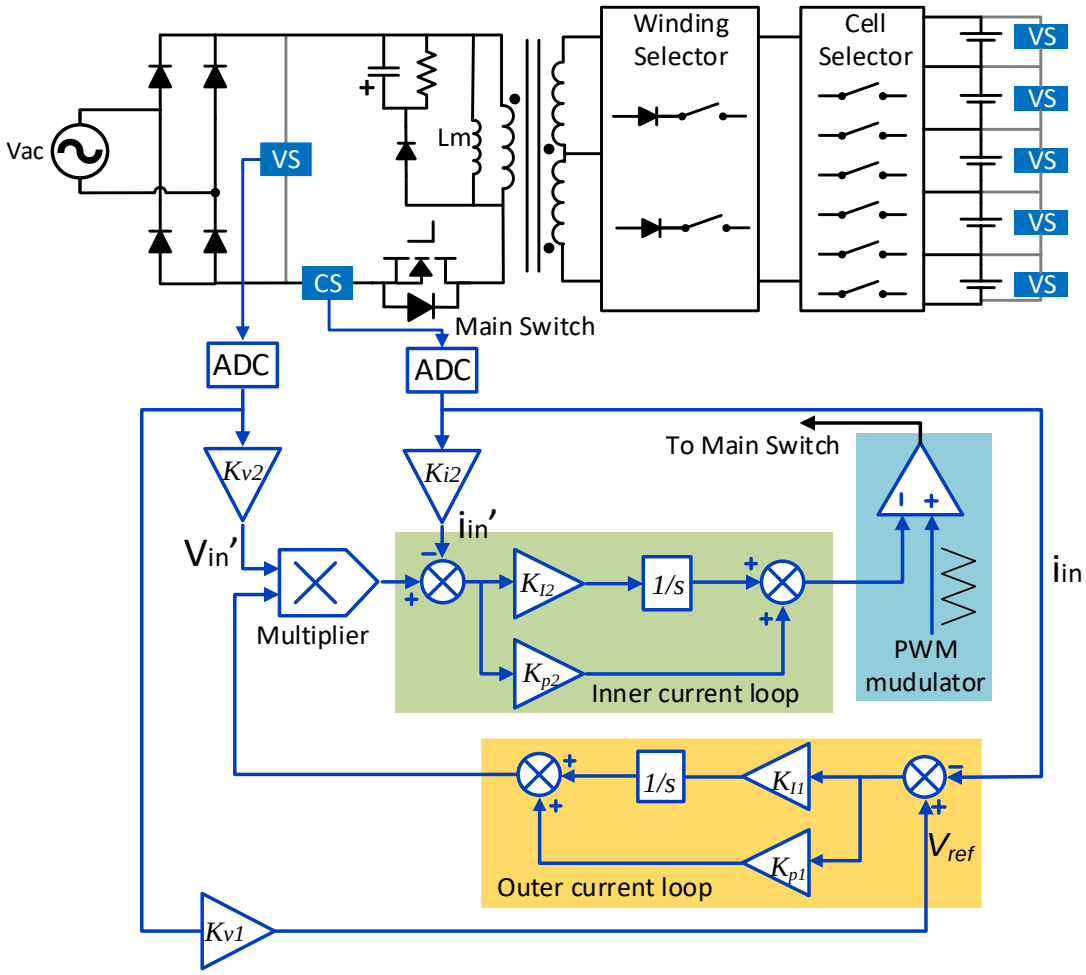


Figure 4- 15 – Schematic of proposed charging circuit with PFC and CC control.

A contrast test is applied to demonstrate the function of the PFC and CC controller. As in the last section, the circuit is tested with a changed load from five to three cells. The initial voltage of each cell is 3V. In the first half period, the output voltage is $3V \times 5 = 15V$, while in the second half period the output voltage becomes $3V \times 3 = 9V$. With the method introduced in Equations (4.11) and (4.12), the duty cycle is set at 0.3 so that the circuit can achieve a high PF with the five-cell load but cannot maintain it with a three-cell load.

Figure 4-16 shows the input voltage and current when the circuit is working under open-loop control. The second half of the current shows obvious distortion in shape, and the peak current is lagging behind the voltage. Applying FFT analysis to the current, the harmonic contents within 1kHz are presented in Figure 4-17.

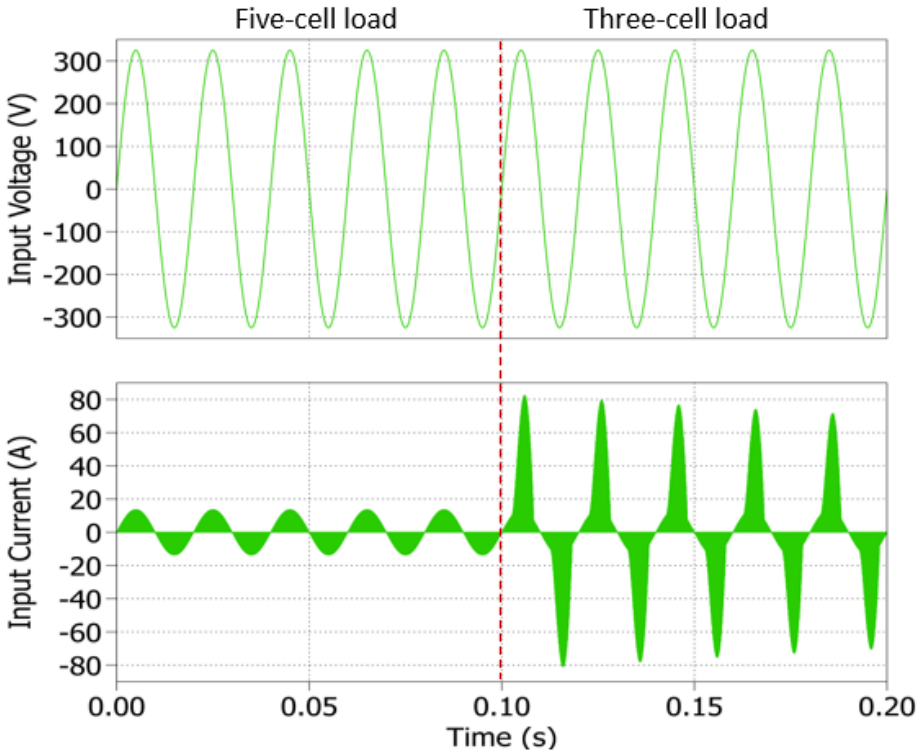
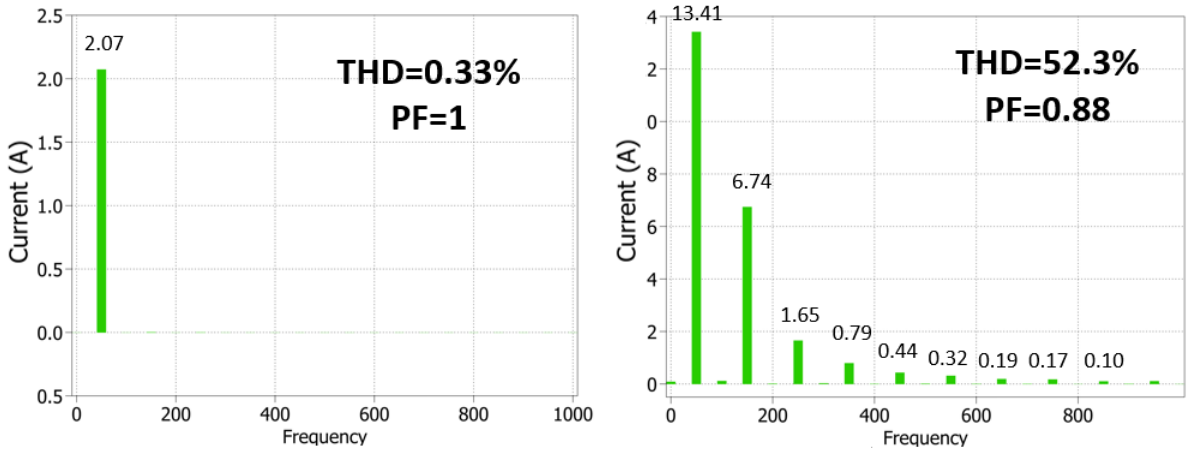


Figure 4- 16 – Simulation for fixed D=0.3 and the load changes from 5 to 3 cells.



(a) (b)

Figure 4- 17 – Harmonic content of the current waveforms in Figure 4-16 with the load of: (a) 5 cells; (b) 3 cells.

The PFC and CC controller is then simulated with the controller parameters shown in Table 4-2. The results for input voltage and current waveforms are shown in Figure 4-18. When the load circuit switches from five to three cells, the peak current wave remains nearly constant, which is as expected since the input current is controlled. Figure 4-19 shows the harmonic contents, the PF and the THD of the circuit.

Table 4- 2 – Simulation parameters in PFC and CC controller

Outer Loop		Inner Loop	
K_{v1}	1/25	K_{v2}	1/325
K_{p1}	1.1	K_{i2}	1/15
K_{I1}	10	K_{p2}	0.1
		K_{I2}	20

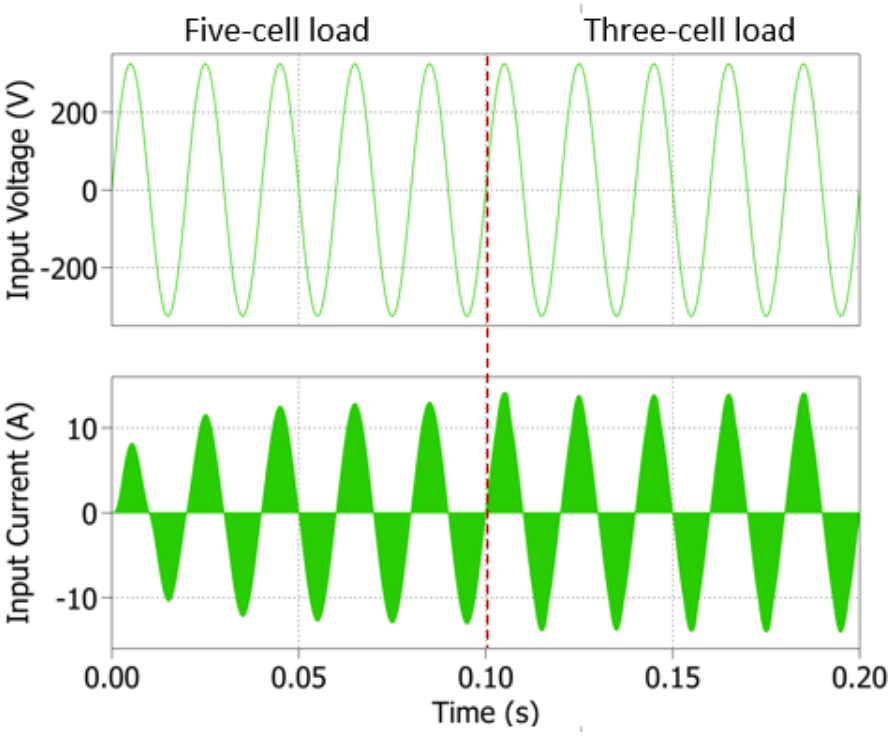
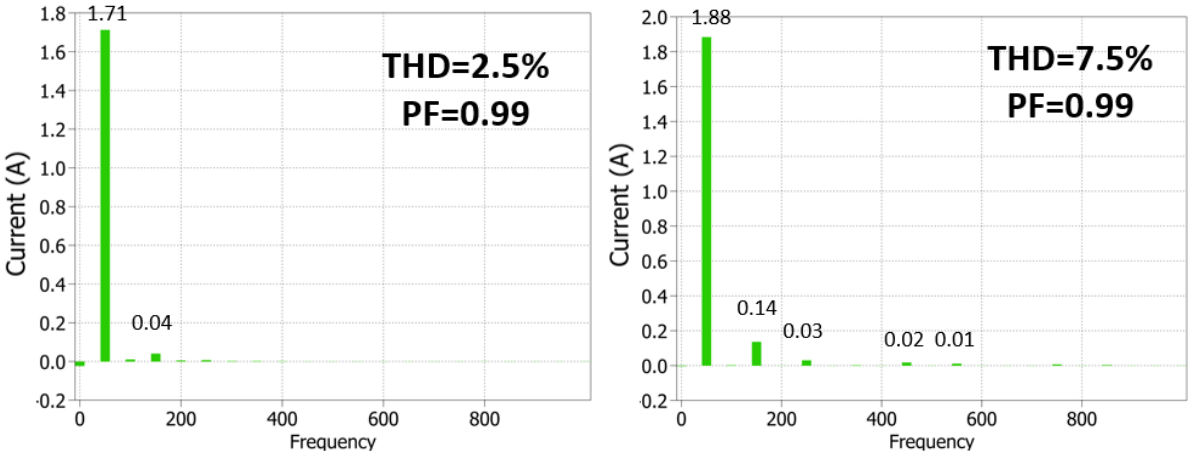


Figure 4- 18 – Simulation waveforms of input voltage and current PFC and CC control for two loads.



(a) (b)

Figure 4- 19 – Harmonic content of the current waveforms in Figure 4-18 with load of: (a) 5 cells; (b) 3 cells.

When the cell voltages approach the rated value, the constant current control needs to be switched to a constant voltage control since a large charging current at this stage may lead to overcharging. In this case, information on the battery voltage is required. This feedback loop, however, has already been implemented in the circuit presented in Figure 4-8. In the PFC controller, the voltage loop aims to compare the circuit output voltage with a voltage reference before regulating the voltage error. Its job is to cause the output voltage to converge to the reference value through a PI controller. If the voltage reference is set as the rated voltage of the cells, the circuit will eventually reach and remain in a state where the average voltage of cells is infinitely close to the rated voltage. In other words, the control circuit proposed in the last section is a PFC and CV controller.

To develop a control method which can be utilized in the whole process of battery charging, the two controllers need to be integrated. For instance, to charge battery cells with a rated voltage of 4.5V, according to the principles of CC-CV charging when the voltages of all cells are under a threshold value (4V, for example), the battery pack can be charged with a large current to reach a high charging speed. Otherwise, the charging needs to slow down with a smaller current to reduce the risk of overcharging. Hence, a selector is needed to switch between PFC and CC control and PFC and CV control in the code. The flow chart of the complete control method is shown in Figure 4-20.

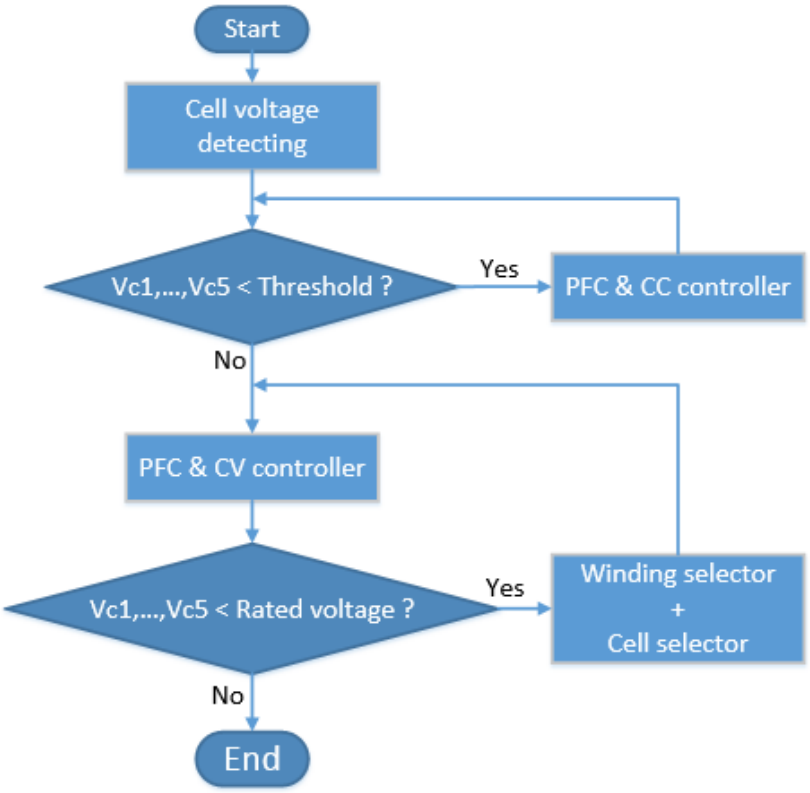


Figure 4- 20 – Flow chart of proposed PFC and CC-CV controller.

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Table 4- 3 –Simulation parameters in PFC and CC-CV controller

Parameters		Value	Parameters		Value
Cell initial voltage (V)	B1, B2, B3	2.8	Input voltage (peak) (V)		325
	B4, B5	3	Threshold voltage (V)		4
PFC and CV	K_v	1/325	PFC and CC	K_{v1}	1/25
	K_i	1/16		K_{p1}	1.6
	K_{p1}	1.25		K_{I1}	10
	K_{I1}	0.8		K_{v2}	1/325
	K_{p2}	0.9		K_{i2}	1/15
	K_{I2}	0.05		K_{p2}	0.1
	V_{ref}	4.5		K_{I2}	20

A simulation has been conducted to demonstrate the control cycle shown in Figure 4-20. In this simulation model, the capacitor which stands for the battery capacity in the battery model is set at 100H to observe the voltage changes in battery cells over a reasonable simulation period. The initial voltage of each of B1, B2 and B3 is 3.8V, and B4 and B5 are 4.0V at the beginning. The parameters in the circuit and PI controllers are listed in Table 4-3

Figure 4-21 shows the voltages of five cells and the input current. The complete charging process can be divided into three stages. In the first stage, the circuit is CC charged. After 5s, B4 and B5 cell reach almost to the threshold of 4V, and therefore the controller switches from CC to CV charging and Stage 2 begins. The input current starts to decline as the cell voltages get closer to the rated voltage, and the charging speed slows down. It takes 5 seconds for B4 and B5 to become fully charged, but B1 to B3 are not yet. Hence, in Stage 3, B4 and B5 are no longer being charged, while B1, B2 and B3 are still charged by a small current. By the end of the simulation, the charging speed is extremely slow so that cells can reach the rated voltage very smoothly.

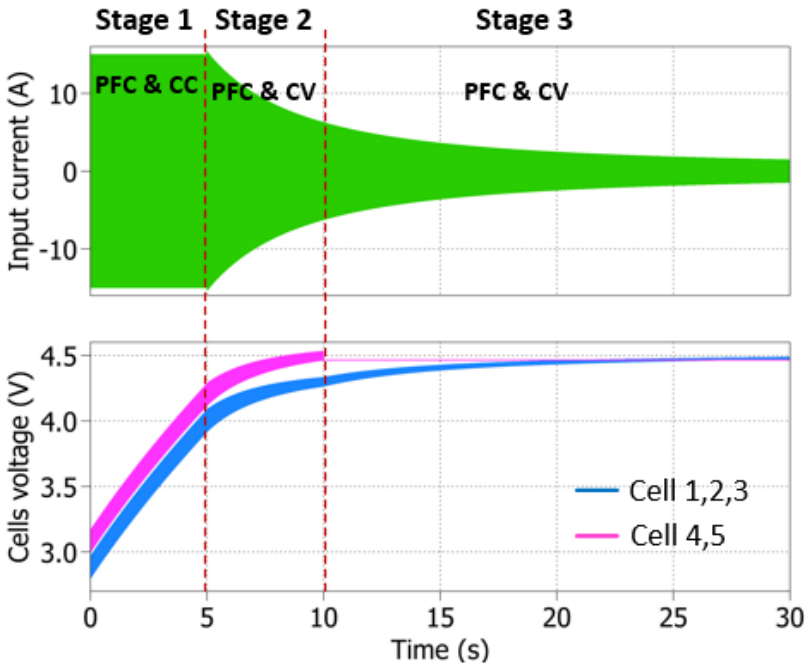


Figure 4- 21 – Waveforms for PFC and CC-CV control by charging from CC to CV.

Figure 4-22 shows the harmonic contents in the above current waveform with THD and PF in the three charging stages.

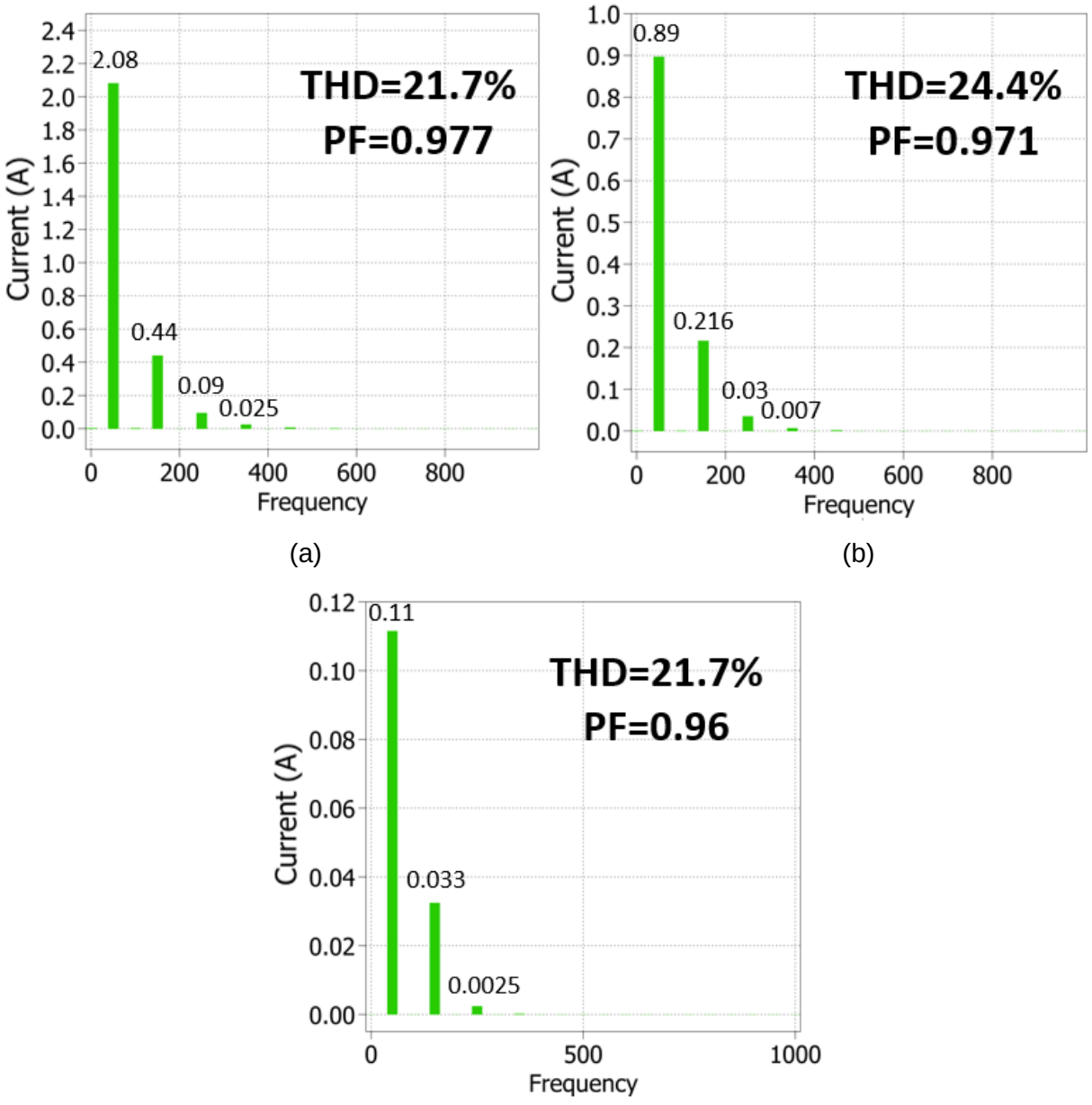


Figure 4- 22 – Harmonic content of the current waveforms in Figure 4-21: (a) stage 1, t = 2.5s; (b) stage 2, t = 7.5s; (c) stage 3, t = 15s.

4.4 Summary

A closed-loop controller has been developed for the proposed multi-functional circuit operating as a grid charger. The controller is able to control the PF under various load conditions. Furthermore, the controller is able to charge the batteries in CC-CV modes depending on the state of health of the battery cells.

The controller consists of two control circuits activated by a selector according to the voltage levels of the cells. The PFC and CC control is used in the early stages of charging to the charge battery cells with a large current, while the PFC and CV control is applied when the voltage of battery cells becomes closer to rated value, protecting cells from overcharging. The next chapter introduces the development of the testing system for the practical work in this study.

Chapter V Experimental Implementation, Results and Discussion

This chapter presents the experimental part of the project. In the first section, a system based on the proposed circuit is introduced, including the hardware and software design. The system is then utilised to test the feasibility of the circuit as both a grid charger and an equaliser. The second section then provides a demonstration and analysis of the experimental results.

5.1 Design and implementation of test system

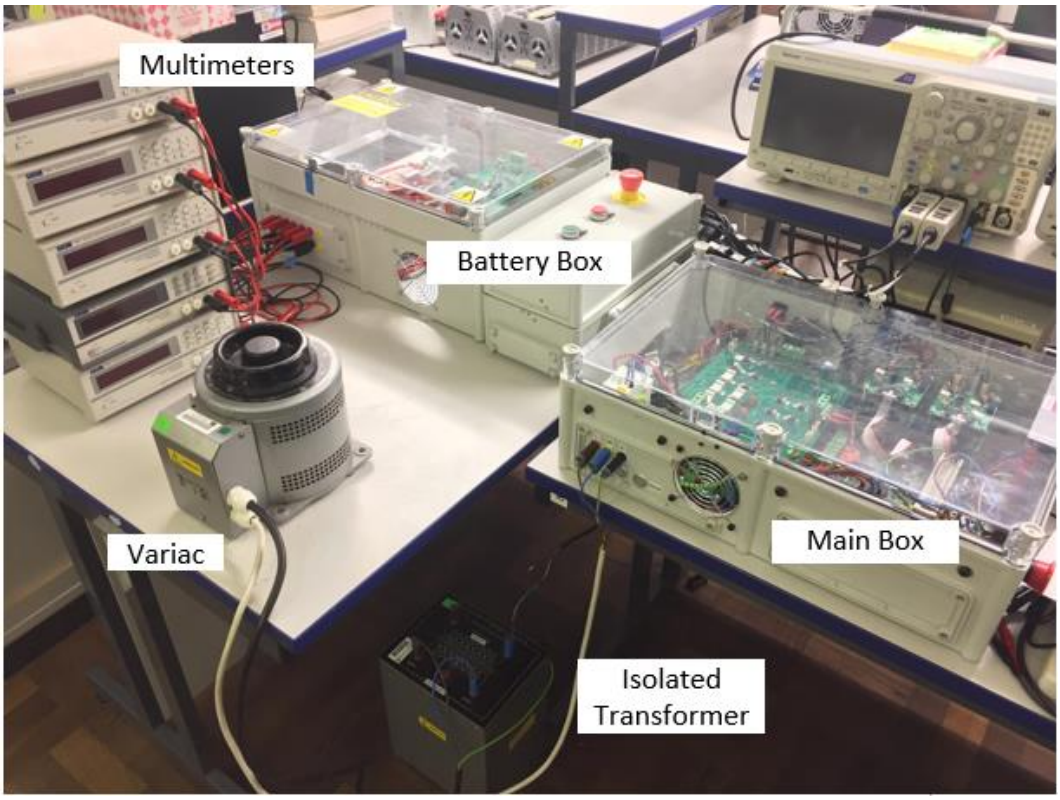


Figure 5- 1 – Photograph of the testing prototype.

5.1.1 Hardware implementation

Figure 5-1 shows a photograph of the testing system in which the proposed charging and equalisation board along with the digital signal processor (DSP) and gate drive boards are assembled in the main box, while the battery pack and its protection boards are kept in the battery box. Beside this, multimeters are connected to the battery cells to monitor their voltage during system operation. The isolated transformer and the

variac connected between the grid and the main box play the roles of isolation and regulating the input voltage.

(a) Main box

To avoid damage to both humans and circuits due to short-circuits caused by any accidental contact, the proposed converter along with the power supply unit (PSU), the DSP, and gate drive boards are constructed in a protective enclosure named the main box, the photograph of which is shown in Figure 5-2.

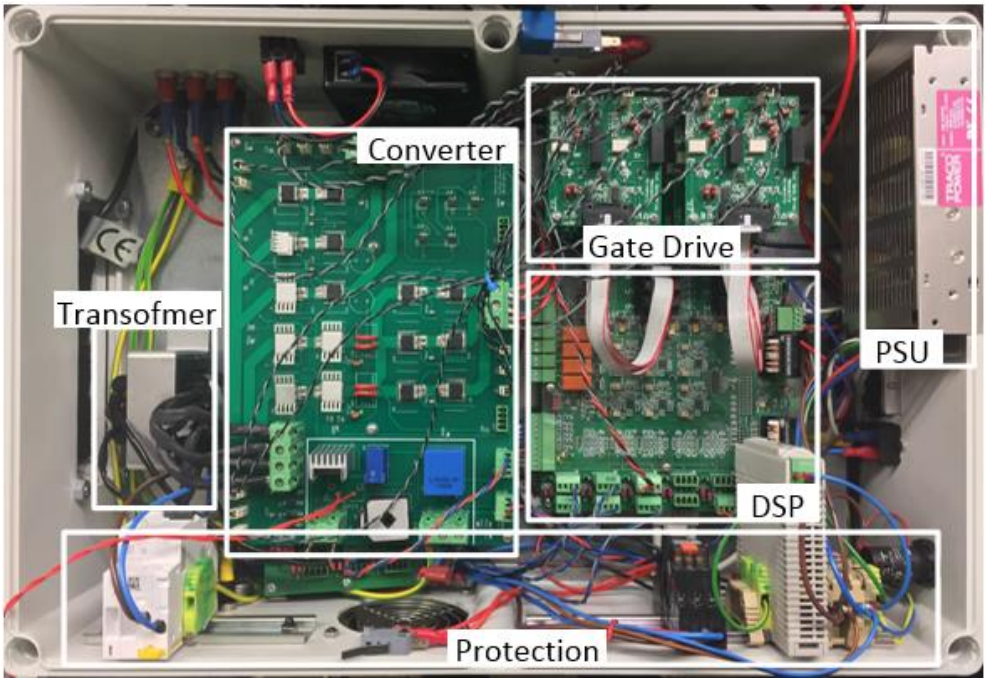


Figure 5- 2 – Photograph of the main box.

The converter and the transformer make up the structure of the proposed charging and equalisation circuit. The schematic circuit of the converter board is shown in Appendix C. Through shrouded terminal blocks, the converter board can be connected to both the main grid and battery loads. The rectifier, RCD snubber, and MOSFETs in the winding and cell selectors are assembled on the converter board.

The input rectifier used in the circuit is the GBPC2504W from Fairchild, which the forward voltage and current are 400V and 25A. The forward voltage drop per leg is 1.1V. A Silicon Carbide power MOSFET C2M0080120D from CREE is selected as the main switch. The rated drain-source voltage is 1200KV to handle the high voltage across the primary winding of the transformer. Compared to the main switch, switches in the winding selector and cell selector are not designed to stand a high voltage, however, low drain-to-source on-resistance is the most important consideration. In this

case, the MOSFET AUIRFS8409-7P is chosen as the on-resistance of a single device is as low as 0.55mΩ.

A Hall voltage sensor LV25-P and a Hall current sensor CAS 6-NP are employed to collect voltage and current information in the primary side, while, in the secondary side, five differential amplifiers AD629 are utilised to measure the individual cell voltages. The voltage and current data are sampled and scaled by protection circuits which will be introduced in the next section, before being fed into a digital signal controller (DSC).

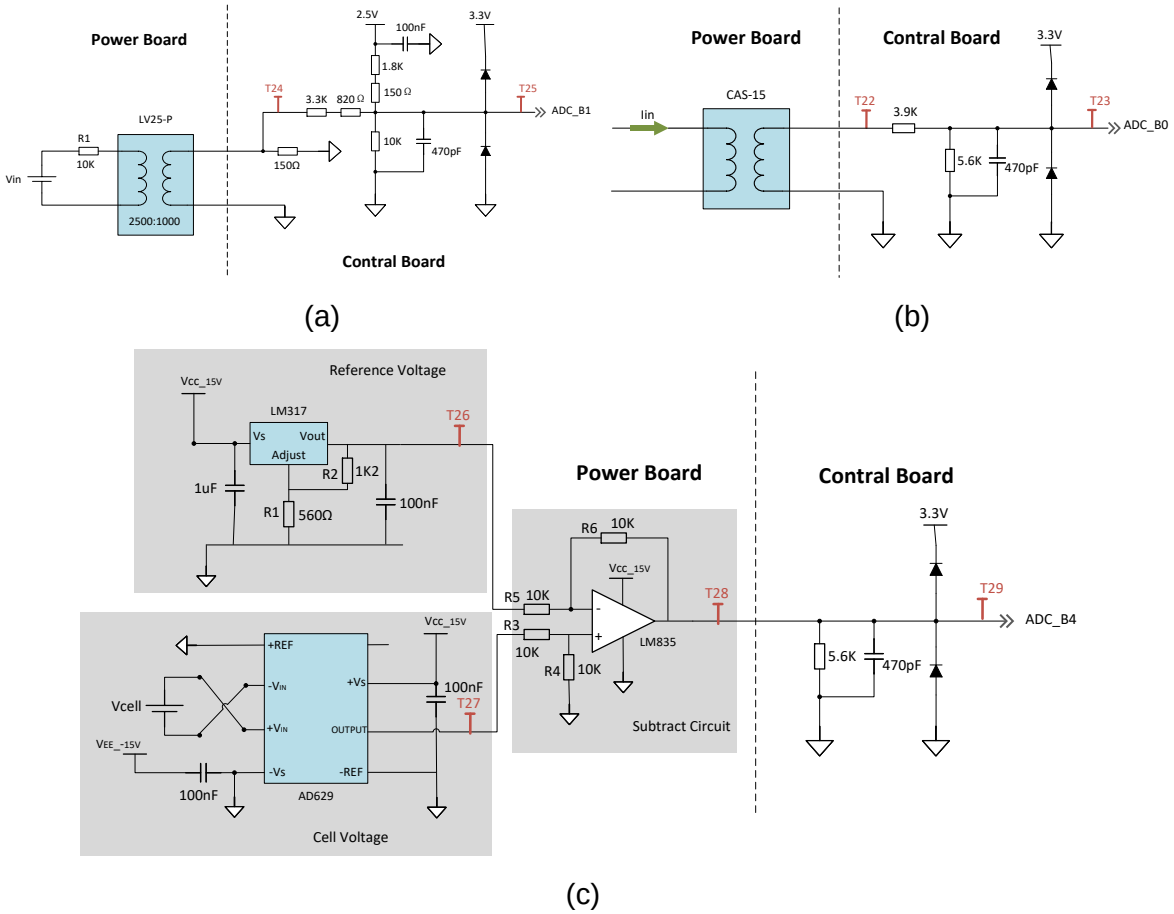


Figure 5- 3 – Signal regulation circuits for (a) Hall voltage sensor LV 25-P; (b) Hall current sensor CAS-6NP; (c) Differential amplifier AD629.

A Texas Instruments TMS320F28335-based DSP controller is utilised as the processor in the system with the functions of voltage and current signal sampling and processing, digital PI control, and generating commands to the gate drive boards. It contains many useful peripheral modules, including a general purpose input and output (GPIO) module, an analogue to digital converter (ADC) module, and an enhanced pulse width modulator (ePWM), to name a few. In this project, an interface board is employed which contains 10 input channels of 12-bit ADC, and six pairs of ePWM outputs. Since the analogue input of the ADC module is up to 3V, an auxiliary circuit is added to the

interface board before each ADC input to protect the DSP. The value in each auxiliary circuit is selected according to the output range of the corresponding sensor, Figure 5-3 shows the auxiliary circuits for the Hall voltage sensor, Hall current sensor and differential amplifiers.

For the Hall voltage and current sensors, the output signal is scaled down by resistive division. Meanwhile, since the voltage of each cell and their voltage differences are the targets, and the terminal voltage for one battery cell is limited, using resistive division to cell voltages will further reduce the voltage differences and as well as the tolerance for error. For example, during voltage equalisation, the voltage of two cells are 3.8V and 3.2V, respectively, and the voltage gap between them is 0.6V. If using a resistor divider to reduce the voltage signal by one-third, the cell voltages will be 2.5V and 2.1V with the voltage gap reduced to 0.4V.

To avoid the narrowing of the voltage difference, a subtraction circuit based on a dual-operational amplifier LM358-N is used to adjust the voltages within 3V. The schematic circuit is shown in Figure 5-3(c). The cell voltage is detected by AD629 and sent to LM 358-N as non-inverting input. Meanwhile an adjustable voltage regulator LM317 offers a reference voltage which is set by its input voltage and two external resistors as follows:

$$V_{ref} = 1.25\left(1 + \frac{R_2}{R_1}\right) = 1.25\left(1 + \frac{560\Omega}{1200\Omega}\right) = 1.83V \tag{5.1}$$

The voltage difference between the non-inverting input (cell voltage VT27) and the inverting input (voltage reference VT26) is obtained by LM358-N, and the output VT28 is based on external resistors R5 and R6 as:

$$V_{T28} = \frac{R_6}{R_5}(V_{T27} - V_{T26}) \tag{5.2}$$

When the external resistances of R5 and R6 are identical, the output of LM358-N is equal to the voltage difference between the cell voltage and the reference:

$$V_{T28} = V_{cell} - 1.83V \tag{5.3}$$

In this method, the cell voltages of 3.8V and 3.2V are regulated to 1.97V and 1.37V respectively, with the voltage gap maintained at 0.6V.

In the DSP, analogue signals of the cell voltages along with the input voltage and current are converted into digital values in the ADC module. With the employment of

the software suite Code Composer Studio (CCS), programs based on the proposed control strategy can be developed, and then complex pulse width switching signals are generated from the ePWM module which are fed to the gate drive block.

The gate drive block consists of six dual-gate drive boards arranged in three layers, which are responsible for converting switching signals to gate drive signals. Each of the dual-gate drive boards is capable of generating a pair of gate drive outputs, either independent or identical/complementary. These outputs are used to drive the MOSFETs on the converter board.

The main box is also equipped with an auxiliary protection circuit comprising emergency switches, micro switches, relays and circuit breakers. Both the DSP and the protection circuits are powered by the power supply unit (PSU).

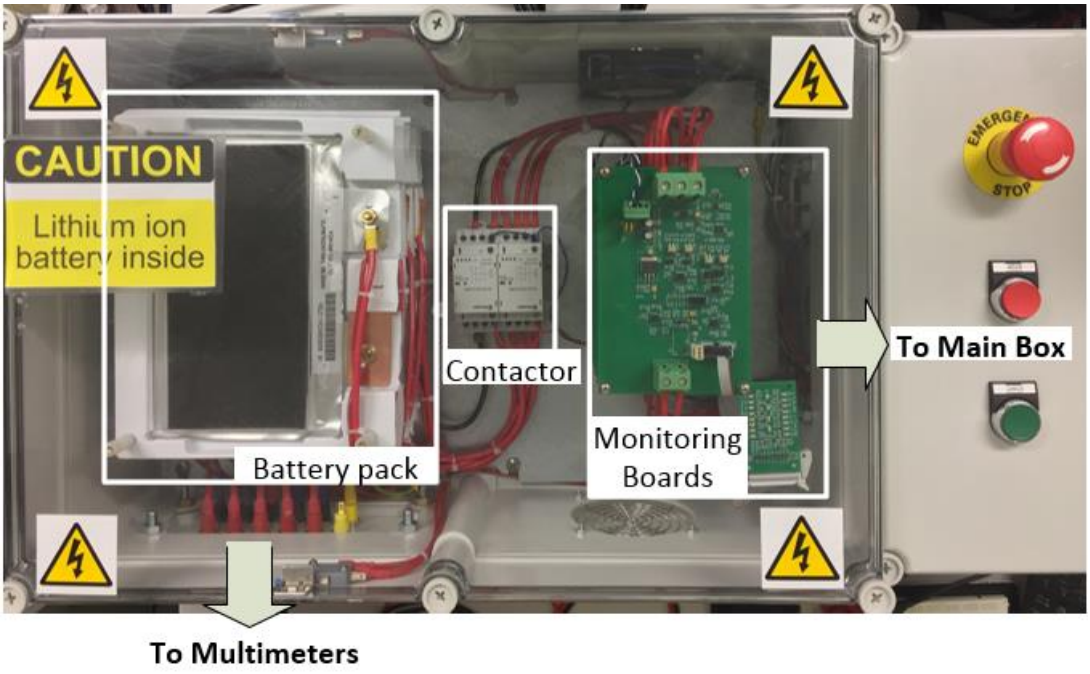


Figure 5- 4 – Photograph of the battery box.

(b) Battery box

To maintain a safe operating environment for the batteries, battery cells are kept in a standalone enclosure with monitoring boards and protection circuits. A photograph of the battery enclosure is shown in Figure 5-4.

The battery pack is composed of five lithium-ion battery cells which are connected in series using copper bus bars. The battery cells used in the test are from Kokam, a pioneering manufacturer of Lithium-ion / Polyer batteries. The model number of the

battery is SLPB78205130H and the key specifications of the cell are listed in Table 5-1.

The battery box is designed with interfaces on the front and the right-hand sides. The interface on the front consists of ten shrouded sockets connected to two terminals for each battery cell through which an individual cell is connected to a multimeter in order to monitor its voltage in real time. The interface on the right-hand side contains six shrouded sockets, corresponding to the six joints in a five-cell pack as shown in Figure 3-11(b), allowing the connection between the main box and the battery box.

Table 5- 1 – Specifications of battery module

Capacity (Ah)	16	Charging C-rate			
Weight (g)	406	Continuous	4C	Pulse	8C
Energy Density (wh/kg)	146	Discharging C-rate			
Voltage Range (V)	2.7-4.2	Continuous	8C	Pulse	15C
Internal Resistor (mΩ)	1.1				

Between battery cells and terminals to the main box, the battery enclosure is equipped with a monitoring unit integrated with a contactor aiming to protect the battery cells from over-charging and over-discharging. There are five monitoring boards in the stack and each is responsible for an individual cell, comparing the cell voltage with two threshold values (2.7V and 4.2V). Monitoring boards and battery cells are connected via a contactor in which the contactor coil is energized through a MOSFET. Once the voltage of one cell is detected to be below or over the rated range, a logic low signal will be sent to the gate of the MOSFET to disconnect the contactor coil, and to further isolate battery cells from the main box.

(c) Battery pre-charging

For the purposes of demonstrating that the performance of the proposed system is identical to that of the simulated circuit presented in the previous two chapters, cells in the battery stack need to be pre-charged to a fixed initial state before each experiment. The initial voltages of the cells are set according to the different operational modes described in section 3.3. In this project, pre-charging is accomplished using a research

grade potentiostat system as shown in Figure 5-5. The potentiostat can be used as a charging power source and a discharging load, and therefore it is capable of either charging or discharging a cell to a pre-set voltage.

Figure 5- 5 – Photograph of the research grade potentiostat system.

5.1.2 Software implementation

Until recently, analogue controllers have been commonly used in practical applications due to cost considerations. However, in these controllers, compensation parameters such as resistors and capacitors are highly dependent on variations in temperature and ageing issues [118]. Compared to analogue ones, controllers implemented digitally ensure higher accuracy, since temperature and ageing issues can be mitigated. Moreover, digital controllers show better performance in terms of improved reliability and greater design flexibility [119-121]. Therefore, in this thesis, a digital controller is implemented to fulfil the functions of PFC and CC-CV charging.

The rectified voltage and current in continuous time are detected and scaled by the Hall voltage and current sensors, and the signals are fed into the ADC module on the DSP. The sampling frequency of the ADC module is set to be as the same as the switching frequency, and the start-of-conversion trigger arrives at the middle point of every switching period, both of which can be accomplished in the programming. The diagram for sampling the voltage and current is shown in Figure 5-6. When a sampling request arrives, the sampled voltage is equal to the value of rectified voltage, while the

current is still increasing. Since the current follows linear growth, the peak value can be regarded as twice the value of the sampled current.

The code programmed in the DSP is developed in CCS to realise different functions, meeting various demands in the experimental testing such as communication between the user and the system and accomplishing the digital PI control.

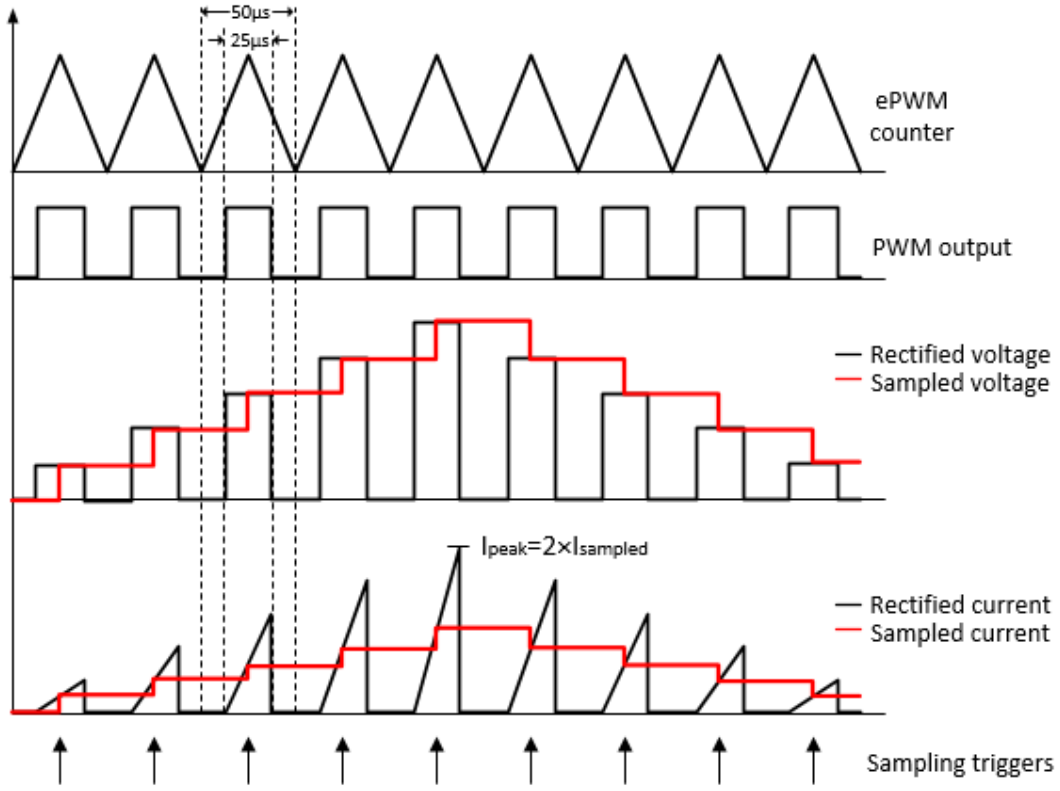


Figure 5- 6 – Diagram of the sampling of voltage and current signals in the ADC module.

The main code of the program is presented in Appendix B. The program starts with the initialisation code, which includes variable definitions and configurations for all relevant registers. Then the Labview data exchange loop is executed, which is responsible for continuous communication between the DSP and the Labview user control panel via the RS232 interface. The communication is two-way, including receiving commands from the user control panel, and sending collected data back to the user. For each switching period, the code is set to jump into the interrupt service routine (ISR) and to complete these tasks, including ADC sampling, digital PI control and updating data. The sampled values of the rectified voltage and current in the ADC converter (Figure 5-5) are fed into the control algorithm unit. This unit achieves the function of calculation in the digital PI controller to guarantee the stable operation of the circuit. Part of the Labview user control panel is shown in Figure 5-7. States of cell voltages are monitored

and displayed in this panel. The panel is designed to be adjustable so that users can switch manually between open-loop control and close-loop control. In addition, some parameters used in the controller can be adjusted manually from the panel to change the operational condition of the converter.

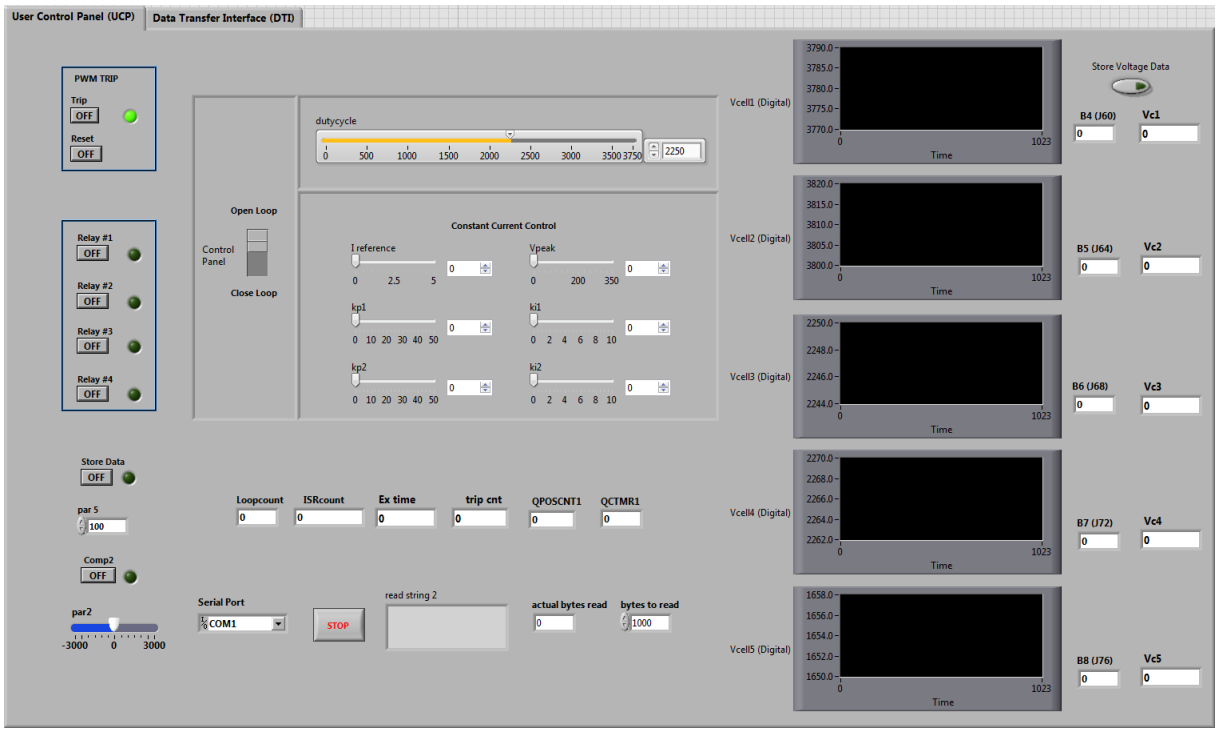


Figure 5- 7 – Part of the user's control panel in Labview.

Data exchange between the DSP and the control panel is repeated at a rate of 5 updates per second, which is determined by the Labview control panel. Thus, cell voltages are displayed in the panel in real time. However, since cell voltage changes slowly in the batteries, users cannot observe the overall voltage change from the panel when the charging or equalisation process lasts for several hours. In order to record the voltage changes throughout the process, cell voltages can be saved as a data file which is stored in the user's computer at a rate of one update per second, but only when the data storage function is switched on.

From the simulation results shown in Figure 3-30, it can be observed that the cell voltage is not constant in a switching period, since there are voltage drops or rises due to the change in current. And in practice, there are oscillations in cell voltages caused by the resonance which occurs between the cell and the winding inductor, as shown in Figure 5-11. This will lead to imprecise voltage measurements while the system operates, and the cell voltages shown on the control panel are extremely unstable and may jump about over a large range. Hence, a function has been realised using the

code so that either the charging or the equalisation process is paused every 200ms when the cell voltages are sampled and sent to the control panel. Figure 5-8 shows an example of the gate drive signals during voltage equalisation between B1 and B2. During the pause, all the three MOSFETs are turned off for 2.5ms.

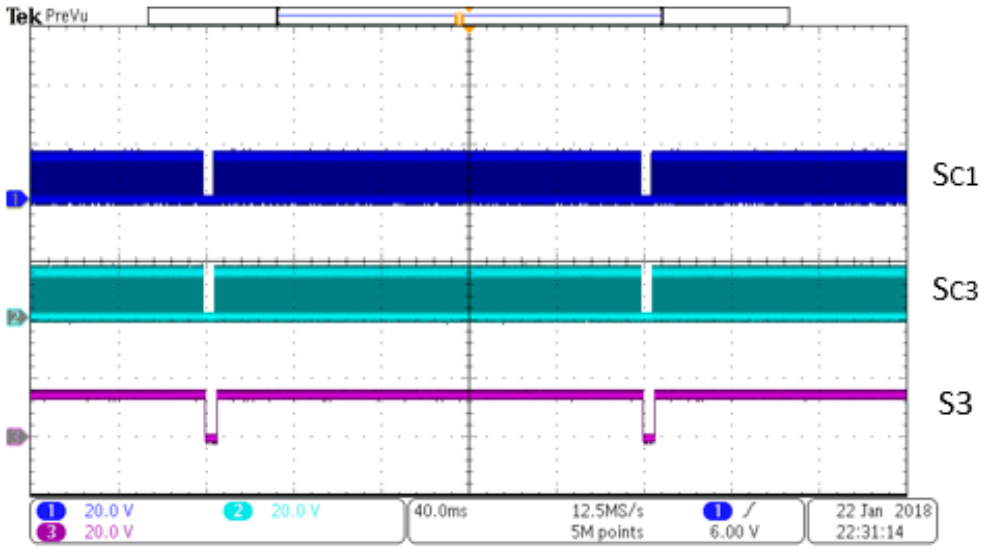


Figure 5- 8 – Switching signals for MOSFETs with pauses every 200ms.

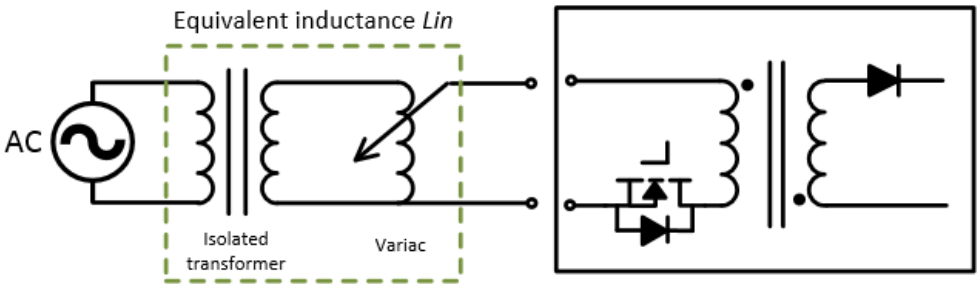
5.2 Experimental results

In this section the system is tested in several scenarios to demonstrate its feasibility as both a charger and an equalisation circuit. Experimental results are presented and discussed, as well as the impact of various parameters on the operation of the circuit.

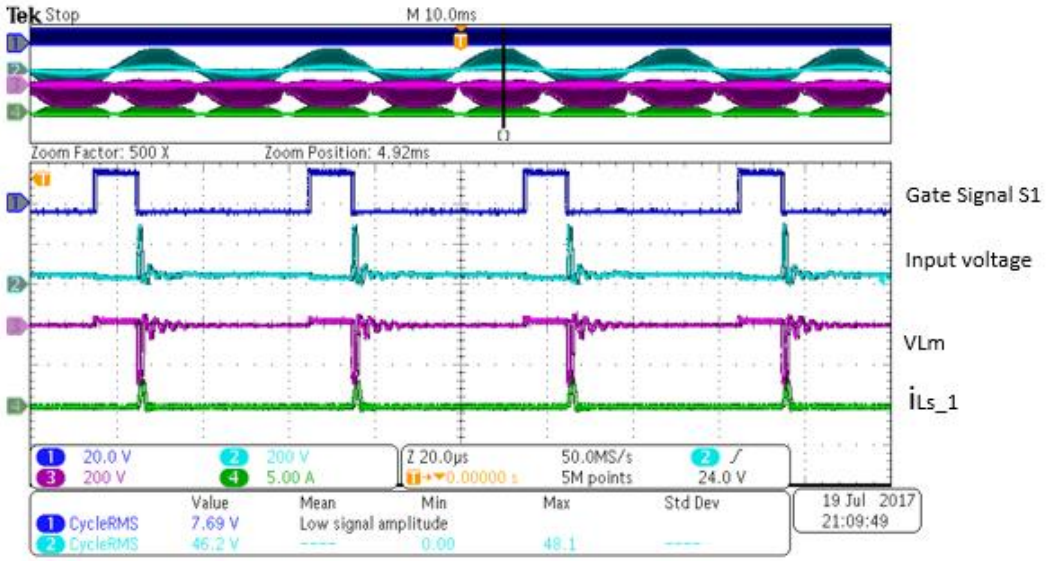
5.2.1 Battery charging

The circuit is designed to be connected to the grid directly when it operates as a battery charger. Hence, as shown in Figure 5-1, the input ports of the main box are connected to a socket via an isolated transformer and a variac. The isolated transformer aims to achieve galvanic isolation between the system and the grid, as well as a protection for the experimental participants, while the variac is used to adjust the input voltage to the system. However, the employment of the transformer and the variac introduces a large equivalent inductance L_{in} (measured as 4.5uH) into the input circuit, as shown in Figure 5-9(a). This inductance will further cause a large voltage spike during the operation of the circuit when the switch in the primary side of the circuit turns off. Even worse, this voltage spike will be superimposed onto the primary winding of the transformer and the MOSFET, increasing the voltage stress on these devices. The waveforms shown

in Figure 5-9(b) indicate that, with an input voltage of 30V, the spike in the input voltage (CH 2) when the MOSFET turns off is up to 310V.



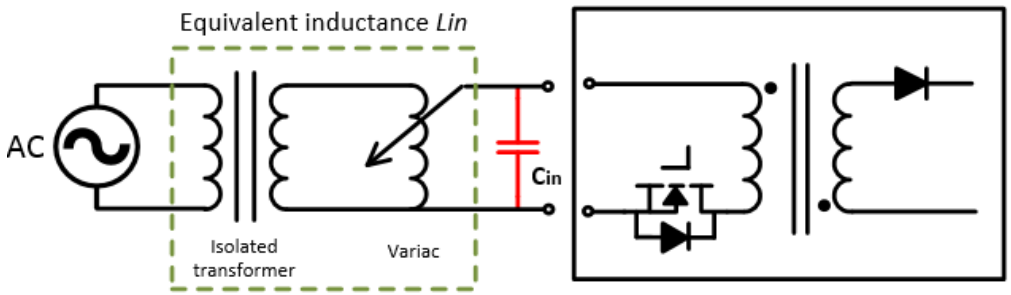
(a)



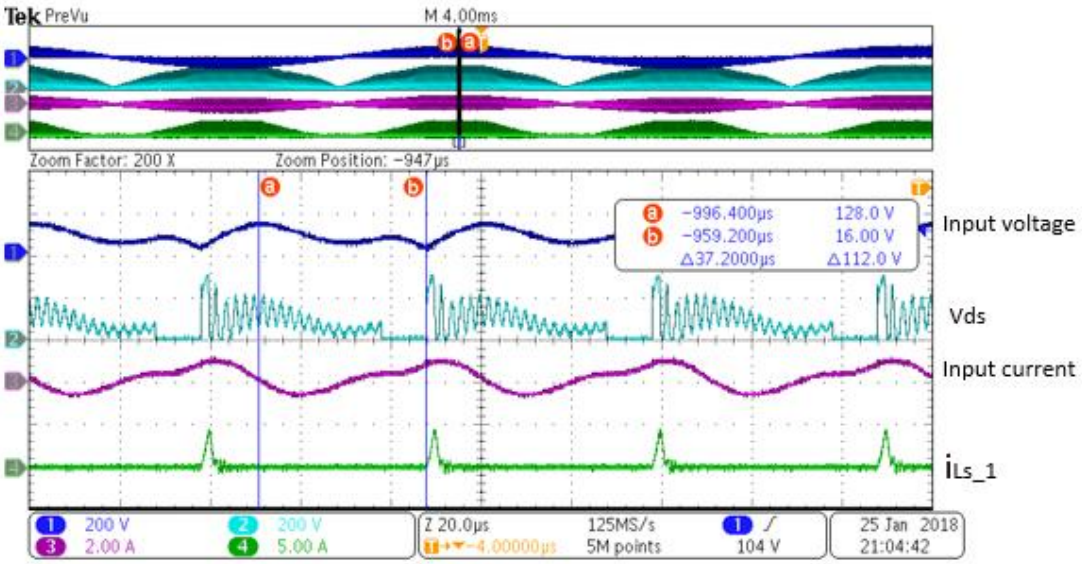
(b)

Figure 5- 9 – Isolated transformer and variac: (a) diagram of the input circuit; (b) waveforms with the input circuit.

An input capacitor *Cin* was shunted at the input port of the main box, as shown in Figure 5-10 (a), in the expectation that the spike in the input voltage can be clamped. Figure 5-10 (b) shows the voltage and current waveforms when the input voltage is 30V, with *Cin* of 80nF. The input voltage (CH1) varies in the range of 16V to 128V and the waveform is smoother without any spike, and the voltage across the MOSFET (CH2) has clamped the spike of 260V.



(a)



(b)

Figure 5- 10 – Input capacitor: (a) diagram of the input circuit; (b) waveforms with the input circuit.

However, oscillations occur in both the input voltage and current, with the frequency measured as 35kHz. This oscillation is considered to be the result of the resonance between the input capacitor and the equivalent inductor of the primary winding of the transformer, since:

$$f_1 = \frac{1}{2\pi\sqrt{L_m C_{in}}} = \frac{1}{2\pi\sqrt{350uH \cdot 80pF}} = 30kHz \tag{5.4}$$

Meanwhile, there are oscillations in the waveform of *Vds* with a much higher frequency, which is measured as 250kHz. This is regarded as the result of the resonance between the input capacitor and the equivalent inductor of the isolated transformer and the variac on the input circuit. The frequency in theory is:

$$f_2 = \frac{1}{2\pi\sqrt{L_{in} C_{in}}} = \frac{1}{2\pi\sqrt{4.5uH \cdot 80pF}} = 265kHz \tag{5.5}$$

To eliminate the oscillations in the waveforms, an AC power supply is utilised instead of the combination of the grid, the isolated transformer and the variac, as shown in Figure 5-11. In this way, the input capacitor is also no longer needed.

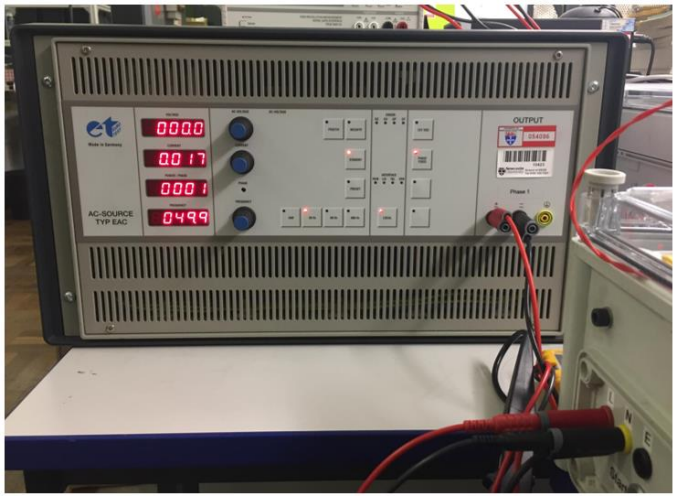


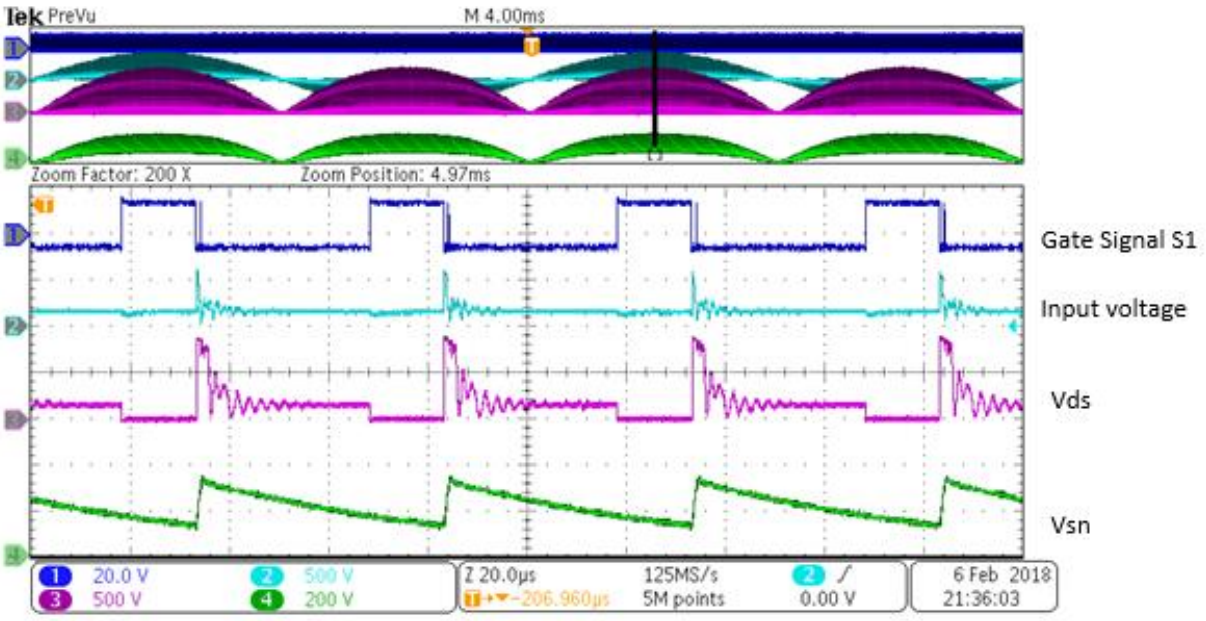
Figure 5- 11 – The AC power supply in the system.

In this test, the voltage level of the AC power supply is limited up to 100V rather than the 230V in the simulation. This is because there are five cells in the battery pack, and the turns-ratio of the transformer is 11:1:1. A large input voltage leads to a large input current in the primary coil and a larger current in secondary coils, which may cause damage to the devices in the secondary side including the switches and cells. Besides, the power level for a flyback converter is quite limited, normally up to 200W. To further increase the power level, the circuit may need to be redesigned with the flyback converter replaced by an interleaved structure. The duty cycle of the control signal for S1 is 0.3 to limit the current level in both the primary and secondary windings.

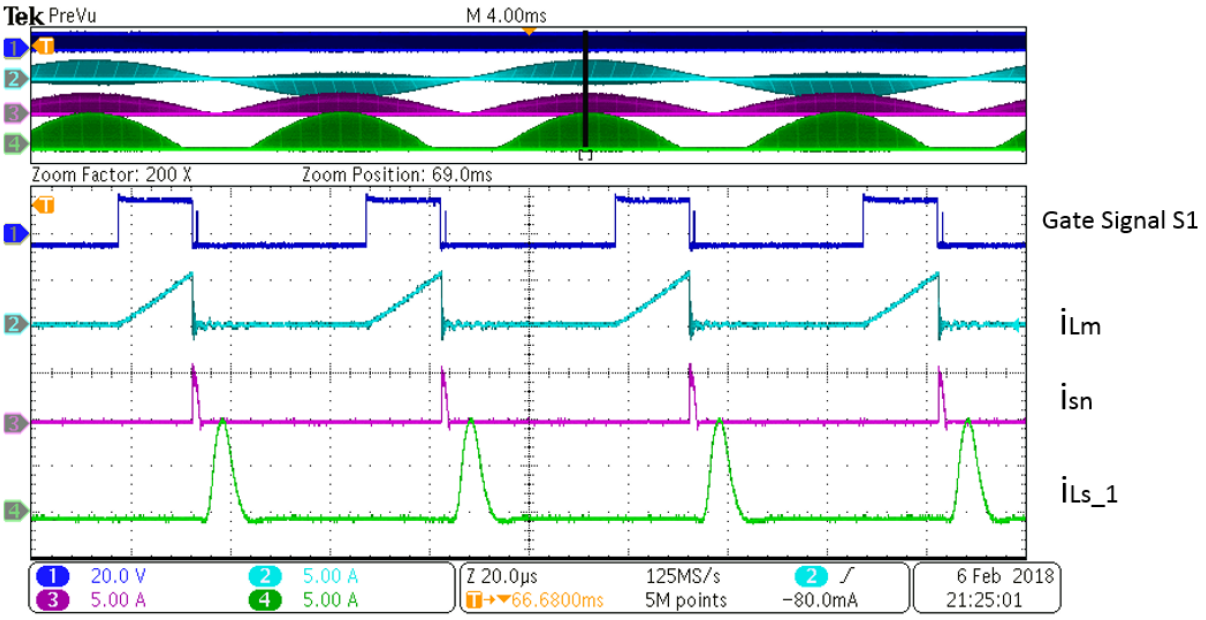
In this test, the circuit operates as a battery charger with open-loop control and targets to the whole battery pack B1 to B5, as the operational Mode 1. Five cells have different initial voltage level, they are at 3.08V, 3.25V, 3.33V, 3.37V and 3.44V respectively. The charging process is completed in two parts. Firstly, all the five cells are charged. It followed by step two that only B1 is continuously charged since its relatively low voltage.

Figure 5-12 shows the key waveforms during the charging stage that all the five cells are charged. Figure 5-12(a) shows the input voltage, and the voltage across S1 and the snubber capacitor, in which the voltage across the MOSFET is clamped at about 870V. Figure 5-12(b) presents the current waveforms, including the current through both the primary and the secondary winding of the transformer and the current flowing

into the snubber circuit. In comparing the voltage and current waveforms with the waveforms shown in Figure 3-28 and Figure 3-25, it is clear that the experimental and simulation results are basically the same, and it is concluded that the circuit is operating as expected.



(a)



(b)

Figure 5- 12 – Experimental results when charging five cells with fixed duty cycle: (a) voltage waveforms; (b) current waveforms.

When the system operates under open-loop control, since the duty cycle of the switching signal is fixed at 0.3 and there are energy losses in the circuit, the demagnetising current in the secondary winding *iLS_1* always falls to zero before the

next switching period, which means that the transformer is not saturated and the circuit operates with a fine power factor.

The charging process is divided into two steps. In the first step, all five cells are charged, and the cell voltages increase at the same speed. After being charged for about 2 hours and 40 minutes, all battery cells have reached 3.7V except for B1 with only 3.5V. Hence, in step two only B1 is charged, and the voltage of B1 increases from 3.53V to 3.83V within one hour. Since the duty cycle of the switching signals is unchanged, the energy converted from the grid to the load in one switching period is the same, and all of the energy goes to one cell instead of five. Therefore, the charging speed of step two is faster than the first step.

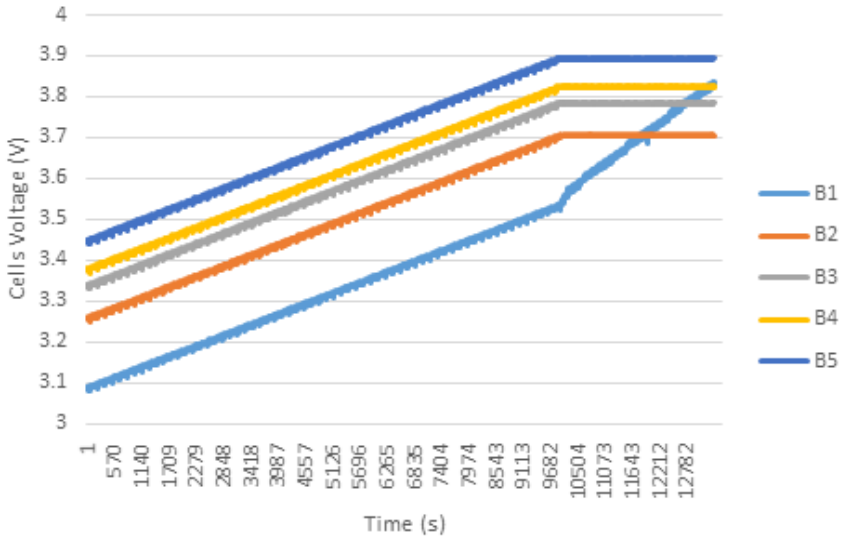


Figure 5- 13 – Cell voltages when charging B1-B5 in two steps.

Using the same method that been used in the simulation, the efficiency of the circuit can be calculated. Based on the input voltage and current in Figure 5-12, and the duty cycle, the input power of the system is:

$$P_{input} = \frac{V_{in} I_{peak} D}{2} = 82.5W \tag{5.6}$$

Figure 5-13 shows that at the end of the first charging stage, voltage of the five cell climb to 3.52V, 3.7V, 3.78V, 3.82V, and 3.88V, respectively. For battery cells with capacity of 16Ah, energy absorbed by cells during charging can be worked out:

$$E_{cells} = 16Ah * 3600 * [(3.52 - 3.08) + (3.7 - 3.25) + (3.78 - 3.33) + (3.82 - 3.37 + (3.88 - 3.44)]V$$
$$= 128448J \tag{5.7}$$

The output power of the circuit is:

$$P_{output} = \frac{E_{cells}}{T} = \frac{128448J}{9600s} = 25.09W \quad (5.8)$$

The circuit efficiency is:

$$ɧ = \frac{P_{output}}{P_{input}} = 30.4\% \quad (5.9)$$

The efficiency can be improved by improve the coupling coefficient between the primary and secondary windings of the transformer. The turns ratio of the primary and secondary winding is 11:1, however, winding currents in Figure 5-12(b) show that the secondary peak current is only the twice of the primary peak current. It indicates that the leakage inductance is quite large. By testing, the leakage inductance on the primary winding is about 15% of the magnetic inductance. It is possible to further reduce the leakage inductance to 10% or even smaller level, which would be helpful to improve the efficiency. Besides, as has been discussed in section 3.4, a larger snubber resistor in the RCD circuit would be helpful to reduce the power dissipation as well.

Figure 5-13 shows the harmonic contents within 1kHz in the input current generated from MatLab. The fundamental current is 0.9664 A. The magnitude of the 3rd harmonic is estimated to be about 0.03A, and higher harmonics such as 5th, 7th, etc. are even smaller. Since the current is a pulsed sine wave and the switching frequency is 20kHz, the magnitudes of harmonics at frequencies of 20kHz, 40kHz, etc. are high. The harmonic contents in an extended frequency span are shown in Appendix A. Large harmonics at 20kHz and 40kHz lead to a poor THD of 175.65%. According to the THD, the PF of the system is expressed as:

$$PF = \frac{1}{\sqrt{1 + THD^2}} = \frac{1}{\sqrt{1 + 1.7565^2}} = 0.495 \quad (5.6)$$

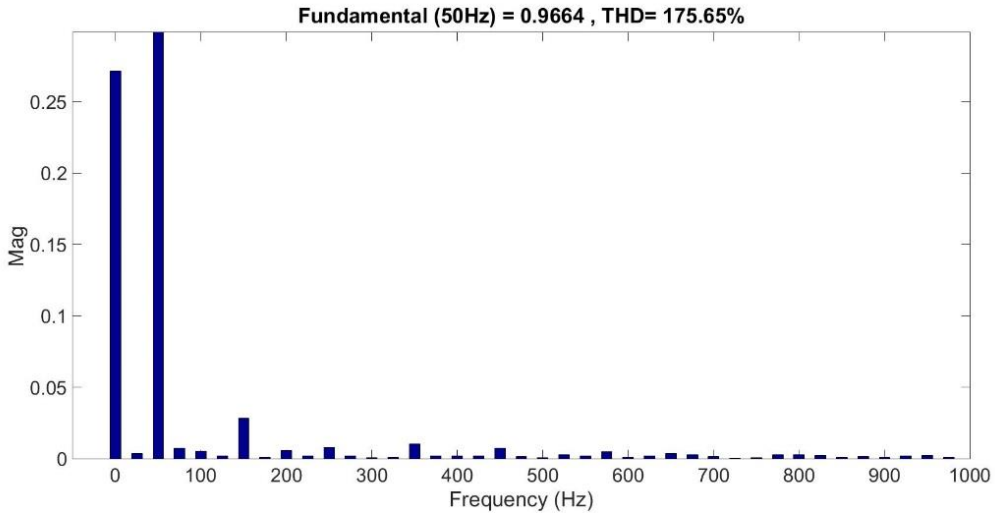


Figure 5- 14 – Harmonic contents in the input current in Figure 5-12.

Even though odd harmonics in the input current are low when the circuit operates under open-loop control, CC-CV charge is still needed to protect battery cells from over-charging. To testify the close-loop controller, another test is done with the circuit operating in Mode 1 but with the PFC and CC-CV control. The input of the circuit remains at 100V. Figure 5-15 shows the voltage of B1 when it is charged under the closed-loop control. The charging took place in two steps. In the first three and half hours, PFC and CC control is applied, during which the voltage of B1 rises linearly from initial voltage of 3.55V to 3.85V. In the second period, the controller is switched manually to PFC and CV control so that the charging speed in this period obviously slows down. After about another two hours, the voltage of B1 reaches 3.9V at the end of charging.

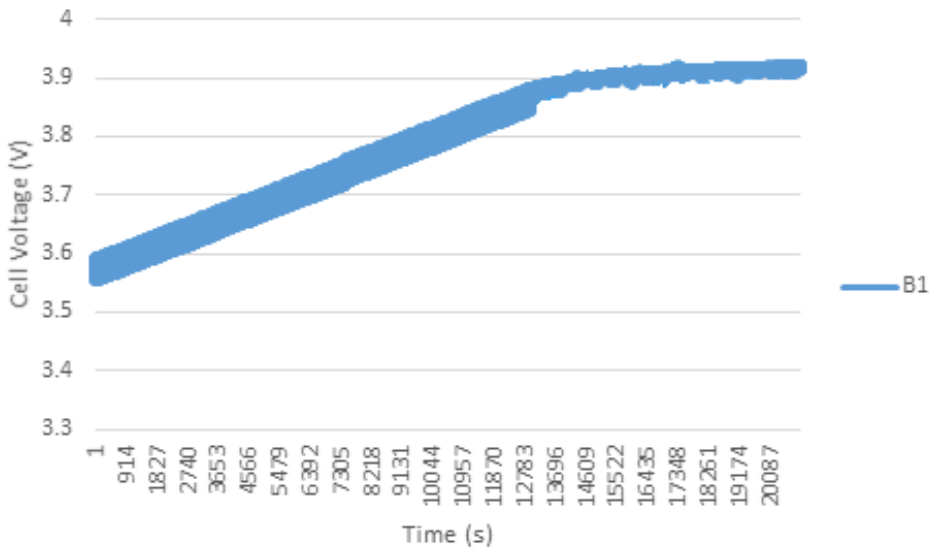
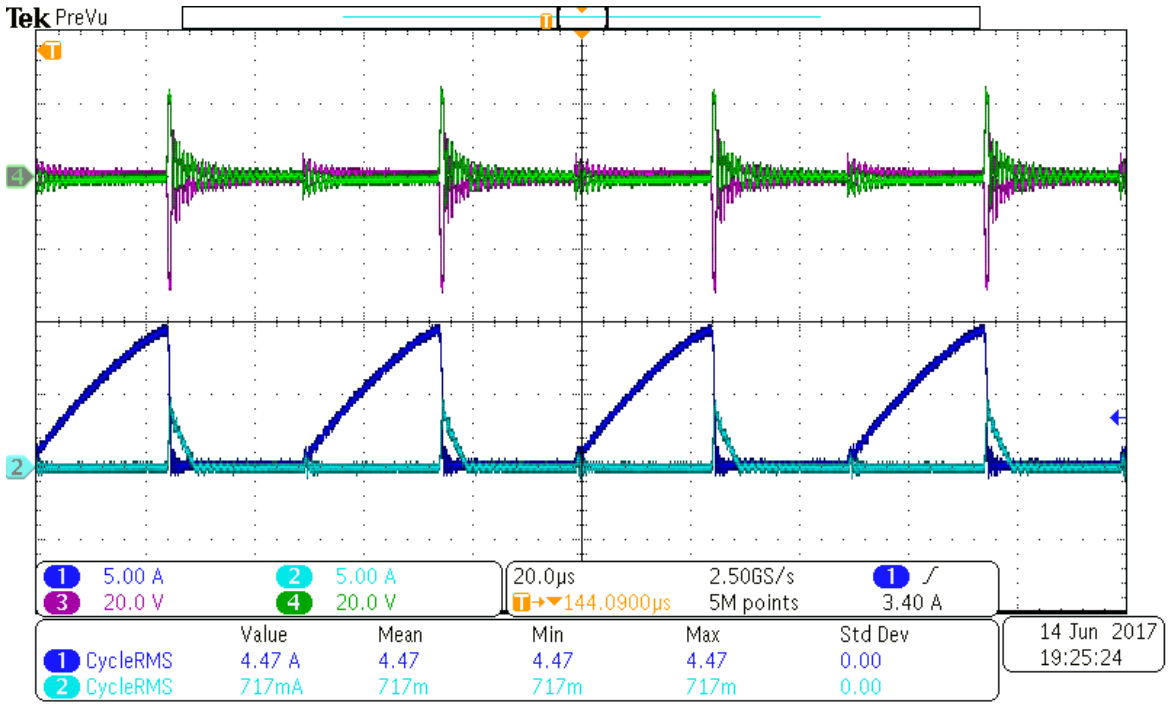


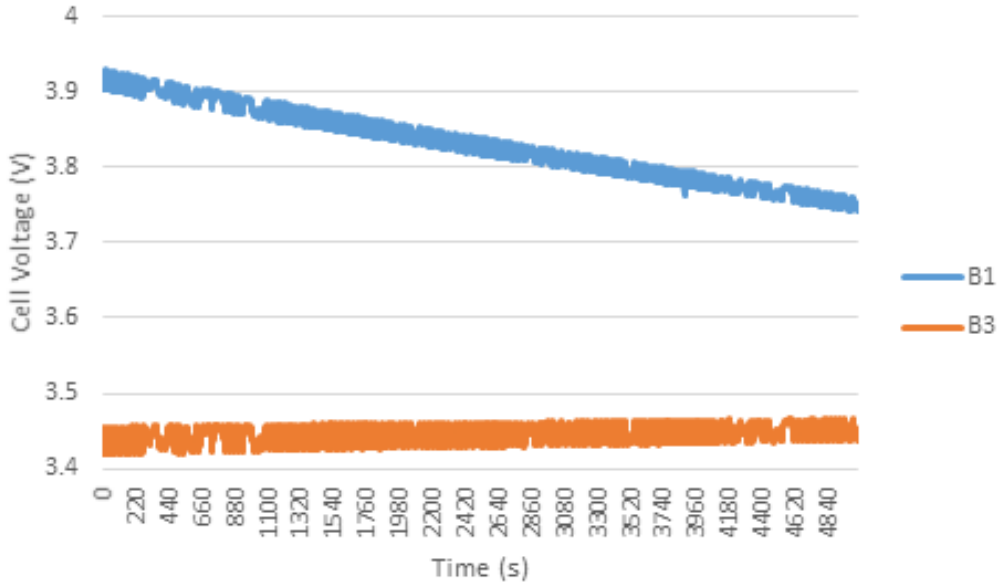
Figure 5- 15 – Voltage of B1 under CC-CV control.

5.2.2 Equalisation B1-B3

This testing scenario is designed to demonstrate the operational Mode 3 that the voltage equalisation between odd numbered cells can be achieved within the proposed circuit, which is between the source cell B1 and the target cell B3 in this experiment. The initial voltages of B1 and B3 are set at 3.71V and 3.44V respectively.



(a)



(b)

Figure 5- 16 – Waveforms of equalisation from B1 to B3 @ Lms_1=4.2uH, f=20kHz: (a) voltage and current in windings; (b) cell voltages.

Waveforms of voltages and currents in the equalisation process are shown in Figure 5-16(a). Channels 1 through 4 stand for the discharging current of B1 (i_{LS_1}, 5A/div), the charging current of B3 (i_{LS_2}, 5A/div), the voltage across the winding N_{s_1} (V_{LS_1}, 20V/div), and the voltage across the winding N_{s_2} (V_{LS_2}, 20V/div) respectively.

During operation, when the source cell B1 is discharging, the peak current reaches 9.5A. However, the peak current that charges the target cell B3 is only 4.5A. The drop in the peak current indicates low circuit efficiency. Furthermore, it causes the equalisation process to be extremely slow, since only a small fraction of the energy is transferred from B1 to B3. After 90 minutes of operation, the voltage of B1 is reduced from 3.9V to 3.75V, while the voltage of B3 only rises from 3.41V to 3.44V as shown in the voltage waveforms in Figure 5-16(b).

The low efficiency of the circuit is mainly caused by three factors. Firstly, the dead-time between the magnetising period and the demagnetising period leads to waste of energy and further causes the drop in the peak current. Secondly, the conduction of the RCD snubber circuit in the transformer's primary winding generates energy wastage as well. These two reasons have been explained in the circuit simulation in section 3.6.2. The third reason is the leakage inductance of the secondary winding. The magnetic and leakage inductances of the top secondary winding have been measured as 4.2uH and 1.49uH respectively, where the leakage inductance greatly exceeds the acceptable range. In order to prove the impact of the transformer on circuit performance, another transformer has been used in a comparative test.

The new transformer is shown in Figure 5-17. It has two windings reversed-coupled on a magnetic core, with a turns-ratio of 1:1. These two windings are connected in the circuit instead of the top and bottom secondary windings in Figure 3-18. The magnetic and leakage inductances of the transformer are measured as 44uH and 4.2uH respectively.

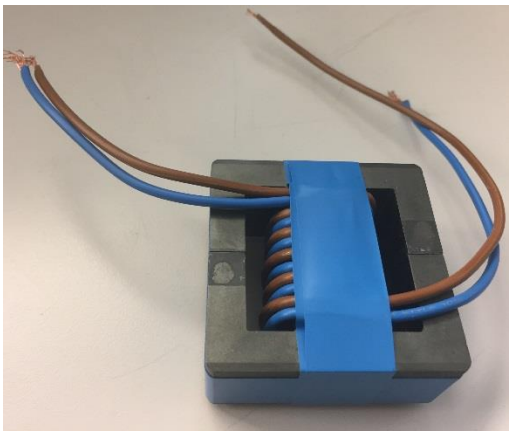
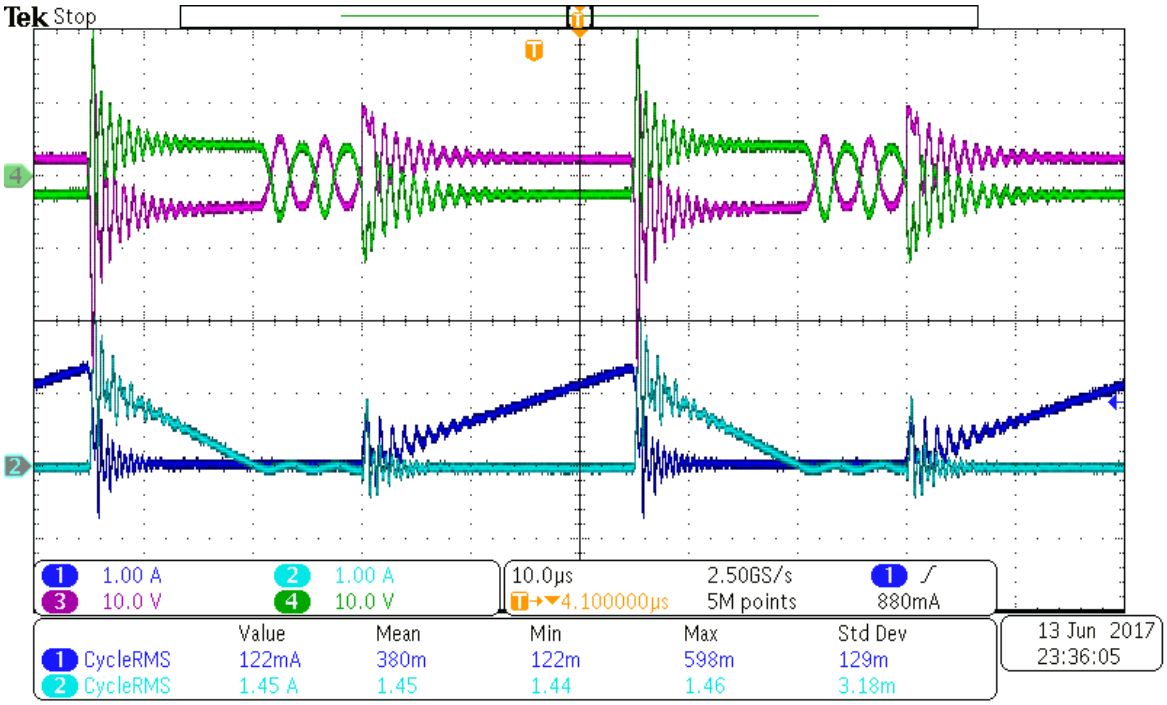


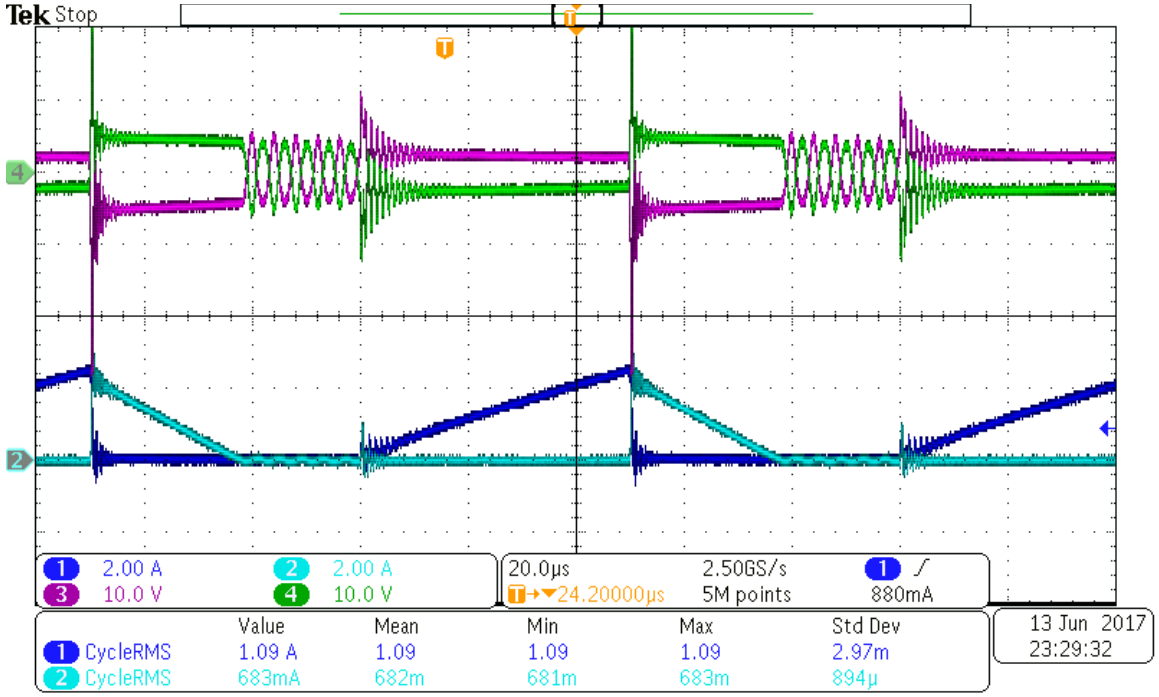
Figure 5- 17 – Photograph of the new transformer in the comparative test.

Results of the test with the new transformer are shown in Figure 5-17. In all three figures, channels 1 through 4 stand for the discharging current of B1, the charging current of B3, the voltage across the winding N_{s_1}, and the voltage across the winding N_{s_2}, respectively.

In Figure 5-18(a), the circuit is operating under a switching frequency of 20kHz and a duty cycle of 0.5. The peak magnetising current is 1.2A, which is smaller than the current shown in Figure 5-16(a) since the magnetic inductance is larger. This result also indicates that the peak current in the demagnetising period is only a little smaller than the peak current in the magnetising period, which means that a greater part of the energy has been transferred from B1 to B3 and the efficiency of the circuit has been improved. To obtain a larger equalisation current, the circuit has been operated under different switching frequency, as the results shown in Figure 5-18(b) and (c). With the lower switching frequencies, the peak magnetising current is larger, as is the peak demagnetising current.


Tek Stop
1 1.00 A
3 10.0 V
2 1.00 A
4 10.0 V
10.0µs
T→▼4.100000µs
2.50GS/s
5M points
1 ⎍
880mA
Value Mean Min Max Std Dev
1 CycleRMS 122mA 380m 122m 598m 129m
2 CycleRMS 1.45 A 1.45 1.44 1.46 3.18m
13 Jun 2017
23:36:05

(a)


Tek Stop
1 2.00 A
3 10.0 V
2 2.00 A
4 10.0 V
20.0µs
T→▼24.20000µs
2.50GS/s
5M points
1 ⎍
880mA
Value Mean Min Max Std Dev
1 CycleRMS 1.09 A 1.09 1.09 1.09 2.97m
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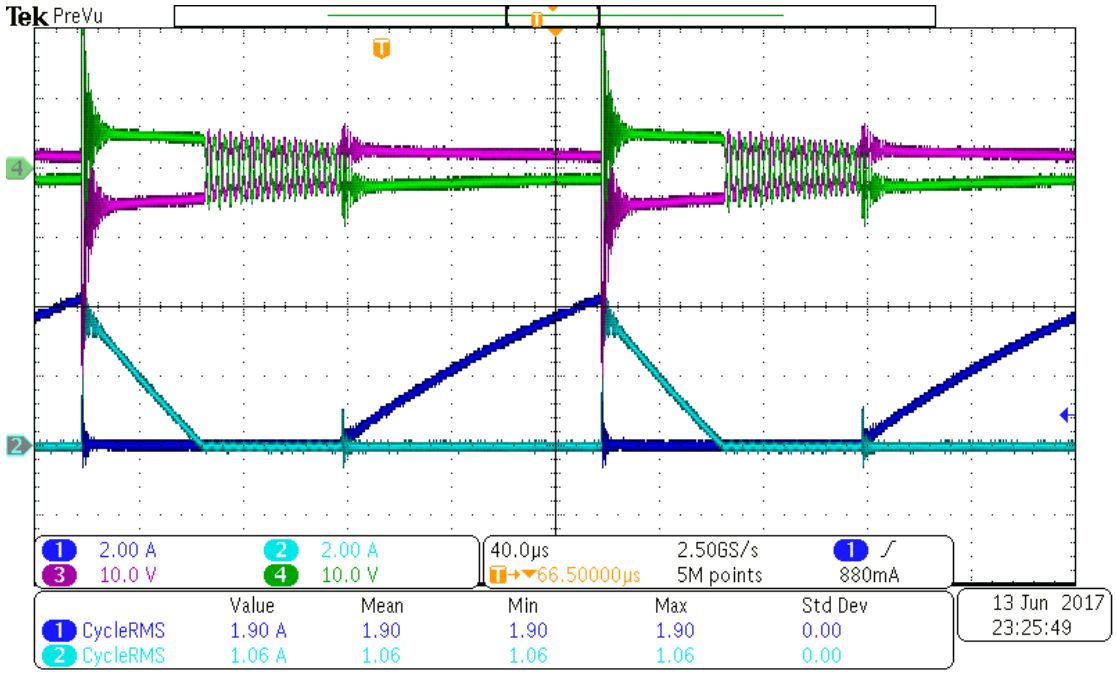
(b)



(c)

Figure 5- 18 – Waveforms of equalisation from B1 to B3 @ Lms_1=54uH, (a) f=20kHz, (b) f=10kHz, (c) f=5kHz.

Figure 5-19 shows the waveforms of the cell voltages when the circuit is operating under a switching frequency of 5kHz and a duty cycle of 0.5 with the initial voltages of B1 and B3 at 3.71V and 3.44V. It takes about 4 hours for B1 and B3 to reach a balanced voltage.

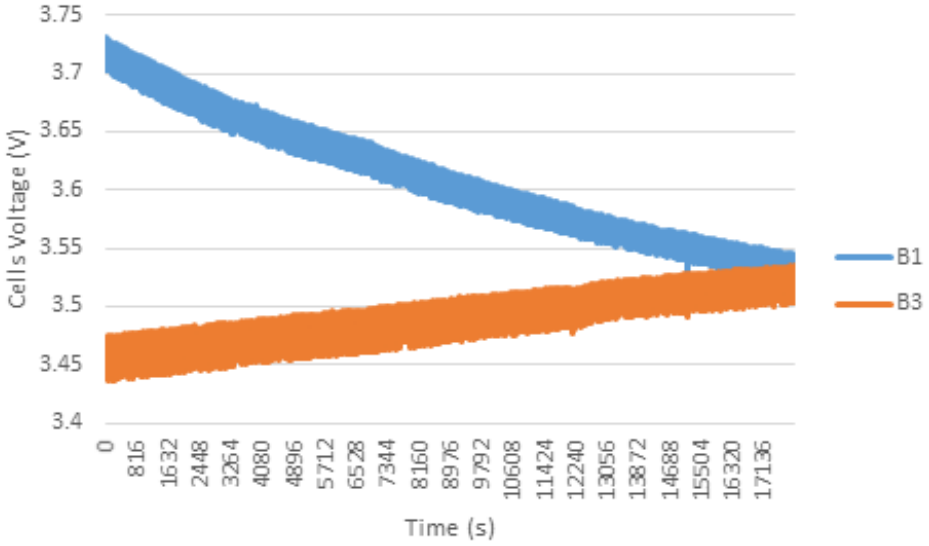


Figure 5- 19 – Cell voltages in equalisation between B1 and B3 in comparative test.

The circuit efficiency for this test can be calculated based on the initial and final voltage of B1 and B3.

$$\eta = \frac{16Ah \times 3600 \times (3.5 - 3.44)}{16Ah \times 3600 \times (3.71 - 3.5)} = 28.57\% \quad (5.10)$$

5.2.3 Equalisation B1-B2

This testing scenario is designed to demonstrate that voltage equalisation between an odd numbered cell and an even numbered cell can be achieved by the proposed converter, as the operational Mode 5. In this experiment, voltage equalisation is between the source cell B1 and the target cell B2. Cells in the pack are pre-charged to initial states where B1 is at 3.8V, B2 is at 3.25V, and all of the other cells are at 3.5V.

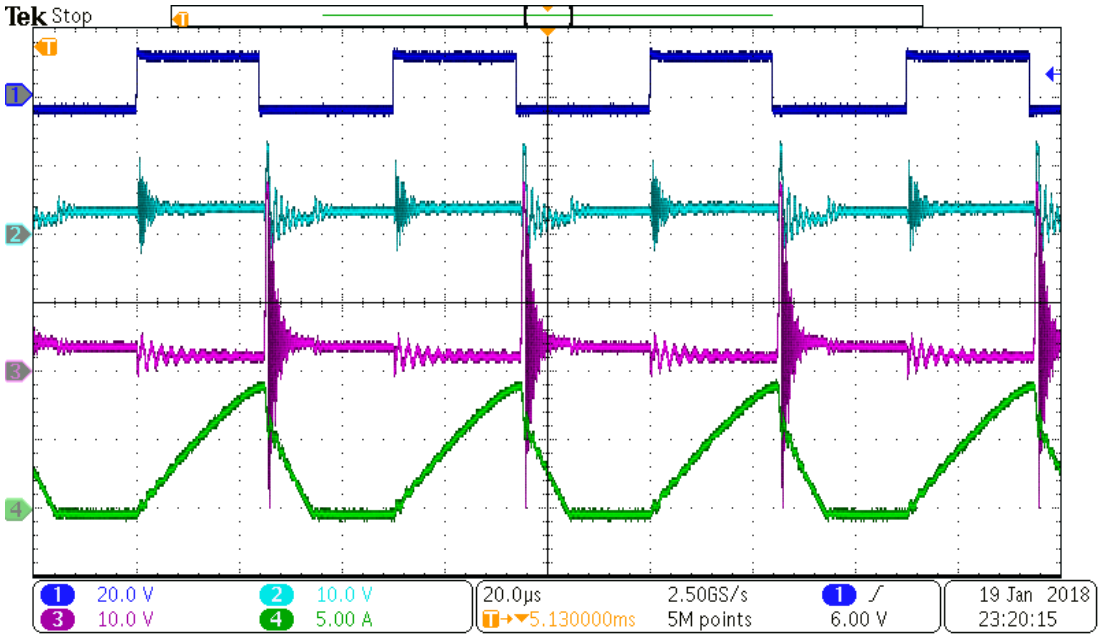
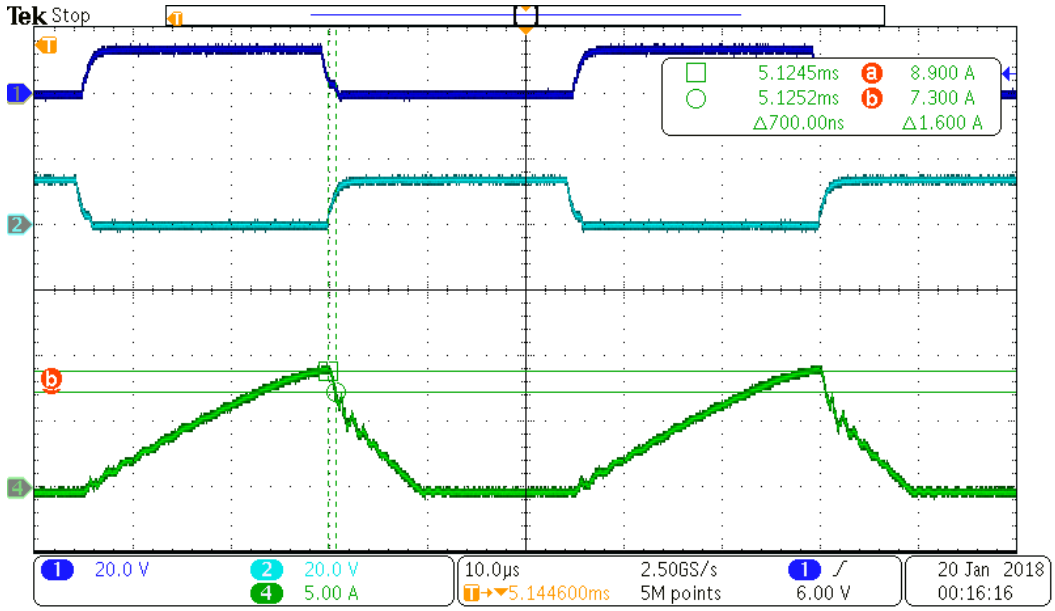


Figure 5- 20 – Waveforms of equalisation from B1 to B2 @ Lms_1=4.2uH, f=20kHz, dead-time=1us.

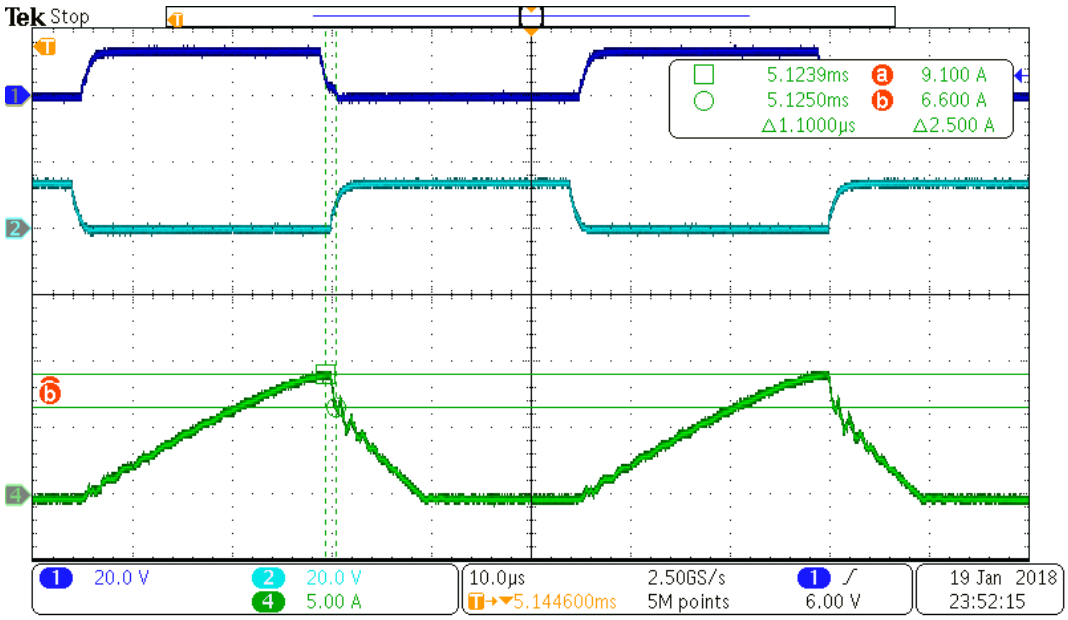
Waveforms of the voltages and currents during the equalisation process have been captured in Figure 5-20. Channels 1 to 4 stand for the gate signal of S_{C1} (20V/div), the voltage of B1 (V_{B1}, 10V/div), the voltage of B2 (V_{B2}, 10V/div), and the current through the winding N_{s_1} (i_{LS_1}, 5A/div). As mentioned in section 3.3.5, the circuit operates as a buck-boost converter-based equaliser where only one secondary coil is involved.

It can be observed that there is a drop in the current wave after MOSFET S_{c1} has been turned off. This is due to the dead-time between the turning off of S_{c1} and the turning on of S_{c3} to protect the cells B1 and B2 from short circuit. The waveforms in Figure 5-21 reveal the relationship between the length of the dead-time and the drop in current within this period. When the dead-time is 0.6us, the current drops from 8.9A to 7.3A with a 1.6A reduction. With the length of the dead-time extended, the current drop is

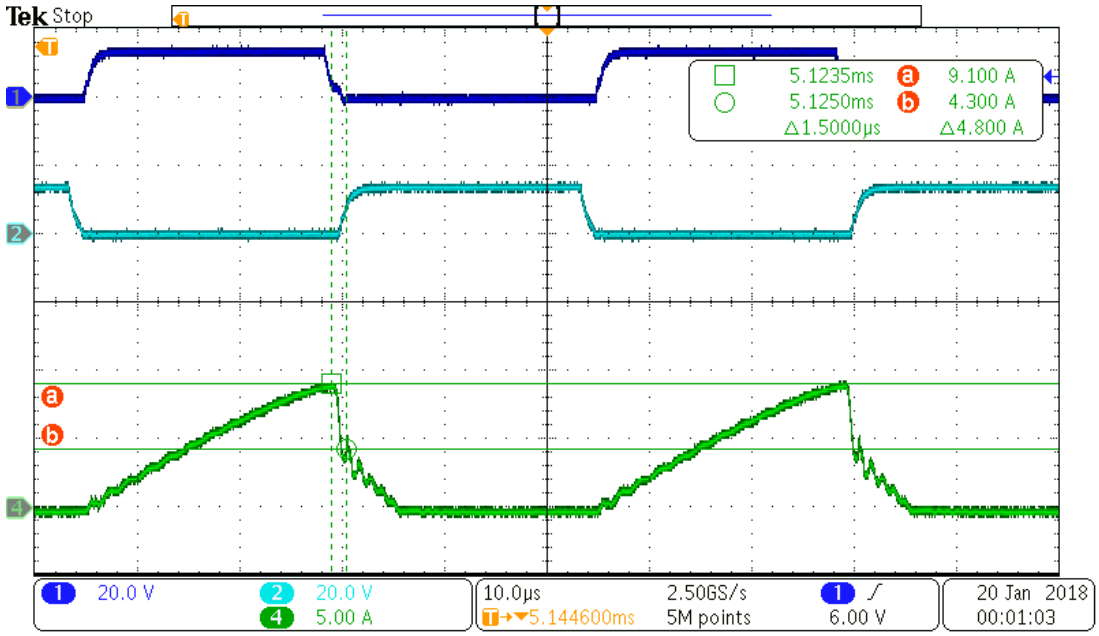
larger, at 2.5A for 1us of dead-time and 4.8A for 1.5us of dead-time. When the dead-time increases to 2us, the current when the target cell is connected to the coil is only 1A, which means that there is barely any energy left in the coil to charge B2. Therefore, the choice of dead-time length requires a compromise between safety and efficiency.



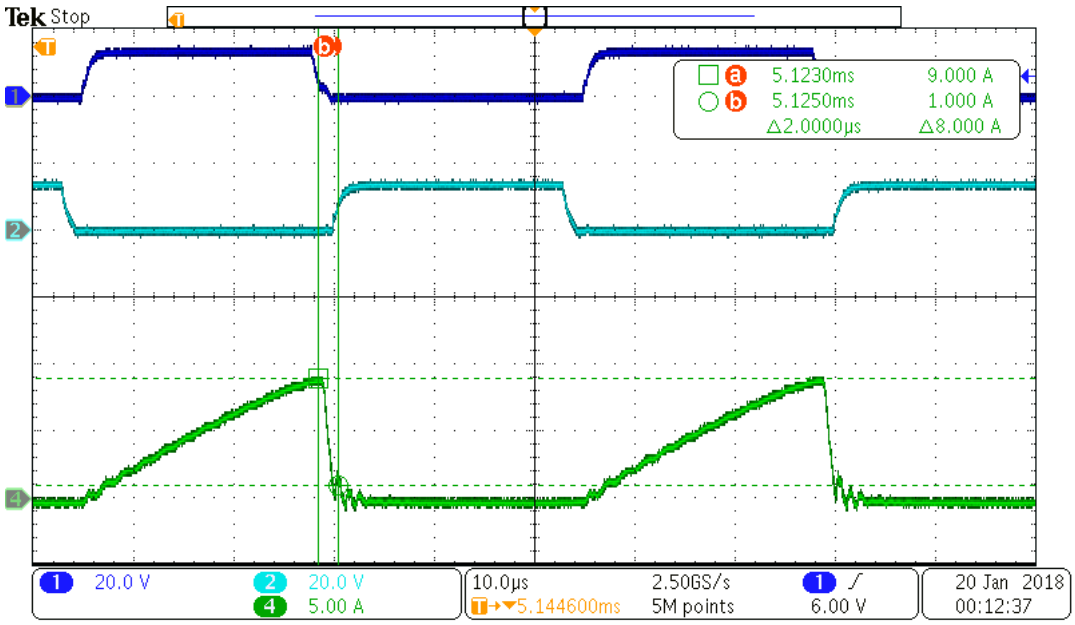
(a)



(b)



(c)



(d)

Figure 5- 21 – Current drop during the dead-time @: (a) dead-time=0.6us; (b) dead-time=1us; (c) dead-time=1.5us; (d) dead-time=2us.

In this experiment, since the turn-on and turn-off times of the selected MOSFET are around 400ns, the dead-time is set at 1us in order to guarantee safety. Figure 5-22 shows the waveforms of the cell voltages during the equalisation process. After more than five hours of operation, a balanced voltage between B1 and B2 has been achieved at about 3.4V for both cells.

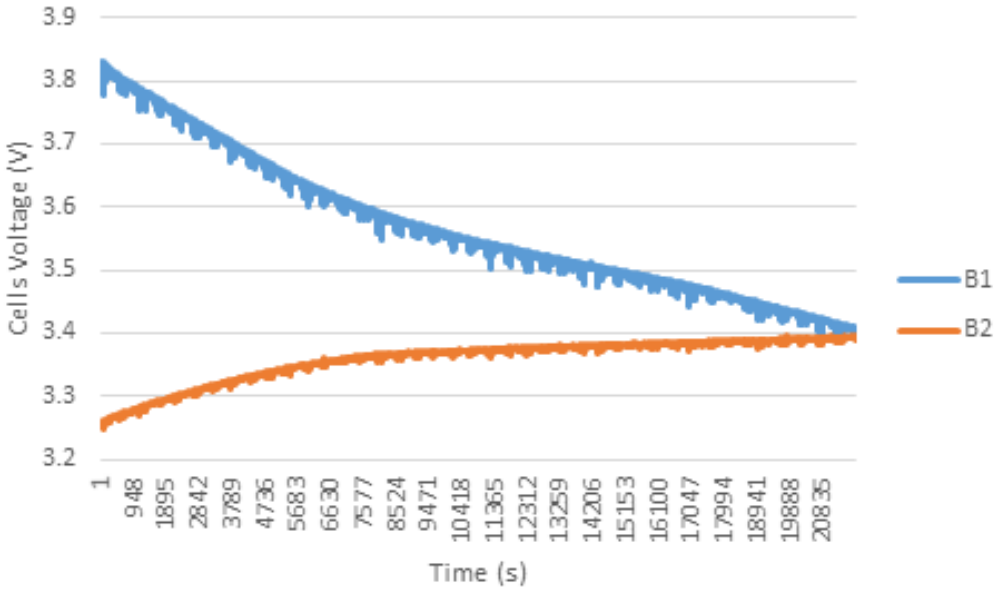


Figure 5- 22 – Cells voltage in equalisation from B1 to B2.

The practical results are consistent with the simulation results that with the voltage difference between two cells getting smaller, the charging speed of B2 became slower as well. The circuit efficiency for this test can be calculated based on the initial and final voltage of B1 and B3.

$$ɧ = \frac{16Ah \times 3600 \times (3.8 - 3.4)}{16Ah \times 3600 \times (3.4 - 3.25)} = 37.5\% \qquad (5.11)$$

For both of the voltage balancing tests, the circuit efficiency are lower than the simulated results. It is because in the simulation model, most components are ideal without or with low impedance. However, in the practical model, all impedance are taken into consideration. And since the voltage balancing process happens between single cells with terminal voltage of only 4V, voltage drop on these impedance has greater impact. To improve the efficiency, impedance in the system needs to be reduced as much as possible, such as reducing the length of connection cables.

5.3 Summary

With the system introduced in the first part of this chapter, the proposed multi-functional circuit has been tested in both charging and equalisation modes. During battery charging, to reduce the voltage stress across the transformer and switch and to eliminate the ripples in voltage waveforms, the system is connected to an AC power supply instead of the grid. In the first test that charge cells under open-loop control, since the duty cycle is fixed at 0.3 and there are energy losses in the circuit, the

transformer never suffers from saturation and the circuit operates with a high PF. The voltage charging is completed by two steps. In the first step, five cells are under charging for 2 hours and 40 minutes, and the voltage of each cell increases about 0.45V. The circuit efficiency during this stage is about 30.4%. In the second step, only one cell with the lowest voltage is continuously charged.

The circuit is then tested with the PFC and CC-CV controller applied. The main difference which occurs is in the waveforms of cell voltages since the charging speed slows down in the last period of charging.

The system also operates as a voltage equalisation circuit in two scenarios. One is equalisation between B1 and B3, corresponding to operation mode 3 described in section 3.3.3, the efficiency of this operational mode is 28.57%. The other scenario is to equalise the voltages in B1 and B2, corresponding to operational mode 5 described in section 3.3.5, with the circuit efficiency of 37.5%. Besides, parameters such as the duty cycle and the dead-time have been studied to illustrate their impact on circuit operation.

Chapter VI Conclusion and Future Work

With the rise of global warming problems due to excessive emissions of greenhouse gases, HEVs and EVs have increased in popularity as they use rechargeable batteries as an energy source instead of petrol. Lithium-ion batteries are prime candidates for EVs because of their high power density and higher cycle life compared to other battery types.

Generally, for applications such as HEVs and EVs, a battery pack may consist of hundreds of individual battery cells in order to meet voltage and energy capacity requirements. To maintain the safety of a battery pack with a large number of cells and to provide good performance, a voltage equalisation circuit is necessary. In order to charge a battery pack from the grid, an on-board charge system is installed in an EV. Thus, today, battery grid charging and voltage equalisation are two separate processes, resulting in two different systems assembled in an EV. To achieve both functions using fewer components, a multi-functional circuit that integrates a battery charger with an equalisation circuit has been proposed.

The proposed circuit can be used as both a grid charger and a voltage equaliser. When the vehicle is static and connected to the grid, the circuit operates as an on-board charger with functional blocks including AC/DC conversion, PFC and isolated DC/DC conversion. When the vehicle is not connected to the grid and unbalanced voltage is detected within the battery pack, the proposed circuit can also operate as a standalone equaliser. Moreover, the proposed circuit can achieve balanced voltage during charging processes. It can be controlled to charge cells with lower voltages only, and to further decrease the voltage gap between cells in the battery pack.

The transformer is the key component in the proposed circuit, which links the charging and voltage equalisation functions. The transformer on the one hand provides the required galvanic isolation and voltage regulation during grid charging mode and, on the other hand, provides short-term energy storage to distribute energy between the battery cells during voltage equalisation mode. Multi-tapped transformers are expensive and, for that reason, the proposed circuit topology has been designed in

such a way that a classical transformer arrangement with one primary winding and two secondary windings can be used.

A summary of the circuit operation modes is as follows:

Grid charging for an odd numbered cell, or a battery string starting with an odd numbered cell. The transformer operates as a flyback converter with the primary winding and the top secondary winding involved;

Grid charging for an even numbered cell, or a battery string starting with an even numbered cell. The transformer operates as a flyback converter with the primary winding and the bottom secondary winding involved;

Equalisation from an odd numbered cell to an odd numbered cell, or from source cells which start with an odd cell, to target cells which start with an odd cell. The transformer operates as a flyback converter with two secondary windings involved;

Equalization from an even numbered cell to an even numbered cell, or from source cells which start with an even cell, to target cells which start with an even cell. The transformer operates as a flyback converter with two secondary windings involved;
Equalization between an odd numbered cell and an even numbered cell, or between source cells which start with an odd cell, and target cells which start with an even cell. The transformer operates as a buck-boost converter with only one secondary winding involved.
Compared with separate charging and equalisation circuits, the proposed circuit uses only one transformer to achieve three functions of voltage regulation, energy transfer, and galvanic isolation. This reduces the number of components and the volume and weight of the system. Besides, the transformer utilised in the circuit has one primary winding and two secondary windings. The design and manufacturing of this transformer is easier and cheaper than the multi-winding transformers which used in transformer-based equalisation circuits.

For grid charging, a PFC controller is developed to allow the proposed circuit to operate within the limits set by the grid regulator. In addition, the proposed circuit charges each cell individually rather than charging a complete stack from the top of the battery string to the bottom. This way each battery is charged to its own healthy level, increasing reliability and safety. Due to the circuit layout, a PFC and CC-CV controller is also

developed so that CC-CV control can be achieved during charging as this is known to be the best charging method for lithium-ion batteries.

A simulation model has been built in PLECS. The proposed circuit is simulated as both a charger and an equaliser. When a battery pack with five cells is charged by the circuit, the results shows that the circuit could not only charge cells in the same rate, but also contributes to reduce the voltage difference among cells by charging low voltage cells only. The simulated circuit efficiency is 89.8%. The simulation of voltage balancing from an odd cell to another odd cell is done as well. The circuit efficiency is 38.25%. Also, an equalisation from an odd cell to an even cell showed that the circuit efficiency is 48.96%.

With the help of simulation the proposed circuit was designed, built and tested based on a five-cell battery pack. Results from experimental tests are in good agreement with simulation results. The system is tested to charge five cells with different initial voltage in two steps. The practical result shows that in the first step, five cells are under charging for 2 hours and 40 minutes, and the voltage of each cell increases about 0.45V. The circuit efficiency during this stage is about 30.4%. In the second step, only one cell with the lowest voltage until it reaches rated voltage.

The system also operates as a voltage equalisation circuit in two scenarios. One is the equalisation between B1 and B3, corresponding to the operational Mode 3. After about four hours, voltage of B1 and B3 is changed from 3.7V and 3.43V to both of 3.5V, with the circuit efficiency of 28.57%. The other scenario is to equalise the voltages between B1 and B2, corresponding to operational mode 5. The initial states for B1 and B2 are 3.8V and 3.25V. After about five hours of operation, a balanced voltage between B1 and B2 has been achieved at 3.4V for both cells. The circuit efficiency is 37.5%.

In this work, the circuit only realises the most basic functions of battery charging and voltage balancing. Future work should focus on the following aspects:

- The proposed circuit is designed to charge battery cells from the grid. In the experiment, an isolated transformer and a variac with a large inductance was used at the input stage for safety reasons. The large supply inductance causes high voltage spikes during the switching of input devices in particular in the proposed circuit. Therefore, the transformer and variac should be taken out for future testing.

- Due to the small number of battery cells used in the experiment, the input voltage was set to 100V which is lower than the grid voltage. An extension in the number of battery cells will reduce the turns-ratio of the transformer, as well as the current in the secondary side. This in principle would allow the input voltage to further increase.
- Experimental results show that the efficiency of the proposed circuit is low and has a great close relationship to the transformer design. Different transformer designs should be studied to manipulate the leakage inductances in all three windings to improve circuit efficiency.
- In the experimental test, the proposed circuit works well for specific scenarios such as with defined cell voltage levels. In the next step, more parameter variations should be tested which will also impact on the control strategy used in order to provide an optimum charging system.

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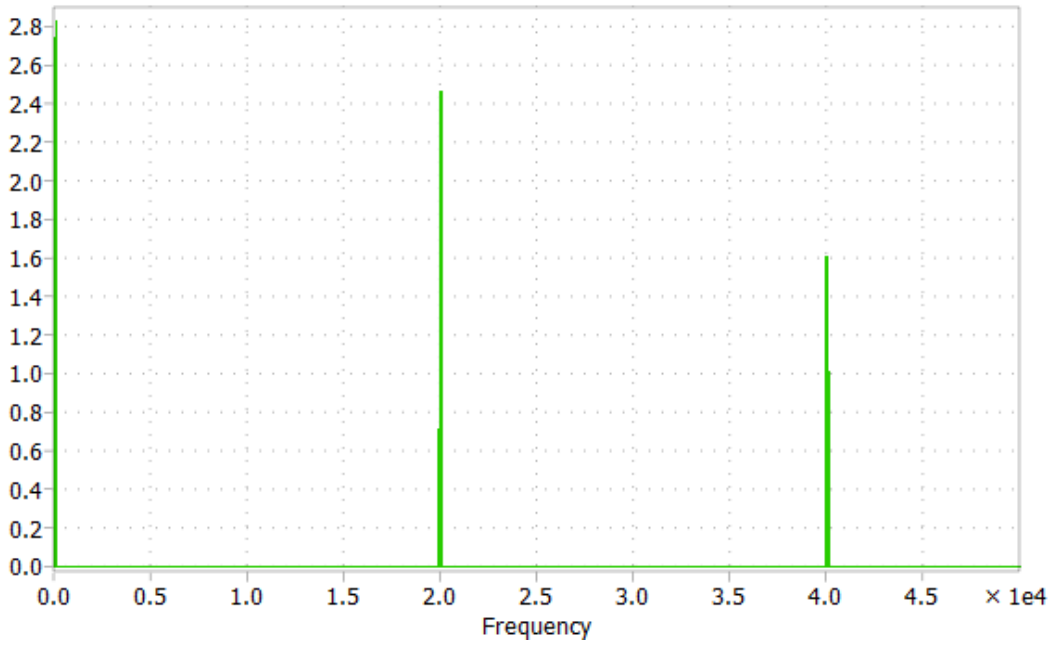
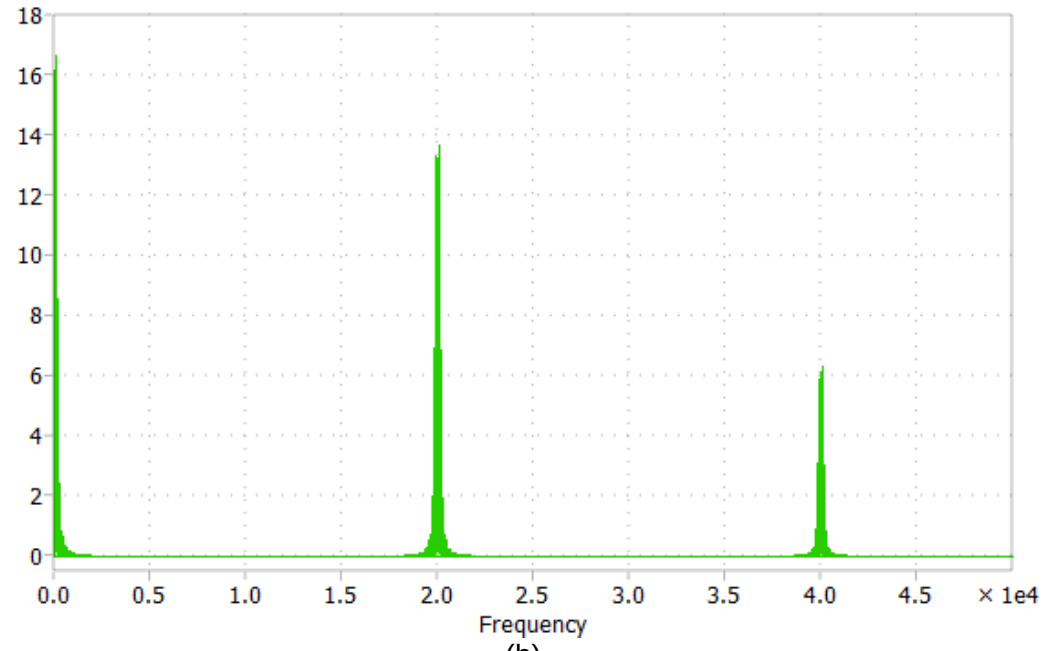
Appendix A

Harmonic contents of current waveforms shown in Chapter IV and V contain only low orders harmonics within 1kHz. Harmonic with extended frequency span up to 40kHz are shown in this appendix.

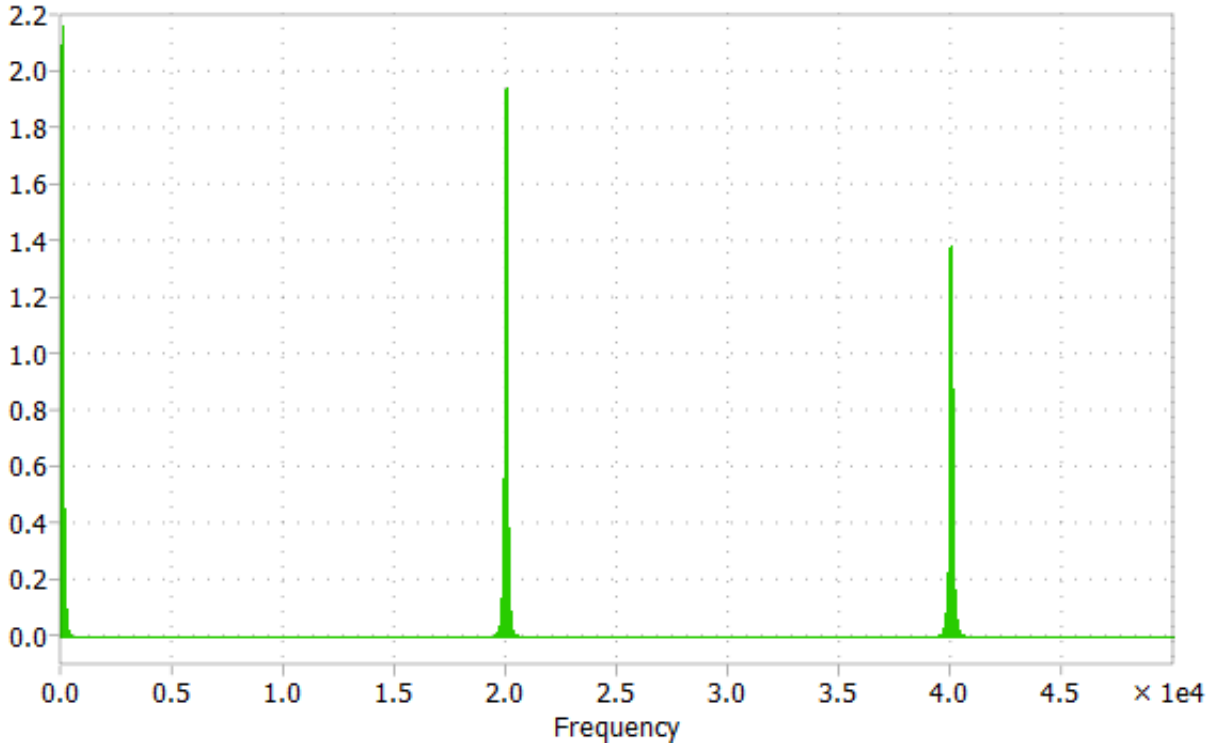


(a)

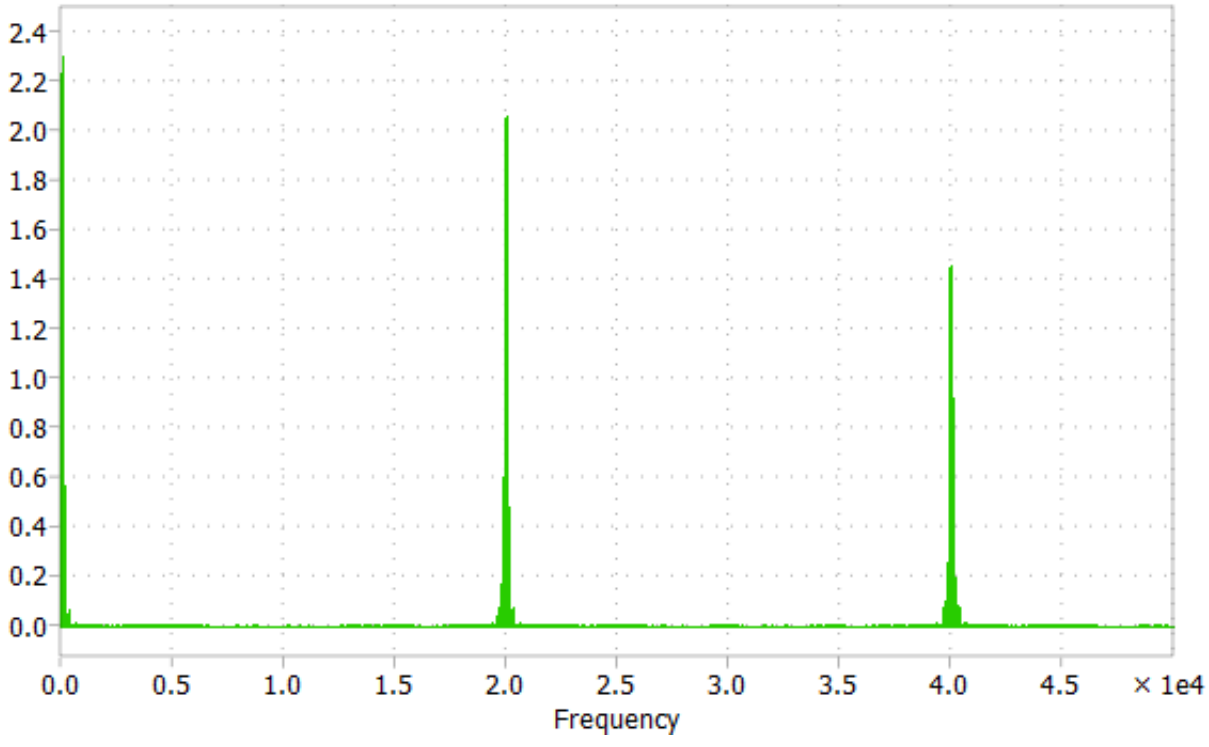


(b)

Figure A- 1 – Harmonic contents in extended frequency span of Figure 4-12.

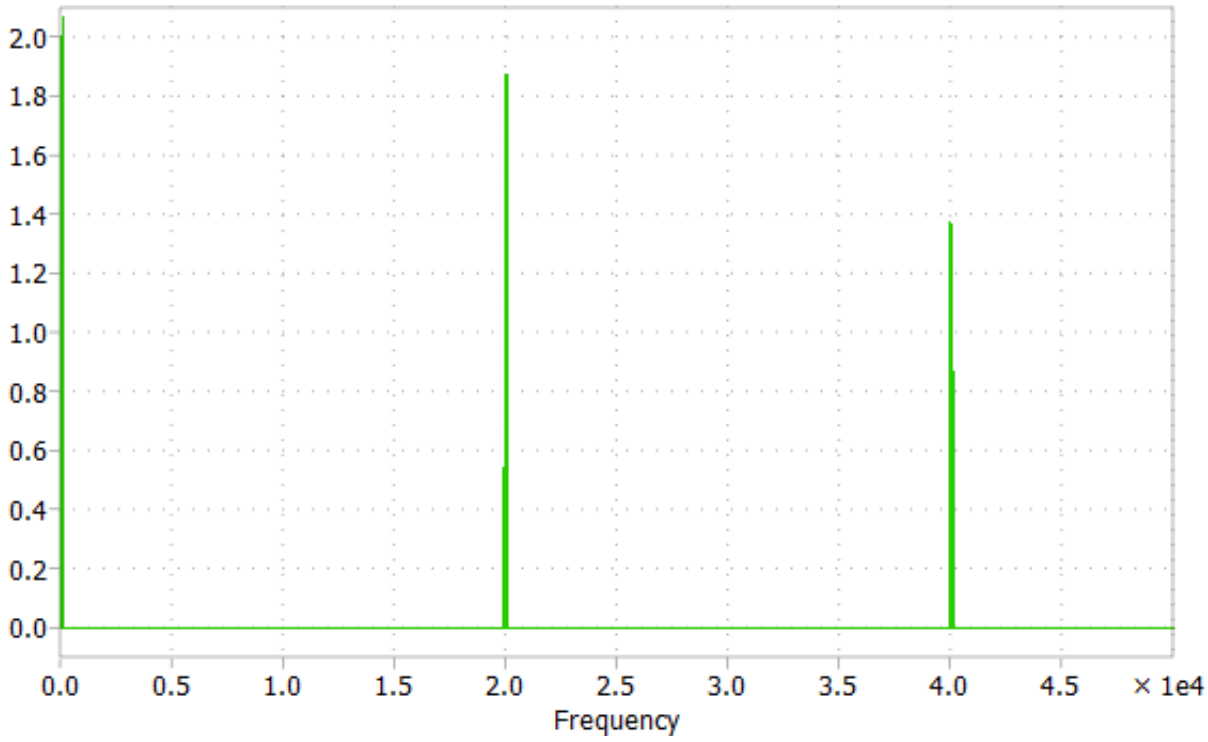


(a)

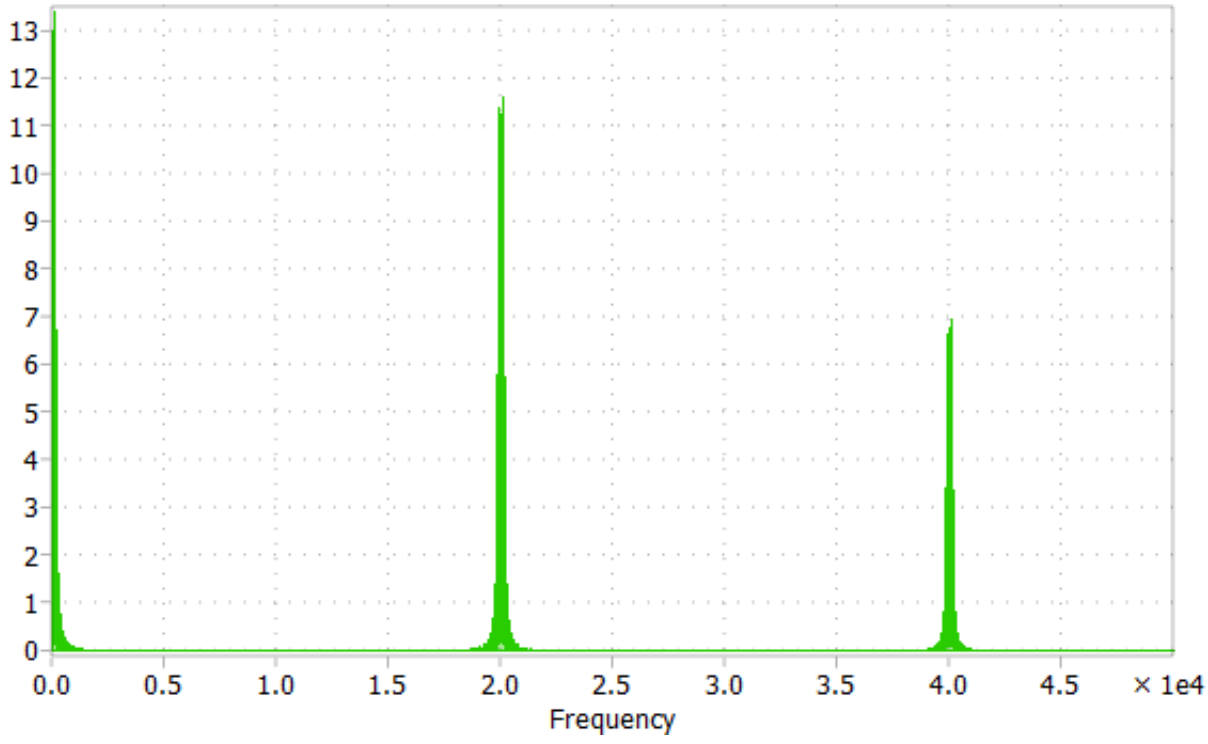


(b)

Figure A- 2 – Harmonic contents in extended frequency span of Figure 4-14.

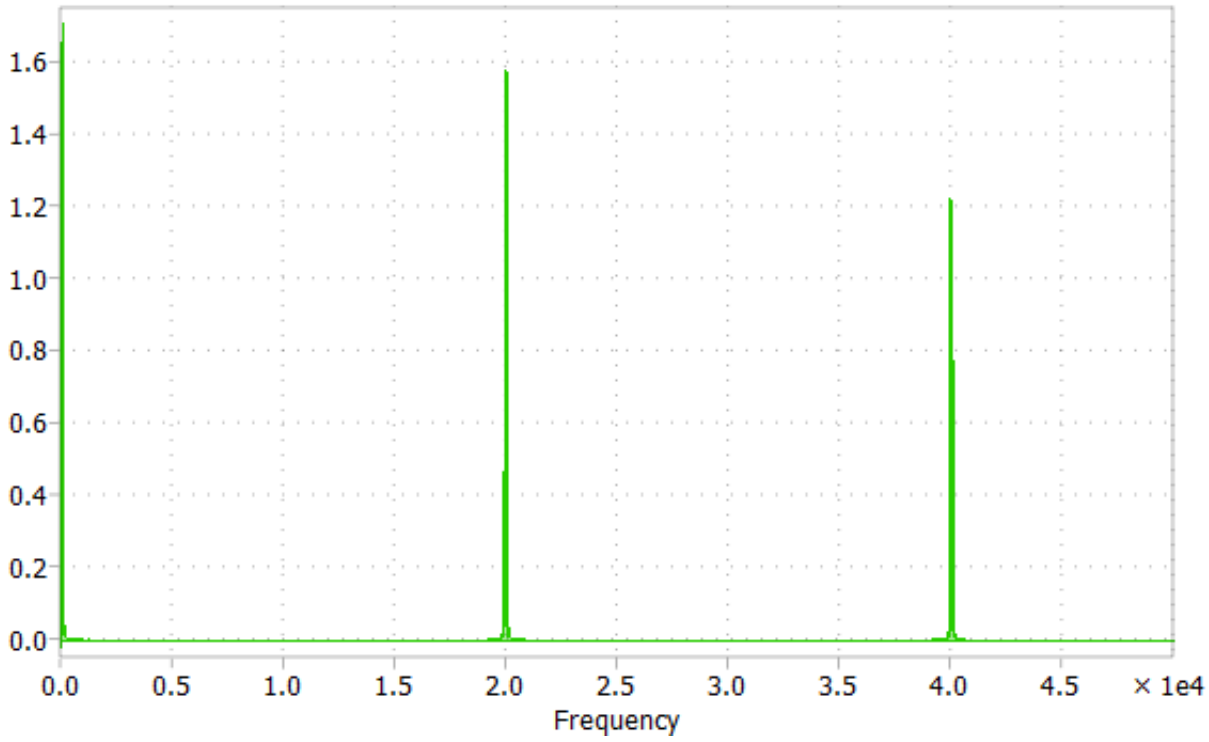


(a)

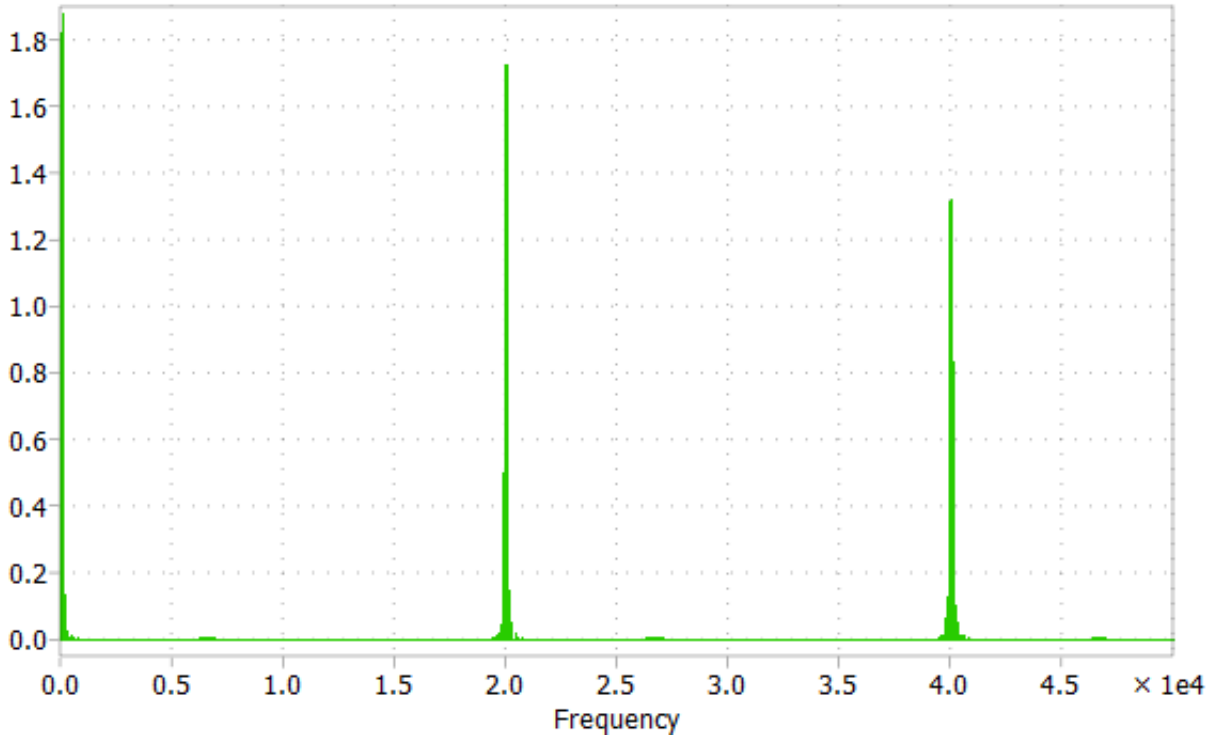


(b)

Figure A- 3 – Harmonic contents in extended frequency span of Figure 4-17.

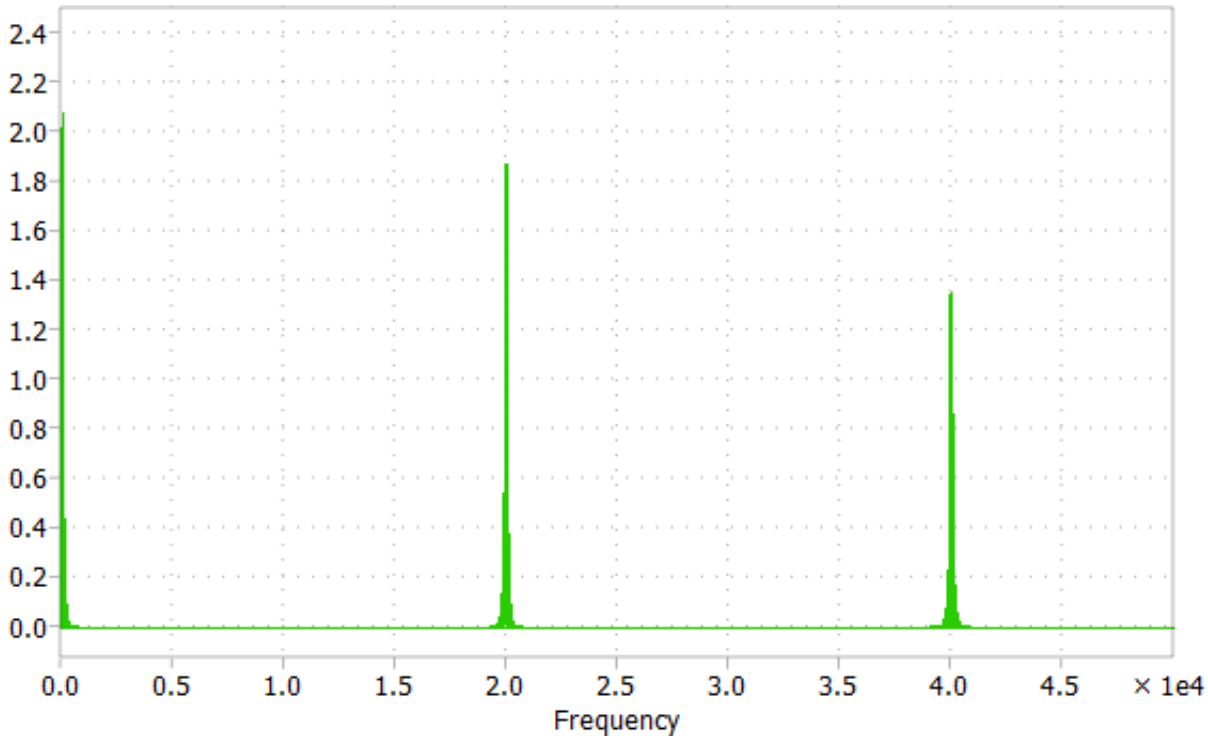


(a)

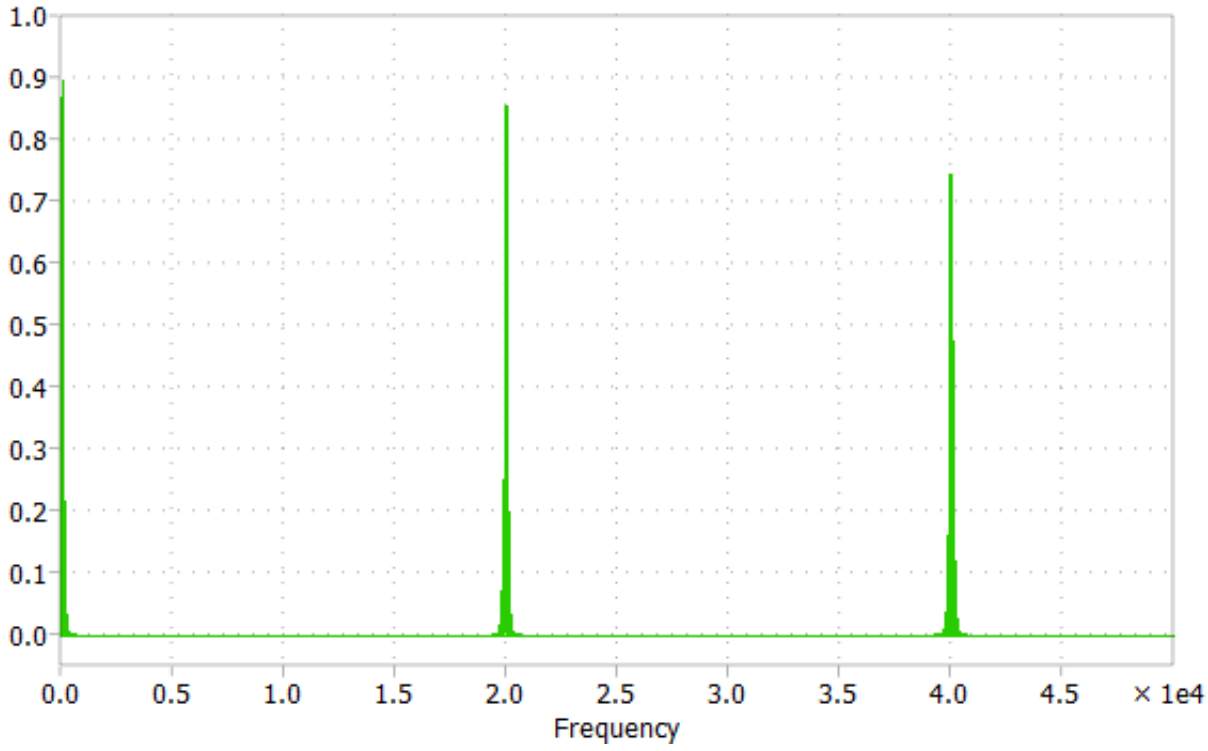


(b)

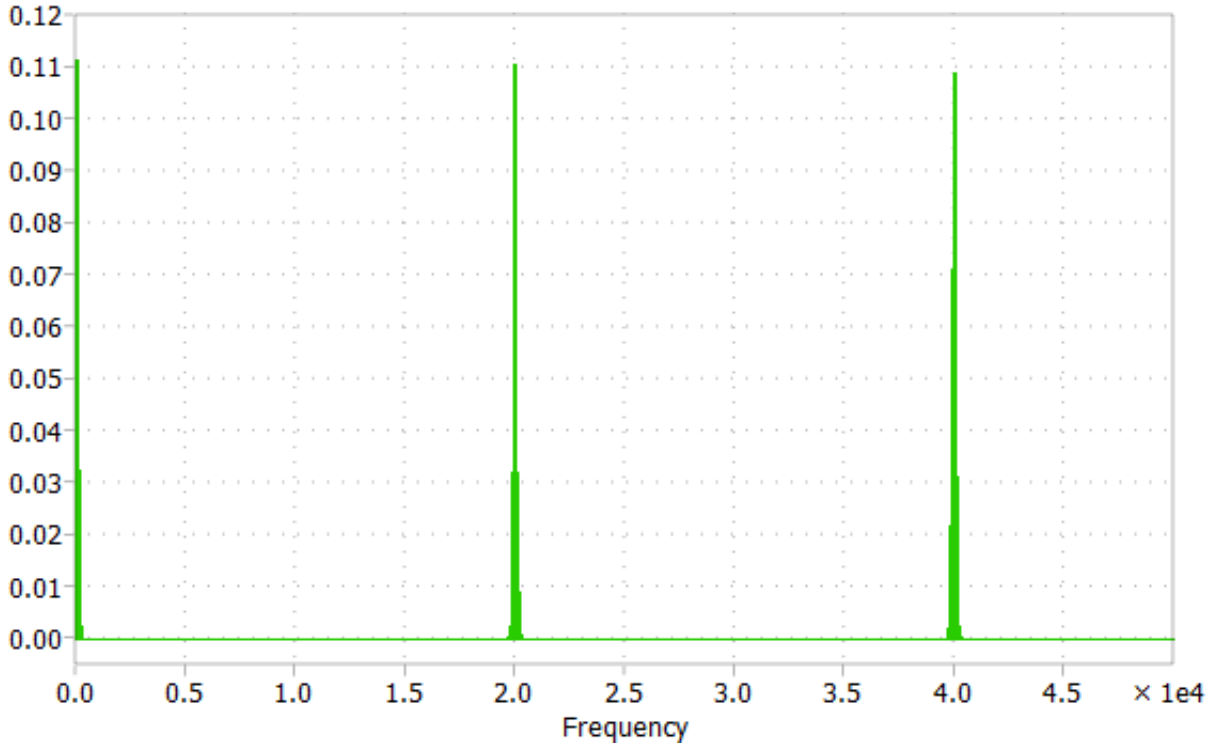
Figure A- 4 – Harmonic contents in extended frequency span of Figure 4-19.


2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
× 1e4
Frequency

(a)


1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
× 1e4
Frequency

(b)



(c)

Figure A- 5 – Harmonic contents in extended frequency span of Figure 4-22.

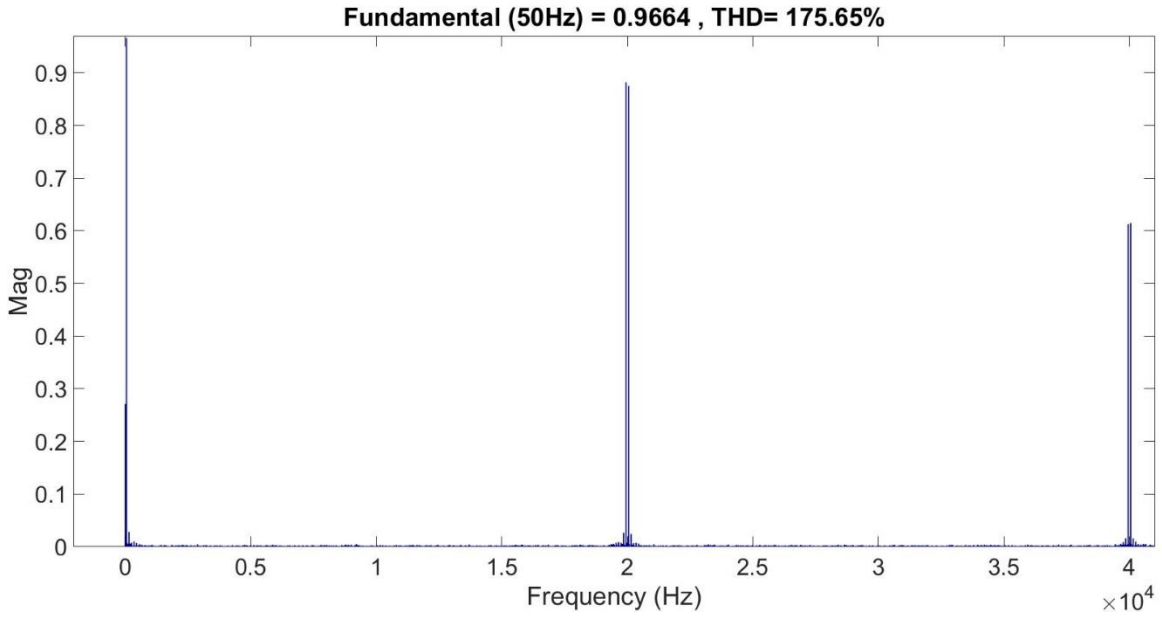


Figure A- 6 – Harmonic contents in extended frequency span of Figure 5-12.

Appendix B

```
// TITLE:  General Purpose Control Board Code
//
//    Features:
//    Configured for "boot to SARAM" operation.
//       20kHz PWM on 6 channels
//    Primary control code runs in epwm1_isr
//    Encoder interfaced via Eqep1
//    User interface using Labview GUI (RS232 via SCIA)
//    4-channel DAC (SPIA)
//    Eqep1 interrupt for encoder watchdog and direction reversal detection
//
//    Changed LSPCLK to 75MHz to increase SPI-A clk to 18.75MBaud to effect faster
transfers to DAC
//    This was done in DSP2833x_SysCtrl.c
//    SCIA (RS232) baud set to 585937.
//
#define CURRENT_LOOP_INT_CLAMP   3750   // Integrator clamp for antiwnd-up
#define SPEED_LOOP_INT_CLAMP     1000
#define POS_LOOP_INT_CLAMP       1000
#define PI 3.141592653589
#define TABLEN      720                                  // Set length of
sine/cosine look-up tables
#define      DATA_STORE_LEN            0x800        // Set length of data store
records to 2k

// Sensor calibration settings
// The gain from CAS15-NP primary current to ADC reading was measured at 100 per
ampere
// 1/100 = 0.01
#define SENSOR_GAIN0      0.0007                 // Sensor gain voltage cell 1
#define SENSOR_GAIN1      0.0007                 // Sensor gain voltage cell 2
#define SENSOR_GAIN2      0.0007                 // Sensor gain voltage cell 3
#define SENSOR_GAIN3      0.0007                 // Sensor gain voltage cell 4
#define SENSOR_GAIN4      0.0007               // Sensor gain voltage cell 5
#define SENSOR_GAIN6      0.0626              // Sensor gain (CAS15-NP)
#define SENSOR_GAIN11     0.076               // Sensor gain (LV-25)
#define SENSOR_GAIN7      0                   // Sensor gain (CAS50-NP)
#define SENSOR_GAIN8      0                   // Sensor gain (CAS50-NP)

#define SENSOR_OFFSET0    1.8943                 // Sensor offset voltage cell 1
#define SENSOR_OFFSET1    1.8874                 // Sensor offset voltage cell 2
#define SENSOR_OFFSET2    1.8857                 // Sensor offset voltage cell 3
#define SENSOR_OFFSET3    1.8983                 // Sensor offset voltage cell 4
#define SENSOR_OFFSET4    1.8918                 // Sensor offset voltage cell 5
#define SENSOR_OFFSET6    1995               // Sensor gain (CAS15-NP)
#define SENSOR_OFFSET11   2067               // Sensor gain (LV-25)
#define SENSOR_OFFSET7    0                // Sensor gain (CAS50-NP)
#define SENSOR_OFFSET8    0                // Sensor gain (CAS50-NP)

#include "DSP2833x_Device.h"           // DSP2833x Headerfile Include File
#include "DSP2833x_Examples.h"         // DSP2833x Examples Include File
#include "F28335_drive_function_prototypes.h"   // F28335 drive header file (DJA)

#include <stdlib.h>                          // needed for calloc()
```

```
#include <math.h>
#include <string.h>
#include <stdio.h>


// Function prototypes for functions defined in this file
// Code located in external RAM
void set_up_data_stores(void);
void set_up_look_up_tables(void);
void panel_controls(void);
// Code located in internal RAM
void update_panel(void);
void transfer_store_data_to_RS232(int frame_count);

// Interrupt service routines defined in this file
interrupt void epwm1_isr(void);        // This ISR contains application control
code
interrupt void eqep1_isr(void);        // This ISR is used for diagnostic only


// Global variables

float vc1=0,vc2=0,vc3=0,vc4=0,vc5=0;   //cells voltage
float ip=0,vp=0;                       //primary current, primary voltage
float is1=0, is2=0;                    //secondary current, Bus1 and Bus2

int    *s1,*s2,*s3,*s4,*s5,*s6,*s7,*s8;             // pointers for external RAM
int par1=0,par2=0,ctrlpanel=100,par5=0,dutycycle=2625;                  //
float Iref;                                    // reference current in CC control
float Vpeak;                                   //peak input voltage
float kp1=1,ki1=0;                             //gains for constant current
control loop
float kp2=1,ki2=0;                             //gains for pfc control loop
int par1b=0;                                                  // used in code
for DESAT single pulse test
Uint16 par4=0;                                                        // use

Uint16 store_enable=0;                                        // data store
enable flag
Uint16 store_counter=0;                                  // data store index
unsigned long ISR_count1=0;                                  // ISR counter
(increments every ISR execution)
unsigned long ISR_loopcountstart=0;             // ISR count value when labview
start to run
unsigned long LoopCount=0;                               // LabVIEW (RS232) data
transfer counter
unsigned long PulseISR=0;                                // pulse ISR to measure
cell voltage


// These following global variables are used to transfer data stored in ISR local
variables to other functions
int vde_m=0,vqe_m=0,ide_m=0,iqe_m=0;

int main(void)
    {
      Uint16 ReceivedChar=0;
      char sbuf[100];                                    // character buffer for
LabVIEW data link (RS232)
      char letter[100],temp=0;
```

```
      Uint16 i=0,nc=0;

      set_up_data_stores();                        // set up and initialise data
stores in ext RAM
      set_up_look_up_tables();               // set up sine and cosine look-up
tables

// Clear RS232 input string buffer
      //for (i=0; i < 100; ++i)
            //letter[i]=0;

// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();
   InitEPwm3Gpio();
   InitEPwm4Gpio();
   InitEPwm5Gpio();
   InitEPwm6Gpio();

// Initialise GPIO (gate drive reset, relays, DAC and test points)
   gpio_init();

   DINT;

   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.

   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.ADCINT = &epwm1_isr;    // ADC triggered ISR
   PieVectTable.EQEP1_INT = &eqep1_isr;// EQEP1 triggered ISR
   EDIS;    // This is needed to disable write to EALLOW protected registers

// Set up ADC (function below is located in DSP2833x_Adc.c)
// The following function sets ADCCLK to 37.5MHz if CPS = 1 (this is too high as
ADCCLK <= 25MHz)
// Need to adjust ADCTRL3 to set to 25MHz
   InitAdc();

// Initialise ADC sequencer
   adc_seq_init();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;     // ePWM TBCLK stopped
   EDIS;

// Initialise PWM modules
   InitEPwmMods();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;     // All enabled ePWMs synchronised
with rising edge of TBCLK
   EDIS;
```

```
// Set up Timer0 for code execution time measurement within epwm1_isr
   Timer0_init();

// Enable CPU interrupts
   IER |= M_INT1;   // Enable CPU INT1 which is connected to PIE group 1 (main
control ISR)
   IER |= M_INT5;   // Enable CPU INT5 which is connected to PIE group 5 (shaft
direction change ISR)


   PieCtrlRegs.PIEIER1.bit.INTx6 = 1;         // Enable ADCINT in the PIE: Group 1
interrupt 6 (i.e. INT1.6)
   PieCtrlRegs.PIEIER5.bit.INTx1 = 1;         // Enable EQEP1_INT in the PIE:
Group 5 interrupt 1 (i.e. INT5.1)

// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global real-time interrupt DBGM

    scia_fifo_init();        // Initialise the SCI FIFO
    scia_echoback_init();  // Initialise SCI for echoback

    LoopCount = 0;               // Set LabVIEW data transfer counter to zero
    ErrorCount = 0;
      i=0;                              // Set RS232 character counter to zero


// IDLE loop. Just sit and loop forever:
// This loop is concerned only with communications with LabVIEW
      for(;;)
   {
            i=0;   //reset input character counter
            do {
                  // Wait for incoming character from RS232 port
                  while(SciaRegs.SCIFFRX.bit.RXFFST !=1) { }    // wait for XRDY
=1 for empty state
                  ReceivedChar = SciaRegs.SCIRXBUF.all;         // Get character
                  temp = ReceivedChar & 0xFF;                                  //
strip off the error bits
                  letter[i]=temp;
                  i++;
                  ISR_loopcountstart=ISR_count1;
            }while(temp != '\n');

            // Get incoming parameters from LabVIEW GUI
            nc =
sscanf(letter,"%d %d %d %d %d %d %f %f %f %f %f %f",&par1,&par2,&ctrlpanel,&par4,&
par5,&dutycycle,&Iref,&Vpeak,&kp1,&ki1,&kp2,&ki2);

            // Test for sensor out-of-range trip (send status to LabVIEW)
            TZflag=EPwm1Regs.TZFLG.bit.OST;


            // Send data to LabVIEW (UCP mode)
            if(par1==200)
                  update_panel();
            // Send data to LabVIEW (DTI mode)
            if(par1==100)
                  transfer_store_data_to_RS232(par2);
```

```
            get_control_panel_button_status();      // Update LabVIEW panel push
button status flags

            panel_controls();   // Implement the pushbutton commands

            LoopCount++;        // Count LabVIEW data transfer cycles

   }
      return 0;
} // end main()


interrupt void epwm1_isr(void)
{

      float kv1,kv2;                        // primary voltage gains, kv1 is to
modify voltage value to Iref, kv2 is to modify voltage to unit value
    float i_value_error;                     // current error in cc control
    float i_phase_error;                     // current error in pfc control
    float icc_demand;
    float ipfc_demand;

    Uint16 cmp1a=3750,cmp1b=0;
    Uint16 cmp2a=3750,cmp2b=0;
    Uint16 cmp3a=3750,cmp3b=0;
    Uint16 cmp4a=3750,cmp4b=0;
    Uint16 cmp5a=3750,cmp5b=0;
    Uint16 cmp6a=3750,cmp6b=0;                  //PWM duty-cycle modulation index
    //Uint16 Duty_cycle_Clamp;                // clamp duty cycle in 40%

      CpuTimer0Regs.TCR.bit.TRB = 1;            // reload timer0 to initiate code
timing

      GpioDataRegs.GPACLEAR.bit.GPIO12 = 1;    // Pulse LDAC/ low on DAC to latch
data into DAC
      GpioDataRegs.GPASET.bit.GPIO12 = 1;

      ISR_count1++;                                       // count ISR events
since start
      //temp_count++;                                          // relative count
(can be useful for timing things)

      PulseISR=(ISR_count1-ISR_loopcountstart)%4000;    // for f=20KHz
      //PulseISR=(ISR_count1-ISR_loopcountstart)%2000;      // for f=10KHz
      //PulseISR=(ISR_count1-ISR_loopcountstart)%1000;      // for f=5KHz

      flag2 = 1;                                             // set flag, can
be useful

#if 1  // Count and display CBC trip events
      if(EPwm1Regs.TZFLG.bit.CBC)
      {
            trip_count++;
            EALLOW;
            EPwm1Regs.TZCLR.bit.CBC = 1;
            EDIS;
      }
#endif
```

```
#if 1
       // Acquire sensor input data and apply gain and offset adjustments
       // The first 6 sensor inputs have out-of-range trip circuits

       ip = (float)SENSOR_GAIN6*2*((int)(AdcRegs.ADCRESULT6 >>4)-SENSOR_OFFSET6);
              //     ADCINA6, primary current
       vp = (float)SENSOR_GAIN11*((int)(AdcRegs.ADCRESULT11 >>4)-SENSOR_OFFSET11);
              //     ADCINB0, primary voltage
       is1 = (float)SENSOR_GAIN7*((int)(AdcRegs.ADCRESULT7 >>4)-SENSOR_OFFSET7);
              //     ADCINB6, secondary current BusA_1
       is2 = (float)SENSOR_GAIN8*((int)(AdcRegs.ADCRESULT8 >>4)-SENSOR_OFFSET8);
              //     ADCINA7, secondary current BusA_2
       vc1 = (float)SENSOR_GAIN0*(int)(AdcRegs.ADCRESULT0 >>4)+SENSOR_OFFSET0;
//     ADCINA3, cell 1 voltage
       vc2 = (float)SENSOR_GAIN1*(int)(AdcRegs.ADCRESULT1 >>4)+SENSOR_OFFSET1;
//     ADCINB3, cell 2 voltage
       vc3 = (float)SENSOR_GAIN2*(int)(AdcRegs.ADCRESULT2 >>4)+SENSOR_OFFSET2;
//     ADCINA4, cell 3 voltage
       vc4 = (float)SENSOR_GAIN3*(int)(AdcRegs.ADCRESULT3 >>4)+SENSOR_OFFSET3;
//     ADCINB4, cell 4 voltage
       vc5 = (float)SENSOR_GAIN4*(int)(AdcRegs.ADCRESULT4 >>4)+SENSOR_OFFSET4;
//     ADCINA5, cell 5 voltage
#endif

#if    1
       // Acquire raw sensor data
       B0 = AdcRegs.ADCRESULT6 >>4;           //     ADCINA6, primary current xxxx
       B1 = AdcRegs.ADCRESULT11 >>4;          //     ADCINB0, primary voltage xxxx
       B2 = AdcRegs.ADCRESULT7 >>4;           //     ADCINB6, secondary current
BusA_1 xxxx
       B3 = AdcRegs.ADCRESULT8 >>4;           //     ADCINA7, secondary current
BusA_2 xxxx
    B4 = AdcRegs.ADCRESULT0 >>4;       //     ADCINA3, cell voltage xxxx
       B5 = AdcRegs.ADCRESULT1 >>4;           //  ADCINB3
       B6 = AdcRegs.ADCRESULT2 >>4;           //  ADCINA4
       B7 = AdcRegs.ADCRESULT3 >>4;           //  ADCINB4
       B8 = AdcRegs.ADCRESULT4 >>4;           //  ADCINA5
#endif

if ((PulseISR >= 50) && (PulseISR <= 3950))               //   for f=20KHz
//if ((PulseISR >= 50) && (PulseISR <= 1950))           //   for f=10KHz
//if ((PulseISR >= 50) && (PulseISR <= 950))            //   for f=5KHz
{
#if 0             // charging cell 1. Set PWM1_A and PWM1_B with same set&clear,
in drive_function file.
       //update dead-band register for epwm 1 2 3 4 5 6
              EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
              EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
              EPwm1Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

              EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
              EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
              EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;


              EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
              EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
              EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
```

```
            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
                   // charge cell 1, with open loop control
            cmp1a=dutycycle;                cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=3749;
            cmp5a=3749;
            cmp5b=0;
            cmp6a=3749;
            cmp6b=0;
#endif

#if 1             // charging cell 1-3. Set PWM1_A and PWM1_B with same set&clear,
in drive_function file.
       //update dead-band register for epwm 1 2 3 4 5 6
       // open loop control
            EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm1Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
 // charge cell 1-3, with open loop control
            cmp1a=dutycycle;          // main MOSFET 0.2 fixed duty cycle
            cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;          // FET3 close
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=0;          // FET8,9 close
            cmp5a=3749;       // FET6,7 and FET10,11 turn on/off alternatively
```

```
            cmp5b=3749;
            cmp6a=3749;
            cmp6b=0;
#endif

#if 0
            EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm1Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
      if(ctrlpanel==100)
                // charge cell 1-3, with open loop control, active 4a and 4b, but
connect cell 1-3
      {
            cmp1a=dutycycle;          // main MOSFET 0.4 fixed duty cycle
            cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;          // FET3 close
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=3749;          // FET8,9 close
            cmp5a=3749;       // FET6,7 and FET10,11 turn on/off alternatively
            cmp5b=0;
            cmp6a=3749;
            cmp6b=0;
      }

      if(ctrlpanel==200)
      {
            //kv1=0.02;
            kv1=Iref/Vpeak;

            //kv2=0.02;
            //Vpeak=50;
            kv2=1/Vpeak;

            //kp1=1;
            //ki1=0;
            //kp2=1;
            //ki2=0;

           // charge cell 1-3, with cc+pfc control
            i_value_error=vp*kv1-ip*2;
```

```
            // PI control for constant current
            icc_demand=kp1*i_value_error+zd1;
            if(release)
                  zd1=zd1+ki1*i_value_error;

            i_phase_error=icc_demand*vp*kv2;
            // PI control for PFC
            ipfc_demand=kp2*i_phase_error+zd2;
            if(release)
                  zd2=zd2+ki2*i_phase_error;

            //clamp icc_demand in 0-1
            if(ipfc_demand>0.99)
                  ipfc_demand=0.99;
            if(ipfc_demand<0)
                  ipfc_demand=0;

            dutycycle=ipfc_demand*3750;

            //clamp dutycycle up to 0.4
            if(dutycycle>3749)
                  dutycycle=3749;
            if(dutycycle<2250)
                  dutycycle=2250;

            //active 4a and 4b, but connect cell 1-3
            cmp1a=dutycycle;
            cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=3749;
            cmp5a=3749;
            cmp5b=0;
            cmp6a=3749;
            cmp6b=0;
      }
#endif

#if 0             // charging cell 1-3. Set PWM1_A and PWM1_B with same set&clear,
in drive_function file.
      //update dead-band register for epwm 1 2 3 4 5 6
      // close loop control  PFC
            EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;      // Active high
complementary
            EPwm1Regs.DBCTL.bit.OUT_MODE = DB_DISABLE; // disable deadband

            EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
```

```
            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
      EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;
      if(ctrlpanel==100)
                // charge cell 1-3, with open loop control, active 4a and 4b, but
connect cell 1-3
      {
            cmp1a=dutycycle;          // main MOSFET 0.4 fixed duty cycle
            cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;          // FET3 close
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=3749;          // FET8,9 close
            cmp5a=3749;       // FET6,7 and FET10,11 turn on/off alternatively
            cmp5b=0;
            cmp6a=3749;
            cmp6b=0;
      }

      if(ctrlpanel==200)
      {
            kv2=(vc1+vc2+vc3+vc4+vc5)*0.2;
            v_value_error=4-kv2;

            icc_demand=kp1*v_value_error+zd1;
                        if(release)
                              zd1=zd1+ki1*i_value_error;

            i_value_error=kv1*vp-icc_demand;

                        // PI control for PFC
                        ipfc_demand=kp2*i_value_error+zd2;
                        if(release)
                              zd2=zd2+ki2*i_value_error;

                        dutycycle=ipfc_demand*3750;

            //clamp dutycycle up to 0.4
            if(dutycycle>3749)
                  dutycycle=3749;
            if(dutycycle<2625)
                  dutycycle=2625;

            //active 4a and 4b, but connect cell 1-3
            cmp1a=dutycycle;
            cmp1b=dutycycle;
            cmp2a=0;
            cmp2b=0;
            cmp3a=3749;
            cmp3b=0;
            cmp4a=0;
            cmp4b=3749;
            cmp5a=3749;
            cmp5b=0;
```

```
            cmp6a=3749;
            cmp6b=0;
      }
#endif

#if 0    //code for equalization: cell 1 to cell 2


      EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
      EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
      EPwm1Regs.DBCTL.bit.OUT_MODE = DBB_ENABLE;

      EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
      EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
      EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;


      EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
      EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
      EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;


      EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
      EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
      EPwm4Regs.DBCTL.bit.OUT_MODE = DBB_ENABLE;

      EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
      EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
      EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

      EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
      EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
      EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

            cmp1a=dutycycle;
                cmp1b=dutycycle;
              cmp2a=3749;
                cmp2b=3749;
                cmp3a=3749;
                cmp3b=0;
              cmp4a=dutycycle;
                cmp4b=3749;
              cmp5a=3749;
                cmp5b=dutycycle;
                cmp6a=3749;
                cmp6b=0;
#endif

#if 0
            EPwm1Regs.DBCTL.bit.IN_MODE = DBB_ALL;
            EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

          EPwm2Regs.DBCTL.bit.IN_MODE = DBA_RED_DBB_FED;
          EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm2Regs.DBCTL.bit.OUT_MODE = DBA_ENABLE;

            EPwm3Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;
```

```
            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_RED_DBB_FED;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

            EPwm6Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;

                cmp1a=dutycycle;
                  cmp1b=dutycycle;
                  cmp2a=3749;
                  cmp2b=dutycycle;
                  cmp3a=3749;
                  cmp3b=dutycycle;
                  cmp4a=dutycycle;
                  cmp4b=dutycycle;
                  cmp5a=dutycycle;
                  cmp5b=dutycycle;
                  cmp6a=3749;
                  cmp6b=0;
#endif

  #if 0      //code for equalization: cell 1,2,3 to cell 2,3,4


          EPwm2Regs.DBCTL.bit.IN_MODE = DBA_ALL;
          EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm2Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;


            EPwm3Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm3Regs.DBCTL.bit.OUT_MODE = DB_DISABLE;


            EPwm4Regs.DBCTL.bit.IN_MODE = DBA_ALL;
            EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_LOC;
            EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

            EPwm5Regs.DBCTL.bit.IN_MODE = DBB_RED_DBA_FED;
            EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_LOC;
            EPwm5Regs.DBCTL.bit.OUT_MODE = DBA_ENABLE;
            EPwm6Regs.DBCTL.bit.IN_MODE = DBA_RED_DBB_FED;
            EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HI;
            EPwm6Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;

                cmp1a=0;
                  cmp1b=0;
                  cmp2a=3749;
                  cmp2b=3749;
                  cmp3a=3749;
                  cmp3b=0;
                  cmp4a=1875;
                  cmp4b=0;
                  cmp5a=3749;
```

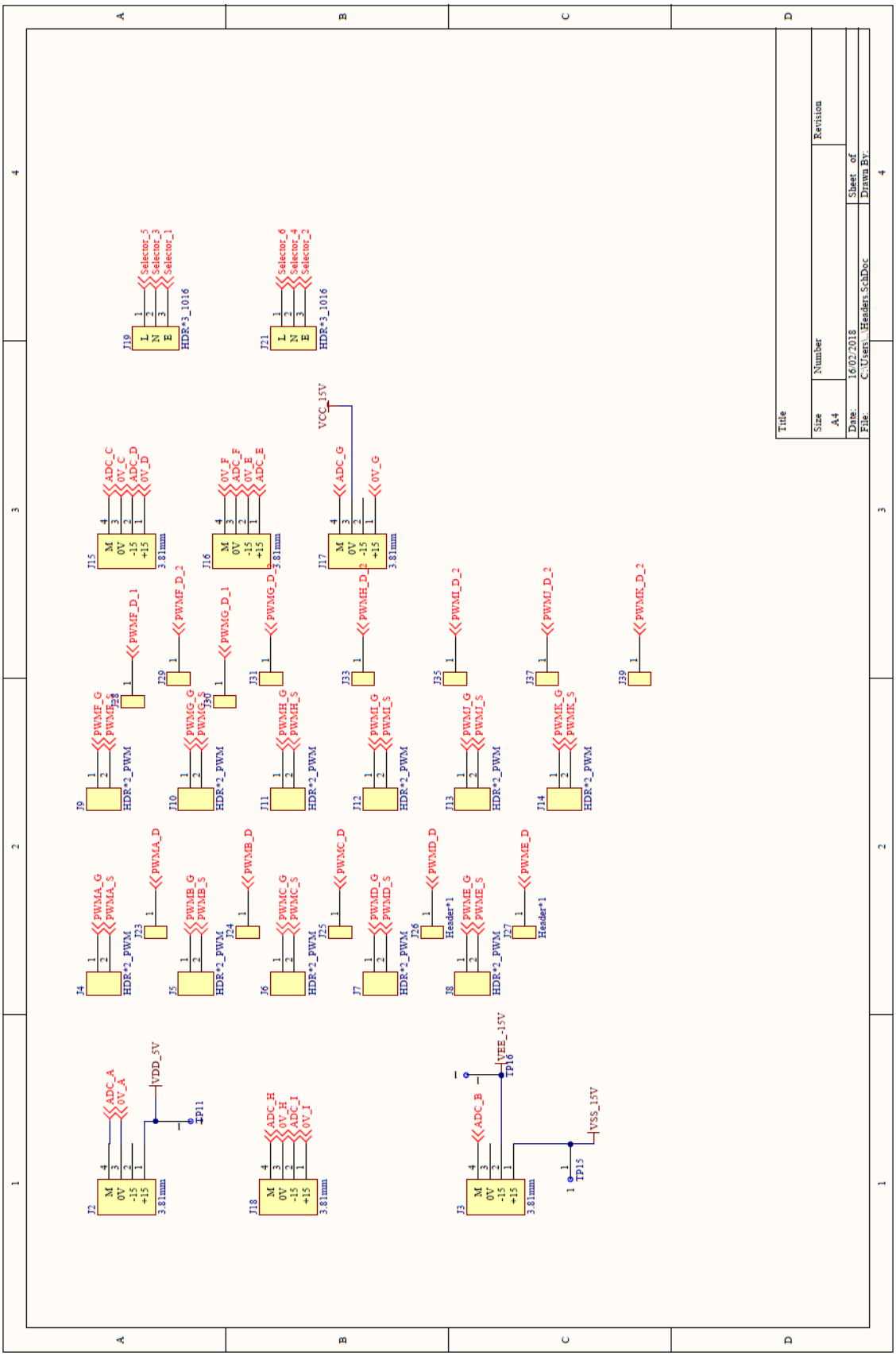
```
                    cmp5b=1875;
                    cmp6a=3749;
                    cmp6b=1875;
#endif
}
else {
#if 1         //charging open loop control
                cmp1a=3749;
                    cmp1b=3749;
                    cmp2a=3749;
                    cmp2b=0;
                    cmp3a=3749;
                    cmp3b=0;
                    cmp4a=3749;
                    cmp4b=0;
                    cmp5a=3749;
                    cmp5b=0;
                    cmp6a=3749;
                    cmp6b=0;
#endif

#if 0                   // equalization 1 to 2
       cmp1a=3749;
       cmp1b=0;
       cmp2a=3749;
       cmp2b=0;
       cmp3a=3749;
       cmp3b=0;
       cmp4a=3749;
       cmp4b=0;
       cmp5a=3749;
       cmp5b=0;
       cmp6a=3749;
       cmp6b=0;
#endif

#if 0                  //equalization 1 to 3
       cmp1a=3749;
       cmp1b=0;
       cmp2a=3749;
       cmp2b=3749;
       cmp3a=3749;
       cmp3b=0;
       cmp4a=3749;
       cmp4b=3749;
       cmp5a=0;
       cmp5b=0;
       cmp6a=3749;
       cmp6b=0;
#endif
}


#if 1   // Update PWM modulation registers (group 1)
       EPwm1Regs.CMPA.half.CMPA = cmp1a;             //ADC trigger
       EPwm1Regs.CMPB = cmp1b;                  //Mosfet in primary side
       EPwm2Regs.CMPA.half.CMPA = cmp2a;             //Mosfet in secondary BusA_1_1
       EPwm2Regs.CMPB = cmp2b;                  //Mosfet in secondary BusA_1_2
       EPwm3Regs.CMPA.half.CMPA = cmp3a;        //Mosfet in secondary BusA_2_1
       EPwm3Regs.CMPB = cmp3b;                  //Mosfet in secondary BusA_2_2
```

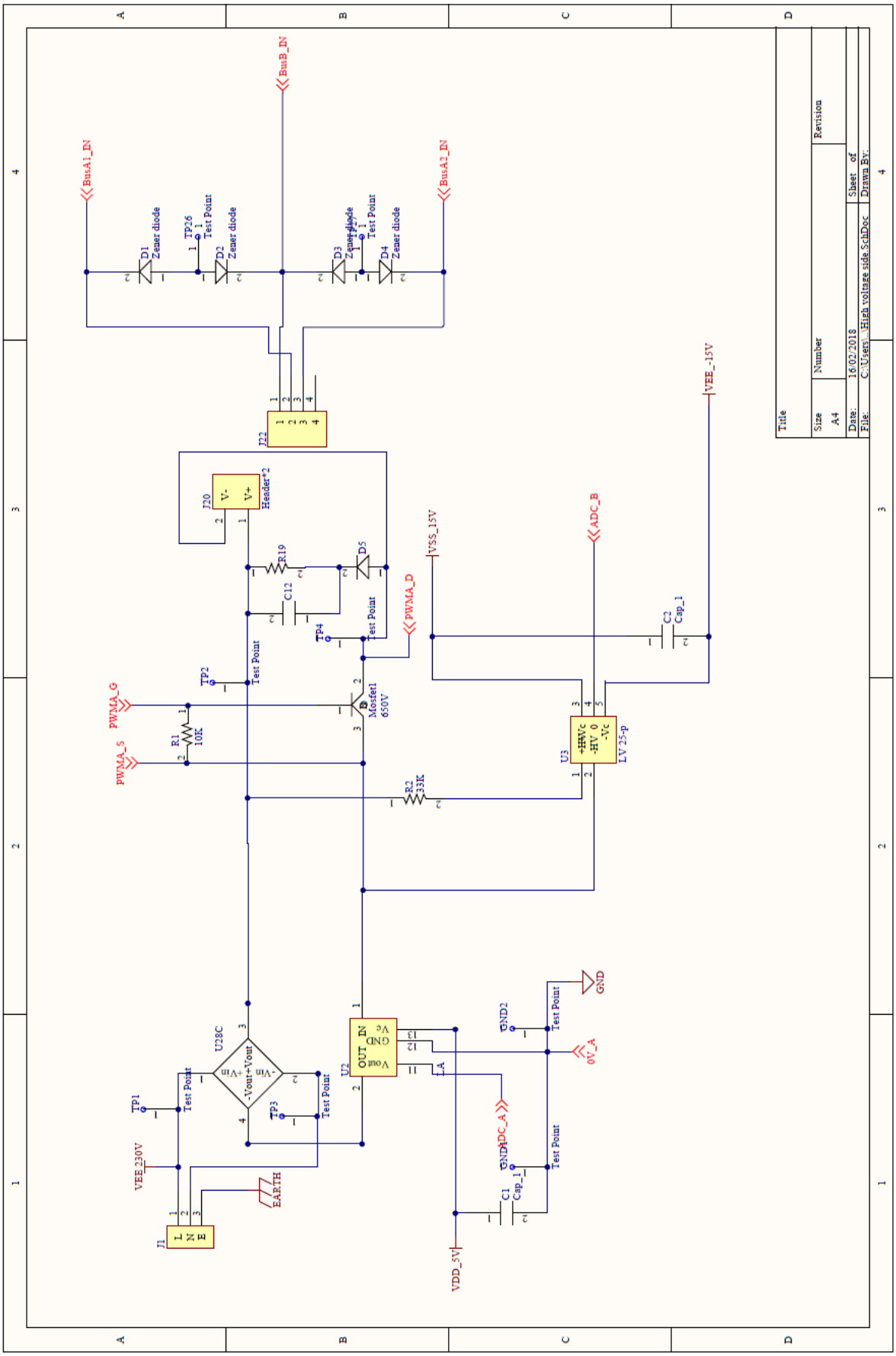
```
      EPwm4Regs.CMPA.half.CMPA = cmp4a;             // mosfet U8,U9
      EPwm4Regs.CMPB = cmp4b;                 // mosfet U10,U11
      EPwm5Regs.CMPA.half.CMPA = cmp5a;             // mosfet U12,U13
      EPwm5Regs.CMPB = cmp5b;                 // mosfet U14,U15
      EPwm6Regs.CMPA.half.CMPA = cmp6a;             // mosfet U16,U17
      EPwm6Regs.CMPB = cmp6b;                 // mosfet U18,U19
#endif


#if 1  // Send selected data to external RAM store
      flag2=1;     // extra store enable qualifier (can be useful)
      if(store_enable && flag2 && (ISR_count1%1 == 0) && (store_counter <
DATA_STORE_LEN))
      {
            s1[store_counter] = (int) B1;       //primary voltage xxxx
            s2[store_counter] = (int) B0;       //primary current xxxx
            //s3[store_counter] = (int) B2;       //secondary current Bus1
            //s4[store_counter] = (int) B3;       //secondary current Bus2
            //s5[store_counter] = (int) B4;
            //s6[store_counter] = (int) 1000*ia;
            //s7[store_counter] = (int) 1000*ib;
            //s8[store_counter] = (int) 1000*ic;
            store_counter++;                //increment store counter
            acc1+=v1;                             //sum selected variables
            acc2+=v2;
            acc3+=v3;
      }
#endif

      // The following code can be useful for calculating averages
#if 0
      ave1 = (int)(0.000488281*acc1);
      ave2 = (int)(0.000488281*acc2);
      ave3 = (int)(0.000488281*acc3);
#endif

      // Housekeeping at end of ISR
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
    AdcRegs.ADCTRL2.bit.RST_SEQ2 = 1;         // Reset SEQ2
      AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;           // Clear INT SEQ1 bit
      AdcRegs.ADCST.bit.INT_SEQ2_CLR = 1;           // Clear INT SEQ2 bit

      // Acknowledge this interrupt to receive more interrupts from group 1
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;

      T0_count = CpuTimer0Regs.TIM.half.LSW; // Latch lower 16-bits of timer0

}     // End of ISR

//---------------------------------------------------------------------------
--------------------
// EQEP1 interrupt (for testing only)
//

interrupt void eqep1_isr(void)

{
      if(EQep1Regs.QFLG.bit.WTO==1)
            enc_wdog++;
```

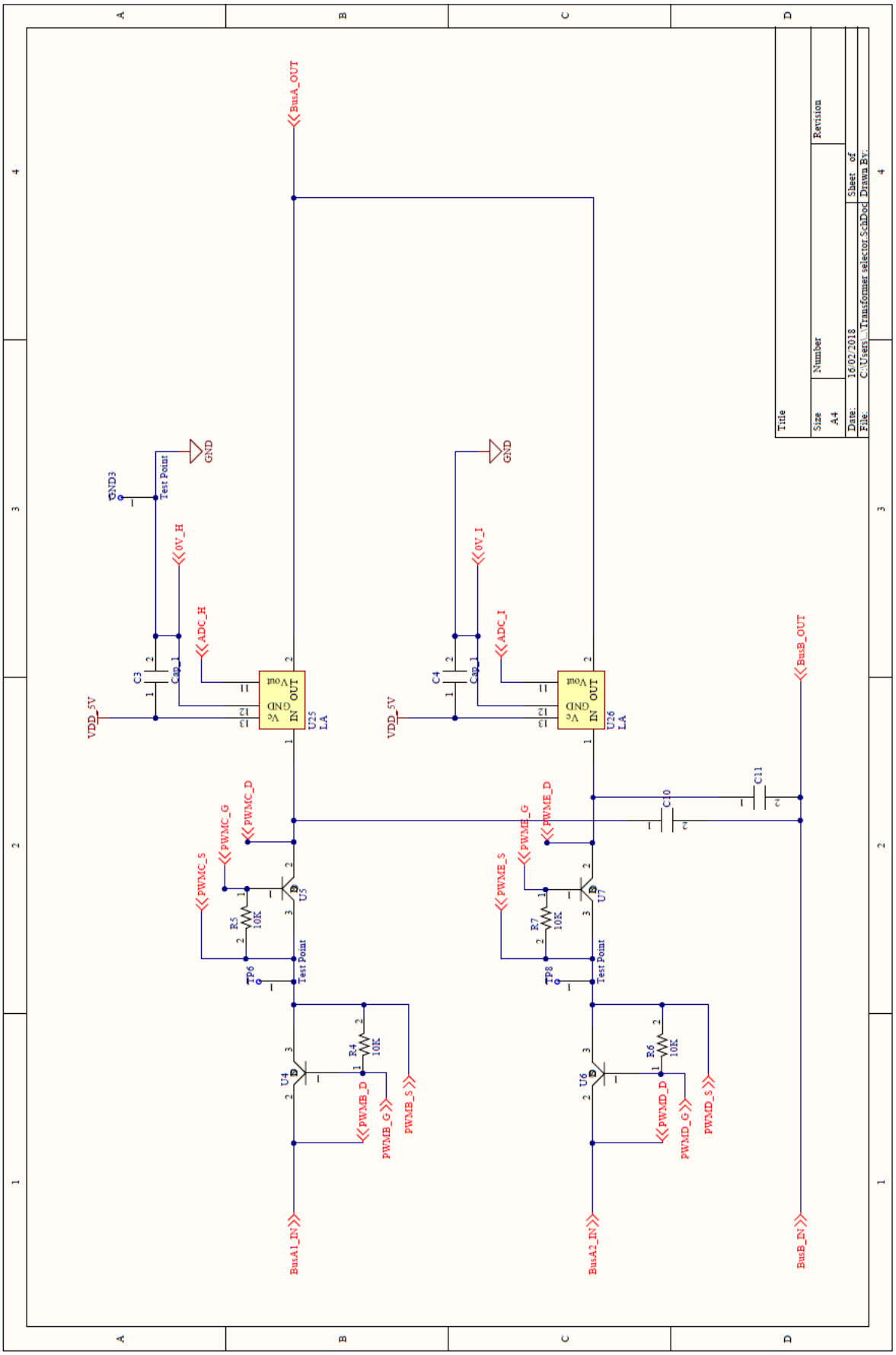
```
        if(EQep1Regs.QFLG.bit.QDC==1)
              reversal_count++;

//      EQep1Regs.QCLR.all = 0x9;               // Clear QDC and INT flags
        EQep1Regs.QCLR.all = 0x19;              // Clear WTO, QDC and INT flags

        PieCtrlRegs.PIEACK.all = PIEACK_GROUP5;
}
//---------------------------------------------------------------------------
--------------------
#pragma CODE_SECTION(set_up_data_stores, "codeA")
void set_up_data_stores(void)
{
        Uint16 i;

    s1 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s2 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s3 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s4 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s5 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s6 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s7 = (int *)calloc(DATA_STORE_LEN,sizeof(int));
        s8 = (int *)calloc(DATA_STORE_LEN,sizeof(int));

        // zero out store - note that this is not necessary when arrays are defined
with calloc()
        // can be useful if if initialising with other data is desired
        for (i=0; i < DATA_STORE_LEN; ++i)
              {
              s1[i] = 0x0;
              s2[i] = 0x0;
              s3[i] = 0x0;
              s4[i] = 0x0;
              s5[i] = 0x0;
              s6[i] = 0x0;
              s7[i] = 0x0;
              s8[i] = 0x0;
              }
}
void update_panel(void)
{
        Uint16 nc;                              // sprintf error code
        static char sbuf[100];          // output string for sprintf

        nc = sprintf(sbuf,"%u %u %u %u %u \r\0",B4,B5,B6,B7,B8);
    scia_msg(sbuf);
        nc = sprintf(sbuf,"%lu %lu %u %u
\r\0",LoopCount,ISR_count1,pos_count,QCTMR_count);
    scia_msg(sbuf);
        nc = sprintf(sbuf,"%d %u %d \r\n\0",trip_count,T0_count,TZflag);
    scia_msg(sbuf);
}
//---------------------------------------------------------------------------
// Send values to LabVIEW Data Transfer Interface (DTI)
void transfer_store_data_to_RS232(int frame_count)
{
        int d01,d02,d03,d04,d05,d06,d07,d08,d09,d10,d11,d12,d13,d14,d15,d16;
        int d17,d18,d19,d20,d21,d22,d23,d24,d25,d26,d27,d28,d29,d30,d31,d32;
        Uint16 index1,index2,index3,index4;
```

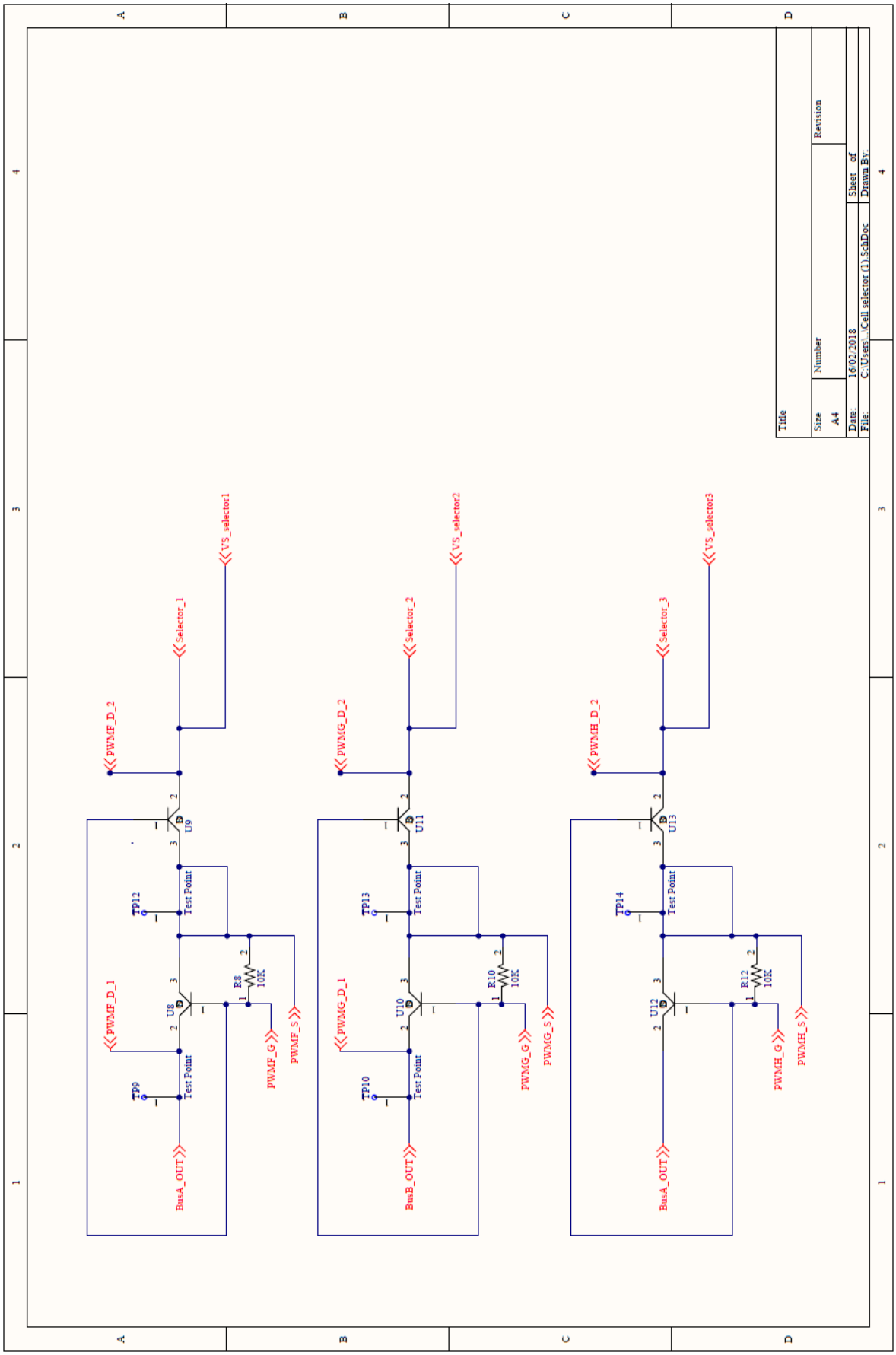
```
        Uint16 nc;
        static char sbuf[100];                          // output string for sprintf

        index1 = 4*frame_count;
        index2 = index1+1;
        index3 = index2+1;
        index4 = index3+1;

        d01  = s1[index1];
        d02  = s2[index1];
        d03  = s3[index1];
        d04  = s4[index1];
        d05  = s5[index1];
        d06  = s6[index1];
        d07  = s7[index1];
        d08  = s8[index1];

        d09 = s1[index2];
        d10 = s2[index2];
        d11 = s3[index2];
        d12 = s4[index2];
        d13 = s5[index2];
        d14 = s6[index2];
        d15 = s7[index2];
        d16 = s8[index2];

        d17 = s1[index3];
        d18 = s2[index3];
        d19 = s3[index3];
        d20 = s4[index3];
        d21 = s5[index3];
        d22 = s6[index3];
        d23 = s7[index3];
        d24 = s8[index3];

        d25 = s1[index4];
        d26 = s2[index4];
        d27 = s3[index4];
        d28 = s4[index4];
        d29 = s5[index4];
        d30 = s6[index4];
        d31 = s7[index4];
        d32 = s8[index4];

        nc = sprintf(sbuf,"%d %d %d %d %d %d %d %d %d
\r\0",index1,d01,d02,d03,d04,d05,d06,d07,d08);
        scia_msg(sbuf);
        nc = sprintf(sbuf,"%d %d %d %d %d %d %d %d %d
\r\0",index2,d09,d10,d11,d12,d13,d14,d15,d16);
        scia_msg(sbuf);
        nc = sprintf(sbuf,"%d %d %d %d %d %d %d %d %d
\r\0",index3,d17,d18,d19,d20,d21,d22,d23,d24);
        scia_msg(sbuf);
        nc = sprintf(sbuf,"%d %d %d %d %d %d %d %d %d
\r\n\0",index4,d25,d26,d27,d28,d29,d30,d31,d32);
        scia_msg(sbuf);
}
//===========================================================================
// End of code
//===========================================================================
```

Appendix C


Title
Size
A4
Number
Revision
Date:
16/02/2018
Sheet of
File:
C:\Users\...\Headers.SchDoc
Drawn By:
HDR*3_1016
HDR*2_PWM
Header*1
3.81mm
VCC_15V
VEE_-15V
VSS_15V
VDD_5V


BusB_IN
BusA1_IN
BusA2_IN
D1 Zener diode
TP26 Test Point
D2 Zener diode
D3 Zener diode
Test Point
D4 Zener diode
J22
J20 V- V+ Header*2
R19
D5
C12
TP4 Test Point
PWMA_D
TP2 Test Point
PWMA_G
PWMA_S
R1 10K
Mosfet 650V
R2 33K
U3 +HV 0 -HV -Vc LV 25-p
VSS_15V
ADC_B
VEE_-15V
C2 Cap_1
U28C -Vin +Vin -Vout +Vout
U2 OUT_IN GND Vout Vc
TP1 Test Point
TP3 Test Point
VEE_230V
EARTH
J1 L N E
GND2 Test Point
GND
0V_A
ADC_A
C1 Cap_1
VDD_5V
Title
Size A4
Number
Revision
Date: 16/02/2018
File: C:\Users\...\High voltage side.SchDoc
Sheet of
Drawn By:


BusA_OUT
BusB_OUT
GND
VDD_5V
0V_H
0V_I
ADC_H
ADC_I
PWMC_G
PWMC_D
PWMC_S
PWME_G
PWME_D
PWME_S
PWMB_G
PWMB_D
PWMB_S
PWMD_G
PWMD_D
PWMD_S
BusA1_IN
BusA2_IN
BusB_IN
U25
U26
U4
U5
U6
U7
C3
C4
C10
C11
R4
R5
R6
R7
10K
TP6
TP8
Test Point
Title
Size
A4
Number
Revision
Date:
16/02/2018
File:
C:\Users\...Transformer selector.SchDoc
Sheet of
Drawn By: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Revision
Date:
16/02/2018
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U9
TP12
Test Point
PWMF_D_1
U8
R8
10K
TP9
Test Point
PWMF_G
PWMF_S
BusA_OUT
VS_selector2
Selector_2
PWMG_D_2
U11
TP13
Test Point
PWMG_D_1
U10
R10
10K
TP10
Test Point
PWMG_G
PWMG_S
BusB_OUT
VS_selector3
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U13
TP14
Test Point
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R12
10K
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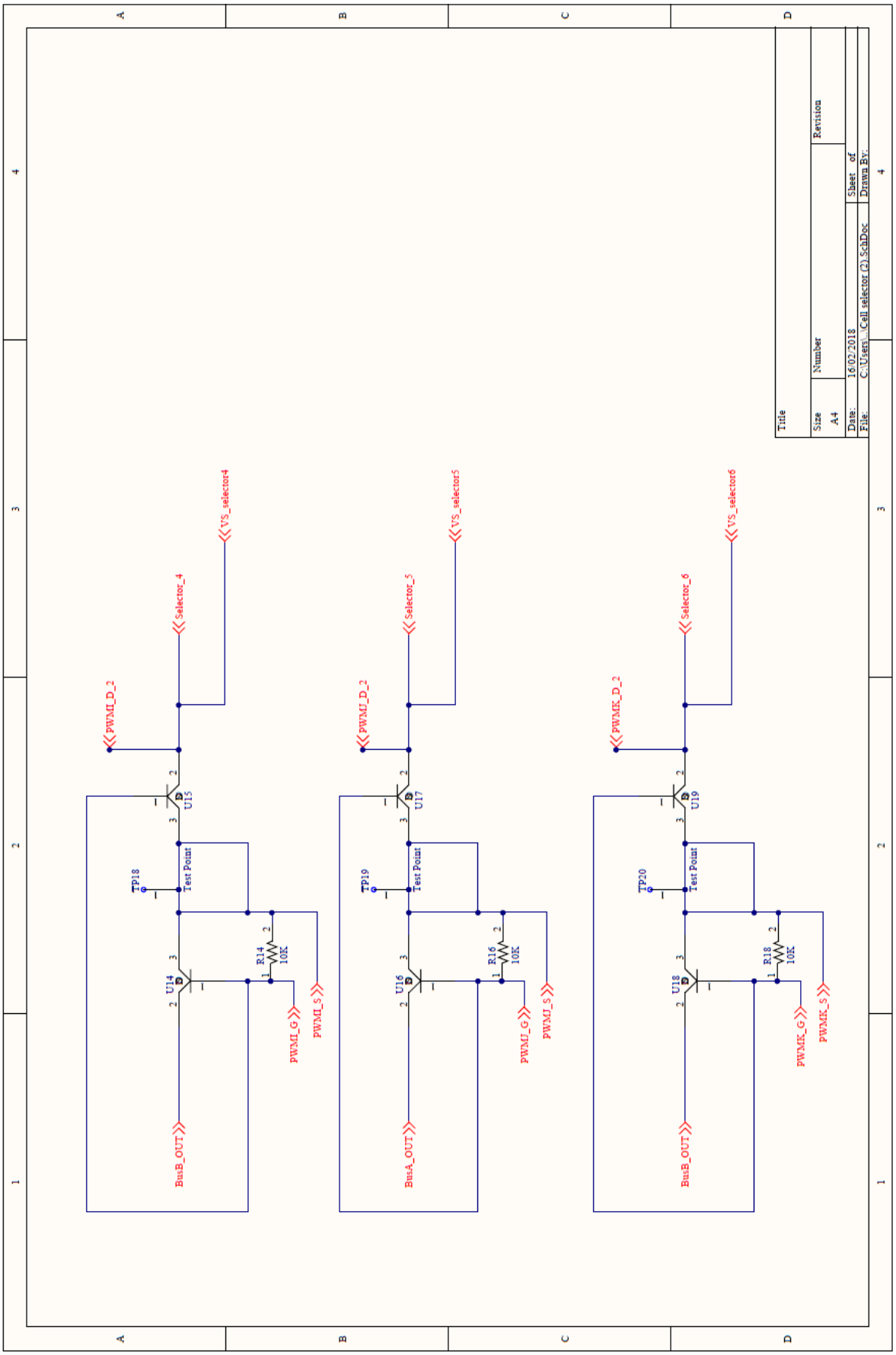
BusA_OUT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Date:
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TP18
Test Point
U14
R14
10K
PWMI_G
PWMI_S
BusB_OUT
VS_selector5
Selector_5
PWMJ_D_2
U17
TP19
Test Point
U16
R16
10K
PWMJ_G
PWMJ_S
BusA_OUT
VS_selector6
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U19
TP20
Test Point
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R18
10K
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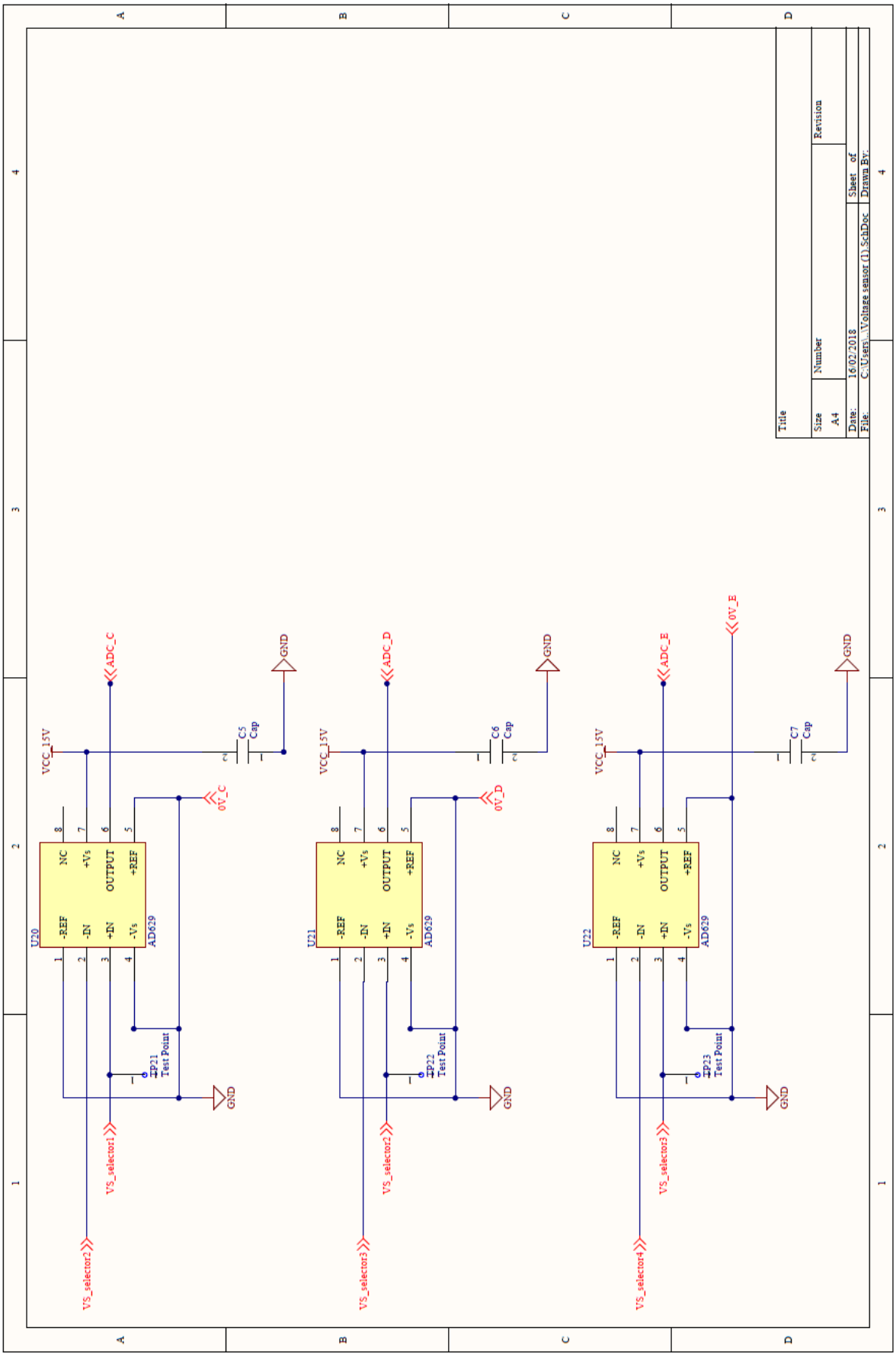
PWMK_S
BusB_OUT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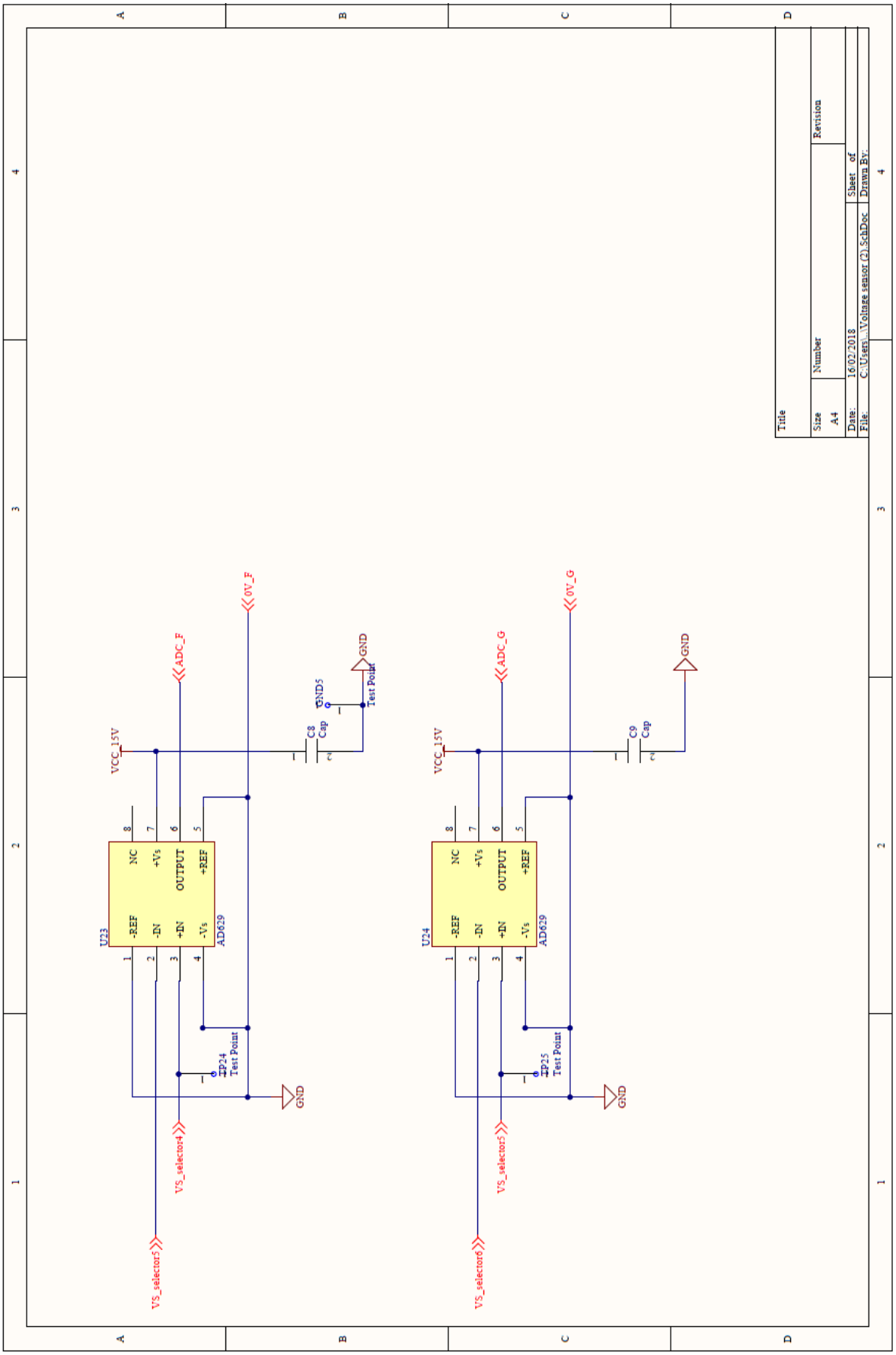
U20
U21
U22
AD629
NC
+Vs
OUTPUT
+REF
-REF
-IN
+IN
-Vs
ADC_C
ADC_D
ADC_E
0V_C
0V_D
0V_E
VCC_15V
GND
C5
C6
C7
Cap
TP21
TP22
TP23
Test Point
VS_selector1
VS_selector2
VS_selector3
VS_selector4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ADC_F
VCC_15V
GND
C8
Cap
GND5
Test Point
U23
AD629
NC
+Vs
OUTPUT
+REF
-REF
-IN
+IN
-Vs
TP24
Test Point
VS_selector4
VS_selector5
0V_G
ADC_G
C9
Cap
U24
TP25
Test Point
VS_selector6