Measurement Schemes with Reduced Number of Sensors for Modular Multilevel Converter

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ABSTRACT

During the last four decades there has been considerable development in voltage source converters (VSCs), which are widely contributed in multilevel converter topologies. Since then, multilevel VSC topologies have been used for applications with different power rating owing to the improvement of the output waveforms quality and minimising filtering requirements. In comparison with the conventional multilevel converters, modular multilevel converter (MMC) is considered as the most attractive topology for high and medium-power applications mainly due to the series connection of a high number of submodules (SMs).

The challenges associated with the implementation of a high number of SMs includes: voltage-balancing of the distributed SM, cost, reliability and the increased complexity in the circuit configuration. Furthermore, achieving efficient and fast closed-loop control of the MMC requires the accurate knowledge of the voltage and current measurements, which means a considerable number of sensors are usually required to operate the MMCs.

The main objective of this research is to propose several novel strategies for the converter to achieve voltage-balancing with fewer number of sensors to produce comparable performance to the sensor-based method. Four different sensorless schemes have been investigated, where two are current sensorless-based techniques and two are voltage sensorless-based techniques. The proposed current sensorless schemes are based on developed sorting algorithm, and the proposed voltage sensorless schemes employ two novel different recursive algorithms with the standard sorting algorithm. In regards to the voltage sensorless schemes, the first proposed method uses an exponentially weighted recursive least square (ERLS) algorithm, while the second proposed method employs a Kalman filter (KF) to estimate the SM capacitor voltages. Capacitance uncertainty has been investigated for the proposed voltage sensorless schemes. The proposed methods have been implemented via simulation but also on a scaled-down laboratory prototype.

The thesis also deals with capacitor diagnosis where a new scheme has been proposed which may be used for health monitoring technique, a comparison with an existing technique has been evaluated.

Detailed simulations and experimental tests are carried out to investigate the performance of the proposed sensorless schemes, and results are compared with the sensor-based approach. These various schemes have been implemented and tested in real-time using a commercial floating point microcontroller where a 4-level single-phase MMC was employed. The results achieved for these novel schemes show an important improvement in the performance of the MMC under different operation conditions while fewer sensors were used.

DEDICATION

I dedicate my dissertation work to my loving parents: "*Alshebani Abushafa & Khiriya Almadhoon*"

اهدي هذه الاطروحة الي احبتي ابي وامي: "الشيباني ابوشعفة و خيرية المدهون"

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First and foremost, my deepest thanks always go to Allah for giving me the ability and the patience to complete this work.

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I have the deepest gratitude for my beloved parents, brothers, sisters, my wife and my little kids for always being supportive whenever I needed them to. Without their support this work would not have been completed, thanks again to my beloved family.

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LIST OF SYMBOLS

L_s : Arm inductor

S_x : Switching states of an MMC SM

C_x : SM Capacitor

e : error between measured and estimated values

f : Output frequency

f_c : Carrier frequency

$f_{sampling}$: Sampling frequency

i_{cir} : Circulating current

i_{cir-ph} : Circulating current of the phase

I_{dc} : DC link current

i_{l-ph} : Lower phase arm current

i_{lower} : Lower arm current

i_{load} : Load current / output current

$i_{load-ph}$: Phase load current

i_{u-ph} : Upper phase arm current

i_{up} : Upper arm current

J_u : Cost function

λ : Forgetting factor

K : Kalman gain

L : Load inductance

LS   : Least Square

N : Total output voltage levels

m_i : Modulation index

n : Number of SM per arm

P : Covariance matrix

r : Number of carrier signals

R   : Load resistor

R : Error covariance matrix

Ra   : Arm resistor

$\boldsymbol{u_a}$: Output voltage

$\boldsymbol{u_l}$: Lower arm voltage

u_u : Upper arm voltage

V_{dc} : DC-link voltage

$\mathbf{V}_{cx}$: Voltage across SM capacitor

$\mathbf{V}_{SM}$: Voltage across SM

w : Processing noise

$\boldsymbol{\alpha}$: Shifted angle between carrier signals

β : Number of SMs to be involved.

θ   : Vector parameter.

Superscripts

$\widehat{...}$: Estimated value

$\overline{...}$: Complementary value

LIST OF ABBREVIATIONS

AC : Alternating current

ADC : Analogy to digital converter

APOD : Alternative phase opposition disposition

BESS : Battery energy storage system

BMS : Battery management system

CCS : Code Composer Studio

CHB : Cascaded H-Bridge

DC : Direct current

DGs : Distributed generations

DSP : Digital signal processor

ERLS : Exponentially weighted recursive least square

ESR : Equivalent series resistance

FACTS : Flexible AC transmission systems

FCC : Flying capacitor converter

HVDC : High voltage direct current

IGBT : Insulated gate bipolar transistor

IGCT : Integrated gate commutated thyristor

KF : Kalman filter

MMC   : Modular multilevel converter

MOSFET   : Metal-oxide semiconductor field-effect transistor

NPC   : Neutral point clamped

PWM   : Pulse width modulation

PD   : Phase disposition

PI   : Proportional integral

POD   : Opposition disposition

RLS   : Recursive least square

RT-WEC   : Real-Time Workshop Embedded Coder

VSCs   : Voltage source converters

SM   : Submodule

SVPWM   : Space-vector pulse-width modulation

STATCOM: Static synchronous compensator

TSP   : Target Support Package

CHAPTER 1

INTRODUCTION

1.1 Voltage Source-Based Converters

It is well known that the growth in the need for power electronic converters has been exponential due to the increased demand for medium-and high-power applications. These applications are usually operated based on voltage source converters (VSCs), which are mainly driven by medium-and high-power semiconductor devices such as the metal-oxide semiconductor field-effect transistor (MOSFET), the insulated gate bipolar transistor (IGBT) and the integrated gate commutated thyristor (IGCT). Two-level and multilevel converters can now be found everywhere. However, as the main advantages of multilevel converters is the increase in output power level, this increase in VSC-based systems provides significant improvements over two-level VSC topologies. These include reduced filtering size and the low switching frequency required, which lead to lower switching losses. In addition, multilevel VSC topologies provide reduced semiconductor stresses due to distribution of the switching effort between the high numbers of semiconductor switches involved [1-4].

1.2 Challenges Associated with Multilevel Converters

Different multilevel converter topologies have already been used in industry. One of the most attractive topologies for medium-and high-power applications is modular multilevel converter (MMC). More details as well as the most attractive features of MMCs compared to other conventional multilevel converter topologies are presented in Chapter 2.

Despite the use of multilevel topologies, each topology provides certain advantages; however, a number of challenges in their operation are also apparent, such as, reducing switching frequencies and the control of internal and output converter signals. Voltage and current control requirements are one of the most important challenges with these converters. Due to the high numbers of components which are usually involved in the multilevel converter structure, achieving such control increases overall system complexity and therefore decreases reliability. These two concerns of complexity and reliability specifically for MMCs are the main focus of this thesis.

1.3 Objectives of the Thesis

The main objectives of the thesis are:

- To conduct a comprehensive study that contributes to the development of multilevel converters in general.

- To investigate the requirements and issues associated with MMCs.

- To propose novel voltage-balancing methods that can reduce the complexity and therefore the cost of the MMC when a medium or high output level of the converter is required. Usually with the conventional voltage-balancing methods, high number of sensors are needed. Therefore, the objectives of this research focus on developing new online sensorless schemes which can achieve the voltage-balancing of the converter with fewer voltage and current sensors.

- To develop a new online health condition monitoring scheme for the capacitors used in the series connected SMs which can improve MMC reliability.

- To develop a scaled down experimental set-up system that confirms the effectiveness of all proposed sensorless methods in this work.

1.4 Topologies and Tools Used

The results achieved in this work are based on detailed simulation and experimental analysis. The simulation results obtained in the thesis are provided by simulations in MATLAB/Simulink/Simpower, of which two different versions have been used (2012 © and 2015 ©). The experimental results achieved in Chapters 4, 5 and 6 are implemented using the TMS320F28335 microcontroller from the Texas Instruments semiconductor manufacturing company. The implementation of the methods proposed in those chapters are uploaded to the digital signal processor (DSP) with the help of Code Composer Studio (CCS5.5) development tools from the same supplier (Texas Instruments). A scaled down 4-level MMC is developed to validate all suggested sensorless schemes. Details of the practical implementation are presented in Chapter 3.

1.5 Thesis Contributions and Publications

The work reported in this thesis focuses on reducing the complexity of the MMC and improving its reliability under different operating conditions. The main contributions of the thesis are summarised as follows:

- Two current sensorless approaches are investigated for the converter to achieve voltage stability with lower cost and complexity (Chapter 4). In the first proposed method, monitoring load current is only required for the controller, whereas the second proposed scheme does not require any current monitor to achieve the voltage-balancing of the converter.

- A novel voltage sensorless scheme is proposed based on an exponentially weighted recursive least square (ERLS) algorithm (Chapter 5). The proposed technique is performed and evaluated at steady-state and dynamic conditions for both simulation and practical studies.

- A novel voltage sensorless approach is proposed for the converter based on the Kalman filter (KF) algorithm (Chapter 6). Employing KF with the converter is used for the first time to address the issue of the high numbers of voltage sensors required. .

- A new capacitance estimation scheme is proposed for the converter to improve system reliability.

- A comprehensive understanding is developed of the MMCs requirement and issues.

The work presented in this thesis has resulted in a number of published and submitted papers to different international conferences and journals as follows:

1. **O. Abushafa**, M. Dahidah, S Gadoue, and David Atkinson "Submodule Voltage Estimation Scheme in Modular Multilevel Converters with Reduced Voltage Sensors Based on Kalman Filter Approach," submitted to *IEEE Transactions on Industrial Electronics*, 17-TIE-0266, 2017.

2. **O. Abushafa**, S. Gadoue, M. Dahidah, and D. Atkinson "Capacitor Voltage Estimation Scheme with Reduced Number of Sensors for Modular Multilevel Converters" submitted to *IEEE Transactions on Emerging and Selected Topics in Power Electronics*, JESTPE-2017-09-0606.

3. **O. Abushafa**, S. Gadoue, M. Dahidah, and D. Aktinson, "Capacitor Voltage Estimation in Modular Multilevel Converters using a Kalman Filter Algorithm," in International Conference on *Industrial Technology* (*ICIT*)*, Seville, IEEE,* 2015, pp. 3016-3021.

4. **O. Abushafa**, S. Gadoue, M. Dahidah, and D. Atkinson, "A New Scheme for Monitoring Submodule Capacitance in Modular Multilevel Converter", *in Power Electronic and Machines Drives* (*PEMD*), *2016, IET, Glasgow.*

5. **O. Abushafa**, S. Gadoue, M. Dahidah, D. Atkinson, and S. Ethni, "Control Strategies for Capacitor Voltage Balancing in Modular Multilevel Converters."in the 7th International Renewable Energy Congress (*IRNC*), 2016, *IEEE*, Hammamet, pp. 1-6.

Throughout the study period, various academic awards have been recevied which are listed below:

- **First place** for the "Best Paper Presentation" in the Annual Research Conference 2016 (ARC-2016) at Newcastle University.

- **Third Place** for the "Best Paper" in the (ARC-2016) of Newcastle University.

- **Best Presentation** of research in the Electrical Power Group at the School of Electrical and Electronic Engineering (ARC-2015) of Newcastle University.

1.6 Layout of the Thesis

The thesis is organised in 8 chapters as follows:

Chapter 2 presents details of the MMC in terms of structure, principles of operation, modelling and control strategies needed. Greater emphasis is given to up-to-date attempts to reduce the converter's complexity. This includes achieving converter stability with fewer voltage and current sensors, and different methods are reviewed and discussed. The chapter also provides a literature review on capacitance estimation strategies.

Chapter 3 provides details of the experimental set-up used in this work. It describes selected components in the converter, including the voltage and current sensors used. In addition, it also provides a brief description of selected digital signal processors.

Following this, the procedure used for implementing all methods proposed in Chapters 4-6 is detailed.

Chapter 4 presents two current sensorless methods for the MMC. A detailed description of the conventional voltage-balancing scheme based on a sorting algorithm is discussed first in the chapter. This conventional scheme is also used in Chapters 5-7. Extensive simulation and experimental results that compare the two proposed methods with the conventional voltage-balancing method are then provided in the rest of the chapter.

Chapter 5 proposes a novel voltage-balancing method with fewer voltage sensors. An ERLS algorithm is employed in this chapter to achieve voltage-balancing with lower complexity. Simulation and experimental studies under different operating conditions are discussed along with the manner in which the proposed scheme is implemented.

Chapter 6 introduces another novel voltage-balancing method based on reducing the number of voltage sensors required. This chapter suggests the use of the KF for the converter. Similar to that in Chapter 5, the results of the scheme proposed in Chapter 6 demonstrate the effectiveness of the proposed algorithm under steady-state and dynamic operating conditions. All the obtained results are experimentally verified using the test rig described in Chapter 3.

Chapter 7 describes a new approach for capacitance estimation based on the KF algorithm. The method is compared with an existing approach based on a recursive algorithm and both methods are validated through simulation analyses.

Finally, Chapter 8 concludes the work, summarises the contributions of the study and makes some possible suggestions for future work.

CHAPTER 2

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MODULAR MULTILEVEL CONVERTER: PRINCIPLES OF OPERATION, MODELLING & CONTROL, AND APPLICATIONS

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2.1 Introduction

The importance of using power conversion is described in this part of the chapter, where the focus is mainly on the MMC. Using power converters is essential nowadays to convert power from one form into another (e.g. AC-DC, DC-AC, AC-AC or DC-DC). However, some challenges remain. The power obtained from such conversion is controlled based on the demand of the application via semiconductor switches. The power can be boosted, bucked or similar to the input level; however, the output frequency may also be different. The application attached to the converter decides this demand. In general, power converters can be found everywhere; in houses, or work, in industry, in various modes of transportation such as trains and electrical vehicle, and in hospitals.

Many studies are still being carried out to overcome the challenges associated with converters. There are many areas which still need to be improved in this regard. As a researcher with engineering background, three main areas are always under the microscope: the efficiency, cost and reliability of the targeted system. Details about these three gaps are addressed later in main body of the thesis including the rest of this chapter.

2.2 Conventional Multilevel Converters

A brief introduction to the conventional multilevel converters and their applications is provided here prior to introducing MMC topology. Three main multilevel converter topologies are well-developed and commonly used [1]. These include neutral point clamped (NPC) converter [5], cascaded H-bridge converter (CHC) [6] and flying capacitor converter (FCC) [7]. According to one review [2], these converters were first proposed more than four decades. A single phase (one-leg) illustrations of these topologies are shown in Fig. 2.2.

Other variations of multilevel converters, including hybrid and matrix configurations have been also investigated and reported in the literature (see Fig. 2.1). Examples of the Hybrid topologies is a combination between NPC and CHC or FCC and CHC [8]. The combination of two conventional or not conventional multilevel converter usually provide more features to the system. For example, the combination between NPC and CHC reduces the common mode voltage and improves power quality [9].

All aforementioned conventional technologies have been widely examined and accepted. They were introduced in the market and have been used in real applications for some time in various industrial applications for both medium and high power voltage rate [8].
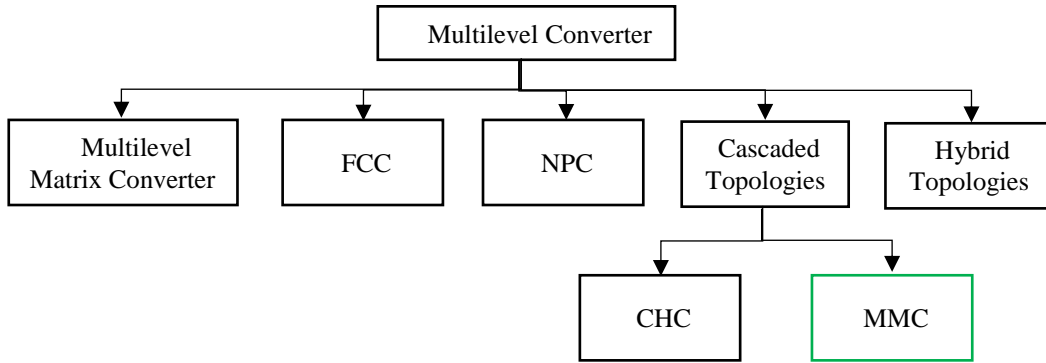
Fig. 2.1. Classification of medium and high voltage multilevel converters.
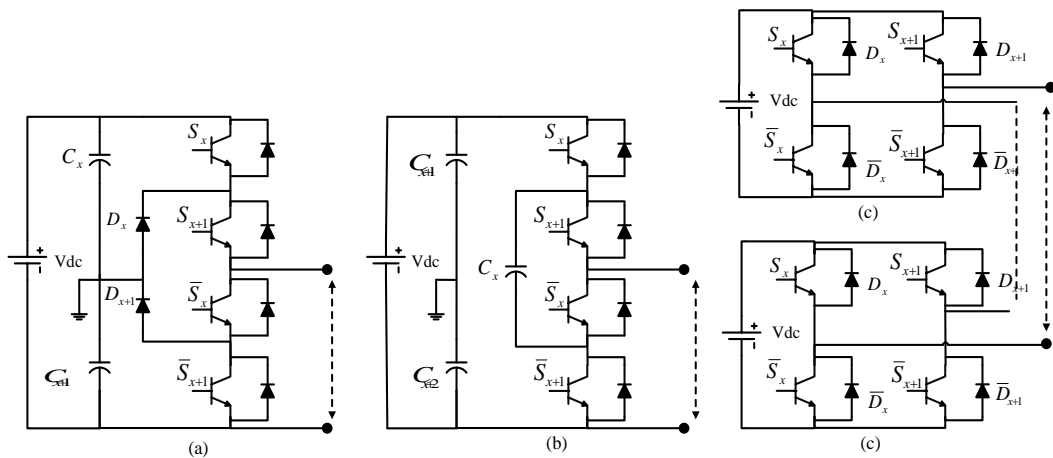
Fig 2.2. Conventional multilevel converter topologies: (a) Three-level NPC converter, (b) Three-level FCC and (c) Five-level CHC.

2.3 The MMC: Structure and Principles of Operation

Fig. 2.3 shows the basic circuit configuration of a three-phase MMC. The converter consists of two arms; each of which has a series connection of cascaded submodules SMs and an arm inductor (L$_s$). In most cases the configuration of these SMs is a half-bridge configuration as illustrated in Fig. 2.3 (b). Although the name MMC is usually related to half-bridge configurations; however, different arrangements can also be found in the literature such as full-bridge SM, three-level FCC, three-level NPC or hybrid arrangements [10]. The application will define the type of SM configuration which fits the system better [11].
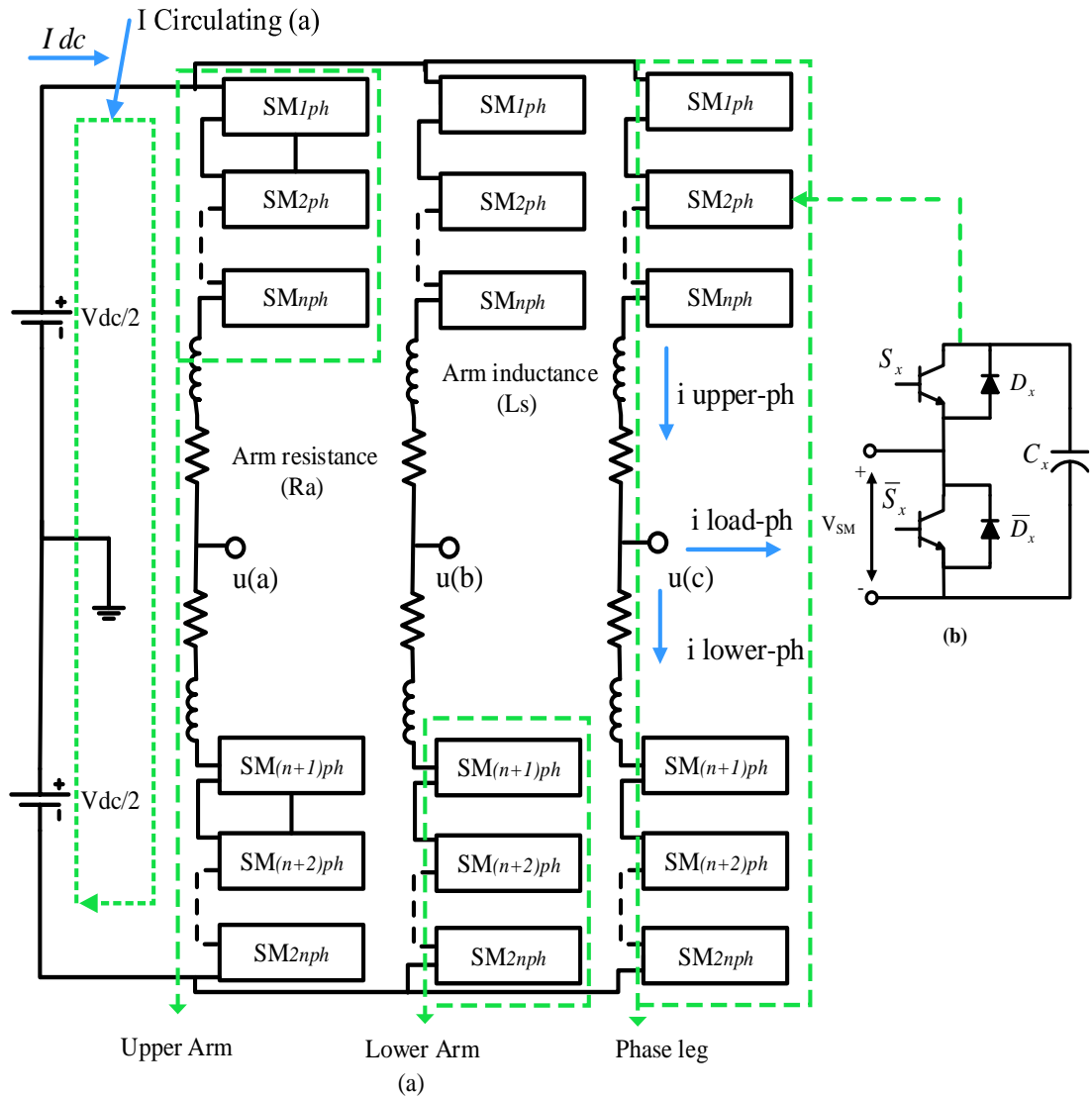
Fig 2.3. Block diagram of MMC. (a) Three-phase block diagram. (b) Half-bridge SM configuration.

Considering the half-bridge configuration in Fig. 2.3, three switching states exist based on the status of S_x and $\bar{S}_x$. In state one, both S_x and $\bar{S}_x$ are **OFF**, and this may happens during start-up or in the case of series failure [12], but this state is usually omitted during software simulation. In the second state, S_x is switched **ON** and $\bar{S}_x$ remains **OFF,** the output voltage is equal to the voltage across the capacitor C_x ($\mathbf{V}_{cx}$), where $x = 1,2, \dots 2n$, and n is the number of SMs per arm. The charging and discharging of the SM capacitor depends on the direction of the current passing

through this SM, and this state is known as the **ON** state [13]. In state three, the SM voltage output is zero (**OFF** state), and this occurred when $\overline{S_x}$ is **ON** and S_x is **OFF**.

For clarity purpose, the directions of the current flowing through both diodes and semiconductor switches in the three states are depicted in table 2.1, whereas, table 2.2 shows the only two main switching states during normal operating conditions [12] [14].

The buffer inductors (L_s) in Fig. 2.3 have an important role in the operation of MMC. They not only assist in reducing the circulating current within the converter arms [15], but they also support the system when faults occur [16].

Total arm resistance (Ra) shown in the figure are usually omitted in the converter model; however, for the sake of accuracy, this small resistor should be added to the overall mathematical model.

Table 2.1. Current flow directions in the half bridge SM
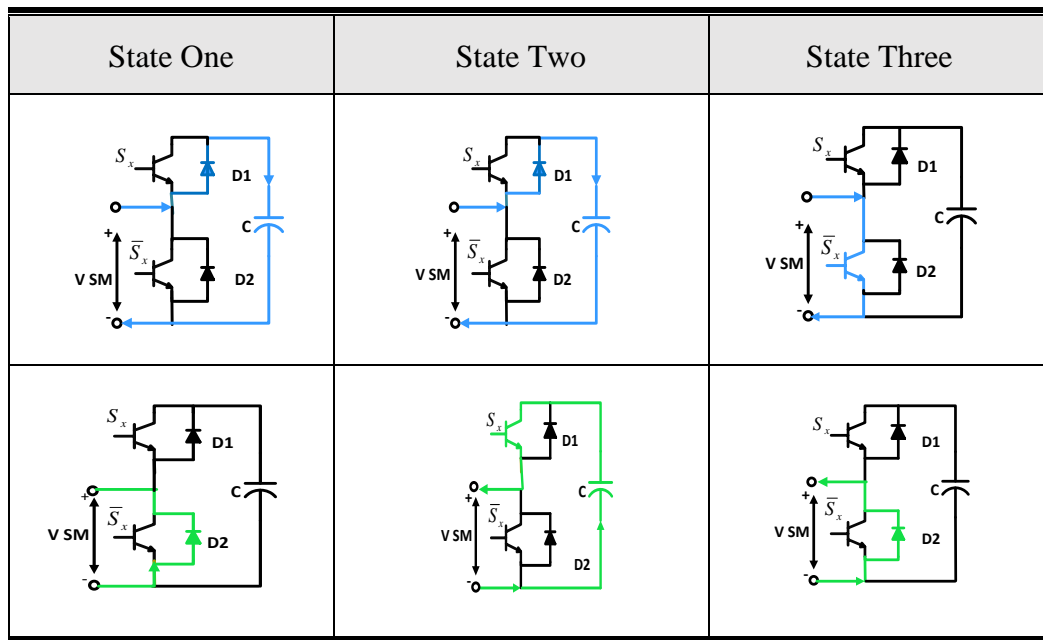
Table 2.2. Switching signals and the output states of the SM

State of the SM	S_x	$\overline{S_x}$	V_{SM}
ON	**ON**	**OFF**	V_{cx}
Off (bypassed)	**OFF**	**ON**	0

2.4 Currents Analysis in MMC

As the operation of MMC relies on the different currents following through the circuit, it is therefore essential to understand these currents in order to fully understand the operation of converter. Fig. 2.3 illustrates the directions of currents in the MMC, which are: output current (i_{load}), DC link current (I_{dc}), arms currents (i_{up}) and (i_{lower}) and circulating current (i_{cir}). These are defined in more details in the following paragraphs.

2.4.1 Output and Arm Currents

The output current $(i_{load-ph})$ can be calculated by subtracting the lower arm current from the upper arm current within the same phase, thus $i_{load-ph}$ is defined as [17]:

$$i_{load-ph} = i_{u-ph} - i_{l-ph} \quad \text{where } ph = a, b \text{ or } c \tag{2.1}$$

where the upper (i_{u-ph}) and lower (i_{l-ph}) arm currents are defined by equations (2.2) and (2.3) respectively:

$$i_{u-ph} = i_{cir-ph} + \frac{i_{load-ph}}{2} \tag{2.2}$$

$$i_{l-ph} = i_{cir-ph} - \frac{i_{load-ph}}{2} \tag{2.3}$$

2.4.2 The Circulating Current

By substituting $i_{load-ph}$ in equation (2.1) into (2.2) or (2.3) the definition of circulating current can then be defined as:

$$i_{cir-ph} = \frac{i_{u-ph} + i_{l-ph}}{2} \tag{2.4}$$

This current is one of the main challenges in the MMC circuit, and many studies have investigated different means to supress or minimise it. Large circulating current can seriously influence the semiconductor components, increases losses and leads high voltage ripple in the SM capacitors [18].

2.5 The MMC Output Voltage

As shown in Fig. 2. 3(a), the output voltage of phase-leg a of the converter (u_a) can be expressed as follows [19]:

$$u_a = \frac{u_l - u_u}{2} - \frac{L_s}{2}\frac{di_{load-ph}}{dt} \tag{2.5}$$

where u_u is the total output voltage of the upper cascaded SM$_S$ (from 1 to n) and u_l is the total output voltage of the lower cascaded SM$_S$ (from $(n+1)$ to $2n$).

The total output voltage levels (N) that can be achieved using this multilevel topology is $N = (1 + n)$ (line-neutral), where n is the number of SM per arm. Higher output levels can be achieved up to $2n + 1$, where the arms of the same phase are modulated independently [20]. More information about increasing output level is presented in Chapter 4.

2.6 Features Associated with the MMC Topology

Due to the modular construction of the MMC in comparison with two, three and some conventional multilevel VSC converters, the MMC topology has the following features [12, 21, 22]:

- Low harmonics can be achieved in the output voltage and current waveforms because of the series connection of high number of SMs.

- Reduced size (or even no) of filtering circuit.

- Generally, the MMC has low switching losses due to the low switching frequency required.

- Due to the fact that each SM has its own DC capacitor, the DC linked capacitor can be neglected [22]. Consequently, this will decrease the total cost of the converter connection as well as improving its performance and reliability in the case the appearance of faults [16]. As is known, the presence of a DC

capacitor will cause a high surge current plus consequent damage to the system, particularly when a fault at the DC bus side is not prevented [22].

- In a DC link when a pole-to-pole fault occurs, the total system stability can be recovered quickly because only a few sub-module capacitors are discharged.

- Arm inductance does not have any side-effects on the systems operation. On the contrary, it supports system stability.

- Similar to the CHC converter, it has scalability and flexibility by adding identical SM cells.

- Fault tolerant feature (i.e. in the case of a sudden fault occurring in one of the SMs, the other residual SMs can manage system stability without switching off the whole leg (phase) when an appropriate control method is used. Only unhealthy cells should be bypassed).

2.7 MMC Modulation Strategies

This section reviews the most commonly used up-to-date modulation strategies for controlling voltage capacitors (voltage-balancing control) in MMCs. Over the last few years, different modulation strategies have been developed and investigated for MMCs. Regardless of the applications, Fig. 2.4 classifies these methods into two main groups: space vector-based algorithms and voltage level-based algorithms. The range of switching frequency has also been taken into consideration in this categorisation. To date, very few studies control the MMC based on the space-vector algorithm [23], whereas the majority of recent studies are based on voltage level-based algorithms as can be seen in the figure. Although multicarrier pulse width modulation (PWM)-based algorithms are classified as high switching frequency algorithms, most of the recent literature still consider them. This is mainly because of their ease of implementation when a sorting algorithm is used. However, several attempts have been reported to achieve successful voltage-balancing with lower switching frequency when the multicarrier PWM-based algorithm is used. For example, an improved phase-shifted-

based algorithm has been proposed for the hybrid MMC [24].

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                          ┌─────────────────────┐
                          │   MMC    Modulation  │
                          │      Techniques      │
                          └─────────────────────┘
                   ┌────────────────┴────────────────┐
          ┌──────────────────┐            ┌──────────────────┐
          │ Space Vector Based│            │   Voltage Level  │
          │ Algorithms [27]   │            │ Based Algorithms │
          └──────────────────┘            └──────────────────┘
           [yellow bar]
```

Fig. 2.4 flowchart:

- MMC Modulation Techniques
  - Space Vector Based Algorithms [27] (Mixed Switching Frequency — yellow)
  - Voltage Level Based Algorithms
    - Hybrid Modulation [29] (High Switching Frequency — red)
    - Multilevel PWM
      - Phase Shifted PWM [32] [33] (High Switching Frequency — red)
      - Level Shifted PWM
        - PD-PWM [34-36] (red)
        - POD-PWM [37] (red)
        - APOD-PWM [37] (red)
    - Selective Harmonic Elimination [30] (Low Switching Frequency — green)
    - Nearest Level Control [31] [36] (Low Switching Frequency — green)

Legend:
- Red — High Switching Frequency
- Yellow — Mixed Switching Frequency
- Green — Low Switching Frequency

Fig. 2.4. MMC Modulation Strategies.

2.8 Challenges Associated with the MMC

Despite the attractive features of the MMC which have been mentioned in section 2.6, there are some challenges associated with this kind of multilevel converters, especially if a high output level is required. Therefore, maintaining the voltage-balancing control of the capacitors' voltage requires many voltage sensors due to the use of high number of semiconductor devices and SM capacitors, which in turns increases the cost and the complexity of the system.

Another considerable challenge is the reliability of the converter. This is mainly because of the series connection of such components (i.e. semiconductor switches and SM capacitors). In addition to voltage-balancing control, the circulating current which

appears within the converter's leg is another challenge (i.e. current control issue). This current influences the level of voltage ripple within the SM capacitors. The main challenges associated with MMCs are surmised below:

- Voltage control (voltage-balancing of SM capacitor voltages)

- Current control (circulating current within the converter legs which may effect on the SM voltage ripple).

- Reliability and complexity due to the series connection of high number of SMs.

- Parameter design (mainly for SM capacitance C_x and arm inductance L_s)

There have been great efforts put by the researchers towards addressing the voltage and current control issues. Three main control objectives for the MMC are widely considered in the literature, which are input current, output voltage and output current [34]. In this study, only the output voltage issue is investigated, aiming to achieve capacitor voltage-balancing with fewer voltage and current sensors. Whereas the issue of inner circulating current within each phase is beyond the scope of this study.

2.9 Control of SM Capacitor Voltage with Voltage and Current Sensors

The majority of the existing solutions for voltage-balancing rely on monitoring each individual SMs voltage and arm current. However, due to the fact that MMCs are usually designed with high output levels, this means high numbers of voltage sensors are also required. For example the commissioned MMC converter presented in [35] utilizes hundreds of SMs per arm, which requires enormous numbers of voltage sensors in order to achieve the voltage-balancing of the SMs capacitors. The control of SM capacitor voltage with voltage and current sensors has been extensively investigated in recent research [27, 28, 30, 36, 37], but many voltage sensors are always used in such studies. However, it would be preferable if this issue could be resolved with lower cost and complexity.

2.9.1 Averaging and Balancing Control Method

This method has been presented in [28], where two steps were used to regulate the converter's voltages: averaging control and balancing control. Both steps are based upon a simple proportional integral (PI) controller. In the averaging step, the average voltage arm is forced to follow its command value. An inner current loop is also included in this step so that the averaging voltage follows its command voltage without being affected by the converter load. However, a higher number of sensors still needed for measuring and monitoring all SM capacitors. Another disadvantage associated with this method is that, when the structure of the MMC is being changed, such as when the output level is increased, the parameters of the controller must be retuned again. In addition, in the case of a fault, when one SM is being bypassed, the proportional and integral gains of the PI controller need to be readjusted.

2.9.2 Sorting Algorithm-based Method

Regardless to the modulation strategies used, such as those illustrated in Fig. 2.4, the idea of a sorting algorithm-based method is to sort all arm SM voltages in descending/ascending order [31]. This means monitoring all SMs' voltages are required. In the Figure bellow the main requirement steps of achieving voltage-balancing control are shown. By considering the upper arm, the lowest capacitors will be charged when the upper current is positive and their values will be increased. However, if the upper current is negative, the capacitors with the highest value will be discharged. The number of capacitors that should be involved in the process is also defined by the algorithm. On the other side of the converter, the lower control algorithm works exactly in the same way. However, charging or discharging actions in the lower part of the converter depend on the direction of the lower arm current rather than the upper arm current. Similarly, the lowest capacitors will be charged when the lower current is positive and their values increases. Conversely, if the lower current is negative, the capacitors with the highest value will be discharged [31]. In terms of the computational complexity, this method does not require high execution time, however and similar to averaging and balancing control method, complexity

might be an issue due to high measurement signals involved in the process. More details on this principle are explained in Chapter 4.

Reference signal
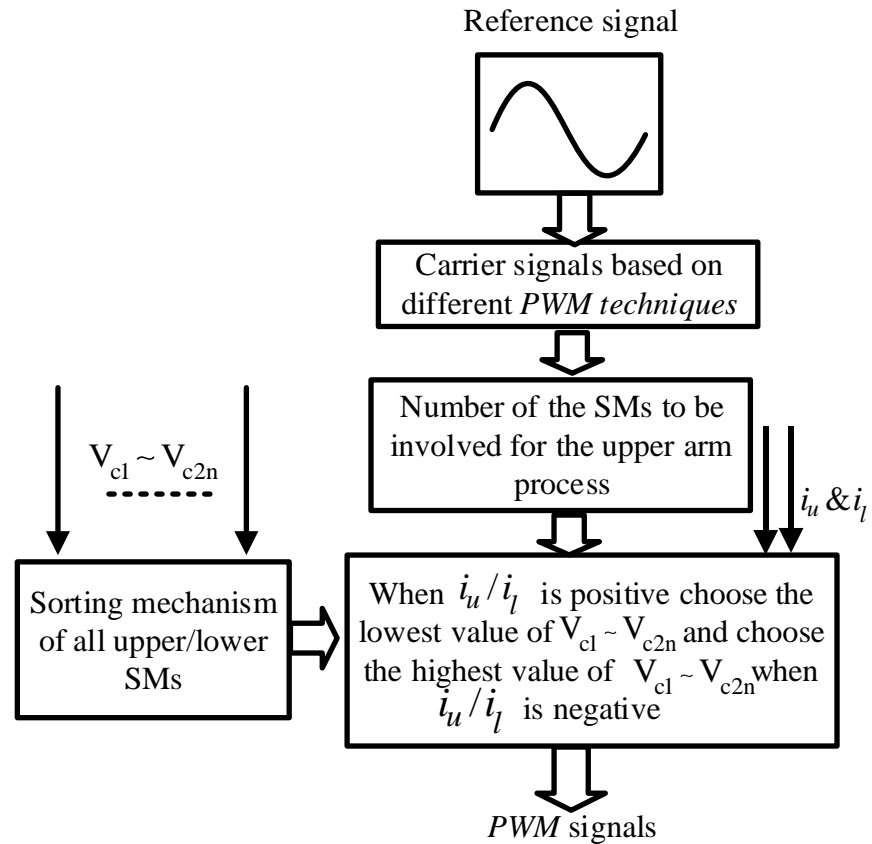
Fig 2.5. Block diagram of voltage-balancing control based on sorting algorithm scheme.

2.10 Control of SM Capacitor Voltage with Fewer Sensors

While most of the reported literature is sensor-based methods, however there have been few attempts to reduce the number of the voltage and current sensors. The following sub-sections classify the up-to-date proposed methods into four main groups.

2.10.1 Sorting Algorithm Methods with Fewer Current Sensors

Reducing the number of required current sensors has been recently considered by few researchers. For instance, in two recent studies [29] and [38], different methods

are introduced and demonstrated with both simulation and practical results. High frequency current components have been analyzed and controlled for the SM capacitors under different operating conditions [29]. Alternatively, the switching frequency of the semiconductor switch has been controlled and minimized [38]. The limitation of these methods is that only PS-PWM modulation technique can be used to control the converter. However, in comparison with the conventional sorting algorithm, arm currents are not required in achieving the voltage-balancing of the system.

In more recent study [23], another attempt to control SM voltage with fewer current sensors has been proposed, where a different modulation strategy was employed to the converter based on a dual space-vector pulse-width modulation (SVPWM) technique. In comparison with [29] and [38], the number of current sensor required for the MMC is one per phase, whilst the other two methods don't require any. Whereas, all methods including SVPWM-based technique are based on voltage sorting mechanism.

2.10.2 Observer-based Methods

Observer-based schemes are based on estimating capacitor voltages by monitoring only input and output signals, where usually the DC-link voltage and arm currents are required. Fig. 2.6 shows a general block diagram of the observer-based methods. Thus, to design such a sensorless control scheme, it is necessary to investigate the observability of the converter [39]. It has been reported that the MMC is observable when the switch at the targeted state is on [40]. In one recent study [40], the proposed observer is employed for the MMC as a fault detection scheme where the algorithm used is based on a sliding mode observer. The sliding mode observer has also been proposed for the CHC [41, 42]. Although it is known that the slide mode-based algorithm is robust against parameter uncertainty in the system equations, however, capacitance uncertainty in the SM has not been investigated neither in [40] nor in [42]. It is important to validate the converter with such deviations representing capacitance uncertainty, especially when the application requires high voltage levels. In another recent study, a KF-based observer has also been proposed for the MMC [43]. One important feature of the KF approach is the ability of the algorithm to cope with both

measurement and processing noise disturbances. However, capacitance deviation was not investigated in this study either.
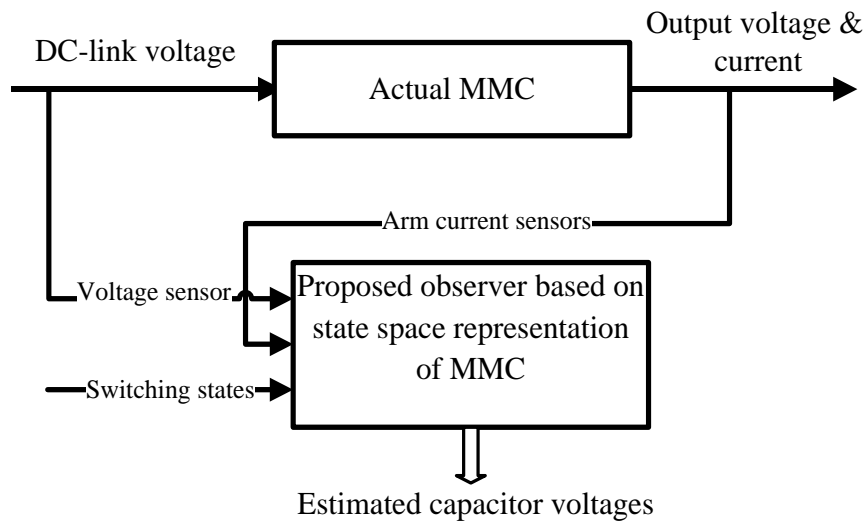
Fig 2.6. General block diagram of the observe-based method

An improvement to the latter research [40] involves the estimation of the capacitance value as well as the capacitor voltage of the SM capacitors was subsequently proposed in [44]. Although this improves the robustness of the system against capacitance uncertainty, however, the effect of the variation associated with the arm inductance value was not considered in the observer design. On the other hand, the authors in the same study [44] have proved that the converter can perform well with up to +10% of the nominal arm inductor value. However, it can be summarised that, none of the observer-based methods consider arm inductance variation in the design analysis.

2.10.3 Sorting Algorithm Methods with Fewer Voltage Sensors

In this group of methods and the observer-based methods have just mentioned above, a sorting algorithm is commonly used to control the voltages of SM capacitors. However, the technique presented here is based on measuring the total arm voltages rather than the DC-link voltage. On the other hand, similar to the observer-based methods, arm currents are also considered in the design.

A majority of the recent proposed methods [45-47], the estimation techniques used are based on prediction and correction stages. In the prediction stage, an initial estimation from the straightforward relationship (see equation (2.6)) between the capacitor current and voltage along with the capacitance value are used as follows:

$$\mathbf{V_{c1}}(t) = \frac{1}{C1} \int_{t_0}^{t} I(t) S_n(t) \, d(t) + \mathbf{V_{c1}}(t) \tag{2.6}$$

One critical issue with this step is the accumulated error caused by the integrator effect in equation (2.6). In [45], the error between the actual and the estimated arm voltages has been found to be divided equally between the number of inserted SM. This error is then used to correct each estimated voltage.

In more recent research [46, 47], the voltage-balancing of a seven-level MMC has been achieved with important reductions in the number of voltage sensors required, where the lowest number of voltage sensors needed are two when 7-level MMC is used. Two sensors contribute to measuring the total arm voltage of the converter. The increase in the number of arm voltage sensors required in these studies reduces the error in the individual SM capacitor estimation voltage. On the other hand, the main concern with these methods is that an advanced voltage-balancing method must be incorporated to guarantee stability. In addition, if the MMC level is higher than 7, more voltage sensors per arm are needed.

2.10.4 Open-loop Control Methods

Different attempts based on open-loop schemes have been suggested, where fixed PWM signals have been applied to the converter switches [48, 49]. Although these proposed schemes do not use any sensors, since they do not require any form of feedback control, the well-known limitations of open-loop control schemes may threaten the performance of the system with such control scheme.

2.11 Capacitance Estimation

As shown earlier in section 2.8, reliability in the MMC is considered as another important issue. Faults in any MMC components may cause serious problems. It is

known that the failure rates in power electronic components are usually caused by six main factors as illustrated by Fig. 2.7. It is well known also that the passive components, such as the electrolytic capacitor, will gradually deteriorate with time [50]. As a result, the performance of the capacitor decreases due to changes in its internal equivalent series resistance (ESR) [51]. It is therefore clear that passive components such as capacitors cause the highest number of potential failures, as reported from several surveys from various companies [52]. However, for the MMC, not many studies so far have investigated the capacitance estimation, and only two recent studies have dealt with this issue [44] [53]. For that reason, such issue should be further investigated as well. For example, the capacitance estimation has been used as a part of an observer-based method to estimate the SM capacitor voltage [44]. The estimation of SM capacitance is used to improve the performance of the proposed sensorless scheme. Whereas in another study [53], the RLS algorithm was proposed to estimate the SM capacitance of the converter.
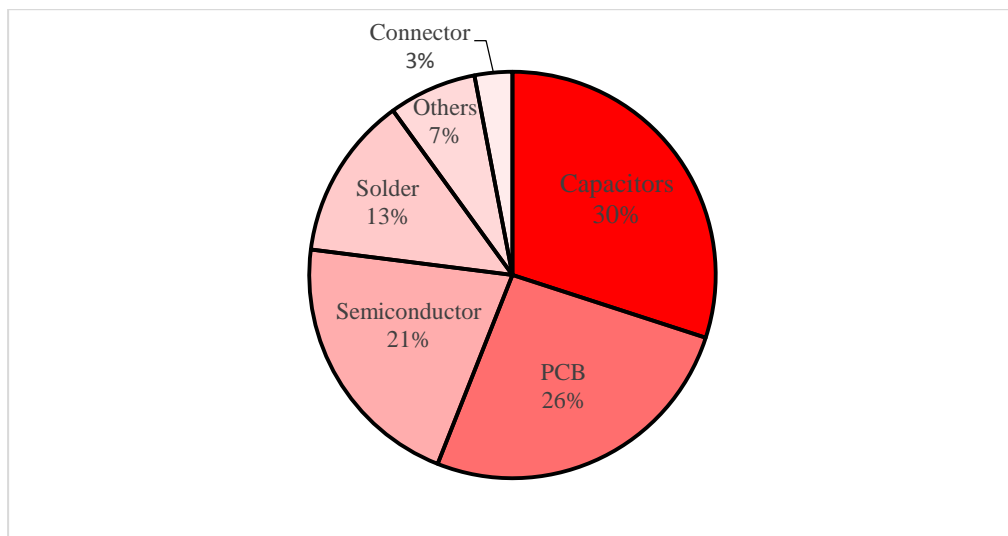
Fig. 2.7. Percentages of failure rates in power electronic devices.

2.12 MMC Applications

Multilevel converters have gained great attention in medium and high power applications due to their distinctive features, especially the modularity and the high quality of the output waveforms [5, 6]. Usually, these converters employ self-

commutated semiconductor switching devices such as IGBTs, IGCTs, etc. These self-commutated converters bring significant improvement to the utility in many aspects such as reactive power support, power factor correction, harmonic compensation and most importantly reduced filtering requirement [54].

Nowadays, multilevel converters are used in many different applications; for instance, pumps, gas turbine starters, reactive power compensation, submarine, compressors, fans, wind turbines, storage device conversion, mixers and high voltage direct current (HVDC) [55]. The following paragraphs mainly focus on the applications of MMCs, which in Fig. 2.8 are classified into three main application areas.

2.12.1 Energy Generation

Due to the high power involved in the conventional and renewable power generation, it is important to use a high quality of power conversion with high capability [56]. Whereas, and owing to the high demand for having clean power sources, such as photovoltaic generation, fuel cells and wind turbine, the numbers of distributed generations (DGs) have significantly increased. Therefore, more multilevel power converters would be needed in order to convert the energy from these sources for the network. The MMC, for example, has been suggested as a DC-DC converter to boost power before connecting the resource to the grid [57-62]. In some other studies, the MMC has also proven to work as a buck converter [57, 63]. Furthermore, the double star bridge cell (based on full-bridge) configuration is capable of tolerating a high range of voltage deviations in the DC-link voltage, due to its greater ability to buck and boost the DC-link voltage in both rectification and inversion sides. Therefore, the MMC with a full-bridge configuration is appropriate for renewable resources such as solar and wind power, where weather conditions always vary, which means that the DC-link input voltage will be affected.

2.12.2 Transmission, Supporting Network and Distribution Systems

Examples of the use of multilevel converters in transmission systems are the HVDC, the static synchronous compensator (STATCOM), active filters and flexible AC transmission systems (FACTS) [64].

One of the most promising applications based on the MMC is HVDC [15, 65-69]. For instance, double star chopper cell based on half-bridge configuration is suitable for HVDC and back-to-back systems [15]. A good and real example of employing MMC into the network is now allocated in a project called "Trans Bay Cable", the converter consists of 200 SMs per phase [70]. For transmitting 400 MVA rated power in that project, 600 SMs are required for each terminal converter.

It is well known that power supply companies have the responsibility to deliver a high power quality to the end terminal networks. In this final stage of delivering power to consumers, power electronic conversion plays a key role. Another promising application of MMC usage is the battery energy storage system (BESS) which can be connected to support a weak grid before delivering power to customers [15].

2.12.3 End-User and Stand Alone Usage Areas

Meanwhile, it is assumed to have a good power quality at this stage of delivering power to costumer; however, and regardless to power quality received, connecting any application including stand-alone to the grid, needs a suitable power electronic converter [71]. MMCs have also been proven to be suitable for different applications in this usage area. In [72] for example, the MMC has been employed for electrical vehicle where the traditional battery management system (BMS) of electric vehicles is replaced by the control of the MMC. The proposed topology integrates the BMS in the system, without the necessity for more balancing circuits. Another usage of MMC in medium power application has been proposed where an induction motor drive with two different configurations has been investigated [73]. Other promising applications based on drives is also been proven for the MMC [72-75].

Examples of the most promising application of the MMCs based on the area of usage are illustrated in the figure below:
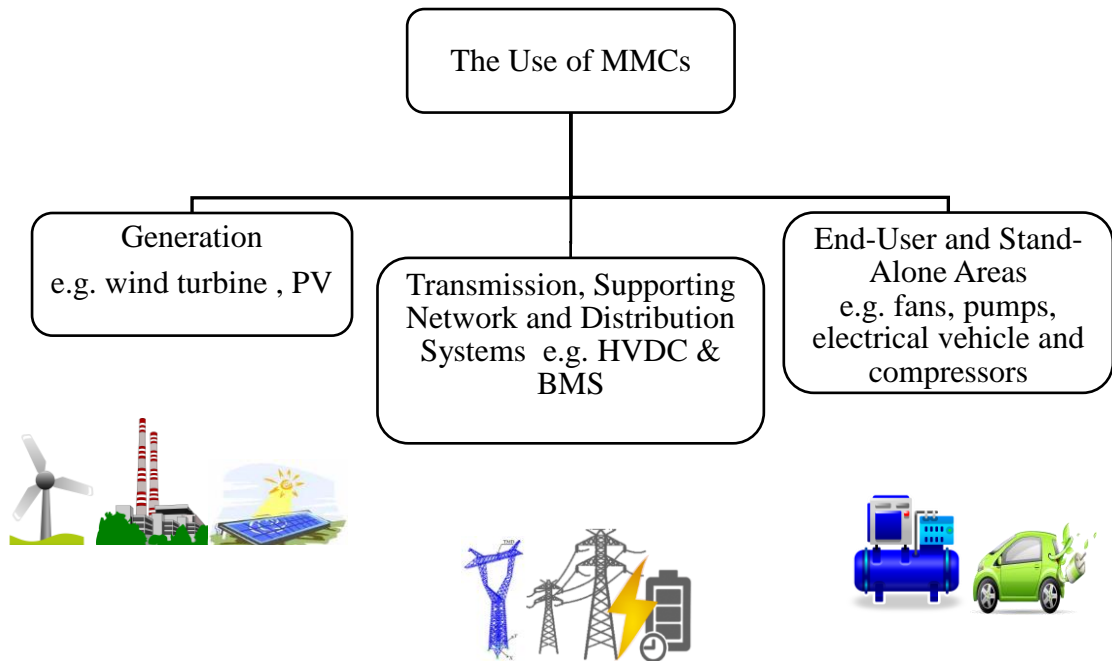
Fig 2.8. Classify MMC applications.

2.13 Chapter Summary

The importance of power conversion has been explained first in this chapter. Most common circuit topologies of multilevel converters with a focus on the MMC circuit configuration and principles of operation, have been demonstrated. Mathematical representations of converter's voltage and currents have also been stated.

In addition, Chapter 2 has described the most commonly used voltage-balancing control methods. A classification of these control methods has also been provided as well as the PWM techniques used. The speed of switching frequency used in the most well-known existing control methods was also considered. The focus in this classification was based on achieving voltage-balancing with fewer sensors, where four different groups of methods have been reviewed. In addition, as another challenge facing MMCs, the capacitance estimation of the converter's SMs has been briefly reviewed.

The chapter has also provided and classified the most attractive applications for MMCs. The advantages and challenges associated with MMCs among other conventional multilevel converters have also been presented.

Next chapter focuses on the experimental set-up system. In addition to the implementation requirement, it also describes most of the selected components in the converter.

CHAPTER 3

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THE EXPERIMENTAL SET-UP SYSTEM

....

3.1 Introduction

To practically evaluate and validate the proposed schemes in this thesis, an implementation in real time is required. A test rig has been developed specifically for this project. However some potential future works have also been considered in the design. Compared to the simulation studies, a scaled-down system is used here; however, the circuit was initially designed for 800W operation. This mainly involves a single-phase 4-level MMC with a dynamic load, DC power supply, number of voltage and current sensors, interphase circuits, dual gate drives and control board. A general block diagram of the whole experimental set-up system is illustrated in Fig. 3.1. Some of these components mentioned above are described in more details in the following sections.

3.2 The 4-Level Single-Phase MMC and R-L Load

Three SMs and two inductors (L_s) per arm are used in the design. An IRF530N power MOSFET is used to construct the converter's SMs. More information about the MOSFET used in this project is detailed in the datasheet. The half-bridge SM capacitor

used as demonstrated in Fig. 3.2 is the VISHAY 56 1000μF 63 V DC with ± 20% tolerance.
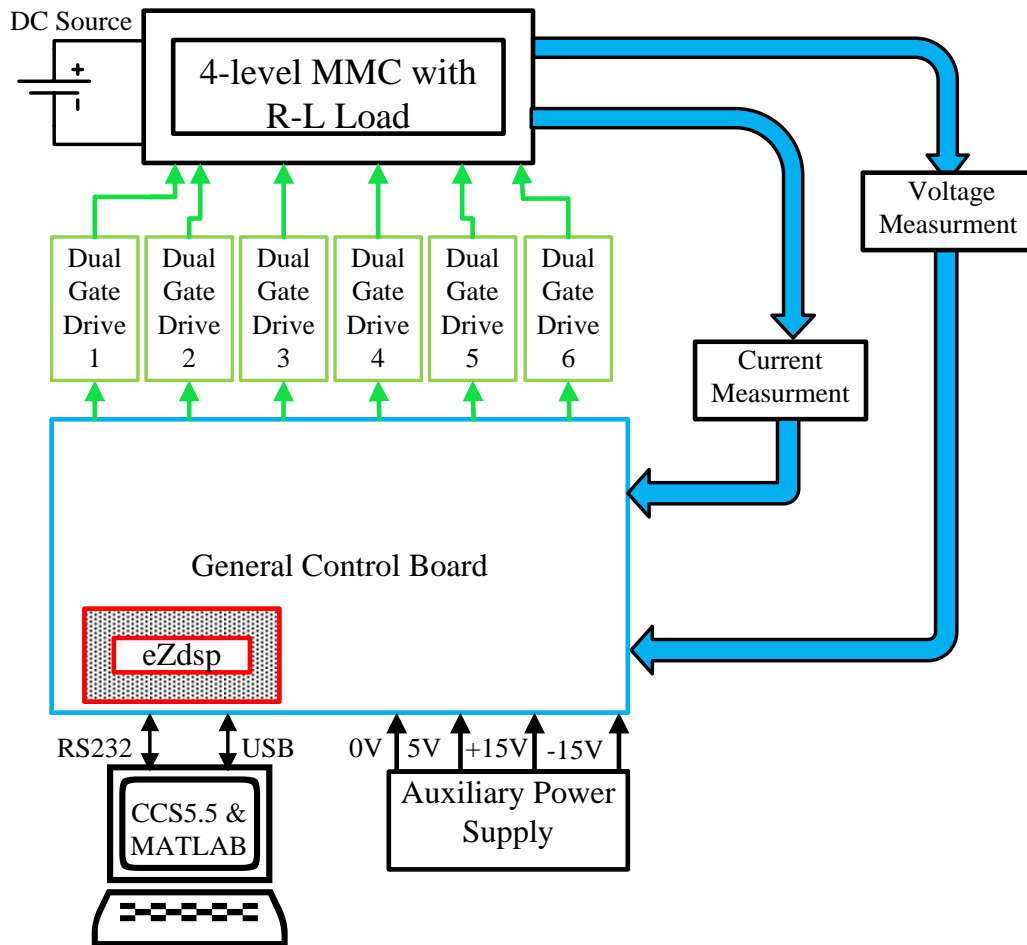
Fig 3.1. Block diagram of the experimental set-up.
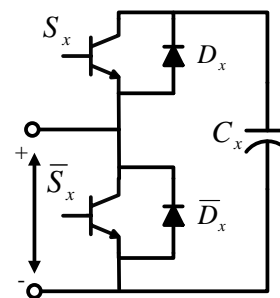
(a)   (b)

Fig 3.2. Half-bridge SM configuration. (a) A photograph of the SM. (b) Schematic diagram of the SM.

A dynamic load is attached to the converter to test the performance of the proposed methods during different load conditions. As shown in Fig. 3.3, two parallel resistors (R_1 and R_2) and a tapped inductor are connected to the output of the converter. Two cases are considered in most studies:

- In the normal operation (case one), R_1 is connected in series with the load inductor (L) where $R_1 = 33\ \Omega$ and $L = 4$ mH while R_2 (68 Ω) is disconnected.

- In case two, two actions have been considered in order to further validate the proposed methods against step changes in the load. Firstly, a sudden change from R_1 to R_2 is applied whilst L is still connected in series. The load current (i_{load}) is decreased by around 100%. Secondly, another sudden change from R_2 to R_1 is applied where the current is approximately doubled to reach its original value. A manual two-way switch is used to alternate between R_1 and R_2 as shown in Fig. 3.3.
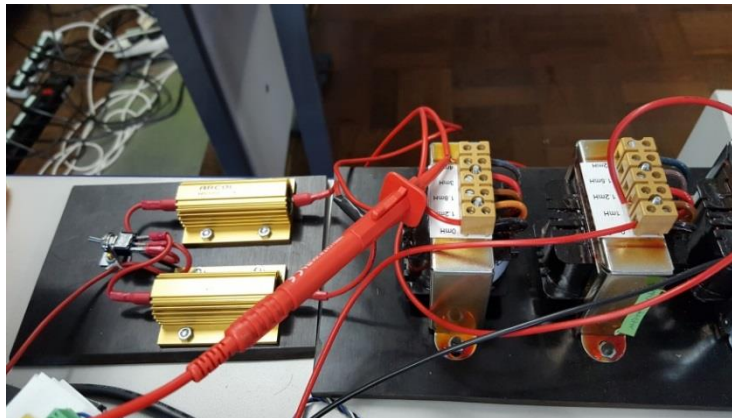
(a)
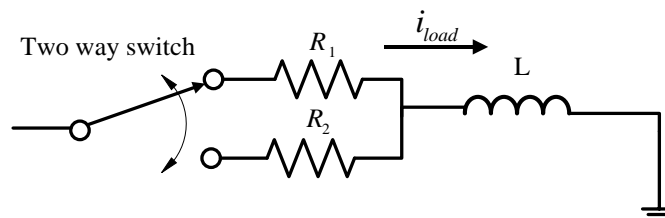
(b)

Fig 3.3. Dynamic R-L load configuration. (a) Photograph of the experimental load. (b) Schematic diagram of the load.

3.3 Microprocessor Control System

To control the 4-level single-phase MMC described earlier, a TMS320F28335 floating point microcontroller is used. The TMS320F28335 is a member of the Texas Instruments C2000 family. In comparison to the fixed point microcontroller from the same supplier (Texas Instruments), the TMS320F28335-based floating point microcontroller offers about 50 percent more in the overall performance [76].

In order to implement and evaluate the proposed estimation schemes and the voltage-balancing algorithm using the TMS320F28335 microcontroller, Code Composer Studio (CCS5.5) development tools from Texas Instruments is used on the host ControlDesk (laptop) to generate the C-code. This was achieved with the help of the MATLAB/Simulink package, where the Simulink Embedded Target Support Package (TSP) and Real-Time Workshop Embedded Coder (RT-WEC) are employed. These tools provide a number of useful features, such as a quick and easy way to generate C-code, and the implementation and evaluation of proposed control schemes in a real-time environment. An External MATLAB mode is also used, where the data inside the DSP can be accessed in real-time processing. This feature (i.e. External MATLAB mode) provides the ability to tune some adjustable parameters in the developed algorithms when the converter is processing in real-time. However, for most of the proposed methods, off-line tuning was achieved first, and consequently the real-time tuning is then accomplished. This technique helps in avoiding the use of any inappropriate parameter values which might damage the circuit.

The execution time of the proposed voltage estimation methods was approximately 34μs, this may lead to the use of a faster and more powerful processor when higher output voltage levels are needed especially for three phase applications. However, for the investigated current sensorless schemes, the execution time was low for all investigated schemes. It should also be noted that most of the MMCs applications are three phase based systems. In other words, microprocessors with parallel processing capabilities must be used for such applications (i.e. three phase with high output voltage levels) to guarantee an appropriate processing time. This condition is only for the proposed voltage sensorless schemes. Nevertheless, FPGA boards for example are

a very attractive and cost-effective alternative parallel processing which may reduce computation time by processing independent calculation concurrently.

3.4 Hardware Implementation and Microprocessor Setting

The converter is fed with an EX354RT TRIPLE 300W power supply, where the input DC volt is 60V for most of the experimental tests. A photograph of the whole experimental test bench system is illustrated in Fig. 3.4. Other details of the hardware implementation system, including converter parameters, are summarized in table 3.1.

Eleven analogue input signals from the test rig are processed inside the controller; three of which are current signals and eight voltage signals. The sampling frequency ($f_{sampling}$) which was used for all experimental tests are $f_{sampling} = 20\text{kH}$. Three CAS-15 current sensors are used to monitor the upper and lower arm and output currents
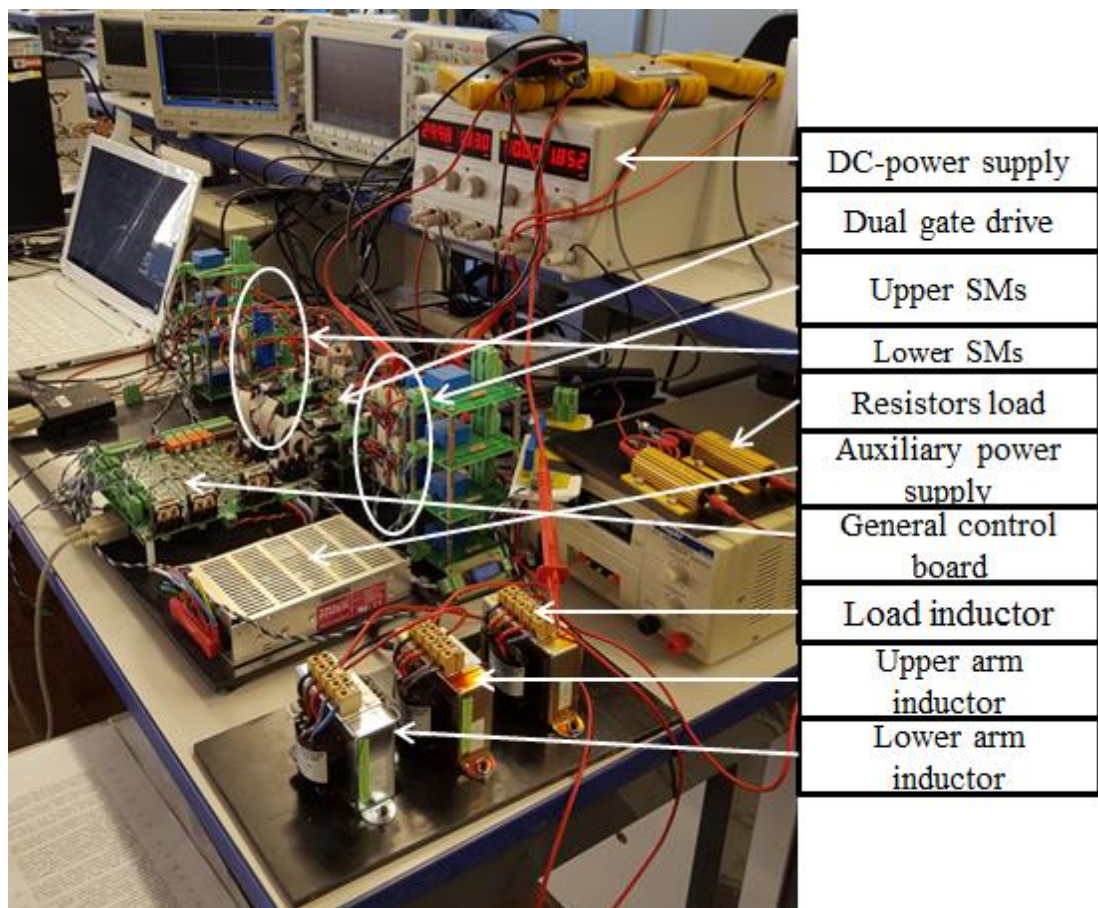
Fig 3.4. Photograph of the experimental test bench.

of the converter, while six LV25-P voltage sensors are used to monitor the SM voltages in order to evaluate the estimated voltages against their measured values. Although the three current sensors are not used for some sensorless current methods; these sensors are still required for the evaluation and comparison investigation with sensor-based current method. Another two voltage sensors are also used to measure the upper and lower arm voltages. These two voltage sensors (AD215AY isolation amplifier) are necessary for the proposed voltage estimation methods to estimate the six SM voltages of the converter.

The CAS-15 sensors require a +5V supply whilst the LV25-P voltage sensors require ± 15V supplies (see Fig. 3.1). Owing to the limited range of the analogy to digital converter (ADC) input channels of the controller, extra interphase circuits (e.g. voltage divider circuit) are implemented to the general control board to be compatible with the limited 0-3V range of the ADC input channels. The built-in ADCs sample the input current and voltage signals. The sampled data is then executed according to the software control algorithms.

Table 3.1. Experimental Parameters

Parameter	Value
SM capacitor (C)	1000 μF
Modulation index (m_i)	0.9
DC-link voltage (V_{dc})	60V
Output frequency (f)	50 Hz
Carrier frequency (f_c)	2.5 kHz
Number of SM per leg (N)	6
Load resistor (R)	33 Ω
Arm inductor (L_S)	1 mH
Load inductor (L)	4 mH
Sampling frequency ($f_{sampling}$)	20 kHz
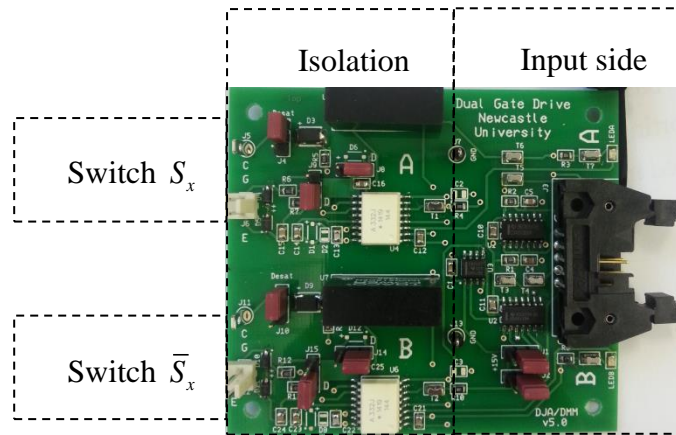
Fig 3.5. Dual gate drive.

The output of the controller provides the *PWM* signals for the 4-level MMC. Due to the feature associated with the TMS320F28335, where the processor can generate 6 dual *PWM* signals, 6 dual gate drive boards are used for the converter (see Fig. 3.5). The design of these boards is beyond the scope of the present research. Each *PWM* signal within the same couple (i.e. PWM_x and $\overline{PWM}_x$) is generated so as to be complementary to the other. All of these signals are switched at the switching frequency obtained for the voltage-balancing algorithm where the reference carrier signals are 2.5 kHz. The dead-time between PWM_x and $\overline{PWM}_x$ is set at 3μs. The *PWM* signals generated are then passed through the input side of the dual gate drive, as shown in Fig 3.5. Random samples of the switching signals after balancing voltages across C_1, C_2 and C_3 for the three upper arm switches (PWM_1, PWM_2 and PWM_3) are shown in Fig. 3.6. The converter is then controlled with such signals.
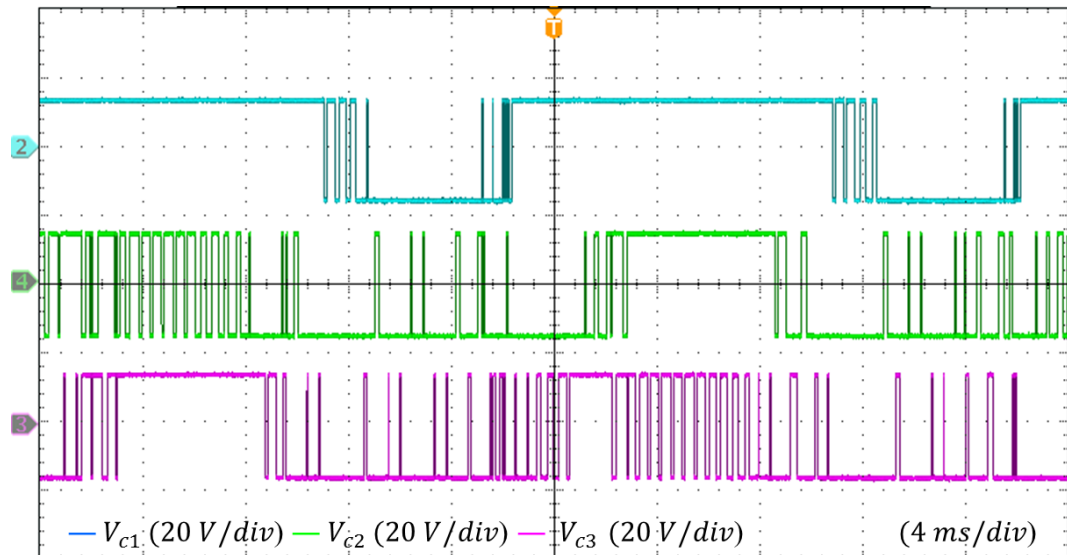
Fig 3.6. Sample of the three upper arm switches (PWM_1, PWM_2 and PWM_3).

3.5 Chapter Summary

This chapter has focused on the experimental set-up system used to verify the effectiveness of the developed schemes based on a 4-level MMC controlled by a TMS320F28335 floating point microcontroller. The main hardware components in addition to software configurations involved in the system have also been described. The main procedure behind the hardware implementation in real-time processing has been introduced; and this configuration set-up is followed in the subsequent chapters (Chapter 4-6).

CHAPTER 4

....

PROPOSED CURRENT

SENSORLESS METHODS

....

4.1 Introduction

The experimental set-up described in the last chapter is used here to validate the proposed current sensorless methods in this chapter. Different schemes of modified conventional sorting algorithm with lower complexity are proposed in order to balance the voltages of SM capacitors for the MMC. Two different procedures are investigated in this chapter. In comparison with conventional sensor-based methods, the main idea here is to achieve voltage-balancing within the MMC arms with fewer current sensors.

In comparison with recent studies [29] [38] of reducing current sensor numbers, the proposed methods in this chapter can be used with both level shifted (LS)-PWM and phase shifted (PS)-PWM. The two different proposed methods are examined under different operating conditions; for instance, with a sudden change in the DC source or when different load values are applied. The advantage of such sensorless control methods is to simplify hardware communication in general. Moreover, the reliability

of the MMC is also improved. Simulations and practical analyses of a single-phase MMC are conducted to show the effectiveness of the proposed methods.

4.2 Conventional method (sensor-based method)

The idea behind the conventional method is to control the converter voltages by sorting all SM voltages in descending / ascending order [30,31]. For example, if the upper arm is considered, the lowest capacitors' voltages will be charged when the upper current is positive and their value will be increased. On the other hand, when the upper current is negative, the capacitors with the highest value will be discharged. The algorithm also defines how many capacitors should be involved in the process. In other words, for each output voltage level, there is a required number of capacitors that need to be charged or discharged, and this number is defined by the intersection of the fundamental sine wave signal and the carrier signals used [30,31]. For the lower arm, the charging or discharging actions of the converter depend on the direction of the lower arm current rather than that of the upper arm current. Similarly, the lowest capacitors will be charged when the lower current is positive and their value increases. The main difference between the conventional and the proposed sensorless methods is the method used to make decisions regarding charging and discharging.

4.3 Load Current Monitoring Method

Compared with the conventional sorting algorithm method [30], only one sensor per leg is required to monitor the load current in this method. The proposed voltage-balancing method is based on several steps, where a sine wave reference signal is compared first with carrier waveforms. These carriers are generated either from a LS-PWM or a PS-PWM strategy. Fig. 4.1 illustrated these two groups in (a-c) and (d) and (e) respectively.
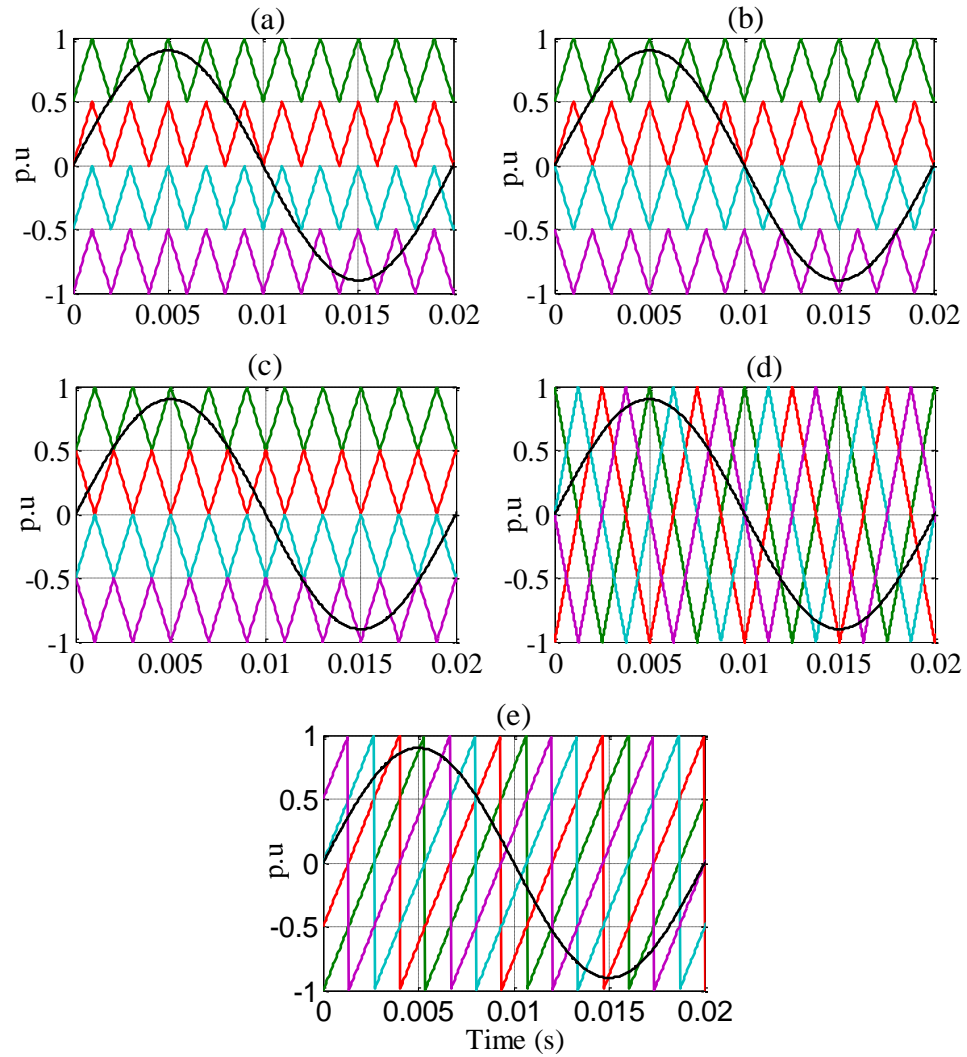
Fig 4.1. LS-PWM and PS-PWM techniques.

In LS-PWM three different techniques can be used: phase disposition (PD)-PWM, opposition disposition (POD)-PWM and alternative phase opposition disposition (APOD)-PWM. The number of carrier signals required for an N-level MMC is r where $r = N$-1. For the PD-PWM technique, r carrier signals with the same phase shift are used; however, they are different in magnitude as can be seen in Fig. 4.1(a). For the POD-PWM technique, there is a 180° phase shift between the positive and negative carriers as shown in Fig. 4.1 (b), while in APOD-PWM the carrier signals in each of two subsequent levels are shifted by 180° (Fig. 4 (c)).

Meanwhile, PS-PWM can also be used for the proposed methods. Two common techniques are used: PS-PWM and saw tooth (ST)-PWM. In comparison with LS-

PWM techniques, the applied carrier signals have the same amplitude; however, they are shifted horizontally by angle α as shown in Fig. 4.1(d) and (e). For an N-level MMC, the angle α is defined by [16]:

$$\alpha = \frac{360}{N-1}$$ 4.1)

Although all aforementioned PWM techniques can be used; however, and for simplicity only, PD-PWM is used in the simulation and experimental analyses here.

In the second step of implementing the algorithm, the number of SMs to be involved (β) are defined for the upper and lower algorithms.

For ease of demonstration, assume that the PD-PWM is used for a four-level MMC only as shown in Fig. 4.2 and Fig. 4.3. Therefore, the number of SMs required for each level can be determined as follows:

- For level one, the number of the involved SMs for the upper arm, which is activated and deactivated by switches $S_1 - S_3$, is 3. In the same instantaneous time, the number required for the lower arm is 0. The total should be always 3 for the whole period of this level (i.e. $\beta_{upper} + \beta_{lower}$=3).

- For level two, the number of the involved SMs for the upper arm, which is activated and deactivated by switches $S_1 - S_3$ is 2 (β_{upper}= 2). In the same instantaneous time, the lower number required for the arm is 1 (β_{lower}=1).

- For level three, the number of the SMs involved for the upper arm, which is activated and deactivated by switches $S_1 - S_3$ is 1. In the same time, the lower arm required number is 2.

- For level four, the number of the involved SMs for the upper arm which is activated and deactivated by switches $S_1 - S_3$, is 0. In the same time, the number required for the lower arm for β_{lower} is 3.

For all levels, the number of the SMs required for lower and upper arm should be 3 (i.e. $\beta_{upper} + \beta_{lower} = 3$)

In parallel with the number of SM required as just described, a sorting mechanism is also involved in the algorithms. In this step, for each measurement period,   arm voltages are sorted in ascending and descending order.

(a)
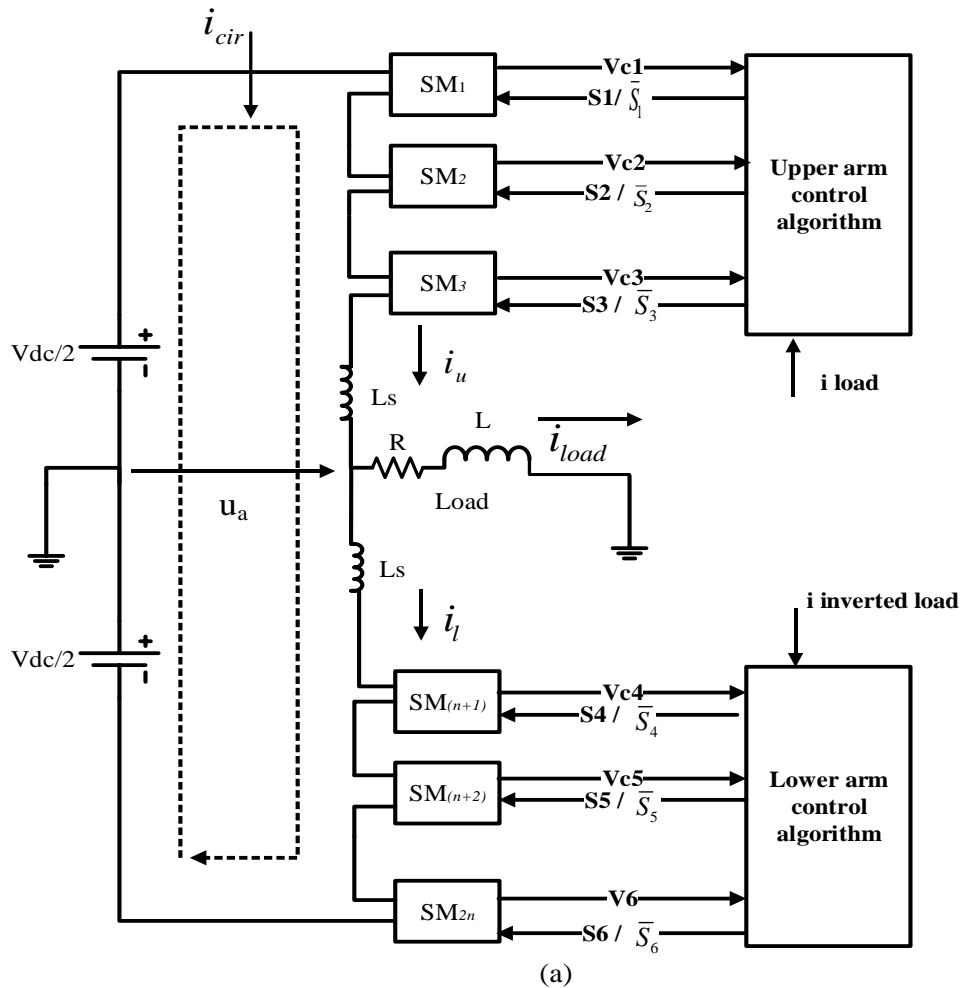
Fig 4.2 General block diagram of the implementation of the load current monitoring method on a 4-level MMC.
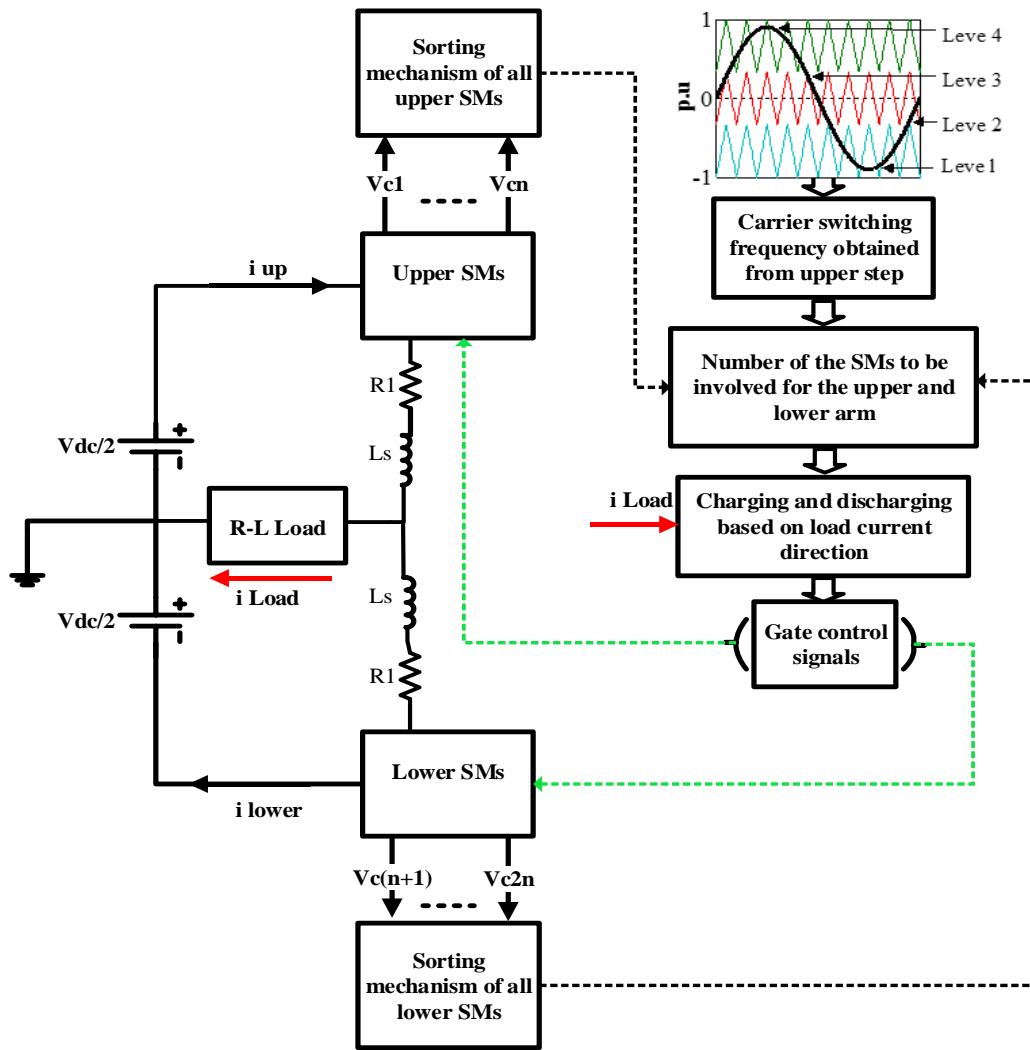
Fig 4.3. Load current monitoring method for *N*-level MMC level.

In the third step, as can be seen from Figs. 4.2 and 4.3, the charging and discharging of the SM capacitors relies on the direction of the load current. If the load current is positive, the upper targeted SM capacitors which have the lowest value will be charged. On the other hand, when the load current is negative, the targeted SM capacitors (i.e. the capacitors with the highest values) will be discharged. In both cases S_1 must be on and $\bar{S}_1$ must be off. Identifying the required SM capacitor to be charged or discharged is based on the sorting mechanism as shown in Fig 4.3.

For the lower arm, the same principle applies; however, an inverted load current ($i_{inv\text{-}Load}$) is inserted into the algorithm which satisfies the following formula:

$$i_{load} + i_{inverted\ load} = 0 \qquad\qquad (4.2)$$

Therefore, the switching signals obtained will be distributed between the upper and lower arms and therefore control the converter.

4.4 Sensor-never Current Monitoring Method

Fig 4.4 illustrates the proposed method. Similar to the conventional methods which have been briefly described earlier for the control of SM capacitor voltages with voltage and current sensors, a sine wave reference signal (sin2πft) is also used here. The method proposed here is similar to the load current monitoring method where same numbers of carrier signals and of SMs to be involved are also applied to the algorithm. The sorting mechanism for all converter SM voltages is similar. However, the charging and discharging of the converter capacitors are based on the sin2πft direction and not the arm current directions.
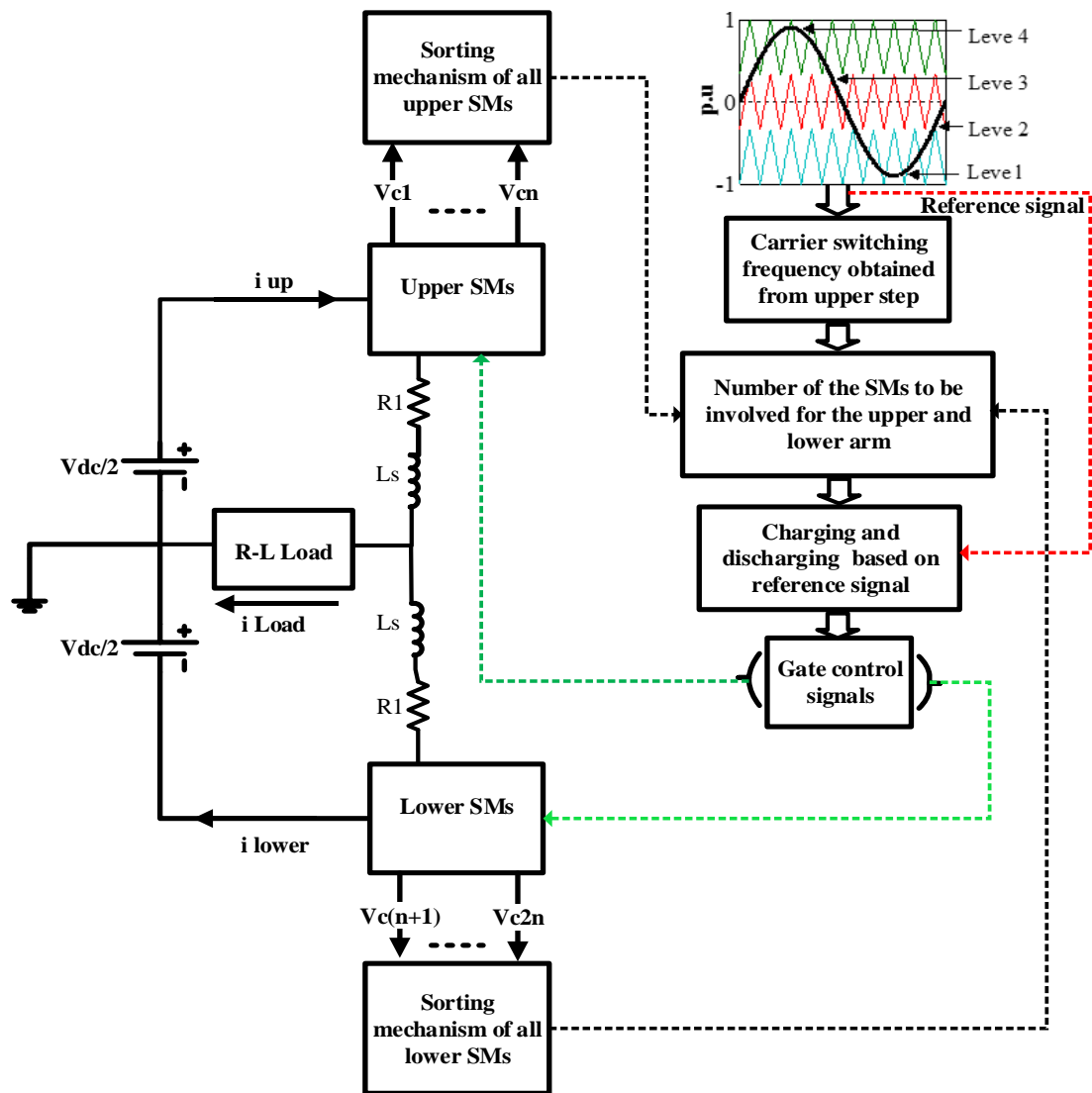
Fig 4.4 Sensor-never current monitoring method for *N*-level MMC

For the upper arm SMs, as in the load current monitoring method, the lowest capacitors will be charged and the highest capacitors will be discharged, but the reference signal ($\sin 2\pi ft$) rather than the load current direction will make the decision concerning the status charging or discharging of the capacitor. To control the lower arm capacitors, the reference signal is shifted by $\pm\pi$ to the lower half of the converter.

In the case of HVDC systems, for example, or any closed-loop control application where the MMC is connected to the grid, the control signal of the closed loop controller can be used for the algorithm. In other words, the decision about which capacitor is

being charged or discharged will depend on the direction of the controlled control signal rather than the sinewave reference signal.

An example is given in table 4.1 to show the importance of the reduction in sensor numbers that the proposed methods can achieve in comparison with conventional sensor-based schemes.

Table 4.1 Comparison of the number of current sensors required for the MMC.

Methods	Application	Number of sensors
Conventional methods	HVDC	12
	Motor drive	6
Load current monitoring method	HVDC	6
	Motor drives	3
Sensor-never current monitoring method	HVDC	Zero
	Motor drives	Zero

4.5 Increasing the Output Level of the Converter

Due the ability of the proposed methods to achieve voltage-balancing with LS-PWM techniques, increasing the output level of the converter is possible. The $2N+1$ level can be achieved by using an interleaving modulation technique [77]. Fig. 4.5 illustrates the interleaving modulation technique for a 5-level MMC where the PD-PWM method is used. As can be noted from the figure, the four carrier signals of the lower arm are shifted by 180 degrees with respect to the upper arm carrier signals. Applying this technique will increase the MMC output level from $N+1$ to $2N+1$. Results and discussion are provided in the next sections.
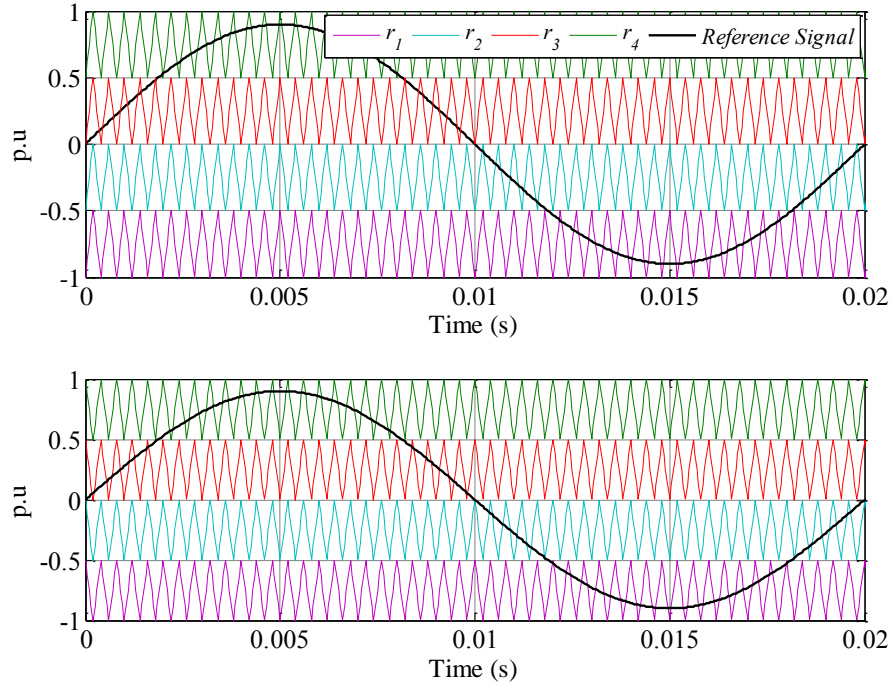
Fig 4.5 Interleaving modulation technique based on PD-PWM Scheme.

4.6 Simulation Results

The results achieved here are divided into two different MMC levels. Firstly, the 4-level MMC is simulated to investigate the two proposed current sensorless methods, and different operating conditions are examined in this part of the results. The second part of the simulated results focuses on the interleaving modulation technique where a 5-level MMC is used. The reason for two different levels being used is because the experimental set-up system is designed on a 4-level MMC only, whilst the interleaving scheme does appear better with an odd number of levels, such as 5, 7 and 9-levels. Therefore, an extension in the converter levels is applied to further investigate the increasing output voltage level of the converter. The parameters of the converter are explained in the following sub-sections.

4.6.1 Output Results of the Converter with Load Current Monitoring Method, Sensor-Never Current Monitoring Method and Conventional Method.

The single-phase 4-level MMC is simulated where the converter is fed with 480 DC V, 3 SMs are used for the upper arm and the same number for the lower arm, each of

which has an arm inductor of 1 mH and three 2 mF capacitors. The SMs are switched at a carrier switching frequency of 2.5 kHz. The same operating conditions and parameters are applied to all methods. In addition, similar tests are examined here; however, the idea is to evaluate and validate the proposed methods with exactly the same conditions so that a comparison between the proposed current sensorless schemes can be made.

4.6.1.1 Steady-State Operating Condition

In this test, the converter is assumed to work on a constant R-L load with values of R=33 Ω and L= 10 mH. The output current and voltage waveforms are shown in Figs. 4.6-4.8. In all figures the voltage across C_1 is also shown in Fig 4.6 (c), Fig. 4.7 (c) and Fig. 4.8 (c). The reference voltage signal is evaluated at a fundamental frequency of 50 Hz. The response of the converter under normal operating conditions is very similar for the proposed and conventional methods, and it is hard to observe any differences between figures.

It should be noted that the output currents in all methods have some noise; however, this is mainly because of the low output voltage level used (i.e. 4-level only) and low arm inductance value (L_s =1 mH).
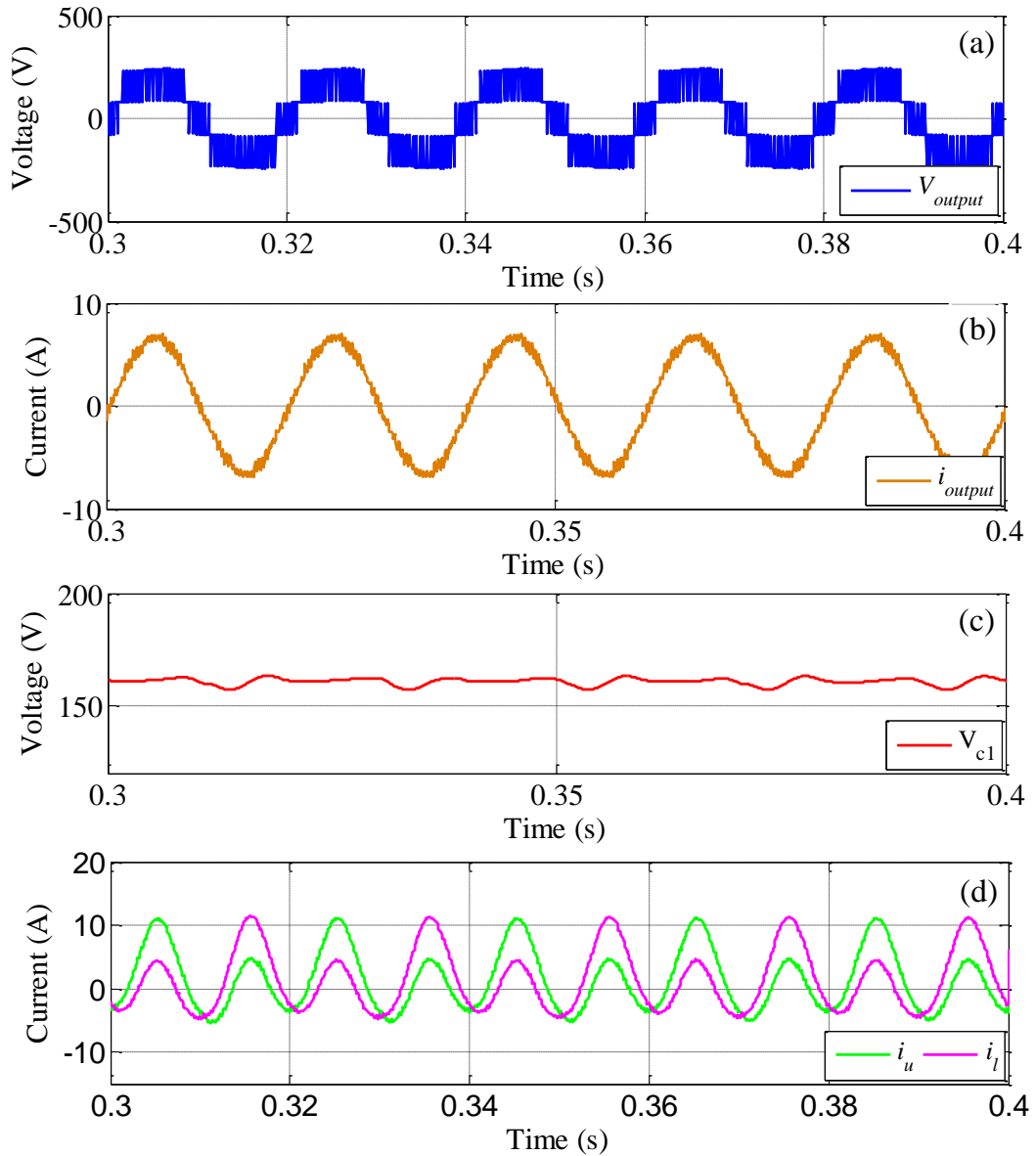
Fig 4.6 Simulation results of the output waveforms of the proposed load current monitoring method. (a) Output load voltage. (b) Output load current (c) Voltage across C1. (d) Upper and lower arm currents.
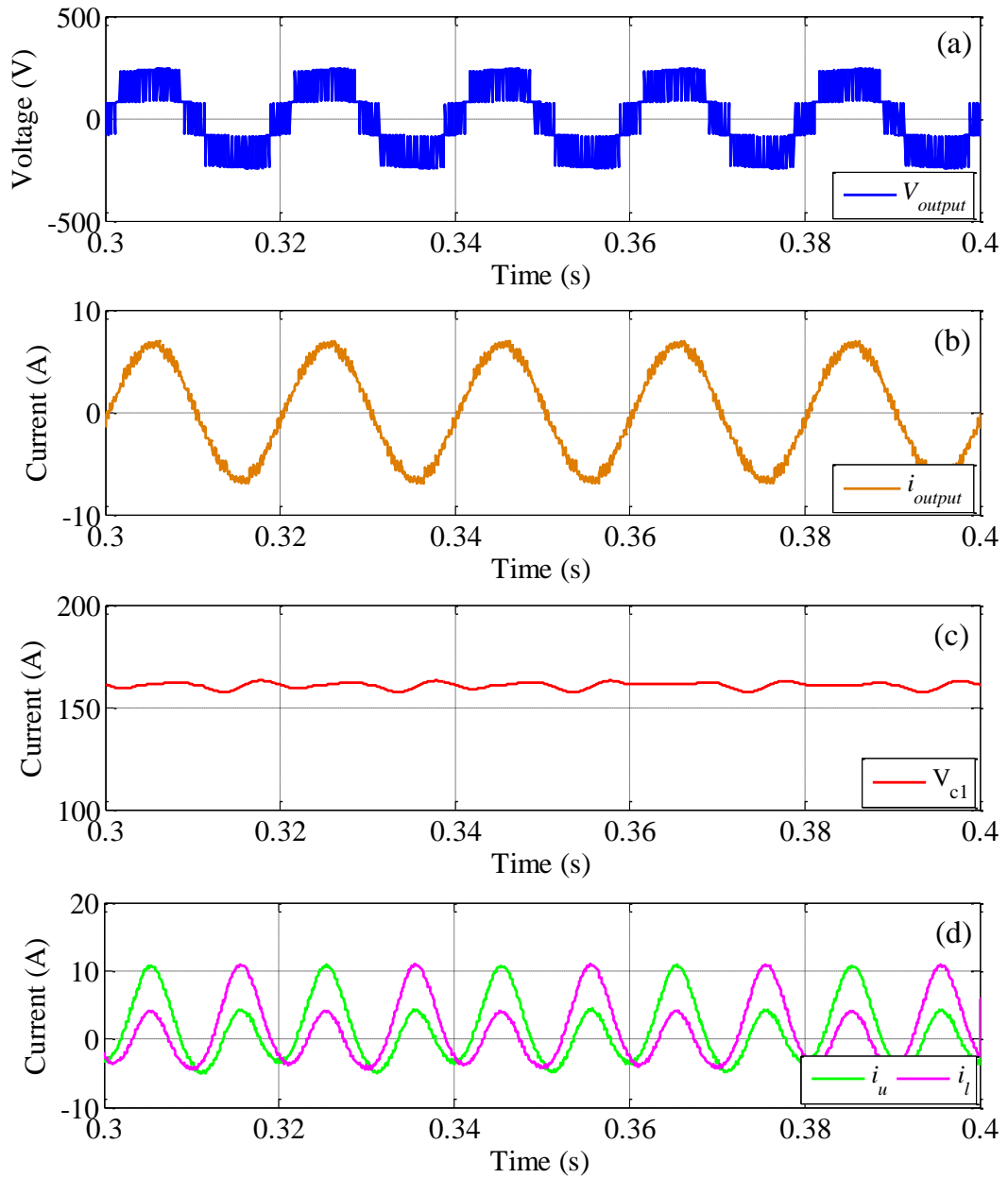
Fig 4.7 Simulation results of the output waveforms of the proposed sensor-never current monitoring method. (a) Output load voltage. (b) Output load current (c) Voltage across C1. (d) Upper and lower arm currents.
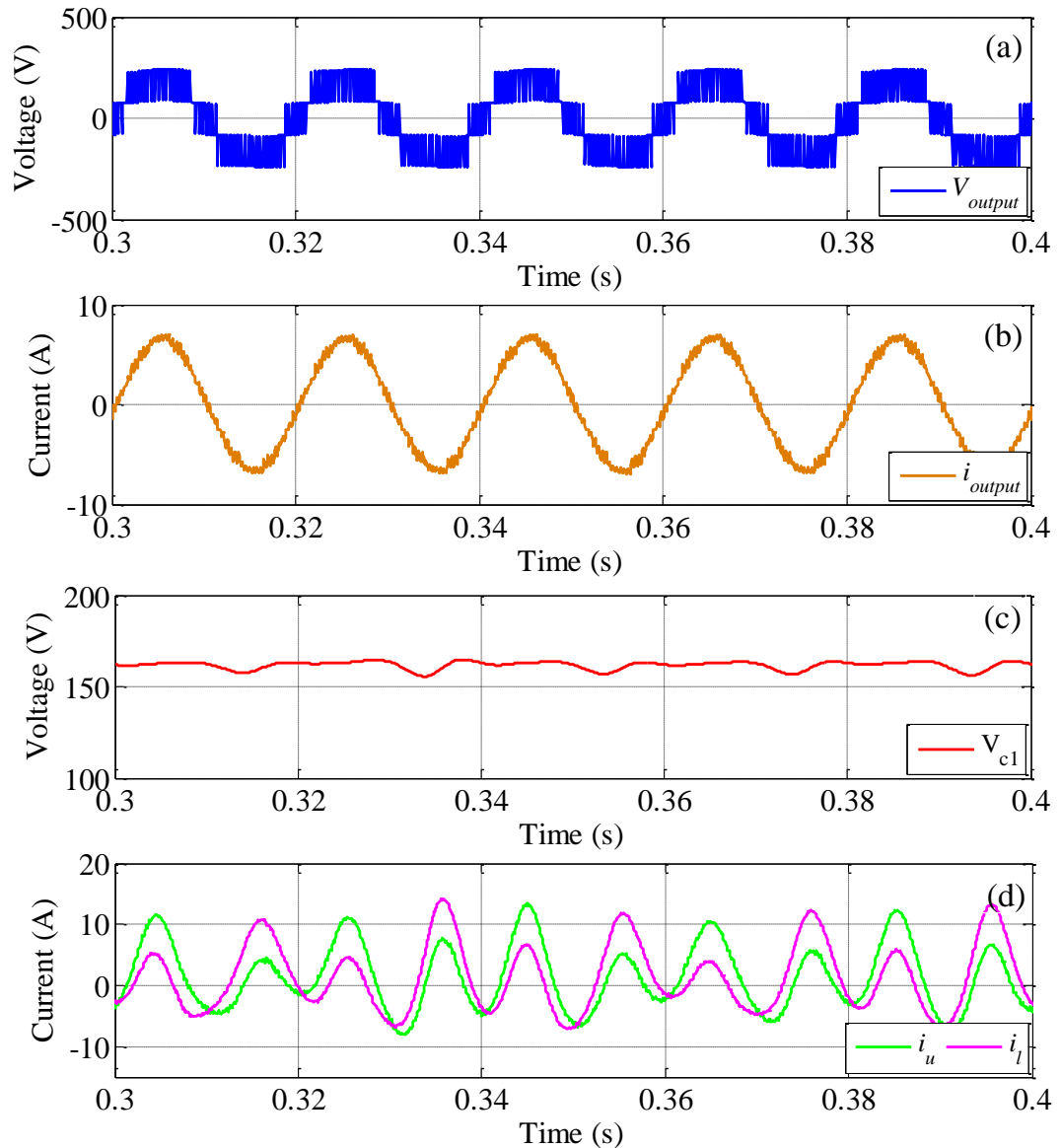
Fig 4.8 Simulation results of the output waveforms of the conventional method. (a) Output load voltage. (b) Output load current (c) Voltage across C1. (d) Upper and lower arm currents

4.6.1.2 Performance of the Proposed Methods during a Step Change in the DC Source

Fig. 4.9 investigates the performance of the first proposed method in terms of the converter output signals where a sudden change in the DC-source is applied at 0.4s. The DC-source is increased by 50% from 480V to 720V. Fig 4.9 (b) shows the effect of this change on the voltage at C_1. In these selected results the arm capacitors are

assumed to be pre-charged (i.e. the initial value of all capacitors are $\frac{V_{dc}}{n}$). It can be noted that the proposed method successfully tracks the reference value, and it takes only around 0.2s to reach the second reference value of 240V. Both output voltage and current reach stability after 0.2s as well.

In comparison with the results of the previous method shown in Fig.4.9 and the present results in Fig. 4.10, both tests also show similar output waveform responses in terms of settling time, output load current and voltage. On the other hand, the only difference which can be observed is in the shape of the voltage across SM1. Similar to the results for the conventional method presented in Fig. 11, the output waveforms are close to those obtained from the proposed sensorless methods. However, the voltage across SM1 shows rather more oscillation, while the average value of Vc1 in Fig. 11 (c) is closer to the reference value (240V).
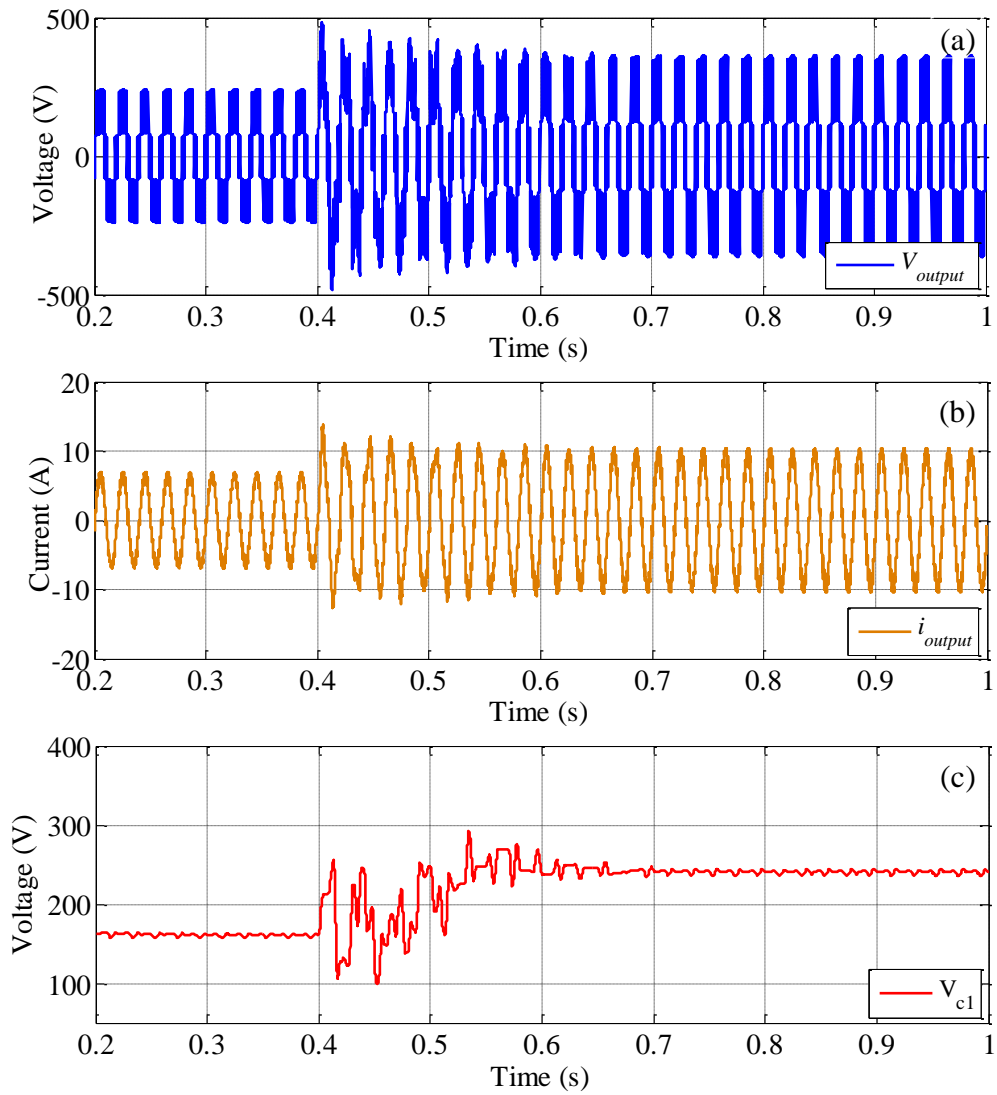
Fig 4.9 Simulation results of the effect of DC step change on the converter waveforms under load current monitoring scheme. (a) Output load voltage. (b) Output load current (c) Voltage across C1.
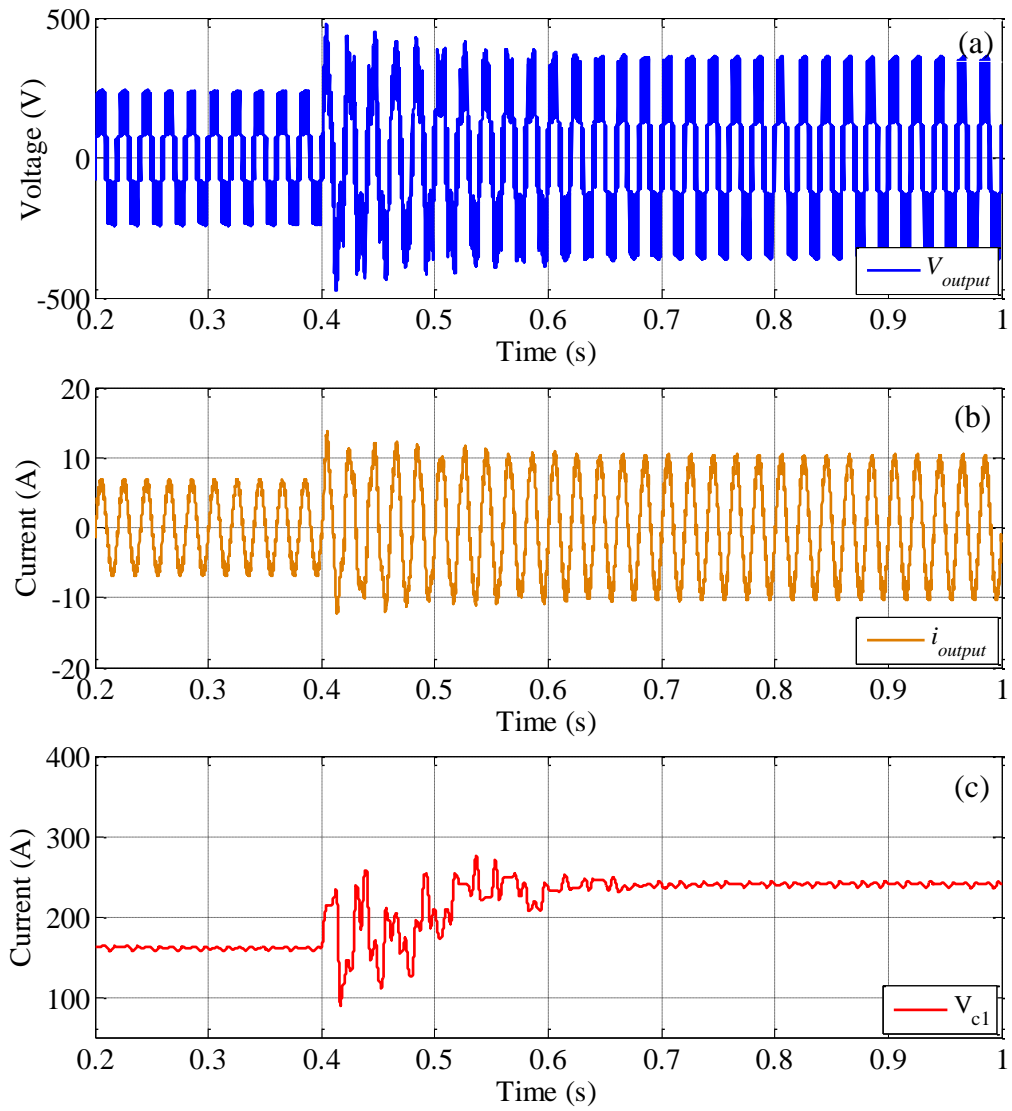
Fig 4.10. Simulation results of the effect of DC step change on the converter waveforms under sensor-never monitoring scheme. (a) Output load voltage. (b) Output load current (c) Voltage across C1.
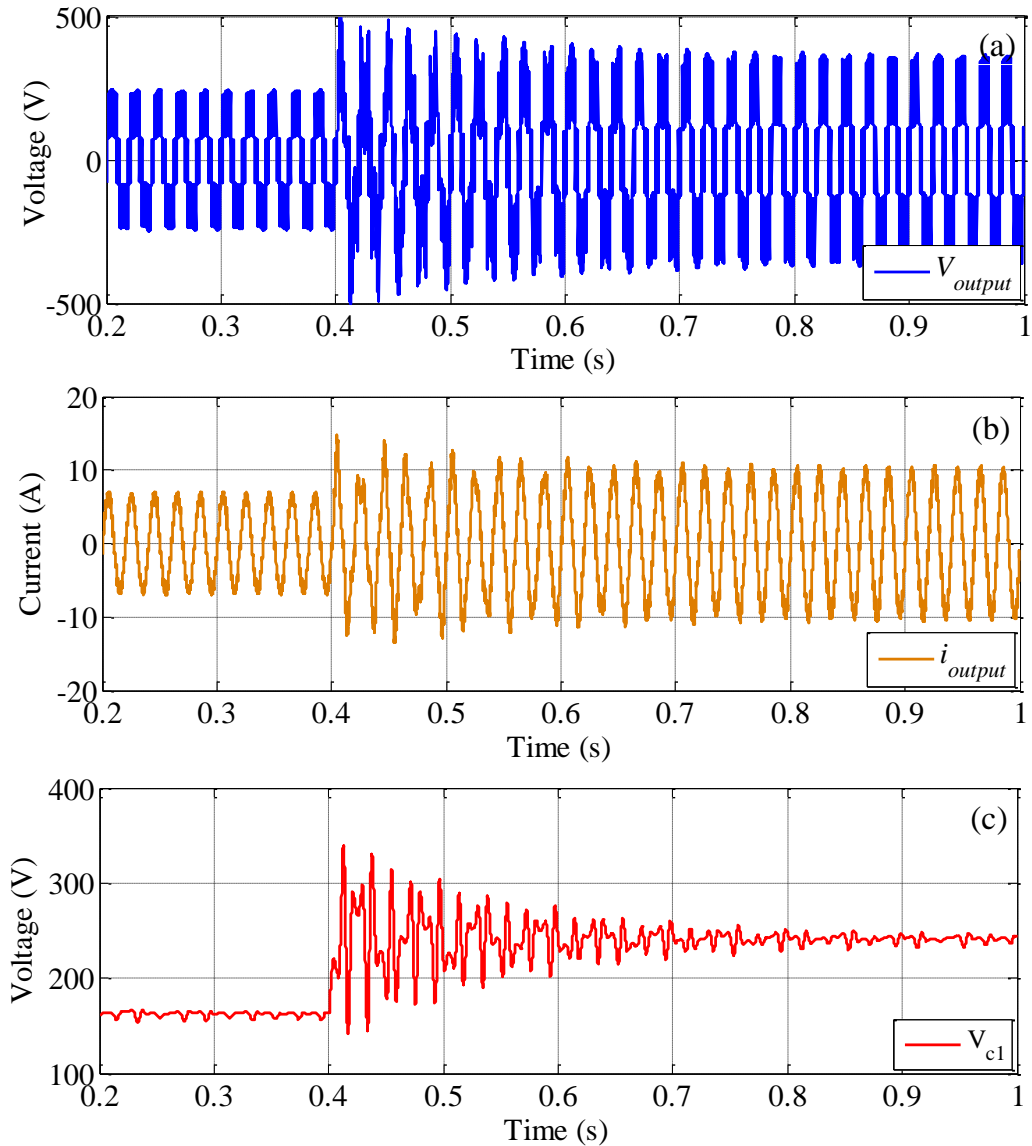
Fig 4.11 Simulation results of the effect of DC step change on the converter waveforms under conventional scheme. (a) Output load voltage. (b) Output load current (c) Voltage across C1

4.6.1.3 Effect of Different Inductive Load Values on the Performance

To farther validate the proposed method, the inductive load in the converter is applied with three different phase shifts between the inductor (L) and resistor (R), so that three different power factors are investigated. The evaluation of the influence of the three different values of the load inductance of 30, 55 and 155 mH on converter performance is shown in Fig 4.12, Fig 4.13 and Fig 4.14 where the voltage at C_1 is considered as an example.
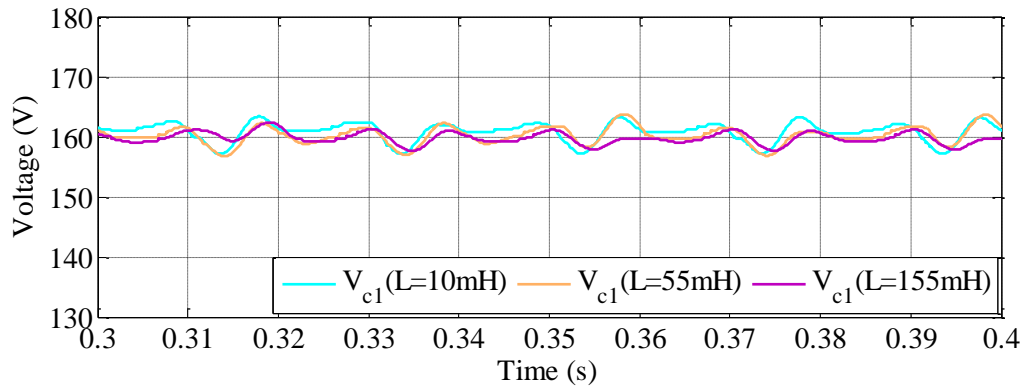
Fig 4.12 Simulation results of the investigation of V_{c1} with three different values of inductive load for the load current monitoring scheme.

Since the sensor-never proposed method does not monitor any currents, this test was necessary to evaluate the second proposed scheme in terms of having an application with high phase shift difference between its output load voltage and current. However and interestingly, it has been found that the second proposed method shows robustness against this assumption. Fig. 4.13 confirms the ability of the proposed sensor-never method to cope with three different inductor values. In comparison with the sensor-based conventional method, the proposed methods show some advantages when the load has high values of inductance.
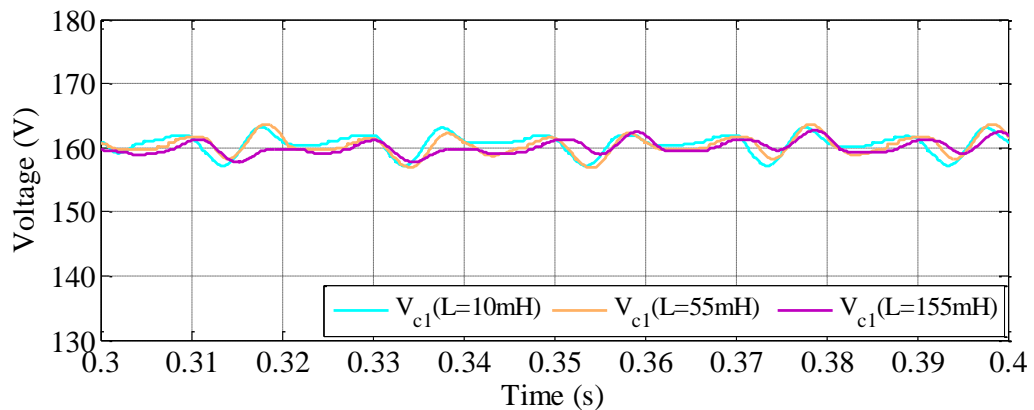
Fig 4.13 Simulation results of the investigation of V_{c1} with three different values of inductive load for the sensor-never current monitoring scheme.
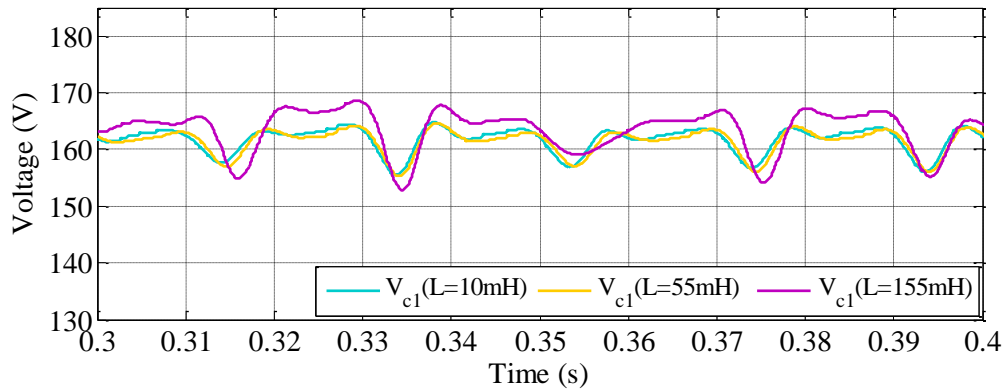
Fig 4.14 Simulation results of the investigation of V_{c1} with three different values of inductive load for the conventional scheme.

4.6.1.4 Step Change in the Load Condition.

To further confirm the effectiveness of the proposed methods, a step change in the load condition is applied to the converter. Fig. 4.15 shows the response of the output load current when the load is changed. This assumed change makes the load increase by 100% at 0.5s. As can be observed from Fig. 4.15 (b), the voltage for the first upper SM still tracks the required value.

The results presented in Fig. 4.16 are very close to those presented in Fig. 4.15 and Fig 4.17, and both proposed methods confirm the effectiveness of the proposed methods under this condition.
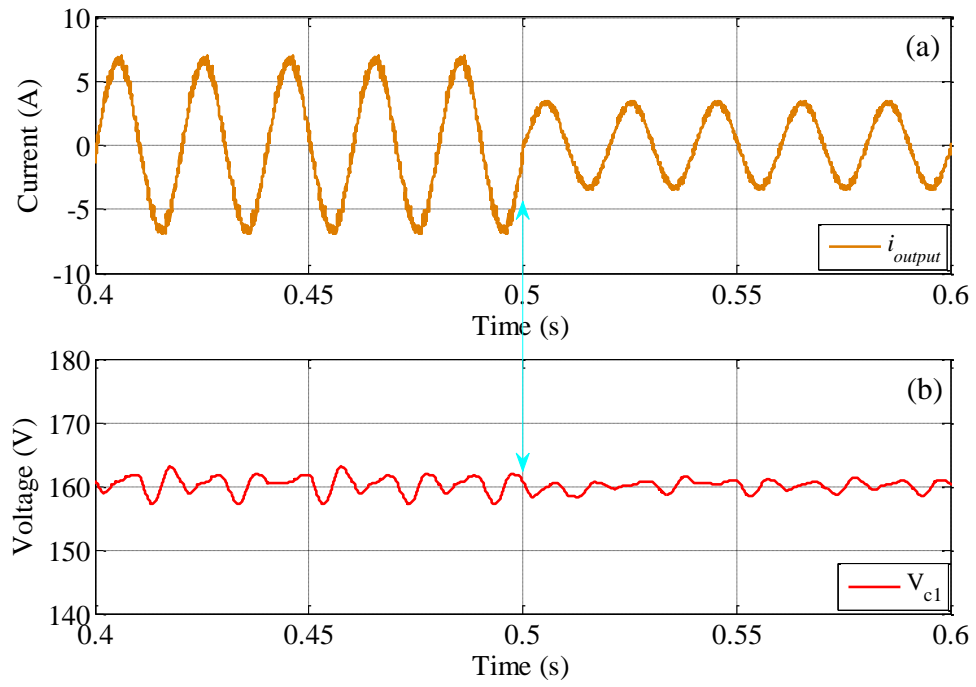
Fig 4.15 Simulation results of applying step change in the load condition for the load current monitoring method.
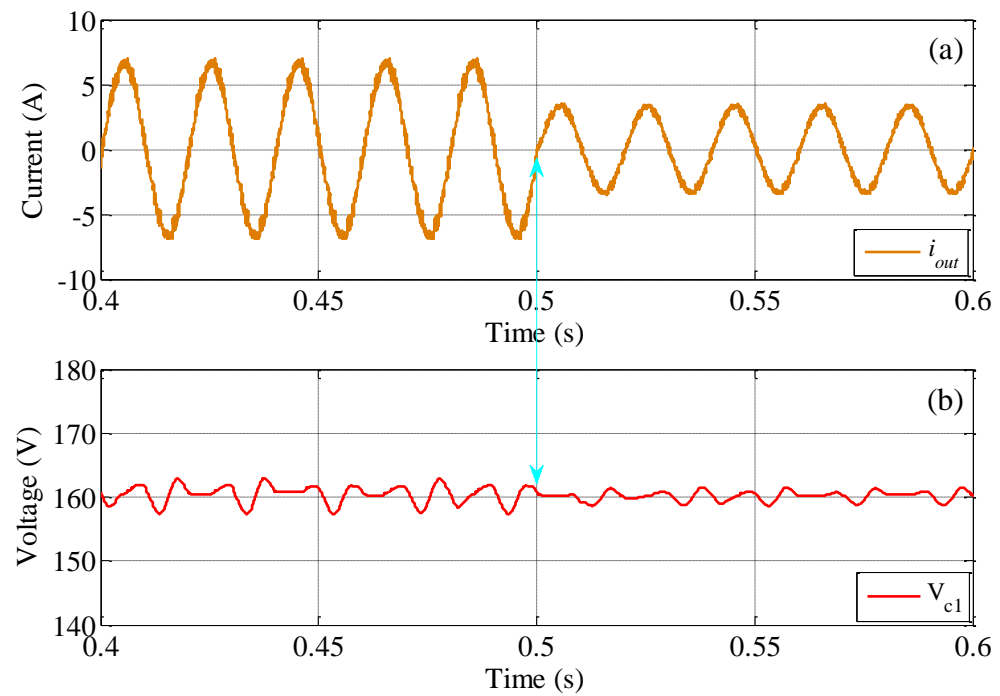
Fig 4.16 Simulation results of applying step change in the load condition for the sensor-never current monitoring method.
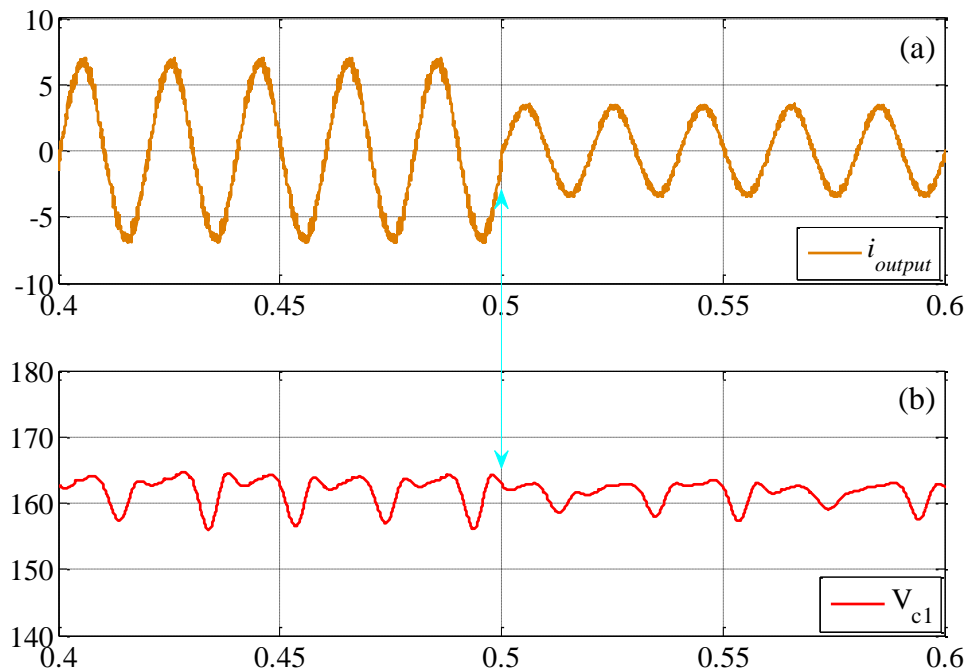
Fig 4.17 Simulation results of applying step change in the load condition for the sensor-based method.

4.6.1.5 Increasing the Output Level of the Converter for the Load Current Monitoring Method

Figs. 4.18-20 show the output response when the interleaving modulation scheme is applied for the proposed schemes and the conventional sensor-based scheme at 1s. The parameters used in this analysis are similar to those in the previous tests, and the only difference here is in the output level of the converter which has been increased from 4- to 5 level.

As can be seen from the figures, the output voltage is increased from 5- to 9-level, which reflects positively on the output load current waveform. This means a considerable reduction in filtering size can be achieved. On the other hand, the circulating and arm currents have increased for all methods.
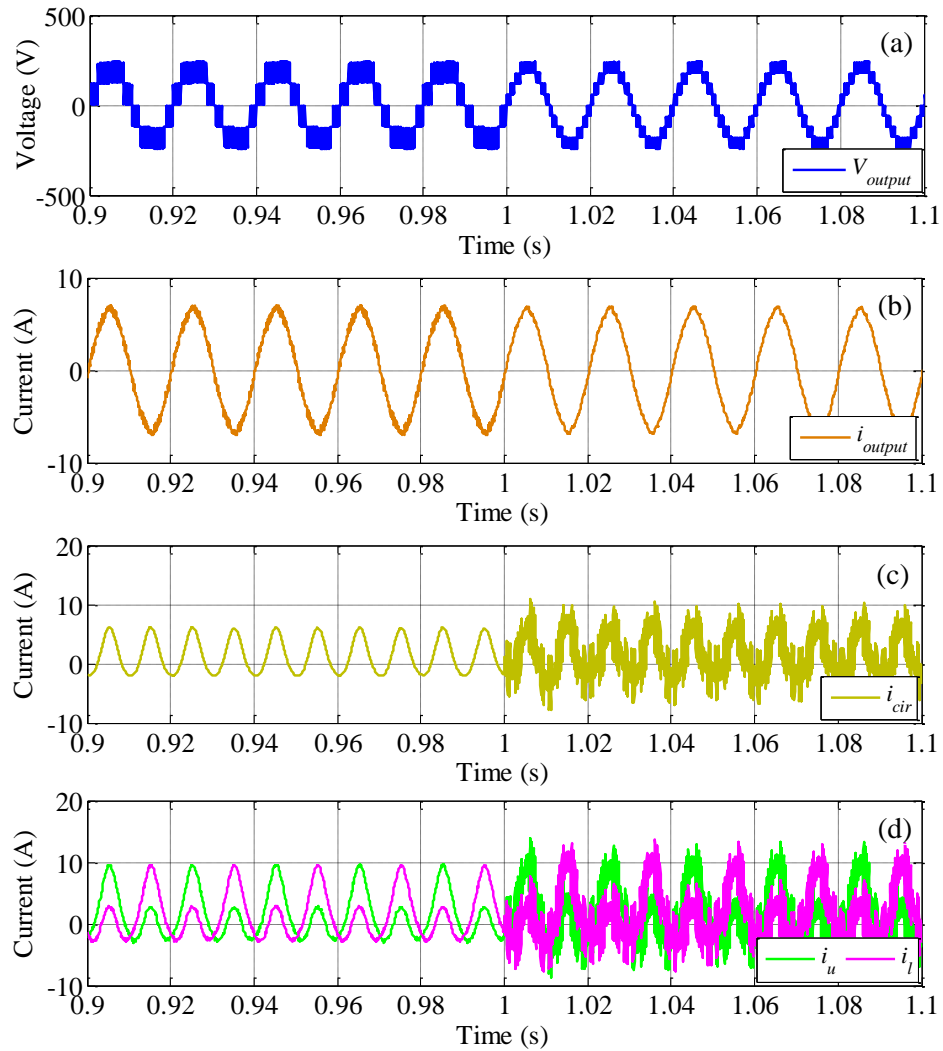
Fig 4.18 Simulation results of applying interleaving modulation scheme on 5-level MMC for load current monitoring method. (a) Output load voltage. (b) Output load current. (c) Circulating current. (d) Upper and lower arm currents.

The interleaving modulation scheme is also implementable for the sensor-never current monitoring method; however, similar to the current monitoring method, the circulating current is also increased as can be observed in Fig. 4.19.
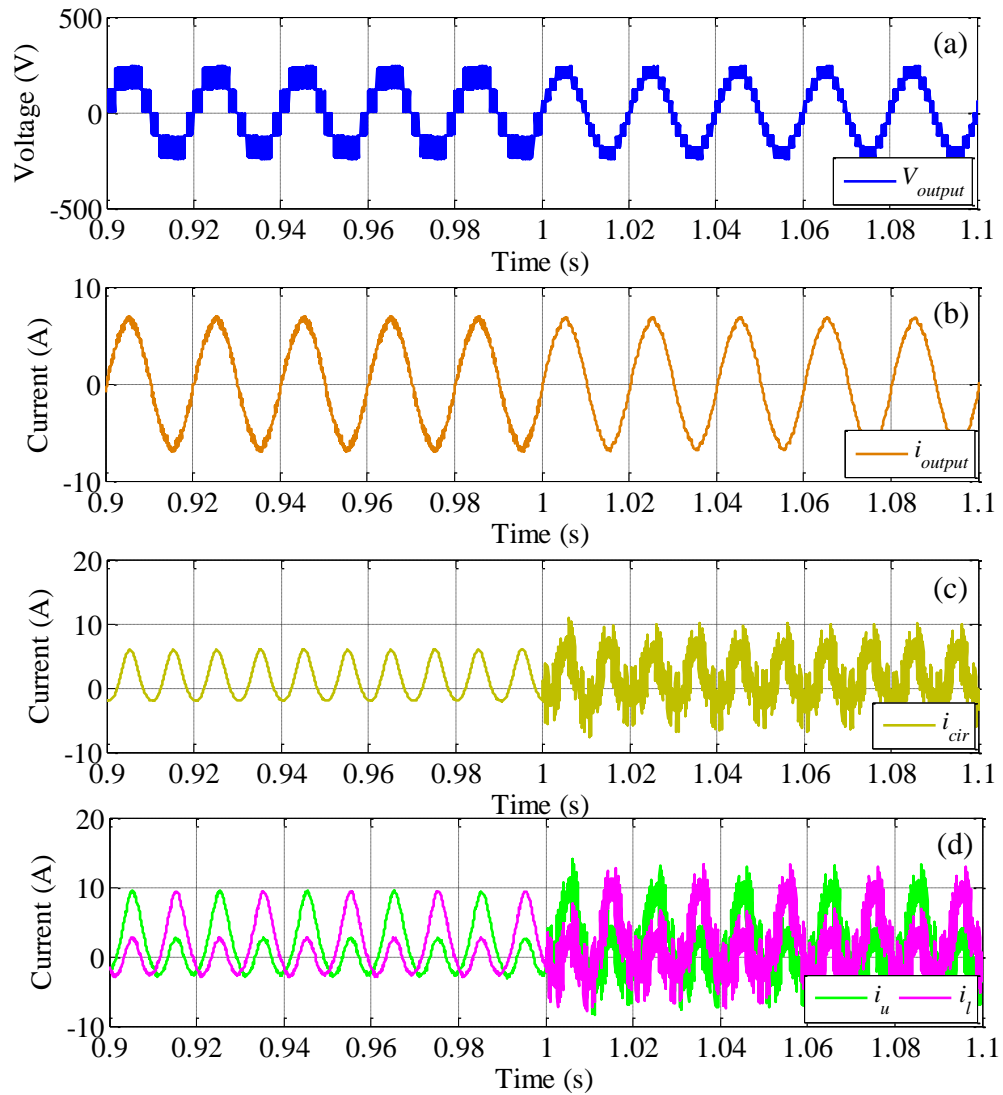
Fig 4.19 Simulation results of applying interleaving modulation scheme on 5-level MMC for sensor-never current monitoring method. (a) Output load voltage. (b) Output load current. (c) Circulating current. (d) Upper and lower arm currents.
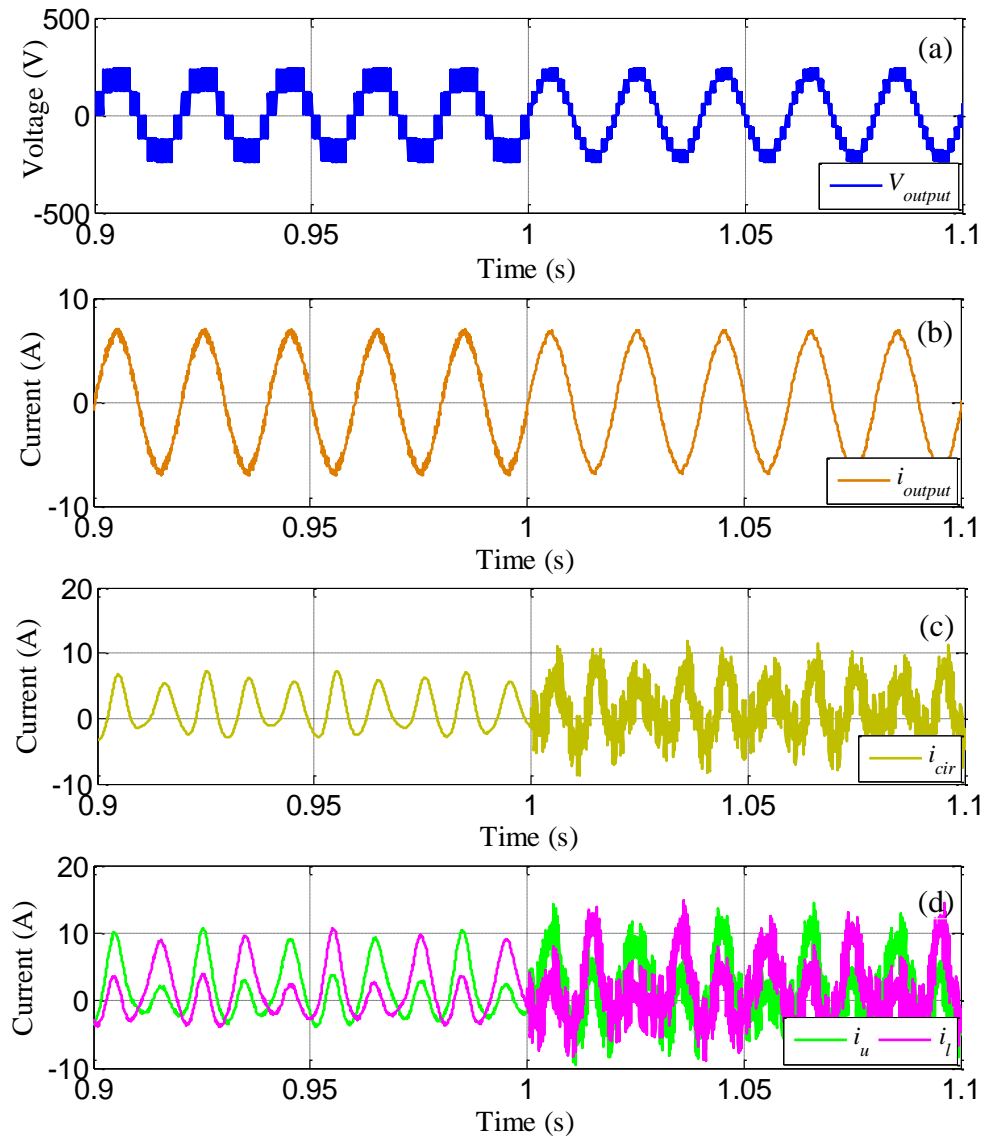
Fig 4.20 Simulation results of applying interleaving modulation scheme on 5-level MMC for sensor-based method. (a) Output load voltage. (b) Output load current. (c) Circulating current. (d) Upper and lower arm currents.

4.7 Experimental Results

Extensive experimental tests were carried out to verify the pre-obtained simulation results in practical environment.

4.7.1 Steady-State Results

To further experimentally validate the simulation results under normal operating conditions, a scaled-down system is used here. Details of the parameters used and

control set-up system are presented in Chapter 3. Figs. 4.21-23 illustrate the output voltage, the upper three SM voltages and the load current. The output current is compared with load voltage and shown in Fig. 4.24-26. Importantly, there is excellent agreement with the original simulation results in Figs. 4.6-8 and those presented here if the power rating difference is taken into consideration.

V_{c1} (3.3 V/div)
V_{c2} (3.3 V/div)
V_{c3} (3.3 V/div)
u_a (20 V/div)
(4 ms/div)
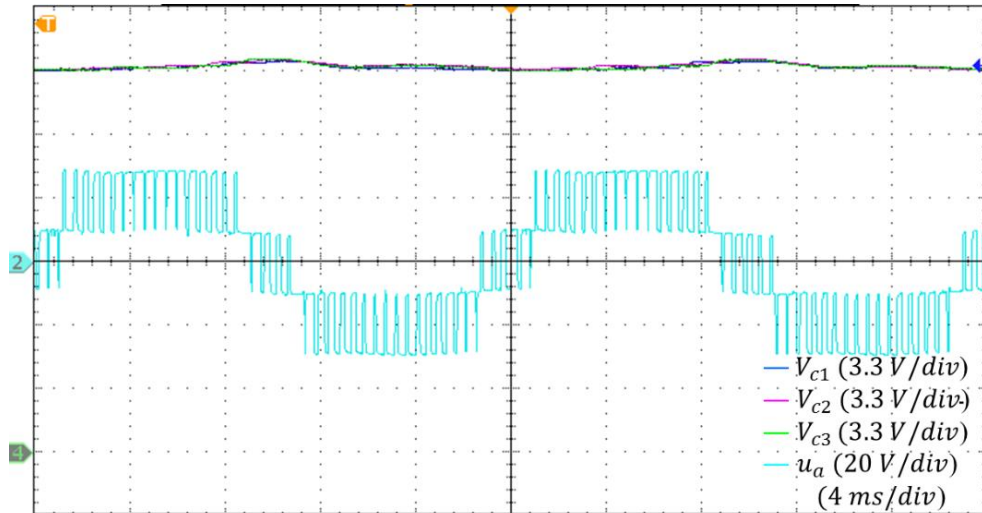
Fig 4.21 Experimental results for the output and three upper SMs voltage of the load current monitoring scheme.

V_{c1} (5 V/div)
V_{c2} (5 V/div)
V_{c3} (5 V/div)
u_a (20 V/div)
(4 ms/div)
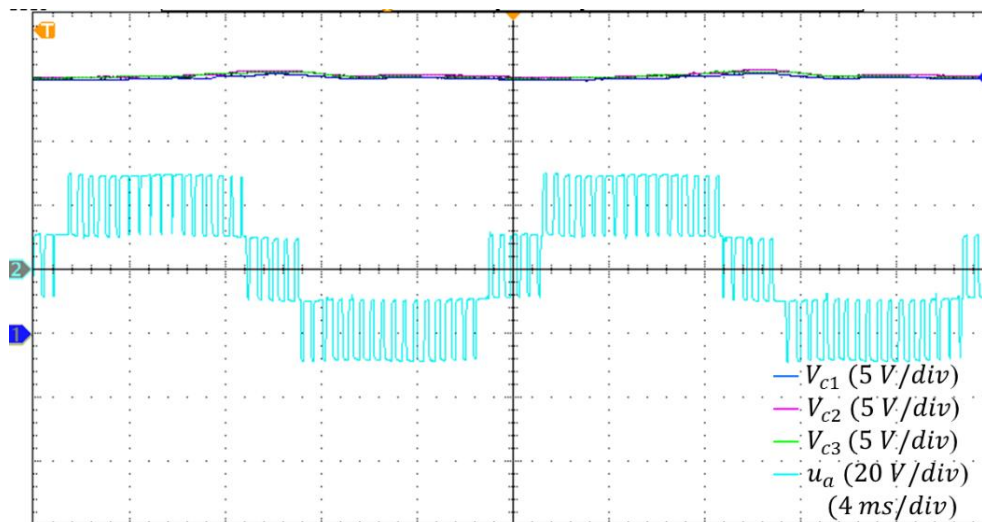
Fig 4.22 Experimental results for the output and three upper SMs voltage of the sensor-never current monitoring scheme.
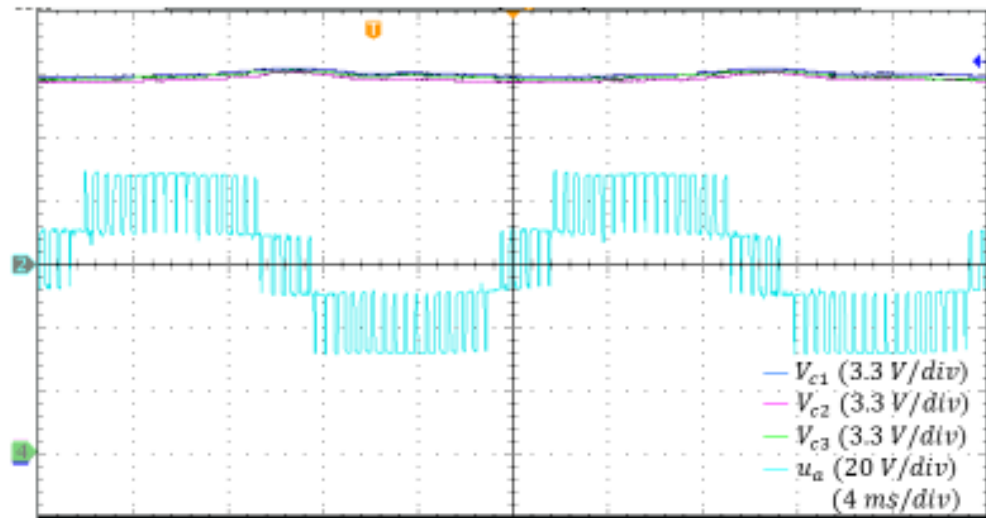
Fig 4.23 Experimental results for the output and three upper SMs voltage of the sensor-based scheme.
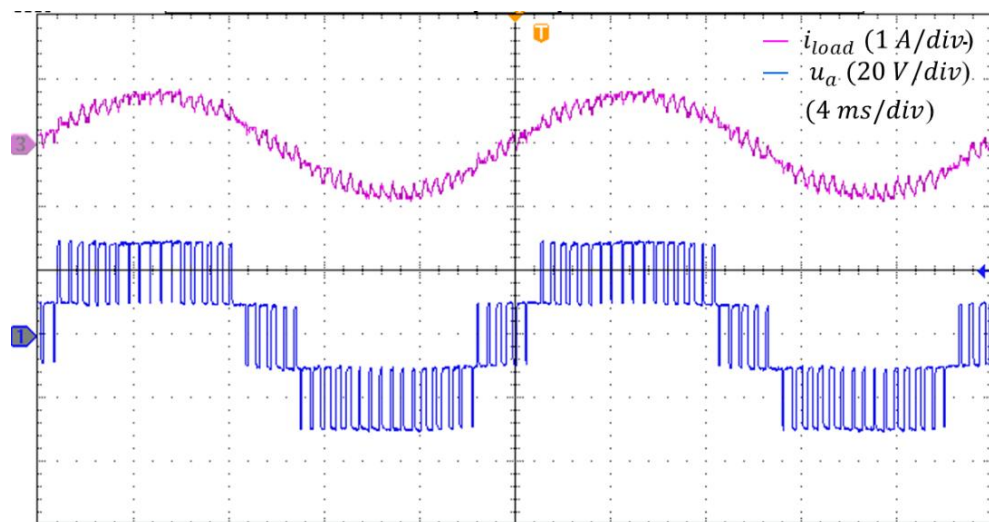
Fig 4.24 Experimental results for the output voltage and current of the load current monitoring proposed scheme.

i_{load} (1 A/div)
u_a (20 V/div)
(4 ms/div)
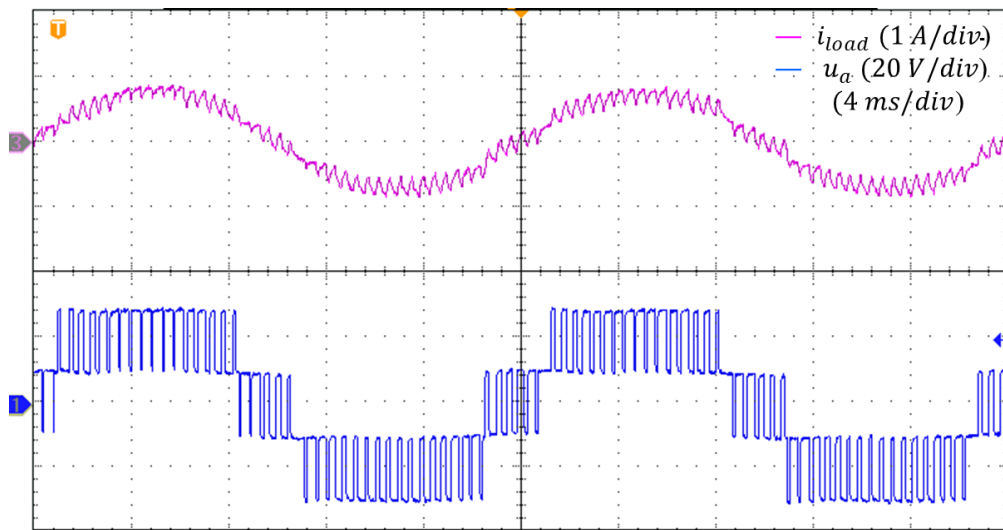
Fig 4.25 Experimental results for the output voltage and current of the sensor-never current monitoring proposed scheme.
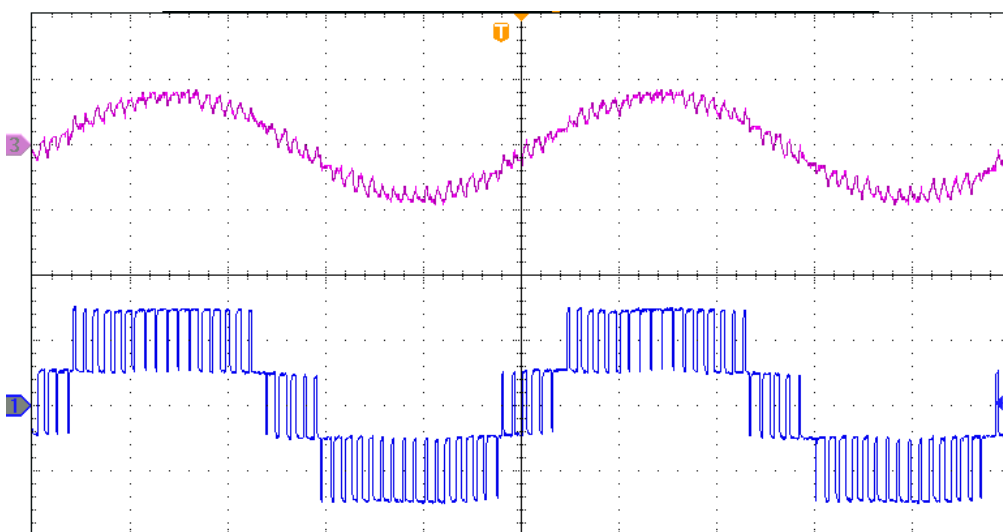
Fig 4.26 Experimental results for the output voltage and current of the sensor-based scheme.

4.7.2 Dynamic Results

After developing confidence concerning steady-state operation, the dynamic operation of the proposed schemes was considered. Firstly a sudden increase in DC voltage was applied with the proposed methods in Figs. 4.27 and 4.28. The first SM was selected as an example in order to evaluate the voltage-balancing of the converter. In comparison with the sensor-never scheme, the load current monitoring scheme requires more time to reach the reference SM voltage (i.e. $V_{c1-reference} = 20$ v), whilst the sensor-never current monitoring scheme has a higher overshoot value. However, both sets of results are within the acceptable range, which once again confirms the capability of the proposed methods.

On the other hand, the same test is applied for the conventional sensor-based method in Fig. 4.29. As can be seen from the figure, the voltage across C_1 also very rapidly tracks its reference value. In contrast with the simulation studies, an averaging filter is applied for all SM voltages for the practical implementation before applying the voltage-balancing control algorithm. The general standard averaging filter used for Vc_1 is shown in Fig. 4.30 where, in this implementation, the delay element D is 5 which satisfies the following formula:

$$Vc_{1(ti)\ filtered} = \frac{1}{D} \left[Vc_{1(ti)} + Vc_{1(ti-1)} + \cdots + Vc_{1(ti-4)} \right] \qquad (4.3)$$

Finally, and to further validate these methods, a common dynamic change test was applied and the results are shown in Fig. 4.31, 4.32 and 4.33 respectively. An increase and decrease in the load condition values by approximately 100% were applied to MMC. The converter successfully dealt with such changes, and the three upper SM voltages presented in the figures prove this for all methods.
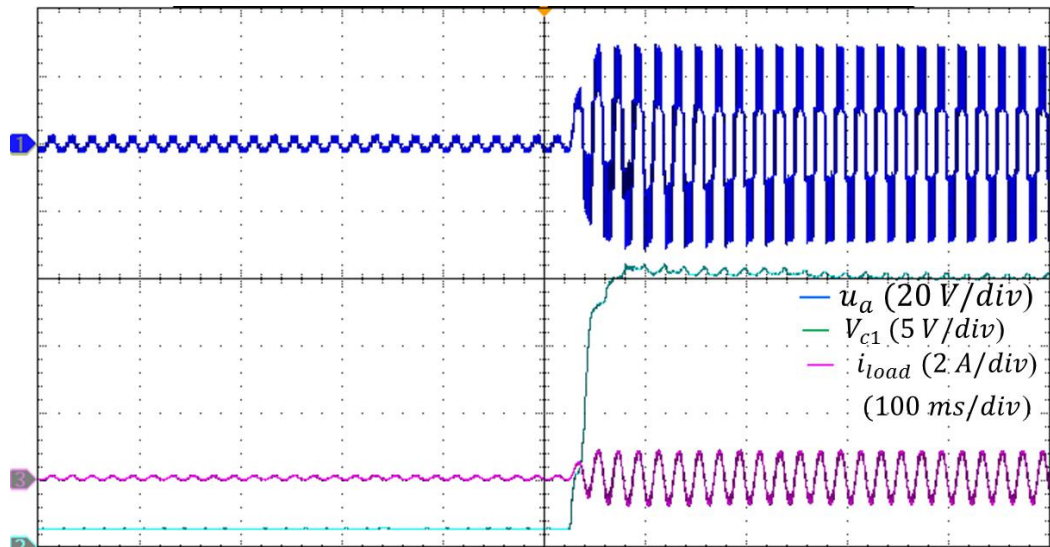
Fig 4.27 Experimental results of step change in the DC voltage and its impact on the voltage across Vc1 / Applied for the load current monitoring proposed scheme.
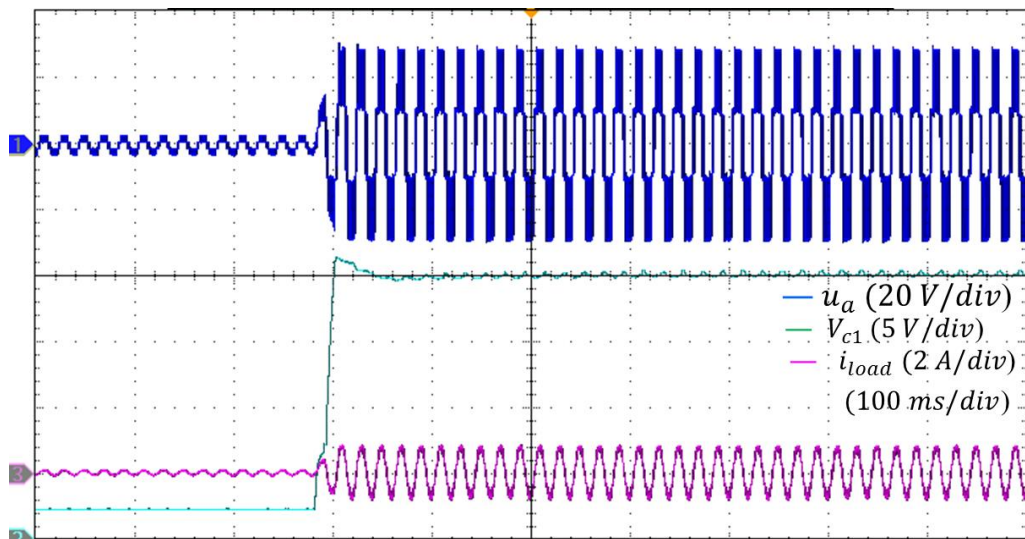
Fig 4.28 Experimental results of step change in the DC voltage and its impact on the voltage across Vc1 / Applied for the sensor-never current monitoring proposed scheme.
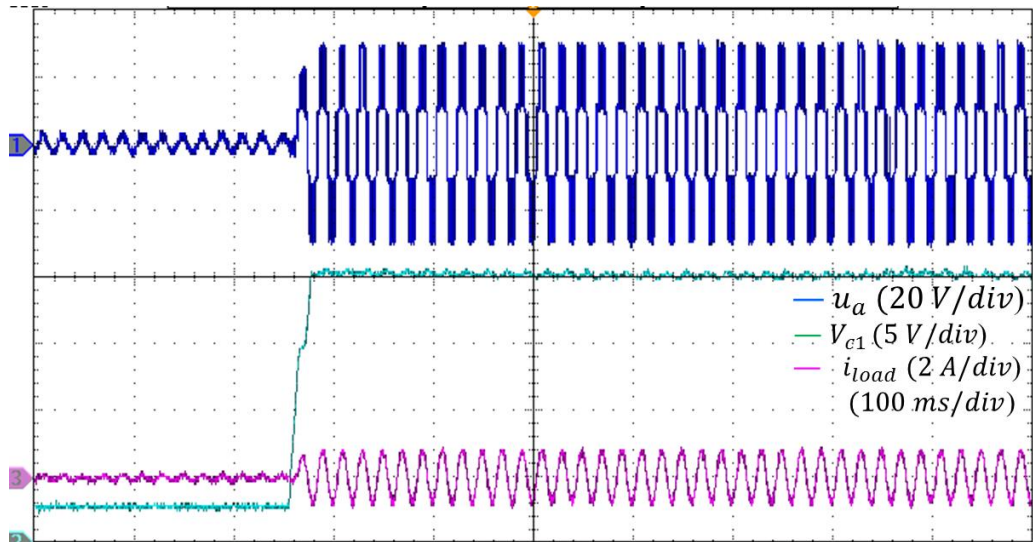
Fig 4.29 Experimental results of step change in the DC voltage and its impact on the voltage across Vc1 / Applied for the sensor-based scheme.
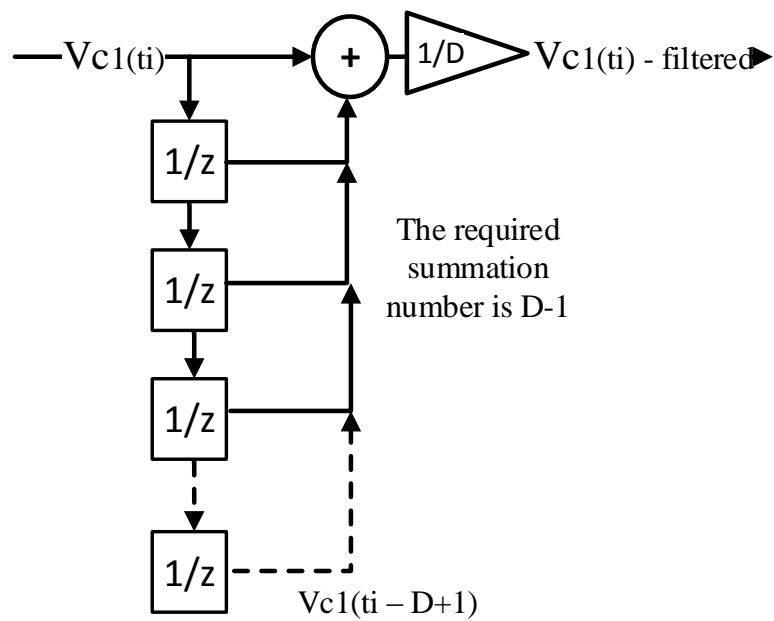
Fig 4.30 Standard averaging filter used in the experimental implementation.
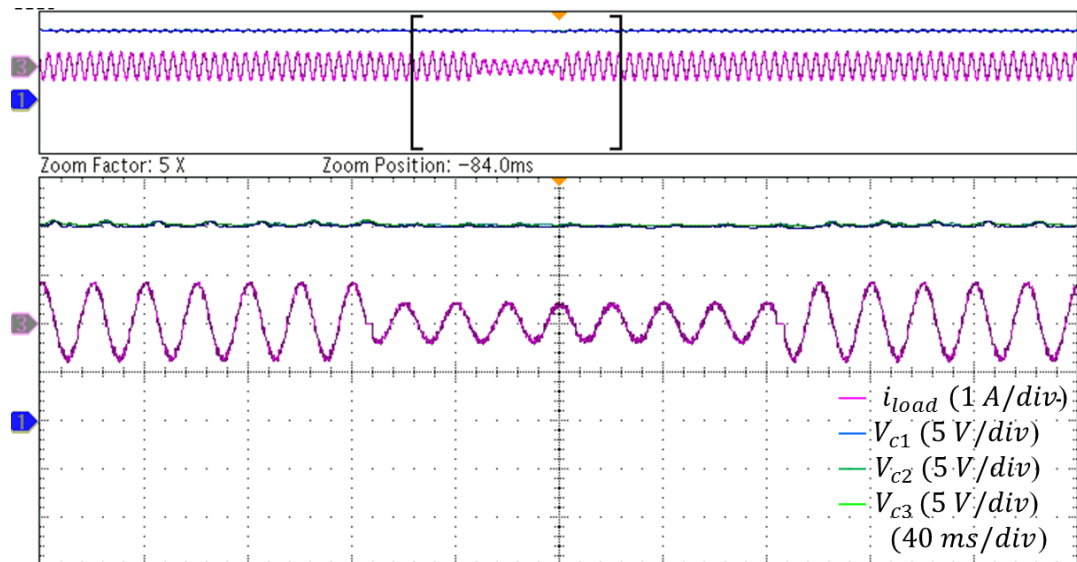
Fig 4.31. Experimental results of step changes in the load condition of the load current monitoring proposed scheme.
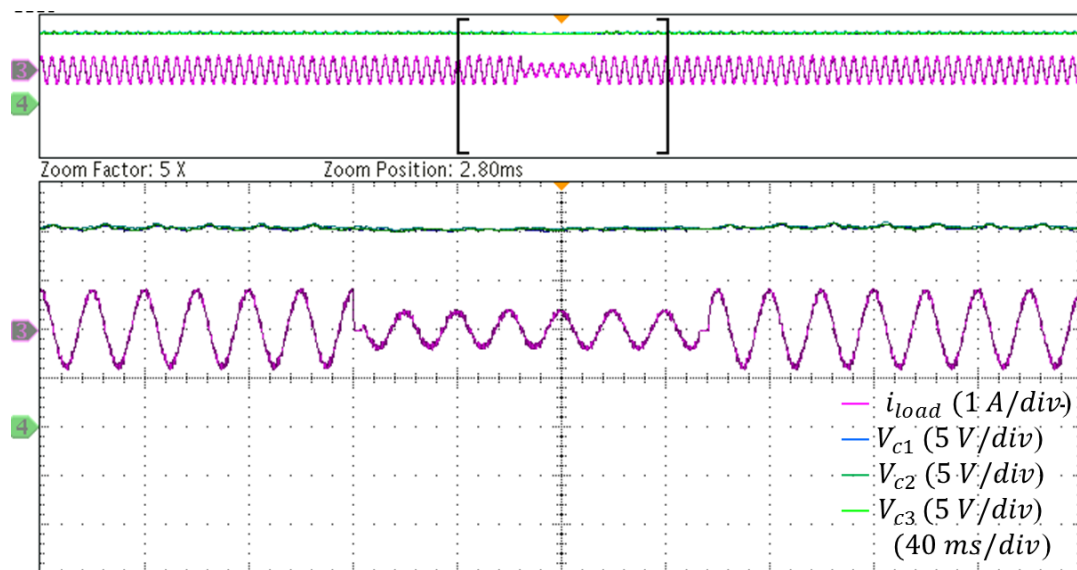
Fig 4.32. Experimental results of step changes in the load condition of the sensor-never current monitoring proposed scheme.
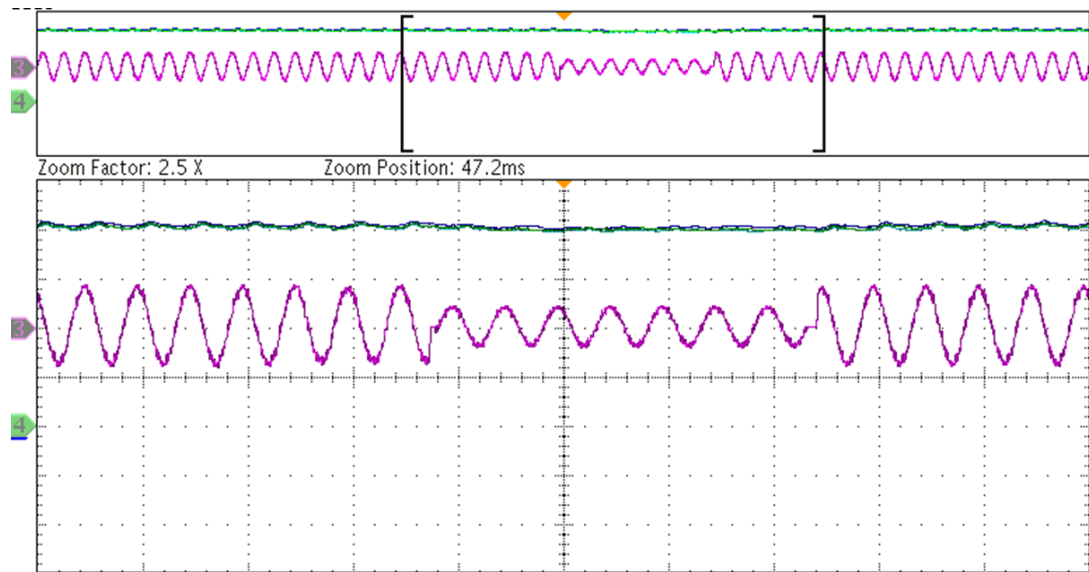
Fig 4.33 Experimental results of step changes in the load condition of the sensor-based scheme.

4.8 Chapter Summary

In this Chapter, voltage balancing control methods have been proposed for the MMC. Two different procedures have been investigated, where the idea was to demonstrate the ability to balance the SM voltage capacitors with fewer current sensors by modifying the conventional sorting algorithm used in previous studies. The first involves only one current sensor per leg, while the second method achieves voltage balancing without any current sensors. With these proposed methods, different PWM modulation techniques can be used. Simulation and experimental studies for both methods show and confirm the performance on a 4-level MMC under different operating conditions.

There are similarity in the two investigated methods in terms of steady-state and dynamic performance. However, following table summarises the differences and performances of all proposed methods versus the conventional method:

Table 4.2. Comparisons of the proposed methods versus the conventional method used.

Methods	Steady-state condition	Dynamic condition	Required current sensors
Load current monitoring method vs conventional method	➤ Output voltages and currents are almost similar. ➤ Circulating currents are almost the same. ➤ Voltage ripples are similar for low inductance load value. However, for higher inductance load, the conventional method has higher voltage ripples.	Voltage across capacitors has more oscillation.	1 vs 2 for each phase
Sensor-never current monitoring method vs conventional method	➤ Output voltages and currents are almost similar. ➤ Circulating currents are almost the same. ➤ Voltage ripples are similar for low inductance load value. However, for higher inductance load, the conventional method has higher voltage ripples.	Voltage across capacitors has more oscillation.	zero vs 2 for each phase
"It should be noted that for all methods, the converter parameters may have different impact on the performance"			

The next Chapter discusses achieving voltage-balancing of the converter with fewer voltage sensors not fewer current sensors, where a new algorithm is introduced with the conventional sorting algorithm.

CHAPTER 5

....

PROPOSED SENSORLESS VOLTAGE ESTIMATION METHOD BASED ON EXPONENTIALLY WEIGHTED RECURSIVE LEAST SQUARE ALGORITHM

....

5.1 Introduction

As mentioned earlier in Chapters 2, the most promising application for the MMC requires a high number of SMs [35]. This means that the same numbers of voltage sensors must be used with the sensor-based measurement technique. Not only are the cost and complexity increased, but reliability can also be seen as another issue where the converter consists of a series of cascaded SMs. Therefore, a scheme to overcome this issue is proposed in this chapter.

This chapter proposes a solution to the voltage-balancing control issue which is always associated with the MMC. With the proposed scheme, voltage-balancing of the converter is achieved with fewer voltage sensors. In the proposed estimation technique, an ERLS algorithm is employed for the first time in MMC applications to estimate the voltage across each SM capacitor. Various simulation and experimental tests are performed to evaluate the effectiveness of the proposed method at different load conditions. Comparisons with the sensor-based measurement technique are also included in the chapter analysis.

The proposed technique requires only the measurement of the total arm voltage and the switching states of the SMs. These switching values are obtained from the controller used and hence no extra sensors are required. In comparison to [46, 47], the use of this algorithm does not require an advanced voltage-balancing method since any conventional or simple scheme can be applied. Compared to observer-based methods the variation in the arm inductance is a critical issue, this method is completely independent of such variation, because the measurement of voltages across arm inductors is not required by the algorithm. Details will be given in the section explaining the algorithm design.

Before describing the ERLS algorithm, other basic algorithms which are the basis of the ERLS algorithm need to be reviewed in the following two sections along with a discussion of suitability of these basic algorithms for the MMC.

5.2 Least Square (LS) Algorithm

The least square (LS) algorithm is a mathematical process which is used to identify unknown parameters for a real physical model from other data accessible within the same model [78]. This has to be expressed mathematically in a very accurate way in order to achieve high accuracy in estimation results (as precise as the mathematical model is as accurate as the estimated results can be achieved). Although this algorithm is not used in the proposed method, it is important to explain the principle behind it as most recursive algorithm families are based on similar concepts.

Assume that a real model is represented by the following mathematical model, where the aim is to identify the values of $\boldsymbol{\theta}_{1(t_i)}, \boldsymbol{\theta}_{2(t_i)}, \dots \boldsymbol{\theta}_{n(t_i)}$:

$$\mathbf{y}_{(t_i)} = \mathbf{z}_{1(t_i)}\boldsymbol{\theta}_{1(t_i)} + \mathbf{z}_{2(t_i)}\boldsymbol{\theta}_{2(t_i)} + \cdots + \mathbf{z}_{n(t_i)}\boldsymbol{\theta}_{n(t_i)} \tag{5.1}$$

in which $i = 1, 2, 3, \dots j$, $\mathbf{y}_{(t_i)}$ is the available measured data, $z_{1(t_i)}, z_{2(t_i)}, \dots z_{n(t_i)}$ are other known variables and $\boldsymbol{\theta}_{1(t_i)}, \boldsymbol{\theta}_{2(t_i)}, \dots \boldsymbol{\theta}_{n(t_i)}$ are the unknown parameters. Therefore, (5.1) can be rewritten in matrix form as follows:

$$\mathbf{y}_{(t_i)} = \mathbb{Z}^T_{(t_i)}\boldsymbol{\theta}_{(t_i)} \tag{5.2}$$

where
$$\mathbf{y} = \begin{bmatrix} \mathbf{y}(1) \\ \mathbf{y}(2) \\ \vdots \\ \mathbf{y}(N) \end{bmatrix}, \ \mathbb{Z} = \begin{bmatrix} \mathbf{z}_1(1) & \mathbf{z}_2(1) & \cdots & \mathbf{z}_n(1) \\ \mathbf{z}_1(2) & \mathbf{z}_2(2) & \cdots & \mathbf{z}_n(2) \\ \vdots & \vdots & \ddots & \vdots \\ \mathbf{z}_1(N) & \mathbf{z}_2(N) & \cdots & \mathbf{z}_n(N) \end{bmatrix} \text{ and } \boldsymbol{\theta} = \begin{bmatrix} \boldsymbol{\theta}_1 \\ \boldsymbol{\theta}_2 \\ \boldsymbol{\theta}_3 \\ \vdots \\ \boldsymbol{\theta}_n \end{bmatrix}$$

The estimated value of $\boldsymbol{\theta}$ is given by [78]:

$$\widehat{\boldsymbol{\theta}} = [\mathbb{Z}^T\mathbb{Z}]^{-1}\mathbb{Z}^T\mathbf{y} \tag{5.3}$$

One critical issue of the LS algorithm is the matrix inverse $[\mathbb{Z}^T\mathbb{Z}]^{-1}$ which needs to be recalculated for every new measurement which means that all previous data needs to be stored. This means that the LS algorithm is valid for off-line estimation problems only [78].

5.3 Conventional RLS Algorithm

Due to the limitations of the LS algorithm mentioned above, recursive LS (RLS) algorithms were proposed for real-time implementation issues [78, 79].

The arrangement of the conventional RLS algorithm is summarised in sequence in table 5.1 [80]. The mathematical derivation of this algorithm is detailed in Appendix A. However, in table 5.1, steps (3-6) may be suitable only if the model described in (5.2) has constant dynamic behaviour. However, MMCs might exhibit variable dynamic behaviour, such as step changes in load value or any other sudden changes in the system's conditions. In addition, applying a closed-loop control strategy where

PWM patterns vary with time may also affect the estimation results. This means that the conventional RLS is not suitable for the target application of MMC. Therefore, a developed adaptive scheme of the conventional RLS algorithm must be used instead.

Table 5.1 Conventional RLS adaptive algorithm

Step	Action and related equation
1. Initialisation	Initiate $P_{(t_0)}$ and $\widehat{\boldsymbol{\theta}}_{(t_0)}$
2. Activate the algorithm	For $i = 1, 2, 3, \dots j$
3. Calculate the gain	$K_{(t_i)} = \dfrac{P_{(t_{i-1})}\, z_{(t_i)}}{\left(z^T_{(t_i)}\, P_{(t_{i-1})}\, z_{(t_i)} + 1\right)}$
4. Calculate prediction error	$e_{\mathbf{y}_{(t_i)}} = \mathbf{y}_{(t_i)} - \hat{\mathbf{y}}_{(t_i)},\ \hat{\mathbf{y}}_{(t_i)} = z^T_{(t_i)}\widehat{\boldsymbol{\theta}}_{(t_i)}$
5. Update the parameter $\widehat{\boldsymbol{\theta}}$	$\widehat{\boldsymbol{\theta}}_{(t_i)} = \widehat{\boldsymbol{\theta}}_{(t_{i-1})} + K_{(t_i)} e_{\mathbf{y}_{(t_i)}}$
6. Update the covariance matrix (p)	$P_{(t_i)} = \left[\left(P_{(t_{i-1})}\right) - \left(k_{(t_i)} Z^T_{(t_i)}\, P_{(t_{i-1})}\right)\right]$

5.4 Exponentially Weighted RLS Algorithm

To cope with the issues mentioned with the previous algorithms, the ERLS algorithm is proposed for the MMC. It is also named as RLS with forgetting factor algorithm [80, 81]. The core concept of the forgetting factor algorithm scheme is to give less weight to elder data and more weight to new data by adding a coefficient called a forgetting factor. The cost function of the ERLS algorithm is given as follows [82]:

$$J_u = \sum_{i=1}^{j} \lambda^{j-i}(\mathbf{y}_{(t_i)} - \mathbf{z}^T_{(t_i)}\widehat{\boldsymbol{\theta}}_{(t_i)})^2 \tag{5.4}$$

where λ is known as the forgetting factor as mentioned above. The smaller the forgetting factor, the faster the tracking of a time-varying unknown parameter will be; however, the algorithm will be more sensitive to noise. Therefore, care has to be taken when λ is chosen. It should be noted that each system has its own standard of

choosing this factor. However, it is recommended that this factor should be chosen within the range of: $0 \ll \lambda < 1$ [83].

Similar to step four in table 5.1, the estimated value of $\boldsymbol{\theta}_{(t_i)}$ is defined by:

$$\widehat{\boldsymbol{\theta}}_{(t_i)} = \widehat{\boldsymbol{\theta}}_{(t_{i-1})} + \boldsymbol{K}_{(t_i)}\boldsymbol{e}_{\mathbf{y}_{(t_i)}} \qquad (5.5)$$

However, $K_{(t_i)}$ here is given by:

$$\boldsymbol{K}_{(t_i)} = \frac{\boldsymbol{P}_{(t_{i-1})}\,\boldsymbol{z}_{(t_i)}}{\left(\boldsymbol{z}^T{}_{(t_i)}\,\boldsymbol{P}_{(t_{i-1})}\,\boldsymbol{z}_{(t_i)} + \lambda\right)} \qquad (5.6)$$

and the covariance matrix will be:

$$P_{(t_i)} = (\frac{1}{\lambda})\left[\left(P_{(t_{i-1})}\right) - \left(k_{(t)}\,z_{(t_i)}\,P_{(t_{i-1})}\right)\right] \qquad (5.7)$$

Table 5.2 summarises the sequence of operation of the ERLS algorithm.

Table 5.2 ERLS adaptive algorithm

Step	Action and related equation
1. Initialisation	Initiate $P_{(t_0)}$, $\widehat{\boldsymbol{\theta}}_{(t_0)}$ and λ
2. Calculate the gain	$K_{(t_i)} = \dfrac{P_{(t_{i-1})}\,z_{(t_i)}}{\left(z^T{}_{(t_i)}\,P_{(t_{i-1})}\,z_{(t_i)} + \lambda\right)}$
3. Calculate prediction error	$e_{\mathbf{y}_{(t_i)}} = \mathbf{y}_{(t_i)} - \widehat{\mathbf{y}}_{(t_i)},$ $\widehat{\mathbf{y}}_{(t_i)} = z^T{}_{(t_i)}\widehat{\boldsymbol{\theta}}_{(t_i)}$
4. Update the parameter $\widehat{\theta}$	$\widehat{\boldsymbol{\theta}}_{(t_i)} = \widehat{\boldsymbol{\theta}}_{(t_i)} + K_{(t_i)}\boldsymbol{e}_{\mathbf{y}_{(t_i)}}$
5. Update the covariance matrix P	$P_{(t_i)} = (\frac{1}{\lambda})\left[\left(P_{(t_{i-1})}\right) - \left(k_{(t_i)}z^T{}_{(t_i)}\,P_{(t_{i-1})}\right)\right]$

5.5 Proposed Estimation Technique

Fig. 5.1 shows a single-phase MMC based on the half-bridge configuration. In this research, only the half-bridge configuration is examined.
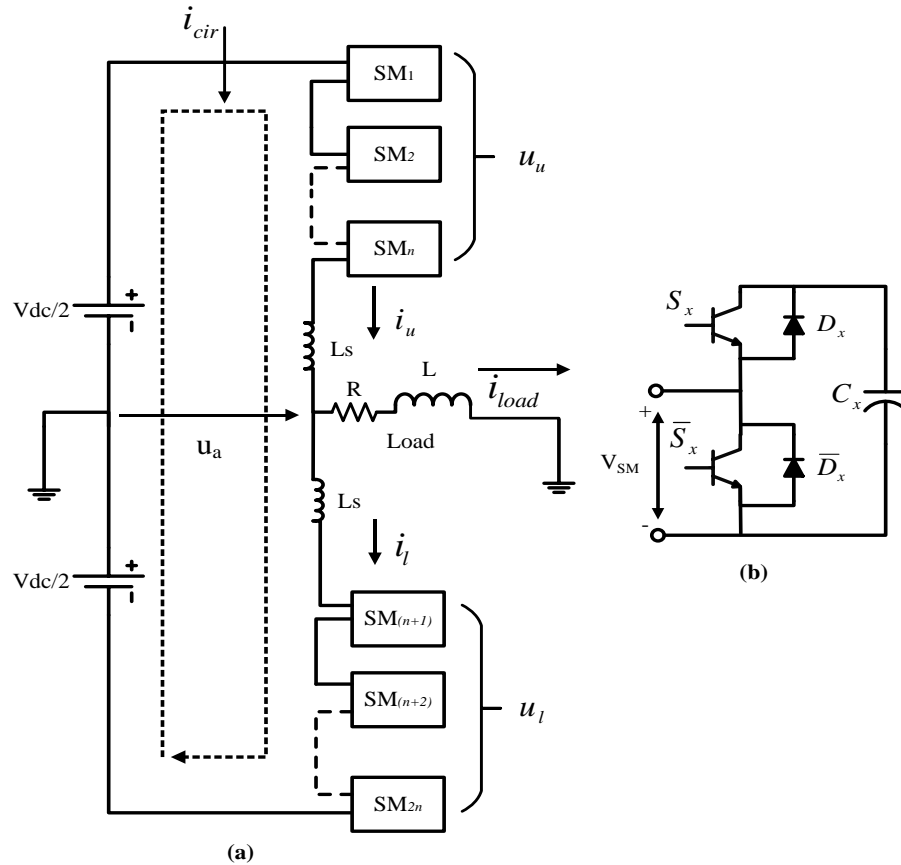
Fig 5.1. Block diagram of MMC. (a) Single-phase (one-leg) Block diagram. (b) Half-bridge SM configuration.

5.5.1 Modelling and System Configuration of the SMs

In the proposed scheme, only one voltage sensor is required for each arm as illustrated in Fig. 5.2. Interestingly, it has been found that there is a similarity between the linear model described for the previous algorithms and the relationship between total arm voltage, SM voltages and the switching states of the converter.

Two sensors are used in the proposed scheme (i.e. upper and lower sensors). The upper sensor is connected at the output of the series-cascaded SMs, where the connection is performed between the top terminal point of the first SM (SM$_1$) and the bottom

terminal point of the last SM (SM_n) within this arm. Similar to the upper arm, the sensor for the lower arm is connected between $SM_{(n+1)}$ and SM_{2n}.

To the positive connection
point of the V_{dc}

SM$_1$

Line 1

SM$_2$

Upper Voltage
Sensor

u_u

SM$_n$

To the top connection point of the upper arm inductor L_s

(a)

To the lower connection point of the lower arm
inductor L_s

SM$_{(n+1)}$

SM$_{(n+2)}$

Lower Voltage
Sensor

u_l

SM$_{2n}$

To the negative connection point of the V_{dc}

(b)
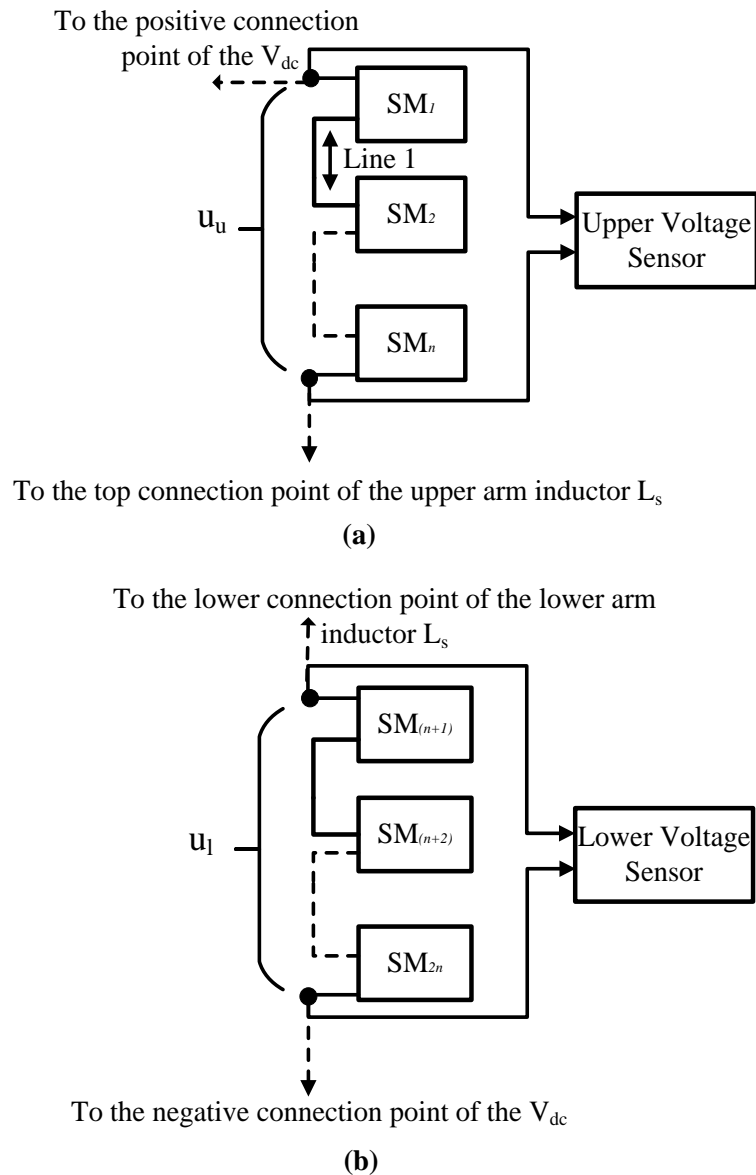
Fig 5.2. Connection arrangement of the proposed measuring technique for the MMC. (a) Upper voltage sensor arrangement. (b) Lower voltage sensor arrangement.

This arrangement makes the method independent of parameter variation associated with the arm inductor value. For an *N*-level converter; where $N = (1 + n)$, the total voltage SMs of the upper and lower arms in Fig. 5.2 can be modelled respectively as follows:

$$\mathbf{u}_u(t_0) = S_1(t_0)\,\mathbf{V}_{c1}(t_0) + \cdots + \ S_n(t_0)\,\mathbf{V}_{cn}(t_0)$$

$$\mathbf{u}_u(t_1) = S_1(t_1)\,\mathbf{V}_{c1}(t_1) + \cdots + S_n(t_1)\,\mathbf{V}_{cn}(t_1)$$

$$\vdots \quad = \quad \vdots \qquad + \cdots + \qquad \vdots \qquad\qquad 5.8)$$

$$\mathbf{u}_u(t_j) = S_1(t_j)\,\mathbf{V}_{c1}(t_j) + \cdots + S_n(t_j)\,\mathbf{V}_{cn}(t_j)$$

$$\mathbf{u}_l(t_0) = S_{n+1}(t_0)\,\mathbf{V}_{c(n+1)}(t_0) + \cdots + \ S_{2n}(t_0)\,\mathbf{V}_{c2n}(t_0)$$

$$\mathbf{u}_l(t_1) = S_{n+1}(t_1)\,\mathbf{V}_{c(n+1)}(t_1) + \cdots + \ S_{2n}(t_1)\,\mathbf{V}_{c2n}(t_1) \qquad 5.9)$$

$$\vdots \quad = \qquad \vdots \qquad\qquad + \cdots + \quad \vdots$$

$$\mathbf{u}_l(t_j) = \ S_{n+1}(t_j)\,\mathbf{V}_{c(n+1)}(t_j) + \cdots + \ S_{2n}(t_j)\,\mathbf{V}_{c2n}(t_j)$$

where $t_1 - t_0 = t_2 - t_1 = \cdots = t_j - t_{j-1} = \ \Delta t$ (sampling period).

Note that, in (5.8) and (5.9) the upper switch (S_x) (where $x = 1,2,\dots 2n$) is the main switch responsible for charging and discharging the SM's capacitor. It also worth noting that due to the small internal resistance of the semiconductor switch, the voltage drop caused by S_x is neglected in this analysis. Furthermore, knowledge of the switching states, obtained directly from the controller, without including the voltage drop has been proven to be sufficient for different estimation methods [40, 44, 46]. However, while this drop is described as negligible in [40, 44, 46], the actual values are not indicated. Nevertheless, it is easy to estimate this drop in order to improve the accuracy of the proposed model. The experimental results section of this chapter gives more details on the effect of voltage drop on the system model.

5.5.2 Proposed Voltage Estimation Technique

It is found that, by employing this algorithm to the MMC model which was described earlier in equation (5.1) and (5.2), the estimation of the individual SM voltage can be accomplished. The arm voltage model of the upper and lower arm in (5.8) and (5.9) can be rewritten as follows:

$$\mathbf{u}_{u(t_i)} = [\mathbf{S^T}_{x(t_i)}][\mathbf{V}_{cx(t_i)}] \qquad\qquad (5.10)$$

$$\mathbf{u}_{l(t_i)} = [\mathbf{S}^T{}_{x(t_i)}] [\mathbf{V}_{cx(t_i)}]$$
(5.11)

Note that, in equation (5.10) $x = 1, 2, \ldots n$ and in equation (5.11) $x = (n + 1), (n + 2), \ldots 2n$.

where $i = 1, 2, 3, \ldots j$, note that, similar to (5.1), equations (5.8) and (5.9) are also linear. Similarity in these equations (i.e. (5.1), (5.8) and (5.9)) allows applying the ERLS algorithm to the MMC arm voltage model easily. The only difference is to substitute $\mathbf{y}_{(t_i)}, z_{(t_i)}$ and $\boldsymbol{\theta}_{(t_i)}$ in equation (5.1) by total SM arm voltage ($\mathbf{u}_{u(t_i)}$ or $\mathbf{u}_{l(t_i)}$), switching states ($S_{x(t_i)}$) and SM voltage $\mathbf{V}_{cx(t_i)}$.

Since the ERLS algorithm is applied to the upper and lower arms independently, only the upper arm is described in this section.

To initiate the ERLS estimation algorithm as illustrated in table 5.2, $P_{(t_i)}$ (covariance matrix), λ and $\widehat{\mathbf{V}}_{cx(t_i)}$ (estimated SM voltage) must be specified with initial values of $P_{(t_0)}$, 0.851 and $\widehat{\mathbf{V}}_{cx(t_0)}$ respectively, in which:

$$P_{(t_0)} = GI$$
(5.12)

In (5.12), G is a constant positive number, (and it is preferable for G to be a large number [83]). In this implementation $G = 1 \times 10^3$ and I is an $n \times n$ identity matrix, where n is the number of SMs within the upper arm, whilst $\widehat{\mathbf{V}}_{cx}(t_0)$ is assumed to be zero (i.e. the capacitors considered initially uncharged).

After defining $P_{(t_0)}$ and $\widehat{\mathbf{V}}_{cx(t_0)}$, an adaptive gain $K_{(t_i)}$ is calculated based on the sequence implementation shown in table 5.2 as:

$$K_{(t_i)} = \frac{P_{(t_{i-1})} S_{x(t_i)}}{\left(S_{x(t_i)}^T P_{(t_{i-1})} S_{x(t_i)} + \lambda\right)}$$
(5.13)

The main idea of the proposed estimation algorithm is to minimise the error between the total measured arm SMs voltages ($\mathbf{u}_{u(t_i)}$) and their estimated values ($\widehat{\mathbf{u}}_{u(t_i)}$):

$$e_{\mathbf{u}(t_i)} = \mathbf{u}_{u(t_i)} - \widehat{\mathbf{u}}_{u(t_i)}$$
(5.14)

where $e_{\mathbf{u}_{(t_i)}}$ is the prediction error for the total voltage SMs of the upper arm. The cost function for the total arm voltage which identifies the weighted sum of the quadratic error is given by:

$$J_u = \sum_{i=1}^{j} \lambda^{j-i}(\mathbf{u}_{u_{(t_i)}} - \widehat{\mathbf{u}}_{u_{(t_i)}})^2 \tag{5.15}$$

To estimate the voltage value in one prediction step ahead, the previous voltage at t_{i-1} ($\widehat{\mathbf{V}}_{cx_{(t_{i-1})}}$) has to be included in the algorithm process as well as the error calculated in (5.14) multiplied by the adaptive gain ($K_{(t_i)}$) which has been calculated in (5.13). In the first initial step $\widehat{\mathbf{V}}_{cx_{(t_0)}} = \widehat{\mathbf{V}}_{cx_{(t_{i-1})}} = 0$, and therefore achieving this goal for the estimation of the upper capacitor voltages at t_i is realized as follows:

$$\widehat{\mathbf{V}}_{cx_{(t_i)}} = \widehat{\mathbf{V}}_{cx_{(t_{i-1})}} + K_{(t_i)} e_{\mathbf{u}_{(t_i)}} \tag{5.16}$$

The new covariance matrix ($P_{(t_i)}$) is then updated with $K_{(t_i)}$ as follows:

$$P_{(t_i)} = \left(\frac{1}{\lambda}\right)\left[\left(P_{(t_{i-1})}\right) - \left(\frac{P_{(t_{i-1})} S_{x(t_i)} S_{x(t_i)}^T P_{(t_{i-1})}}{\left(\lambda + S_{x(t_i}^T P_{(t_{i-1})} S_{x(t_i)}\right)}\right)\right] \tag{5.17}$$

For simplicity, the proposed algorithm steps are summarised in the flowchart shown in Fig. 5.3.

The block diagram of the proposed estimation topology, including the voltage-balancing algorithm for the upper arm, is shown in Fig. 5.4. For the lower arm of the converter, the same algorithms are processed. However, some rearrangements have to be considered. For example, in (6.13), (6.16) and (6.17) $x = n + 1, n + 2 ....2n$ instead of $x = 1,2 ... n$. It is worth noting that the sorting algorithm used in Fig. 5.4 is similar to that presented in [30], and it should be also noted that the voltage-balancing (i.e. the sorting algorithm) used in this thesis has nothing to do with the proposed estimation method. However, in the present research, achieving voltage-balancing relies on estimated voltages of the SM capacitors rather than their measured values. Therefore, sorting these voltages ($\widehat{\mathbf{V}}_{c1} \sim \widehat{\mathbf{V}}_{cn}$ and $\widehat{\mathbf{V}}_{c(n+1)} \sim \widehat{\mathbf{V}}_{c2n}$) is evaluated in descending order to charge and discharge the most desired capacitors; where the states of the capacitors (charging and discharging) depend on arm current direction. Therefore, monitoring the arm current is mandatory. Furthermore, phase disposition

sinusoidal pulse-width modulation (PD-*PWM*) strategy is used, where r carrier signals with the same phase and different levels are required for *N*-level. The voltage-balancing method used for the upper arm is shown in Fig. 5.5, where more details about the technique can be found in [30].

```
                    ┌─────────┐
                    │  Start  │
                    └─────────┘
                         │
                         ▼
              ╱─────────────────────╲
             ╱ Read total SMs voltages╲
             ╲   (upper and lower)    ╱
              ╲─────────────────────╱
                         │
                         ▼
             ┌──────────────────────┐
             │  Initiate: estimated │
             │ voltages, P(t_o), λ  │
             │    and i=0           │
             └──────────────────────┘
                         │
                         ▼
                 ┌───────────┐
                 │   i=i+1   │
                 └───────────┘
                         │
                         ▼
                 ┌───────────┐
                 │Calculate k(t_i)│
                 └───────────┘
                         │
                         ▼
                 ┌───────────┐
                 │Calculate errors in│
                 │   (5.14)  │
                 └───────────┘
                         │
                         ▼
              ╱─────────────────────╲
             ╱ Calculate estimated   ╲
             ╲ voltages from (5.16)  ╱
              ╲─────────────────────╱
                         │
                         ▼
                      ◇ i = j ◇
```

Fig 5.3 flow chart elements: Start; Read total SMs voltages (upper and lower); Initiate: estimated voltages, $P_{(t_o)}$, λ and i=0; i=i+1; Calculate $k(t_i)$; Calculate errors in (5.14); Update $P_{(ti)}$; Calculate estimated voltages from (5.16); i = j — No / Yes; End.

Fig 5.3. Flow chart of the proposed SM voltage estimation method for the upper arm.

As a result, PWM_n and $PWM_{\bar{n}}$ will be applied to the converter with a unit delay (Z^{-1}) in order to activate S_n and $\bar{S}_n$, respectively in the appropriate time. A dead-

time period is added to $PWM_{\bar{n}}$ before switching $\bar{S}_n$. In consequence of a very small voltage drop caused when S_n and $\bar{S}_n$ are activated, it is assumed that $PWM_n = S_n$ and $PWM_{\bar{n}} = \bar{S}_n$.
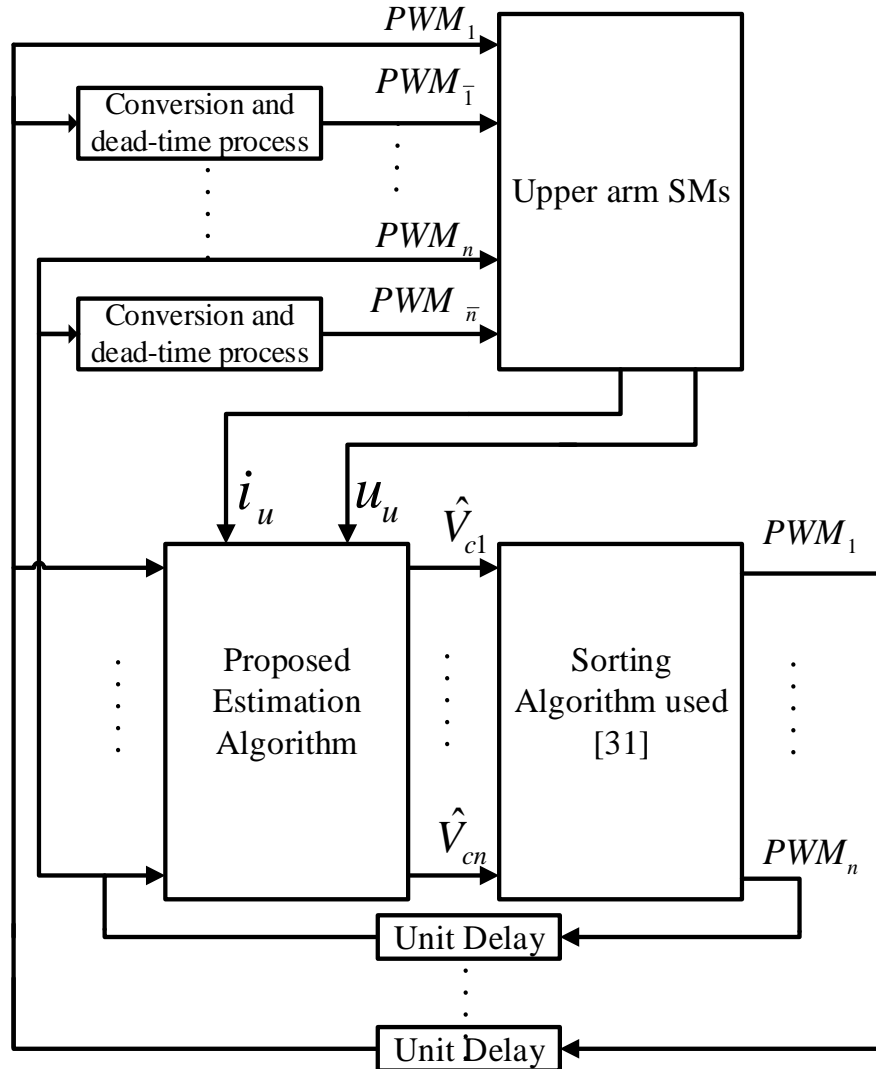
Fig 5.4. The proposed estimation method and the associated sorting algorithms for the upper arm control.

Reference signal

Carrier based on PD-*PWM*

Number of the SMs to be involved for the upper arm process

$\hat{V}_{c1} \sim \hat{V}_{cn}$

i_u

Sorting mechanism of all upper SMs

When i_u is positive choose the lowest value of $\hat{V}_{cn}$ and choose the highest value of $\hat{V}_{cn}$ when i_u is negative

PWM signals
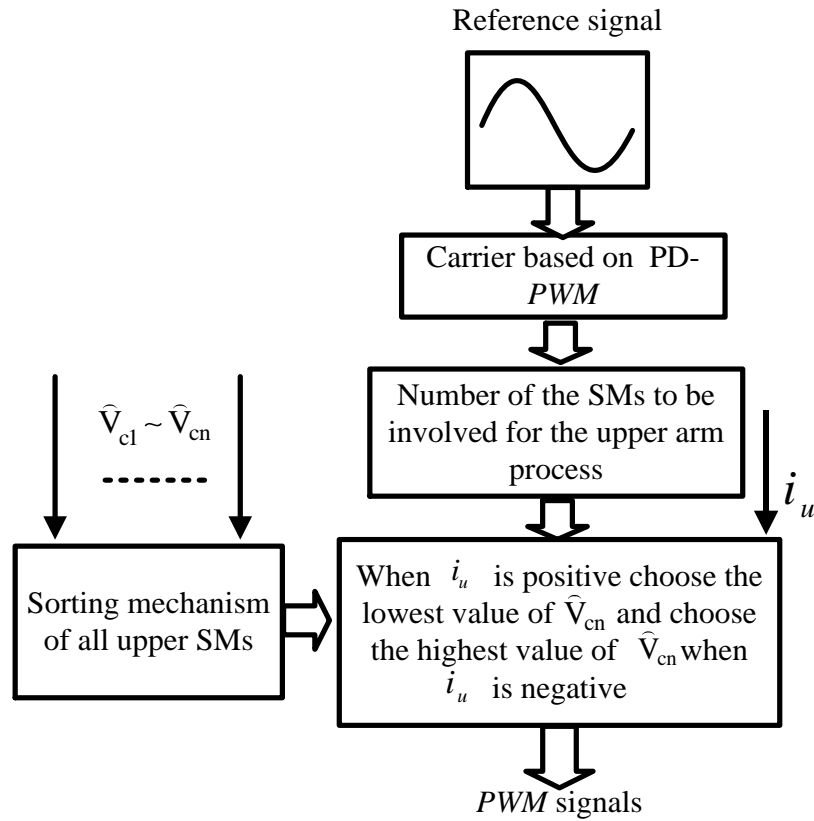
Fig 5.5. Block diagram of the upper arm voltage-balancing strategy used.

5.6 Simulation Results

In order to verify the proposed estimation scheme for the MMC, a single-phase 9-level MMC is considered and simulated. Eight SMs per arm ($x = 16$) are used to construct this converter and only one voltage sensor for each arm is used. The system parameters are tabulated in table 5.3.

5.6.1 Conventional RLS Results

Although it has been mentioned earlier in this chapter that the conventional RLS scheme is not suitable for the MMC; however, giving a proof and showing the sequence of all of the mentioned methods might give a sense of what can be done in the future to improve the existing study.

In this part of the simulation study, only the voltage across C_1 (V_{c1}) is investigated. As expected, the error between the measured and estimated voltage is high and

unacceptable, as shown in Fig. 5.6. However, the estimated value still follows the real signal ($V_{c1(\textbf{Measured})}$), and this tracking encourages the belief that developments of the conventional RLS might provide a solution.

Table 5.3 Parameters of the simulated 9-level single-phase MMC

Parameter	Value
SM capacitor (C)	2000 μF
Modulation index (m_i)	0.80
DC-link voltage (V_{dc})	10 kV
Output frequency (f)	50 Hz
Carrier switching frequency (f_c)	2.5 kHz
Number of SM per leg (N)	16
Load resistor (R)	33 Ω
Arm inductor (L_S)	1.2 mH
Load inductor (L)	15 mH
Sampling frequency ($f_{sampling}$)	20 kHz
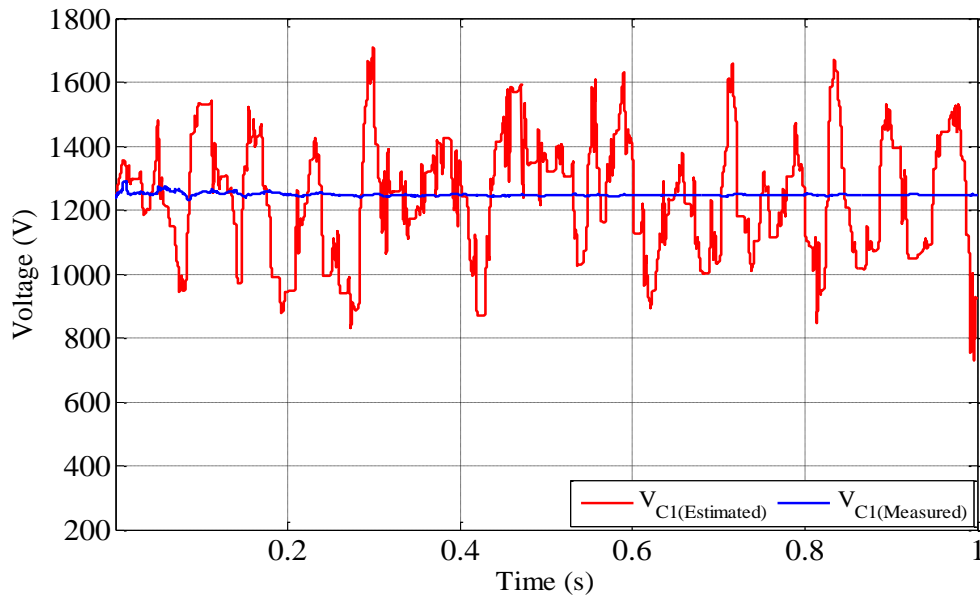
Fig 5.6. Simulation results of the 9-level MMC with the conventional RLS scheme.

5.6.2 ERLS Results

The effectiveness of the proposed technique is confirmed by different simulation results which include steady-state and dynamic condition analyses as discussed in the following cases.

5.6.2.1 The Performance of the Proposed Method for Normal Operating Conditions.

In this case the performance of the 9-level MMC is evaluated under normal steady-state operating conditions, where the converter is assumed to work with a constant R-L load. Voltage sensors are used for each SM at first to measure the capacitor voltages as shown in Fig. 5.7 (a)-(c). The performance of the converter with the proposed method is illustrated in Fig. 5.8 (a)-(c). Owing to a small error between the measured and estimated voltages, voltages across the upper arm capacitors in Fig. 5.8 (a) show extra deviation compared to those presented in Fig. 5.7 (a). However, this small difference between the two signals does not have any notable effect on the converter output voltage and current as can be clearly seen from Fig. 5.8 (b), and (c). This confirms the accuracy of the proposed technique. Moreover, it should also be noted that the sensor-based measurement technique requires 16 voltage sensors for the 9-

level MMC, while the proposed measuring technique needs only two voltage sensors to achieve voltage-balancing of the converter.

The voltage across capacitors in the simulation results for this chapter and next chapter appeared to be different from what is in the literature due to the converter was designed with the aim of using the smallest size of the SM capacitors possible.
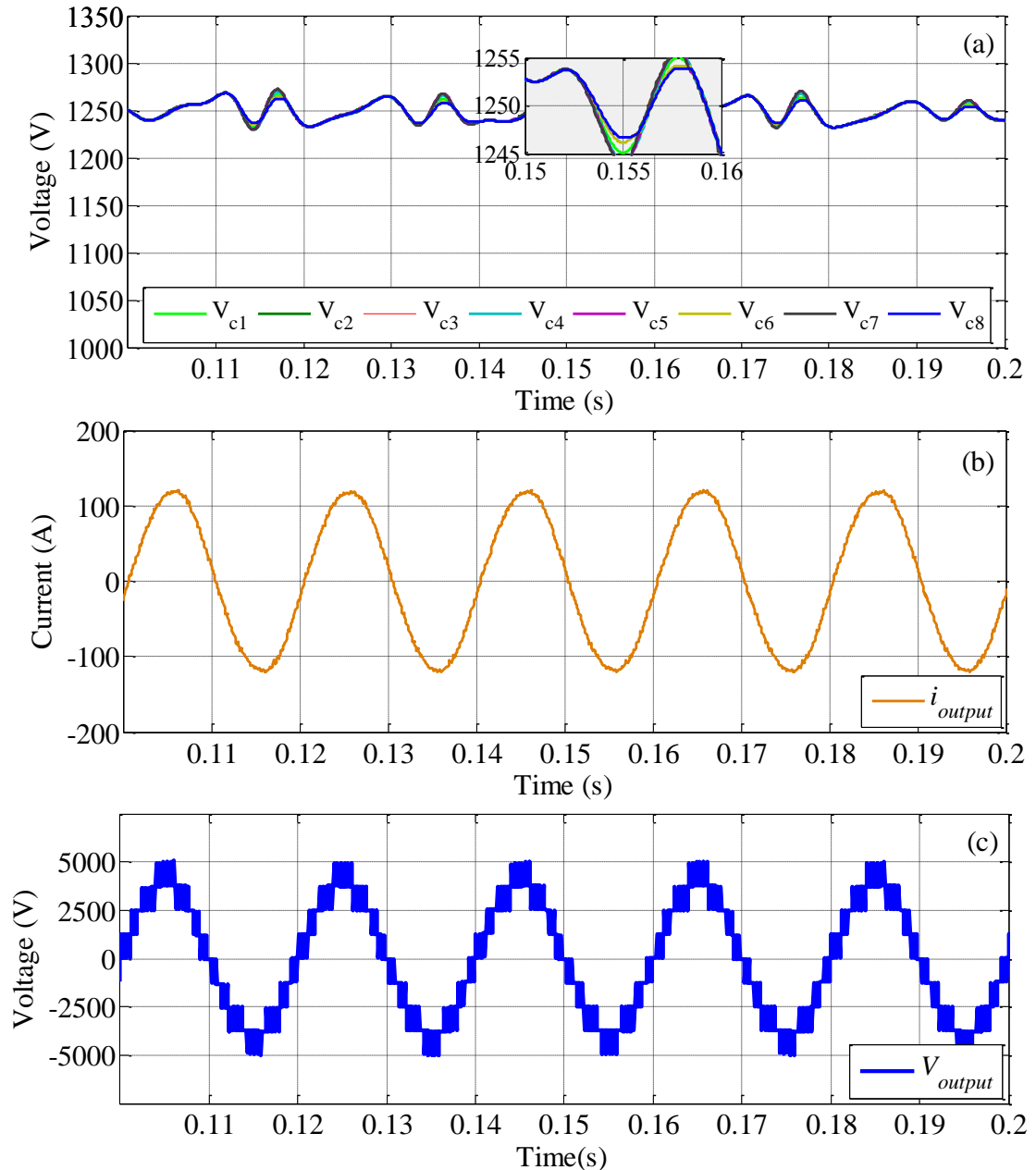
Fig 5.7. Simulation results of the 9-level MMC with the sensor-based measuring technique. (a) Upper capacitor voltages (V_{C1} ~ V_{C8}). (b) Output current. (c) Output voltage.
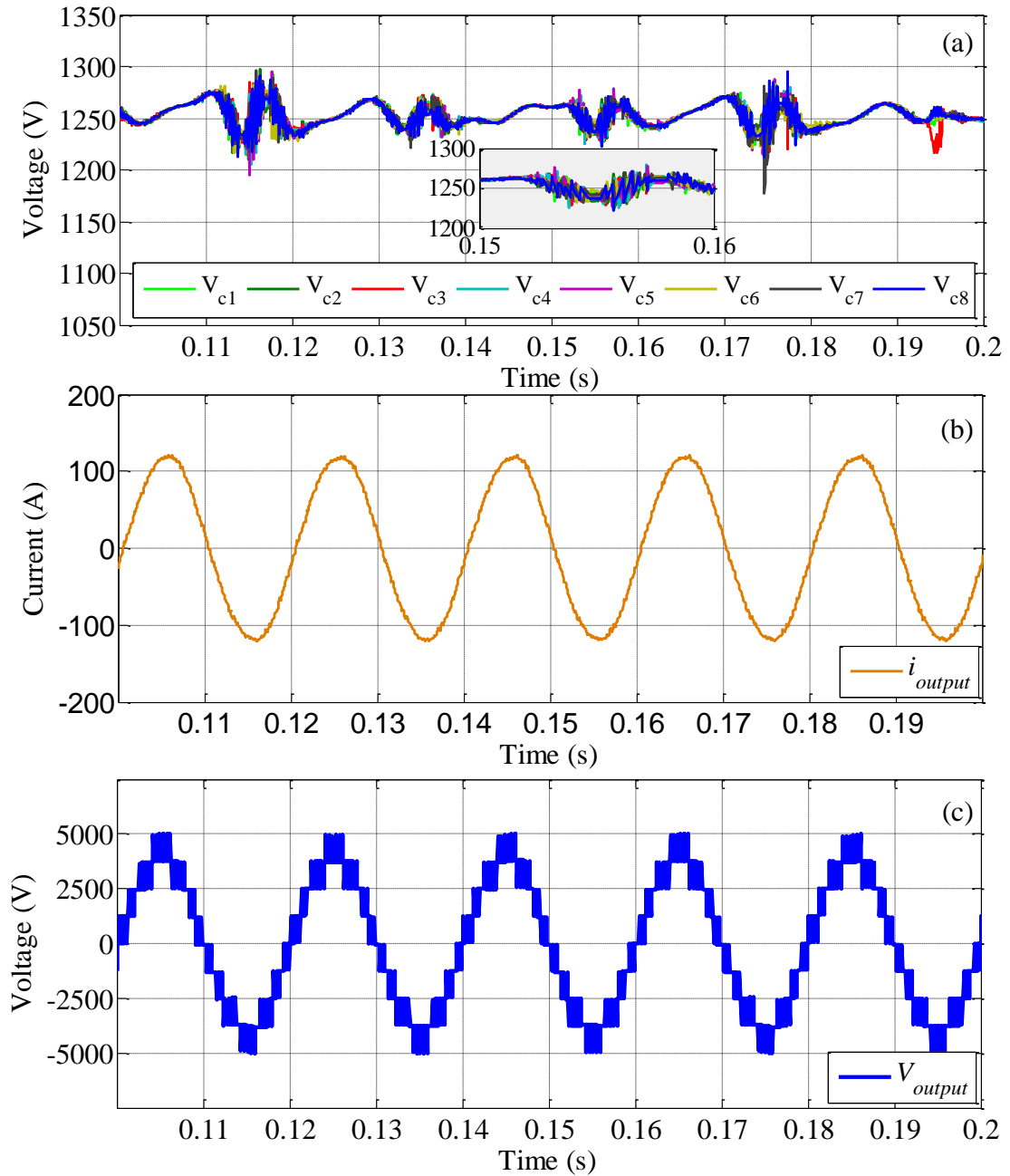
Fig 5.8. Simulation results of the 9-level MMC with the proposed estimation scheme and nominal parameters (a) Upper capacitor voltages (V_{C1} ~ V_{C8}). (b) Output current. (c) Output voltage.

5.6.2.2 Performance of the Proposed Method with Capacitance Deviation

To further validate the effectiveness of the proposed scheme, due to an expected manufacturer tolerance in the capacitor value, deviations in SMs capacitance are considered in this case. Extensive simulation studies with wide range of variations in

SM capacitance are carried out to illustrate the robustness of the proposed method in estimating the capacitor voltages. In this case, C_1 with different deviations (i.e. ±22%, ±40%, and ±70%) is selected as an example.
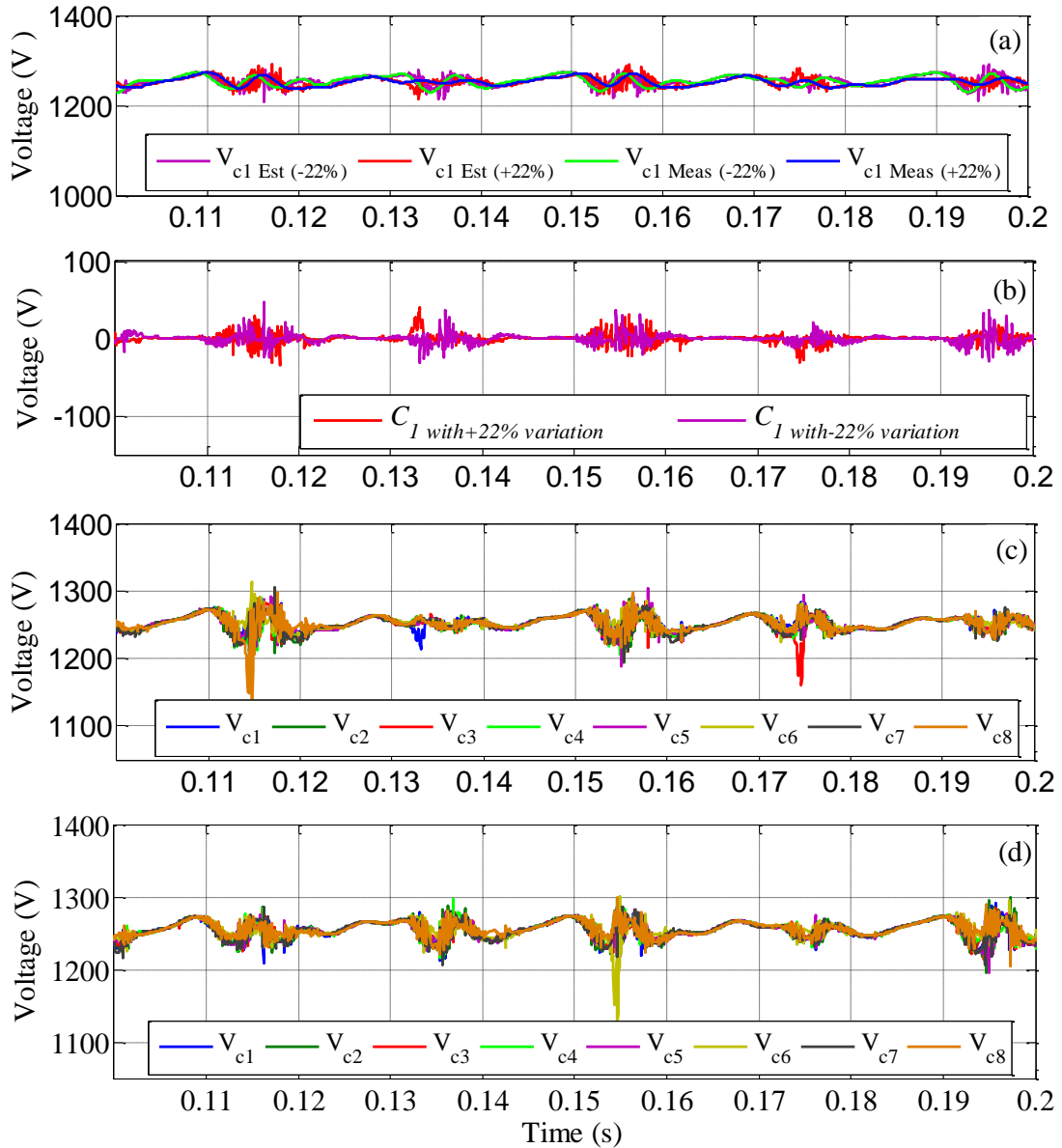
Fig 5.9. Simulation results of the upper arm capacitor errors with variations in all capacitors. (a) Measured and estimated voltage across C_1 with ±22% variations. (b) Errors between the measured and estimated voltage values when C_1 variations are ±22%. (c) Estimated voltages for ($C_1 \sim C_8$) where the capacitors values are : 2440 μF ,1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively. (d) Estimated voltages for ($C_1 \sim C_8$) where the values are : 1560 μF ,1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively.

The other capacitors $C_2 \sim C_8$ are also given different deviation values to emulate the close to reality situation where all capacitors possibly deviate from their nominal values.
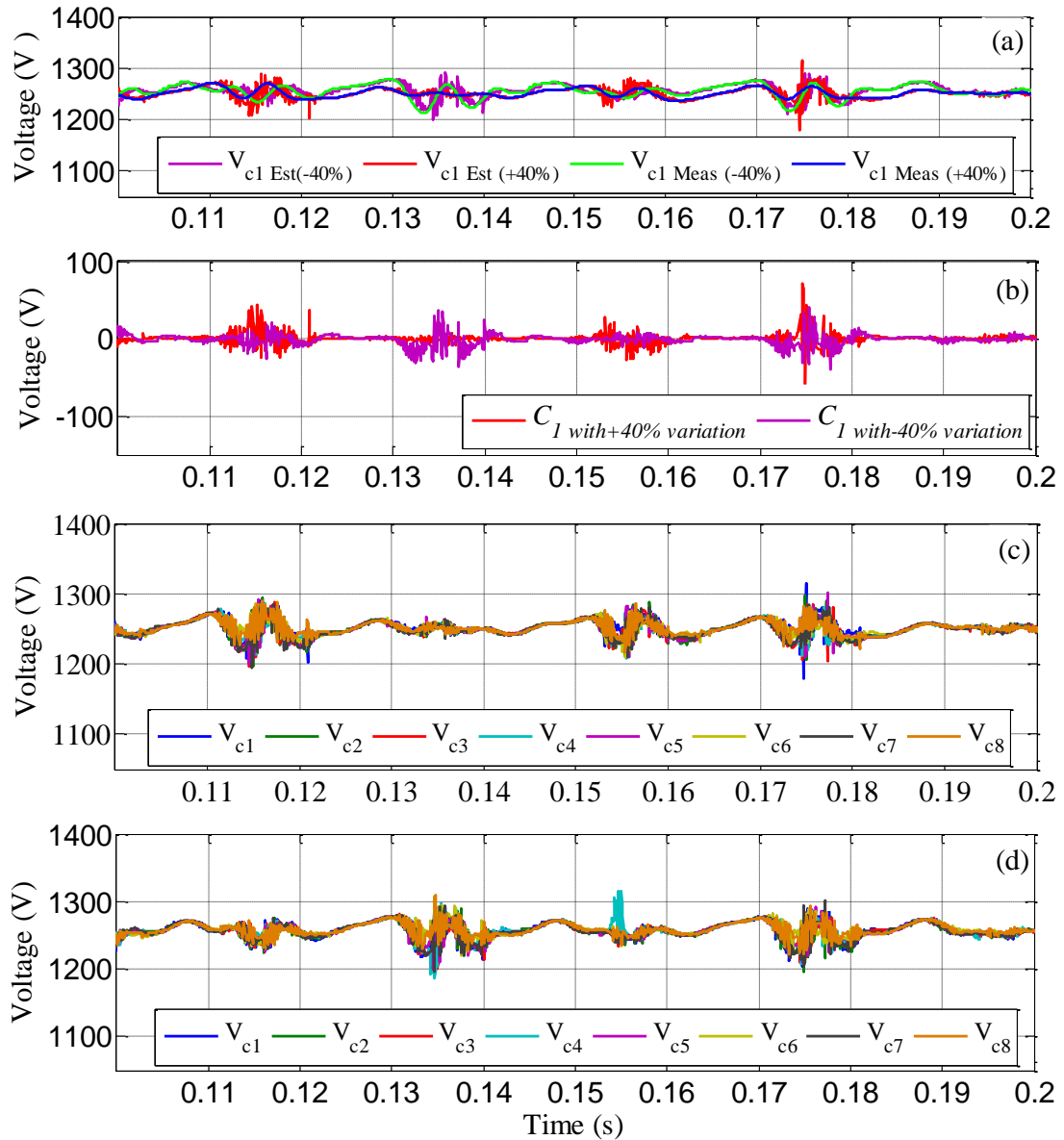
Fig 5.10. Simulation results of the upper arm capacitor errors with variations in all capacitors. (a) Measured and estimated voltage across C_1 with ±40% variations. (b) Errors between the measured and estimated voltage values when C_1 variations are ±40%. (c) Estimated voltages for ($C_1 \sim C_8$) where the capacitors values are : 2800 μF ,1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively. (d) Estimated voltages for ($C_1 \sim C_8$) where the values are : 1200 μF, 1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively.

For $C_2 \sim C_8$ the deviations considered are: -25%, -12%, +7%, -16%, +40%, -30%, and +50%, which results in the values of $C_2 \sim C_8$ as: 1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF, respectively.
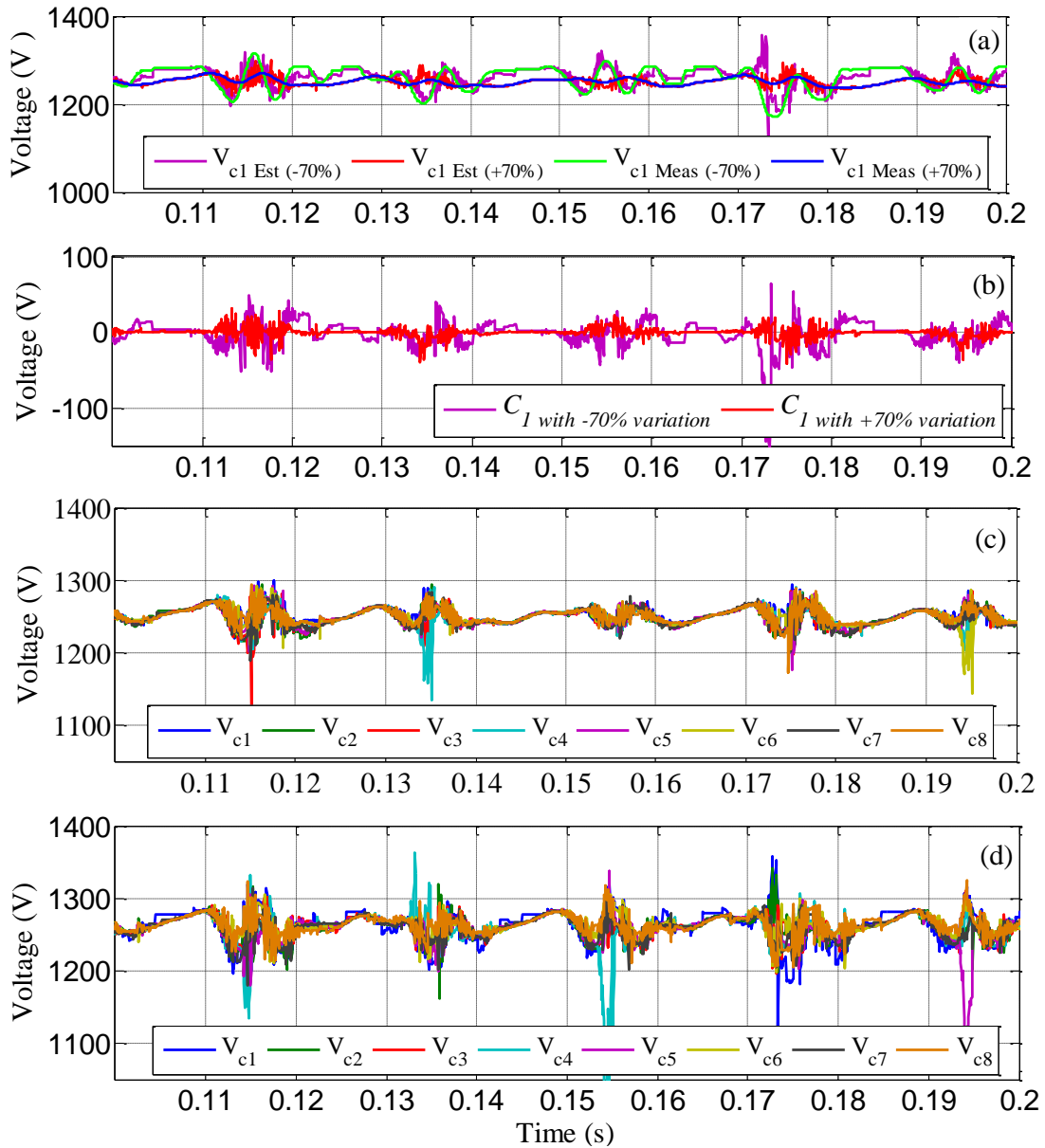
Fig 5.11. Simulation results of the upper arm capacitor errors with variations in all capacitors. (a) Measured and estimated voltage across C_1 with ±70% variations. (b) Errors between the measured and estimated voltage values when C_1variations are ±70%. (c) Estimated voltages for ($C_1 \sim C_8$) where the capacitors values are : 3400 μF ,1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively. (d) Estimated voltages for ($C_1 \sim C_8$) where the values are : 600 μF, 1500 μF, 1760 μF, 2140 μF, 1680 μF, 2800 μF, 1400 μF, and 3000 μF respectively.

Fig. 5.9(a) shows the measured and estimated voltages across C_1 where $\pm22\%$ deviation are considered, four signals ($\mathbf{V}_{c1}$ estimated / measured with $+22\%$ deviations and $\mathbf{V}_{c1}$ estimated / measured with -22%) are illustrated in the figure.

In Fig. 5.9(b), it can be noted that the maximum error when C_1 has variations of $\pm22\%$ is almost 3% only. The effect of $\pm22\%$ deviation of C_1 in addition to the deviations of $C_2 \sim C_8$ on the all arm capacitor, are illustrated in Fig. 5.9(c) and (d) respectively. The maximum error can be seen in Fig. 5.9(c) and (d) is around 8%. As can be noted from the figures (Fig. 5.9(c) and (d)), the maximum error appears when the deviation considered for C_6 and C_8 were 40% and 50%. However, in the real capacitors it is unlikely to have such deviations.

Furthermore, when the capacitor (C_1) has a tolerance of $\pm40\%$, the maximum error can be noticed is almost less than 4% as depicted in Fig. 5.10(b). Interestingly, the error remains minimal even when all other capacitors ($C_2 \sim C_8$) deviated too as shown in Fig. 5.10(c) and (d). These results strongly suggest that the proposed method is suitable for real implementations where the manufacturing tolerance of the capacitors usually does not exceed $\pm20\%$ of their nominal values.

It is worth noting that the reason for these errors being so small is that the proposed estimation method does not involve the capacitance parameter in its algorithm process, as can be seen from equation (5.10) and (5.11). When a larger variation of $\pm70\%$ is considered, the error can reach 12% as shown in Fig. 5.11(b). However, in real implementations, it is unlikely that such large capacitance deviations (i.e. $\pm70\%$) would occur.

5.6.2.3 Performance of the Proposed Method during Step Load Change

The performance of the proposed method is now examined for a step change in load. In this study, voltage across C_1 ($\mathbf{V}_{c1}$) is selected as an example. As depicted in Fig. 5.12, the load is increased by 100% at time t= 0.3s and back to the original load at t = 0.4s. Remarkably, in both cases; the estimated voltage value ($\widehat{\mathbf{V}}_{c1}$) perfectly tracks the measured voltage, as demonstrated in Fig. 5.12 (b).
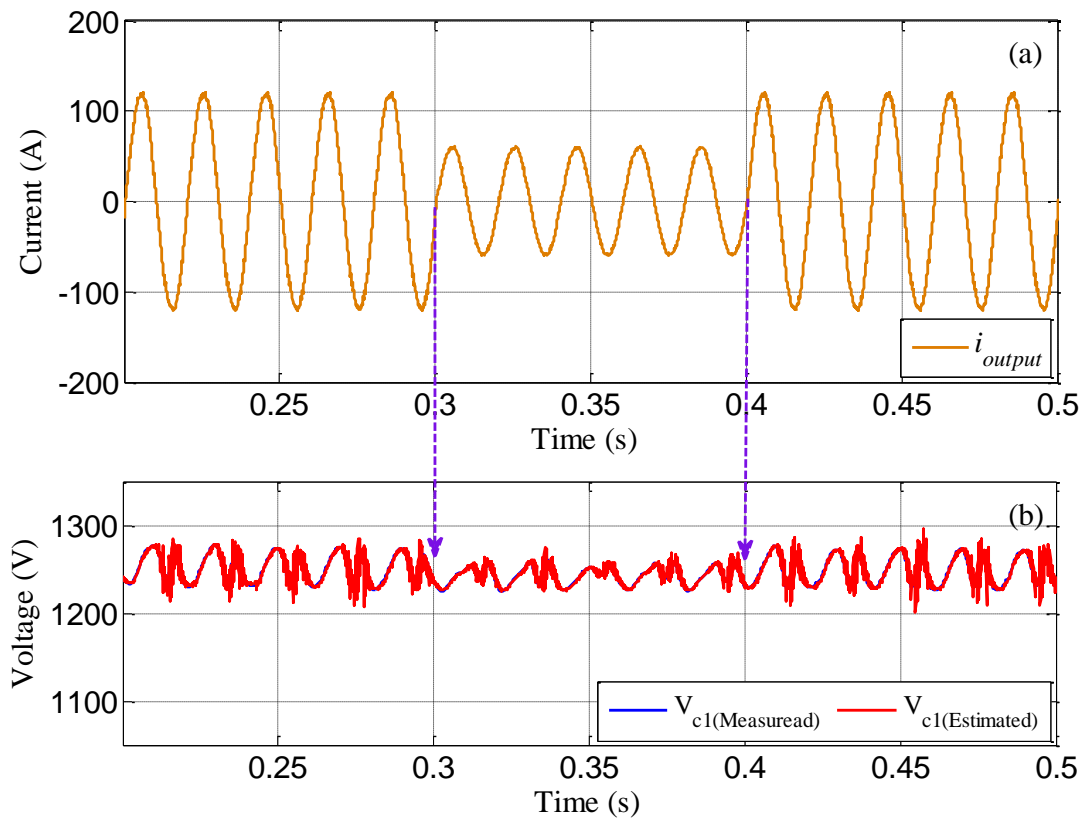
Fig 5.12. Simulation results for the 9-level MMC with step load change. (a) Output current. (b) Upper arm capacitor voltages across C_1.

5.6.2.4 Start-up and Low Carrier Switching Frequency Performance.

In this part of the simulation study, start-up performance and operation with different low carrier switching frequencies are investigated.
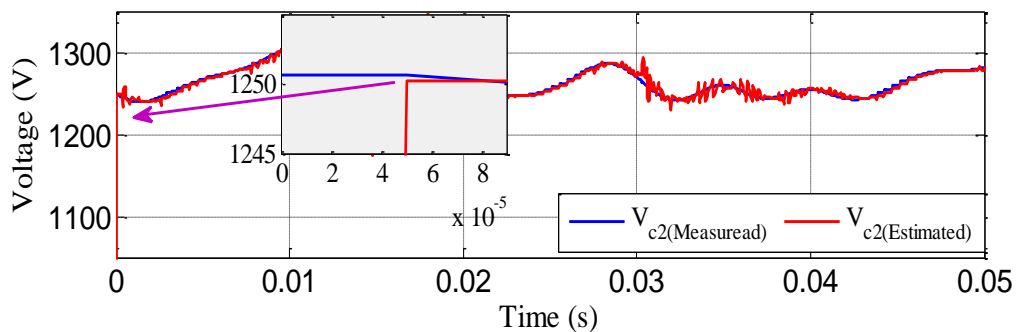
Fig 5.13. Start-up transient condition performance of the proposed estimation method / simulation results.

Fig. 5.13 shows the performance of the proposed estimation method during the start-up transient condition. It is clear that the proposed ERLS algorithm tracks the measured voltage very quickly; only one sampling time ($\frac{1}{f_{sampling(20\,k\,Hz)}} = 5 \times 10^{-5}$) is required to start tracking the measured value.
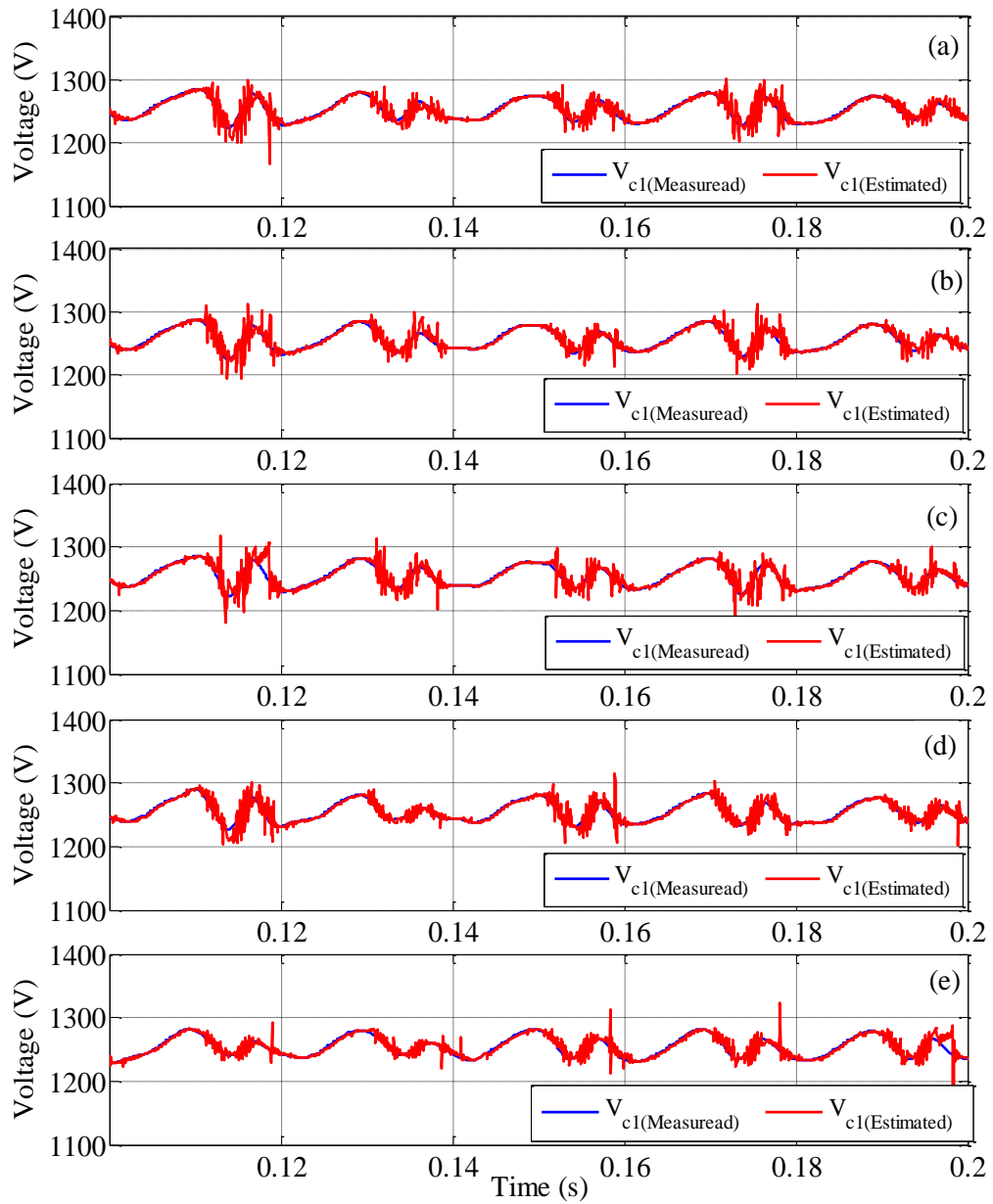
Fig 5.14. Effect of the carrier switching frequency on the proposed estimation method. (a) f_c =2.5 kHz. (b) f_c =1.5 kHz. (c) f_c = 750 Hz. (d) f_c = 250 Hz. (e) f_c = 45 Hz / simulation results.

Due to the possibility of the MMC to work on low switching frequency when a different voltage-balancing control method is used, a further investigation with different frequencies values are performed in Fig. 5.14. Five carrier switching frequencies are evaluated respectively: f_c = 2500, 1500, 750, 250 and 45 Hz. It can be noted that for the all cases, the proposed algorithm performs well even with a carrier switching frequency lower than the fundamental frequency (i.e. when f_c =45 only).

5.6.2.5 Performance of the Proposed Method during DC Fault.

A fault is applied to the system to further validate the method where the DC voltage of the converter is dropped suddenly by 90%. Fig. 5.15(a) and (b) show the corresponding changes in the output current and voltage when the estimation method is used.
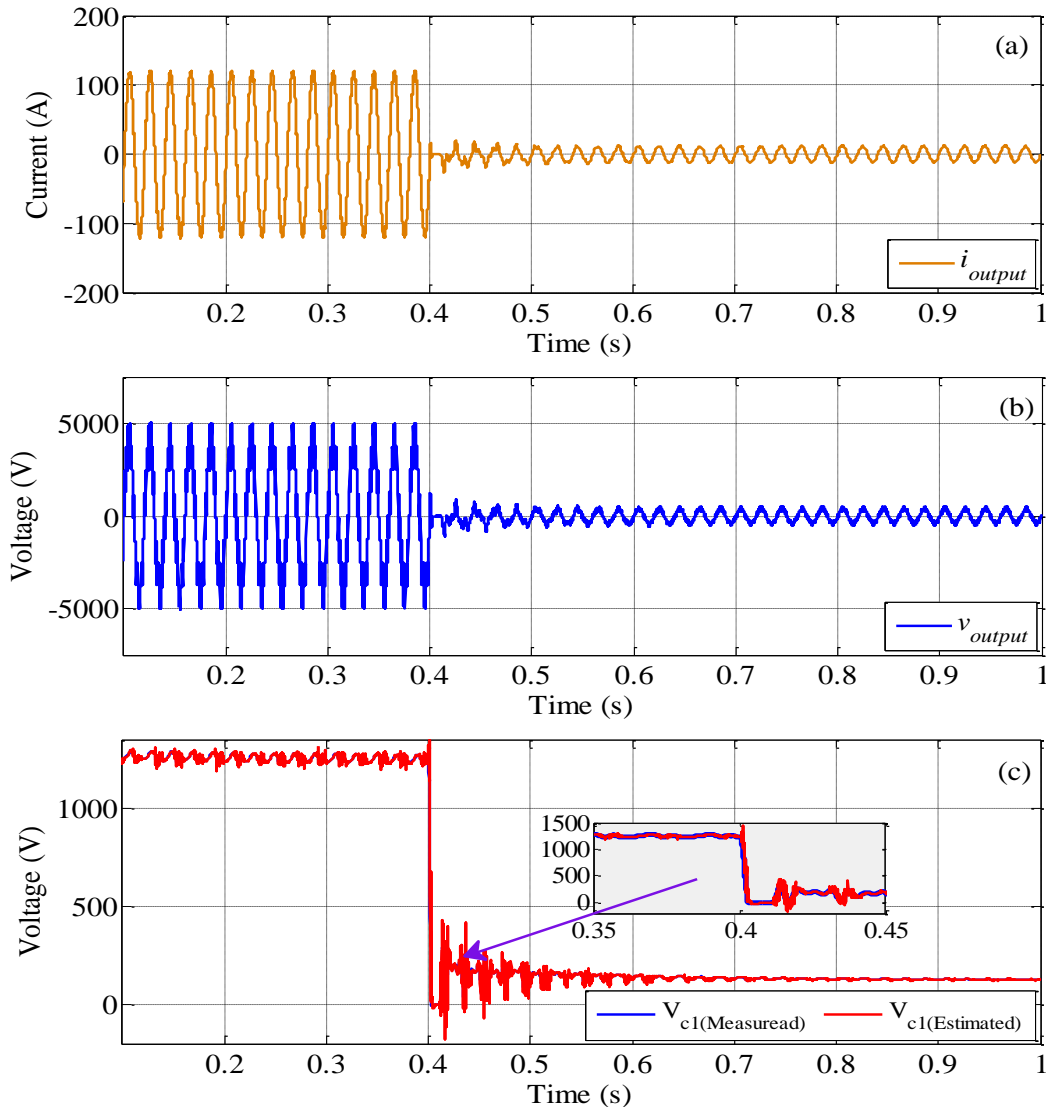
Fig 5.15. Simulation results of the performance of the proposed method during a DC fault. (a) The output current response. (b) The output voltage response.

In addition, Fig 5.15(c) shows the measured and estimated voltage across C_1. It is obvious that the estimated voltage can successfully track this extreme change in both transient as well as steady state conditions.

5.6.2.6 The Performance of the ERLS Method with a High Number of SMs

In this section of the analysis results, the proposed method is applied to a high MMC level and evaluated. Fig 5.16-18 show the performance of the proposed method with 32, 64 and 204 SMs per leg.
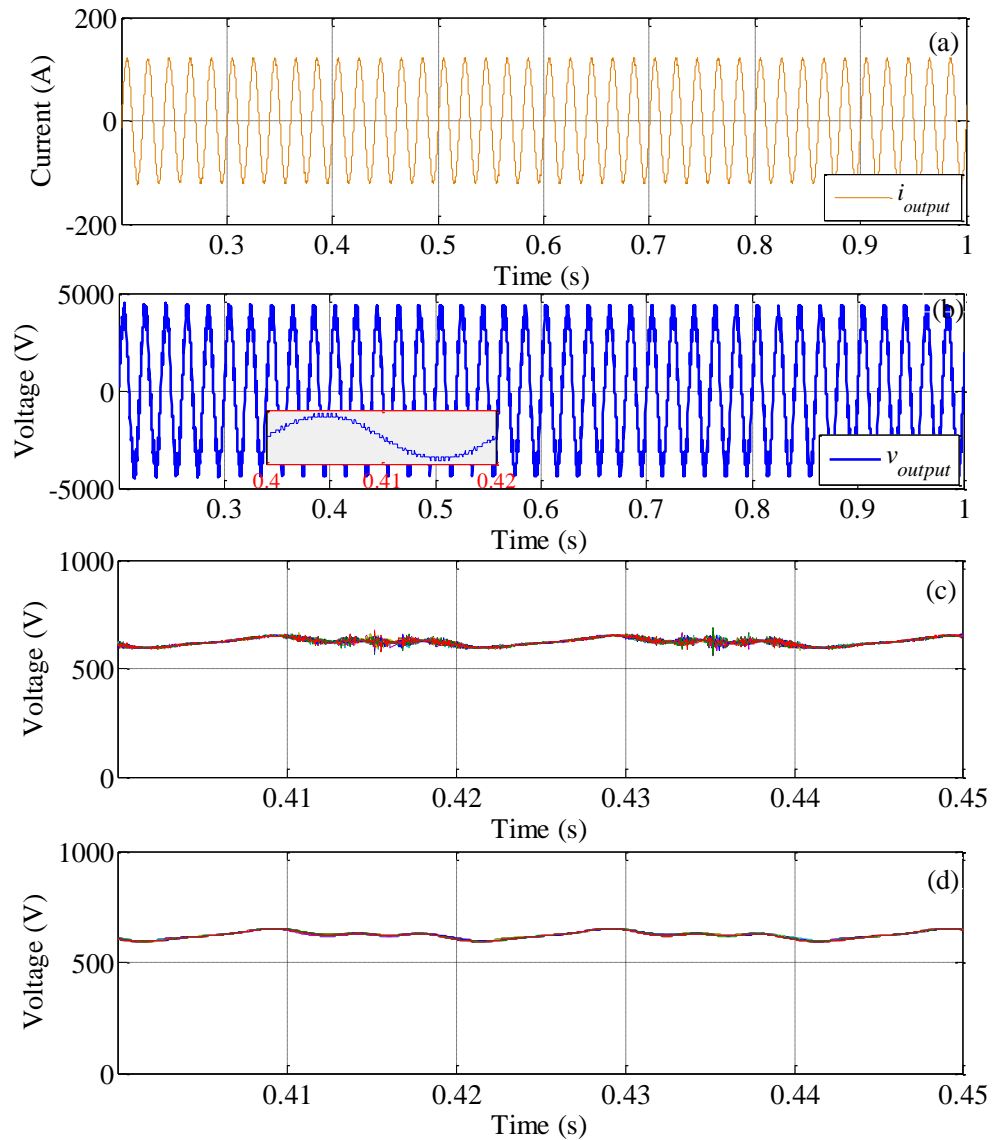
Fig 5.16 Simulation results of the performance of the proposed method with 32 SMs per leg ($f_{sampling}$=35 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor voltages $\widehat{V}_{c1} \sim \widehat{V}_{c16}$. (d) Upper capacitor voltages $V_{c1} \sim V_{c16}$.

It is clear from the figures that all simulated levels performed well which once again confirms the proposed scheme; however, the required sampling frequency is proportional to the level required which may affect computation time. This can be addressed with more an advanced and powerful processor.
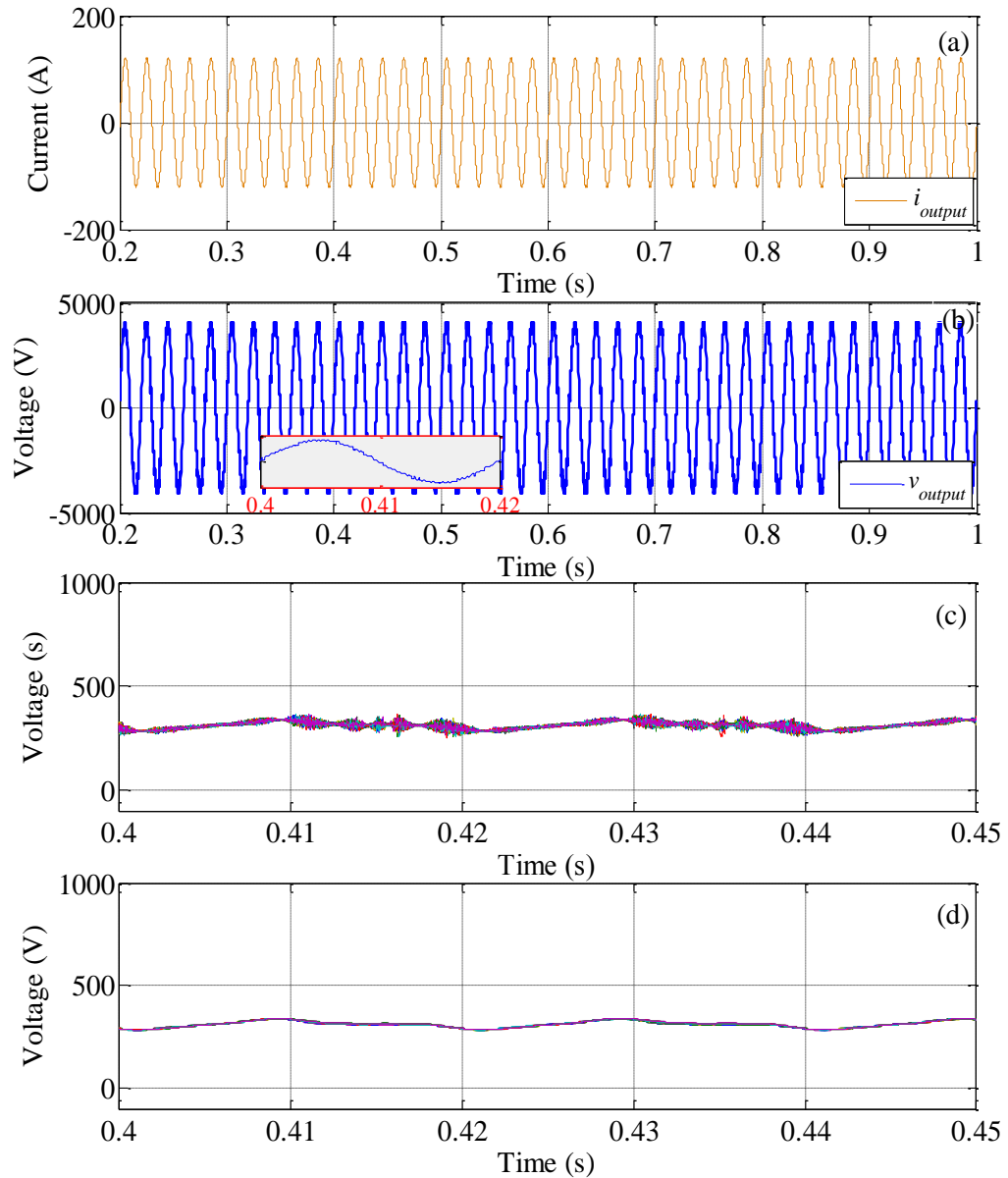
Fig 5.17 Simulation results of the performance of the proposed method with 64 SM per leg ($f_{sampling}$< 50 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor voltages $\widehat{V}_{c1} \sim \widehat{V}_{c32}$. (d) Upper capacitor voltages $V_{c1} \sim V_{c32}$

Alternative, more sensors can be added within each arm based on the same connection arrangement described earlier in 5.6. For instance, technologies with parallel processing capabilities such as FPGA boards are a very attractive and cost-effective alternative parallel processing which can reduce computation time by processing independent calculation concurrently.
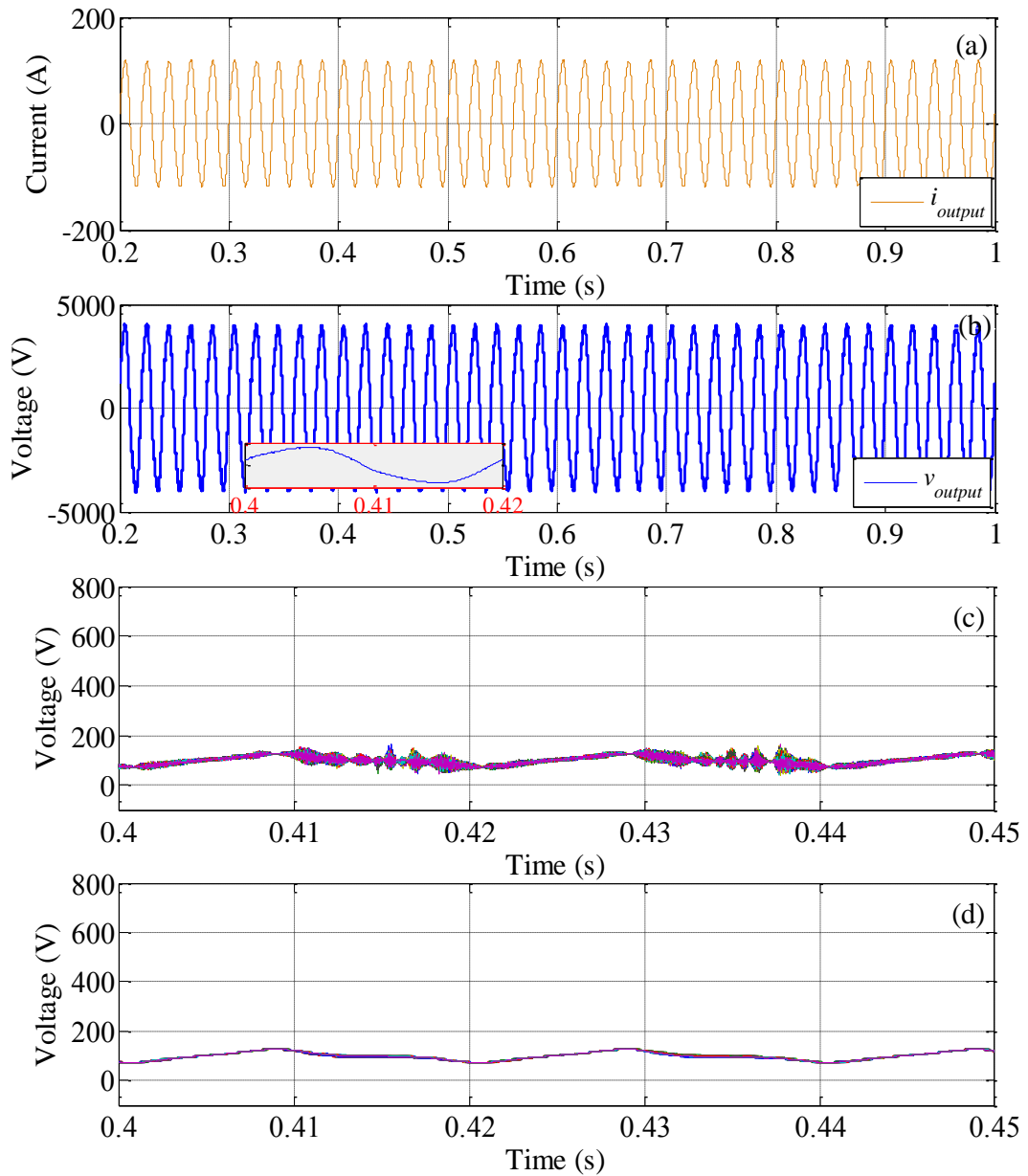
Fig 5.18 Simulation results of the performance of the proposed method with 204 SM per leg ($f_{sampling}$=250 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor voltages $\widehat{V}_{c1} \sim \widehat{V}_{c102}$. (d) Upper capacitor voltages $V_{c1} \sim V_{c102}$

It should note that the MMC is commonly used for lower SM based-applications where the required SMs is around 10 SM per leg only. For example, drive applications presented in [73-75] require 30 voltage sensors if a sensor-based method is used whereas with the proposed method only requires 6 sensors to achieve system stability.

5.7 Experimental Results

To further validate the proposed method, extensive experimental test are carried out in this section. As mentioned in Chapter 3, a scaled down 4-level MMC system with the pre-mentioned parameters are used to evaluate the proposed estimation technique. Five main points are investigated here; the effect of SM voltage drop on the system's model; the performance of the MMC in normal operating conditions; the effect of a load step change on converter performance where the proposed method is applied; the effect of a fault in the DC source on the estimation value; and finally an extreme increase in DC voltage.

5.7.1 Impact of Voltage Drop on the System Model

Realistically there will always be some deviations between ideal and practical systems caused by various factors. The voltage drop due to the internal resistance of the semiconductor devices ($S_{x\,drop}$) and the stray impedance of the connecting wires ($V_{Line\,x\,drop}$) are two examples. To experimentally validate the assumption made earlier that this voltage drop has a minimal effect on the performance of the proposed method and can be ignored; equation (5.10) is experimentally implemented as example and the result is shown in Fig. 5.19. This was accomplished using External MATLAB mode, where the data inside the DSP can be accessed in real-time processing. As it can be clearly seen from Fig. 5.19, there is a very small difference between the two signals (blue and red), which is caused by the practical aspects explained above. This therefore confirms the assumption made earlier that these voltage drops can be safely neglected in the calculation without having a significant impact on the system model. However, for a more accurate formula of the four-level MMC, equation (5.10) can be rewritten as follows:

$$\mathbf{u}_u = S_1 * V_{c1} + S_{1\,drop} + V_{Line\,1\,droop} + \cdots + S_3 * V_{c3} + S_{3\,drop} + V_{Line\,3\,drop} \quad 5.18)$$

Note: see Fig 5.2 for the $V_{Line\,n\,droop}$
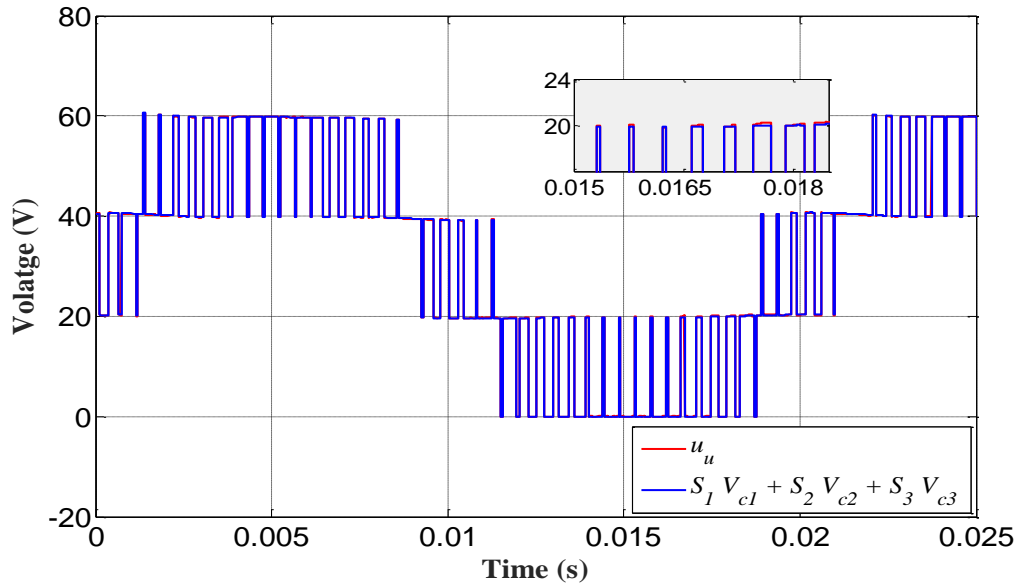
Fig 5.19. Experimental results for measured (u_u) and calculated $S_1V_{c1} + S_2V_{c2} + S_3V_{c3}$ total upper arm voltage.

For the lower arm, it should be noted that a similar equation can be written for $\mathbf{u}_l$, Fig. 5.20 illustrates $\mathbf{u}_u$ in comparison with the total lower arm voltage $\mathbf{u}_l$ and the output voltage $\mathbf{u}_a$.
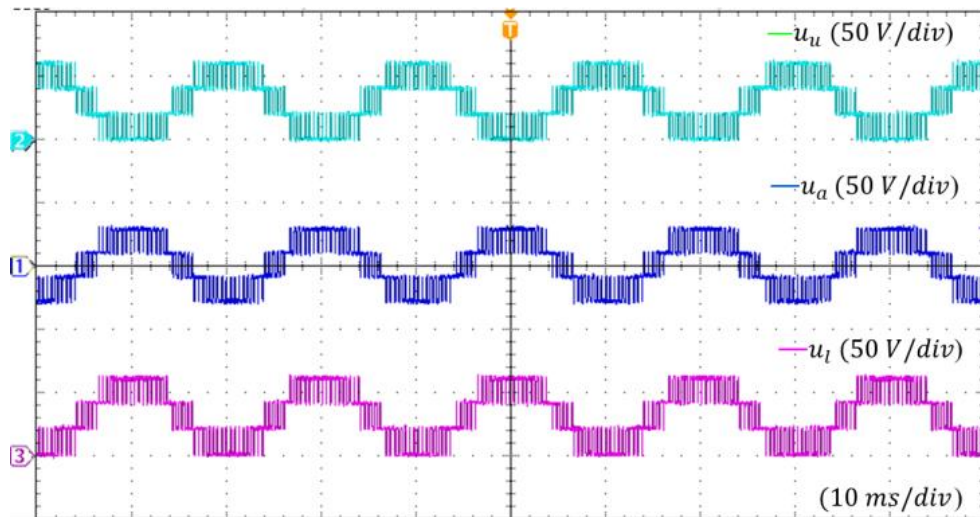
Fig 5.20. Total upper arm voltage ($\mathbf{u}_u$), output voltage ($\mathbf{u}_a$) and lower arm voltage ($\mathbf{u}_l$) / Experimental results.

5.7.2 Steady-State Condition Results

Experimental results of the sensor-based measurement and the proposed technique based on the steady-state condition are presented in Figs. 5.21 and 5.22. Figs. 5.21 (a) and 5.22 (a) show the three upper SM capacitor voltages ($\mathbf{V}_{c_1} \sim \mathbf{V}_{c_3}$). It can be observed that Fig 5.22 (a) shows a slight deviation in comparison with Fig. 5.21 (a). However, this does not have a notable impact either on the output current or on the output voltage as illustrated in Fig. 5.22 (b).
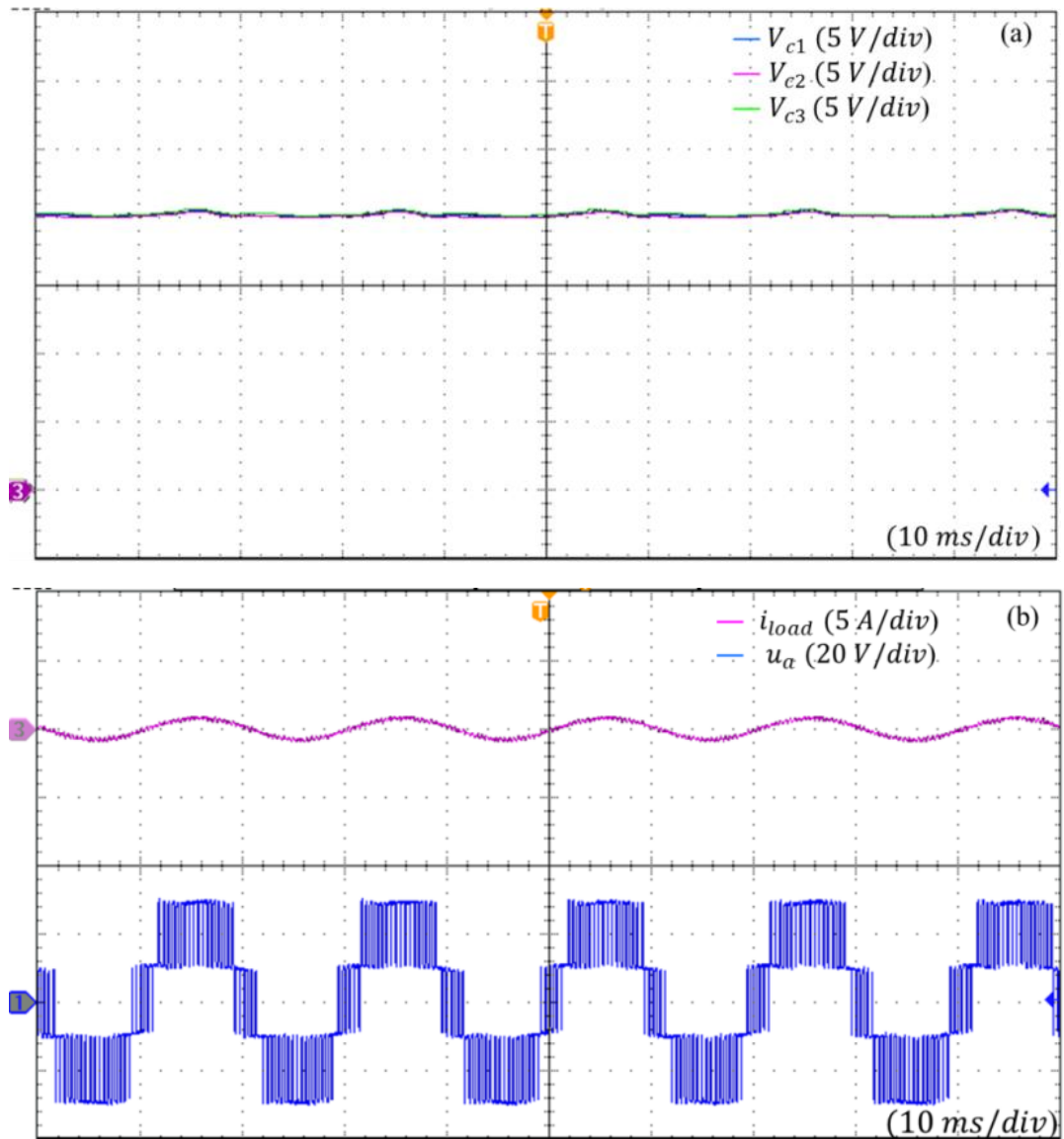
Fig 5.21. Experimental results of the sensor-based estimation method. (a) Three upper SM voltage capacitors. (b) Output current and voltage.

Interestingly, zoomed-in samples of Fig 5.21 (b) and 5.22 (b) verify this; however, only very small differences in the voltage waveforms can be observed as shown in Fig. 5.23, which is acceptable for the reduction in sensors count. Furthermore, with the proposed scheme, the same number of two sensors is sufficient to achieve voltage-balancing for even the N-level MMC. Additionally, comparison between the voltage across C_1 achieved from the conventional sensor-based method and the proposed estimated method is illustrated in Fig. 5.24.
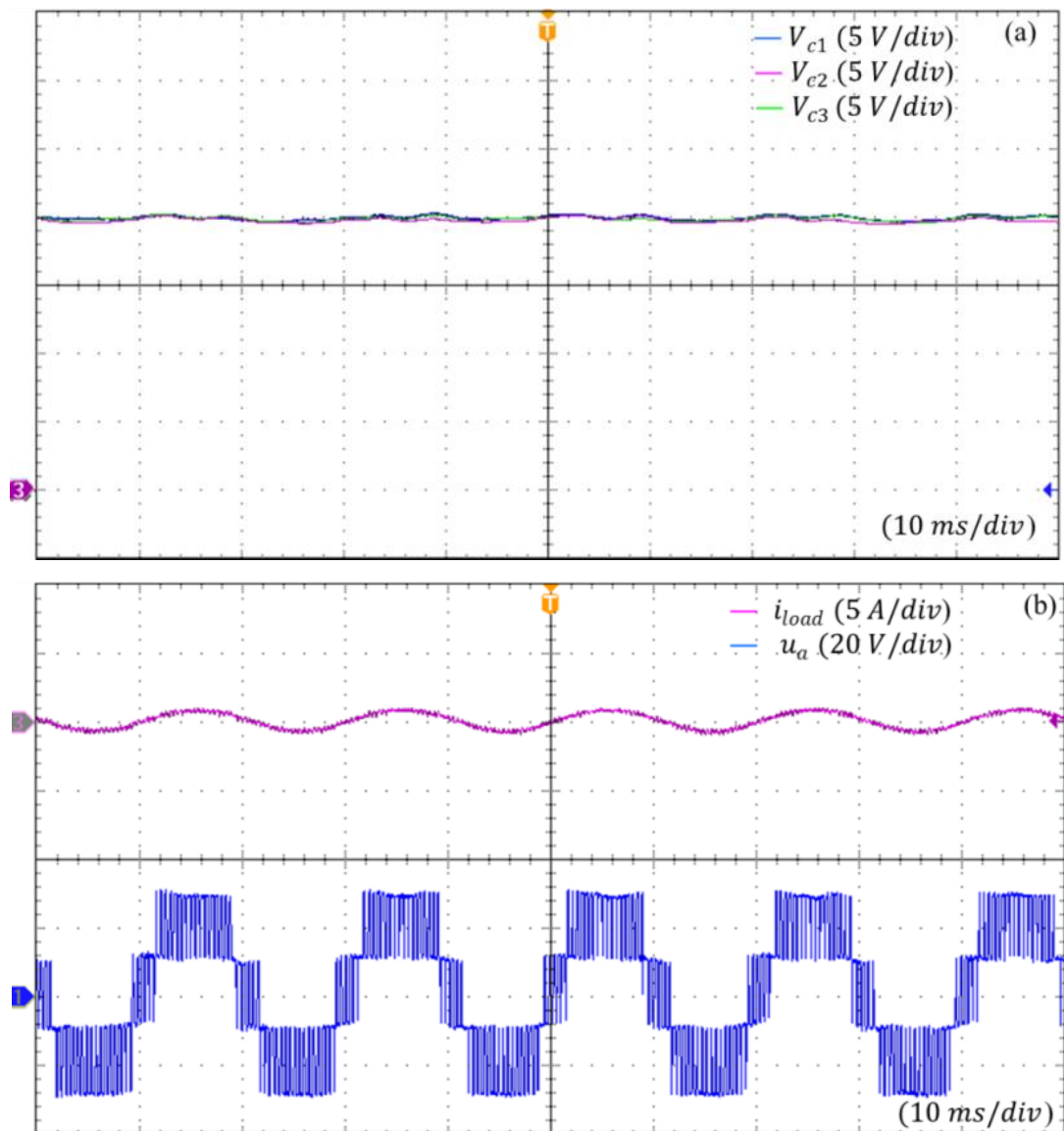
Fig 5.22. Experimental results of the proposed estimation method. (a) Three upper SM voltage capacitors. (b) Output current and voltage.
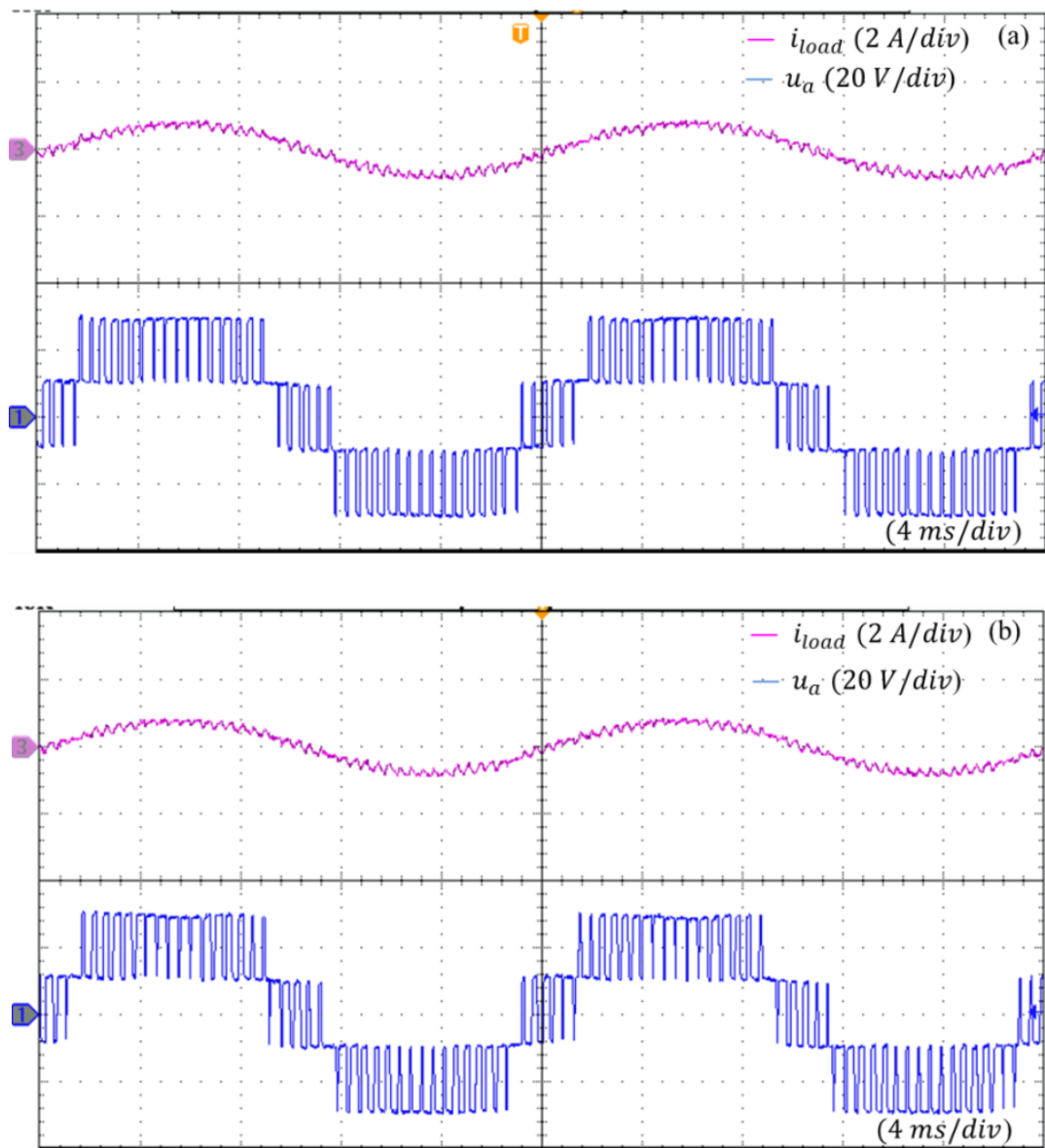
Fig 5.23. Experimental results of the output current and voltage. (a) Results of the sensor-based measurement technique. (b) Results of the proposed estimation technique.
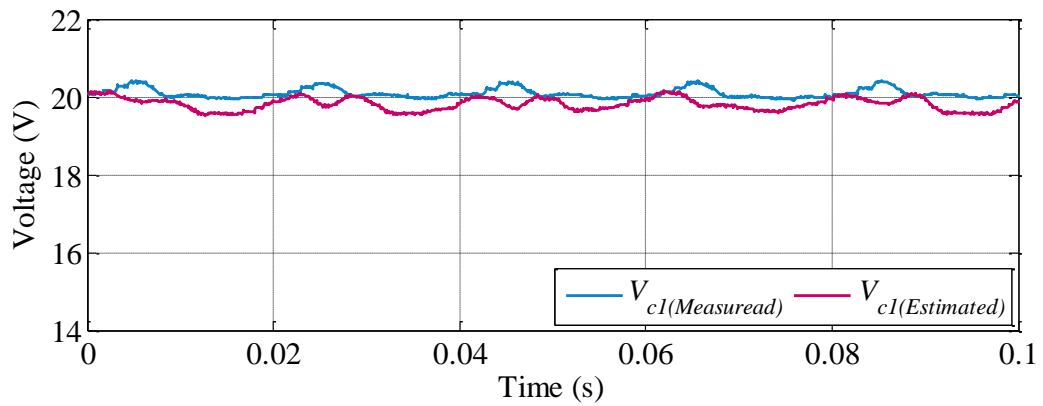
Fig 5.24. Experimental results of the voltage comparison between the conventional sensor-based method and the proposed method across $C1$.

5.7.3 Results for Load Step Change Condition

To further validate the robustness of the proposed technique for a step change in the load, additional experimental tests have been conducted by altering the load resistance (R). An additional resistance of 68 Ω is added in parallel and then removed from the load to stimulate the step change in the load.
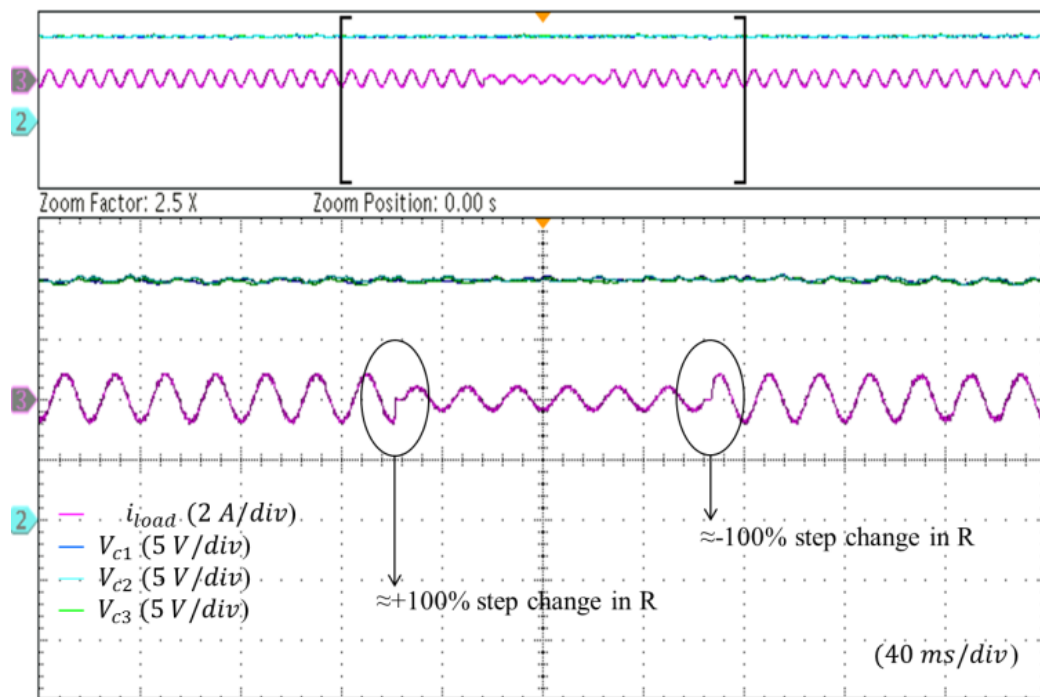
Fig 5.25. Experimental results of the proposed scheme performance at step changes (increase and decrease) in the load resistor (R).

As can be noted from Fig. 5.25, the converter was able to successfully achieve voltage-balancing. It is also worth noting that, because the additional load is switched in and out manually, a small dead-time can be seen in Fig. 5.25.

5.7.4 Effect of a Fault in the DC Source on the Voltage Estimation Value

Other dynamic analyses have been conducted to verify the proposed method in the case of a DC voltage fault occurs and when a sudden extreme change in the DC voltage is applied to the converter. Fig. 5.26 illustrates the DC voltage fault when the input voltage has been decreased by $\approx 90\%$. Interestingly, the results obtained here confirm the simulation results given in Fig. 5.15, and the only difference which can be observed is in the discharge time. In comparison with the simulation results obtained earlier, the practical results suggest that more time is needed for discharge to occur; however, this is logical due to the practical requirements of the implementation.
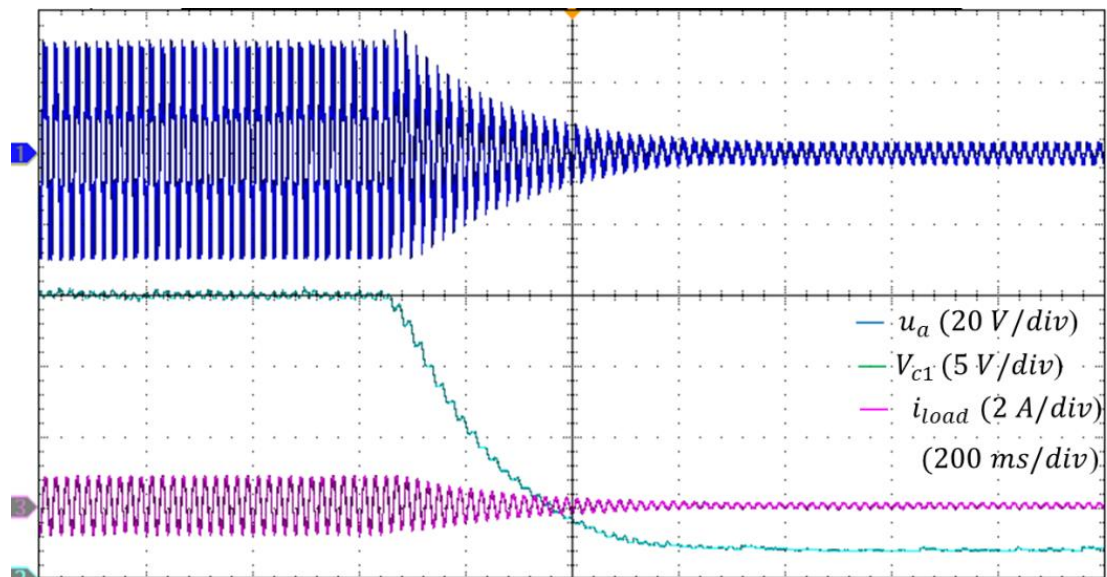
Fig 5.26. Fault occur in the DC voltage and the corresponding changes in V_{c1}, output voltage and current / Experimental results.

5.7.5 Effect of an Extreme Increase in DC Voltage

An extra extreme change is also investigated in Fig. 5.27. In this figure, an increase of approximately 90% in the DC voltage is applied to the converter. The proposed

method quickly and successfully responds to this change. It can be observed that the $\widehat{V}_{c1}$ can successfully follow up this change to reach its reference value $(\frac{Vdc}{n})$.
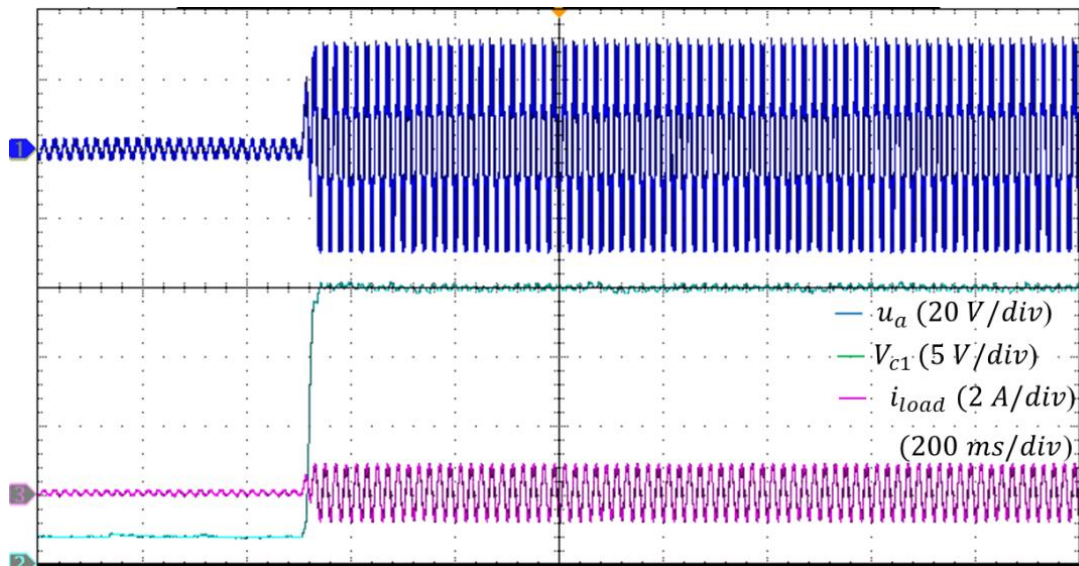
Fig 5.27. Extreme increase in the DC voltage value and corresponding changes in the V_{c1}, output voltage and current / Experimental results.

5.8 Chapter Summary

In this chapter, a novel estimation technique for MMC has been proposed in which a novel SM voltage estimation scheme has been developed using the ERLS algorithm. The ERLS algorithm was successfully employed for the first time to control the SM capacitor voltages of the MMC. Detailed simulation and experimental tests for a single-phase MMC are conducted to demonstrate the effectiveness of the proposed scheme in various normal and dynamic change conditions. Different tests have been carried out for the converter to investigate the effect of capacitance deviations, different carrier switching frequencies effect, a sudden change in load conditions, DC faults and the start-up transient condition. The results show that the proposed technique is capable of providing accurate voltage estimation and achieving voltage-balancing in the converter with only one voltage sensor per arm. The effect of voltage drops in the SM switch and wire resistance between SMs on the proposed model has been also evaluated. With this proposed technique, any voltage-balancing method can be used. This improvement allows a significant reduction in the number of voltage sensors

required. As a result, this improvement will reduce the total cost and the complexity of the converter. The application of this technique will also improve the system reliability, especially when the MMC reaches high output levels.

The proposed method was successfully validated in terms of variation in SM capacitance, where high tolerances in capacitance values have been considered. However, it would be preferable if more accurate results could be achieved in terms of capacitance uncertainty, which is the purpose of the next chapter, where a new implementation of Kalman filter algorithm is proposed.

CHAPTER 6

PROPOSED SENSORLESS VOLTAGE ESTIMATION METHOD BASED ON KALMAN FILTER ALGORITHM

6.1 Introduction

This chapter proposes another solution to the voltage-balancing control issue of the MMC previously discussed in Chapter 2. There is a similarity between the method proposed in the previous chapter (Chapter 5) and the one proposed in this chapter where two voltage sensors (per phase) are used to achieve the voltage-balancing of the converter. However, a different technique, based on a (KF) algorithm, is used here with the aim of gaining more accurate estimation results. In the proposed scheme, a (KF) algorithm is employed. The KF is used in an original way in this research for the MMC.

Although KF has been used in [43] to estimate voltage across SM capacitors, the concept used in that study was based on an observer technique which is totally different from the present proposal. In fact, two problems were associated with the previous study [43]: parameter uncertainty concerning SM capacitance, and arm inductance

values. Meanwhile in the proposed KF method and the ERLS method proposed in Chapter 5, arm inductance variations are not any more problem.

This chapter also aims to improve the previous estimation strategy presented in Chapter 5 against SM capacitance uncertainty. Numerous simulations and experimental tests are performed to assess the effectiveness of the proposed KF scheme. The results are compared with those of the sensor-based measurement technique. Further discussion is also included in the chapter summary comparing the ERLS method (described in Chapter 5) and the KF method in terms of robustness against capacitance deviation and the accuracy.

6.2 Kalman Filter

The KF is a sequential mathematical-based estimator [84] which is widely used in power electronics applications to estimate state and system parameters in differential equations or state-space model representations. The KF has the ability to consider the effect of measurement noise which may be caused by sensors [85-87]. It is also guaranteed to cope with white Gaussian processing noise [87]. This makes this algorithm more superior to some other recursive algorithms, such as conventional RLS and RLS with forgetting factor algorithm.

Table 6.1 shows the generalised sequence for KF implementation when a linear system is implemented. For simplicity, it is assumed that a linear regression dynamic system can be described as follows:

$$\boldsymbol{\theta}_{(t_i)} = \boldsymbol{\theta}_{(t_i-1)} + \boldsymbol{w}_{(t_i)} \tag{6.1}$$

$$\mathbf{y}_{(t_i)} = \emptyset^T_{(t_i)}\boldsymbol{\theta}_{(t_i)} + \boldsymbol{v}_{(t_i)} \tag{6.2}$$

where only the input ($\emptyset^T_{(t_i)}$) and the output ($\mathbf{y}_{(t_i)}$) of the system are measurable. In equations (6.1) and (6.2) $\boldsymbol{\theta}_{(t_i)}$ represents the unknown parameter of the model which is required to be estimated, $w_{(t_i)}$ is the processing noise with covariance matrix $Q_{(t_i)}$ which is also known as a random vector that drives the parameter changes, in which $Q_{(t_i)}$ is an N × N diagonal matrix. In equation (6.2) $v_{(t_i)}$ is the measurement noise with variance $r_{(t_i)}$ where $r_{(t_i)}$ is a positive real number ($r_{(t_i)} > 0$).

<p style="text-align:center">Table. 6.1. General KF Sequence for Linear Regression Dynamic System Implementation</p>

Step	Action and related equation
1. Initialisation	Initiate $P_{(t_0)}$, $\widehat{\boldsymbol{\theta}}_{(t_0)}$, $Q_{(t_i)}$ and $r_{(t_i)}$
2. Activate the algorithm with the same sampling period (Δt)	For, $t_i = t_1, t_2 \ldots t_j$ where $\Delta t = t_{2-}t_1 = \cdots = t_j - t_{j-1}$
3. Calculate the Kalman gain	$K_{(t_i)} = \dfrac{P_{(t_{i-1})}\, \emptyset_{(t_i)}}{\left(\emptyset^T{}_{(t_i)}\, P_{(t_{i-1})}\, \emptyset_{(t_i)} + r_{(t_i)}\right)}$
4. Calculate the prediction error	$e_{\mathbf{y}_{(t_i)}} = \mathbf{y}_{(t_i)} - \hat{\mathbf{y}}_{(t_i)}$
5. Update the parameter $\widehat{\boldsymbol{\theta}}_{(t_i)}$	$\widehat{\boldsymbol{\theta}}_{(t_i)} = \widehat{\boldsymbol{\theta}}_{(t_i)} + K_{(t_i)}e_{\mathbf{y}_{(t_i)}}$
6. Update the covariance matrix $P_{(t_i)}$	$P_{(t_i)} = P_{(t_{i-1})} \left[\dfrac{P_{(t_{i-1})}\emptyset_{(t_i)}\emptyset^T_{(t_i)}P_{(t_{i-1})}}{r_{(t_i)} + \emptyset^T_{(t_i)}P_{(t_{i-1})}\emptyset_{(t_i)}} + Q_{(t_i)} \right]$

6.3 Proposed Kalman Filter Voltage Estimation Scheme

The proposed sensors arrangement for the upper and lower arm of the MMC is shown in Fig. 6.1.

Due to the similarity between the linear regression dynamic model described in equations (6.1) and (6.2) and the voltage MMC model described earlier in Chapter 5 (in equations (5.10) and (5.11), a new updated model can be formulated for the MMC. Therefore, incorporating measurement and processing noise into the model gives the following developed model:

$$\mathbf{V}_{\mathbf{cx}(\mathbf{t_i})} = \mathbf{V}_{\mathbf{cx}(\mathbf{t_{i-1}})} + \mathbf{w}_{(\mathbf{t_i})} \tag{6.3}$$

$$\mathbf{u}_{\mathbf{u}(t_i)} = \sum_{x=1}^{n} \left\{ \left[S^T_{x(t_i)} \right] \left[\mathbf{V}_{cx(t_i)} \right] + v_{x(t_i)} \right\} \tag{6.4}$$

$$\mathbf{u}_{l(t_i)} = \sum_{x=(n+1)}^{2n} \left\{ \left[S^T_{x(t_i)} \right] \left[\mathbf{V}_{cx(t_i)} \right] + v_{x(t_i)} \right\} \tag{6.5}$$

Because the upper arm implementation is independent of the lower arm, only the upper arm is described here. Therefore, following the general sequence illustrated in table 6.1, this results in the following implementation:

To initially activate the proposed KF algorithm, the covariance matrix ($P_{(t_i)}$), and estimated voltage ($\widehat{\mathbf{V}}_{cx\,(t_i)}$) should be initialized with $P_{(t_0)}$ and $\widehat{\mathbf{V}}_{cx\,(t_0)}$. As in conventional recursive algorithms, $P_{(t_0)}$ in the KF algorithm is $P_{(t_i)} = GI$, where G is a large and positive constant number whilst I is an $x \times x$ identity matrix. An adaptive Kalman gain is then calculated as follows:

$$K_{(t_i)} = \frac{P_{(t_{i-1})} \, s_{x(t_i)}}{\left(S^T_{x(t_i)} \, P_{(t_{i-1})} \, s_{x(t_i)} + r_{(t_i)} \right)} \tag{6.6}$$

Based on the sequence of implementation in table 6.1, the error of the upper arm is calculated as follows:

$$e_{\mathbf{u}(t_i)} = \mathbf{u}_{u(t_i)} - \widehat{\mathbf{u}}_{u(t_i)} \tag{6.7}$$

As the first sampling time is processed, $P_{(t_{i-1})} = P_{(t_0)}$, and the variance coefficient $r_{(t_i)}$ in this implementation of the KF is defined as a constant number for the whole sampling period, therefore it is assumed that: $r_{(t_1)} = r_{(t_2)} = \dots r_{(t_j)}$. The SM voltage estimation values for the upper arm are then updated with the error calculated using equation (6.7) and the Kalman gain derived from equation (6.6) and the previously estimated values ($\widehat{\mathbf{V}}_{cx\,(t_{i-1})}$). Therefore, to estimate these voltages in one prediction step ahead, the upper SM voltage estimated values can be identified as follows:

$$\widehat{\mathbf{V}}_{cx(t_i)} = \widehat{\mathbf{V}}_{cx(t_{i-1})} + K_{(t_i)} \, e_{\mathbf{u}(t_i)} \tag{6.8}$$

To further enhance the algorithm, the new covariance matrix is then updated recursively with the values $K_{(t_i)}$ and $Q_{(t_i)}$ as shown in table 6.1. Therefore, a new prediction step ahead of $P_{(t_i-1)}$ can be calculated as follows:

$$P_{(t_i)} = P_{(t_i-1)} - \left[\frac{P_{(t_i-1)} s_{x(t_i)}\, S^T_{x(t_i)} P_{(t_i-1)}}{r_{(t_i)} + S^T_{x(t_i)} P_{(t_i-1)}\, s_{x(t_i)}} + Q_{(t_i)} \right] \tag{6.9}$$
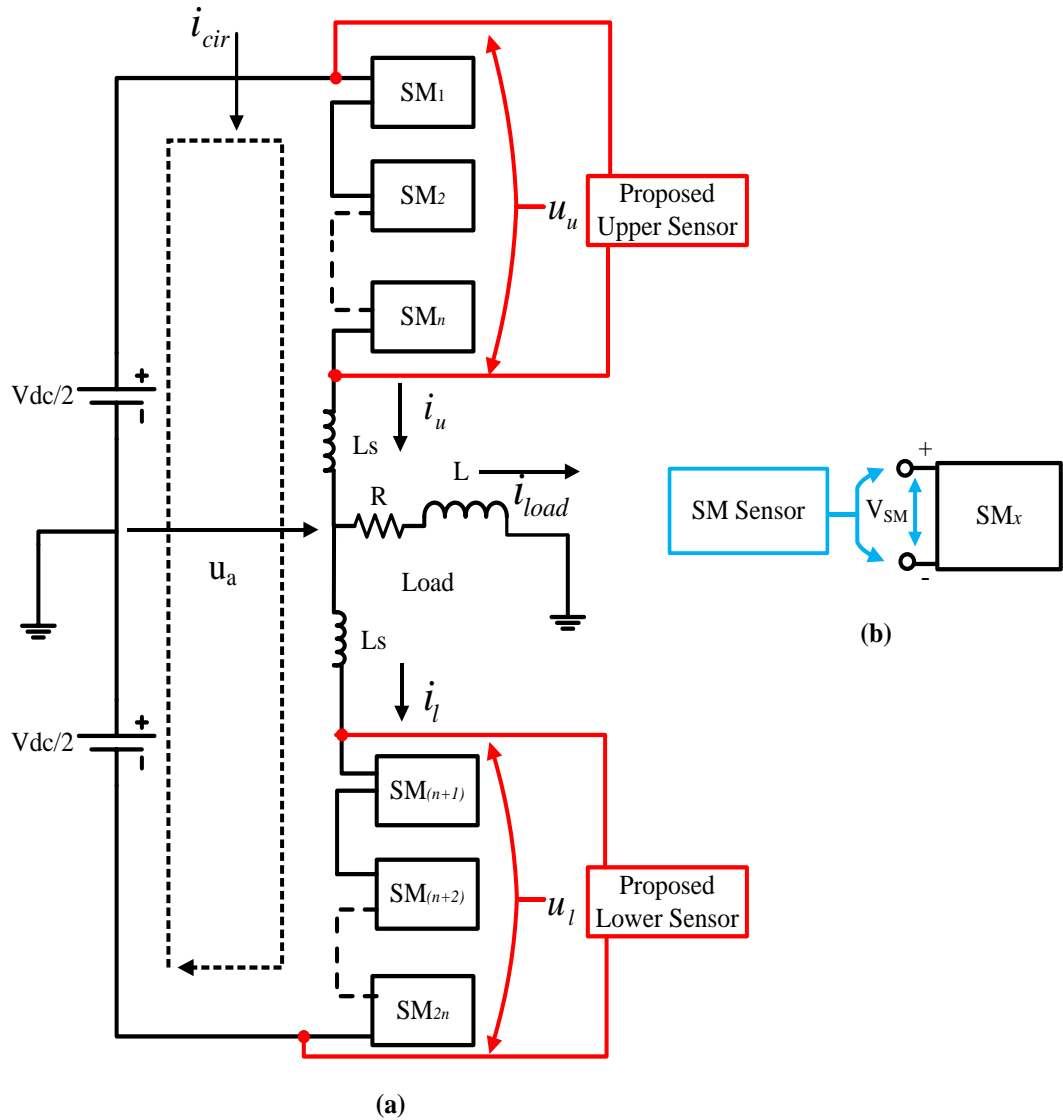
Fig 6.1. The proposed sensors arrangement. a) Block diagram of single-phase (one-leg) MMC with the proposed sensors. (b) Sensor-based SM arrangement.

The proposed upper arm estimation scheme with its associated voltage-balancing control is shown in Fig. 6.2. The voltage-balancing algorithm used here is similar to the algorithm presented in [30]. As previously mentioned in Chapter 5, it is worth noting that the voltage-balancing method used in this research has nothing to do with

the proposed estimation scheme and any other voltage control method can be used with this proposed estimation scheme. In comparison with the algorithm presented in [30], the voltage-balancing of the SM capacitors used here depends on the estimated voltages $(\widehat{V}_{c1} \sim \widehat{V}_{cn})$ rather than the actual voltages. Additionally, a unit delay (Z^{-1}) is applied to the switching patterns $(PWM_1, PWM_2, \dots PWM_n)$ obtained in order to activate $S_1, S_2, \dots S_n$ at the appropriate time (see Fig. 6.2).
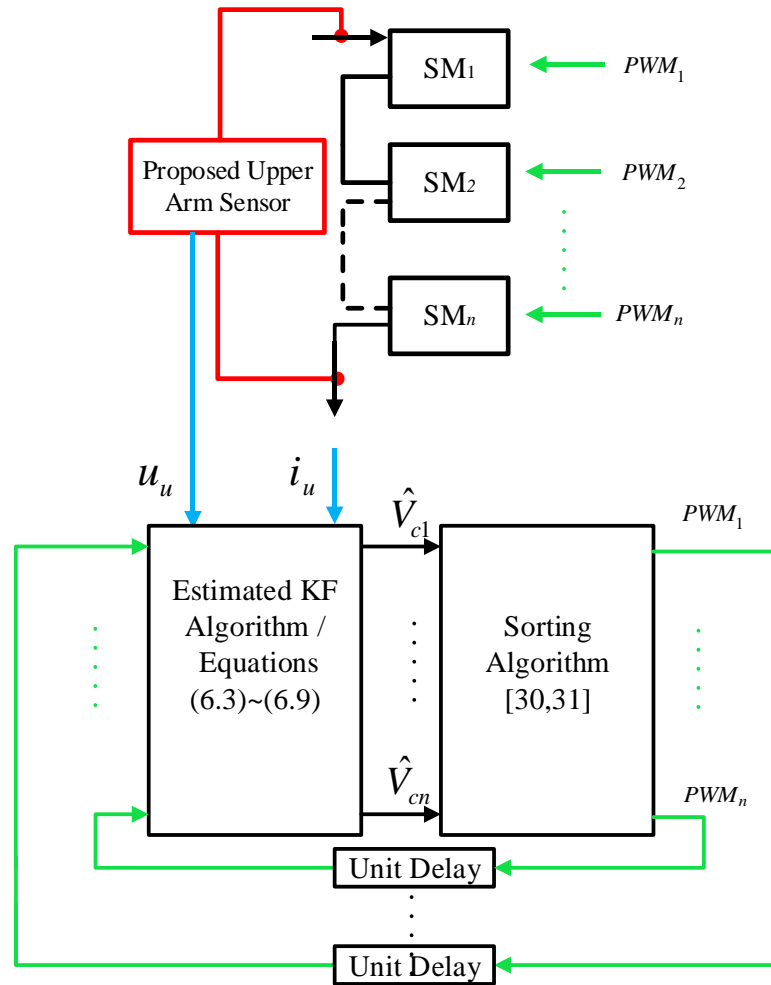
Fig 6.2. Upper arm proposed estimation scheme and associated voltage-balancing control.

6.4 Simulation Results

A single-phase 9-level MMC is also simulated in this chapter with the aim of validating the proposed estimation scheme. Sixteen SMs are used per leg, while only

one voltage sensor is used instead of eight sensors per arm. The converter, DC source value and load parameters are the same as in the previous chapter (see table 5.3). The validation of the proposed method is confirmed below according to the results of different simulation studies.

6.4.1 The Performance of the Proposed Method for Normal Operating Conditions.

In this part of the simulation study, a comparison of the proposed estimation scheme and a sensor-based scheme is conducted with a constant R-L load. Fig. 6.3 shows the performance of the converter waveforms where voltage sensors are used for each SM (sensor-based method). In contrast, Fig. 6.4 illustrates the performance of the proposed estimation scheme under the same load conditions.
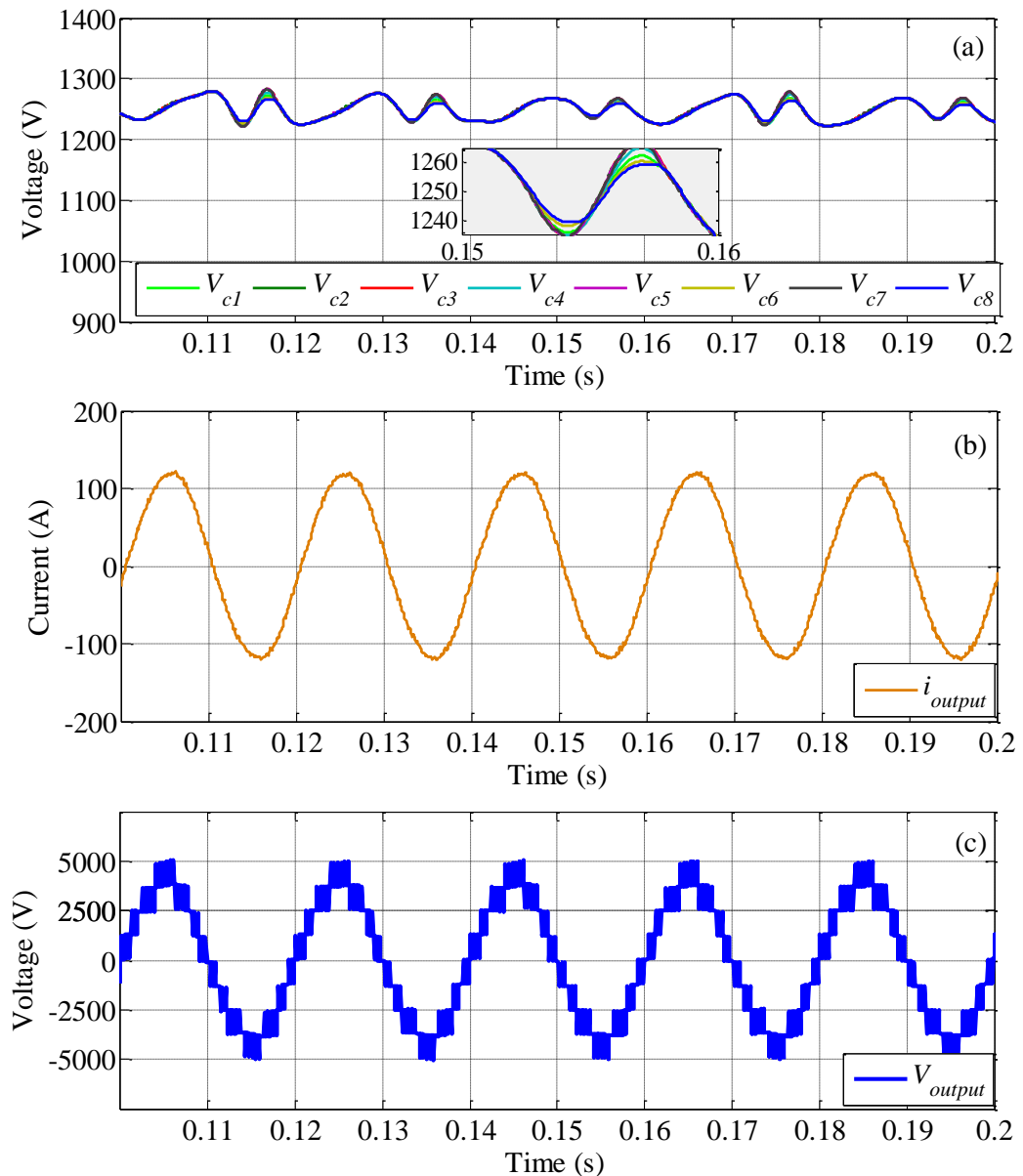
Fig 6.3. Steady-state simulation results for the 9-level MC with the sensor-based method. (a) Upper capacitor voltages $V_{c1} \sim V_{c8}$. (b) Output current. (c) Output voltage.

In comparing the two methods, only small deviations in the upper arm SM voltages can be observed (see Fig. 6.4 (a)). However, this error does not have any noticeable effect on either the output voltage waveform or the output current waveform. It should be noted that, with the proposed method, only two voltage sensors are used rather than sixteen when the sensor-based method is used.
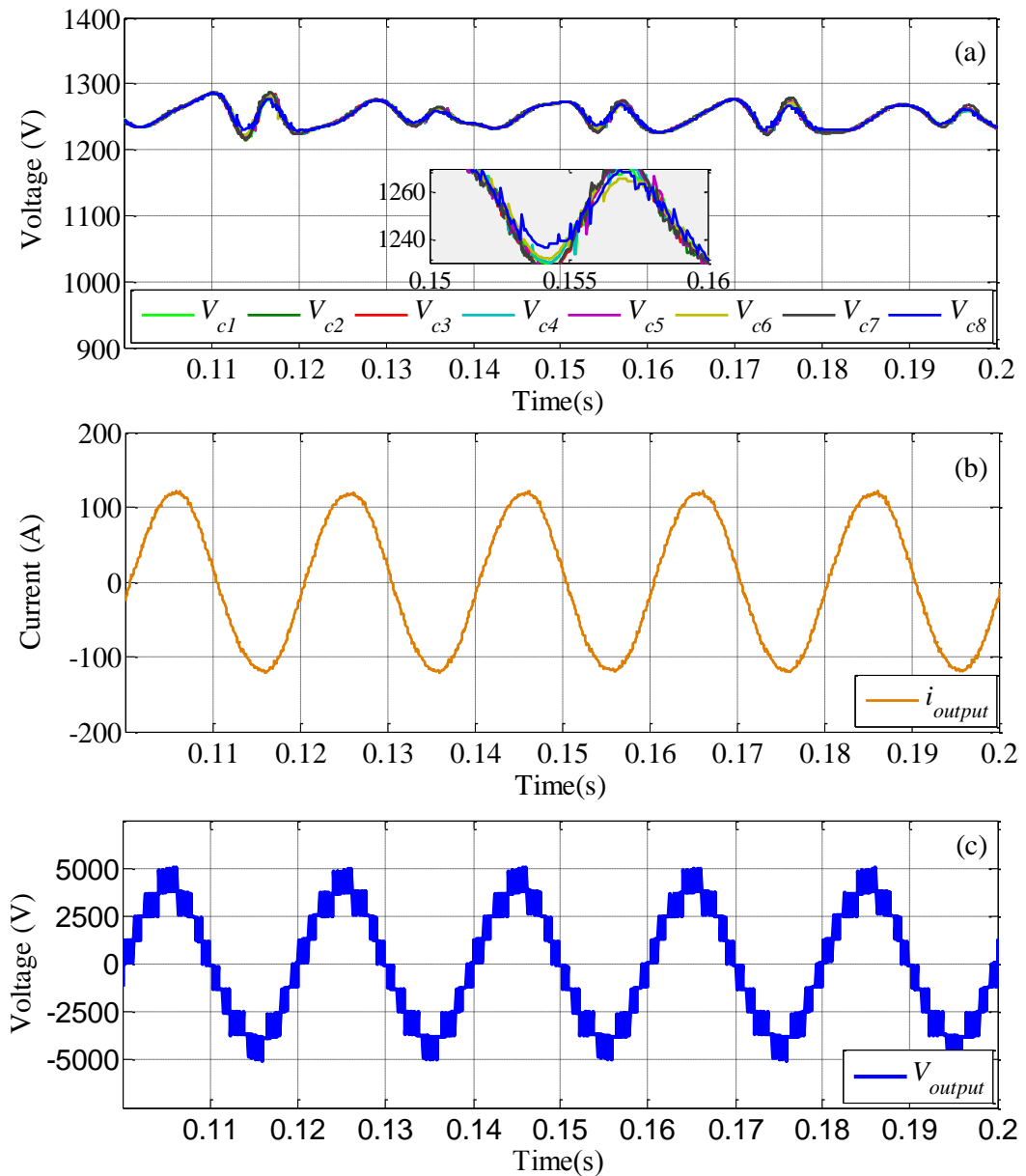
Fig 6.4. Steady-state simulation results for the 9-level MMC with the proposed estimation scheme. (a) Upper capacitor voltages $V_{c1} \sim V_{c8}$. (b) Output current. (c) Output voltage.

6.4.2 Performance of the Proposed Method with Capacitance Deviation

In comparison with the observer-based methods which were proposed in [40, 44], the method proposed here is independent of variations in arm inductance. This is because the arm inductor is not involved in the algorithm design. However, further investigation in terms of capacitance uncertainty is required.
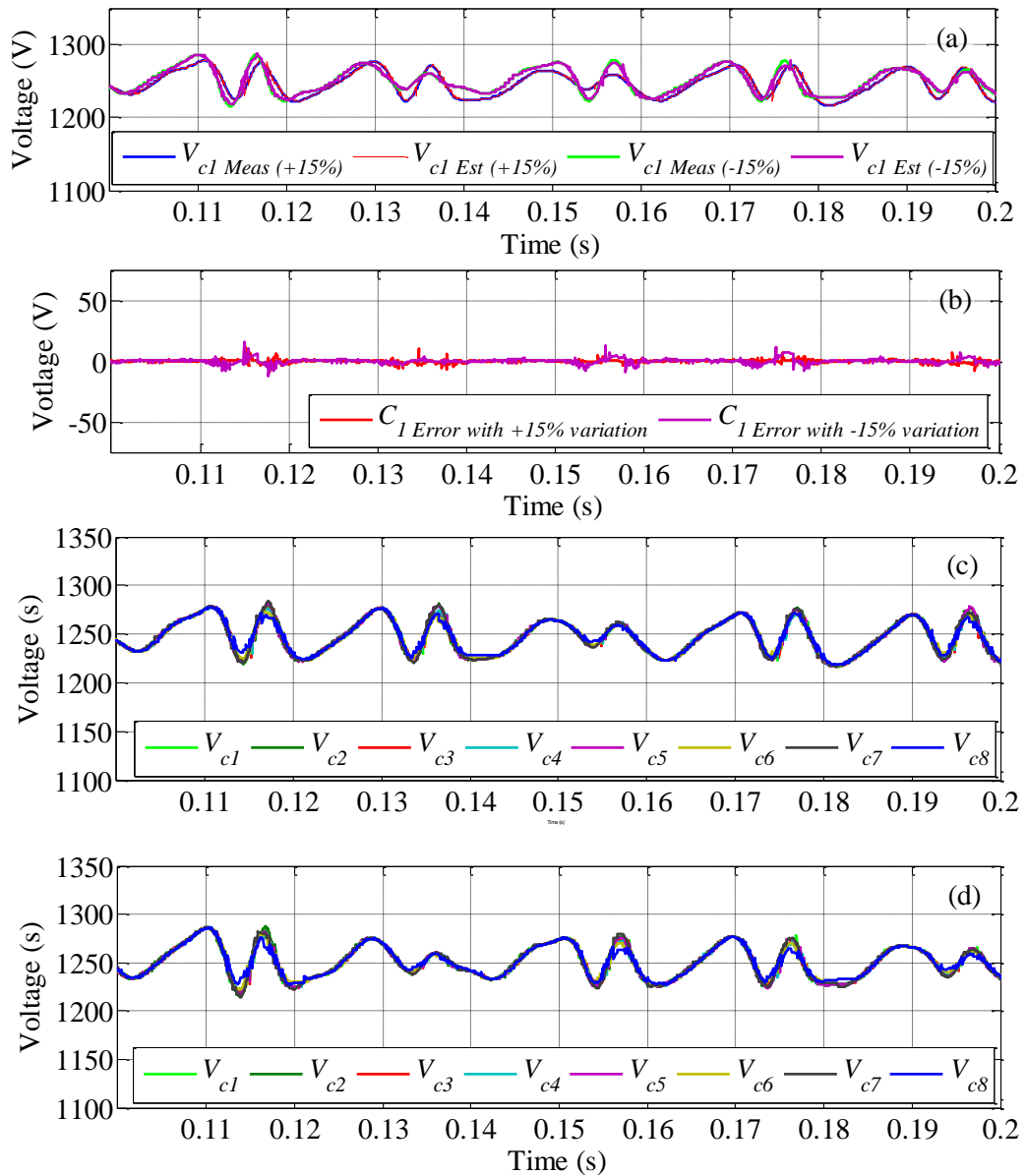
Fig 6.5. Simulation results of the upper arm voltages with deviations for all arm capacitors. (a) Measured and estimated voltage across C_1 with ±15% variations. (b) Errors between the measured and estimated voltage values when C_1 variations are ±15%. (c) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is +15%. (d) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is -15%.

Extensive simulation results have been carried out to validate the robustness of the proposed estimation method against capacitance deviation. Here, C_1 is chosen as an example with different values of deviations: ±15%, ±30%, and ±80%. For each case, random values are chosen for the other SM arm capacitances ($C_2 \sim C_8$). For example,

as shown in Fig. 6.5 when C_1 has deviations of $\pm15\%$ from its nominal value (case I), $C_2 \sim C_8$ are also given random deviations of -20%, +10%, +5%, -15%, +40%, -30%, and +60% which result in values of 1600 μF, 2200 μF, 2100 μF, 1700 μF, 2800 μF, 1400 μF, and 3200 μF respectively. For case I, Fig. 6.5(a) shows the measured and estimated voltage for C_1 where $\pm15\%$ variation is considered, and Fig. 6.5(b) illustrates the error for $\pm15\%$ variation. It can be observed that the maximum error is only around 0.8%. Figs. 6.5(c) and 6.5(d) show the effect of these variations on the other arm capacitors.

Table 6.2. Capacitance Variations in $(C_1 \sim C_8)$

Capacitor	Case I $C_1 = \pm15\%$ of its nominal	Case II $C_1 = \pm30\%$ of its nominal	Case III $C_1 = \pm80\%$ of its nominal
C2	-20% $=1600\mu$F	+5% $=2100\mu$F	+40% $=2800\mu$F
C3	+10% $=2200\mu$F	-15% $=1700\mu$F	-30% $=1400\mu$F
C4	+5% $=2100\mu$F	+40% $=2800\mu$F	+60% $=3200\mu$F
C5	-15% $=1700\mu$F	-30% $=1400\mu$F	-20% $=1600\mu$F
C6	+40% $=2800\mu$F	+60% $=3200\mu$F	+10% $=2200\mu$F
C7	-30% $=1400\mu$F	-20% $=1600\mu$F	+5% $=2100\mu$F
C8	+60% $=3200\mu$F	+10% $=2200\mu$F	-15% $=1700\mu$F
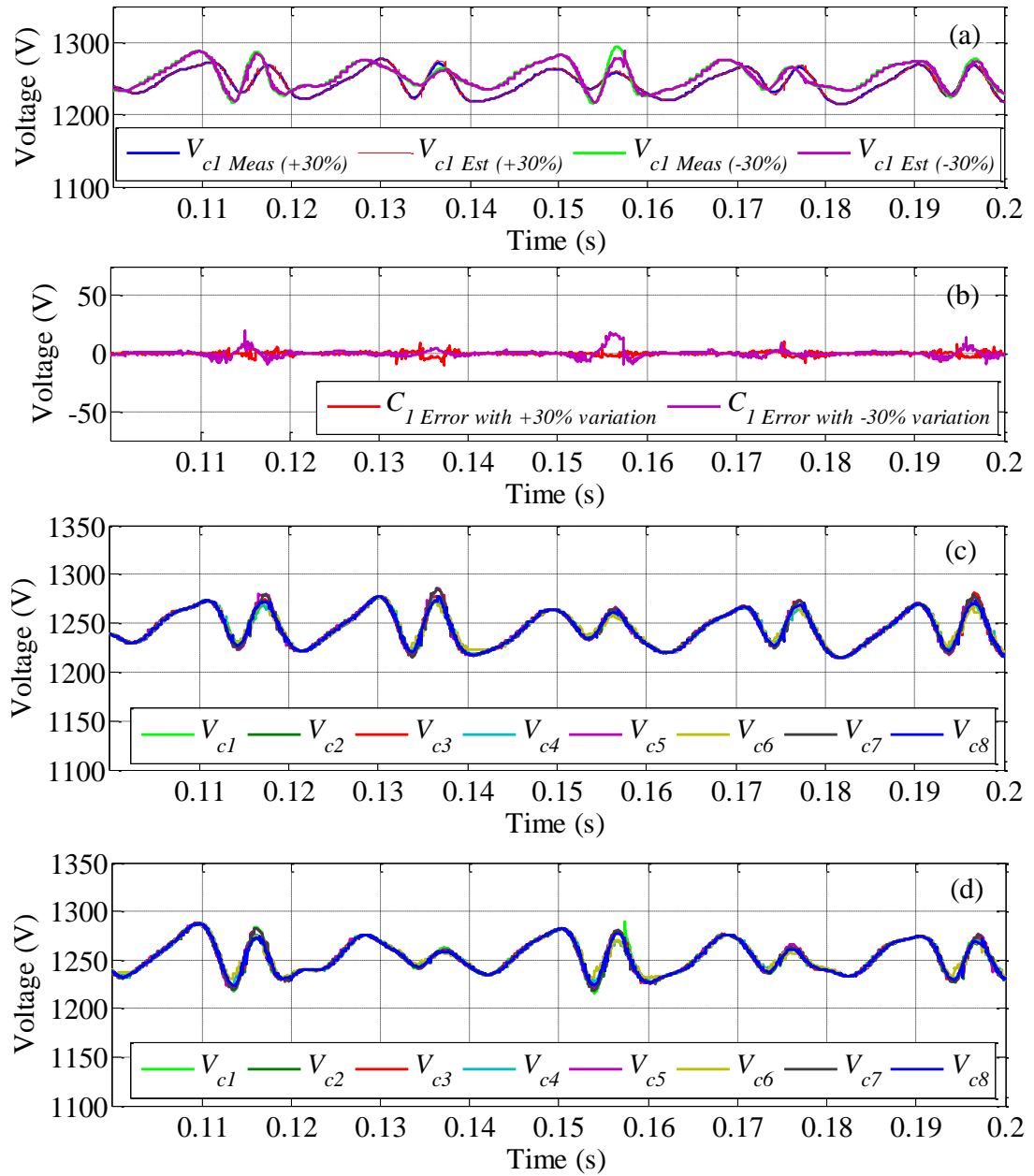
Fig 6.6. Simulation results of the upper arm voltages with deviations for all arm capacitors. (a) Measured and estimated voltage across C_1 with ±30% variations. (b) Errors between the measured and estimated voltage values when C_1 variations are ±30%. (c) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is +30%. (d) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is -30%.

For case II, C_1 is given as ±30% variations of its nominal value while the other capacitors are given different random values as illustrated in table 6.2. The error when the variation in C_1 is given as +30% is almost 0.8%; however, with -30% variation the

maximum error can be observed to be around 1.6%. Similarly for case III, when the deviation is +80%, the error is only about 0.9%. However for -80% deviation, the maximum error is 8%. It should be noted that this tolerance of -80% in capacitance variation would not be expected in real implementations.
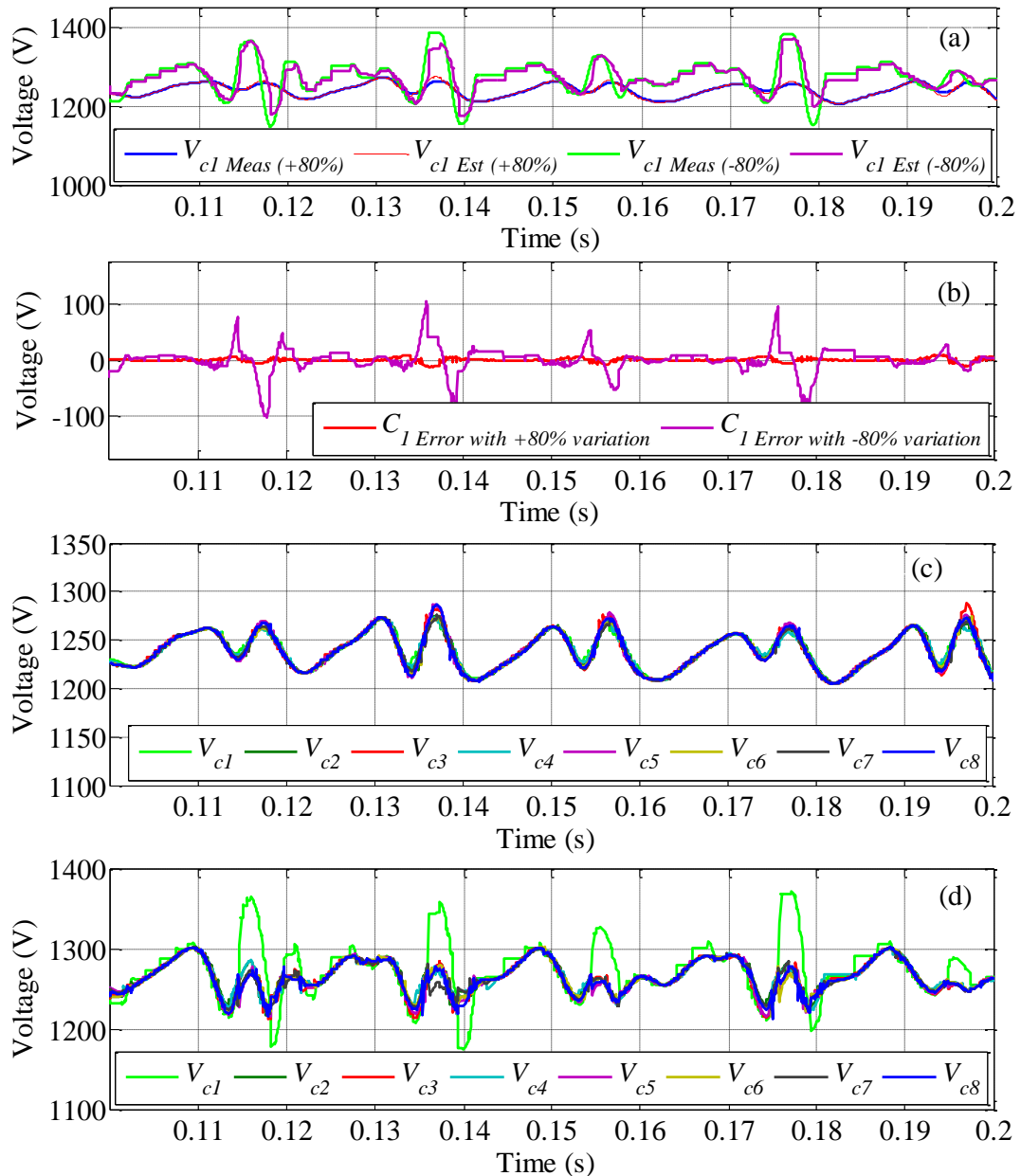

Fig 6.7. Simulation results of the upper arm voltages with deviations for all arm capacitors. (a) Measured and estimated voltage across C_1 with ±80% variations. (b) Errors between the measured and estimated voltage values when C_1 variations are ±80%. (c) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is +80%. (d) Estimated voltages for all arm capacitors ($C_1 \sim C_8$) when the deviation is -80%.

6.4.3 Effect of Load Change on Performance

To further validate the proposed estimation scheme, a dynamic test is also carried out. ±100% step change in the load conditions are applied to the converter as shown in Fig. 6.8. At 0.3s the R-L load was increased first by +100% and then at 0.4s it was forced back to the previous value. The effect of these changes on voltage estimation across C_1 is shown in Fig. 6.8(b). For both cases when the load increases or decreases, the error does not exceed 0.6% as can be seen in Fig. 6.8(c).
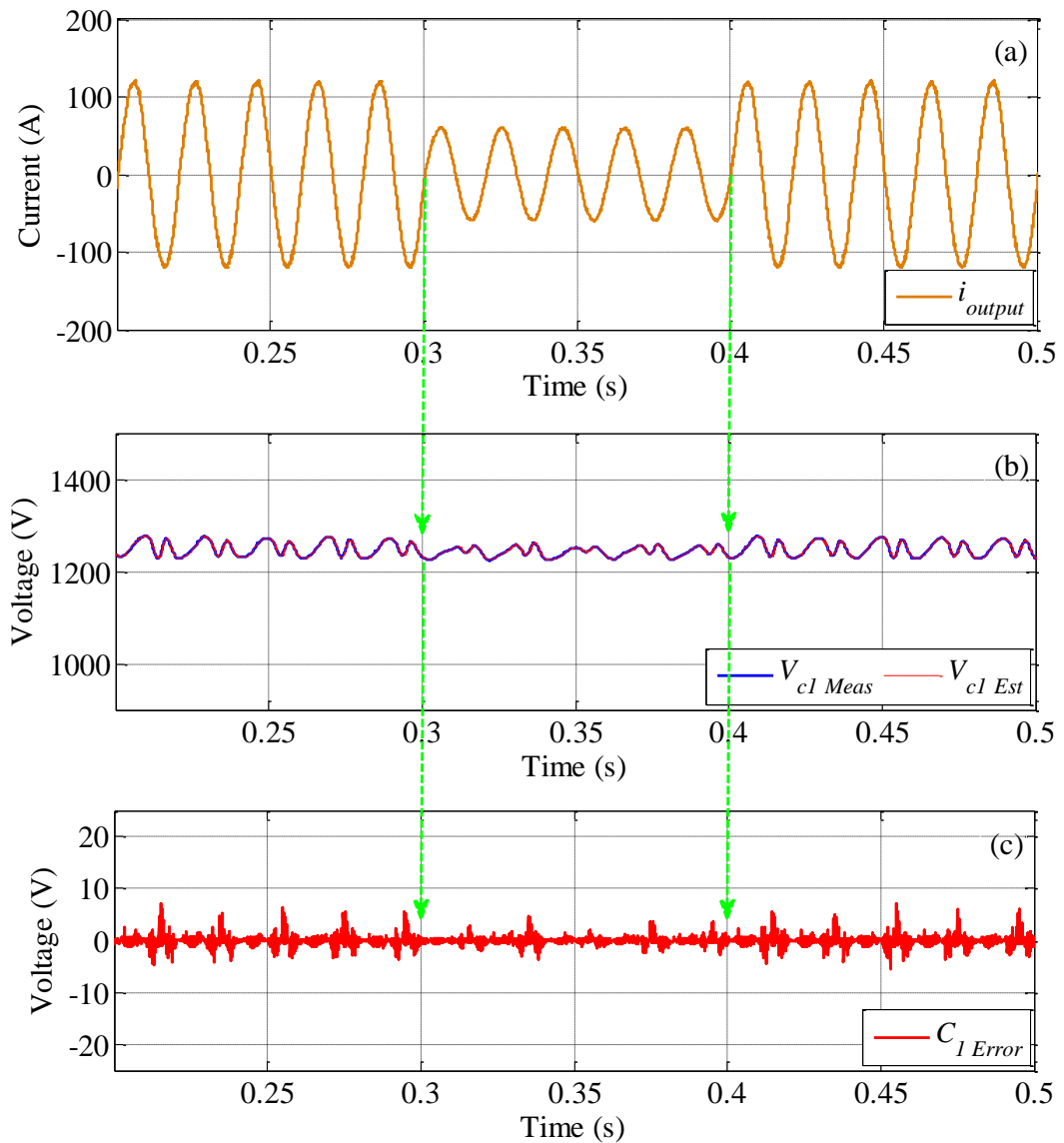
Fig 6.8. Simulation results of the effect of step load change on the 9-level MMC. (a) Output current. (b) Voltages across C_1. (c) Error.

6.4.4 The Effect of Low Carrier Frequency on Performance

Owing to the ability of the MMC to work at different carrier switching frequency when other voltage-balancing control methods are used, the proposed estimation method is further investigated, as shown in Fig. 6.9.
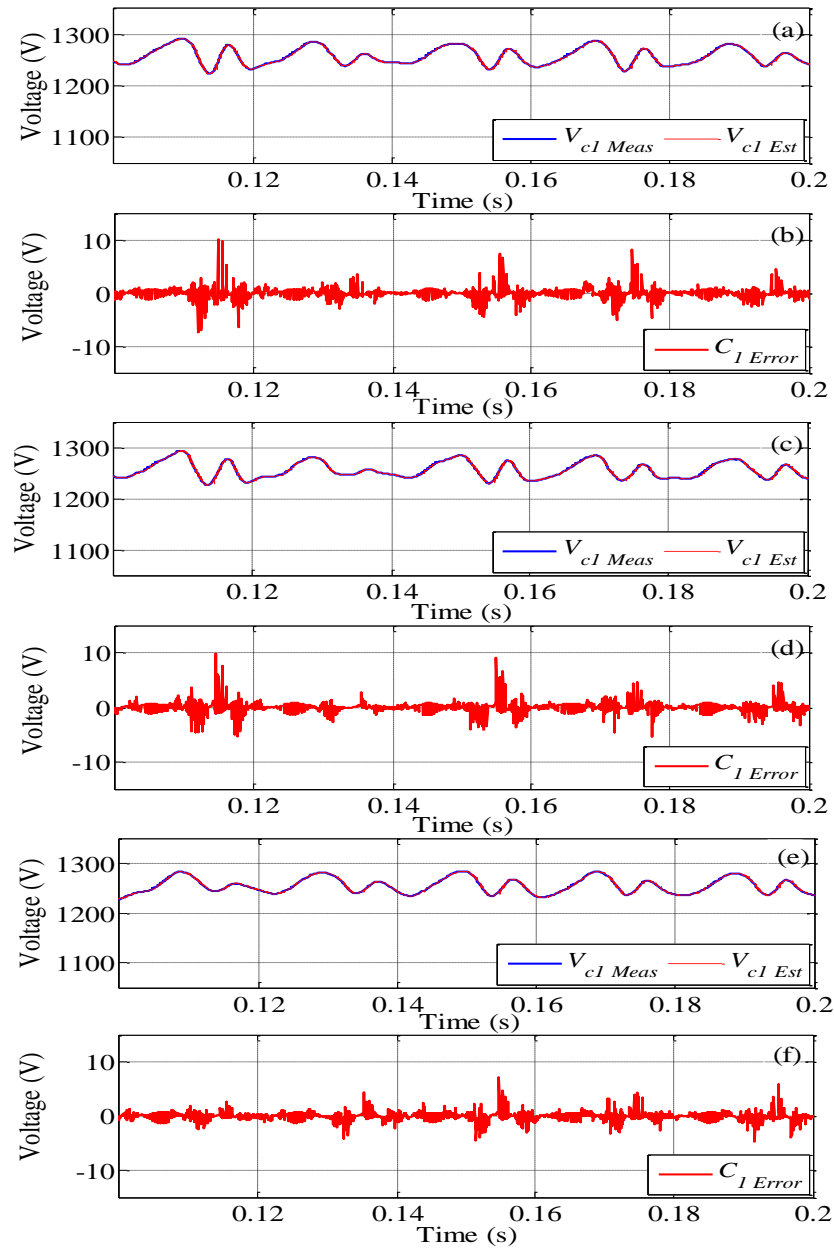
Fig 6.9. Performance of the proposed estimation scheme when low switching operating frequencies are used. (a) Measured and estimated voltage values when $f_c = 1.5$ kHz. (b) Error across C_1 when $f_c = 1.5$ kHz. (c) Measured and estimated voltage values when $f_c = 750$ kHz. (d) Error across C_1 when $f_c = 750$ Hz (e) Measured and estimated voltage values when $f_c = 45$ Hz. (f) Error across C_1 when $f_c = 45$ Hz / Simulation results.

The effect of different low carrier frequencies are shown respectively (f_c =1500, 250 and 45 Hz). For all operating frequencies used the error of the estimation value across C_1 does not exceed 0.8%.

6.4.5 DC Fault and Start-up Performance

To further validate the proposed estimation scheme, a fault in the DC source is applied to the MMC.
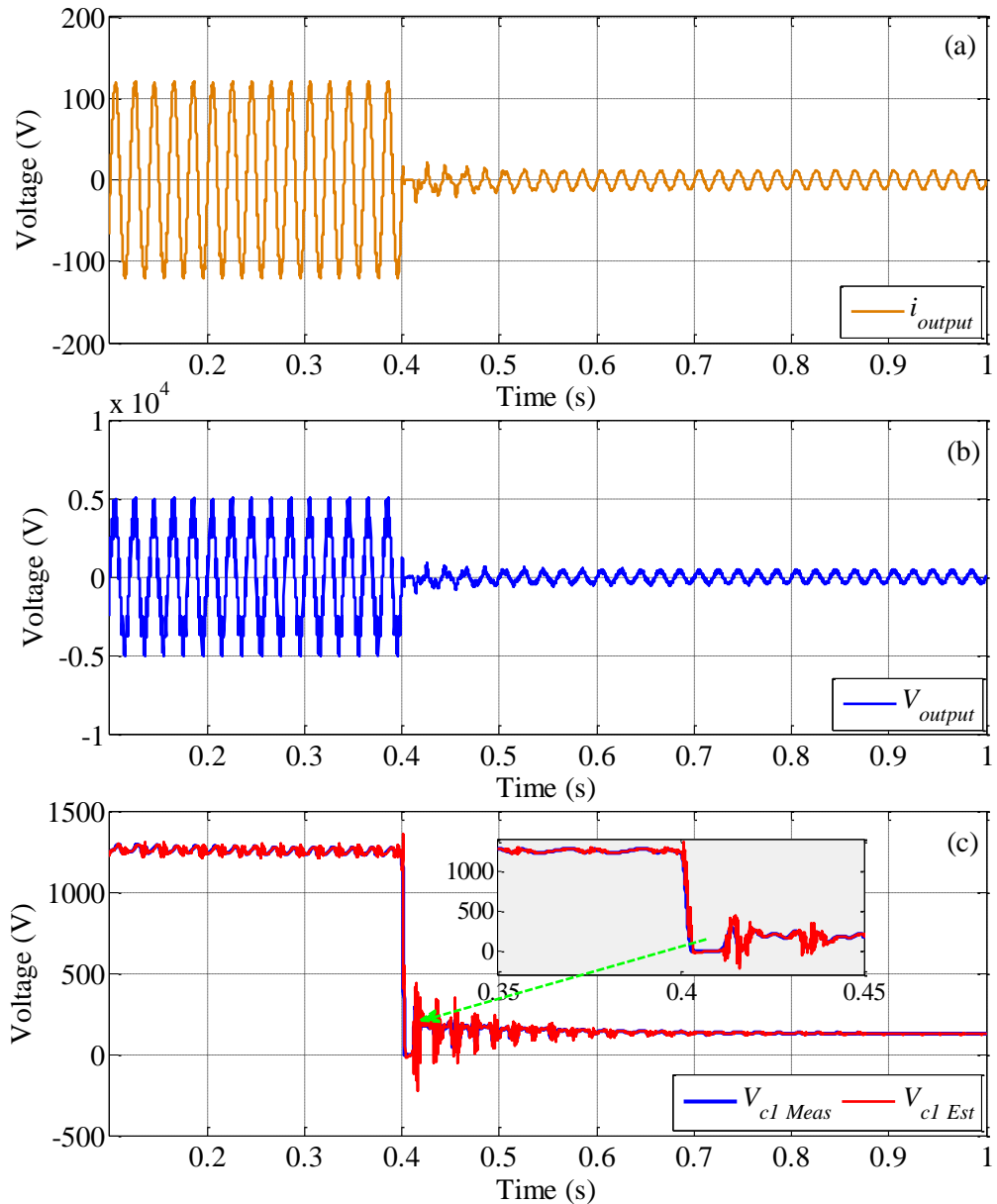
Fig 6.10. Simulation results of the performance of the proposed method during DC fault. (a) Output current response. (b) Output voltage response. (c) The effect of the DC fault on the estimation of voltage value at C_1.

In this case study, a sudden drop of 90% in the DC is considered. The corresponding changes in the output waveforms of the converter as well as the performance of the estimation of voltage value at C_1 are shown in Fig. 6.10 (a), (b) and (c) respectively.

The start-up voltage estimation performance at C_1 is shown in Fig. 6.11. For the measured voltage, the capacitor is assumed to be pre-charged at its reference value (i.e. $\widehat{V}_{c1(t_0)}$= 1250 V). From the figure it can be seen that the proposed KF estimation algorithm tracks the measured voltage very rapidly; it takes only one sampling time ($\frac{1}{20\,k\,Hz} = 5 * 10^{-5}$) for the algorithm to start tracking the measured value.
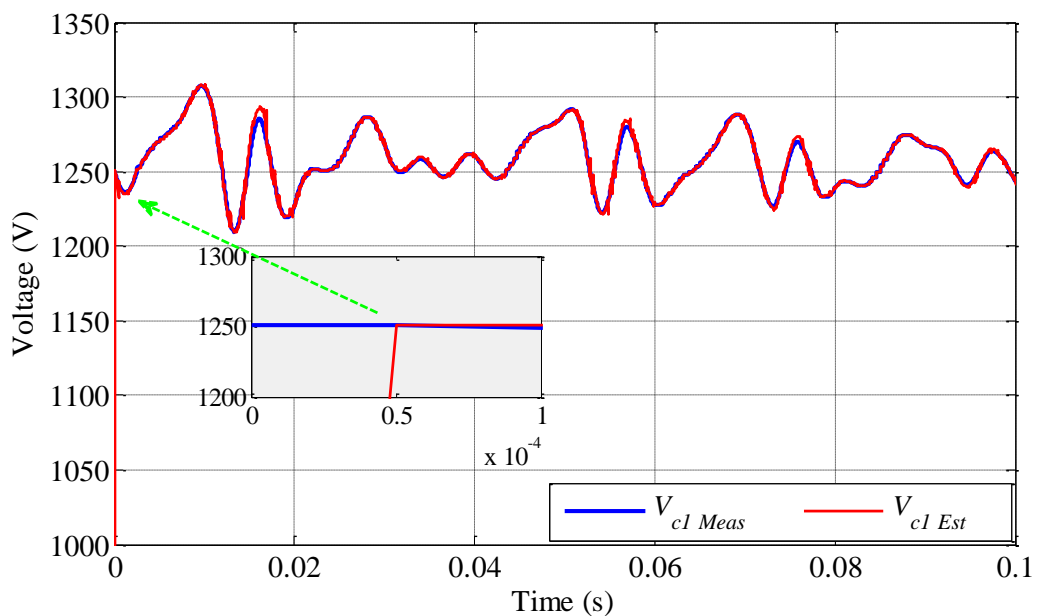
Fig 6.11. Performance of the proposed estimation scheme under start-up transit condition / Simulation results.

6.4.6 The Performance of the Proposed KF Method with a High Number of SMs

Further investigation on the effect of high number of SMs on the converter performance is carried out in three different levels. The performance of the proposed KF with 32, 64 and 204 SMs per leg are illustrated in Fig 6.12-14 respectively. For all levels, the required sampling frequencies is constant and equal to 20 KHz only.
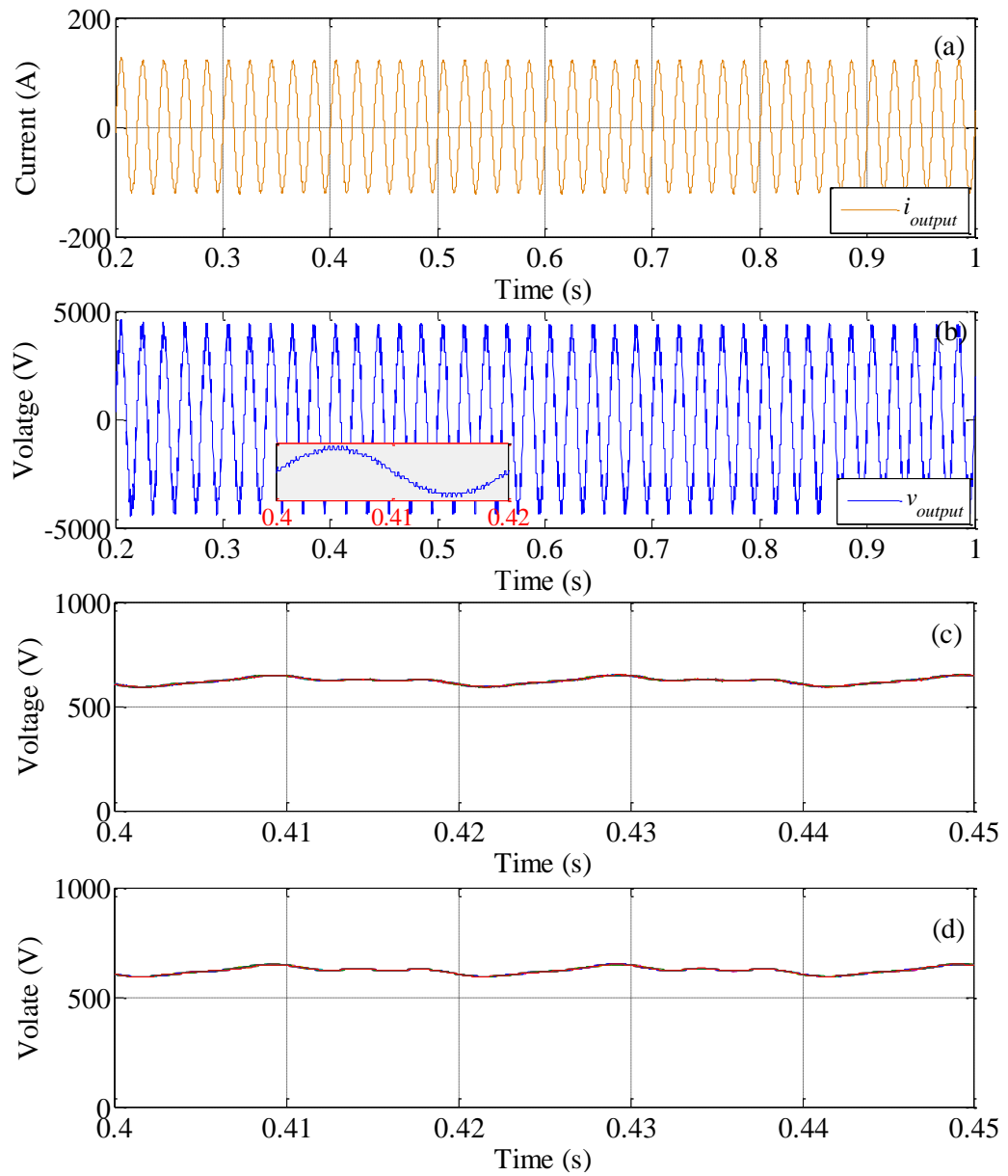
Fig 6.12 The performance of the proposed KF with 32 SMs per leg
($f_{sampling}$=20 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor
voltages $\widehat{V}_{c1} \sim \widehat{V}_{c16}$. . (d) Upper capacitor voltages $V_{c1} \sim V_{c16}$ / Simulation results.
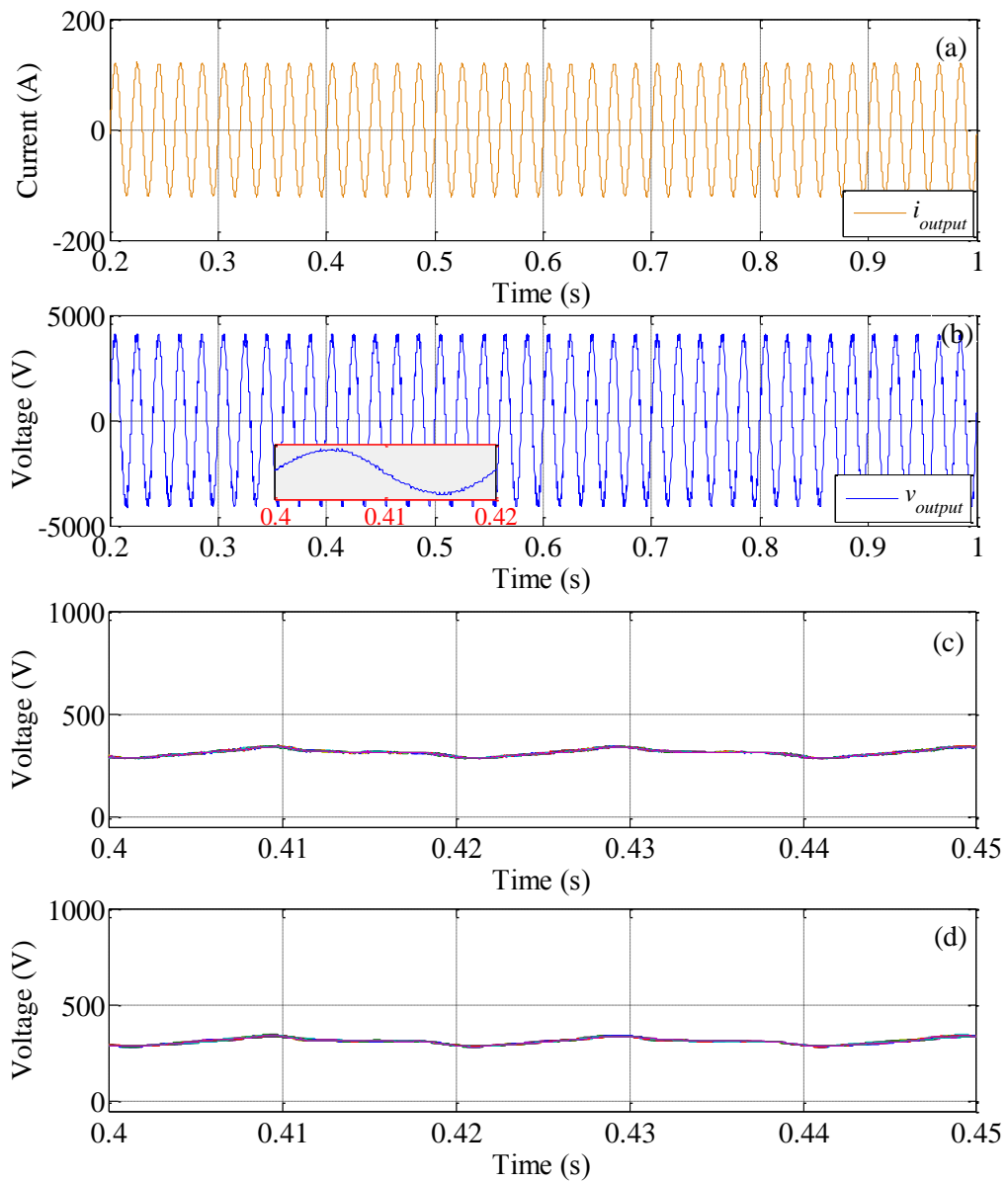
Fig 6.13 The performance of the proposed KF with 64 SMs per leg
($f_{sampling}$=20 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor
voltages $\widehat{V}_{c1} \sim \widehat{V}_{c32}$. . (d) Upper capacitor voltages $V_{c1} \sim V_{c32}$ / Simulation results.
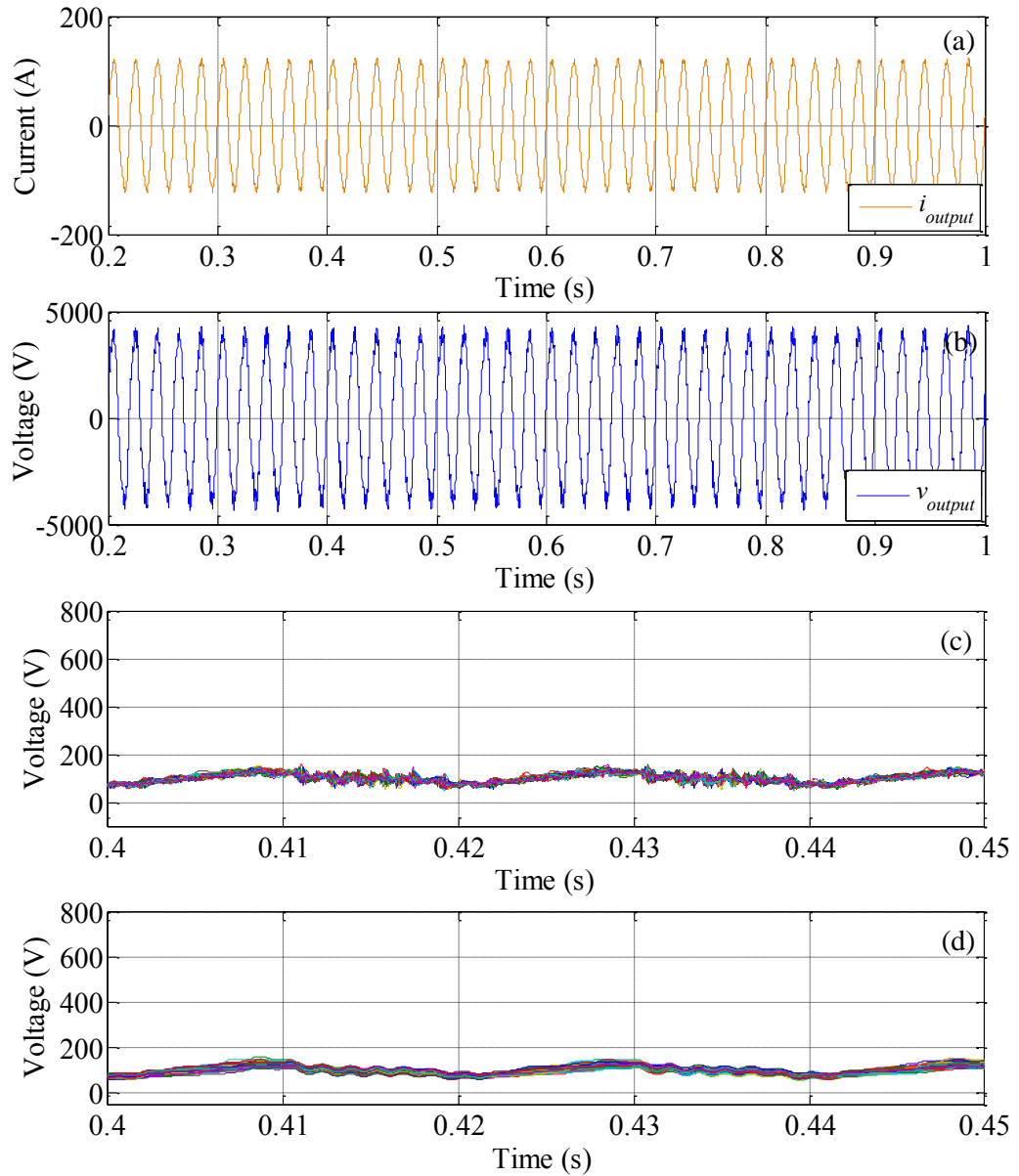
Fig 6.14 The performance of the proposed KF with 204 SMs per leg
($f_{sampling}$=20 kHz). (a) Output current. (c) Output voltage. (c) Upper capacitor
voltages $\widehat{V}_{c1} \sim \widehat{V}_{c102}$. (d) Upper capacitor voltages $V_{c1} \sim V_{c102}$ / Simulation
results.

6.5 Experimental Results

To evaluate the performance of the proposed estimation scheme, extensive experimental tests in different operating conditions were carried out. These include investigation of steady-state performance, dynamic analysis under step change in the

load conditions (up and down), a fault in the DC voltage and the corresponding changes which result, and the effect of an extreme increase in the DC voltage on the performance of the proposed method. The parameters of experimental tests are given in Chapter 4.

In comparison with the simulation studies, some experimental tests are already included in this practical implementation; however, they are not directly presented in the analysis. For example, variation in capacitance is considered, since the capacitor used already has a possible variation of ± 20% according to the datasheet from the manufacturer.

6.5.1 Steady-State Operation Performance

A comparison has been made between the proposed estimation scheme and the sensor-based method to verify the simulation results. A constant R-L load is applied to the converter, and its output waveforms are illustrated in Fig. 6.15 based on the sensor-based method. The three upper capacitor voltages are shown in Fig. 6.15 (a), whilst the output load current and voltage waveforms are shown in Fig. 6.15 (b).

In comparison with the proposed estimation scheme, Fig. 6.16 (b) shows no differences in terms of the output converter waveforms for current and voltage. However, similar to the results achieved earlier in the simulation analysis, the three capacitor voltages shown in Fig. 6.16 (a) exhibit slight deviations in comparison with those in Fig. 6.15(a). However, as described above, there is no marked impact on the output waveforms of the converter, which confirms the simulation results. Fig. 6.17 shows the voltages across C_1 when the sensor-based method (V_{c1} measured) and the proposed method ($\widehat{V}_{c1}$ estimated) are used.
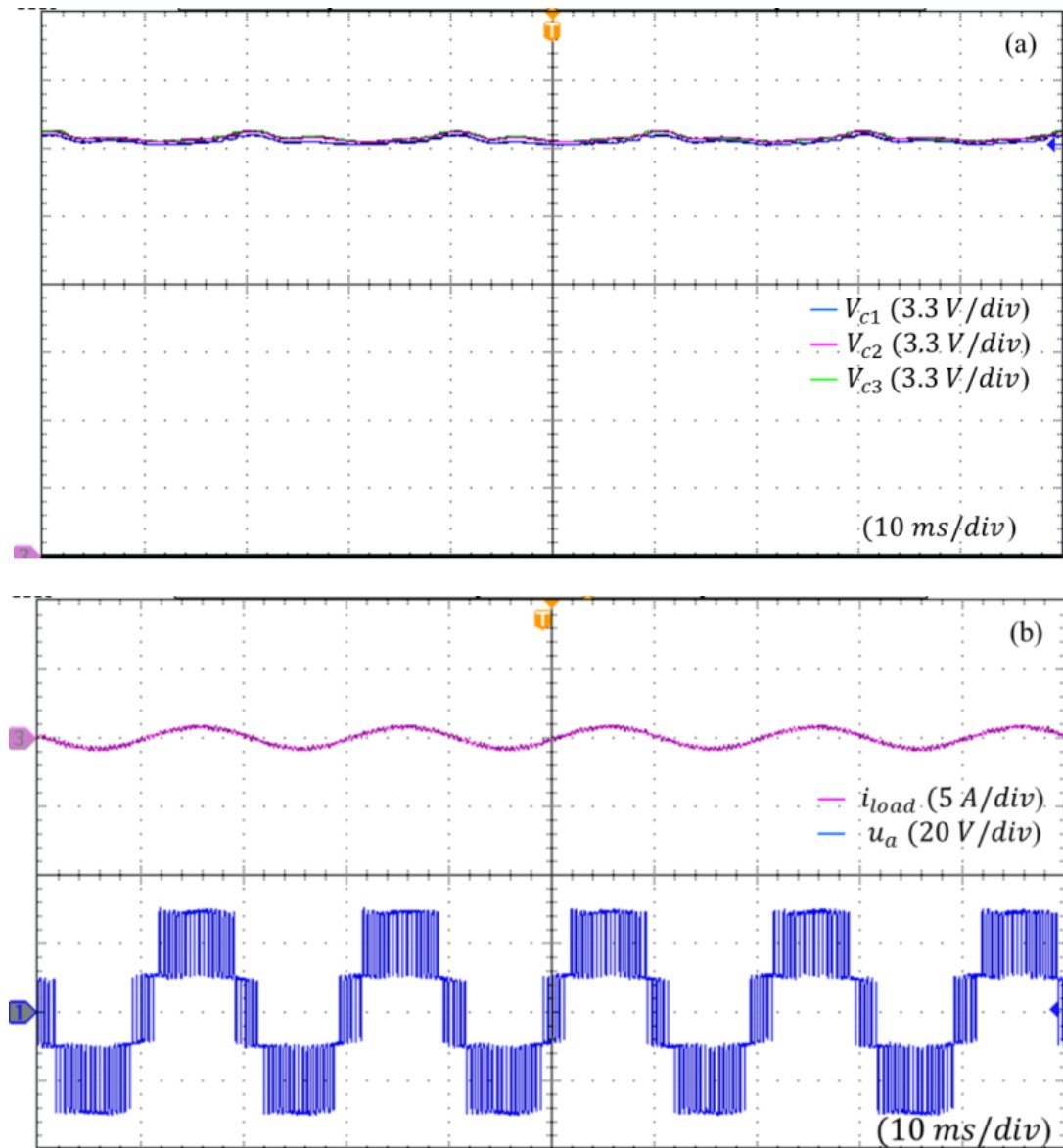
Fig 6.15. Experimental results of the sensor-based method at constant R-L load. (a) Upper SM voltage capacitors. (b) Output current and voltage waveforms.
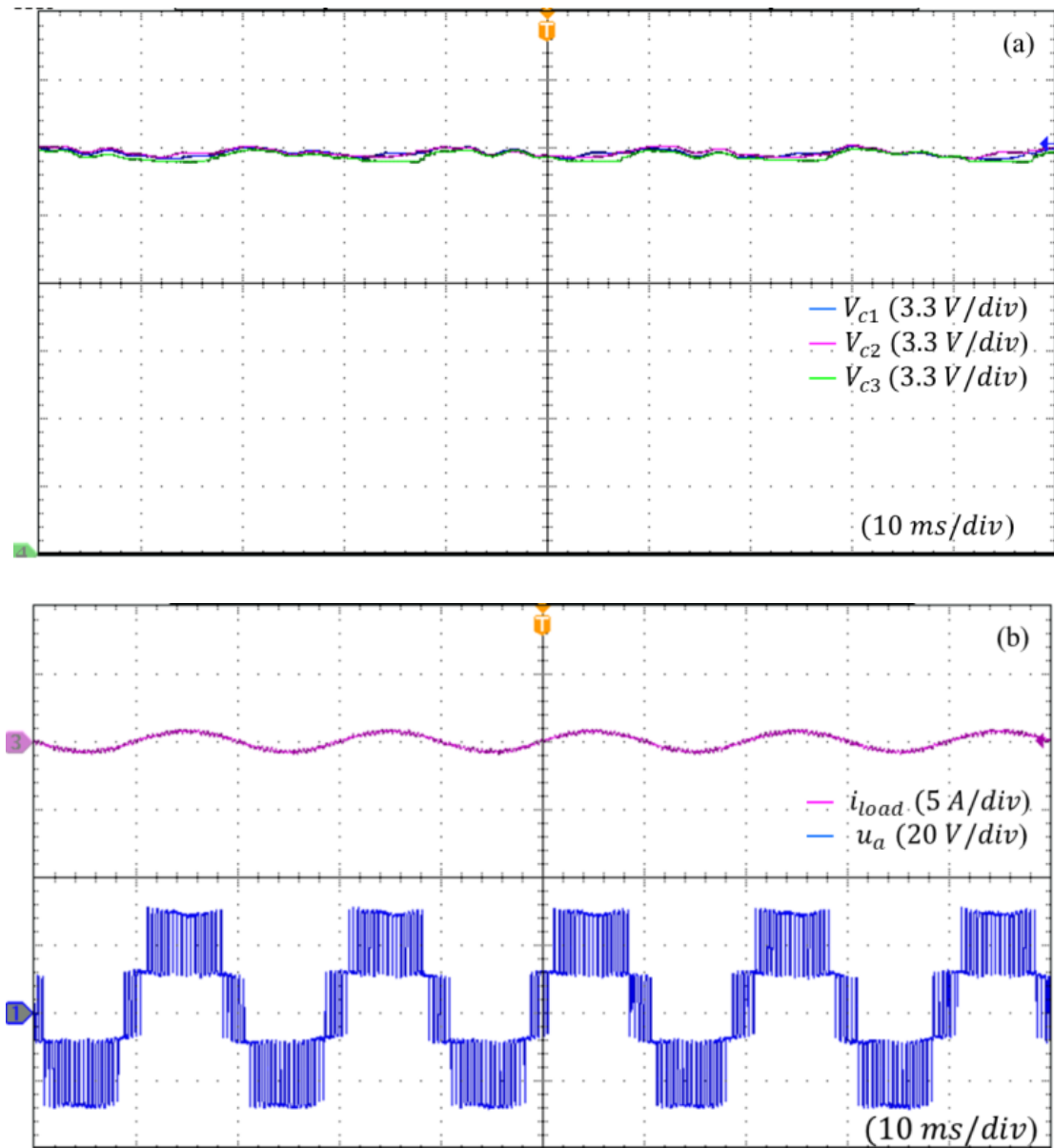
Fig 6.16. Experimental results of the proposed estimation scheme at constant R-L load. (a) Upper SM voltage capacitors. (b) Output current and voltage waveforms.
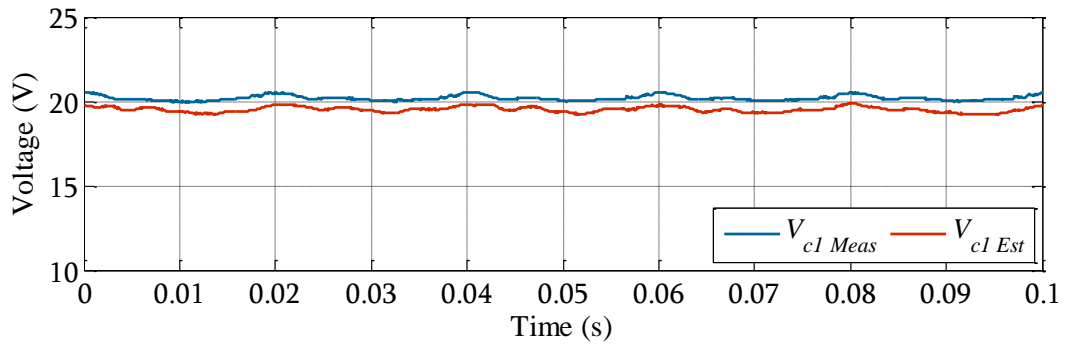
Fig 6.17. Experimental results of the voltages across C_1 when the sensor-based method and proposed estimation scheme are used.

6.5.2 Effect of Load Change on Performance

Further validation in a dynamic change analysis is illustrated in Fig. 6.18. In this study, step changes in the load condition are applied to the MMC when the load resistance (R) is changed. The value of R is altered between 33 Ω and 68 Ω first, and then between 68 Ω and 33 Ω. For both cases of increases and decreases, as can be seen in Fig. 6.18, the capacitor voltages still track the reference value $(\frac{Vdc}{n})$, which confirms the simulation results obtained earlier.
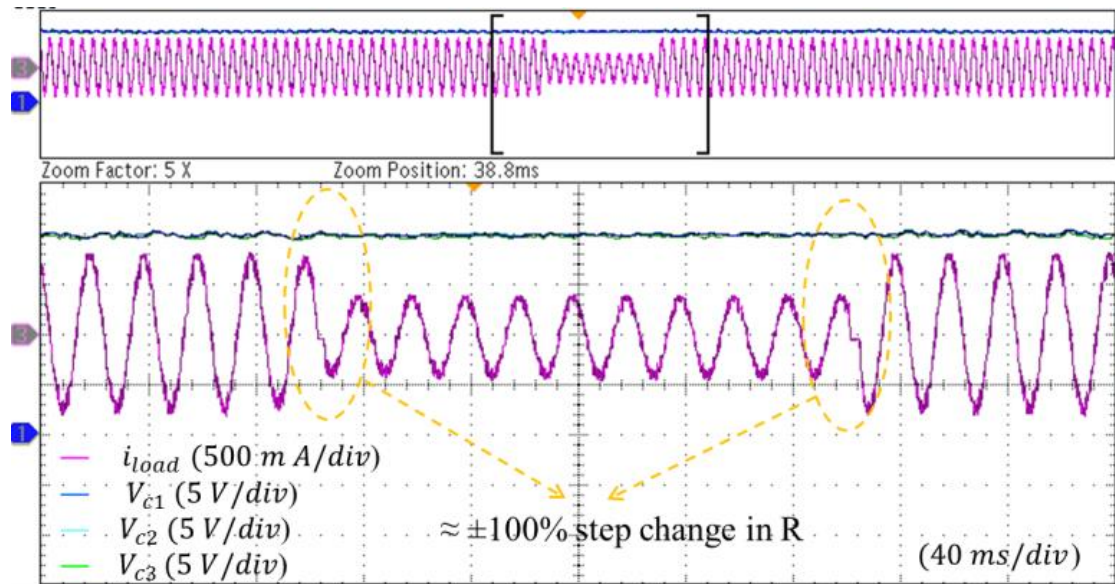
Fig 6.18. Step load change analysis of the load resistance (R) in the proposed method / Experimental results.

6.5.3 The effect of a Fault in the DC Source on the Estimation Value

To further confirm the robustness of the proposed scheme in terms of more dynamic changes, another case has been investigated. A DC voltage fault is applied to the MMC by applying a sudden extreme change in the DC voltage to the converter. The DC input voltage of the converter has been decreased by $\approx 90\%$. Although this is an extreme change in the DC voltage, the proposed scheme successfully tracks this change as shown in Fig. 6.19 where the estimated voltage $\widehat{V}_{c1}$ in Fig. 6.19 achieves its reference value $(\frac{Vdc}{n})$.
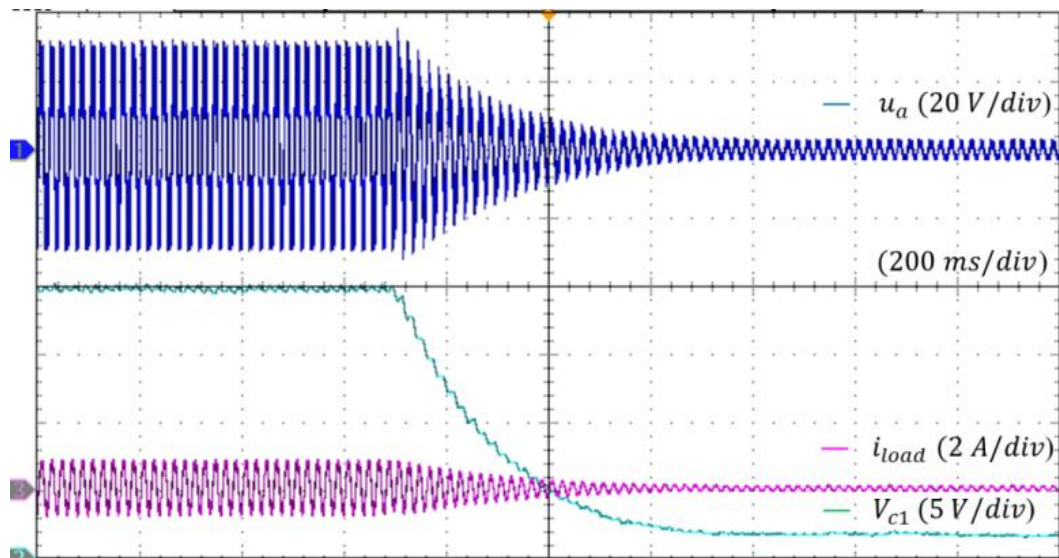
Fig 6.19. Fault in the DC voltage value and corresponding changes in converter waveforms / Experimental results.

6.5.4 Extreme Increase in the DC Source

An extra change is also examined in Fig. 6.20 where a sudden increase change is applied to the converter this time. In this investigation, a sudden increase of around 90% in the DC voltage is applied to the system. It can be observed from Fig. 6.20 that the voltage across C_1 rapidly and successfully reacts to this change.
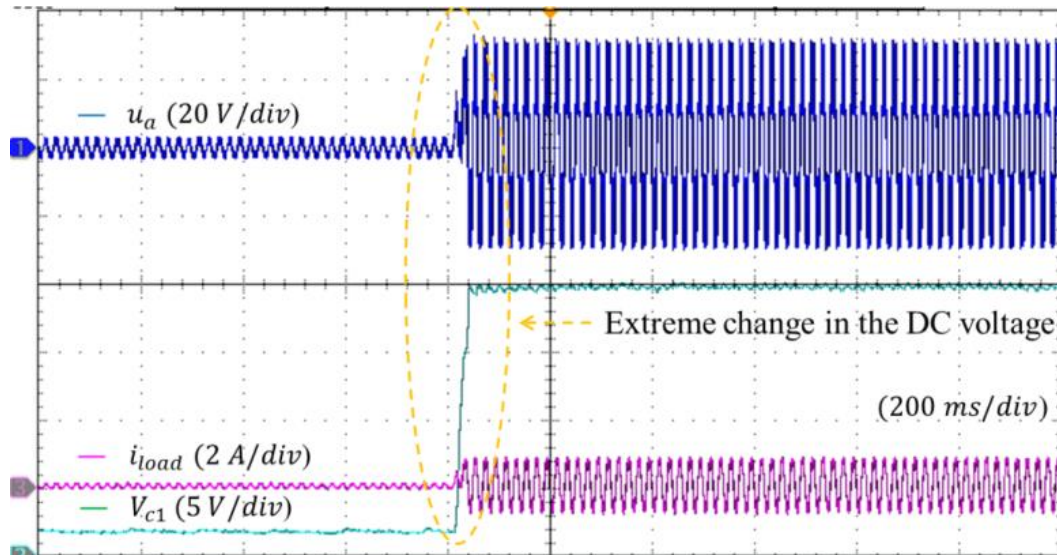
Fig 6.20. Extreme increase in DC voltage and corresponding changes in converter waveforms / Experimental results.

6.5.5 Comparison of ERLS and KF Proposed Methods.

Due to the similarity between the tests applied for ERLS and KF in the proposed methods in this chapter and Chapter 5, a comparison is made in this section to further evaluate the differences between them. In general the proposed method using the KF algorithm method is superior to the ERLS-based method. For the steady-state operating condition, both methods perform well; however, the KF shows important improvement in terms of voltage ripple in the estimated voltage values. This can be noticed in Fig. 5.8 (a) and 6.4 (a).

On the other hand, the results of some other tests, such as start-up, the effect of low carrier frequency, step change in load and DC voltage conditions, are almost the same for both experimental and simulation results. However, if high level is required for the MMC, the ERLS method requires higher sampling frequency. This may affect the computation time, as can be understood from Figs 5.16-5.18 and Figs 6.12-6.14 in sections 5.9 and 6.5. For example, when the level required for the converter was 16 and 102, the sampling frequencies needed for the ERLS were 35 and 250 kHz respectively; while the KF requires only 20 kHz for all levels presented. This gives the KF scheme another advantageous feature in comparison with the ERLS scheme.

The effect of variation in capacitance on the estimation value is also improved by using the KF approach. This can be clearly observed from Figs 5.8-5.10 and 6.5-6.7. An example of this improvement is given in Figure 6.7(b) when a large deviation of +80% is considered for the KF approach, and the maximum error found is approximately 0.9%. Meanwhile when a deviation of +70% is considered for ERLS, the maximum error is around 5% as shown in Fig. 5.11(b).

6.6 Chapter Summary

This chapter proposes another new estimation method for MMC where a novel employment of the KF algorithm is developed for the converter. Comprehensive studies of a one-leg MMC have been conducted to demonstrate the effectiveness of the proposed scheme in simulation and experimental environment analyses. Extensive steady-state and dynamic analyses are performed. The results show that the proposed estimation scheme succeeded in providing accurate estimation results, and therefore the voltage- balancing of the MMC is achieved with only one voltage sensor per arm.

In comparison with the method proposed in Chapter 5, the method presented here shows better performance, this is surmised in the table below:

Table 6.3. Comparisons between KF and ERLS proposed methods.

Methods	Steady-state / Dynamic conditions	Parameter uncertainty	Sampling frequency
KF method vs ERLS method	Output voltages and currents are similar. However, voltage ripples for all capacitors are lower.	KF method has much lower error.	20 kHz is only required for the proposed KF method, while with the ERLS method, the sampling frequencies needed were proportional to the converter output level required.

The improvement in the effect of capacitance deviations in the SM capacitance has led the present author to use the KF algorithm as an alternative solution for some existing health monitoring schemes, as discussed in the next chapter.

CHAPTER 7

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PROPOSED SCHEME FOR MONITORING SUBMODULE CAPACITANCE

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7.1 Introduction

Despite the modularity of the MMC structure, where the converter consists of a cascaded series of SMs, this feature does easily allow increases and decreases in its output level. However, the SMs involved in the converter structure make the reliability of the converter another significant challenge, particularly when the MMC has a high number of SMs. In other words, the series connection of SMs may cause a significant problem if a fault suddenly occurs, which means that the whole leg of the converter will be disconnected. This might lead to disaster if the application of the MMC is an HVDC system, for example. Usually a converter with such an application is responsible for converting power in megawatts. Therefore, it is important to monitor the SM components.

Up to now, most researchers have focused on fault detection only [47, 86, 88], where the idea in such studies is to detect and locate faults within an acceptable time. However, the monitoring and diagnosis of the condition of an MMC component before a fault occurs would be preferable. Consequently, any component which does not match the required health condition can be bypassed and replaced. Therefore, applying such a method will help in replacing any weak capacitor before a fault occurs.

This chapter presents a novel online capacitance estimation scheme based on the KF algorithm. This proposed technique is used for the first time for the MMC.

7.2 Proposed KF Capacitance Estimation Method

KF and RLS algorithms are investigated in this chapter. Although the RLS algorithm has been proposed for the MMC [53] as a capacitance estimation technique; however, its employment in this thesis is slightly different due to the use of a different voltage-balancing control method. As in previous chapters, a conventional sorting algorithm is used here, whereas the previous work [53] uses an averaging and balancing control approach. Nevertheless, the RLS algorithm is mainly used in this chapter to compare the outcomes from the proposed KF capacitance estimation method and the existing RLS scheme.

The proposed KF method is achieved through a sequence of two steps: current estimation and capacitance estimation. Details are given in the following paragraphs.

7.2.1 Current Estimation

The proposed capacitance estimation method basically involves a calculation using the well-known relationship between the voltage difference between a capacitor's plates and the current passing through it. This relationship is expressed as:

$$i_{C_{X(t)}} = C_X \, \frac{dv_{CX}}{d(t)} \tag{7.1}$$

where x is the number of capacitors within the leg.

Fig 7.1 illustrates a block diagram of the proposed method for upper arm capacitors only. However, for the lower arm, the lower current and corresponding PWM signals

and capacitor voltage signals are used instead. In the current estimation block shown in Fig 7.1 (b), and regardless of the direction of the upper arm current (i_{up}) illustrated in Fig 7.1 (a), the estimated current ($i_{C_{x-Estimated}}$) passes through the required capacitor can be calculated from the upper arm current and the upper switching state (S_x) of the targeted SM_x as follows:

$$i_{C_{x-Estimated}} = i_{up} \ S_x \tag{7.2}$$

On the other hand, due to a voltage drop caused by the semiconductor switch, some error is expected. Although this error has been proven earlier to be minor (see section 5.7.1 in the experimental results); however, in the capacitance estimation method, any error between the estimated and real capacitor current might cause a high error in results. For a more accurate representation of the estimation current, equation (7.2) is updated to (7.3). Note that this error (i_{error}) is reported in the simulation studies section.

$$i_{C_{x-Estimated}} = i_{up} \ S_x + i_{error} \tag{7.3}$$
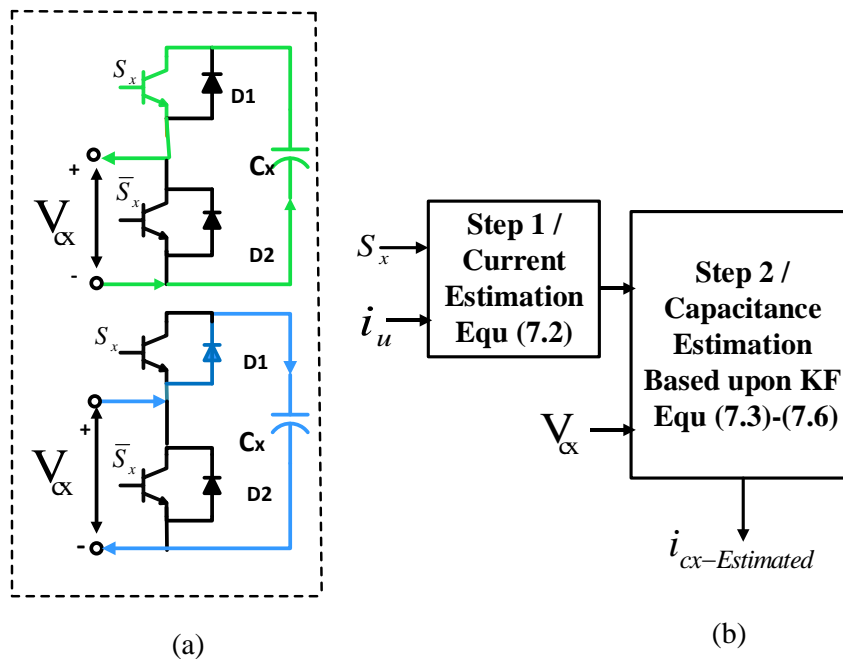
Fig 7.1. Block diagram of the proposed capacitance estimation method for the half-bridge MMC. (a) Current direction through SM. (b) proposed current and capacitance estimation steps.

7.2.2 Capacitance Estimation

The KF algorithm has been discussed in Chapter 6 in some detail. To employ this algorithm with the aim of estimating SM capacitance, the following advanced calculations should be accomplished:

$$C_{x-Estimated(t_i)} = C_{x-Estimated(t_{i-1})} + K_{(t_i)}e_{(t_i)} \tag{7.4}$$

$$K_{(t_i)} = [\frac{[P_{(t_i-1)}\frac{d(V_{cx(t_i)}^T)}{d(t_i)}]}{[1+\frac{d(V_{cx(t_i)})}{d(t_i)}P_{(t_i-1)}\frac{d(V_{Cx(t_i)}^T)}{d(t_i)}]}] \tag{7.5}$$

$$p_{(t_i)} = P_{(t_i-1)} - [K_{(t_i)}\frac{d(V_{cx(t_i)}^T)}{d(t_i)}P_{(t_i-1)} + Q] \tag{7.6}$$

where K is the Kalman gain, e is the error between the measured and the estimated capacitor current value, P is the covariance matrix (1×1 dimension) and Q is the error covariance matrix (1×1 dimension). The initial values of the updated covariance matrix and the error covariance matrix have been tuned manually.

As can be noticed from equations (7.1) – (7.6) no high order matrices are used in the calculation, and all parameters are 1×1 dimension only. This makes the proposed scheme very fast and implementable without any execution time issues.

In an earlier study [89], it was reported that the electrolytic capacitor is classified as a failure when the ESR is doubled and its capacitance decreases by up to 20% of its nominal value. However, the nominal value must be confirmed experimentally before applying the proposed estimation method. Hence, applying this method will help the operator of the MMC to replace any weak capacitor before a fault occurs. This can be achieved without switching off all SMs, but just bypassing the unhealthy SM in the circuit. Consequently, these actions will guarantee continuous power through the MMC without a loss of energy.

7.3 Results

As compared with RLS (with the forgotten factor), the analyses presented here were conducted to evaluate the performance of the proposed scheme under different

operating conditions. The parameters used in these analyses are summarised in table 7.1, where as in other chapters, a single-phase MMC was considered. The capacitance value of the first SM is investigated in all subsequent tests.

Table 7.1. System parameters

Parameter	Value
Modulation index (*mi*)	0.9
DC-link voltage (V_{dc})	(480 & 960) V
Number of SMs (n)	3
Switching frequency	2.5 k Hz
Load resistor (R)	(33 & 66) Ω
Inductive load (L)	(1.2 & 2.4) mH
SM capacitor	(1.0 & 2.0) mF
Arm inductance (L_s)	1 mH
Sampling frequency ($f_{sampling}$)	20 kHz

7.3.1 Steady-State Results

The error of the estimated current is presented first in Fig.7.2. A comparison is made in the figure between the actual current which flows though the capacitor and the estimated current given by equation (7.2). As expected, an error exists due to the voltage drop and leakage current during the ON/OFF operation of the semiconductor switch. This error may accumulate with time if no further action is taken in the algorithm to minimise that effect. However, and due to the actual voltage across the targeted capacitor being measured, this action is used as a correction step which will correct the error shown in Fig. 7.2 (c).
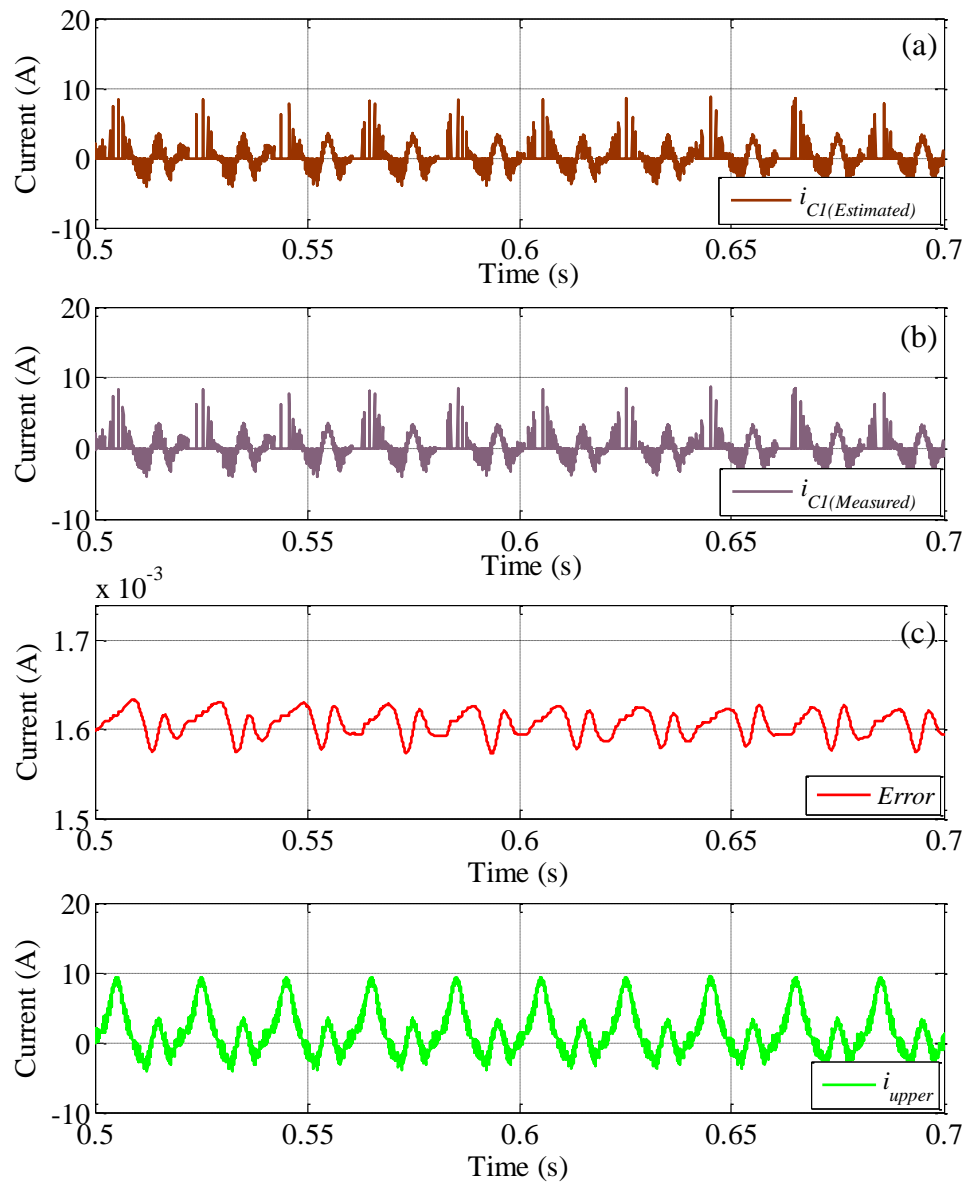
Fig 7.2 Investigation of the current estimation step of the proposed scheme. (a) Estimated current through C1. (b) Measured current through C1. (c) Error between estimated and measured current. (d) Upper arm current/ Simulation results.

In the second step of the algorithm, where the voltage across C_1 is measured and used to correct the aforementioned error, the performance of the proposed KF is reported in Fig. 7.3. In this test, the converter is assumed to work under normal operating conditions. The parameters used are similar to those presented in table 7.1, whereas the DC voltage used is 480V, R = 33Ω and L=1.2mH. In comparison with the RLS scheme in the same figure, the proposed scheme achieves an important

improvement in terms of the ripple amount in the estimated value. This can be observed in the value of error shown in Fig. 7.3 (a) and (b) where the reference value of C is 1mF. On the other hand, the two methods have similar settling times.
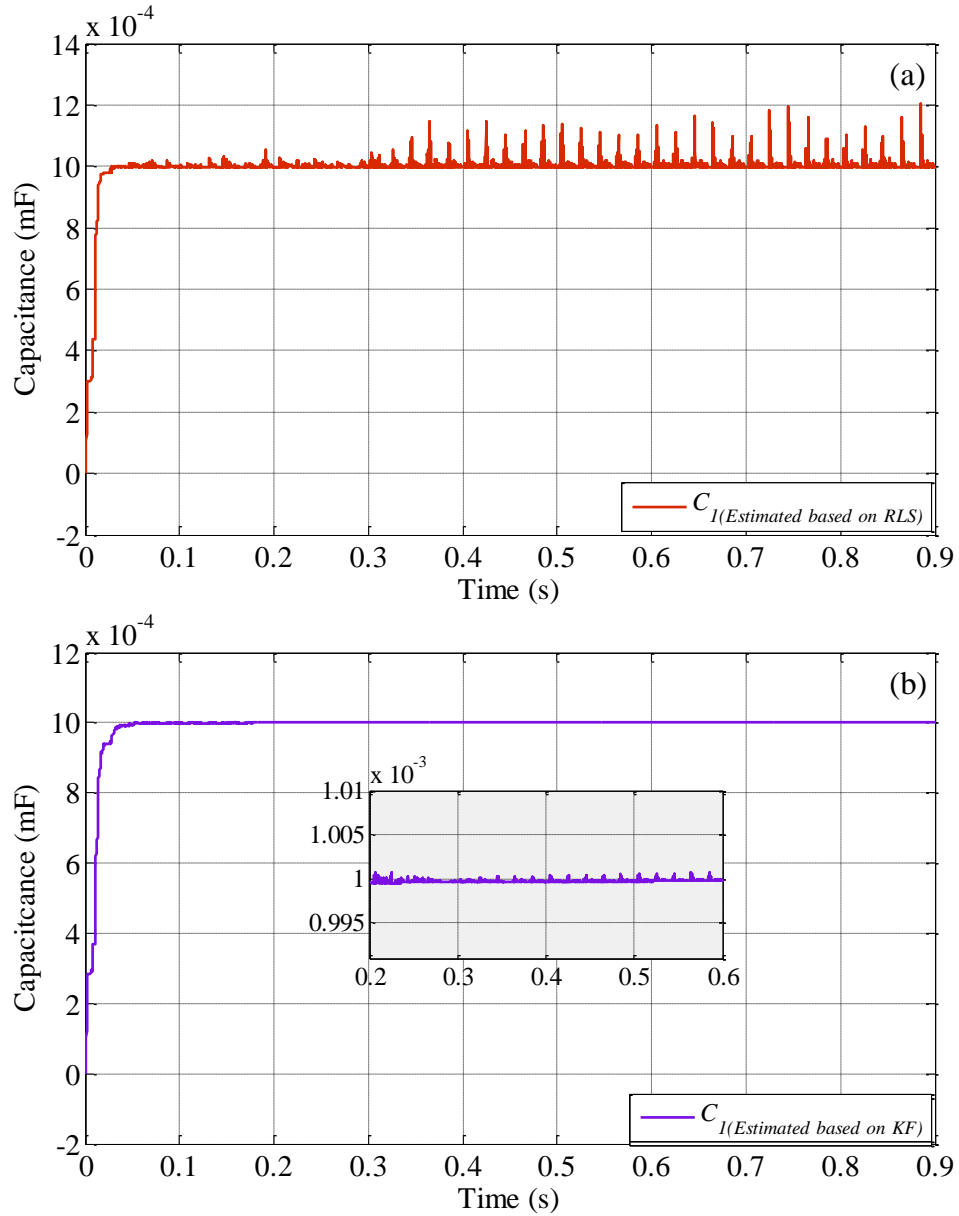
Fig 7.3 Steady-state performance. (a) Capacitance estimation based on RLS algorithm. (b) Capacitance estimation based on KF algorithm / Simulation results.

7.3.2 Dynamic Results

Two tests were conducted to simulate and evaluate the proposed method under abnormal operating conditions. In Fig. 7.4, a step change in the input DC voltage was applied first at 1s. It is clear that the proposed scheme still shows a superiority even with such dynamic change. As can be seen in the figure, when the voltage is increased at 1s, the RLS estimation scheme has a higher overshoot error than the KF method.
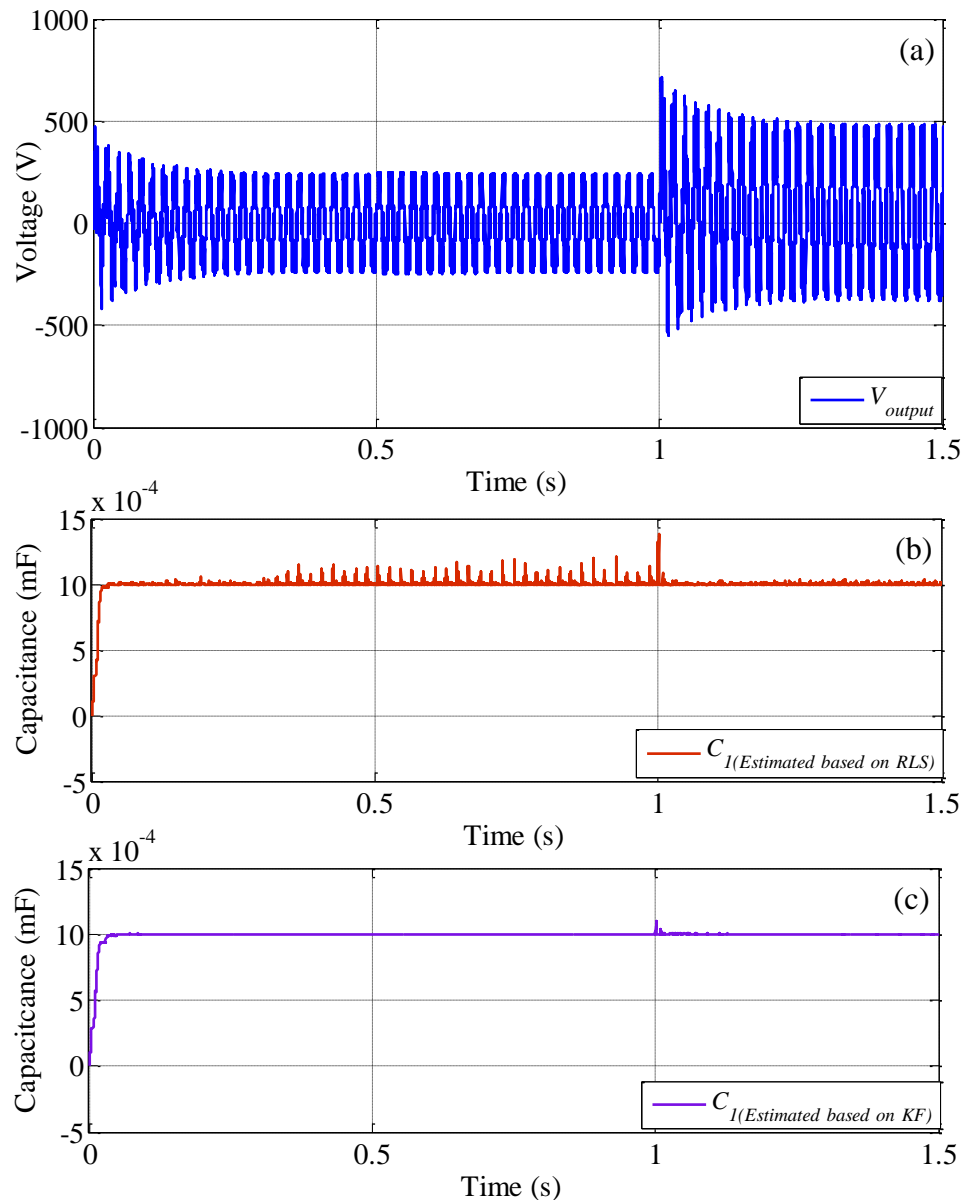
Fig 7.4 Capacitance estimation with step change in the DC source. (a) Capacitance estimation based on RLS algorithm. (b) Capacitance estimation based on KF algorithm / Simulation results.

To further validate the proposed method under another dynamic change, a sudden change in the load condition was applied to the MMC. Fig. 7.5 shows the response for the two methods when the converter load is increased and decreased by 100% at 0.5s and 0.6s respectively. Interestingly, the proposed KF method still shows superiority.
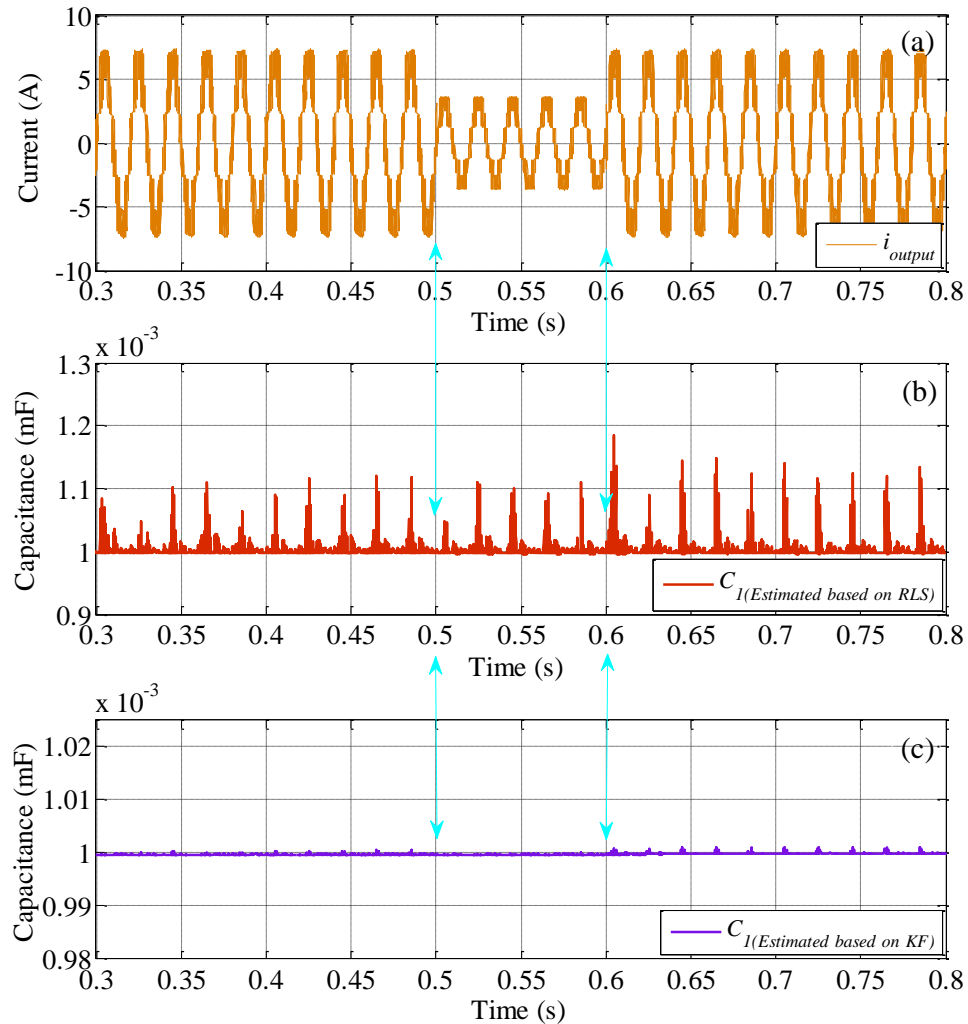
Fig 7.5 Capacitance estimation with step change in the load condition. (a) Capacitance estimation based on RLS algorithm. (b) Capacitance estimation based on KF algorithm / Simulation results.

Another test is carried out in Fig. 7.6 where a step change in the SM capacitance value has been applied. In this test, the SM capacitance has been changed from 1.0 mF to 2.0 mF. The two methods (i.e. RLS & KF) are performed well as can be seen in the figure; however, the proposed KF method still shows better performance.
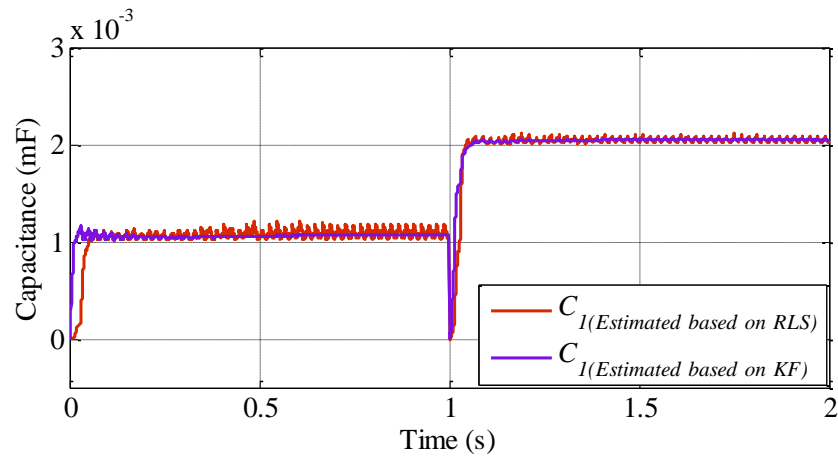
Fig 7.6. Capacitance estimation with step change in the SM capacitance value from 1.0 mF to 2.0 mF / Simulation results.

7.4 Chapter Summary

In this chapter, an online condition monitoring method for capacitors in the MMC is proposed. Owing to the series connections of high numbers of SMs in MMCs, the proposed method can be considered to be a very competitive solution in terms of reliability issues. The method is based on the KF approach, where comparisons have been made with the RLS algorithm. The results show very good performance with different operating conditions. The results obtained have verified the proposed method for a four-level MMC. Therefore, the idea can be attractive for HVDC systems where the MMC can include hundreds of SMs.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Summary

The aim of this chapter is to sum-up the findings and conclusions of the present study and to offer suggestions for some possible future work to extend the research. The work described in this thesis has focused on attempts to improve the overall performance of the MMC. A general framework on the requirements of challenges associated with MMCs has been presented. The main objective was to develop different estimation techniques to reduce overall system complexity. The work in this study has been divided into two main objectives: the design of sensorless based methods to achieve the voltage-balancing of the converter with fewer sensors, and an online capacitance estimation scheme which may improve the converter's reliability.

Chapter 2, discussed the most common challenges which are usually linked to MMCs. Achieving the voltage-balancing of the SM at lower cost has been investigated, considering up-to-date proposals in recent studies. Four groups of sensorless schemes were reviewed, which mainly consist of observer-based methods, open-loop control

methods, and sorting algorithm-based methods with fewer voltage and current sensors. One disadvantage of observer-based schemes is parameter uncertainty. As stated earlier in Chapter 2, no single study has fully determined the effect of the variation associated with arm inductance value on system performance. Instead, only the effect of variations in capacitance has been considered in previous studies. In the second group, different open-loop control methods were reviewed. Although these topologies do not use any form of feedback control, the well-known weaknesses of open-loop control methods can significantly compromise performance, especially when the MMC operates in conditions of dynamic change. Therefore, and due to the ease of implementing sorting algorithms, more attention was paid to the third and fourth groups of methods using soring algorithm-based techniques with fewer voltage and current sensors in order to devise new schemes for accomplishing converter stability with the minimum possible number of sensors.

An experimental set-up system has been developed in Chapter 3 before discussing the outcomes achieved using all of the proposed methods. Following this, detailed information on the system's implementation with sensorless and sensor-based proposed schemes was presented. The sensorless schemes were divided into two groups: current sensorless and voltage sensorless schemes.

The current sensorless schemes were evaluated and compared with the conventional sensor-based sorting algorithm scheme. In the first current sensorless scheme, the value of phase load current was used by the controller rather than arm load current. This improvement led to a 50% saving in sensor count when a comparison was made with the sensor-based scheme. In the second scheme, a further improvement in the number of sensors needed was achieved. Values of neither phase load current nor upper or lower arm current were needed to achieve the voltage-balancing of the converter topology. With the proposed methods, different PWM modulation techniques can be used. A further outcome with these two methods was that, both were able to easily increase their voltage levels with the use of a common interleaving technique. This means that a reduction in filtering size can be achieved. The methods were evaluated in simulation and practical studies with different voltage scales.

Different input and output conditions were applied to the system, including step changes in load state. Interestingly, the two methods showed some improvements when a load with a high inductance value was applied. Although the conventional sensor-based method showed higher oscillation, the average value of SM voltage was closer to its reference. These were the main outcomes of Chapter 4.

Two novel voltage sensorless methods have been also developed. Two original recursive algorithms are proposed for the MMC for the use in the voltage estimation technique. The techniques have some similarities in terms of the measurement used as input to the controller. In comparison with the sensor-based scheme, only the total arm voltages and switching pattern are required, with no additional hardware sensors needed. Although the use of a switching pattern is commonly used in estimation techniques, this research has proven for the first time, that the voltage drop caused by the semiconductor switch and the stray impedance of connecting wires have minimal effects on performance. Therefore, this outcome may support any other future estimation schemes which rely on switching patterns.

Different algorithms are combined with the conventional sorting algorithm in Chapters 5 and 6 in order to achieve an accurate SM estimation value. The ERLS-based method was developed first and its success has been confirmed by the results of extensive simulations and experiments. Various dynamic and steady-state analyses have been confirmed in practice for a 4-level MMC. In the simulation studies, a 9-level MMC has been successfully validated. The tests conducted evaluated the effect of different carrier switching frequencies, a sudden change in load conditions, the start-up transient condition, and DC faults. Interestingly a high level of agreement has been achieved for all tests between the simulation and experimental results obtained for the prototype.

One more important test was carried out for the converter to investigate the effect of deviation in capacitance on system performance. The effect of this type of deviation could theoretically have no effect on accuracy, since the proposed technique relies only on the SM voltages, arm voltage and the switching states and is independent of capacitance. However, further investigations of such deviations has also conducted in

Chapter 5. The results showed only a minor effect on estimation accuracy when high tolerances in SM capacitance values were considered. However, achieving more accurate results in terms of capacitance uncertainty would be preferable, which was the purpose of Chapter 6.

Another novel recursive algorithm was proposed based on the KF approach. In common with the proposed ERLS method, thus scheme does not require any specific control method to regulate capacitor voltage within the converter. Any conventional control method can be used with both the ERLS and KF algorithms. Therefore similar tests were carried out with the KF-based method. Some of the tests for normal and abnormal operating conditions showed similar performance levels in terms of the accuracy of the estimated values. Practical and simulation results of the tests investigating the effect of a step change in load and DC voltage conditions, and the consequences of low carrier frequency and start-up performance were nearly the same. Nevertheless, in comparison with the ERLS method, some of the KF results showed even better performance, such as in the effect of voltage ripple in the SM estimation value for normal operating conditions. Moreover, it was clearly observed that when the output level required for the MMC was high, the ERLS scheme needed a higher sampling frequency than the KF approach. Using the KF technique, only 20 kHz was sufficient for all simulated levels, while with ERLS the sampling frequency was proportional to the converter output voltage level needed. For the simulated levels of 16, 32 and 102 the sampling frequencies needed were 35, <50 and 250 kHz respectively. In addition, capacitance deviation had less effect compared to the ERLS-based method, thus demonstrating the superiority of the KF.

This improvement in parameter uncertainty paved the way for further investigation to develop a new scheme for capacitance estimation as discussed in Chapter 7. The studies reviewed in Chapter 2 only used the RLS algorithm as a capacitance estimation technique, and as the KF gave better results in terms of the effect of capacitance deviation in Chapter 6, it was expected that it may also give better results for capacitance estimation. Indeed, it has been found that the KF performed better than the RLS-based approach. Tests were carried out on a 4-level MMC for different

operating conditions. The proposed online estimation scheme can improve system reliability and, therefore, the idea can be attractive for HVDC systems where the MMC can include hundreds of cells.

To sum up, this research has achieved the main objectives stated earlier in Chapter 1. Therefore, it can be said that applying such contributions may improve MMC performance with lower cost and complexity.

8.2 Future Work

The work achieved in this thesis leads to the possibility of further investigation, this including the following:

> ➢ Applying the proposed voltage estimation schemes with different multilevel converters such as FCC and CHB converters.

> ➢ Extending the implementation of the proposed voltage estimation algorithms with parallel processor features such as the FPGA.

> ➢ Investigate other recursive algorithms and compare them with the proposed capacitance and voltage estimation schemes.

> ➢ Combination of the proposed current and voltage sensorless schemes and investigate the outcome results. This may include: combination of load current monitoring method with ERLS / Kalman filter voltage sensorless method or sensor-never current monitoring scheme with ERLS / Kalman filter voltage sensorless method.

> ➢ Developing alternative or hybrid configurations of multilevel topologies which may reduce the drawbacks of multilevel converters in general.

REFERENCES

[1]   N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Transactions on Power Electronics,* vol. 24, pp. 592-602, 2009.

[2]   J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 724-738, 2002.

[3]   J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 2930-2945, 2007.

[4]   J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. Á. M. Prats*, et al.*, "Multilevel Converters: An Enabling Technology for High-Power Applications," *Proceedings of the IEEE,* vol. 97, pp. 1786-1817, 2009.

[5]   H. Miyazaki, H. Fukumoto, S. Sugiyama, M. Tachikawa, and N. Azusawa, "Neutral-point-clamped inverter with parallel driving of IGBTs for industrial applications," *Industry Applications, IEEE Transactions on,* vol. 36, pp. 146-151, 2000.

[6]   P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model Predictive Control of Multilevel Cascaded H-Bridge Inverters," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2691-2699, 2010.

[7]   J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats*, et al.*, "Multilevel Converters: An Enabling Technology for High-Power Applications," *Proceedings of the IEEE,* vol. 97, pp. 1786-1817, 2009.

[8]   S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu*, et al.*, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2553-2580, 2010.

[9]   C. Silva, S. Kouro, J. Soto, and P. Lezana, "Control of an hybrid multilevel inverter for current waveform improvement," in *2008 IEEE International Symposium on Industrial Electronics*, 2008, pp. 2329-2335.

[10]   S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics,* vol. 30, pp. 37-53, 2015.

[11]   H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," *IEEE Transactions on Power Electronics,* vol. 26, pp. 3119-3130, 2011.

[12]   B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Transmission and Distribution Conference and Exposition, 2008. T&D. IEEE/PES*, 2008, pp. 1-16.

[13]   A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 2003, p. 6 pp. Vol.3.

[14]   G. Minyuan, X. Zheng, and C. Hairong, "Control and modulation strategies for modular multilevel converter based HVDC system," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 849-854.

[15]   H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3119-3130, 2011.

[16]   G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *Industrial Electronics and Applications, 2009. ICIEA 2009. 4th IEEE Conference on*, 2009, pp. 3399-3404.

[17]   J. W. Moon, C. S. Kim, J. W. Park, D. W. Kang, and J. M. Kim, "Circulating Current Control in MMC Under the Unbalanced Voltage," *IEEE Transactions on Power Delivery,* vol. 28, pp. 1952-1959, 2013.

[18]   R. Picas, J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, 2013, pp. 318-324.

[19]   F. Deng and Z. Chen, "Voltage-Balancing Method for Modular Multilevel Converters Switched at Grid Frequency," *IEEE Transactions on Industrial Electronics,* vol. 62, pp. 2835-2847, 2015.

[20]   G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electronics,* vol. 6, pp. 96-107, 2013.

[21]   L.-A. G. Wei LI, Jean BÉLANGER, "Control and Performance of a Modular Multilevel Converter System," September 6-8 2011.

[22]   R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 502-507.

[23]   A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A Space-Vector PWM-Based Voltage-Balancing Approach With Reduced Current Sensors for Modular Multilevel Converter," *IEEE Transactions on Industrial Electronics,* vol. 63, pp. 2734-2745, 2016.

[24]   S. Lu, L. Yuan, K. Li, and Z. Zhao, "An Improved Phase-Shifted Carrier Modulation Scheme for a Hybrid Modular Multilevel Converter," *IEEE Transactions on Power Electronics,* vol. 32, pp. 81-97, 2017.

[25]   Y. Long, X. Xiao, Y. Xu, Y. Xu, and B. Yu, "A hybrid Modulation method for improved modular multilevel converter applied for power quality compensation in medium voltage," in *2013 1st International Future Energy Electronics Conference (IFEEC)*, 2013, pp. 789-793.

[26]   G. S. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Operation of a modular multilevel converter with selective harmonic elimination PWM," in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 999-1004.

[27]   P. M. Meshram and V. B. Borghate, "A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)," *IEEE Transactions on Power Electronics,* vol. 30, pp. 450-462, 2015.

[28]   M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 24, pp. 1737-1746, 2009.

[29]   F. Deng and Z. Chen, "A Control Method for Voltage Balancing in Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 29, pp. 66-76, 2014.

[30]   M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," *IEEE Transactions on Power Delivery,* vol. 25, pp. 2903-2912, 2010.

[31]   M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," in *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-1.

[32]   R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A Modified Voltage Balancing Algorithm for the Modular Multilevel Converter: Evaluation for Staircase and Phase-Disposition PWM," *IEEE Transactions on Power Electronics,* vol. 30, pp. 4119-4127, 2015.

[33]   G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *2009 4th IEEE Conference on Industrial Electronics and Applications*, 2009, pp. 3399-3404.

[34]   M. A. Perez and J. Rodriguez, "Generalized modeling and simulation of a modular multilevel converter," in *Industrial Electronics (ISIE), 2011 IEEE International Symposium on*, 2011, pp. 1863-1868.

[35]   M. Guan and Z. Xu, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," *IEEE Transactions on Power Electronics,* vol. 27, pp. 4858-4867, 2012.

[36]   S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control," *IEEE Transactions on Power Electronics,* vol. 30, pp. 358-371, 2015.

[37]   A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "Dynamic Voltage Balancing Algorithm for Modular Multilevel Converter: A Unique Solution," *IEEE Transactions on Power Electronics,* vol. 31, pp. 952-963, 2016.

[38]   H. Peng, Y. Wang, Z. Lv, Y. Deng, X. He, and R. Zhao, "Capacitor voltage balancing based on fundamental frequency sorting algorithm for modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 1639-1644.

[39]   D. Basic, F. Malrait, and P. Rouchon, "Euler-Lagrange Models With Complex Currents of Three-Phase Electrical Machines and Observability Issues," *IEEE Transactions on Automatic Control,* vol. 55, pp. 212-217, 2010.

[40]   S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson, "Fault Detection for Modular Multilevel Converters Based on Sliding Mode Observer," *IEEE Transactions on Power Electronics,* vol. 28, pp. 4867-4872, 2013.

[41]   M. Almaleki, "*Sliding mode observation of capacitor voltage in multilevel power converters*," (2010), PhD Thesis, Univesity of Nottingham

[42]   M. Almaleki, P. Wheeler, and J. Clare, "Sliding mode observation of capacitor voltage in multilevel power converters," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[43]   O. Abushafa, S. Gadoue, M. Dhaidah, and D. Aktinson, "Capacitor voltage estimation in modular multilevel converters using a Kalman filter algorithm," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, 2015, pp. 3016-3021.

[44]   H. Nademi, A. Das, and L. E. Norum, "Modular Multilevel Converter With an Adaptive Observer of Capacitor Voltages," *IEEE Transactions on Power Electronics,* vol. 30, pp. 235-248, 2015.

[45]   S. D'Arco and J. A. Suul, "Estimation of sub-module capacitor voltages in modular multilevel converters," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[46]   R. Picas, J. Zaragoza, J. Pou, S. Ceballos, and J. Balcells, "New Measuring Technique for Reducing the Number of Voltage Sensors in Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 31, pp. 177-187, 2016.

[47]   R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable Modular Multilevel Converter Fault Detection With Redundant Voltage Sensor," *IEEE Transactions on Power Electronics,* vol. 32, pp. 39-51, 2017.

[48]   K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," *IEEE Transactions on Power Electronics,* vol. 27, pp. 3482-3494, 2012.

[49]   K. H. Ahmed and G. P. Adam, "New modified staircase modulation and capacitor balancing strategy of 21-level modular multilevel converter for HVDC transmission systems," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, 2014, pp. 1-6.

[50]   L. Kwang-Woon, K. Myungchul, Y. Jangho, L. Kwang-Woon, and Y. Ji-Yoon, "Condition Monitoring of DC-Link Electrolytic Capacitors in Adjustable-Speed Drives," *Industry Applications, IEEE Transactions on,* vol. 44, pp. 1606-1613, 2008.

[51]   A. M. R. Amaral and A. J. M. Cardoso, "A Simple Offline Technique for Evaluating the Condition of Aluminum–Electrolytic–Capacitors," *Industrial Electronics, IEEE Transactions on,* vol. 56, pp. 3230-3237, 2009.

[52]   S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Transactions on Power Electronics,* vol. 25, pp. 2734-2752, 2010.

[53]   Y. J. Jo, T. H. Nguyen, and D. C. Lee, "Condition monitoring of submodule capacitors in modular multilevel converters," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 2121-2126.

[54]   U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *Power Delivery, IEEE Transactions on,* vol. 26, pp. 316-324, 2011.

[55]   S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, W. Bin*, et al.*, "Recent Advances and Industrial Applications of Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2553-2580, 2010.

[56]   J. R. Rodriguez, J. Pontt, M. Perez, P. Lezana, and P. W. Hammond, "High Power Synchronous Machine fed by a Cascaded Regenerative Inverter," in *2008 IEEE Industry Applications Society Annual Meeting*, 2008, pp. 1-7.

[57]   H. Yang and M. Saeedifard, "A Capacitor Voltage Balancing Strategy With Minimized AC Circulating Current for the DC–DC Modular Multilevel Converter," *IEEE Transactions on Industrial Electronics,* vol. 64, pp. 956-965, 2017.

[58]   J. Zhang, Z. Wang, and S. Shao, "A Three-Phase Modular Multilevel DC–DC Converter for Power Electronic Transformer Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 5, pp. 140-150, 2017.

[59]   Q. Ren, C. Sun, and F. Xiao, "A Modular Multilevel DC–DC Converter Topology With a Wide Range of Output Voltage," *IEEE Transactions on Power Electronics,* vol. 32, pp. 6018-6030, 2017.

[60]   B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "High-Frequency-Link Modulation Methodology of DC–DC Transformer Based on Modular Multilevel Converter for HVDC Application: Comprehensive Analysis and Experimental Verification," *IEEE Transactions on Power Electronics,* vol. 32, pp. 3413-3424, 2017.

[61]   Y. Chen, Y. Cui, X. Wang, X. Wei, and Y. Kang, "Design and implementation of the low computational burden phase-shifted modulation for DC–DC modular multilevel converter," *IET Power Electronics,* vol. 9, pp. 256-269, 2016.

[62]   A. A. J. Far, M. Hajian, D. Jovcic, and Y. Audichya, "High-power modular multilevel converter optimal design for DC/DC converter applications," *IET Power Electronics,* vol. 9, pp. 247-255, 2016.

[63]   X. Zhang, T. C. Green, and A. Junyent-Ferré, "A New Resonant Modular Multilevel Step-Down DC–DC Converter with Inherent-Balancing," *IEEE Transactions on Power Electronics,* vol. 30, pp. 78-88, 2015.

[64]   L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *Industrial Electronics Magazine, IEEE,* vol. 2, pp. 28-39, 2008.

[65]   F. B. Ajaei and R. Iravani, "Dynamic Interactions of the MMC-HVDC Grid and its Host AC System Due to AC-Side Disturbances," *IEEE Transactions on Power Delivery,* vol. 31, pp. 1289-1298, 2016.

[66]   L. Cai, U. Karaagac, and J. Mahseredjian, "Simulation of Startup Sequence of an Offshore Wind Farm With MMC-HVDC Grid Connection," *IEEE Transactions on Power Delivery,* vol. 32, pp. 638-646, 2017.

[67]   Y. Liang, J. Liu, T. Zhang, and Q. Yang, "Arm Current Control Strategy for MMC-HVDC Under Unbalanced Conditions," *IEEE Transactions on Power Delivery,* vol. 32, pp. 125-134, 2017.

[68]   S. Samimi, F. Gruson, P. Delarue, F. Colas, M. M. Belhaouane, and X. Guillaud, "MMC Stored Energy Participation to the DC Bus Voltage Control in an HVDC Link," *IEEE Transactions on Power Delivery,* vol. 31, pp. 1710-1718, 2016.

[69]   R. Vidal-Albalate, H. Beltran, A. Rolán, E. Belenguer, R. Peña, and R. Blasco-Gimenez, "Analysis of the Performance of MMC Under Fault Conditions in HVDC-Based Offshore Wind Farms," *IEEE Transactions on Power Delivery,* vol. 31, pp. 839-847, 2016.

References

[70] G. Minyuan and X. Zheng, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 4858-4867, 2012.

[71] V. G. A. g. E. Acha, O. Anaya-Lara and T.J.E. Miller, *Power Electronic Control in Electrical Systems*. Great Britian MPG Books Ltd, Bodmin, Cornwall, 2002.

[72] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency Assessment of Modular Multilevel Converters for Battery Electric Vehicles," *IEEE Transactions on Power Electronics,* vol. 32, pp. 2041-2051, 2017.

[73] Y. Okazaki, W. Kawamura, M. Hagiwara, H. Akagi, T. Ishida, M. Tsukakoshi, *et al.*, "Experimental Comparisons Between Modular Multilevel DSCC Inverters and TSBC Converters for Medium-Voltage Motor Drives," *IEEE Transactions on Power Electronics,* vol. 32, pp. 1805-1817, 2017.

[74] A. Antonopoulos, L. Ängquist, L. Harnefors, and H. P. Nee, "Optimal Selection of the Average Capacitor Voltage for Variable-Speed Drives With Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 30, pp. 227-234, 2015.

[75] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *IEEE Transactions on Power Electronics,* vol. 30, pp. 349-357, 2015.

[76] A. Soukup. Enabling greener embedded control systems with floating-point DSCs [Online].

[77] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, and V. G. Agelidis, "Circulating current control and evaluation of carrier dispositions in modular multilevel converters," in *2013 IEEE ECCE Asia Downunder*, 2013, pp. 332-338.

[78] Y. Zhu, *Multivariable system identification for process control*: Elsevier, 2001.

[79] J. A. Apolinário, *QRD-RLS adaptive filtering*: Springer, 2009.

[80] A. Vahidi, A. Stefanopoulou, and H. Peng, "Recursive least squares with forgetting for online estimation of vehicle mass and road grade: theory and experiments," *Vehicle System Dynamics,* vol. 43, pp. 31-55, 2005.

[81] S. S. Haykin, *Adaptive filter theory*: Pearson Education India, 2008.

[82] M. Badoni, A. Singh, and B. Singh, "Variable Forgetting Factor Recursive Least Square Control Algorithm for DSTATCOM," *IEEE Transactions on Power Delivery,* vol. 30, pp. 2353-2361, 2015.

[83] J. A. Apolinário and J. G. McWhirter, *QRD-RLS Adaptive Filtering*: Brazil, Springer, 2009.

[84]   M. A. Eleffendi and C. M. Johnson, "Application of Kalman Filter to Estimate Junction Temperature in IGBT Power Modules," *IEEE Transactions on Power Electronics,* vol. 31, pp. 1576-1587, 2016.

[85]   L. Cao and H. M. Schwartz, "Analysis of the Kalman filter based estimation algorithm: an orthogonal decomposition approach," *Automatica,* vol. 40, pp. 5-19, 1// 2004.

[86]   F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters," *IEEE Transactions on Power Electronics,* vol. 30, pp. 2721-2732, 2015.

[87]   R. Antonello, K. Ito, and R. Oboe, "Acceleration Measurement Drift Rejection in Motion Control Systems by Augmented-State Kinematic Kalman Filter," *IEEE Transactions on Industrial Electronics,* vol. 63, pp. 1953-1961, 2016.

[88]   S. Shao, A. J. Watson, J. C. Clare, and P. W. Wheeler, "Robustness Analysis and Experimental Validation of a Fault Detection and Isolation Method for the Modular Multilevel Converter," *IEEE Transactions on Power Electronics,* vol. 31, pp. 3794-3805, 2016.

[89]   K. Abdennadher, P. Venet, G. Rojat, J. M. Retif, and C. Rosset, "A Real-Time Predictive-Maintenance System of Aluminum Electrolytic Capacitors Used in Uninterrupted Power Supplies," *Industry Applications, IEEE Transactions on,* vol. 46, pp. 1644-1652, 2010.

APPENDIX A

Derivation of RLS Algorithm

Explaining the equations stated in table 5.1, requires the general model which is described in (5.1)-(5.3). By considering the matrix form of (5.2) the estimation value of θ is given by [81]:

$$\hat{\theta}_{(t_i)} = [\mathbb{Z}^T_{(t_i)} \mathbb{Z}_{(t_i)}]^{-1} \mathbb{Z}^T_{(t_i)} y_{(t_i)} \tag{A.1}$$

For simplicity redefine $\mathbb{Z}_{(t_i)}$ Substute Thus, the derivation can be given as follows:

First define $\mathbb{Z}^T_{(t_i)} \mathbb{Z}_{(t_i)} = P^{-1}_{(t_i)}$,

Thus
$$P^{-1}_{(t_i)} = \sum_{t_0}^{t_i} z_{(t_i)} z^T_{(t_i)} = \sum_{t_0}^{t_{i-1}} z_{(t_i)} z^T_{(t_i)} + z_{(t_i)} z^T_{(t_i)} \tag{A.2}$$

$$P^{-1}_{(t_i)} = P^{-1}_{(t_{i-1})} + z_{(t_i)} z^T_{(t_i)} \tag{A.3}$$

The term $\mathbb{Z}^T_{(t_i)} y_{(t_i)}$ in (A.1) can be rewritten as follows:

$$\mathbb{Z}^T_{(t_i)} y_{(t_i)} = \mathbb{Z}^T_{(t_{i-1})} y_{(t_i)} + z_{(t_i)} z^T_{(t_i)} \tag{A.4}$$

Recall (A.1) and $\mathbb{Z}^T_{(t_i)} \mathbb{Z}_{(t_i)}$ by $P^{-1}_{(t_i)}$ and substitute (A.4) into (A.1):

$$\hat{\theta}_{(t_i)} = P_{(t_i)} \mathbb{Z}^T_{(t_i)} y_{(t_i)} = P_{(t_i)} (\mathbb{Z}^T_{(t_{i-1})} y_{(t_{i-1})} + z_{(t_i)} y_{(t_i)}) \tag{A.5}$$

Because the parameter estimate of $\hat{\theta}_{(t_i)}$ at the time instant (t_{i-1}), can be given as:

$$\hat{\theta}_{(t_i-1)} = P_{(t_{i-1})} \mathbb{Z}^T_{(t_i-1)} y_{(t_i-1)} \tag{A.6}$$

and
$$P^{-1}_{(t_{i-1})} \hat{\theta}_{(t_i-1)} = \mathbb{Z}^T_{(t_i-1)} y_{(t_i-1)} \tag{A.7}$$

Therefore,

$$\hat{\theta}_{(t_i)} = \hat{\theta}_{(t_{i-1})} + P_{(t_i)}z_{(t_i)}(y_{(t_i)} - z^T_{(t_i)}\hat{\theta}_{(t_i-1)}) \qquad (A.8)$$

$$\hat{\theta}_{(t_i)} = \hat{\theta}_{(t_{i-1})} + K_{(t_i)}e_{y_{(t_i)}} \qquad (A.9)$$

Where

$$e_{y_{(t_i)}} = y_{(t_i)} - z^T_{(t_i)}\hat{\theta}_{(t_i-1)} \qquad (A.10)$$

$$, K_{(t_i)} = P_{(t_i)}z_{(t_i)} \qquad (A.11)$$

And

$$P_{(t_i)} = (P^{-1}{}_{(t_{i-1})} + z_{(t_i)}z^T_{(t_i)})^{-1} \qquad (A.12)$$

In order to find the invers of (A.12), a mathematical expression called the matrix inversion lemma is used:

$$(A + BCD)^{-1} = A^{-1} - A^{-1}B(C^{-1} + DA^{-1}B)^{-1}DA^{-1} \qquad (A.13)$$

The expression given in (A.13) is called matrix inversion lemma, and by rearrange (A.13) with $A = P^{-1}{}_{(t_{i-1})}, B = z_{(t_i)}, C = 1$, and $D = z^T{}_{(t_i)}$, the covariance matrix $P_{(t_i)}$ can be written as:

$$P_{(t_i)} = P_{(t_{i-1})} - \frac{P_{(t_{i-1})}z_{(t_i)}z^T_{(t_i)}P_{(t_{i-1})}}{1 + z^T_{(t_i)}P_{(t_{i-1})}z_{(t_i)}} \qquad (A.14)$$

From (A.9) and (A.12) the gain $K_{(t_i)}$ can by rewritten by:

$$K_{(t_i)} = \frac{P_{(t_{i-1})}z_{(t_i)}}{1 + z^T_{(t_i)}P_{(t_{i-1})}z_{(t_i)}} \qquad (A.15)$$

$$\hat{\theta}_{(t_i)} = \hat{\theta}_{(t_i-1)} + K_{(t_i)}(y_{(t_i)} - z^T_{(t_i)}\hat{\theta}_{(t_i-1)}) \qquad (A.16)$$