Distributed static series compensator in 11kV networks

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A thesis submitted for the degree of
Philosophy of Doctorate

May 2015

Newcastle University School of Electrical, Electronic & Computer Engineering

Abstract

Series compensation techniques can be very effective when applied in an electrical network to increase the power transfer capacity of existing power lines. Distributed Static Series Compensation (DSSC) is a power electronics based series compensation scheme in which a DSSC device comprises of a single-phase H-bridge voltage source converter, a dc link capacitor and a low pass filter suspended from the power line via a single turn transformer. The application of DSSC in the 11kV distribution network is investigated in this thesis. This is followed by a study of existing control strategies employed in DSSC and Static Synchronies Series Compensation (SSSC) schemes.

Most of these controllers are based on dq transformation methods in which balanced conditions are assumed and zero sequence currents are assumed to be negligible. While this might be a reasonable assumption at transmission level voltages, but it can be argued that in the presence of unbalanced loads and currents (a common feature of lower voltage distribution networks) these strategies can be inaccurate, leading to the wrong amount of compensation being injected. In addition some of the studied controllers are based on the 90° phase shift of line current. Practically, the injection angle must be slightly different in order to compensate the internal losses of the DSSC. The need for the diversion from the 90° can change over the time and this can threaten the stability of the system.

A new single-phase control strategy based on the instantaneous power exchange between the DSSC devices and each of the three phase conductors is proposed in this thesis to address this issue. The new control method does not employ a dq transformation and is immune from the probable errors resulting from the presence of unbalanced network conditions. In the same time the injection angle is not fixed and it is adjusted by the controller.

The operation of DSSC can be categorized in two modes and transfer function of system is obtained based on these two modes. The transfer function is used in the design of controller. This is followed by analyzing immunity of the designed controller against change of system parameters. The proposed scheme is simulated (using PSCAD software) to examine the operation of the new control method and the resulting impact on the 11kV distribution feeder, including the ability to divert power from one line to another and the ability to improve network voltage profiles. Performance of DSSC using the proposed controller is compared with performance of DSSC when the traditional controllers are employed.

Effect of line resistance on the performance of the DSSC is studied and relation between the compensation and X/R ratio of compensated line is highlighted. A fault management study is conducted in order to find a fault recovery strategy in the occurrence of fault.

A 50V test rig has been designed and built to verify the operation of the DSSC devices employing the new control method. This includes the design and construction of a single turn transformer (STT), filter and all of required electronic boards to execute the control strategy. Different types of low pass filters are investigated and their capabilities are considered in selection of power topology of filter. Capacitive and inductive injection capability of the proposed controller is examined power flow control capability is demonstrated. Results obtained from the test rig are in good agreement with simulations validating the proposed controller. The experimental results of proposed controller are compared against those of traditional controller.

ACKNOWLEDGEMENT

First of all, I would like to thank all people who have encouraged me in pursuing this research topic and for having always supported me during the course. I am grateful to all my friends in the Power Electronics, Drives and Machines group (PEDM) at the School of Electrical and Electronic Engineering, Newcastle University. Their discussion was extremely helpful. I also take this opportunity to express my gratitude to the administrative, especially Ms. Gill Webber, and technical staffs at the school, whose have made my work as trouble-free as possible. I would like to express my appreciation to my supervisor Dr Bashar Zahawi and my examiners Dr Shady Gadoue and Dr Ahmed Khaled who provided productive comments.

I also would like to dedicate this work to my parents, who had always filled up my memory with their sweetest love. I am really missing them as well as their encouragement and support in my life. They have sacrificed whatever they could in order to get me educated and understood importance of lifetime study. Without bearing that in my mind I would not be as I am nowadays.

The list of thanks would not be complete without special thanks to my brother and sisters who have always been there when I need help. Bringing me up and guiding me with their endless love, they always mean a lot to me throughout my life.

At last but not least, I would like to express my deep gratitude to my beloved wife and my dearest son for their patience with the time spent away from them, their love and support throughout the work. Thank you, Sara, because I could not have finished the writing without your support and love. Thank you, Aryaz, for being my joy and motivation of my life.

Newcastle University, May of 2015

Afshin Pashaei

List of Symbols

w	Angular frequency
B	Flux density
H	Magnetic field strength
μ	Magnetic permeability
Hz	Hertz
kN	Kilo neton
lb	Pound
Ω	Ohm
P_w	Horizontal force of wind
X_L	Line reactance
V_s	rms value of sending end bus voltage
V_r	rms value of receiving end bus voltage
P_{sr}	Receiving end power
δ	Load angle
X_{inj}	Injected reactance
K	Boost Factor
X_C	Reactance of TCSC device capacitor
X_{TCSC}	Effective reactance of TCSC
λ	Root square X_C divided by X_L
β	Firing advance angle
i_L	Line current
DC	Link Electrical node across the DC capacitor
V_{inj}	Phasor of injected voltage
I_l	Phasor of line current
V_{injp}	Direct component of V_{inj}
V_{injq}	Quadrature component of Vinj
α	Phase angle between injected voltage and line current
Q_{sr}	Receiving end reactive power
F_2	Generated force by mass of DSSC module
F_1	Generated force by mass of line
F	Sum of two forces F_1 and F_2
F_H	Generates force by line
T_v	Vertical load on the cross-arm

W_w	Weight of wire
il	Cross section of ice load
dw	Cross section of wire
T_{t1}	Horizontal force of wind
P_w	Wind pressure
S_w	Effective length of the span
T_{t2}	Resultant horizontal force
H_{ten}	Horizontal tension
L_{min}	Minimum distance between line and pole
PC	Minimum distance between two phases
F_v	Vertical force on to the pole
S_l	Length of span
F_{WH}	Horizontal force generated by the wind
W_{mf}	Maximum wind force through one meter of wire
ρ	Parameter defined by environmental parameters
V_d	d component of the reference signal
V_q	q component of the reference signal
I_{dcref}	Reference dc current
I_{dc}	Measured DC current
K_c	Percentage of the compensation
L_{XS}	Inductances of the line at the sending end bus
L_{RS}	Inductances of the line at the receiving end bus
I_{abc}	Amplitude of current in three phases
I_d	Direct component of line current
I_q	Quadrature component of line current
V_{dc}	Voltage across the dc link
V_{Ave}	Average voltage
θ_{dc}	Angle needed for adjustment of dc voltage
θ_{an}	From the PLL
V_{Cinj}	Calculated capacitive compensation voltage
V_{Linj}	Calculated inductive compensation voltage
p(t)	Instantaneous power
$V(t)_{Inj}$	Instantaneous injected voltage
$I(t)_{Line}$	Instantaneous line current

I_{CE}	Current flowing from collector to emitter
V_{CE}	Voltage across collector emitter
V_{GE}	Voltage across gate emitter
Wt	Withstand time
R_G	Resistor between the gate drive and IGBT
Ipeak	Maximum peak output current of gate drive
Re	External resistor
V_{PN}	Input voltage of transducer
V_{PN}	Measured current at the primary of transducer
$\mathcal{R}$	Reluctance
r	Thickness of the core
l	Length of the cylinder
N	Number of turns of the winding around the core
A	Net cross-sectional area of the core
f_c	Cut off frequency
vr	Percentage of the ripple on dc voltage
V_{drop}	Voltage drop across a segment of line

Abbreviations

DSSC	Distributed static series compensator
FACTS	Flexible AC transmission system
UPFC	Unified Power Flow Controller
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
ATC	Available Transmission Capacity
SSR	Sub-synchronous resonance
SSSC	Static synchronous series compensators
STT	Single turn transformer
MVAr	Mega var
MOV	Metal Oxide Varistor
SCL	Short circuit level
TSSC	Thyristor Switched Series Capacitors
TCSC	Thyristor Controlled Series Compensation
GCSC	GTO Thyristor-Controlled Series Capacitor
GTO	Gate turn off Thyristor
IGBT	Insulated Gate Bipolar Transistors
TSC	Thyrsitor switched capacitor
SVC	Static VAr Compensators
SVS	Synchronous Voltage Source
VSC	Voltage Source Converter
SSSC	Static Synchronous Series Compensation
SSR	Sub-Synchronous Resonance
DSPS	Distributed static phase shifter
MTTR	Mean time to repair
D-FACTS	Distributed flexible AC transmission system
ACSR	Aluminium-conductor steel-reinforced
MCP	Maximum Conductor Pressure
MCW	Maximum Conductor Weight
AAAC	All Aluminium Alloy Conductors
CSI	Current source inverter
PWM	Pulse width modulation
PLL	Phase locked loop

TOV	Transient Over Voltage
VT	Voltage transducer
PCB	Printed circuit board
Op-amp	Operational amplifier
CT	Current Transducer
EMF	Electromechanical force
DMA	Direct Memory Access
ADC	Analogue to Digital Converter
RAM	Read access memory
CPU	Central processing unit
I/O	Input output
MW	Mega watt
VA	Volt amper
MVA	Mega volt amper
UG lab	Upper ground lab

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1 Introduction

1.1 Background

Distributed static series compensator (DSSC) is a type of FACTS (Flexible AC Transmission System) devices that is utilized to compensate the line reactance in electrical networks. Through means of series compensation the line reactance can be reduced and the Available Transmission Capacity (ATC) can be increased. It can then maximize the utilization of the existing networks and postpone the construction of new electrical networks.

However, series compensation traditionally is achieved by implementation of fixed capacitors in series through the power lines. The combination of fixed capacitors and inductance of the line can initiate sub-synchronous resonance (SSR) phenomenon. This is a challenging issue with the application of fixed capacitors and it is established the idea of using power electronics based compensations.

DSSC is the most novel power electronic based series compensation in the transmission lines. Furthermore, by connection of solar generators and wind farms (in most of the cases) to the distribution networks the need of expansion in these networks become more important. Application of DSSC in the 11kV distribution networks along with a new control strategy to enhance the performance of the DSSC device has been introduced in this study. The proposed control system has been simulated and simulation results are presented to validate the proposed scheme. In addition a test bench has been designed and implemented to conduct experimental tests.

1.2 Research objectives

This research focuses on series compensation and the aim, thus, is to primarily build up an inclusive understanding of the principle of series compensation. This includes investigation of existing series compensation solutions and highlighting their strengths and weaknesses. For example, the concept of fixed capacitors and power electronics based compensators are required to be studied in depth and their advantages and disadvantages identified. Sequentially, applied control strategies are required to be studied and drawbacks to be identified.

Control strategy of DSSC device has not received adequate attention in the literature and in most of the cases it is simply limited to stating that the injected voltage by DSSC must be orthogonal to the line current [1]. In the same time among series compensation devices, Static Synchrounes Series Compensator (SSSC) also operates with the same concept [2]. This is encouraging to consider investigating control strategies which have been employed within SSSC devices. However those strategies are mainly based on the abc to dq conversion [3] which they have own disadvantages in presence of unbalance AC system. Most of these controllers employ dq conversion in which balanced conditions and negligible zero sequence are necessary assumptions. The assumptions might be sensible at transmission level, however because of presence of unbalanced loads and currents it can be unreasonable assumption the distribution networks. As a result these strategies can be erroneous and provide wrong amount of compensation being injected.

Some of the control strategies are based on the 90° phase shift and practically in order to compensate the internal losses of the DSSC the voltage is slightly diverted from 90°. The diversion can vary over the time and this can put the stability of the system at risk.

A new control system needs to be developed to overcome drawbacks with the existing control systems. The controller must guaranty the 90° voltage injection and regulate the DC voltage at the desired value. It should be immune against the unbalance of the AC system and should provide reference signal for DSSC modules installed in three phase independently from each other. In order to address these requirements a new single-phase controller conceptually based on the instantaneous power exchange between power system and DSSC is proposed.

The developed control therefore is simulated and tested experimentally. In order to conduct experimental tests, a test rig is designed and implemented.

The objectives of the research are:

- To build up a broad understanding of series compensations
- To identify the drawbacks within the existing series compensation methods
- To investigate potential application of DSSC in 11kV distribution networks
- To develop an understanding of existing control methods and their drawbacks
- To develop a new control method for enhancing the performance of the system
- To design and implement a single turn transformer and a test rig for conducting of experimental tests
- To validate the proposed control strategy

1.3 Thesis layout

This thesis introduces application of DSSC devices in 11kV distribution networks. At the same time it develops a new control method to enhance the performance of DSSC.

In chapter 2 a brief summary of compensations is stated and the principle of series compensation and available commercial solutions are explained and examined. Furthermore, their power topologies and the associated advantages and disadvantages are clarified. Fixed series capacitors, as a traditional and simple solution, are investigated in detail. This is then followed by explanation of power electronics based series compensators. In this category static synchronous series compensators (SSSC) are explained in detail and their drawbacks explained. DSSC is found to overcome some of the issues of application of SSSC in the electrical networks. It is followed by explanation of power topology and principle of operation of DSSC.
Subsequently, existing control algorithms of SSSC and DSSC are explained. The advantages and disadvantages of different control systems (existing control strategies in the literature review) have been studied. The drawback with dq conversion based controllers has been presented.
Chapter 3 presents potential applications of DSSC in 11kV distribution networks. Different applications of the DSSC device has been explained and simulated. The effect

of line resistance on the performance of DSSC has been investigated. Relationship between X/R ratio and power transfer capability of line with and without compensation is studied. In this chapter it has been shown that how this device can improve the voltage profile through an 11kV distribution feeder.. It has been shown that the device can contribute toward power flow control by diverting current from one line to another one.

Chapter 4 is organized so that it primarily introduces the novel control algorithms and thereupon presents simulation results of its utilization. The modelling approach of DSSC to be employed in controller design using MATLAB is also explained in this chapter. The designed controller is implemented in the PSCAD model and the simulation results show the capability of controller in the injection of both capacitive and inductive voltages through the line. Sensitivity of the designed controller against change of system parameters has been investigated. An exhaustive list of simulation result comparing the performance of the developed controller with the performance of the traditional controllers is presented. Satisfactory performance of the developed controller in presence of unbalance system and voltage dip has been demonstrated. A fault management strategy has been developed in this chapter and the related simulation results are presented. An investigation regarding the effect of change of power system parameters on the performance of the DSSC has been conducted.

The design procedure of the test rig is presented in chapter 5. The explained procedure includes design of single turn transformer (STT), LC filter, all electronics and power electronics boards. This is followed by demonstrating full design steps of STT to be employed in an 11kV system. Different type of low pass filters has been studied and LC filter is selected to be employed in the DSSC device. Moreover, all hardware design calculations and implementation process are included. Finally, the chapter includes the procedure of conducting the experimental tests and the description of low voltage power system required for the tests. The experimental tests include demonstrating the capability of developed controller in injecting capacitive and inductive reactance through the line. Thereafter, performance of the proposed controller is compared with a traditional controller. Finally, load flow capability of DSSC has been demonstrated.

In chapter 6 represents the conclusions and author contributions. The publication from this research work is listed. This is followed by recommendations for the future works.

At the end of the thesis four appendixes A, B, C and D are presented. Appendix A provides expanded information about dq conversion and appendix B is about components specifications. Appendix C presents detailed information about microcontroller respectively. Feasibility study of application of DSSC devices in 11kV distribution networks in terms of mechanical withstand capability of the existing networks has been demonstrated in appendix D

2 Compensation in electrical networks

This chapter describes different types of compensations including series, shunt and hybrid in the electrical networks. Shunt and hybrid compensators are explained briefly as they are not main subject of study. However series compensators are explained exhaustively with comprehensive literature review. This includes all available series compensation methods and related topologies.

This chapter presents the principle of control of SSSC and DSSC and it is followed by investigation on the existing employed control strategies in their applications. The advantages and disadvantages of the controllers are also discussed.

2.1 Compensation methods

Compensation in electrical networks can be achieved in different ways and they can be employed to increase efficiency of the AC system and enhance its controllability. Efficiency of the system can be increased by optimal utilizing of ATC and avoiding unnecessary reactive power flow through the power lines [4], [5]. Different types of compensation, shunt, series and hybrid are categorized in Fig.2.1.

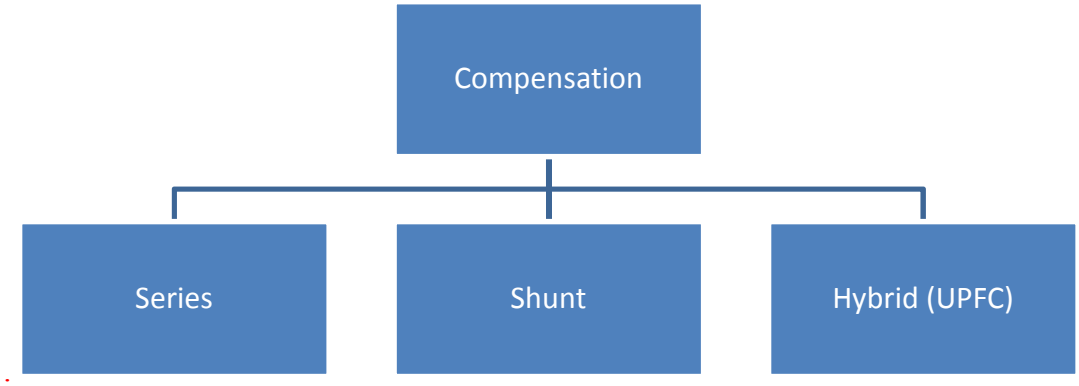


Fig.2.1: Different type of compensation

Shunt compensation can be accomplished by using Static Synchronous Compensator (STATCOM) or Static VAR Compensator (SVC) to regulate voltages in the connected buses of an electrical network. They can supply all or part of required reactive power locally and avoid occupying line capacity to deliver reactive power [6]. Shunt compensators act as current source and inject a current in parallel with the line.

However, series compensation is mainly used to alter reactance of line. This can be performed by inserting a capacitive reactance through the power line. Series compensation helps to release ATC and enhance power flow in the network. This compensator is of voltage source type and it injects a series voltage through the line.

In addition, series and shunt compensation simultaneously can be achieved by hybrid compensation. Unified Power Flow Controller (UPFC) is a hybrid compensator which can control active and reactive power flow through the power lines independently [7, 8]. This device is comprised of a shunt compensator and series compensator. UPFC regulates bus voltage and compensates line reactance by injecting current in parallel and voltage in series respectively [9, 10].

2.2 Shunt Compensation

Shunt compensation is usually used to regulate voltages in an electrical network. Shunt compensators generate leading current to compensate the lagging current of the load, i.e. they inject reactive power into the system and thus regulate the local voltage at the point of injection. Shunt compensator can also be inductive and in this case it can be used to reduce voltage levels if these are increased beyond the operating limits of a circuit. Shunt compensation is traditionally provided using fixed capacitors, reactors or rotating synchronous condensers. Compensation can also be provided using static switches and power electronics based devices such as STATCOM and SVC allowing a very fast response to system transients. Such devices have the capability of injecting both inductive and capacitive reactive power on demand [6].

2.2.1 Synchronous Voltage Source

Rotating synchronous condensers (over excited synchronous generators running on no load) have been used as a shunt compensator in transmission and distribution networks for many years. Although the synchronous machine has an inductive nature and cannot therefore contribute toward any sub-synchronous resonance oscillations [11], [12], the scheme still has some disadvantages. For example, it has a slow response which disqualifies it from being used for system dynamic control enhancement. Furthermore, it has low short circuit impedance and high maintenance costs [13].

A SVS shunt compensation device using static switches is discussed in [13].This has some advantages in comparison with the rotating synchronous condenser. For example,

it does not have inertia and its output can be controlled dynamically. Fig.2.2 shows a parallel connection of SVS into a power line.

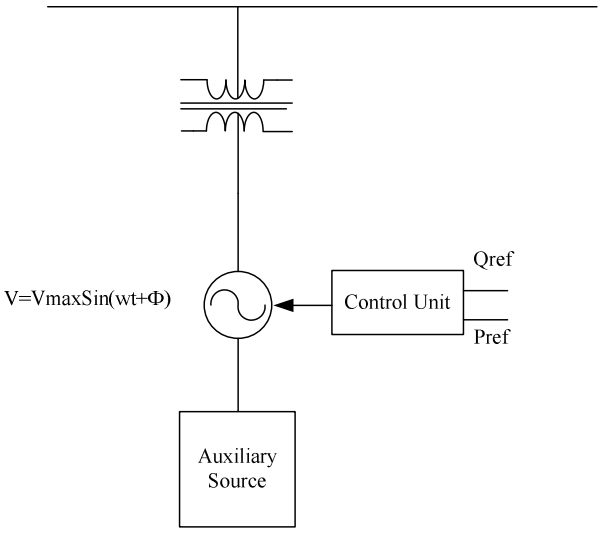


Fig.2.2: SVS shunt compensation

Converters with different power topologies can be employed as a SVS. In [13], a six pulse voltage source converter (VSC) is utilized as a static synchronous voltage Source. The converter, shown in Fig.2.3, comprises three legs connected in parallel with a DC capacitor, each leg consisting of two sets of GTOs with an anti-parallel diode. When the GTO in each leg is triggered, the voltage across the capacitor will appear at the corresponding ac output. With sequential switching of the GTOs, the converter output will be a three-phase ac voltage as shown in Fig.2.4.

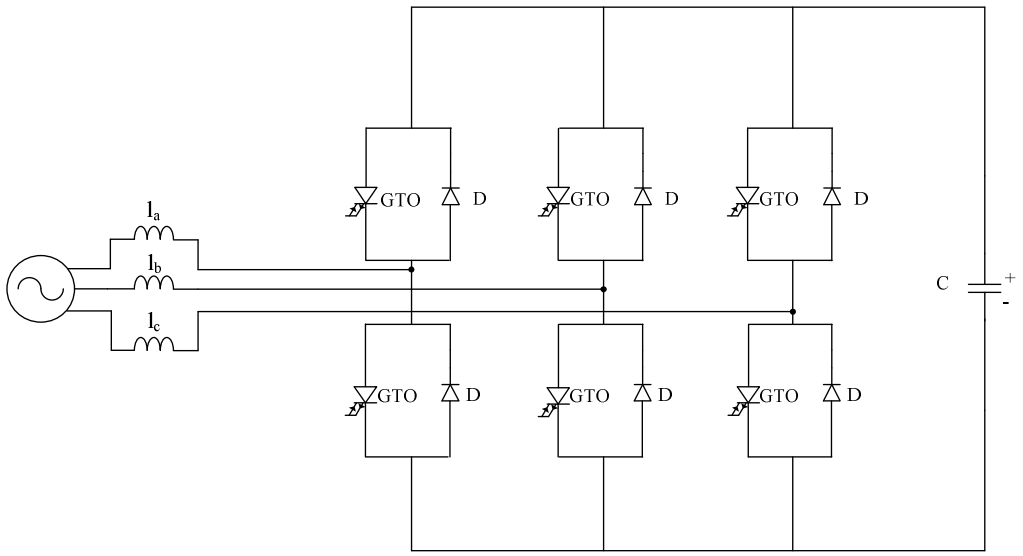


Fig.2.3: Voltage Source Converter

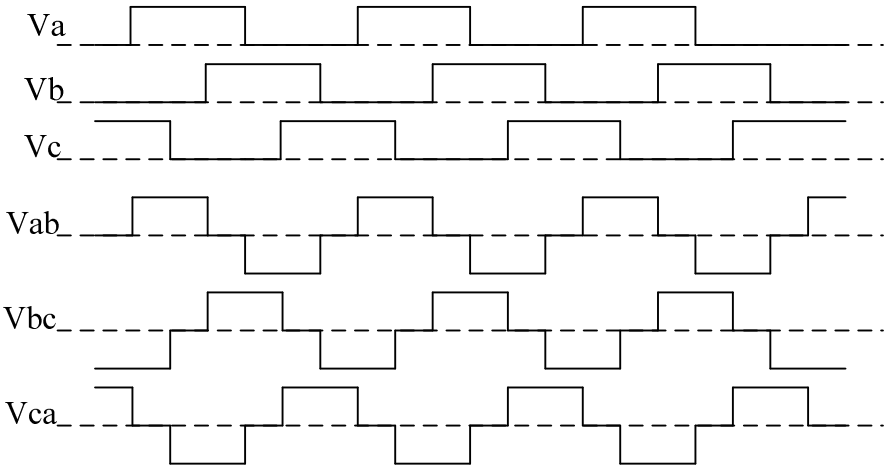


Fig.2.4: Output voltage

The VSC converter shown in Fig.2.3 has the ability to exchange both active and reactive powers with the supply (if an auxiliary power supply is provided on the dc side). Power can flow in both directions across the converter (from the DC link into the AC system and vice versa) governed by the amplitude and phase angle of the converter output voltage. If the amplitude of the AC output voltage is higher than the voltage of the AC system, then the converter generates reactive power and behaves like a capacitor. However, if the amplitude of the ac output voltage is lower than the voltage of the AC system, the converter consumes reactive power and appears as an inductive load. Active power exchange can be achieved by controlling the phase angle of the ac output voltage (in the presence of an auxiliary dc power source). The converter can absorb active power from the AC system if the output voltage of the converter lags the AC system voltage and can inject active power into the AC system if the output voltage leads the AC system voltage [14].

2.3 Series compensation

Applications incorporating series compensators within power lines are increasing nowadays, where they are becoming more important multi-purpose devices in power systems. The application of series compensation in transmission lines to increase the ATC by changing the line reactance has been proposed and implemented in high voltage transmission networks across the world [15, 16]. This provides a cost effective and fast solution which can have environmental benefits by reducing the need for the construction of new power lines. Additionally, series compensation can improve both power system stability and voltage stability as are explained in subsection 2.3.1 and 2.3.2.

2.3.1 Improvement of power system stability

Because of the difficulties of building new transmission or distribution lines it is desirable to utilize existing power lines as much as possible. However there are some limitations and requirements which must be met for the proper operation of the system. Power system stability is one of these important issues that must be considered.

Power transfer between two buses in a power system (with ignored line resistance) is described by the equation (2.1)

$$P_{sr} = \frac{V_s V_r \sin\delta}{X_L} \qquad (2.1)$$

where V_s and V_r are the rms bus voltages (Fig.2.5) and δ is the load angle (i.e. the phase angle between the sending end voltage $\mathbf{V}_s$ and receiving end voltage $\mathbf{V}_r$. X_L is the reactance of the line and P_{sr} represents the received power at the destination bus. X_L could be altered by using fixed capacitor type of series compensation. With the insertion of the compensator, X_C is inserted into line and (2.1) can be rewritten as:

$$P_{sr} = \frac{V_s V_r \sin\delta}{X_L - X_C} \qquad (2.2)$$

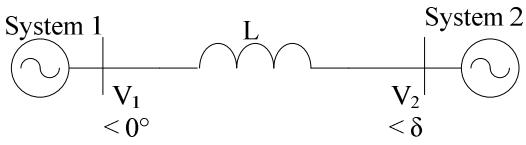


Fig.2.5: Two bus power system

Fig.2.6 shows the amount of transmitted power versus the load angle (δ) for two different line reactances. Compensation of line reactance increases the capability of power transmission through the line. Therefore it can be concluded that if the transmission of a certain amount of power can cause instability in an uncompensated system, the compensated system would be more stable and more likely to be able to handle the extra power transmission.

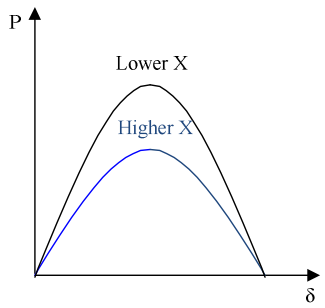


Fig.2.6: Power transmission versus the phase angle with different amount of compensation

2.3.2 Improvement of voltage stability

The stability of system voltage in a power system can be affected by the amount of transmitted power. The improvement in system voltage stability as a result of reactance variation has been well argued in [8, 17].

It has been shown that series compensation can even enhance the transient stability of the system [17]. Fig.2.7 shows the power-voltage characteristics of the line with and without compensation. This figure shows how the demanded active power (horizontal axis of the power-voltage characteristics) can be delivered to the load with a lower voltage drop at the receiving end bus in the compensated system.

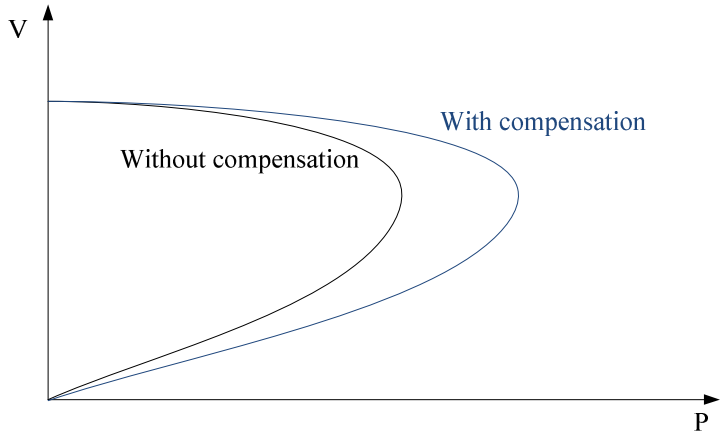


Fig.2.7: Line power-voltage characteristics

2.4 Fixed Series Capacitor Compensation (Series compensation)

Series compensators can be categorised into fixed series capacitor and power electronics based devices. In the fixed series capacitor simply a capacitor has been inserted in series through the line and alters the line reactance as shown in Fig.2.8.

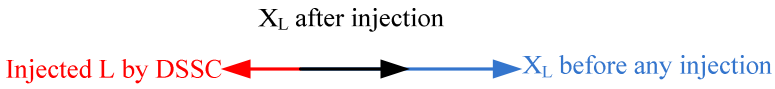


Fig.2.8: Compensation of line reactance

As a result of compensation, more transmission capacity will be available and more active power can potentially be delivered to the load. Without line compensation, a new line may be required to transmit the increased power demand. In a case study carried out

by ABB [18], two systems were considered for transmitting 2000 MW, as shown in Fig.2.9.

System A with two parallel 500 kV lines, each compensated by 40% and system B, with three parallel 500 kV lines without compensation.

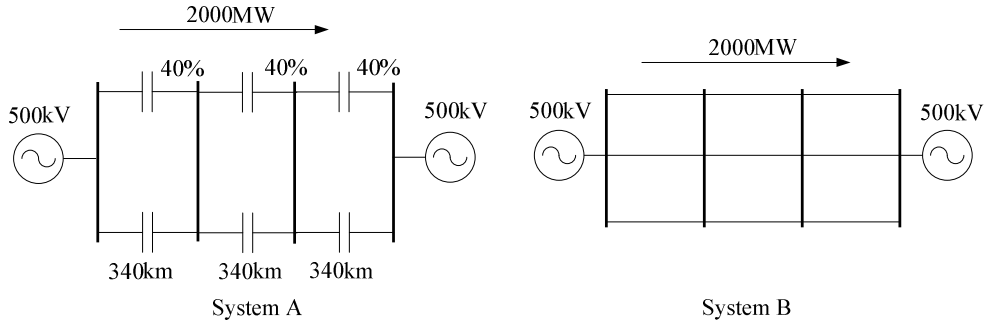


Fig.2.9: Two possible solutions for transmitting 2000 MW

The total implementation cost of system A was found to be 35% less than system B. System A also enjoyed other environmental benefits in terms of generating fewer "right of way" issues than system B.

Although high percentage compensation of transmission lines seems to be economically efficient, the compensation level must not approach 100%. If this were to be the case, fault levels would be very high and line current and power flow would be highly vulnerable to any network voltage changes. Furthermore, it would make the protection system more complicated. In practice, the maximum recommended level of compensation is about 80% [19].

2.4.1 Power topologies of fixed series compensator

Series capacitors must be combined with other equipment in order to make them controllable while they are being used to compensate the power system [20, 21]. Another issue is the high voltages across the capacitors in case of a short circuit fault. For economic reasons, capacitors cannot be designed to withstand such high voltages and they must be protected against such conditions. Two topologies (Figs.2.10) have been employed in the past to achieve this [19], [21].

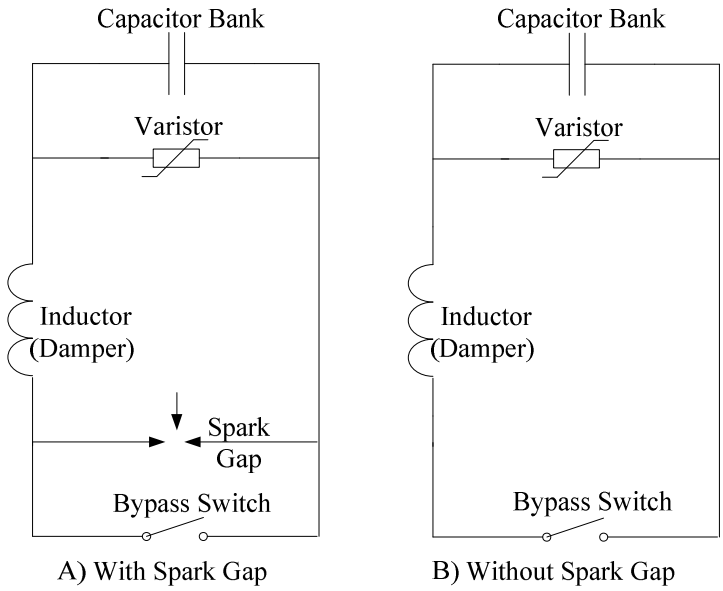


Fig.2.10: Power topologies for series capacitor connection

The circuits consist of the following components:

- Capacitor bank: this is the main component of the series compensator circuit and is constructed using parallel and series connection of capacitors to meet the required MVAr, voltage and current ratings.
- Damping circuit: made of a reactor (mainly air cored) to restrict the current which can be generated by the bypass switch or spark gap.
- Metal Oxide Varistor (MOV): protects the series capacitors from any possible over voltages before the bypass switch operates.
- Bypass switch: to bypass the capacitors (can be of SF6 type).
- Spark gap: to bypass the capacitor bank in case the energy absorption capability of the varistor is exceeded.

The short circuit level (SCL) of the compensated system will increase as a result of the line reactance reduction. High SCLs will lead to high fault currents and this will put a high voltage stress across the series capacitors. For this reason some protection is needed for the capacitors. The Spark Gap bypasses the capacitor when an over voltage appears across the capacitor. The stored energy in the capacitor will then be absorbed by the damping reactor. By closing the bypass switch, the Spark Gap will be bypassed and the current will pass through the switch. Finally, when the current drops back to its' normal value the capacitor is reinstated and compensation is resumed. The minimum and maximum reinsertion times for the topology shown in Fig.2.10 (A) are 200ms and

400ms, respectively [19]. In Fig.2.10, the MOV has a nonlinear characteristic with a high resistance for the voltages below the protective level and a lower resistance for voltages above this level. For this reason, immediately after overvoltage across the capacitor the varistor quickly initiates conduction and bypasses the capacitor. After current returns to its normal value, varistor conduction will cease and this will reinsert the capacitor into the line [19]. The Spark Gap comes into operation to bypasses the varistor and capacitors current diverted in case the energy absorption capability of the varistor is exceeded.

2.4.2 Point of connection of fixed series capacitors

The point of connection for series capacitors is important in terms of cost, reliability, short circuit level and accessibility. In practice, the midpoint of the line as well as the sending and receiving end points are recommended for the installation of series capacitors. It would be cheaper to install all the compensation at the sending end or at the receiving end of the line but this would complicate the requirements of some protection systems such as distance protection schemes. To avoid any complications with the protection system, it is more convenient to install the capacitor bank in the middle of the line [19] despite the extra cost involved.

2.5 Thyristor Switched Series Capacitors (TSSC)

A thyristor switched series capacitor (TSSC) compensator [22] is comprised of a capacitor in parallel with two anti-parallel connected thyristors as shown in Fig.2.11.

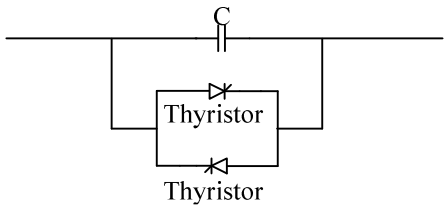


Fig.2.11: Power topology of TSSC

To insert the capacitor into the power system the thyristors should be turned off. This can occur only if the current passing through the thyristor becomes smaller than required minimum turn off current. To avoid any possible surge currents, a thyristor can be turned on when the voltage across its' terminals is zero (soft switching). In this case, the thyristor may be switched on at the voltage zero crossing points and turned off at the current zero crossing points. In order to have enough compensation in the system, there might be a number of series connected TSSC units, as shown in Fig.2.12.

The implementation and operation of TSSC in a power system can obviously affect the power-angle characteristics of the line (Fig.2.13). The transmission capability increases with capacitive compensation, as shown in Fig. 2.13, and vice versa.

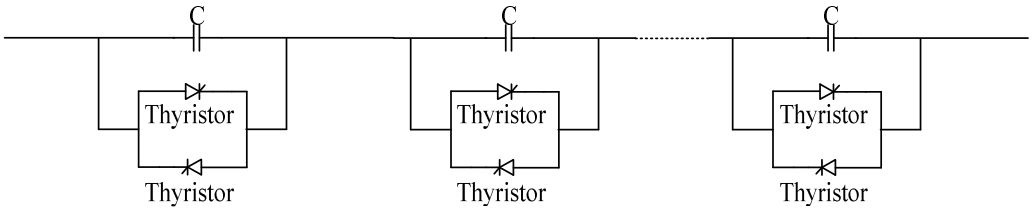


Fig.2.12: Number of TSSC units which are connected in series

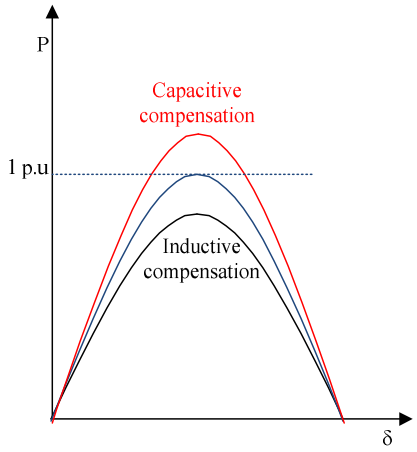


Fig.2.13: The effects of TSSC on power versus angle

2.6 Thyristor Controlled Series Compensation (TCSC)

A thyristor controlled series compensator comprises a capacitor in parallel with a thyristor controlled reactor (as explained and presented in [10], [23]), as shown in Fig.2.14. In order to avoid over voltages across the module, it always comes with a metal oxide surge arrester as shown in figure 1 in [24].The total required compensation might be achieved by the series connection of number of TCSC modules as shown in Fig.2.15 [11], [24], [25].

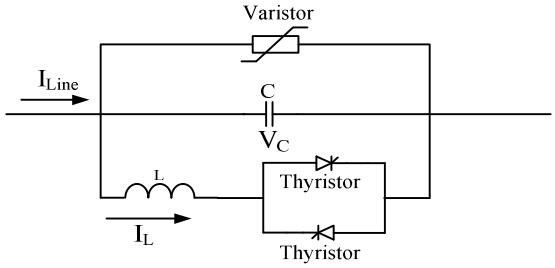


Fig.2.14: Power topology of TCSC

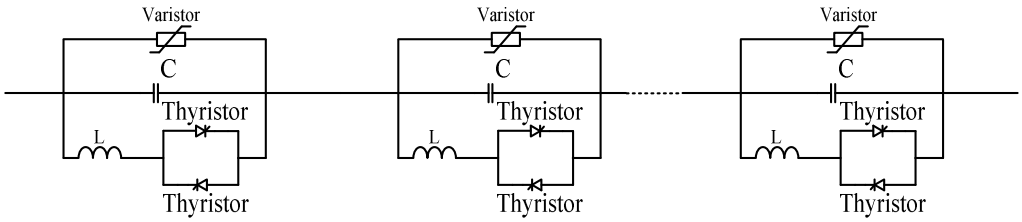


Fig.2.15: Series connection of TCSC

The operation of a TCSC can be divided into 4 distinct modes based on the circuit Boost Factor [22], K, defined as:

$$K = \frac{X_{TCSC}}{X_C} \tag{2.3}$$

Where X_C is the reactance of the device capacitor and X_{TCSC} is given by:

$$X_{TCSC} = \mathrm{Img}\left\{\frac{V_C}{I_L}\right\} \tag{2.4}$$

Another important parameter of a TCSC circuit is given by λ defined as [22]:

$$\lambda = \sqrt{\frac{-X_C}{X_L}} \tag{2.5}$$

The four operation modes [26], [27] are explained in the following sub-sections.

2.6.1 Bypass mode

In this mode, the thyristor is in conduction and the capacitor is connected in parallel with the reactor. The effective reactance of each module is then given by:

$$X_{TCSC} = \frac{X_C * X_L}{X_C + X_L} \tag{2.6}$$

In a practical circuit operating at 50Hz, the resultant reactance of the parallel LC connection is inductive. For this reason this mode is mainly used to limit the fault current and reduce the voltage across the capacitor in the case of a line short circuit fault [22].

2.6.2 Blocked mode

In this case the thyristors are off and the reactor is disconnected from the rest of the circuit. The reactance of the TCSC device is then equal to X_C and the Boost Factor is unity. In this mode, the capacitor carries the full line current and the current in the reactor is zero [28]. Capacitor is fully inserted in series with the power line and TCSC acts as a fixed series capacitor [29], [30].

2.6.3 Capacitive boost mode

If the thyristors are fired just before the capacitor voltage zero crossing point, current will begin to flow through the reactor, thyristors and capacitor as shown in Fig.2.16. This charges the capacitor to a high value of voltage (because the current which pass through the reactor is added on top of the line current). The generated voltage is capacitive and compensates part of the line inductive reactance. The time interval which the thyristors are ON is defined by the firing advance angle β which in turns affects the amount of compensation provided by the TCSC circuit [22].

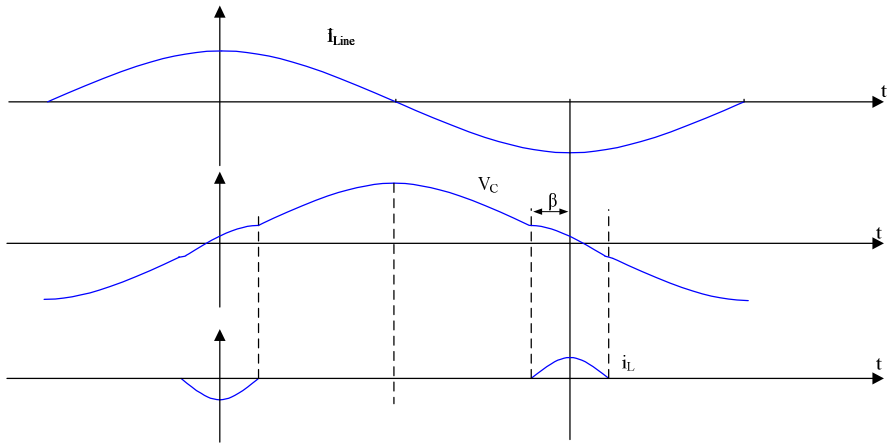


Fig.2.16: Line current, capacitor voltage and reactor current

Current passing through inductance (i_L) has non zero value when Thyristor is conducting. The current is plotted in Fig.2.16 and its non zero value is an indication for conduction of Thyristor.

2.6.4 Inductive boost mode

The operation of a TCSC circuit in inductive boost mode is similar to the capacitive boost mode. However in this mode the angle β is higher than $\frac{\pi}{2\lambda}$ and the current flowing through the thyristors is extremely high. This mode can be used to limit the fault current in the line. However, because of voltage distortion issues across the capacitor and extremely high currents in the thyristors, operation of TCSC in this mode is not recommended.

Fig.2.17, shows the operation of TCSC in both capacitive and inductive with values of the boost factor plotted against the firing advance angle β [22].

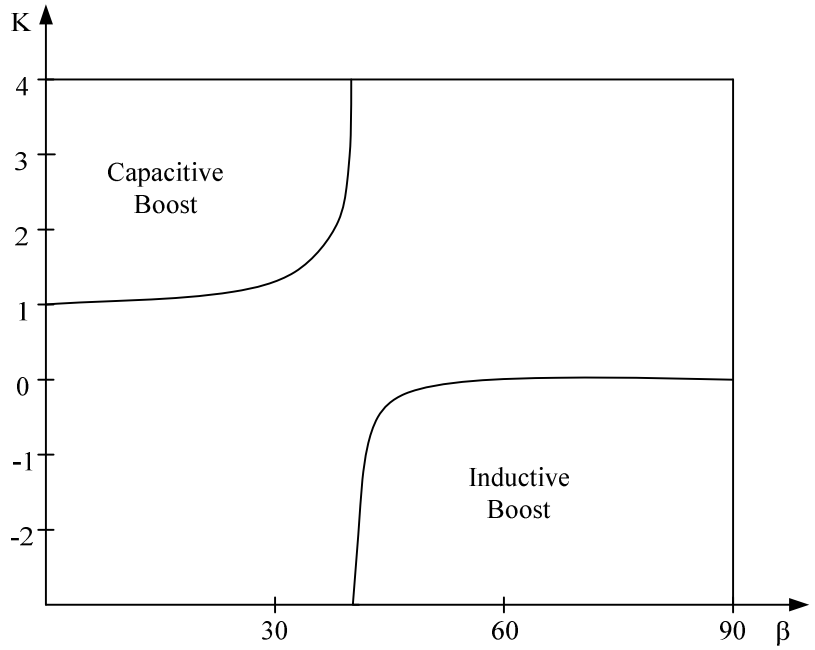


Fig.2.17: Boost factor K versus β; Operation of TCSC in capacitive and inductive boost mode.

2.7 GTO Thyristor-Controlled Series Capacitor (GCSC)

A GTO Thyristor-Controlled Series Capacitor (GCSC) unit is comprised of an anti-parallel GTO pair connected in parallel with a capacitor, as shown in Fig.2.18. The whole device is connected in series with the power line.

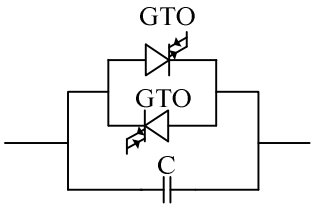


Fig.2.18: GTO Thyristor-Controlled Series Capacitor

In a GCSC circuit there is no need to wait for zero voltage conditions before switching the GTOs which can be fired any point on the voltage wave [31], [32]. This is because GTO is a controlled switch and it can be switched on and off using a control signal. In the configuration shown in Fig.2.19, a fixed capacitor is used in conjunction with the GCSC circuit. In this topology, the main compensation comes from the fixed capacitor with the GCSC providing fine tuning of the required compensation [31].

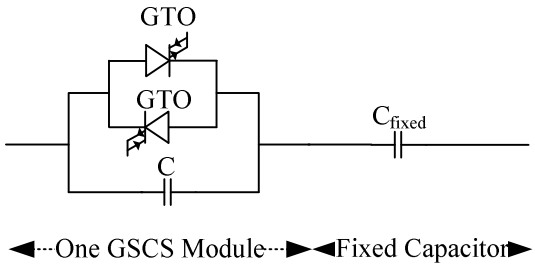


Fig.2.19: GCSC series with a fixed capacitor

Another topology discussed in [31] is shown in Fig.2.20. In this arrangement, a number of GCSC units is connected in series with each contributing a different percentage of its rated power (down to zero contribution in bypass mode).

In this approach, there would be a considerable amount of steady state voltage distortion because of the in/out switching of the capacitors. In order to reduce the amount of voltage distortion, a combination of TSC and GCSC can be used as shown in Fig.2.21. In this configuration, the main part of compensation is achieved by the TSC circuit and the GCSC provides fine tuning [33], [34].

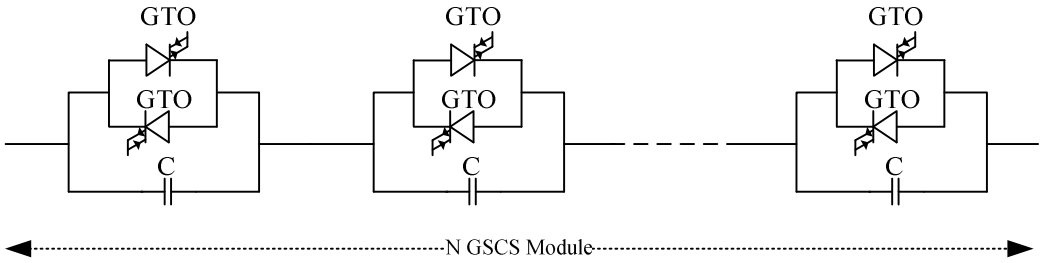


Fig.2.20: Numbers of GCSC connected in series

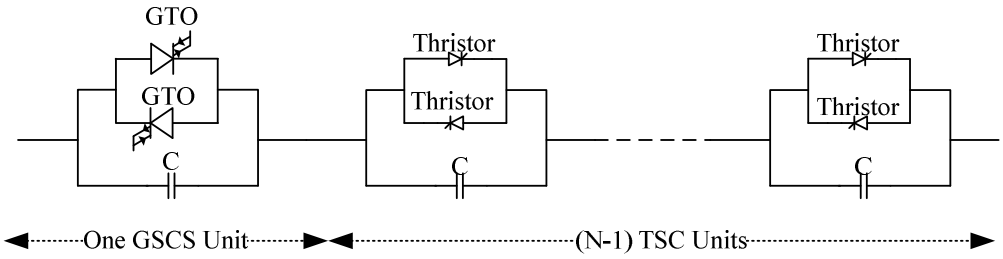


Fig.2.21: Combination of number of TSC and a GCSC

2.8 Application of synchronous voltage source in series compensation

The VSC converter, previously shown in Fig.2.3, is a synchronous voltage source and it can be employed in series compensator [13]. This device does not insert a physical capacitor in the system. Hence, the reactance of the system remains unchanged for all

frequencies other than the power frequency of the network. The device employs fast switching and forced commutated switches within its converter. Feasibility of the application of static switches in series compensation devices in transmission and distribution lines is well described in [34].

The converter is connected in series with the power line (shown in Fig.2.22) via a series transformer and in the DC side it is connected to a DC capacitor. If active power compensation is required capacitor must be supplied with an auxiliary power sources to provide active power. The connection of capacitor to an auxiliary power source is shown with dash line indicating that it is optional and required only if active power compensation is required (to supply the consumed active power by compensation). The required active power can be supplied by another power converter (auxiliary power source) which is feeding active power into the DC link (DC capacitor) [13], [1].

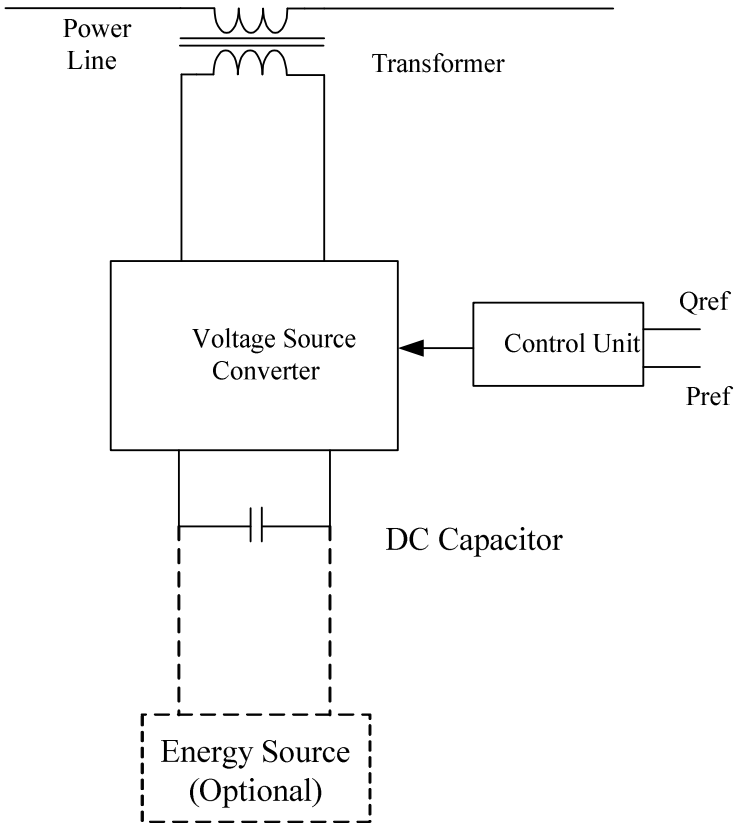


Fig.2.22: VSC connected in series with the power line (series compensation)

The operation of VSC in series compensation applications can be divided into four categories. These modes of operation provide different types of power exchange possibilities for the VSC as shown in Fig.2.23. For example, in order to supply active power and absorb reactive power the VSC module must operate in the 1st quadrant of Fig.2.23. In this figure V_{inj} is the injected series voltage while, V_{injp} and V_{injq} are the in

phase and orthogonal component of injected voltage with respect to the line current. Phase angle between the injected voltage and line is shown by α and exchanged active and reactive power is calculated in equation (2.6).

$$P = V_{inj} I_{Line} \cos \alpha \qquad (2.6)$$

$$Q = V_{inj} I_{Line} \sin \alpha$$

Polarity of P or Q and the corresponding convention are tabulated in Table (2.1).

Parameters	Operation mode	
	Supply	Absorb
P	Positive	Negative
Q	Negative	Positive

Table 2.1: P or Q and the corresponding convention

For supplying both reactive power and the active power the operation of VSC converter falls into quadrant four. In the absence of an external power supply the VSC can operate only in quarters two and three and must absorb a minimum amount of active power (losses) to maintain reactive power compensation.

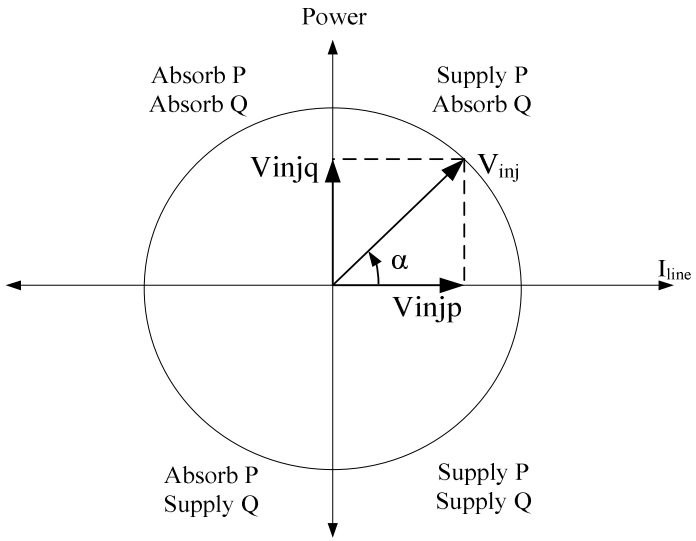


Fig.2.23: The operation of VSC in series compensation applications

The phase angle of the injected voltage with respect to the line current is an important parameter in VSC series compensation. For instance, if the phase angle difference between the injected voltage and the line current is zero, this means that the VSC supplies only active power. However, if the phase angle is 90°, then the VSC injects (or absorbs) reactive power only. When the injected voltage lags the line current by 90°, capacitive compensation is being provided. If we assume that V_{inj}=-$JX_{inj}i_L$ is the injected

voltage and i_L is the line current, then X_{inj} will represent the effective reactance of the injected capacitance.

The phase angle of the injected voltage can vary between 0 and 360 degrees and this determines the functionality of the VSC. For example, VSC connected to a AC system as shown in Fig.2.24 can contribute towards voltage regulation by injecting voltage in-phase or in anti-phase with respect to the bus voltage [13].

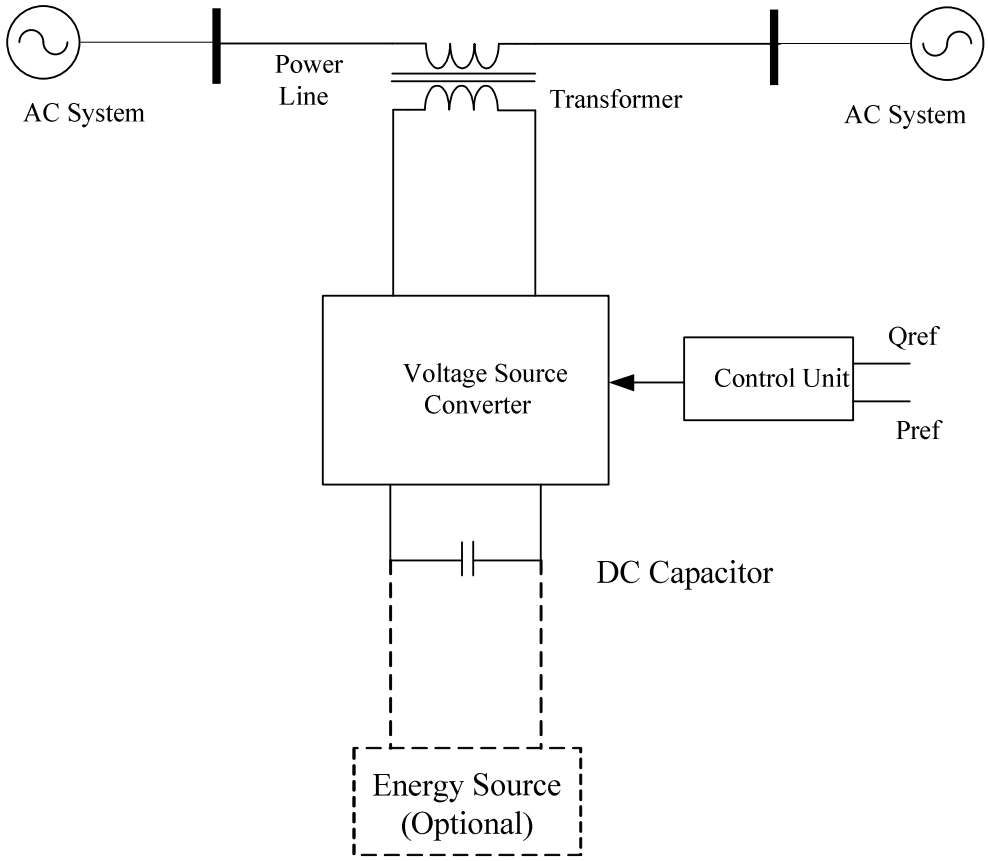


Fig.2.24: Regulating bus voltage by VSC based compensator

The phasor diagrams explaining the injections are shown in Fig.2.25. The compensator regulates the bus voltage (V_r as shown in Fig.2.25 and Fig.2.26) and bus voltage before and after compensation is shown in this figure.

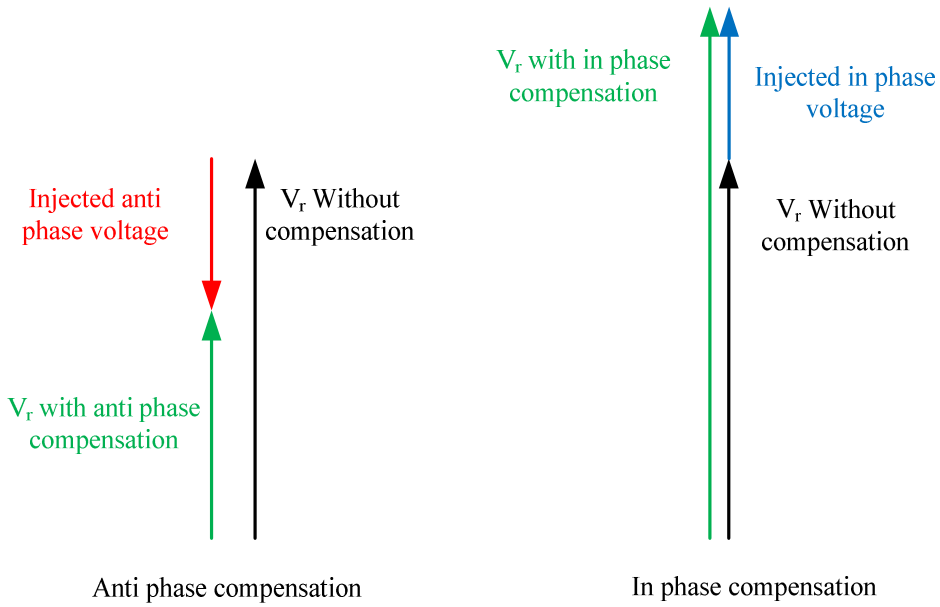


Fig.2.25: In-Phase and anti-phase (with respect to the bus voltage)voltage injection

Circuit representation of the corresponding injection is shown in Fig. 2.26.

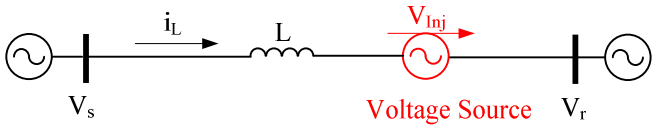


Fig.2.26: Circuit representation of the injection

where V_s and V_r are the sending end and receiving end bus voltages. Injected voltage is shown by V_{inj}. In this figure the injected voltage is represented by a series voltage source moreover its angle and amplitude is being controlled by the controller. For example, if compensation of line reactive along with the regulation of the bus voltage is required, then there must be an injected voltage which can be decomposed into two components as shown in Fig.2.27. Bus voltage regulating component is in phase with the bus voltage and line reactive compensator component is in quadrature with line current [13], [1]. It must be noted that voltage source only injects V_{inj} which includes V_1 and V_2 and these voltages are not being injected separately. The compensated bus voltage is shown with V_r before and after compensation in Fig.2.27.

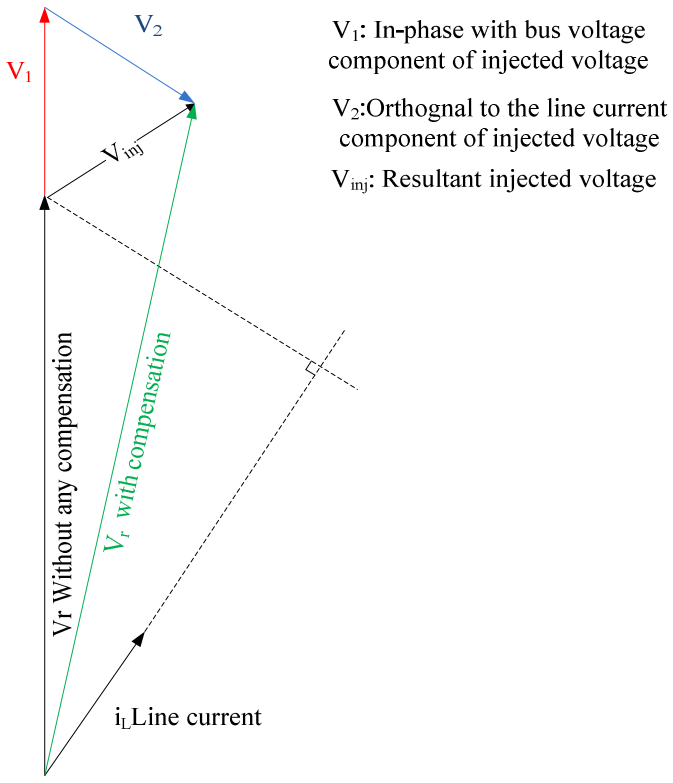


Fig.2.27: Compensating line voltage drops

The VSC can regulate the load angle in a transmission or distribution line, and at the same time regulate bus voltage. To do so (Fig.2.28), the device injects an in-phase voltage (in phase with the bus voltage) responsible for voltage drop compensation and another voltage component which is trying to alter the phase angle in such a way that the resultant rms voltage remains unchanged but with a phase angle shifted of α degrees [13], [1]. The resultant injected voltage is V_{inj} which is being injected in series through the line as represented with a voltage source in Fig. 2.26. The compensated bus voltage (V_r) is shown in Fig.2.28 before and after injection.

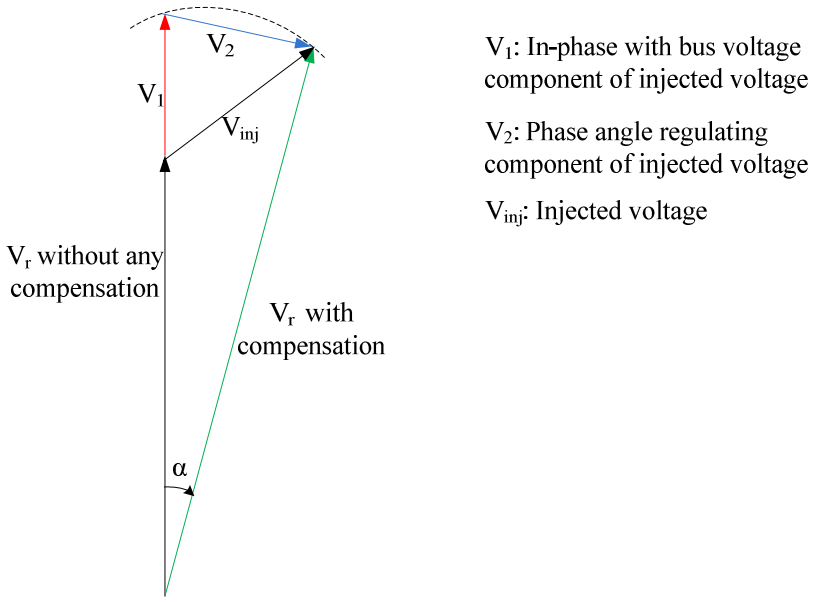


Fig.2.28: Compensation of voltage drop and regulating the phase angle

Finally, the VSC can be employed to regulate bus voltage and the transmission load angle while it is compensating line reactance. In order to meet all these requirements, an injected resultant voltage combining three different elements is needed, as shown in Fig.2.29. In this figure V_1 represents the in-phase with bus voltage component whileV_2 and V_3 show the line reactance compensating and phase angle regulation components of the injected voltage, respectively[13], [1]. However at the end only V_{inj} (which is the resultant voltage) is being injected as shown in Fig.2.26. The regulated bus voltage (V_r) is shown in Fig.2.29 before and after compensation.

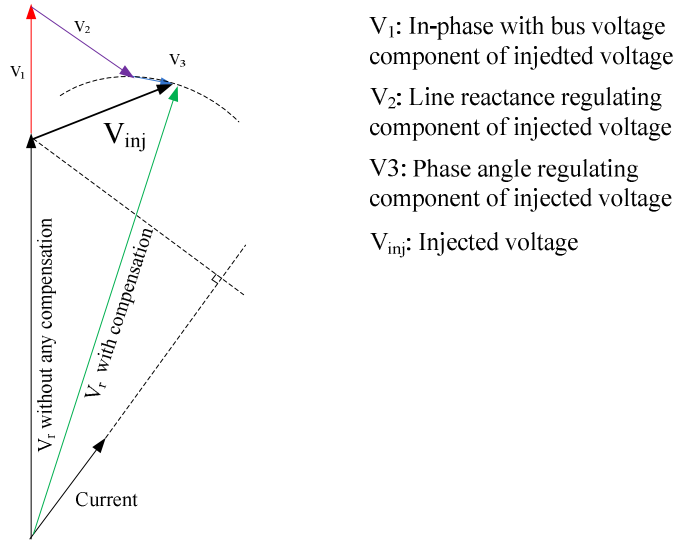


Fig.2.29: Regulating bus voltage, line reactance and load angle regulation

2.9 Static Synchronous Series Compensator (SSSC)

SSSC is a series compensator device and it is connected in series with the power line via a transformer. It employs VSC converter to inject series voltage in quadrature with the line and alters the effective line reactance by injecting a voltage. Its principle of operation is similar to those explained in pervious section. However, in SSSC the main purpose is to compensate the line reactance which can be achieved by injecting a fully controlled voltage in quadrant with the line current [14], [35]. In three phase systems, SSSC is comprised of a three phase power converter connected in series with the power lines through a series transformer. SSSC is mainly used to provide VAr compensation and its typical block diagram is shown in Fig.2.30. SSSC needs to absorb active power in the start up period to charge up its DC capacitor it needs to absorb active power to compensate the ohmic losses within the SSSC device.

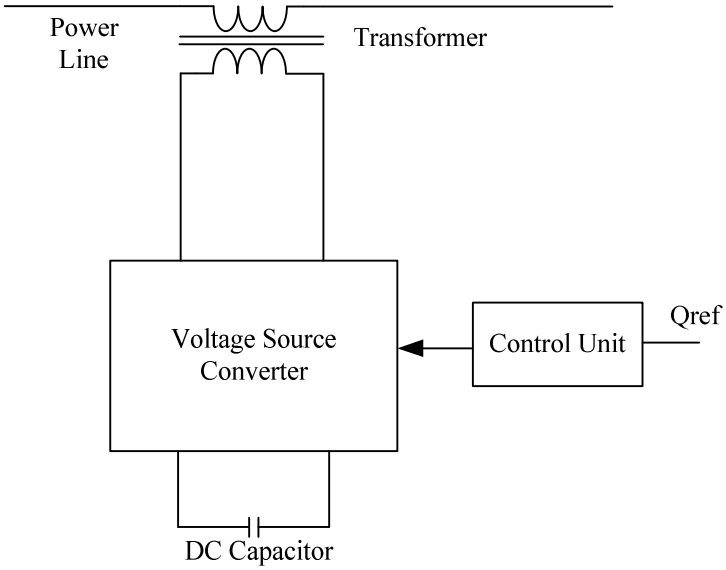


Fig.2.30: SSSC block diagram

Line reactance in transmission and distribution lines can restrict the available transmission capacity. Since there is no physical connection of a capacitor in series with the line, SSSC can be used to compensate a percentage of the reactance of the line without the initiation of Sub-Synchronous Resonance (SSR) in the network [36]. SSSC can also increase the line reactance partially diverting the current in an existing line into another parallel line.

However, application of SSSC is not restricted to the power flow control in electrical networks; it can also be used for reactance compensation. For example, in [37] SSSC is

applied in a wind farm to compensate the line reactance in order to release more transmission capacity. The different modes of operation of static synchronous compensation were explained earlier in section 2.8. In all of schemes, compensation is achieved by injecting a series voltage through the power line. The injected voltage by SSSC device is shown as a voltage source in Fig.2.31.

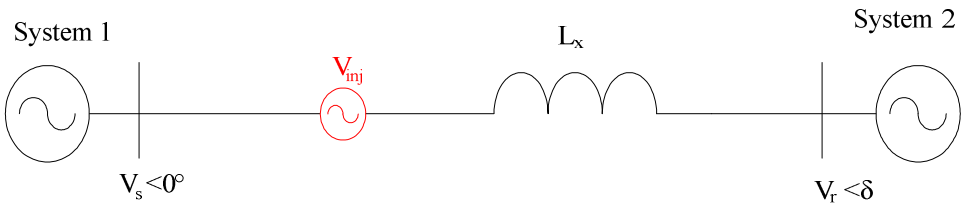


Fig.2.31: A two bus power system with compensated line

δ presents the phase angle between the two voltages V_s and V_r in the compensated line and the value of δ depends on the percentage of compensation. Fig.2.32 shows a phasor diagram of the sending end and receiving end voltages and the injected voltage.

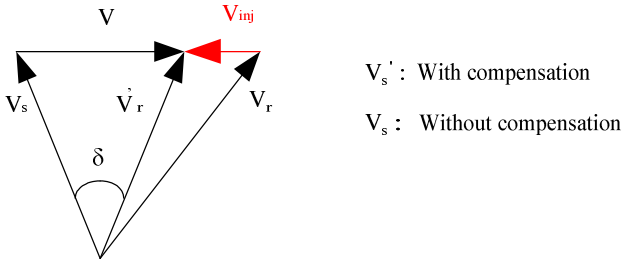


Fig.2.32: Phasor diagram of the sending end and receiving end voltages and the injected voltage

Injected voltage is negative for capacitive compensation and positive for the inductive compensation. Inductive compensation is important when SSSC is used for power flow control purposes. The positive reactance is generated by injecting a voltage which is leading the line current by 90° while the negative reactance can be inserted by generating a voltage which lags the line current by 90°. The SSSC injected voltage is usually modelled as a voltage source with a variable amplitude and phase angle based on system requirements [38], [39].

2.10 Comparison between power electronics based series compensators and series fixed capacitors

The implementation of series capacitors is a superb solution to increase the transmission capacity of an existing line as it is a low cost and time saving approach. This solution removes the need to build another line, with all the associated cost, right of way and environmental concerns. However there are some technical issues with application of fixed capacitors in the power lines. Some of these issues can be addressed by using power electronics based compensators.

For example the voltage across the series capacitors depends on the line current in fixed capacitor solutions and any changes in the line current can alter the compensation. Also the compensation provided by series capacitors is restricted to the reactive power and they cannot contribute toward the active power compensations. However, these can be tackled using VSC based devices which they inject a series voltage irrespective of line current and if it is connected to another external power source it can provide active power compensation as well.

Sub-synchronous Resonance (SSR) is a major concern associated with the employment of fixed series capacitors in transmission lines, restricting the application of series capacitor compensation in electrical networks [40], [41].Since the probability of the initiation of SSR as result of series compensations has been identified, many research studies have been conducted to try to overcome such barriers [12], [42]. To address this issue in [42] Hingorani introduced a thyristor controlled capacitor (Fig.2.33) and argued that this can be used for a variety of purposes including damping of SSR. By replacing the resistor in the scheme with an inductor, a TCSC circuit is introduced.

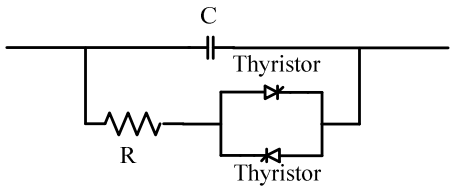


Fig.2.33: Scheme introduced by Hingorani

Some researchers [43], [44] have argued that SSR in electrical networks can be mitigated by employing TCSC [45]. However, the circuit needs to stand very large voltages across the capacitor and high currents through the thyristors during fault conditions. This increases the rating of components and means that a complicated control system is needed to protect the devices.

In order to achieve a higher percentage of compensation a combination of Fixed Capacitors and TCSC can be employed [46]. In this approach, the main compensation is provided by the fixed capacitors and the TCSC device only contributes a small part of compensation. For example, in [46], in order to achieve 0.7 pu compensation, the TCSC circuit provides just 1/3 of the required compensation and the rest comes from the fixed capacitors.

TCSC has been broadly employed as a series compensator in electrical networks [47] and provides a low cost solution for high percentage compensations. It can alter the effective reactance of the lines within the network and can be used to enhance the transient stability of system [48], [49]. However there are some concerns related to the use of TCSC. Firstly, it injects some harmonics into the system [50], [51], [52] and lowers the power quality. In [50] a harmonic analysis of the TCSC circuit was presented and a control strategy using a PWM controller was proposed in order to mitigate the level of injected harmonics (mainly a combination of the 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics) [50, 51]. Secondly, as thyristors can turn off only at the current zero crossing points, their turn off time can extend up to half a cycle. This affects the response time of the TCSC circuit and requires a complicated control system [53].

SSSC using a VSC can be another solution to replaces TCSC [48], [49], [54]. In SSSC, the capacitor is not connected directly to the power system. For this reason the short circuit current does not pass through the capacitor which therefore does not see an excessive voltage across its terminals. In SSSC compensation is achieved by the injection of voltage and no physical capacitor is involved [1], [55]. SSSC provides compensation at system frequency which is immune against oscillations at other frequencies. For this reason compensation cannot contribute toward the SSR phenomenon which occurs at lower frequencies in the electrical network [38].

2.11 Distributed Static Synchronous Compensation (DSSC)

There has been continuous improvement in series compensation devices in recent years in terms of enhancement of their functionality and practicality. However, more improvements are needed and there are still many issues and problems associated with their use which need a solution.

For example, the complexity of SSSC circuit design can be increased as equipments within the device need to cope with short circuit currents in the fault events. To do so, the equipments can be rated high but this can increase costs. In addition, as the devices are connected in series with the line, any failure of a device will disconnect the line.

Maintenance costs are high because repairs are carried out on site and consequently the mean time to repair (MTTR) will be high increasing the cost of operation such a system. Furthermore, each transmission line will have its own requirements and specifications for SSSC and consequently this device must be designed and build specifically for each line, making it more expensive and increasing lead times significantly [56].

In order to overcome some of these problems the new concept of DSSC, was introduced in 2005 [58]-[62]. Generally, DSSC has the same functionality as SSSC however DSSC has distributed nature in low power ratings. With using DSSC, the required compensation is provided by employing a large number of low power DSSC devices. These devices can be mass produced, decreasing design and production times and making it more economical solution.

DSSC uses VSC to inject voltage through the line. The injected voltage is orthogonal to the line current and depends on the injection angle it generates a virtual capacitance or inductance through the line. The possible injection angles are shown in Fig.2.34.

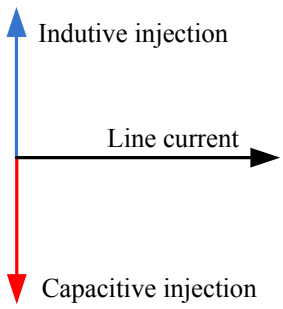
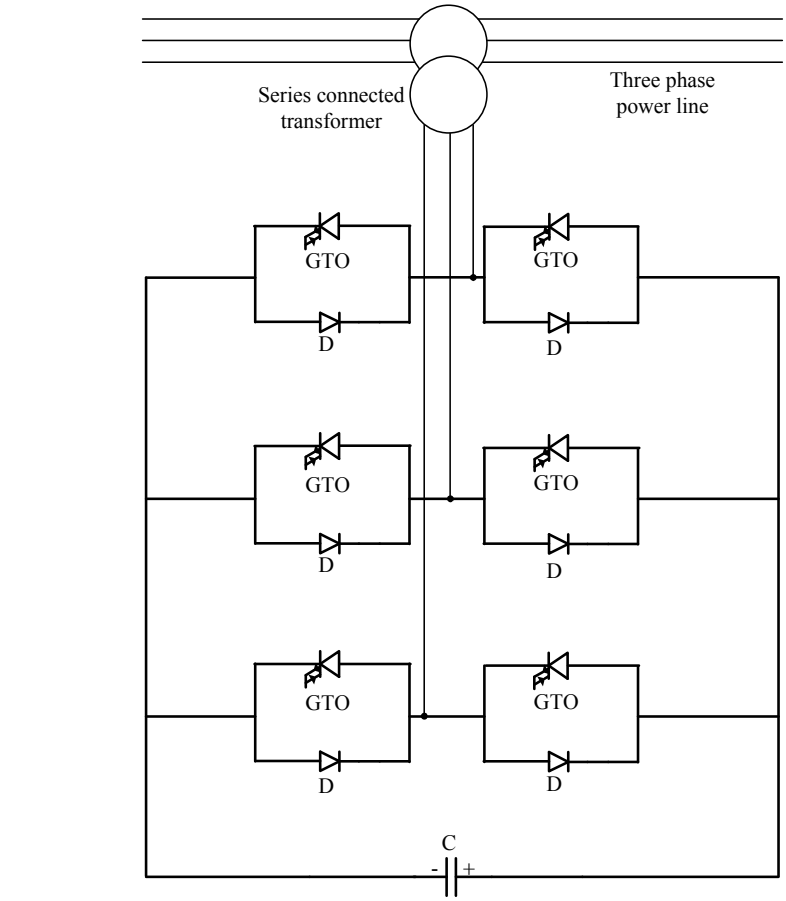
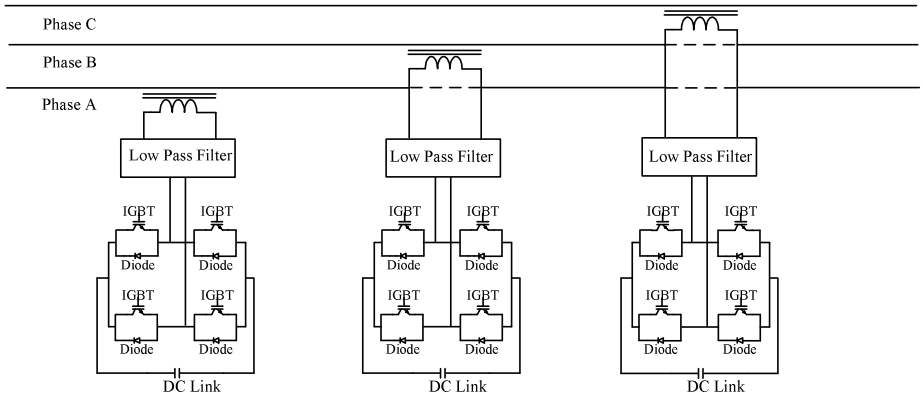


Fig.2.34: The possible injection angles to generate virtual capacitance or inductance

Although, the DSSC and SSSC have almost same concept (and principle of operation) but topologically and practically they are not same. For example DSSC comprises of three single phase VSC converter but SSSC is made of a three phase converter. Furthermore, in DSSC each module has own DC capacitor in each phase but in SSSC the DC capacitor is shared between the three phases. The amplitude of the injected voltage by DSSC is in the range of few volts and it does not need high power switches while the SSSC does. Fig.2.35 a and b show the power topology of the SSSC and DSSC respectively.



a) Power topology of SSSC



b) Three single phase DSSC

Fig.2.35: Power topology of SSSC and DSSC connected to a three phase power system

Each DSSC employs a single phase H-bridge voltage source converter. In this method (Fig.2.37) a single turn transformer (STT) is used to inject a series voltage which is orthogonal to the line current [59]. The STT is suspended from the power line and uses the power line itself as a secondary winding to inject the voltage. For this reason there are no concerns about voltage insulation as the device is fully isolated with no

connection to ground [60]. Another advantage of DSSC is that it provides more reliable operation as the number of modules provide redundancy in case of failure of even a few numbers of devices.

In addition, STT within the DSSC is a two part device which can be easily clamped around the power line then there is no need for the DSSC modules to be repaired on site as they can easily be disassembled and carried to a repair centre. This will reduce the cost of maintenance and increase the reliability and availability of the system. DSSC also has the capability to cope with short circuit currents following a fault in the power system. The short circuit current passes through the power line itself and just a small amount of current(which depends on the turn ratio of the single turn transformer) is induced on the primary side of the STT. This is a challenging problem for SSSC compensators because the fault current passes through the series transformer and this can be extremely dangerous for the transformer [60].

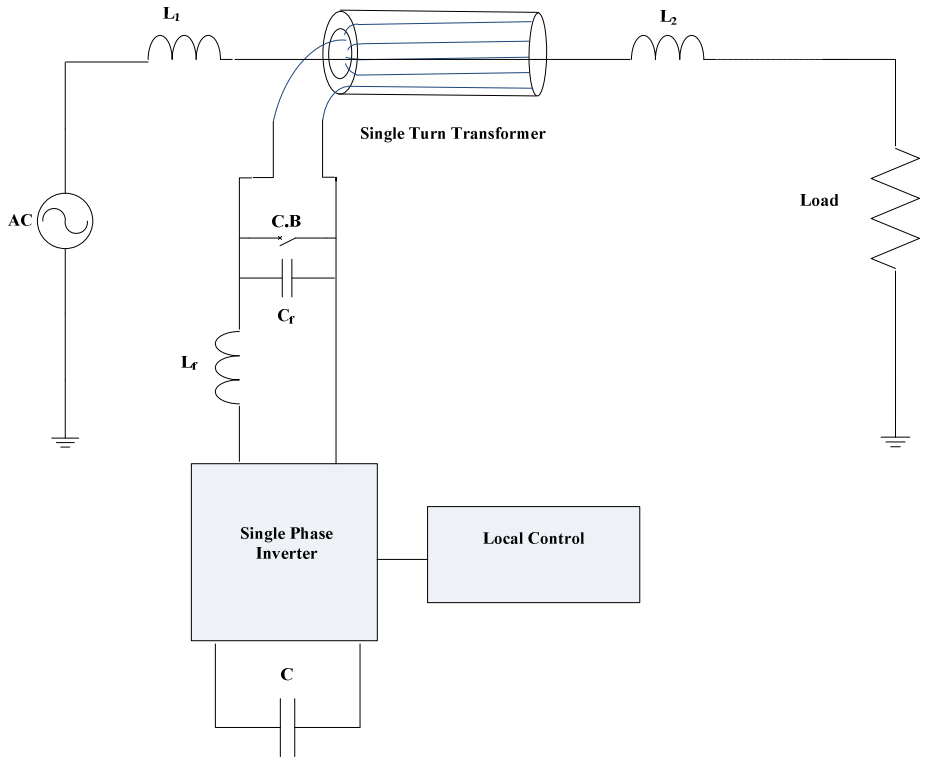


Fig.2.36: Distributed Static Series Compensation (DSSC)

DSSC is also more flexible than SSSC. For example, if more power flow control is deemed necessary, the number of DSSC units can be increased later-on, unlike SSSC, which once it has been designed and built there is no possibility for further functionality. SSSC needs customised design and to be manufactured for specific project however DSSC can be mass produced and later on more modules can be added

through the line. A line reactance profile with DSSC is shown in Fig.2.37. This figure shows that line reactance can be made capacitive or inductive depending on the number of switched-in DSSC units and the characteristics of their compensation. It also shows that the change of reactance is achieved in a stepwise fashion and each step can be positive, for inductive insertion, or negative, for capacitive compensation. Each DSSC device can be switched on in order to insert some reactance through the line. In the following figure in each step one DSSC device is switched on. This process can be continued in order to meet the required compensation.

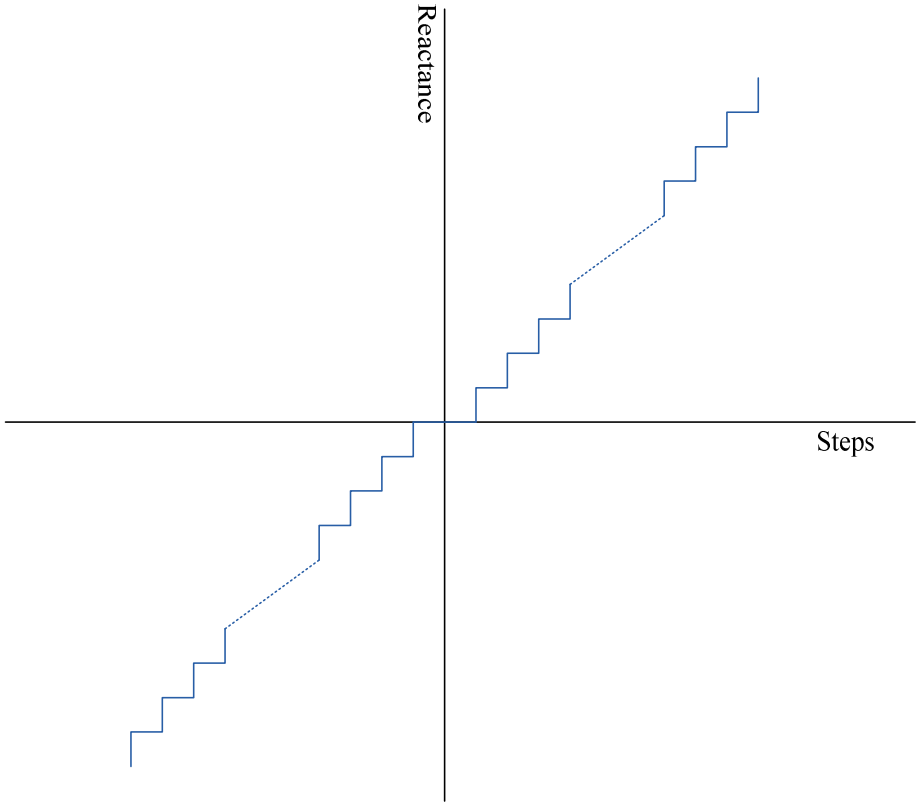


Fig.2.37: Example line reactance profile

DSSC devices also have low weight and it is therefore possible to suspend them from the line. In a three phase power system, each phase has its own independent DSSC module (as shown in Fig.2.38) which operates independently from the each other. Meaning that different levels of compensation can be injected into each phase which is an important consideration in low voltage distribution networks where there are significant levels of load imbalance.

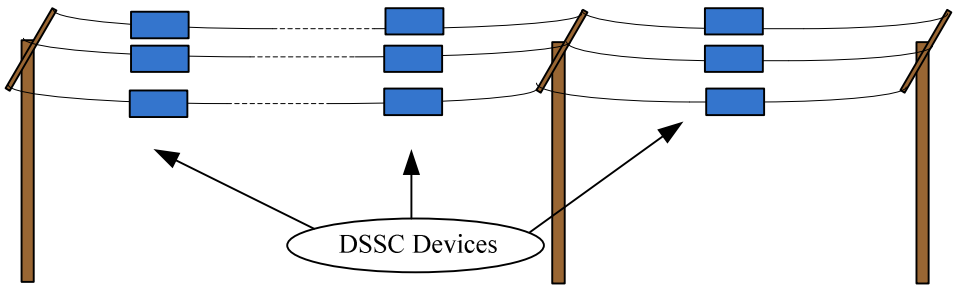


Fig.2.38: A distribution line with suspended DSSC through the line

Each DSSC module comprises a STT which provides an electromagnetic connection to the power system. The STT is connected to an H-bridge converter via a low pass filter located between the output of the converter and the STT (Fig.2.39).

The low pass filter is employed to eliminate the converter generated high switching harmonics. The converter itself includes four Insulated Gate Bipolar Transistors (IGBTs) connected in anti-parallel with four diodes as shown in Fig.2.39. On the DC side, the converter is connected to a DC link capacitor used to hold the DC voltage at the required level. The STT transformer is built of two separate parts which can then be easily clamped around the power line to suspend the whole DSSC module. For this reason a DSSC unit can be easily assembled and dissembled [61]. All the control and communication equipment are built inside the module and are supplied internally from the unit's power supply fed by the current drawn from the STT.

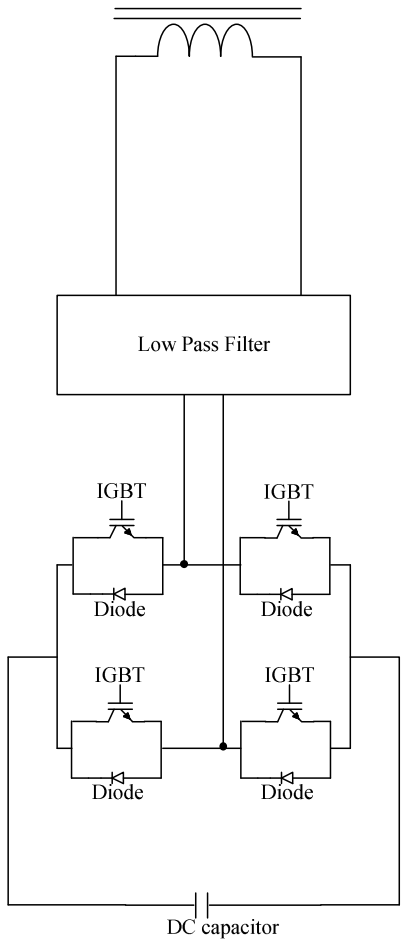


Fig.2.39: Circuit schematic of DSSC

From the power system point of view, the DSSC modules provide a "smart wire" option for transmission lines allowing for a more flexible and effective power flow control. DSSC does not contribute towards the active power compensation because it is not connected to another auxiliary power source. However, it has a huge impact on the reactive power by significantly compensating it through the line. It has also been argued that the deployment of DSSC in an electrical network can reduce the environmental impact of electricity transmission and distribution as it releases some line capacity and ease congestion issues [62]. In comparison with SSSC, DSSC has the benefit of using low rated components as the whole device is working at low power and low voltage. For example, in [63] the DSSC device is rated for only 10 kVA and the injected voltage is less than 10 volts. This reduces the total cost of manufacturing because components like IGBT's and capacitors can be easily and cheaply sourced.

Power flow control using DSSC devices has been attracting some attention during the past few years [64]. A PSCAD/EMTDC model of DSSC is presented in [65] for simulation studies and power flow control investigations. A simple three phase model of

DSSC is proposed in [66] to be employed in Newton-Raphson power flow studies. Other DSSC application such as improvement of voltage stability in power systems has also been proposed [67]. This is achieved by changing the impedance of critical lines in the electricity network.

2.12 Control of DSSC

The amount of compensation that comes from DSSC can be controlled locally or via a centralised control system. In both cases, a special control system is required in order to operate the DSSC device itself. The control system implemented within the device is responsible for the proper operation of the device only and it receives the set point for the required injection from the central controller.

In a DSSC, the compensation is achieved from a controlled voltage source converter (H-bridge converter). However, the converter just tracks the reference signal that comes from the controller. That shows importance of the employed controller. The generated reference signal must be synchronised with the AC power system, having the correct phase angle and amplitude in order to meet the requirements of the compensation. The compensation percentage can be changed by the control system that is provided by the network operator, where it is required that the controller be able to cope with the new parameters. In addition, there may be disturbances or an unbalance within the AC power system, thus the employed controller in the DSSC must be able to overcome such issues.

From the control point of view, the DSSC tackles the issues slightly different than the SSSC. Each phase in the DSSC is independently controlled and therefore, the injected voltage through each phase could be totally different from the other two phases. While in the SSSC, generally, balanced three-phase is injected into the power system. However, the aim is the eventual compensation of the line reactance and control of power flow in the electrical networks. Different approaches have been used in the SSSC applications, however some of them cannot be employed in the DSSC because of either their three-phase nature or they have drawbacks and disadvantages that will be discussed later in this chapter.

DSSC is a new concept however its principle of operation is same as the SSSC device. Employed control strategies in the SSSC have been investigated in order to evaluate the possibility of their employment in the DSSC devices. L.Gyugyi proposed a system using a controlled VSC to provide a series compensation in the transmission lines. In this work, the use of a voltage source converter was proposed to adjust the transmission

angle between the sending and receiving end buses. Further to this, L. Gyugyi explained the principle of series compensation with the applied control strategy, in that it is mainly structured by presenting a 90 degree phase shift between the injected voltage and line current [62, 2].

The phase shift between the line current and injected voltages has been provided by different methods suggested in the literature. Some studies are based on the regulation of the phase angle and amplitude [68], [3]. In this method the angle is derived from the difference of the DC voltage and the target voltage after passing through a controller (holding the DC voltage in a desired value is commonly respected by all of the controllers). The amplitude of the injected voltage is then calculated by using the required percentage of compensation.

Another method, which is widely used in most of the control strategies, is simply shifting the line current signal by 90 degrees [35], [69]-[71]. In the control strategies that are found to be frequently implemented within the literature are using dq conversion in the control system [35], [68]-[71]. The dq conversion system is used to convert the three AC voltages or currents to the dq domain and then apply the control strategy within this domain.

There are two main factors in control of DSSC that must be properly addressed. The first involves finding the right amplitude of the injected voltage, which is significant to the extent that it defines the percentage of compensation, or the amount of injected capacitive or inductive reactance. The second is the phase angle of injected voltage, which must be orthogonal to the line current phasor in order to guarantee the stable injection by the device. Moreover, this angle can be controlled so that the injected voltage is either leading or lagging the line current in order to create inductive or capacitive reactance.

2.12.1 Control strategy based on dq

In order to calculation phase angle and amplitude of the injected voltage different methods have been used in the literature review. For example, in [2] and [3], the amplitude of the injected voltage and its phase angle are calculated separately. The block diagram of control strategy to generate reference signal in [2] is shown in Fig.2.40. In this method, the main part of the control is based on the dq conversion. The I_{abc} is converted to the I_{dq} and synchronous conversion can be done by the use of a phase locked loop (PLL). After providing I_{dq}, the amplitude of the line current is calculated as

$$I_l = \sqrt{I_d^2 + I_q^2} \quad (2.7)$$

where I_d and I_q are the direct and quadrature components of the dq conversion, resulting in the line current I. Having the line current calculated and knowing how much capacitive reactance is required to be injected, the amplitude of the reference voltage is calculated by the multiplication of I and X_{inj}. In the following control block diagram, X_{inj} represents the reactance of injected capacitance, which can also be viewed as the percentage of the compensation.

Reference DC voltage level (shown by V_{dcref}) and measured DC voltage (shown by V_{dcm}) are compared and the error is used controller to provide the phase angle of the injected voltage. The phase angle can be defined by comparing the exchanged AC power with the obtained error. This will regulate the DC voltage in the DC bus of the converter and at the same time, will stabilise the system to the steady state. This part of the controller provides only the required phase shift, where it will be added on top of the *wt* that originates from the PLL.

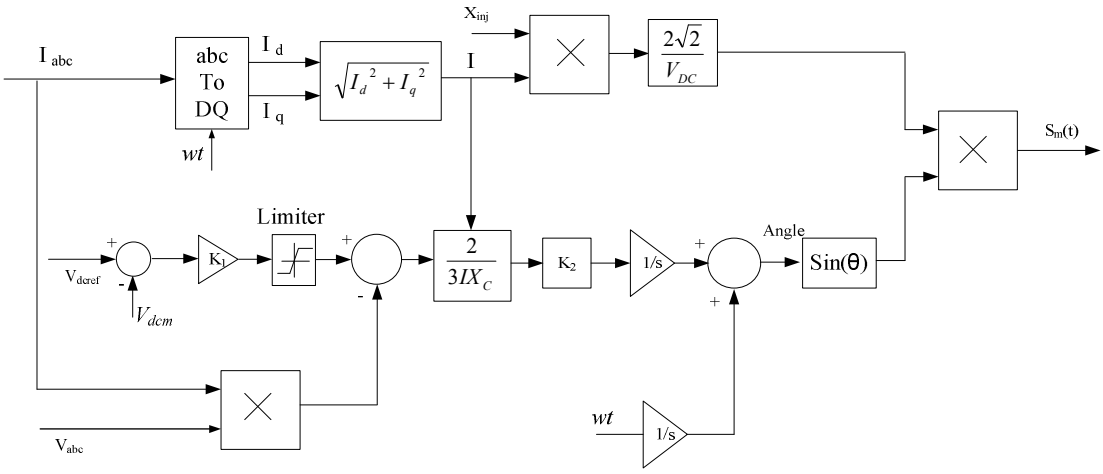


Fig.2.40: Control block diagram for generating the reference signal

In [3], a similar control strategy has been proposed and shown in Fig.2.41. However, this strategy does not monitor the exchanged AC power and its power control is mainly based on the control of the DC voltage on the DC link. To do so, the DC voltage is compared against a reference DC voltage and the error is added on top of the both *w*and *wt*. In this controller, w comes from the PLL then fed into an integrator. The integrator will provide the *wt* and the error of V_{dc} will be added on top of the wt. As a result, the generated signal will include information about the wt of the power system as well as

the error of the DC voltage. It means that the signal is synchron with the system and tries to eliminate the error within the DC voltage.

The phase angle of injected voltage can be altered in order to provide proper angle of injection. This is because when the DC voltage in the capacitor is less than the reference voltage then the error will have non-zero value. Consequently, it will shift the phase angle, making the exchange of active power possible. The problem with this controller is that the 90 degree phase difference between the injected voltage and the line current is not of the utmost importance. The first priority is to keep the DC voltage constant. While keeping the DC voltage at a constant value can bring stability to the system, the orthogonal injection is still not guaranteed. This type of controller is partly the same as the control block diagram as shown in Fig.4.40.

In order to obtain the amplitude of the injected voltage, the dq conversion has been used, thus bringing up some disadvantages. It must be noted that in both controllers that are shown in Fig.2.40 and Fig.2.41, the X_{inj} can be positive and negative. The positive X_{inj} represents the capacitive injection, where the aim of the compensation is to reduce the inductive reactance of the line. The negative X_{inj} represents the inductive reactance, whereby injecting such a reactance into the power system results in the total reactance of the line to increase. The injected voltage in inductive mode has exactly a 180 degree phase difference with the capacitive injection.

Generally, in both of the discussed controllers, the phase angle of the injected voltage controls the power exchange of the series compensator, and the amplitude of the injected voltage determines the percentage of the compensation. These two pieces of information are obtained from a sinusoidal signal and the generated signal can be fed into a PWM generator, providing the switching pattern.

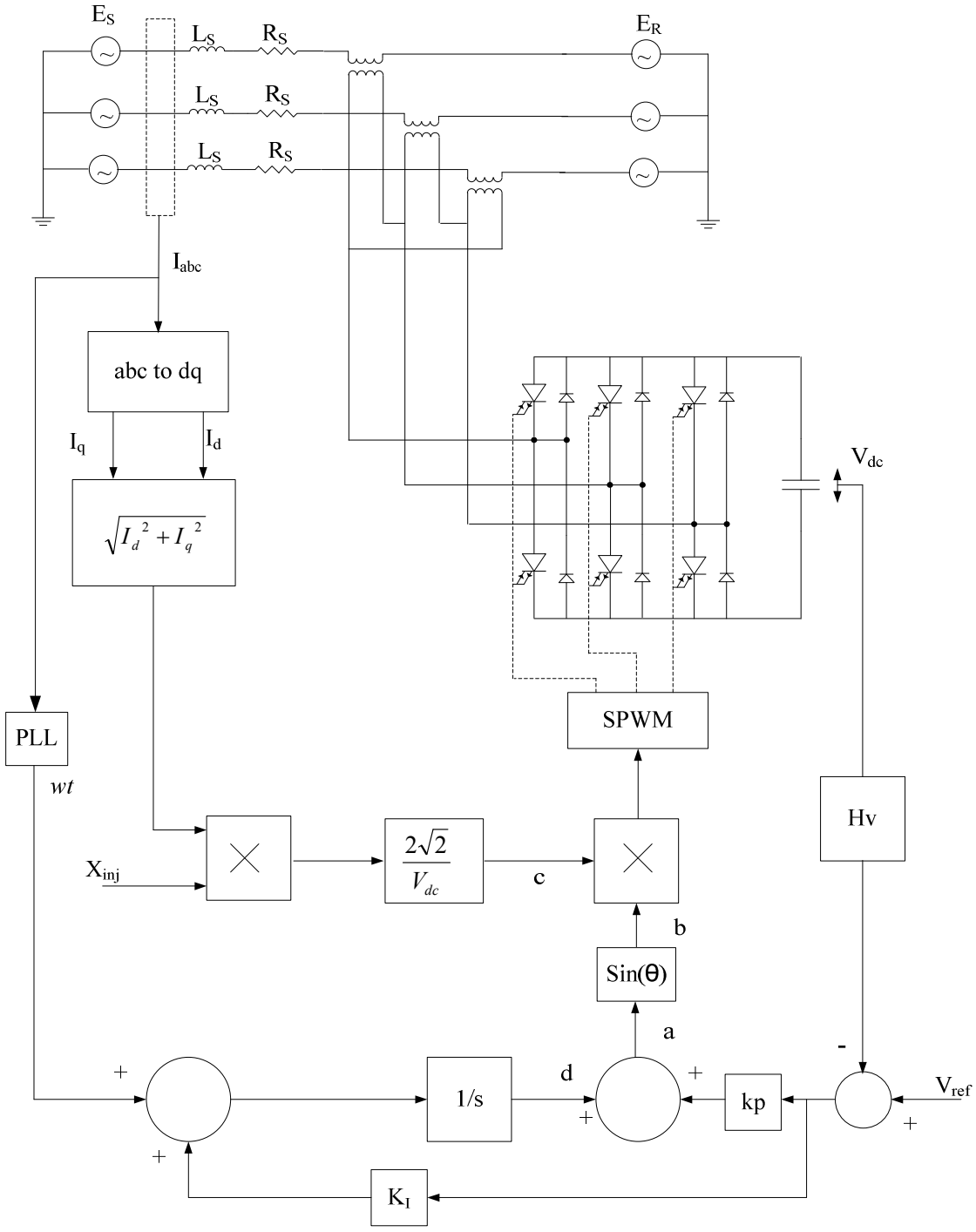


Fig.2.41: Block diagram of dq based controller

2.12.2 Control strategy based on 90 degree phase shift

In another approach the required phase angle i provided by shifting the phase of the line current by 90 degrees. This method is simple, as shown in Fig.2.42, and can be executed by locking to the power system using a PLL. To do so, a PLL must provide the online and synchronised angular frequency of the system based on the line current information. To proceed, $\pm\pi/2$ must be added on top of the phase angle of the line current phasor. However, the amplitude of the injected voltage can be calculated in different ways. For example, it can be included in the phase angle of the reference signal and changed in the DC voltage. Consequently, the DC voltage amplitude can be changed by the amplitude of the final injected voltage. Alternatively, the amplitude of the reference signal can be calculated separately and can be multiplied with the reference sinusoidal signal. While having the amplitude of the reference signal is calculated separately, the DC voltage level remains unchanged. This can be an advantage in the system design and can reduce the cost of equipment.

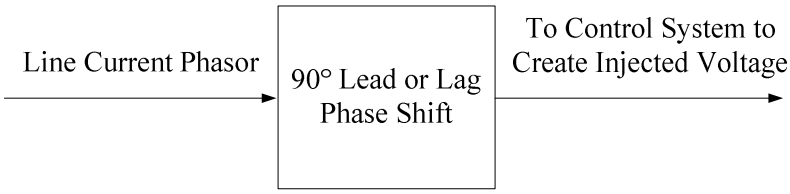


Fig.2.42: Shifting line current

Although this is a simple approach and can even be used in the single phase control, there are some inherent problems with this method that makes its application practically difficult. For example, in this approach it is assumed that if a 90 degree phase shift is introduced between the injected voltage and line current then the injected voltage will produce pure inductive or capacitive reactance. Consequently, there will be no active power exchange between the compensator device and power system. However, to practically in compensate the ohmic and switching losses inside the device, the phase angle of injected voltage needs to be diverted slightly from 90 degrees. Furthermore, the losses can vary for the different amplitude of the injected voltage, allowing the required amount of diversion of phase angle from 90 degree to also vary. As a result, the diversion must dynamically track the losses and try to compensate it. For this reason, having only a 90 degree phase shift within the phasor of the line current and establishing the injected voltage based on the shifted signal cannot be 100% accurate.

However, in the literature review this method is widely used in the implemented control strategies of the SSSC and DSSC [72]. For example, Fig.2.43 shows a control block diagram that is implemented in [35]. In this block diagram, I_d and I_q, the two orthogonal components of line current are calculated using the dq conversion and provide the angular frequency of the power system by PLL. The phase angle is obtained in (2.8) and the magnitude of the current can be calculated from (2.7).

$$\theta = \tan^{-1}\left(\frac{I_q}{I_d}\right) \quad (2.8)$$

The calculated phase angle is used as a base angle and synchronises the injected voltage with the power system voltage phasor. However, in order to have a 90 degree phase shift, as can be clearly observed in the control block diagram, a value of $-\pi/2$ is added on top of the obtained phase angle. The added angle does not consider any losses within the SSSC device, which can threaten the steady state stability of the system.

In the block diagram shown in Fig.2.43, similar to the control systems shown in Fig.2.44, the amount of the injected voltage is calculated based on the amplitude of the line current and the required injected reactance. In control system shown in Fig.2.43, X_q represents the required injected reactance and is multiplied with I, which is calculated using equation (4.6). The resultant signal, after passing through the gain, represents the reference signal for the required DC voltage in the DC link. It means that DC voltage is different for different amount of required reactance injections and the amplitude of the voltage varies based on the value of injected reactance. The signal is compared with the measured DC voltage and the error is added on top of the injected phase angle. This will help the system to maintain the DC voltage for the desired value as by changing the phase angle the system will be able to absorb or inject active power into the system.

The DC voltage can then be regulated and the amplitude of the injected voltage will be adjusted. However, the DC voltage needs to be changed by a different level of compensation. The capacitive or inductive injection by the system will be defined by changing the sign of the added value such that it becomes $-\pi/2$. The system continues by changing the sign of the error, which comes from the deduction of the measured voltage from the reference DC voltage. Finally, the generated phase angle is fed into a sine function to provide the sinusoidal signal. This signal is used by a PWM generator to provide the required switching pattern for the IGBTs.

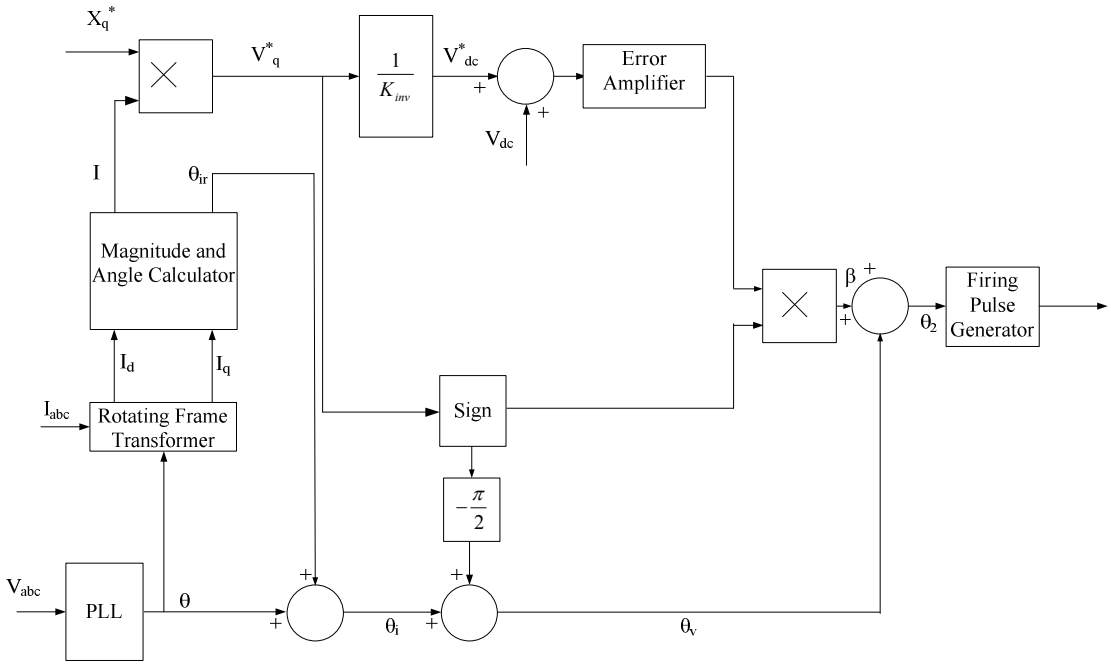


Fig.2.43: Line Current shifted ± 90 degree

A similar approach has been used in [69], where the dq conversion is used to obtain the angle and amplitude. However, in [70]-[71], adding a 90 degree phase has been implemented as shown in Fig.2.44 with slightly differences. In this control strategy, the feedback of the injected voltage is converted to V_d and V_q.

Orthogonal element of the voltage is used to calculate X_S, which is the compensated reactance. The parameter X_S is then compared with the reference reactance and the resultant error is fed into a PI controller. The error provides the fine tuning angle and the angle must be added on top of the *wt* (representing the angular frequency of the power system) which comes from a PLL. However, a value of $\pm\pi/2$ must be added on top of the angle coming from PLL (θ) and the error angle ($\Delta\alpha$) to provide the inductive or capacitive injection.

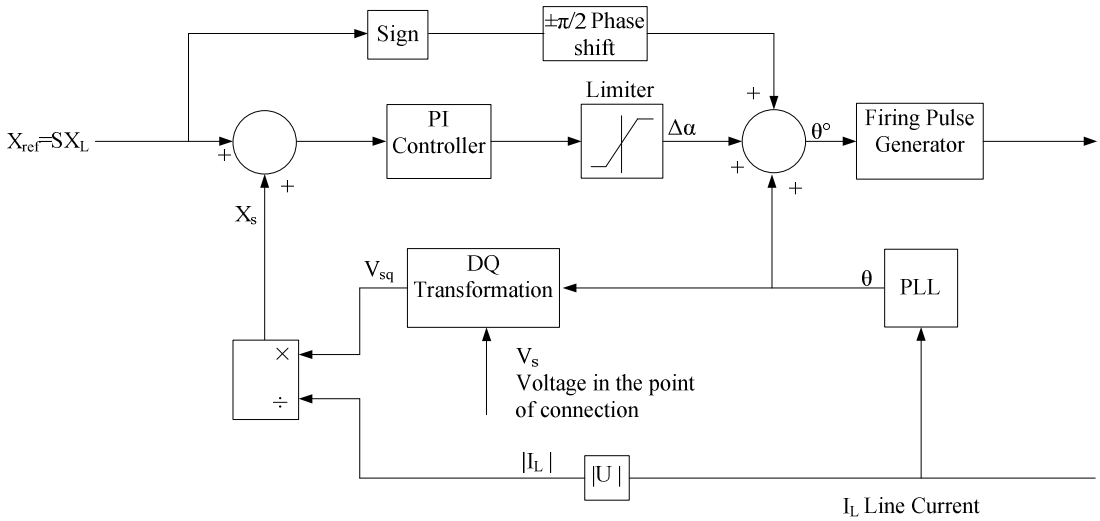


Fig.2.44: Control block diagram of SSSC using 90 degree phase shift

In this strategy, the losses through the filter and even the converter itself are not considered, where the practical experiments can result in instability. To avoid such a problem, there must be another factor which is added on top of the final calculated angle that provides an active power absorption possibility by the converter in order to compensate for the losses.

2.13 Drawbacks with dq based controllers

The dq conversion and its equations have been explained in Appendix A. Using a dq control within a power system can raise some problems when it is unbalanced or harmonically polluted. In unbalance power systems dq components are oscillatory and zero sequence is not zero any more. The oscillatory dq components can cause malfunction of controllers and it will lead to failure of the converter. Furthermore, a dq control can lose the stability in connection with power system with low short circuit levels. The issue is, to a large extent, related to the phase-locked loop and its ability to stay in synchronism with the PCC voltage. As the power changes then the PCC voltage angle changes too. This requires the PLL to re-establish its lock. If the system is weak, this impact is more significant. The situation escalates if we take the resistive part of the system impedance into account (i.e. relatively low X/R ratio) [73].

2.13.1 dq conversion in balanced three-phase system

In all the equations which are explaining the dq conversions in the appendix A, the power system is assumed to be balanced. Otherwise, the conversion can be incorrect

and results in an inaccurate calculation. For example, power systems can be unbalanced if the amplitudes of the voltages in the three-phases are different or if the phase angles between the phases are not identical.

A dq conversion of a balanced three-phase voltage is shown in Fig.2.45. The amplitude of the abc axes is one per unit and the dq axes is also shown with a one per unit amplitude. The amplitude of "q" and "o" are zero and it shows that the applied three-phase system is a balanced system.

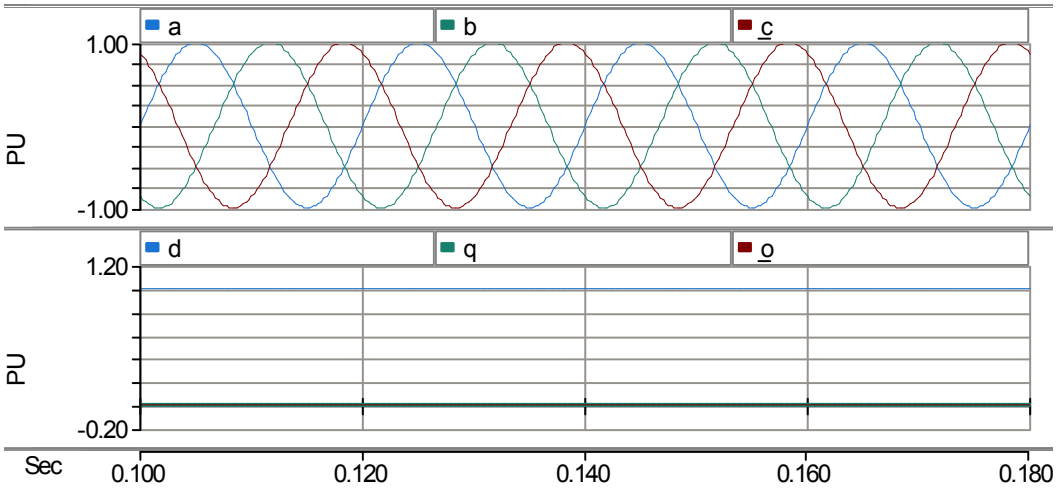


Fig.2.45: dq conversion of a balanced three-phase system

In an ideal case the phase angle between the "d" and "q" components must be 90 degrees. Their amplitude must be also completely independent from each other. This figure shows that with a balanced three-phase system, the "d" and "q" components will be identical. Even if the resultant "d" and "q" components are fed into a dq to abc converter, the resultant abc waveforms will be the same as the original. However, in all of the conversions, the PLL plays a very important role and any failure within the PLL will endanger the synchronicity of the power system.

In the case of an unbalanced three-phase system, the amplitude of the "d" and "q" components can be different. At the same time the phase angle between them can also be different from the previous 90 degree constraint.

2.13.2 dq conversion in unbalanced three wire three-phase system

A three wire three-phase system can be unbalanced because of the different amplitude of voltages in each phase and/or different phase angles between them. The definition of percentage of unbalance is explained in the appendix A. If the phase to phase voltages for the three phases in a three-phase system are 1.2p.u, 0.8p.u and 1p.u, then the average voltage can be calculated as

$$V_{Ave} = \frac{1.2+1+0.8}{3} = 1 \quad (2.8)$$

and then the Max ΔV will be

ΔV=1-0.8=0.2.

The percentage of unbalance can be calculated using equation (A.16) as follow:

$$\text{Percentage of Unbalance} = \frac{100 * 0.2}{1} = 20\ \% \quad (2.9)$$

The dq conversion of unbalance three phase three wire AC system with an unbalance of 20% is shown in Fig.2.46.

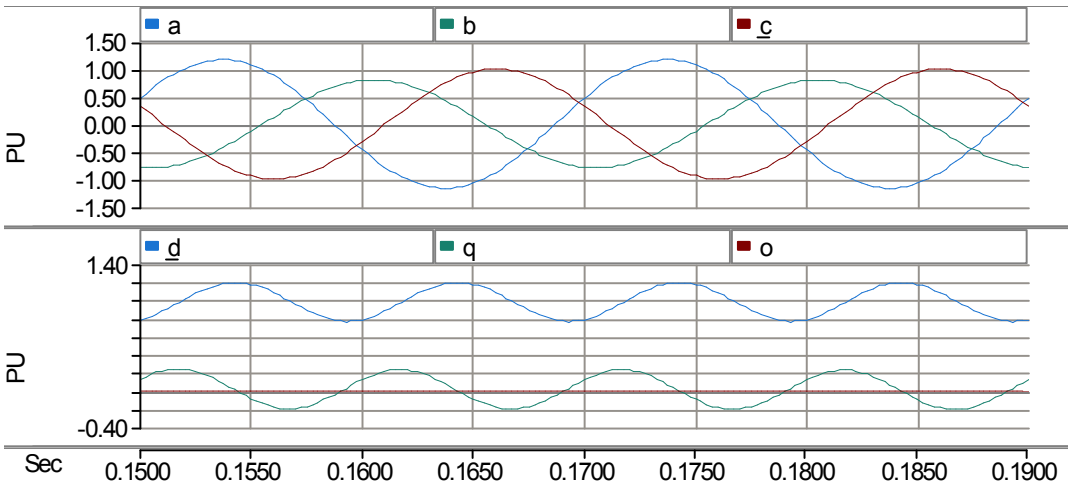


Fig.2.46: abc to dq conversion of unbalance three-phase system

It can be clearly observed that in the dq conversion of the unbalanced system, the amplitude of the "d" and "q" components are different and oscillatory.

Having an unbalanced three-phase system converted to dq and again converted from dq to abc is shown in Fig.2.47. It can be clearly observed that the final conversion to abc is unbalanced, which can increase the disturbance in the AC system. In SSSC applications, when the dq conversion is applied to an unbalanced AC system in order to provide the dq components, the compensation cannot be same in the three-phases. This is because the provided dq components can be inaccurate and the phase angle between them can be

different from the 90 degree requisite. Consequently, after applying the control strategy, the converted signals to abc components will carry incorrect information.

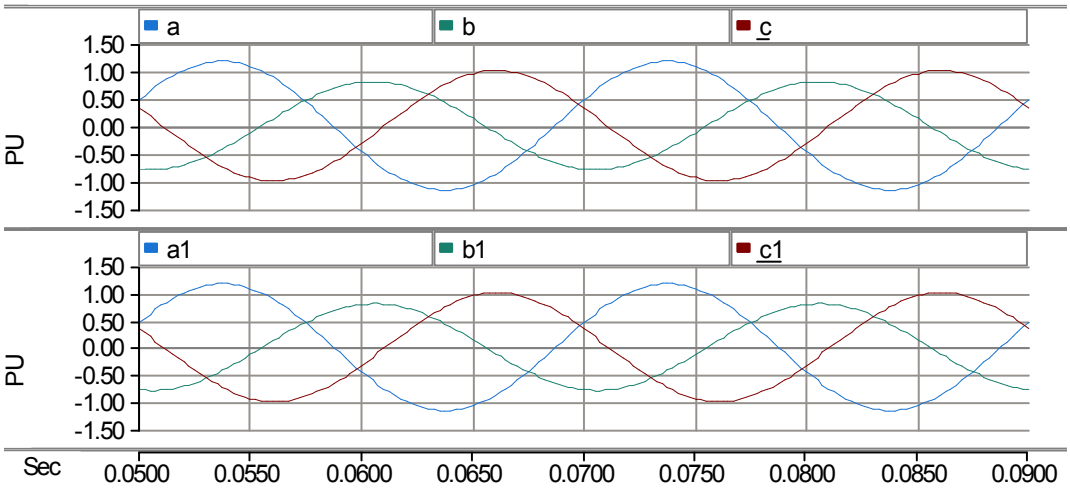


Fig.2.47: Conversion from abc to dq and from dq to abc in an unbalance three-phase system

In another unbalanced three-phase system with identical voltage amplitudes but different phase angles of 100, 110 and 150 degrees, the results of dq conversion can be far from the ideal case. The conversion of abc to dq is shown in Fig.2.48, where it can be observed that when there is a difference in the phase angle in the three-phase system, the amplitude of the "d" and "q" components will be different and oscillatory. In order to observe clearly the detail of the dqo, Fig.2.48 has been spanned through the time axis and it is shown in Fig.2.49.

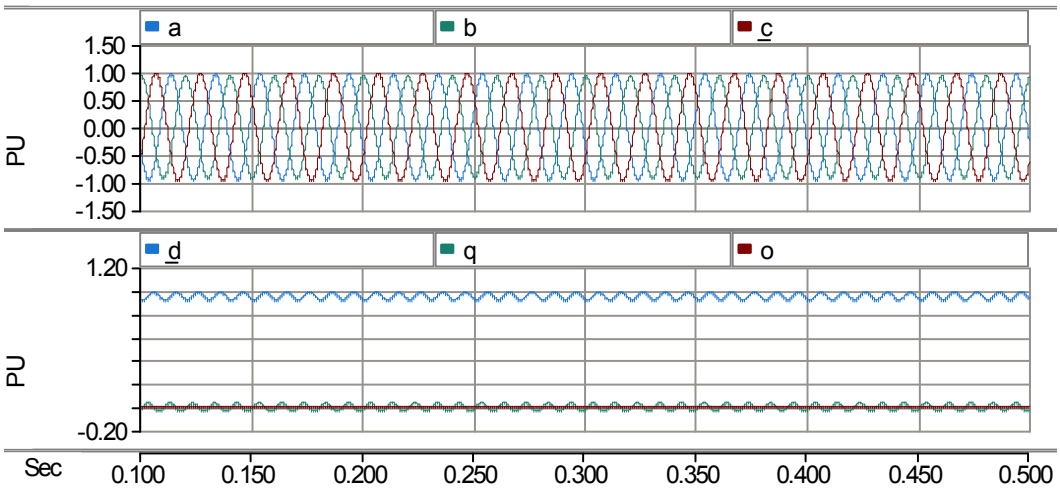


Fig.2.48: abc to dq conversion in an unbalanced system

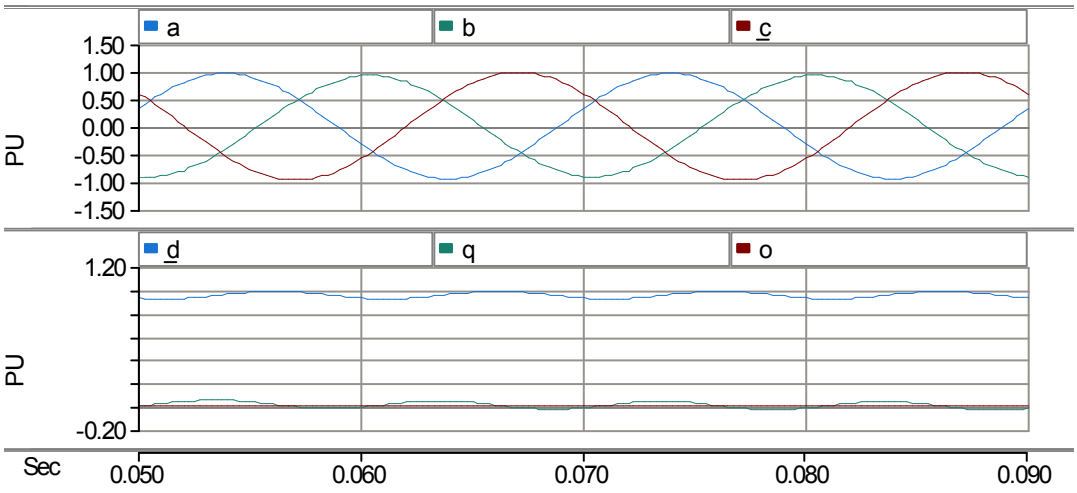


Fig.2.49: abc to dq conversion in an unbalanced system spanned through the time axis

With the intention of investigating dq conversion in the presence of a difference in the angle between the three-phases, the angle between the "d" and "q" components is plotted in Fig.2.50.This figure shows that the angle is approximately 107 degrees, which shows a deviation from the 90 degree. It also means that the dq components are not orthogonal to each other, which can be problematic. For example, in control strategies that establishes all of the calculations related to the active power on the "d" component where all of the calculations pertaining to the reactive power are based on the "q" components, the 90 degree phase angle between the dq components are required in order to control active power and reactive power independently. Consequently a malfunction of a control system through the missing of such a requirement can be expected.

For instance, if an unbalanced system is converted to dq and simply converted back to abc, the resultant waveform will also become unbalanced. This is shown in the Fig.2.51. It can be seen that the $a_1b_1c_1$-, which is converted from dq to abc-, is same as the abc. It means that in the case of the application of dq conversion in SSSC controllers, the injected voltage itself is not balanced and can result in a different amount of compensation through the line.

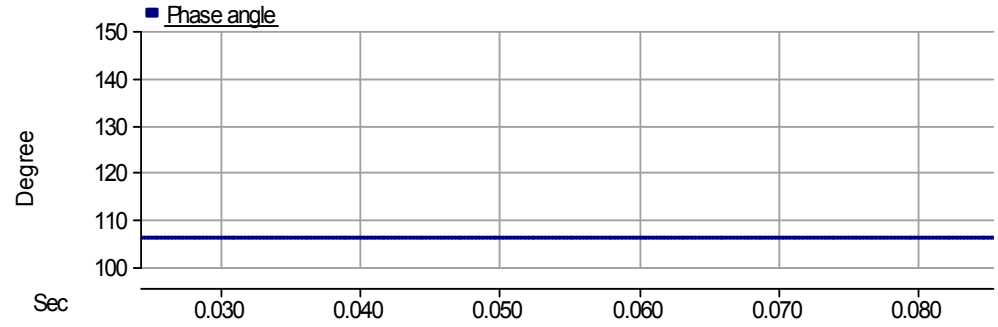


Fig.2.50: The angle between the "d" and "q" components in an unbalance system

In addition, the unbalanced compensation can unequally change the impedance of the line and consequently increase the unbalance of the system.

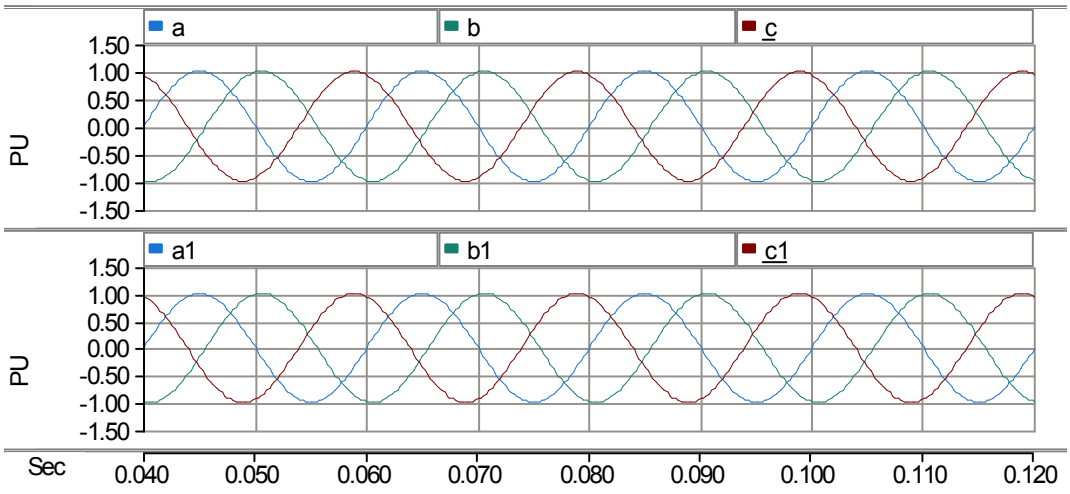


Fig.2.51: Conversion from abc to dq and from dq to a1b1c1

However, the simulation results show that the resulting dq components can carry wrong information, thus the control system will be fed with incorrect signals. In the literature review of the SSSC and the DSSC, the unbalanced system has not received much attention and therefore there is a drawback in this subject.

2.13.3 Decomposition of an unbalanced AC System

However, the problems of the unbalanced system, along with its side effects, have been investigated in other applications using VSC. For example, in a vector control based systems, an unbalanced AC system is decomposed into positive and negative sequences and both of them have been used separately in the control algorithm [74]-[76].

However, the decomposition of an unbalanced system into the three balanced system is needed. An unbalanced three-phase system can be written as

$$[Unbalance\ three\ phase\ system] = [conversion\ matrix][balanced\ three\ phase\ system]$$

or

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix} \tag{2.10}$$

After having the positive and negative sequences obtained using (2.11) they are then converted to dq components. The control strategy is then applied separately to the negative and positive sequences [3], [77] as shown in Fig.2.52.

$$[V_{abc+} \quad V_{abc-} \quad V_{abc0}]^T = \frac{1}{3} \begin{bmatrix} 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \\ 1 & 1 & 1 \end{bmatrix} [V_a \quad V_b \quad V_c]^T \tag{2.11}$$

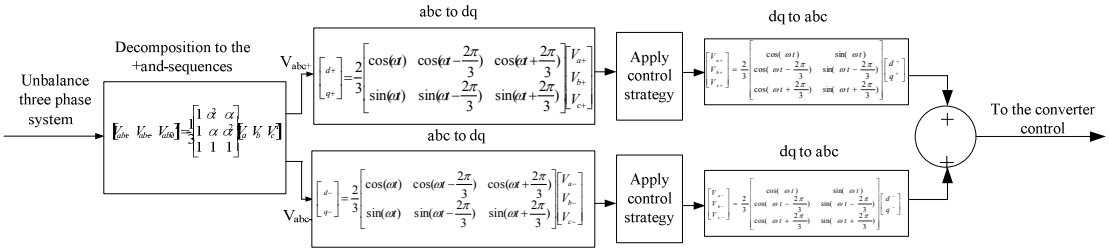


Fig.2.52: Block diagram of decomposition of an unbalance system and applying dq conversion

In the block diagram shown in Fig.2.52, the control strategy has been applied to the dq^+ and dq^- separately. The resultant signals are then individually fed into a dq-to-abc conversion in order to generate the signals in the abc format. The generated signals are summed up to provide final signal which will be fed into the rest of the controller.

Although the above mentioned method is useful for unbalanced systems, it cannot be recommended when there is a zero sequence with positive and negative sequences in the system.

The presence of zero sequence depends on type of unbalance load. For example in four wire star three phase system zero sequence will appear in the natural wire and all three phases however in three wire star system there will be no zeros sequence. In delta three wire system there is no natural wire but in presence of unbalance load there will be zero sequence in phase currents [78].

If there is zero sequence then it will not be compensated in the approach shown in Fig.2.52 and as such, it can disturb the final signal. For example, an unbalanced signal that is a combination of 0.85 p.u positive sequence, 0.1 p.u negative sequence and 0.05 p.u zero sequence has been investigated. The resultant final signal, as shown in Fig.2.53, in abc format is the conversion of the combination of the positive and negative sequences. However, the amplitude of the waveform shows that it is less than 1p.u, in fact it is actually 0.95 p.u. It can be argued that the contribution of the zero sequence, which is equal to 0.05 p.u, is missing and for this reason, the final value of the converted signal is less than 1 p.u. One of the advantages of this method is that the final converted waveform, which includes the positive and negative sequences, is in phase with the positive sequences and rotates synchronously with the positive sequences. With the intention of comparing the phase angle between these two signals, the positive sequence and the final converted signal are plotted in Fig.2.54.

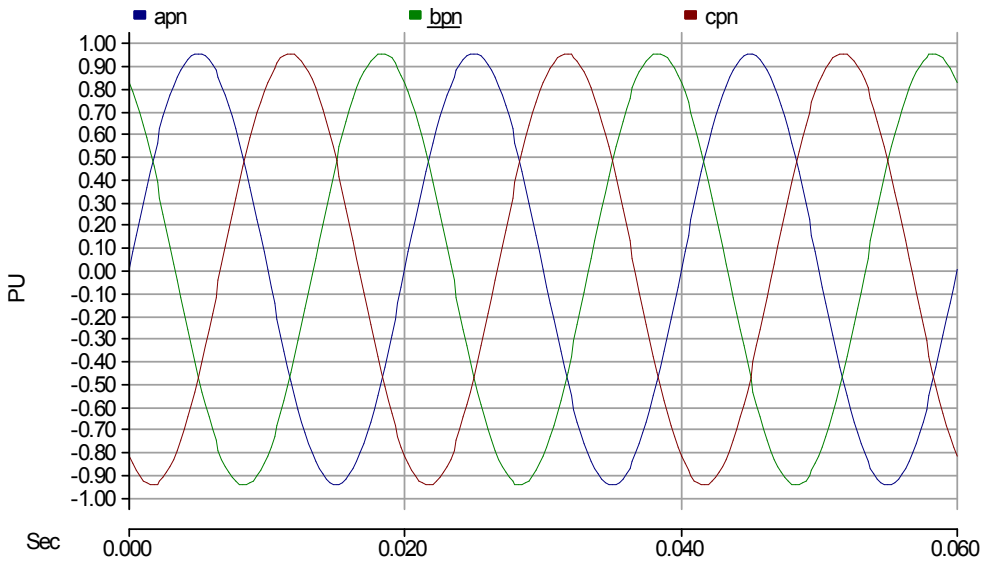


Fig.2.53: Conversion of combination of positive and negative signal

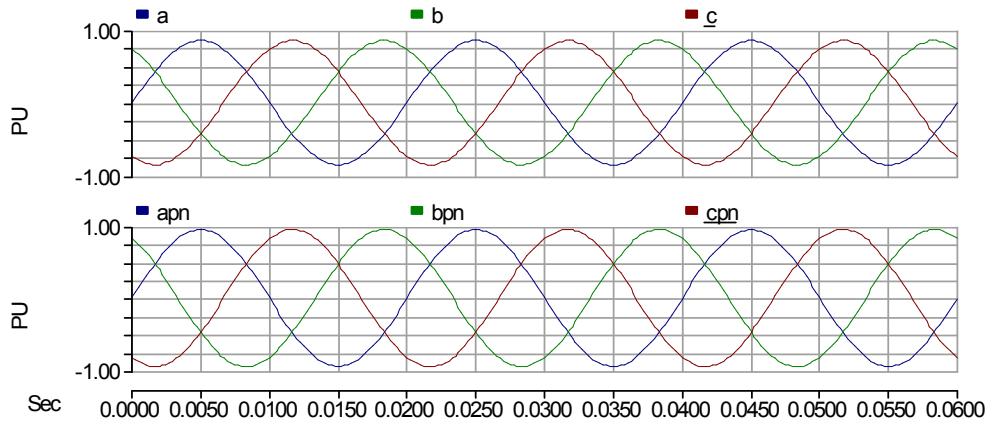


Fig.2.54: Positive sequence and final converted waveform

In the above figure the synchronicity among the positive sequences and the final converted waveform is obvious, but for the purpose of clarity, the phase angle difference between them is plotted in degree in Fig.2.55. This plot shows that the phase difference between them is absolutely zero.

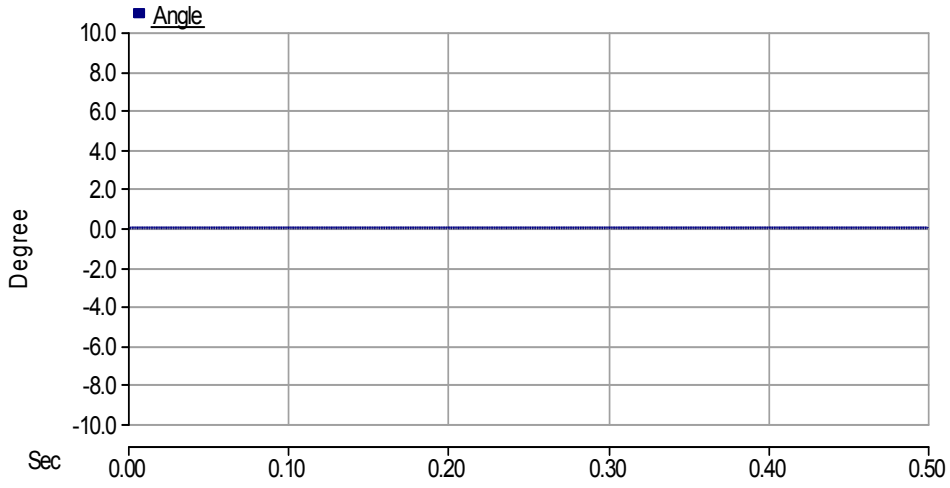


Fig.2.55:Phase angle difference between the positive sequences and the final converted waveform

The dq conversion clearly has the advantage of synchronisation with the final waveform with the positive sequence. However, this advantage can easily disappear with a malfunction of the PLL. The reason for this is based on the equations (A.11) and (A.13), where the synchronisation is ensured by providing an accurate value of wt, and the value wt is updated constantly by PLL. At the same time, the proper operation of the

PLL can be endangered by various issues. For example, in harmonically polluted electrical networks, tracking the correct frequency can be an issue. Furthermore, in weak AC electrical networks, switching events or even a load rejection can cause the PLL to lose synchronicity because of a SCL. Moreover, the PLL itself has a PI controller as shown in Fig.2.56 [79], [80] which is tuneable based on the value of its proportional or integrator gain, such that the output error can be minimised.

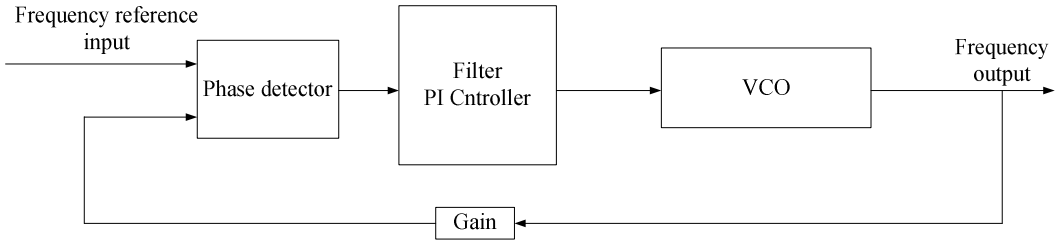


Fig.2.56: Block diagram of the phase locked loop (PLL)

The tuning of the PLL for a SCL of an AC system is one of the key parameters which must be considered [81]. However, the SCL of a power network can be changed by some events such as tripping a line or coming in or out of a power plant. Practically, the mentioned events usually happen in the electrical power networks and when the change of a SCL is unavoidable. On the other hand, a PLL that is tuned for a system with a high short circuit level may not work or may not have the same performance for a system with a low SCL. Subsequently, any change in the SCL may result in an out of tune PLL, which will require retuning for updated system parameters.

Based on the aforementioned problems regarding the operation of a PLL in connection with an AC system, it can be argued that a PLL can reduce the reliability of the dq conversion. In this study and in the literature review, it has been noted that the dq conversion has been used in most of the controllers in the literature review. However, synchronicity is a key requirement of a control system that must be met otherwise the controller will lose the orthogonal injection of series voltage.

In addition the amplitude of the “d” and “q” components must be accurate, otherwise a pure reactive power injection that is mainly based on the “q” component can be mixed with the active power injection. This can lead to instability and finally the DC voltage will collapse. Furthermore, the phase angle between the “d” and “q” components can be diverted from the 90 degree in the presence of unbalanced power systems and consequently this will disturb the assumption of having two orthogonal components in

the dq domain. It is worth mentioning that having two “d” and “q” components that are orthogonal is a key requirement to provide an independent control of active and reactive power. This future is very dominant when the dq conversion is used by a vector control through the control system.

In order to avoid employment of dq conversion within the control of either DSSC, it is required that a controller to be independent from the unbalance in the system. A novel approach based on the single phase control rather than three-phase will be introduced in chapter 4.

2.14 Summery

Line reactance is a key parameter in determining the available transmission capacity of a power line. Also, it is an important factor in the voltage stability and power system stability enhancement. To achieve these, line reactance can be altered and one of the alteration methods is the use of series compensation techniques. Series compensation can be achieved in different ways. Traditionally, fixed capacitors are employed in series with transmission lines in order to reduce the effects of line inductance. However, fixed capacitors can only introduce capacitive compensation and are not able to provide an inductive reactance which may be required in a power flow control problem. There are also other issues associated with the application of fixed capacitor in an electrical network. Fixed capacitors can initiate a SSR phenomenon and the resultant resonance can damage the network.

For this reason, the use of series compensation devices utilising power electronics switches was established. A number of such schemes, such as TSSC and TCSC devices, were reviewed in this chapter and their principles of operation outlined. The use of voltage source converters as series compensation devices in SSSC schemes has also been described. The many operational advantages of SSSC circuits have been discussed as well as their drawbacks in terms of their high costs and reliability issues associated with the flow of short circuit currents.

DSSC was introduced as a concept to overcome some of these problems. This device is a single phase device and it is comprised of a VSC converter and STT. It is suspended from the power lines and it can be easily assembled and disassembled. It has low power rating in comparison with the power electronics based series compensators.

Concept of control of DSSC is discussed followed by an explanation of the commonly used controllers in the literature review. Two different methods of using 90° phase shift

and dq conversion based control strategy have been identified. Both methods have been explained and their advantages and disadvantages were discussed.

In 90° phase shift method the injected voltage can be built based on the shifting 90° phase of the line current. This will provide a signal that is orthogonal to the line current. However, because of the losses, it can cause instability in the system. To avoid instability, the injected phase angle must be slightly different from the 90°. Although the adjustment of the phase angle in order to be diverted slightly from 90° degree to compensate the internal losses inside the DSSC must occur frequently, otherwise the operation of device will not be stable.

In dq based controllers use of PLL is necessary and in most of the phase control strategies applied here, the dq conversion has been used. Nevertheless, the dq conversion in the presence of unbalanced system can result in inaccurate dq components in terms of amplitude or the angles in between. Furthermore, an unbalanced system can be decomposed into positive, negative and zero sequences. The negative sequence can be compensated by its conversion to the dq domain, applying the same control strategy as that used for the positive sequence. However, the compensation can only be obtained in systems where their unbalance limited to a very low percentage, less than 5% for example. Additionally, in this approach only a negative sequence is being compensated and the zero sequence remains uncompensated.

To overcome the investigated control problems, there is a requirement for a controller to operate as a single phase controller and adjust the angle automatically.

3 Applications of DSSC in distribution networks

In this thesis, DSSC is proposed as a Distributed FACTS (D-FACTS) device in 11kV electrical power distribution networks. The proposed approach is presented in Fig.3.1. In this figure, an 11 kV overhead line distribution feeder is being fed from a distribution substation and is supplying a residential and industrial load.The aim of application of DSSC in the distribution network is to dynamically compensate line reactance through the power line. By decreasing or increasing the line reactance it is possible to push away current from or pull into a specific line. In addition DSSC can help to increase the ATC of the compensated feeder. This is a very valuable achievement in the distribution networks because the rate of increasing demand for the consumption of electricity and consequently its generation is high.

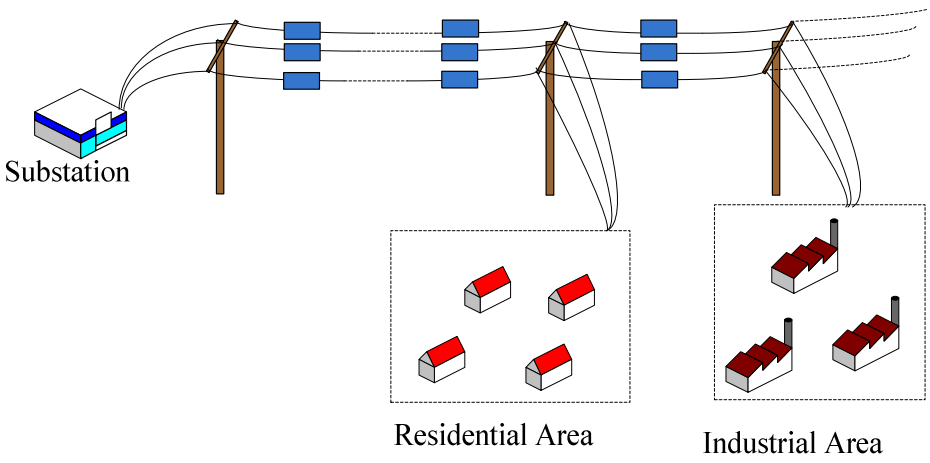


Fig.3.1: Application of DSSC in electrical distribution networks

However, expansion of distribution utilities has not received much attention. Extra tension is applied to the distribution networks by direct connection of the renewable energy resources such as wind farm and solar panels. For this reason application of DSSC in the distribution utilities can release the capacity of distribution lines, hence provide capability of enhancing the distribution networks reliability.

Usually distribution feeders supply loads using radial topology. The drawback of this arrangement is that all loads will be cutout when a trip occurs. Such interruption in these feeders is not acceptable, therefore DSSC can be a solution for these networks. DSSC suspends from the power line through STT, so the line current does not pass

through the DSSC directly. It means that it is not in series with the line directly and in the case of failure it can be easily bypassed without interrupting the power flow in the power line. By passing one DSSC device will not have a big effect on the compensation because other DSSC device are still in order and they can continue providing compensation.

In this study, the application of DSSC in the distribution networks and the consequent side effects has been investigated. Further to that the main body of research is focused on the control of DSSC itself (control of voltage source H-bridge converter).

3.1 Applications of DSSC in the distribution networks

DSSC has distributed nature and its application through the distribution feeders can make the power lines to act like a smart wire. This means that injecting proper voltage (with controlled amplitude and phase angle) in series through the line can improve different parameters of the power system. For example DSSC can be employed to help load flow control in the networks. It can mitigate congestion in a particular line or it can divert the load current in other alternative corridors. In another application it can be used as a voltage profile improver. These applications have been investigated and are explained in the following subsections. However, line resistance in the distribution networks is higher and proper operation of the DSSC in distribution networks must be investigated.

3.1.1 Effect of line resistance on the control of DSSC

Employed controller within a DSSC provides a reference signal for the converter to inject a voltage for line reactance alteration purpose. Alteration of line reactance by DSSC can affect the transmission capability of the line both by increasing or decreasing the transmitted power. It depends on the X/R ratio of the uncompensated line and for low ratios compensation can reduce the transmission capability of the line.

Transmitted power (including active power and reactive power) between two buses in a power system shown in Fig.3.2 can be calculated using equation (3.1).

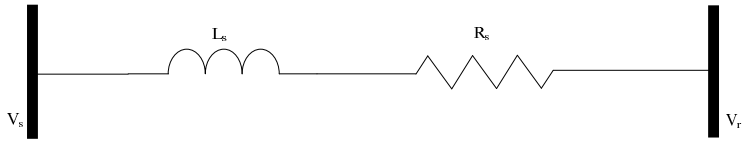


Fig.3.2: Two bus AC power system

$$S = \overline{V}_S \left[\frac{\overline{V}_S - \overline{V}_r}{R_S + jX_L}\right]^* \quad (3.1)$$

Where V_S and V_r are the sending end and receiving voltages and R_S, X_L are representing the resistance and reactance of the line. V_s and V_r can be substituted with their amplitude and angle, then (3.1) can be rewritten in equation (3.2).

$$S = \frac{V_S V_r e^{-j(\theta_1 - \theta_2)} - V_S^2}{R_S - jX_L} \quad (3.2)$$

Using Euler formula represented in (3.3) and substituting equation (3.4) the complex power is recalculated in (3.5).

$$e^{j\alpha} = \cos\alpha + j\sin\alpha \quad (3.3)$$

$$\delta = \theta_1 - \theta_2 \quad (3.4)$$

$$S = \underbrace{\frac{R_S V_S V_r \cos\delta - R_S V_r^2 + X_L V_S V_r \sin\delta}{R_S^2 + X_L^2}}_{\text{Active Power}} + j\underbrace{\frac{XV_r^2 - V_S V_r(\cos\delta - R_S V_S V_r \sin\delta)}{R_S^2 + X_L^2}}_{\text{Reactive Power}} \quad (3.5)$$

assuming bus voltages in both ends are 1p.u then V_s will be equal to V_r and with substituting this assumption in (3.5) active power and reactive power is calculated in (3.6) and (3.7) respectively.

$$P = \frac{V^2}{R_S^2 + X_L^2}[X_L \sin\delta - R_S(1 - \cos\delta)] \quad (3.6)$$

$$Q = \frac{V^2}{R_S^2 + X_L^2}[R_S \sin\delta + X_L(1 - \cos\delta)] \quad (3.7)$$

in long lines $\frac{R_s}{X_L}$ is negligible and by substituting this in equations (3.6) and (3.7) active and reactive power equations are written in (3.8) and (3.9).

$$P = \frac{V^2 X_L \sin\delta}{R_S^2 + X_L^2} \quad (3.8)$$

$$Q = \frac{V^2 X_L(1 - \cos\delta)}{R_S^2 + X_L^2} \quad (3.9)$$

Practically, power lines have some ohmic resistance along with reactance and with considering nonzero value for R_s the transmitted active power is written in (3.10) by rearranging (3.8) and substituting R_S with R and X_L with X.

$$P = \left(\frac{X}{R}\right)\frac{V^2 \sin\delta}{R\left(1 + \left(\frac{X_L}{R}\right)^2\right)} \quad (3.10)$$

Then transmitted power versus δ(phase angle difference between voltages at the both ends of line) will be affected by X/R ratio of line. This is shown by plotting P using equation (3.6) for different values of X/R ratio in Fig.3.3.

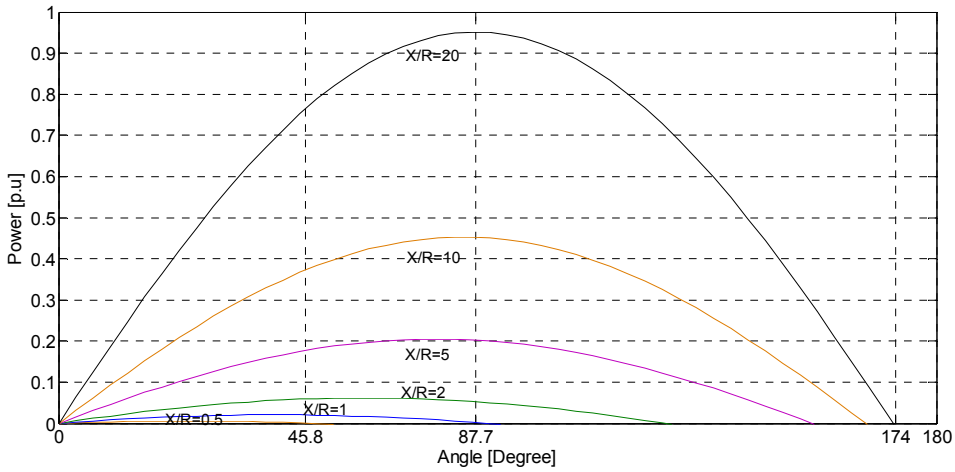


Fig.3.3: Effect of X/R ratio on the transmitted power

This plot clearly shows that if the X/R ratio goes high the ATC will be high and vice versa. In addition with low X/R ratio peak value of power occurs in lower angles which can endanger stability of the system. For example in Fig.3.3 peak value of power for X/R ratios of 20 and 10 take place in almost 87° however for lower ratios such as 1 it happens in 45.8°.

In order to investigate the effect of X/R ratio on the transmitted power a two bus AC power system as shown in Fig.3.4 has been utilized and simulated in PSCAD.

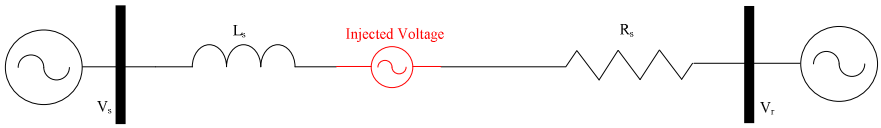


Fig.3.4: Compensated AC power system

In power lines with higher X/R ratio normally capacitive compensation is required to reduce the effect of inductive reactance. However the reduction of X must be in a way to not endanger the stability of power system.

In compensation using DSSC the transmitted power between the sending end and receiving end buses becomes function of injected voltage and it is obtained in (3.11) [1], [55].

$$P_{sr} = \frac{V^2 \sin\delta}{X_L} - \frac{\overbrace{VV_{Inj}\cos(\frac{\delta}{2})}^{P_{com}}}{X_L} \qquad (3.11)$$

where P_{com} is the contribution of compensation provided by injected voltage V_{Inj}. In (3.11) the following assumption has been used

$$V_s = V_r = V \tag{3.12}$$

where V_s and V_r are the bus voltages. By substituting V_r and V_s with V in (3.11) the new equation is obtained in (3.13).

$$P_{sr} = \frac{V_s V_r \sin\delta}{X_L} - \frac{V_s V_{Inj} \cos(\frac{\delta}{2})}{X_L} \times \overbrace{\left[\frac{\sin(\frac{\delta}{2})}{\sqrt{(\frac{V_s+V_r}{2V_r})^2 - \frac{V_s}{V_r}\cos^2(\frac{\delta}{2})}}\right]}^{is\ unity\ if\ V_s=V_r=V} \tag{3.13}$$

The parameter X_L is the line reactance and δ is the phase angle between V_s and V_r. The effective inductance will be changed by injecting capacitive or inductive reactance through the line by using DSSC between the two buses. As a result, the transmitted power will be changed, as shown in Fig.3.9.

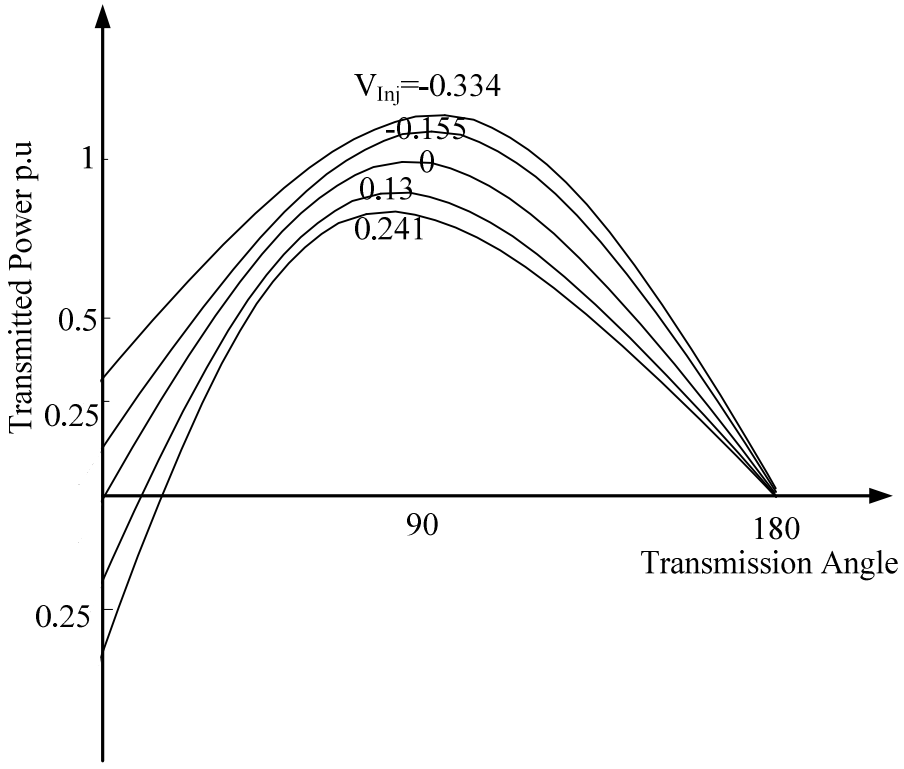


Fig.3.5: Change of transmitted power against transmission angle

However, by compensating the line reactance then the phase angle of voltages at the receiving end buses will also change. For this reason, the DSSC can also be employed as a distributed static phase shifter (DSPS) through the networks. Theoretically phase

angle of 90° and above can lead to instability in the power system due to interaction with governor of generators [85].

3.1.2 Calculation of required numbers of DSSC

The provided compensation by DSSC is calculated in equation (3.14).

$$X_{inj} = \frac{V_{inj}}{I_{line}} \tag{3.14}$$

where X_{inj} is the provided reactance and V_{inj} is the injected series voltage by each DSSC module and line current is represented by I_{line} in this equation. Assuming K_c percentage of the line reactance, X_l, is required to be compensated and it can be calculated as follow

$$X_{cd} = K_c X_l \tag{3.15}$$

where X_{cd} is demanded compensation reactance.

In the other hand each DSSC devices has a limited capability in providing compensation, X_{inj}, through the line. The restriction is defined mainly by the rating of the components and the voltage source converter within the DSSC device. However, number of required modules is calculated in equation (3.16).

$$n = \frac{X_{cd}}{X_{inj}} \tag{3.16}$$

where n is the required number of DSSC devices through the line. For example, in a power line (as shown in Fig.3.2) with 20 miles length, total reactance of 6.25Ω and resistance of 2.86Ω for FeAl234 conductor can be obtained from Table 3.1. This table shows typical line parameters in an 11kV distribution system. Assuming a compensation of 20% is required then DSSC modules must provide 1.25Ω capacitive reactance. Each module can be designed to inject 10V (depends on the design of DSSC the injected voltage can be customized to different values) orthogonal with line current of 345A then provided capacitive reactance by the module will be 0.02898Ω. By dividing required capacitive reactance, 3.98Ω, with provided reactance of 0.057Ω the number of DSSC modules will be 43. Summary of parameters and corresponding values within the explained example is presented by Table 3.2 [84].

ACSR Type	Cross section	Current capacity	R	L
FeAl234	234mm2	345A	0.143Ω/mile	0.996mH/mile
Chickadee	1118mm2	575A	0.2281Ω/mile	1.19mH/mile

Table 3.1: Typical bare conductors in an 11kV distribution system

Parameter	Value
Reactance of the line	6.25Ω
Resistance of the line	2.86Ω
Percentage of compensation	20%
Line current	345A
Injected voltage	10V
Injected reactance	1.25Ω
Required number of DSSC devices	43

Table 3.2: Summary of parameters and corresponding values

3.2 Load flow control using DSSC

In order to investigate capability of DSSC in controlling load flow in electrical distribution networks a power system including two parallel lines has been considered. The power system is shown in Fig.3.10 and the system parameters are tabulated in Table 3.3. Line1 is equipped with 20 DSSC devices and its reactance can be compensated. Current capacity of line1 is higher than line2 and the aim is to divert current from line2 to line1 using DSSC.

Line number	Conductor type	Line resistance	Line reactance	Compensation	Line current capacity
1	ACSR (Chickadee)	2.368Ω	5.175Ω	Yes	575A
2	ACSR (FeAl234)	2.86Ω	6.25Ω	No	345A

Table 3.3: System parameters for two parallel lines

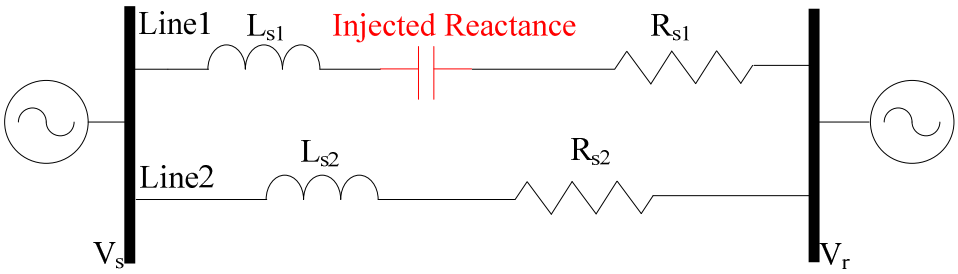


Fig.3.6: Compensation of two parallel lines

Line1current in at different level of compensation is plotted in Fig. 3.11. In this figure current in line1 is shown with blue line and in line2 is shown with green. First time interval belongs to the system with no compensation and the second belongs to a system with 20 % compensation provided by DSSC modules in line1. In this time interval as a result of compensation, current in line1 increases because of less line impedance and in the line2 the current decreases. Third time interval of the plot show the result of further compensation and corresponding changes of current in the lines. This is a very useful feature of application DSSC in the distribution networks which allows the operator to divert current partially from one line to another.

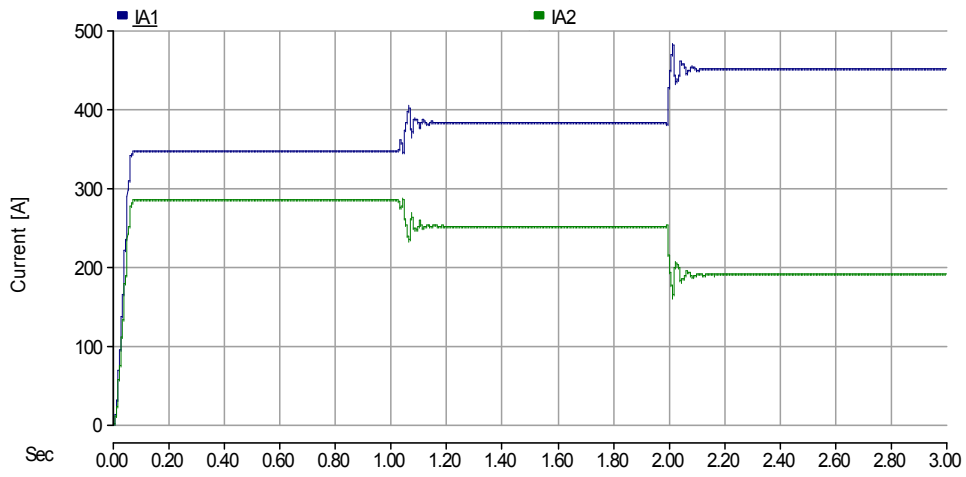


Fig.3.7: Phase current with different level of compensation

DSSC not only can push current into the compensated line but also it can pull away current from the compensated line. This can be achieved by injecting inductive current through a line. Fig.3.12 shows current is pulled away from line1 and pushed into line2. In this figure at first there is no voltage injection but afterward with injection of 20 % inductive reactance current in line1 goes down and in the same time it goes up in the line2. Moreover with increasing the injection of inductance furthermore the line current in line1 decreased further and it is increased in line2.

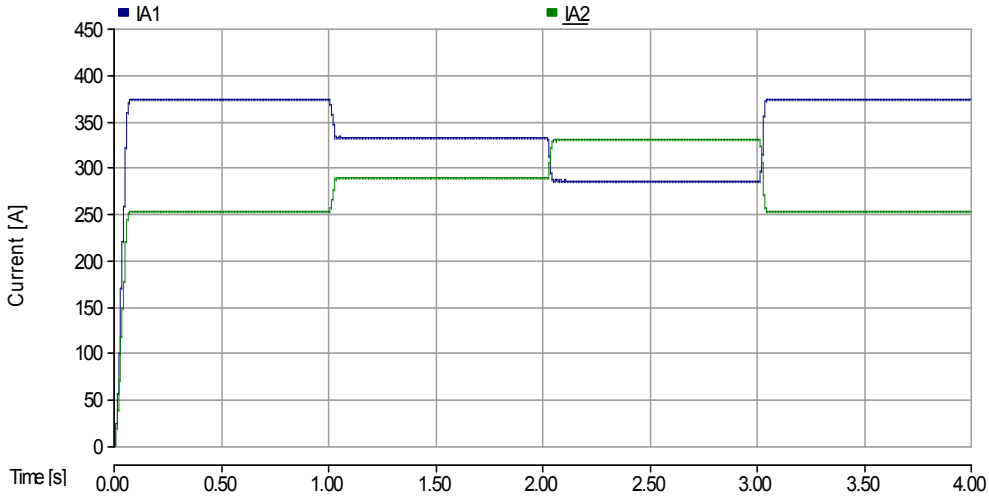


Fig.3.8: rms value of lines current in presence of inductive injection

3.3 Voltage profile improvement using DSSC

In the distribution feeders the loads connected to line in different distances from the distribution substation. Consequently the impedances of the lines are different and then the amount of voltage drop across the lines will be different. Actually, the voltage drop increases when the distance increases. The voltage drop is a combination of the drop produced by the ohmic resistance of the wire and its inductive reactance. Because the inductive reactance can be compensated by using DSSC [88], therefore this opens a new application for the DSSC, which is proposed in this study to improve voltage profile in the power distribution networks and compensate the voltage drop which comes from the inductive resistance of the line.

The distributed nature of DSSC units facilitates their independent operation even with the reconfiguration of the network. Generally, the overhead line distribution networks are more vulnerable to short faults but the DSSC modules are immune against the consequence of flowing the short circuit currents. This is because in the case of a short circuit fault in the power system, a very small amount of current will be transferred to the power electronics side of the DSSC device, which is connected in the secondary side of the single turn transformer with turn ratio of, let say, 1:100. The mentioned feature nominates the DSSC as a reliable solution in reactive power compensation in the distribution feeders.

In this application the DSSC modules are connected to the feeder in series as shown in

Fig.3.13 in order to compensate the reactive consumption of the line itself. Fig.3.14 shows part of a loop distribution network with DSSC devices and lumped loads along the length of the line. The loads through the feeder can be supplied from both substations A and B. However, conventionally in the distribution feeder in order to increase the voltage at the end of feeder some fixed capacitors have been used. However, with the reconfiguration of the network topology the voltage at the end of feeder (which is now the begging of the feeder) can be high enough and then there is no need to have the capacitors to increase the voltage. In that situation the application of fixed capacitors can be problematic. In contrast to that, the application of DSSC modules is independent from the reconfiguration of topology of the network because it can provide compensation through the line rather than in one point of the feeder.

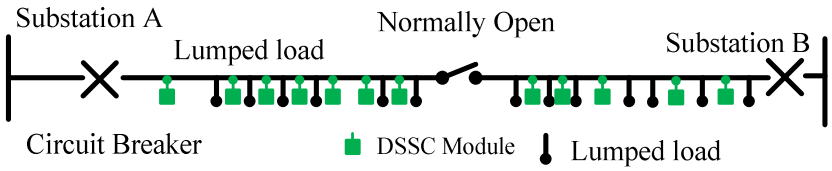


Fig.3.9: 11kV loop distribution network including DSSC devices

Each DSSC module behaves like voltages source through the line. It works based on injecting capacitive voltage in order to eliminate the effect of line reactance. Fig.3.14 show the model of feeder equipped with the DSSC modules. In this model R_i and L_i (i=1, n) are the resistance and inductance of the section of the line which are located between two DSSC modules and the DSSC models are represented by the voltage sources.

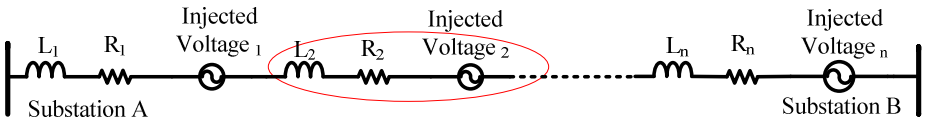


Fig.3.10: The model of feeder equipped with the DSSC module

Considering one segment of the line in Fig.3.14, the voltage drop in that section can be calculated as follow:

$$V_{drop} = R_n I + jX_n I + V_{injn} \quad (3.17)$$

where V_{drop} is the series voltage drop across the segment, I is the current through the feeder and V_{injn} is the voltage injected by the DSSC module number n. As V_{injn} is orthogonal with the line current, it can be expressed as:

$V_{injn} = (\pm jX'_n I)$ (3.18)

where X'_n is the effective injected reactance. It must be noted that since X'_n is not a physical reactance then it cannot affect the system impedance at frequencies other than fundamental frequency. For this reason it can contribute toward amplifying or mitigating the amplitude of the harmonics through the line and it cannot initiate an oscillation through the system.

Furthermore, in the presence of an inductive load, the line current can be expressed as follow:

$I_l = I_P + jI_Q$ (3.19)

Substituting (3.18) into (3.17), the V_{drop} can be calculated as follow:

$$V_{drop} = \sqrt{R^2 + (X \pm X')^2}\, I_l \quad (3.20)$$

From the above equation V_{drop} can be decreased or increased (based on the polarity of X' which depends on whether the injected voltage lags or leads the line current) allowing the line voltage profile to be controlled. In the distribution networks resistance of the line is bigger than reactance however manipulating of reactance still will change voltage profile. The application of DSSC not only alters the voltage drop across the line but also decreases or increases the inductive reactive power flow through the line. This is demonstrated by the following calculations:

$$V_{drop}\ I^* = R(I_P^2 + I_Q^2) + j(X \pm X')(I_P^2 + I_Q^2) \quad (3.21)$$

The first term in (3.17) is the active power losses and it dissipates as heat in the line. The second term represents the line reactive power consumption which can be reduced by injection of X'. This will release part of occupied capacity of the line and also will reduce the voltage drop through the line. Furthermore, providing the reactive power consumption of the line DSSC module will reduce the absorbed reactive power from the substations which will improve the voltage at the compensated buses.

The application of DSSC in the distribution networks has been simulated using the PSCAD/EMTDC software. In this simulation, it is assumed that the circuit breaker is closed at substation A and it is open at substation B so that the circuit is effectively working as a 20km radial feeder which is fed only from substation A. A lumped load of 3MVA was assumed at the remote end of the 20km, 11kV line. Line resistance of 2.86Ω and reactance of 6.25Ω are used in the calculations [84]. Twenty DSSC modules are distributed along the length of the line and each of them is connected in series through a single turn transformer with a turn ratio of 1:100. The amount of compensation as a

percentage of line reactance can be varied by adjusting the amplitude of the injected voltage between -10V and 10V. The capacitance of the DC link capacitor is 500μF. The capacitor is rated at 1.5kV however expected dc voltage will be less than the rating.

Normally, maximum allowed voltage drop is between 5% and 10% [89]. Fig.3.15 shows the voltage profile through the line without any compensation. The voltages at 4 locations through the line (at distances of 0.2km, 2km, 10km and 20km from the substation) are shown in Fig.3.16. This figure shows the voltage profile before and after compensation by DSSC. Before compensation voltage drop is 700V and this more than 5% acceptable voltage drop. With compensation voltage drop along the line is reduced from about 700V to 400V. The amount of compensation for each line segment is not the same and varies according to the distance from the source which supplying the load. Fig. 3.16 shows that the amount of improvement at 1st point of the line is negligible but this value in the 2nd point is sensible. Voltage improvement becomes almost 500 volts at the end of feeder. This is showing that when the length of feeder increases the need for compensation will increase. In the same way the compensation of line by DSSC is less at the beginning of the line and it is more at the end of the line. The line voltage profile is plotted with and without compensation in Fig.3.17. The figure shows that the amount of required compensation by increasing the length of the feeder increases. Then the DSSC can provide an excellent balance between the demand and production of the reactive power through the line.

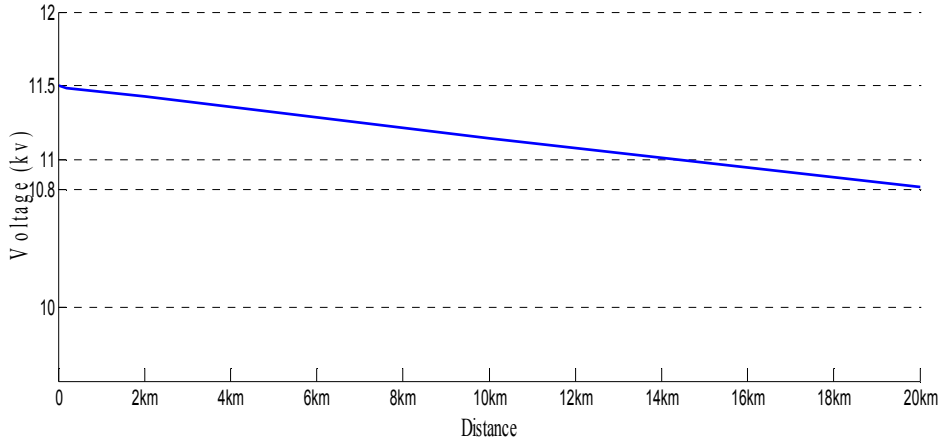


Fig.3.11: Feeder voltage profile before compensation

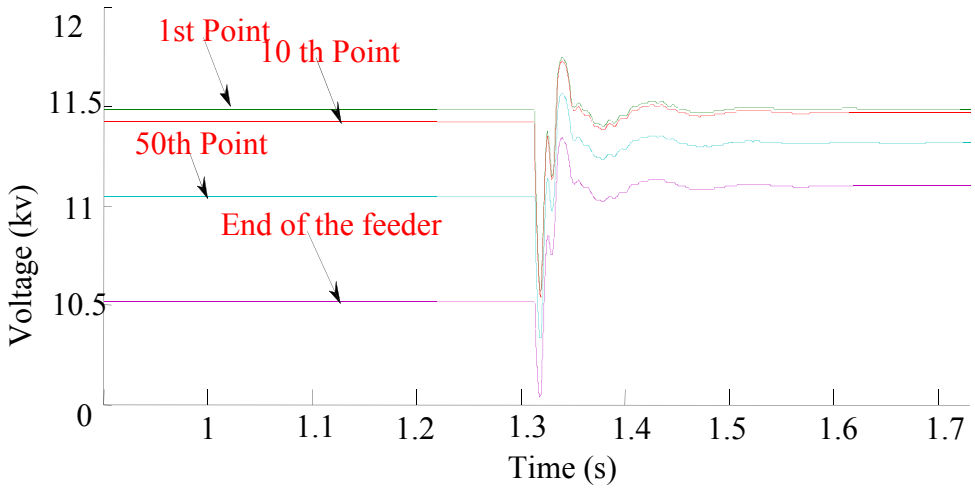


Fig.3.12: Voltages at different distances along the feeder

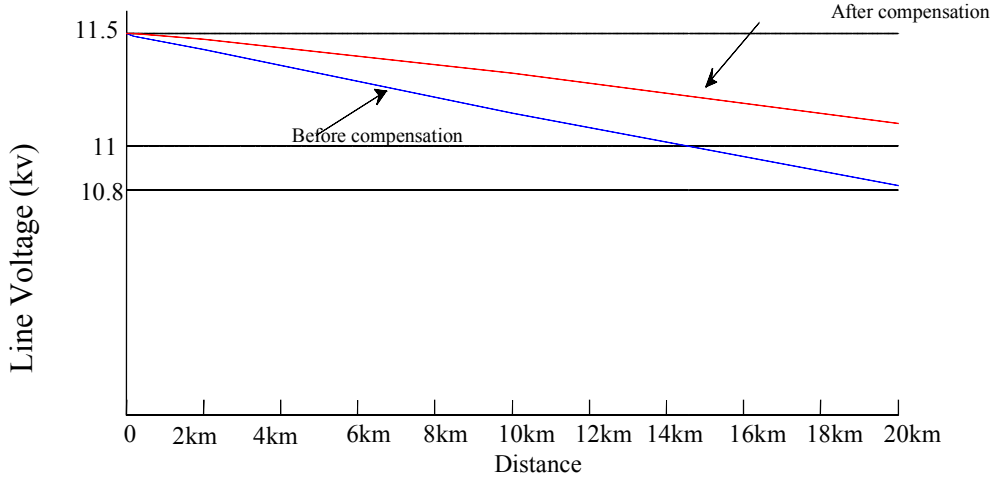


Fig.3.13: Feeder voltage profile after compensation

3.4 Summary

DSSC devices can be used in the distribution networks to enhance electrical parameters of the system. In distribution networks resistance of the lines are higher and in some occasions even the X/R ratio can be less than one. Operation of DSSC device is not affected by the X/R ratio and the device can operate without any malfunction. However, with X/R ratio of 1 or less capacitive compensation is not increasing the ATC. It has been note that in such cases inductive injection can increase power transfer capability of the line.

The required numbers of the devices in each system can be calculated based on the demanded amount of compensation, line current and compensation capability of each DSSC device. DSSC device can be designed to inject voltage with different amplitudes.

Using DSSC within the electrical power distribution networks can provide more flexible load flow control capabilities to the network operators. It has been demonstrated that impedance of the compensated line is decreased (or increased) using DSSC in order to divert current to the desired line in a parallel lines.

DSSC also has been employed to enhance the voltage profile through the feeder length. The voltage profile improvement is achieved by injection of capacitive reactive power through the line to compensate inductivity of the line. The injection is compensating the reactive power consumption of the line. This application of DSSC has been simulated using the PSCAD/EMTDC simulation. The simulation results show that the voltage drop caused by the line reactance is compensated by DSSC. The voltage profile before and after application of DSSC in a 20km, 11kV distribution feeder has been compared.

4 New Control Strategy

In this chapter, in order to overcome drawbacks with existing control strategies a new closed-loop control strategy based on the exchange of instantaneous power is proposed. The control guarantees an orthogonal injection of voltage with respect to the line current. It also optimizes the active power absorption by the DSSC device and holds the DC voltage at desired value at the same time. The controller is applied in order to enhance the performance of DSSC which is employed as a FACTS device on an 11kV distribution line. The proposed control is studied in the novel application of DSSC in the distribution networks. The study starts with a DSSC connected to 11kV distribution system. The proposed method is extensively investigated with simulation in PSCAD for different working scenarios.

4.1 New approach of controlling DSSC with single phase control

This section presents a new control approach which is used to force the phase angle between injected voltage and line current to be 90 degree. Based on single phase control the proposed control has capability to control the injected series voltage in each phase of a three phase system separately. The control strategy is based on the minimisation of the exchanging instantaneous power and holding the voltage of the DC link at a desired value. For this reason it can be divided into two parts as follows.

The first part is the regulation of capacitor voltage and holding the voltage at a desired value. To do so, the magnitude of DC voltage across the capacitor is monitored continuously and then compared to a constant reference value (control block diagram is shown in Fig.4.1). The comparison generates an error signal which is carrying information about the status of the DC link voltage and it is fed into a PI controller. The error is then smoothed out by a PI controller before being added on top of the other signals coming from the second part of the controller and the PLL. PLL is locked to the system and provides up to date status of the *wt* of the power system.

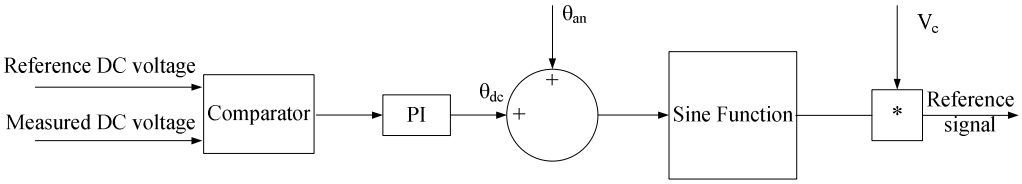


Fig.4.1: Control block diagram of DC voltage regulating

In Fig.4.1, θ_{dc} represents the need for adjustment of the dc voltage. When the DC voltage is equal to the desired voltage this angle becomes zero. Also in this figure the θ_{an} is carrying information about the angle of injection and *wt* from the PLL. Furthermore in this control block diagram K_c determines the percentage of the compensation which must be provided by the DSSC. This percentage can be calculated based on the line current and amount of the capacitance which must be injected through the line as follow:

$$K_c = \frac{I_l}{jwc} \quad (4.1)$$

where *w* is the angular frequency of the power system and I_l is the line current. C is the capacitance which needs to be inserted into the system and calculated from capacitive reactance X_{inj}

$$X_C = K_c X_L \quad (4.2)$$

where K_c is the percentage of compensation and X_L the reactance of the transmission or distribution line. Because the DSSC has the capability to inject inductive reactance through the line as well, therefore the K_{cl} for inductive injection is obtained using L.

$$K_{cl} = I_l jwL \quad (4.3)$$

where, L is the inductance required to be injected.

The second part of the controller, which is the most important and the novel part of the controller proposed, provides a proper angle of injection. This part of controller focuses on the adjustment of phase angle between the injected voltage and the line current. Ideally the phase angle should be 90°. However, due to ohmic losses, this is not achievable and it will be different from 90°.

The solution, which has been employed in the literature, is that to divert the injection phase angle to some extent from 90° in order to compensate the losses inside the DSSC device. This is because by diverting the injected voltage from the 90° DSSC will be able to exchange the active power. To compensate the losses, absorption of active power is required and it can be achieved by introducing injection angle of less than 90 degree. Although the amount of diversion from the 90° is an important parameter, surprisingly it has not received much attention in the literature review. It must be noted that if the absorbed active power becomes more than the power losses then the DC voltage in the DC link will get increased. This will change the amount of compensation and may cause instability in the system. Similarly if the amount of absorbed active power is less than that required by losses then the DC voltage will collapse, i.e. the series compensator device will lose the stability.

However, in the new control strategy, which is based on the instantaneous power exchange, the required amount of active power is exactly absorbed. This can be achieved by firstly forcing the phase angle between the injected voltage and line current to be 90°, then introducing a slightly different phase angle in order to compensate the losses. This phase angle obviously needs to be dynamically updated by the controller. To do so, line current and injected voltage wave form are being multiplied to each other instantaneously as follows:

$$p(t) = I(t)_{Line} * V(t)_{Inj} \quad (4.4)$$

where p(t) is the instantaneous exchanged power between the DSSC and power system. In equation (5.4) $V(t)_{Inj}$ and $I(t)_{Line}$ are the injected voltage and line current respectively and can be written as follows:

$$I(t)_{Line} = \mathrm{I_l}\cos(wt + \theta_1) \quad (4.5)$$

$$V(t)_{Inj} = \mathrm{V_{inj}}\cos(wt + \theta_2) \quad (4.6)$$

where θ_1 and θ_2 are the initial phase angle of the line current and voltage. I_l and V_{inj} are the maximum amplitude of line current and injected voltage. By substituting the equations (4.5) and (4.6) to the equation (4.4) the p(t) can be rewritten as follow:

$$p(t) = \frac{1}{2} * A * (\cos(2wt + \theta_1 + \theta_2) + \cos(\theta_1 - \theta_2)) \quad (4.7)$$

where A is the maximum amplitude of the p(t) and defined in equation (4.8).

$$A = V_{inj} * I_l \quad (4.8)$$

Equation (4.7) can be decomposed into two parts: the oscillatory and the DC components. The oscillatory part, $p(t)_{ac}$ as defined by equation (4.9), has 2nd order frequency and must be filtered out.

$$p(t)_{ac} = \frac{1}{2} * \mathrm{A} * \cos(2wt + \theta_1 + \theta_2) \quad (4.9)$$

The remaining part, $p(t)_{dc}$ as defined by equation(4.10) is DC signal. It carries out information regarding phase angle between the line current and the injected voltage.

$$p(t)_{dc} = \frac{1}{2} * \mathrm{A} * \cos(\theta_1 - \theta_2) \quad (4.10)$$

Ideally, if the line current and injected voltage become orthogonal then the $(\theta_1 - \theta_2)$ will be 90°. Consequently the $p(t)_{dc}$ will be zero. However a non-zero $p(t)_{dc}$ means that the injected voltage is not orthogonal to the line current. Practically, this can happen because the voltage in the DC link is diverted from the desired value or due to compensation of internal losses of DSSC. Diversion of DC voltage from the desired value is temporary and it will reach to desired value by change of injection angle. Thereafter, an orthogonal injected voltage is expected. However, in order to compensate

internal losses of DSSC the injected voltage is slightly diverted from 90°. Then it will introduce an error in $p(t)_{dc}$ which will pass through the low pass filter and after that will be smoothed out by a controller. In order to avoid accumulating the error a P controller has been used. PI controller accumulates the steady state error and should be avoided in this application.

The output of controller is called θ_{err} and includes the error of diversion of phase angle between the injected voltage and line current from 90°. The diversion is generated in corresponding to a temporary and permanent error. The temporary one disappears after DC voltage reaches to desire value however the permanent error will exist to compensate internal losses. The control block diagram of the aforementioned procedure is shown in Fig.4.2.

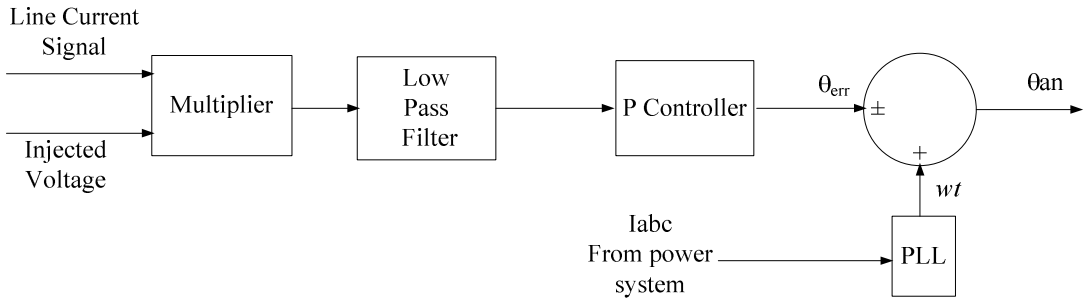


Fig.4.2: Injection phase angle regulation control block diagram

The new proposed controller in this study benefits from the DC voltage regulation and orthogonal voltage injection independently. This will provide an opportunity to obtain different level of DC voltage across the DC link while the injected voltage phase angle is still guaranteed by the rest of the controller. Block diagram of whole controller shown in Fig.4.3 the angles from both sides (from DC voltage regulator and injection angle provider) will be added on top of each other. The resultant signal, i.e. output of the controller (reference signal), will be fed into PWM generator in order to generate the switching pattern. The signal generated by the converter is injected through the power line and fed back to the controller at the same time.

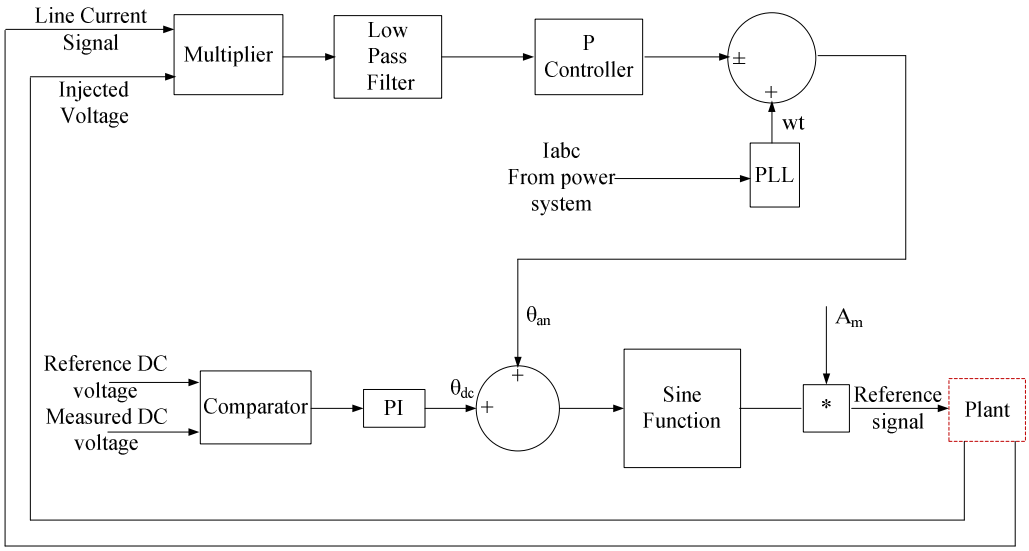


Fig.4.3: Block diagram of the proposed controller

In order to prove the concept, the proposed strategy is simulated using PSCAD/EMTDC software. Simulation of application of the proposed control system with a DSSC device will follow later in this chapter.

Injected voltage and line current are multiplied to each other and the result is shown in Fig.4.4. The results are satisfying equation (4.7), hence validating the proposed control strategy. In Fig.4.4 the first waveform (*p(t)*ACDC) represents the equation (4.7) and the second one (*p(t)*DC) shows the DC part of the equation. This is expressed in equation (4.10) and shown with p(t)DC in Fig.4.4.

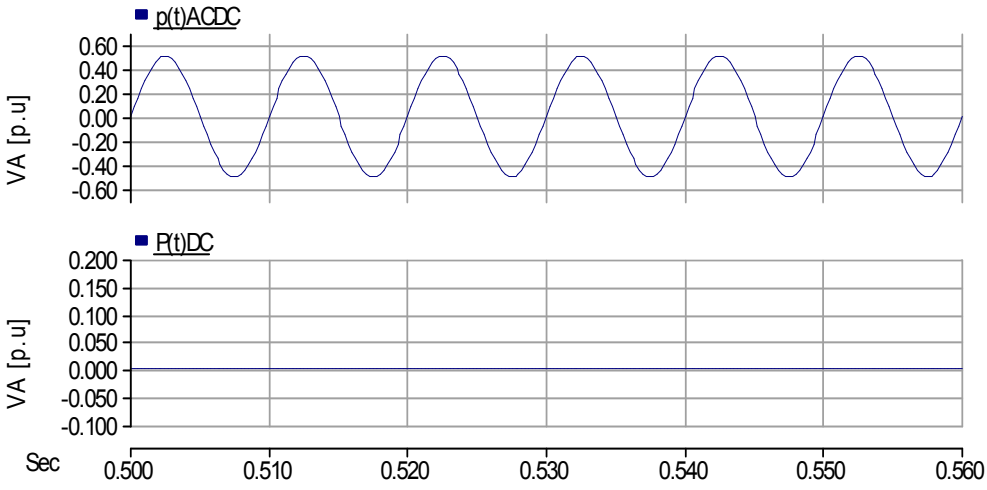


Fig.4.4: Multiplication of “line current signal” and “injected voltage”

In Fig.4.4 the DC signal is zero which is representing 90 degree phase angle between the two signals and it is a prove for orthogonally of multiplied signals. Also in this figure the AC signal (representing the instantaneous exchanged power) shows that, in the presence of 90 degree phase difference between the multiplied signals, there will be no active power absorption. This is because in this signal the positive half cycle is exactly equal to the negative half cycle. Consequently the absorbed active power at the end of one period is zero.

With the intention of investigating the dependency of active power absorption on the phase angle of injected voltage the voltage has been applied in different phase angle and the results are shown in Fig.4.5. In this figure at first there is only 90 degree phase shift between the injected voltage and line current. Therefore it can be easily observed from the figure the DC signal is zero and the AC signal completely symmetrical (the positive and negative amplitude of the signal are same). In the next step a 10 degree difference has been introduced on top of the previous phase angle. As a result, the DC signal has been moved from zero to -0.85. The AC signal is not symmetrical anymore and there is negative bias in the signal. Finally, with introduction of -10 degree phase difference the DC signal moves to 0.85 and the AC signal has been shifted up. Phase shift of ± 10º is added just to show the dependency of active power absorption to injected angle.

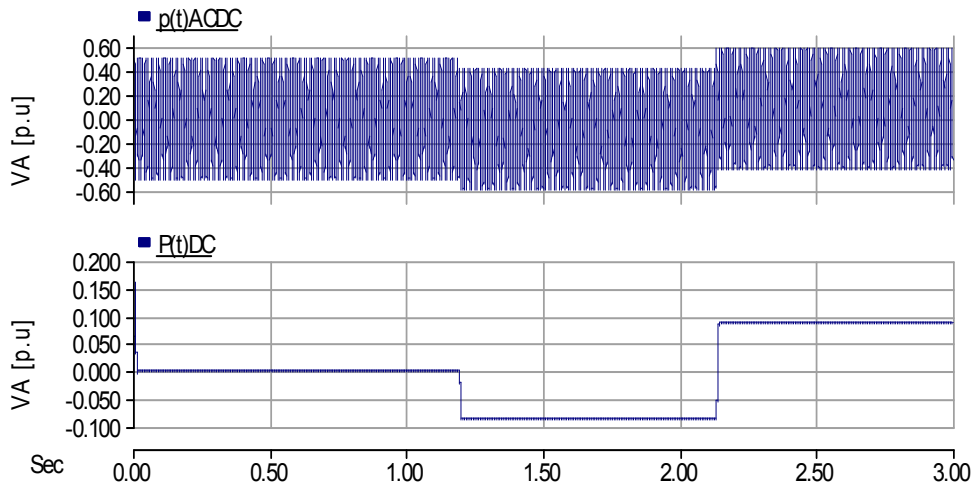


Fig.4.5: Dependency of active power absorption on the phase angle of injected voltage

4.1.1 Advantages of the proposed controller

The proposed controller is not using the dq conversion, which is used widely in the literature review. As a result it does not have the associated problems as discussed earlier in chapter 2. In addition to that the amount of compensation becomes independent from the line current by using this controller as well. For example, Fig.2.40 and Fig.2.41 in chapter 2 show control block diagram (typically used in the literature) where the amount of compensation is being dynamically changed by changing the line current. In contrast to that, in proposed control system shown in Fig.4.3 the amount compensation is determined by A_m which is calculated based on the required percentage of compensation. As another example the amount of compensation by the fixed series capacitors totally depends on the line current. Consequently the compensation will increase with an increase of the current and vice versa. However in the proposed controller the compensation achieved by the DSSC is measured by means of p(t) and compared to the demanded value.

A further advantage of control system presented in the above figure is its immunity against possible harmonics in the power system. It means that as long as the PLL is functioning properly and controller has not lost the synchronism the harmonics will not penetrate into the control system. This is because with considering some harmonics (for example 5th) in the power system the equation (5.5) can be rewritten as follow:

$$I(t)_{Line} = I_l[\cos(wt + \theta_1) + \cos(5wt + \theta_3)] \quad (4.11)$$

By substituting equation (5.11) into (5.4), finally the equation (5.7) becomes

$$p(t) = \frac{1}{2} * A * (\cos(2wt + \theta_1 + \theta_2) + \cos(\theta_1 - \theta_2) + \cos(6wt + \theta_1 + \theta_3) + \cos(5wt + \theta_3 - \theta_1))) \quad (4.12)$$

Comparing equations (4.7) and (4.12) shows that the dc part, $(\cos(\theta_1 - \theta_2))$, remains unchanged in presence of the harmonics. It is only the AC part of the equation (4.7) that will be changed. However the AC part will be filtered out and it cannot contribute toward the θ_{an} signal in the control block diagram shown in Fig.4.3.

Furthermore an additional advantage of the proposed control is that it takes feedback directly from the output voltage of the DSSC and tries to minimise the θ_{an} .This aspect makes the control system to be a closed loop controller rather than being an open loop controller. This provides the self-adjusting capability, thus stability, for the control.

In the polluted power systems along with the fundamental current there will be other harmonics as well. It has been shown by equations (4.11) and (4.12) that the harmonics

cannot penetrate in the control system. The simulation results validating the proper operation of the controller in presence of the harmonics are represented later on in this chapter.

4.2 Modelling of DSSC

In order to simulate the operation of DSSC using the proposed control strategy the DSSC device is modeled as shown in Fig.4.6. It comprises of a single-phase H-bridge IGBT converter, a dc capacitor, an AC filter and a single turn transformer which is connected in series with the power line. The current flowing inside the DSSC is proportional to the line current (depends on the turn ratio of STT) and the line current is governed by electrical network. The equivalent model of the power system including STT (shown inside dashed red rectangle) seen by DSSC is represented as a current source which is shown in red in the following figure.

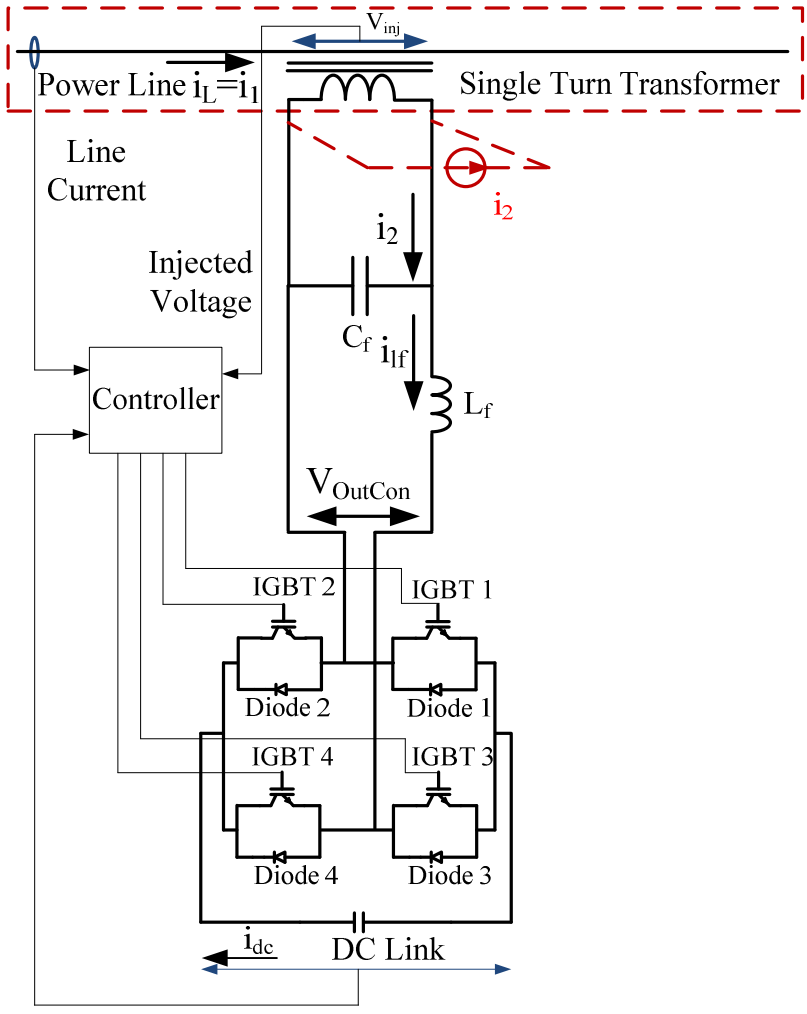


Fig.4.6: DSSC in connection with the power line

The functionality of H-bridge converter includes two different modes of operation. In mode 1 IGBT's 1 and 4 are conducting and IGBT's 2 and 3 are off. In mode 2 IGBT's 1 and 4 are switched off and IGBT's 2 and 3 are conducting. Timing diagram of switching of IGBT's is shown in Fig.4.7. In this figure T_s is equal to $1/f_s$ and f_s is the switching frequency also d represents the duty cycle of switching.

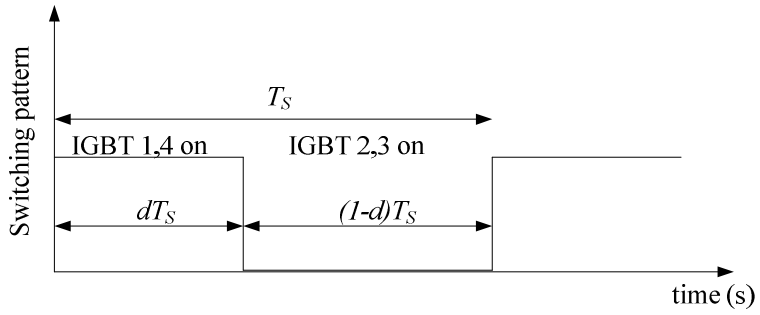


Fig.4.7: Timing diagram of switching pulses of IGBT's

4.2.1 Operation mode 1

The equivalent model of DSSC for the operation mode of 1 is shown in Fig.4.8.

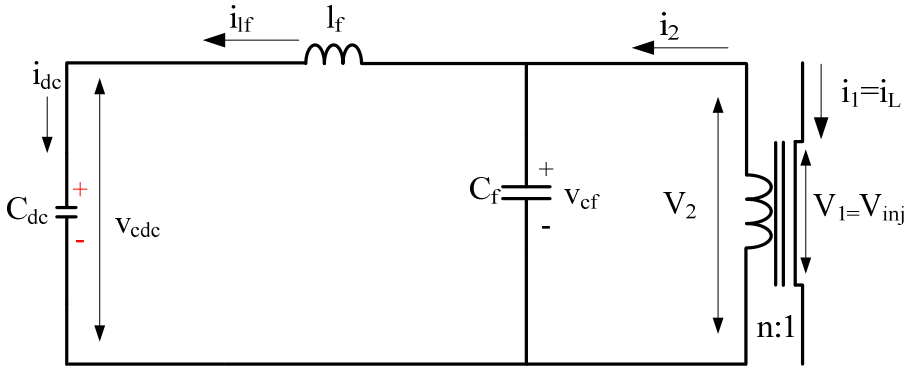


Fig.4.8: Equivalent circuit in mode 1

In the above equivalent circuit C_{dc} is the dc capacitor and l_f and C_f are the inductance and capacitance of the LC filter. V_2 and V_1 (injected voltage) are representing the secondary and primary side voltages of the STT respectively and n is the turn ratio of transformer. Transfer function of the system can be obtained by writing KVL and KCL equations in the equivalent circuit shown in the Fig.4.8. To do so, the following equations can be written in the S (Laplace) domain in mode 1:

$$i_{dc} = i_{lf} \qquad (4.13)$$

$$SC_{dc}V_{cdc} = i_{dc} \quad (4.14)$$

where i_{lf} and i_{dc} are the current passing through the l_f and C_{dc} respectively. In (4.14) v_{cdc} is the voltage across the C_{dc} capacitor.

Current through the inductance, i_{lf}, is obtained in the (4.15) by writing KCL equation in common connection point of STT, l_f and C_f .

$$i_{lf} = i_2 \frac{l_f C_{dc} S^2}{1+(l_f C_f+2C_{dc}l_f)S^2+(l_f^2 C_f C_{dc}+l_f^2 C_{dc}^2)S^4} \quad (4.15)$$

or

$$i_{lf} = ni_1 \frac{l_f C_{dc} S^2}{1 + (l_f C_f + 2C_{dc}l_f)S^2 + (l_f^2 C_f C_{dc} + l_f^2 C_{dc}^2)S^4}$$

where i_1 and i_2 are the primary and secondary current of the SST respectively.

4.2.2 Operation mode 2

In mode 2 the polarity of voltage at the output of the converter will change as shown in Fig.4.9.

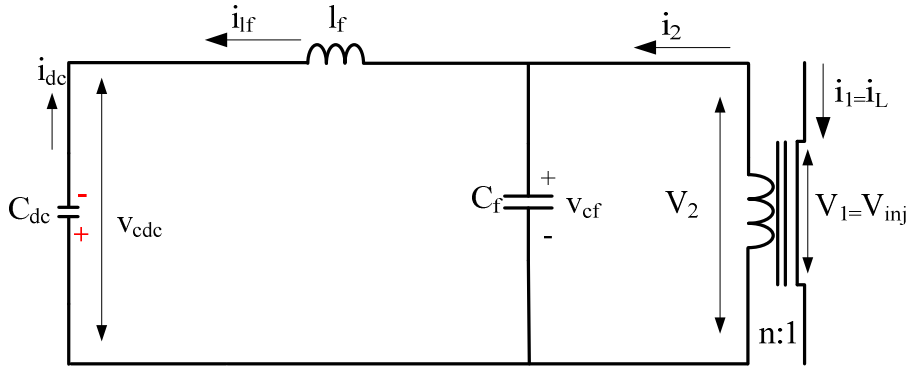


Fig.4.9: Equivalent circuit in mode 2

Voltage across the DC capacitor in mode 2 still can be obtained from (4.14) in the Laplace domain. However in this mode direction of current passing through the C_{dc} is changed and it is presented in (4.16)

$$i_{dc} = -i_{lf} \quad (4.16)$$

4.2.3 Average of current through DC capacitor

During a period, T_s, we shall assume that DSSC circuit operates in mode 1 and mode 2 for a time period of dT_s and $T_s(1\text{-}d)$ respectively, where d, as shown in Fig.4.7, is the duty cycle for switching between mode 1 and mode 2. Considering the fact that the

switching frequency, f_s, is fast enough to have negligible change in absolute value of the i_{lf} during mode 1 and mode 2 the average value of i_{dc} in one period is obtained in (4.17).

$$\overline{i_{dc}} = \frac{dT_s i_{lf} + (1-d)T_s(-i_{lf})}{T_s} = (2d-1)i_{lf} \quad (4.17)$$

Voltage across the DC capacitor is recalculated in (4.18) by substituting the average value of i_{dc} in (4.14).

$$V_{cdc} = \frac{(2d-1)i_{lf}}{sC_{dc}} \quad (4.18)$$

By replacing equivalent of i_{lf} from (4.15) in (4.18) v_{cdc} is recalculated in (4.19).

$$v_{cdc} = ni_1 \frac{(2d-1)l_f S}{1+(l_f C_f + 2C_{dc}l_f)S^2 + (l_f^2 C_f C_{dc} + l_f^2 C_{dc}^2)S^4} \quad (4.19)$$

in (4.19), (*2d-1*) is the control term and it can be represented by *u*. Having considered this in (4.19) transfer function of v_{cdc} to *u* is obtained in (4.20).

$$G = \frac{V_{cdc}}{u} = ni_1 \frac{l_f S}{1+(l_f C_f + 2C_{dc}l_f)S^2 + (l_f^2 C_f C_{dc} + l_f^2 C_{dc}^2)S^4} \quad (4.20)$$

4.3 Controller design

Employed control strategy is based on the regulating the DC voltage in the desired value in order to minimize the active power exchange with the AC system. In addition to the DC voltage regulation the error of multiplication of injected voltage (v_1) and line current (i_1) after passing through a low pass filter is being added to the feedback loop in order to fine tune the injection angle. Block diagram of control strategy is shown in Fig.4.10.

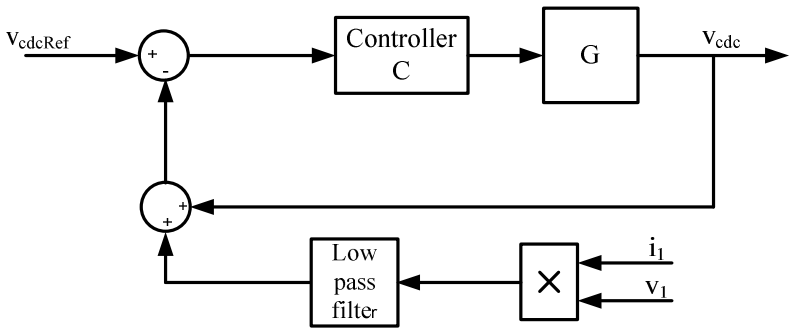


Fig.4.10: Block diagram of control strategy

In the block diagram shown in Fig.4.10 v_{cdcRef} and v_{cdc} are representing the reference DC voltage and the voltage across the DC capacitor respectively. Transfer function of DSSC device is shown by *G* in the block diagram and it can be obtained, in the Laplace

domain, by replacing the values of capacitors and inductance from the system design parameters (tabulated in Table 4.1) in (4.21).

Component	Symbol	Value
DC capacitor	c_{dc}	500 uF
Filter capacitor	c_f	500 uF
Filter inductor	l_f	80 uH

Table 4.1: System parameters

$$G = \frac{V_{cdc}}{u} = \frac{1.6e^{-7}S}{3.2e^{-15}S^4+1.2e^{-7}S^2+1} \quad (4.21)$$

Root Locus diagram of the transfer function, *G* (transfer function of open loop system), is presented in Fig.4.11. The right hand side of the diagram (positive real axis) is an indication of unstable system.

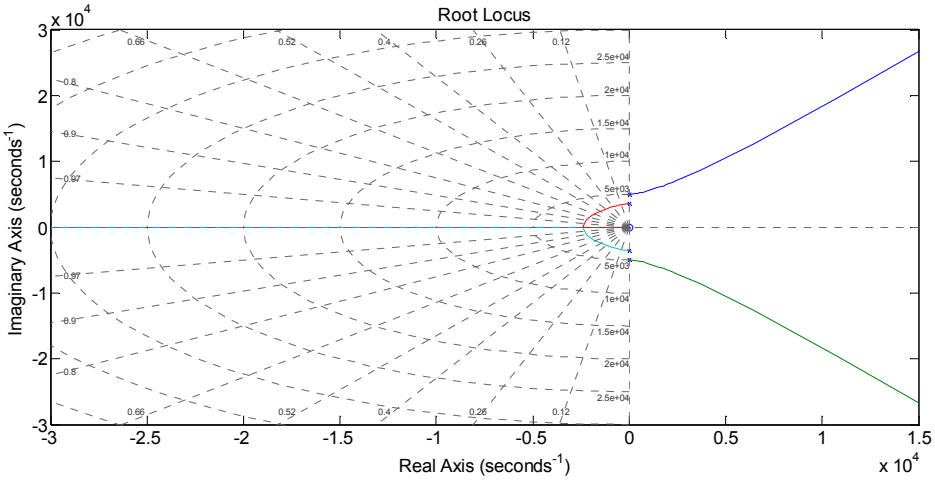


Fig.4.11: Root Locus diagram of the transfer function G

For closed loop system locations of poles and zeroes are shown in Fig.4.12. This figure shows that, there are two poles in the positive real axis which makes system unstable.

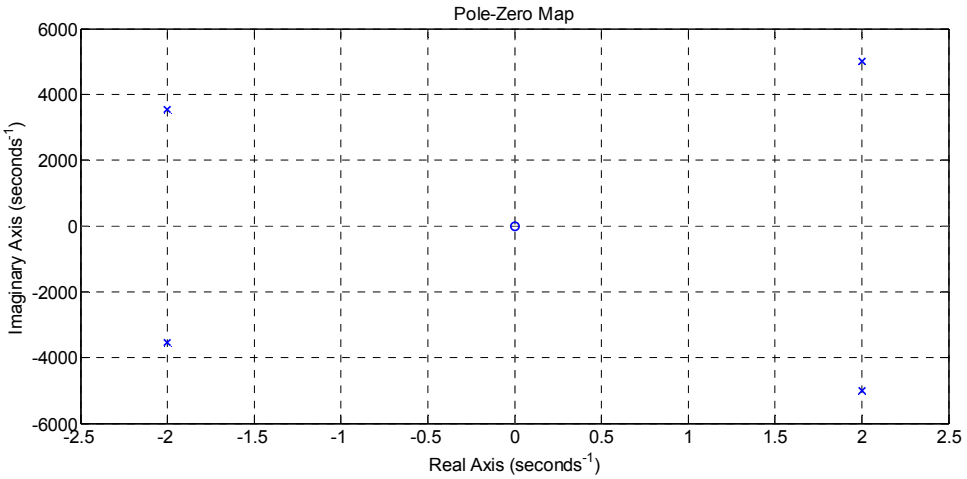


Fig.4.12: Poles/zeroes map for closed loop system

In order to make closed loop system to be stable, a controller as shown by *C* in Fig.4.10 is needed. The controller is obtained using MATLAB in a way to meet the criteria which are tabulated in Table 4.1.

Parameters	Values
Rise time	To reach 95% in 0.05 Sec
Settling time	99% settle in 0.5 Sec
Max overshoot	5%
Steady state error	0
Gain margin	Greater than 10 dB
Phase margin	Greater than 60°

Table 4.2: Criteria in zero/pole placement

In controller design Root Locus has been used. This is a graphical design tool allows moving the zero/pole to achieve the design criteria.

For start in the controller design only gain has been employed. With the initial gain value controller has left a steady state error. By increasing the gain steady state error was improved but still it is not fully converged to zero. Further increment of gain introduces oscillations in the step response.

In order to eliminate steady state error an integrator has been added to the controller and a PI controller has been employed. Adding integrator makes system response to become slow and increment of the gain, however this can introduce overshoot and oscillation in

the step response. It has been noticed that there is a relationship between oscillation in the step response and poor phase margin. In order to eliminate the oscillations and improve phase margin, a lead compensator added to the controller. It means that the controller C shown in Fig. 4.10 includes a PI controller and a lead compensator. The aforementioned explanation describes the employed approach in the controller design.

In the design process of the controller for start, pole of PI controller is located in "0" (which is obvious) and MATLAB is used to find the approximate location (first location) of zero. Root Locus diagram of open loop transfer function after insertion of zero/pole is plotted in Fig.4.13. Gain of controller has been chosen from the Root Locus diagram shown in Fig.4.13 in order to respect required criteria of design.

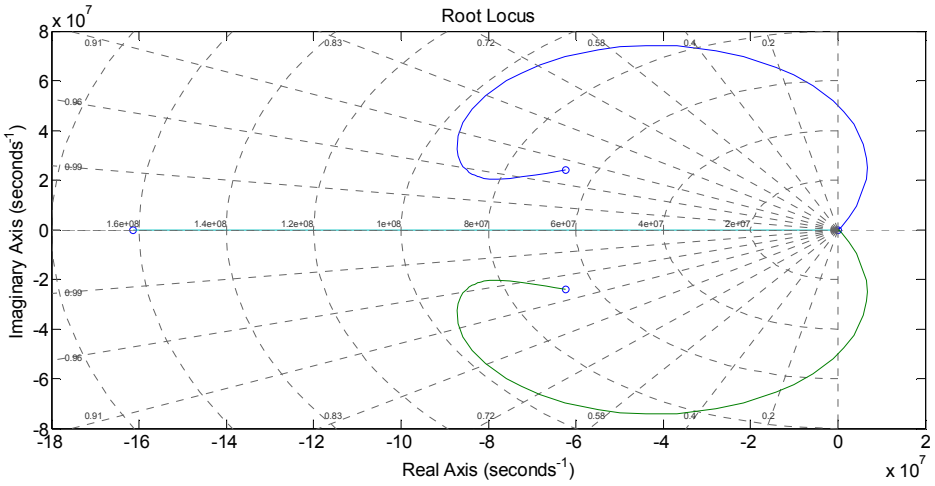


Fig.4.13: Root Locus diagram of the open loop system including controller C

For example, for overshoot of 76.3% and damping factor of 0.0856 the corresponded gain of 0.0163 can be obtained from Fig.4.13. By including the selected gain in the controller *C* the step response of the closed loop system is plotted in Fig.4.14. It can be observed that peak of overshoot reaches to 1.58 and it oscillates for few cycles before settling down and reaching steady state.

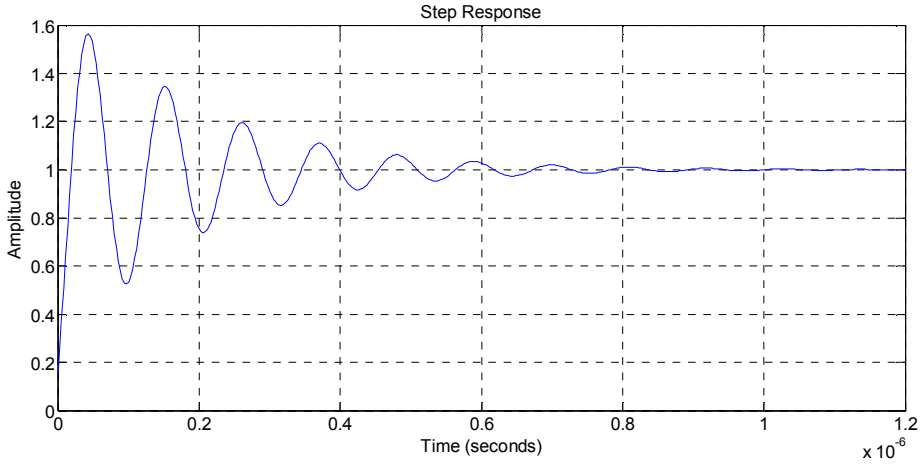


Fig.4.14: Step response of closed loop system when gain of controller is 0.0163

The step response of the system can be improved by increasing the damping factor and reducing the percentage of overshoot. In order to reduce the peak value and suppress the oscillations overshoot of 0.018% and damping factor of 0.93 has been targeted. The corresponding gain of 2.85 is obtained from Fig.4.14. In the same time in order to meet the required gain margin and phase margin of design criteria the lead compensator has been applied. By moving the zero/pole of the lead compensator using the MATLAB locations of zero/pole were found in a way to achieve phase margin of 66° and gain margin of 72 db. Controller C with the designed gain value and zeros/Poles are represented in (4.22).

$$C = \overbrace{2.85}^{Gain} * \frac{\overbrace{(s+3e3)}^{PI\ Controller}}{s} * \frac{\overbrace{(s+9e3)}^{Lead\ compensator}}{(s+12e3)} \qquad (4.22)$$

Bode diagram of system with obtained phase margin and gain margin is plotted in Fig.4.15. The positive values of obtained phase margin and gain margin are showing system stability.

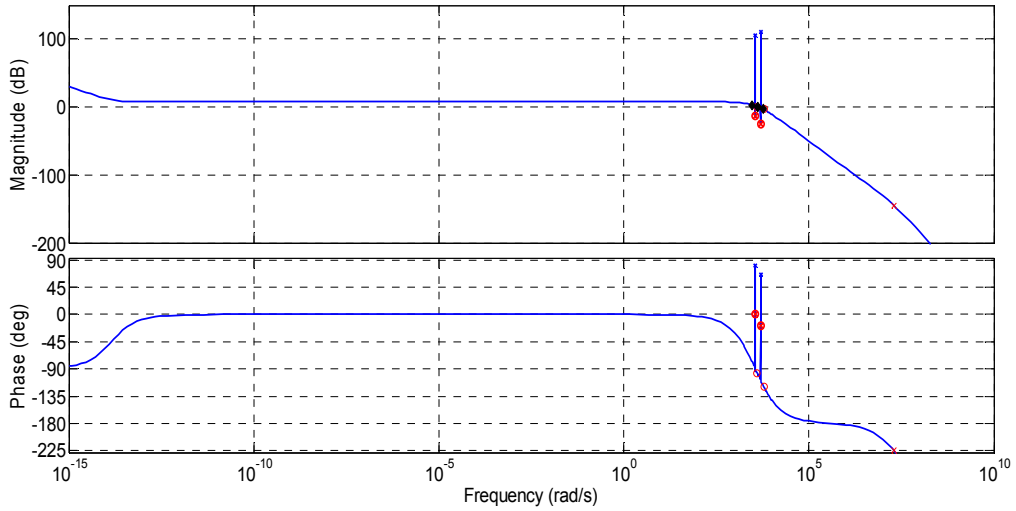


Fig.4.15: Bode diagram of system

By applying the newly obtained gain the lead compensator the step response of closed loop system has been improved as shown in Fig.4.16.

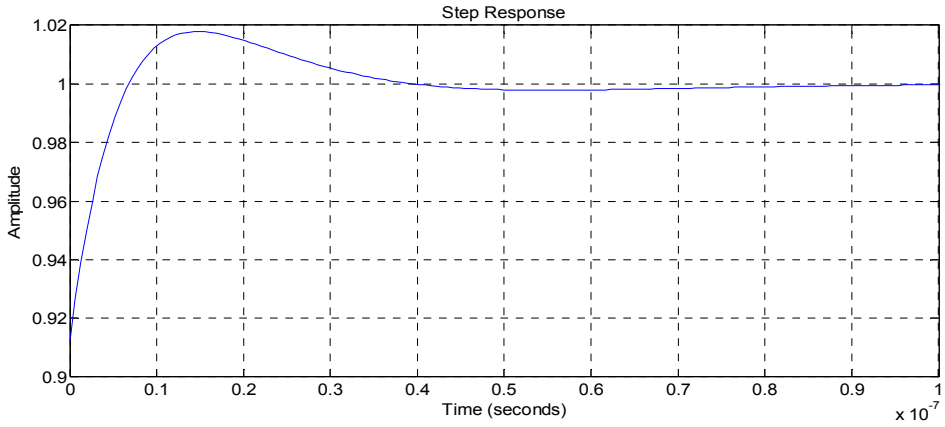


Fig.4.16: Step response of closed loop system meeting overshoot of 0.018% and damping factor of 0.93

In order to validate the designed controller DC voltage across the DC capacitor must be checked. The designed controller is employed in the simulation of DSSC to control the operation of system and Fig.4.17 shows the voltage across the DC capacitor. It can be observed that the voltage is being held in the desired value.

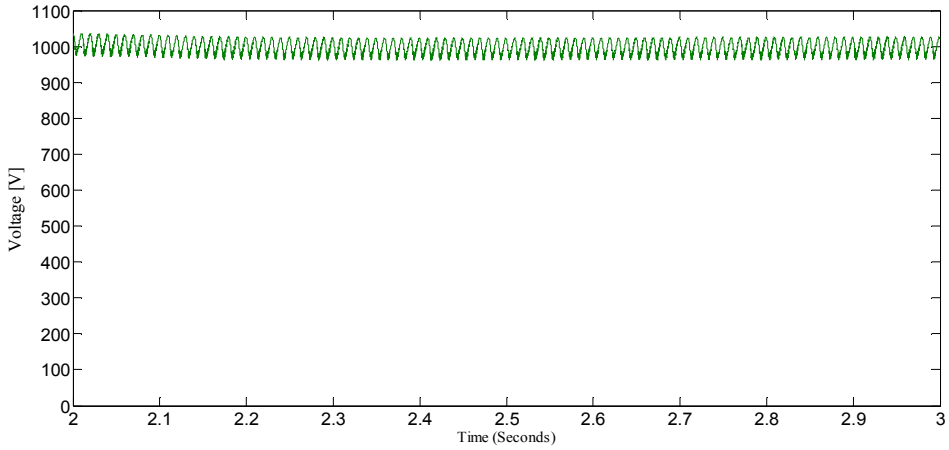


Fig.4.17: Voltage across the DC capacitor

4.4 Sensitivity analysis of designed controller

Effect of change of system parameters on the performance of the designed controller has been investigated. Change of system parameters includes change in the capacitance of DC capacitor, AC capacitor (filter capacitor) and inductance of filter. These parameters can put stability of system at risk by relocating the poles and zeros. Moreover, the step response of the system and the related overshoot can be affected by these changes.

4.4.1 Effects of change in the system parameters

System parameters can be changed. For example, capacitance of a capacitor reduces over time [90] and the reduction can affect the stability and step response of the system. With the intention of investigating the issue, c_{dc} is reduced by 10%. Resulted step response and map poles and zeros of closed loop system are presented in Fig.4.18 and Fig.4.19 respectively. It can be observed that still system is stable and step response is more or less remains same.

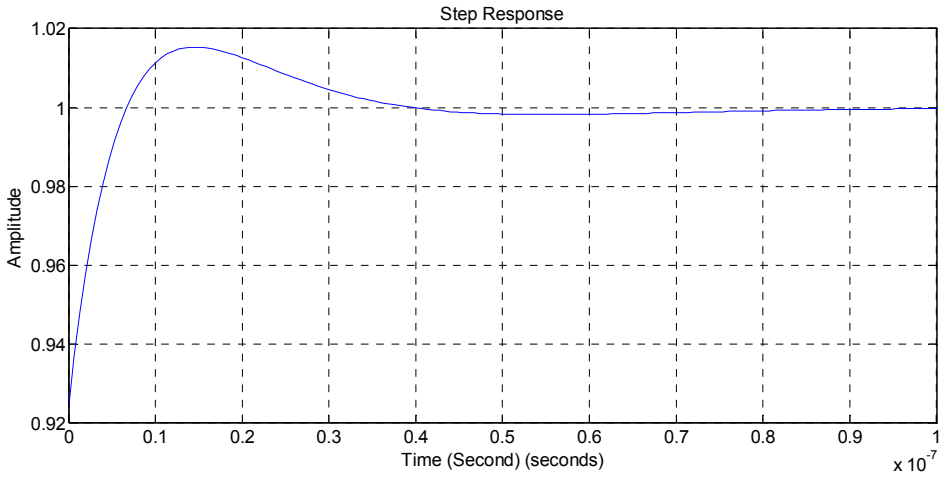


Fig.4.18: Step response of system after applying 10% reduction in the capacitance of cdc

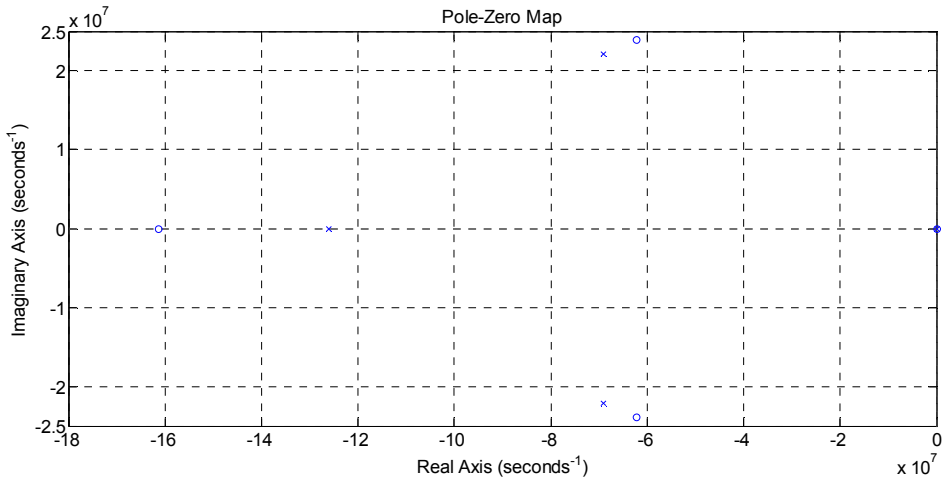


Fig.4.19: Pole/zero map for a closed loop system after applying 10% reduction in the capacitance of cdc

It must be noted that applying 10% reduction in the capacitance of AC capacitor or inductance of inductor within the LC filter provides same results as shown in Fig.4.18 and Fig.4.19.

It has been validated by the simulation that with 10% change in the system parameters still system is stable. This is shown in Fig.4.20 by reducing capacitance of c_{dc} by 10% at 0.76s. Changing of capacitance of the c_{dc} is followed by a transient overvoltage and thereafter the DC voltage comes back the pre event value.

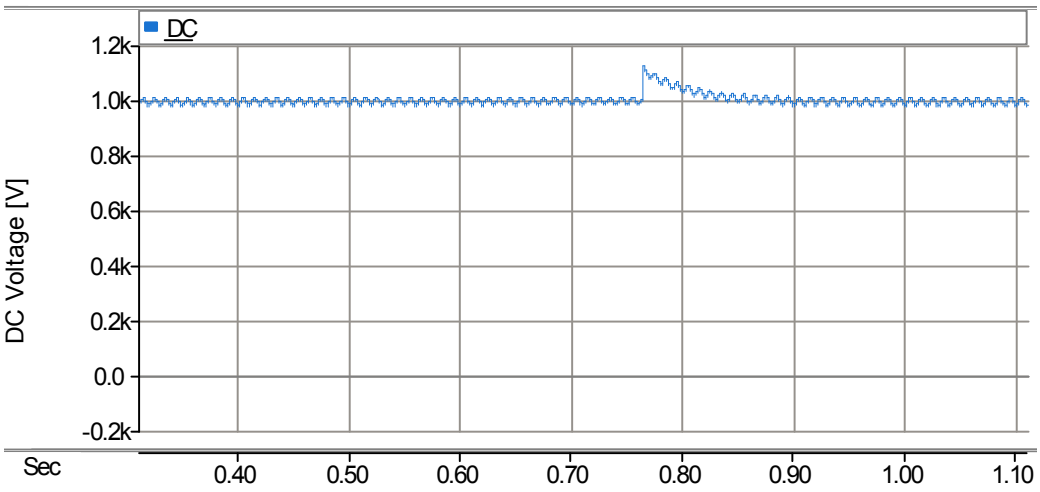


Fig.4.20: Effect of changing capacitance of cdc

However, further reduction in the parameters can lead to instability. For example, with 50% reduction in the c_{dc}, two poles appear in the right hand side of pole/zero map of closed loop system and it becomes instable. Fig.4.21 and Fig.4.22 show the step response of system and the pole/zero map after having 50% reduction of capacitance of c_{dc}.

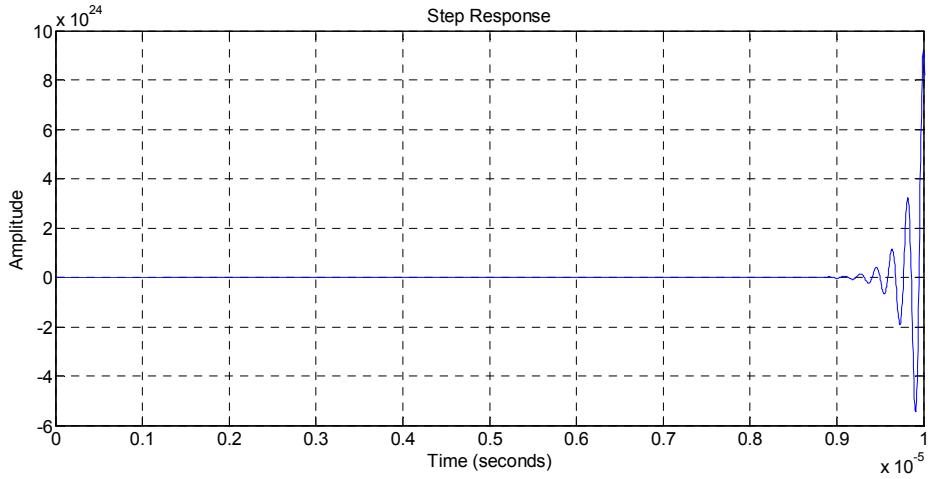


Fig.4.21: Step response of instable system after applying 50% reduction in capacitance of cdc

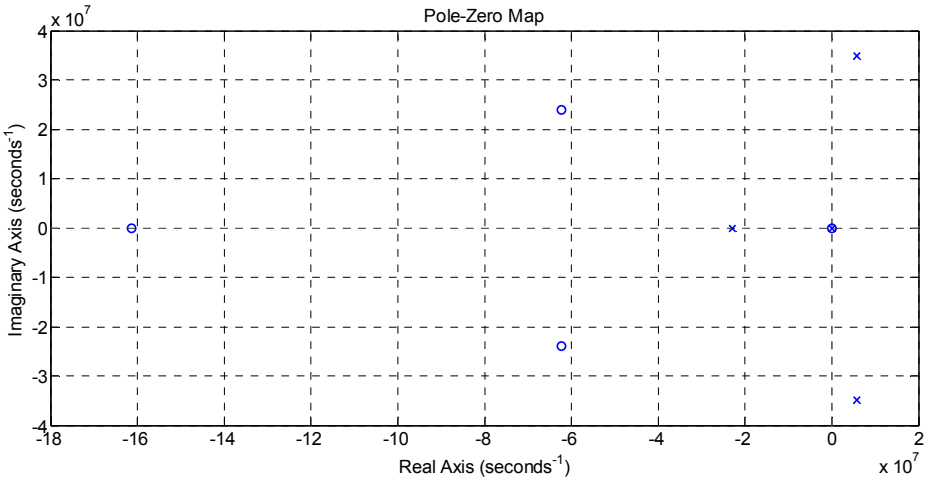


Fig.4.22: Pole/zero map of closed loop system after applying 50% reduction in capacitance of cdc

Simulation results show that after reducing the capacitance of c_{dc} by 50% system becomes unstable and DC voltage shown in Fig.4.23 becomes unstable.

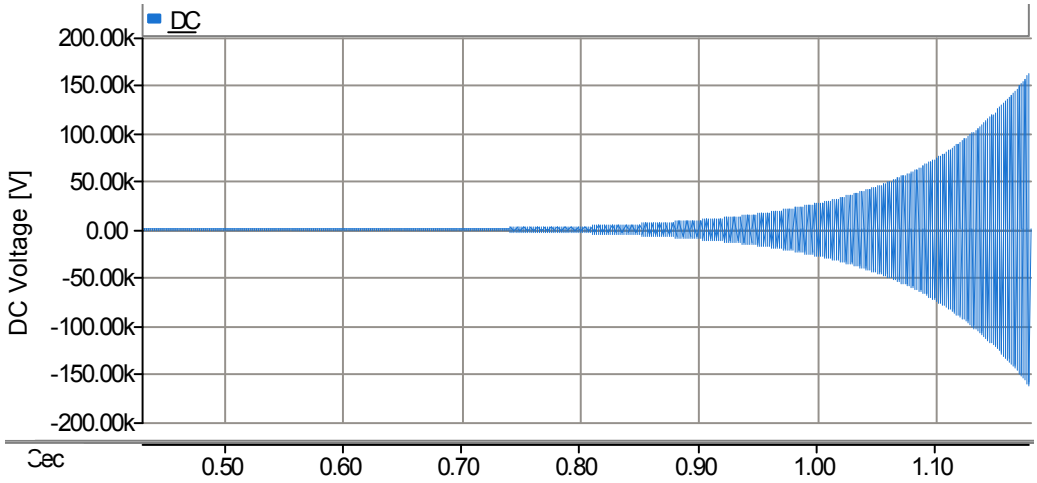


Fig.4.23: Instability of system after reducing capacitance of cdc by 50%

4.5 Effect of adding a low pass filter to the proposed controller

Equation (4.7) presents the proposed control strategy for fine tuning and it shows that the signal includes dc and 2nd order harmonics. Due to presence of 2nd order harmonics in this equation (4.2) a low pass filter is needed to be applied in order to eliminate the harmonics. Transfer function of the employed second order low pas filter is presented in equation (4.23).

$$tf_{lp}(s) = \frac{G}{1+2\xi\left(\frac{s}{w_c}\right)+\left(\frac{s}{w_c}\right)^2} \qquad (4.23)$$

where G is the gain, w_c is the cut off frequency of the filter and ξ is the damping factor of the filter. These parameters for the employed low pass filter within the proposed controller are provided in Table 4.3.

Parameter	Value
G	900
W_C	30
ξ	0.7

Table 4.3: Parameters for the employed low pass filter

One of the typical approaches to investigate the performance of a filter is to plot its frequency response over a range of frequencies. Logarithmic magnitude response of the low pass filter with presented parameters in Table 4.3 is plotted in Fig.4.24. This figure shows that DC signals (signals below 1Hz) passes through the filter without any attenuation however those are above 10Hz have been attenuated based on their frequency.

In the proposed controller it is required to filter out the AC signals and the frequency response of the applied filter shows that it well matches with the requirements of the controller.

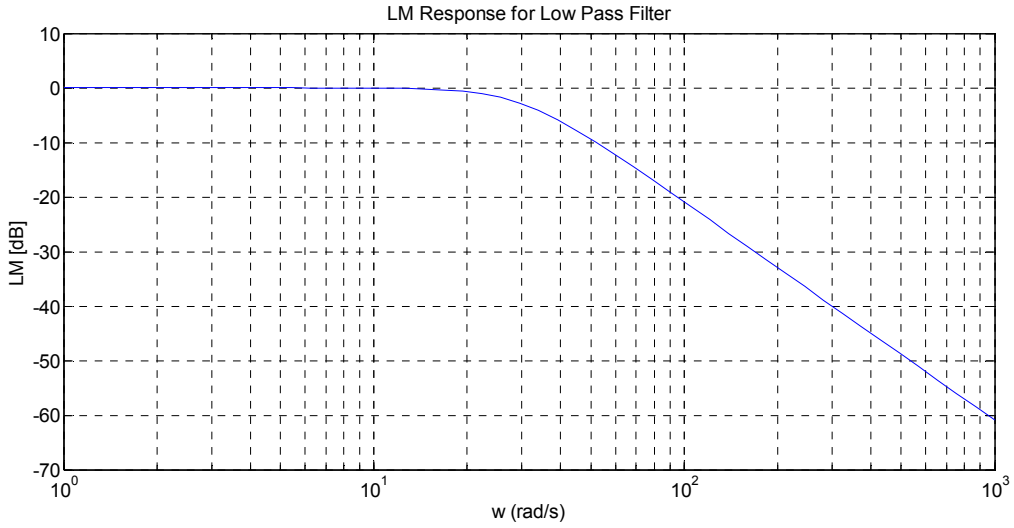


Fig.4.24: Logarithmic magnitude response of the low pass filter

However, applying a filter to clean up a signal always raises concern about undesirable phase delay which in turn can affect the bandwidth of the controller. The phase response

of the applied low pass filter is plotted in Fig.4.25. It shows higher phase delay for the high frequency signals and less delay for low frequency signals. In the proposed controller only DC signal is required to be employed and applied filter must not disturb it.

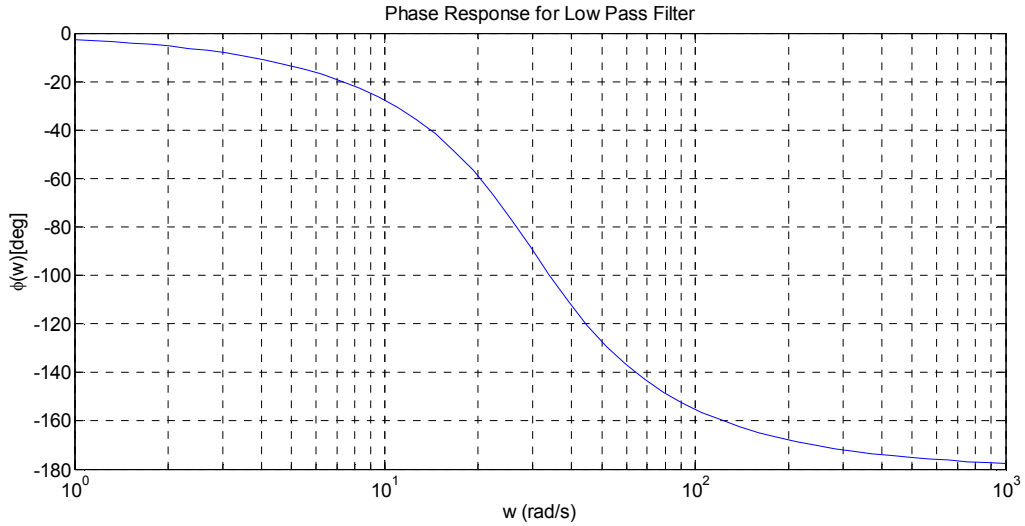


Fig.4.25: Phase response of low pass filter

In addition the proposed controller is just for the fine tuning purposes and it is mainly employed to reduce the error of injection voltage angle in steady state and it is not expected to contribute toward the transients. In the other hand the phase delay introduced by low pass filter mainly affects the transient of the system. For this reason 2 or 3 degree phase delay for DC signal created by filter is negligible. This is not affecting the bandwidth of the main controller (DC voltage controller) as the main controller operates independently in order to regulate the DC voltage across the DC capacitor.

In the DSSC device because of losses within the converter and other components the injection angle practically cannot be 90°. However, the target value is 90° and a steady state error is expected to persist between the reference (target) value and practically achieved value. It means that steady state error of zero practically is not achievable.

In a PI controller, integrator part corrects the steady state error by accumulating the error and increasing the amplitude of controller output. The aim is to eliminate the error in the injected voltage and it means that the angle of injected voltage is desirable to become exactly 90°. However as discussed earlier this is practically unachievable and as a result the integrator in the PI controller will keep accumulating the error and amplitude of the output will increase continuously. Having considered this and taking into account the steady state error in the injection angle (which controller must live with

it) only a proportional controller has been used as shown in Fig.4.2 in order to avoid the aforementioned issue. The gain of the controller is proportional to the offset value of the angle.

4.6 Simulation of performance of proposed controller

In this study, an 11kV distribution network, shown in Fig.4.26 has been considered. This network contains two parallel lines. Both of them are connected to an 11kV substation at one end and supplying a lumped load at another end. Line1 has 20miles (typical long distribution feeder) in length, 2.368Ω resistance and 5.175Ω reactance which is equipped with DSSC. Furthermore the Line1 and other line parameters are tabulated in Table 4.4.

Line number	Line resistance	Line reactance	Compensation	Line current capacity
1	2.368Ω	5.175Ω	Yes	575A
2	2.86Ω	6.25Ω	No	345A

Table 4.4: System parameters

For simulation studies twenty DSSC modules are distributed along the length of this line; each of them connected in series through a single turn transformer with a turn ratio of 100/1(in single turn ratio the primary side is only one turn). A DC link capacitor of 500μF, rated at 1.5kV, is used in the calculations.

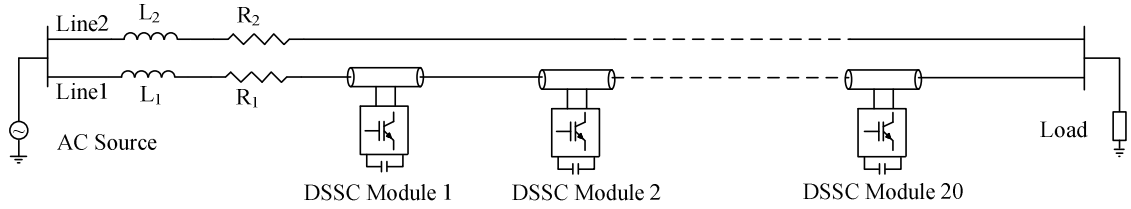


Fig.4.26: One of the two feeders is equipped with 20 DSSC devices

DSSC device parameters can be found in Table 4.5.

Parameter	Value
Capacitance of DC capacitor	500uF
Ratio of STT	1:100
Range of injected voltage	Between -10 and 10 volts

Table 4.5: DSSC device parameters

The amount of compensation as a percentage of line reactance can be determined by adjusting the amplitude of the injected voltage between -10V and 10V depending on the system's control strategy. The DSSC devices are seen as a voltage source through the power line as shown in Fig.4.27.

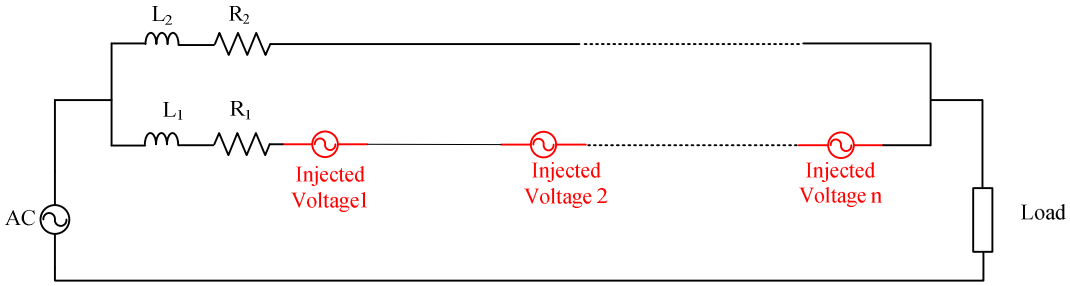


Fig.4.27: DSSC is seen as a VSC through the power line

The proposed new control strategy, as explained earlier, has been used to control the DSSC modules through the line1. The PSCAD/EMTDC software is used for simulation to show that using the proposed controller the DSSC device is able to inject capacitive and inductive voltage through the line. The simulation results also approve the claimed advantages of the controller in this chapter.

4.6.1 Capacitive injection

With the intention of investigating the capability of DSSC modules in injecting the demanded capacitive voltage the devices are set to inject 10 volts in total. The output voltage of the H-bridge converter which is pulse voltage is shown in the Fig.4.28. The polarity of the voltage is keep changing based on the switching of the IGBTs in the converter. Peak value of the output voltage, 1kV, is equal to voltage across the DC capacitor.

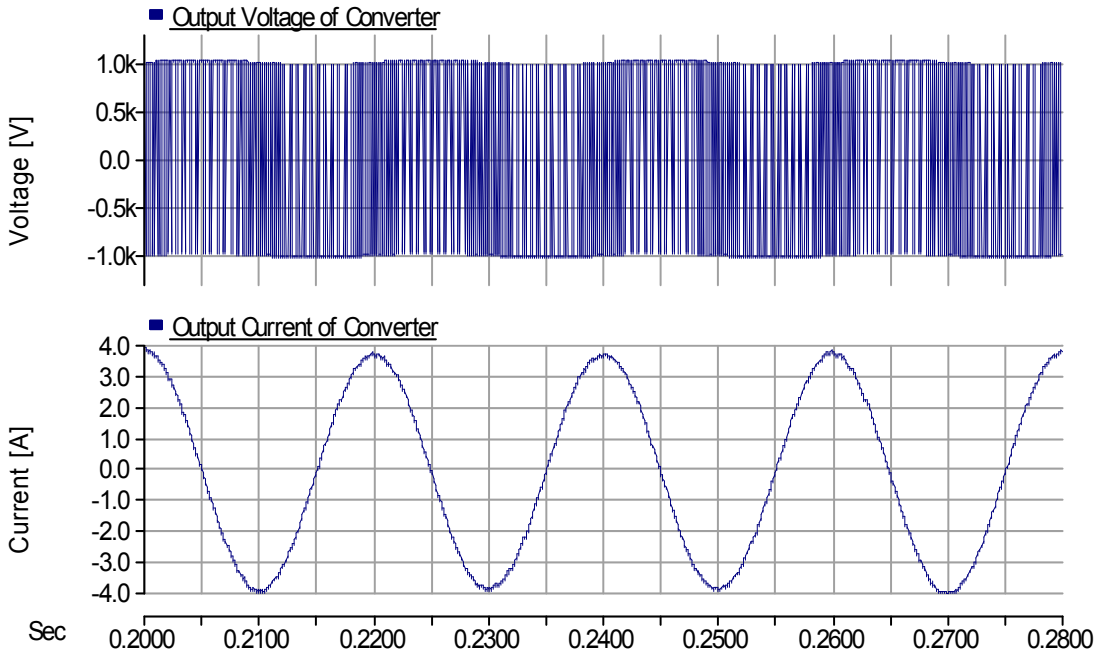


Fig.4.28: The output voltage of the converter and its input current

Input current of the converter also is shown in this figure which is proportional to the line current. The current, passing through the DC link and the current which is fed into the converter are shown in Fig.4.29. The converter current, as shown in this figure, is sinusoidal and proportional to the line current. The DC link current clearly shows effect of switching action. The flow direction of current is being changed in the DC link in order to charge and discharge the capacitor voltage to hold the DC voltage in a desired value.

Actually a certain level of DC voltage is required in establishing the output voltage of the converter. As discussed earlier and shown in Fig.4.28 the output voltage of the converter is a chain pulse of the DC link voltage with positive and negative polarities. However the chain pulse is filtered out by LC filter and generates a sinusoidal waveform with fundamental frequency at the secondary side of the STT. The voltage of the secondary side of STT along with the associated current is shown in Fig.4.30.

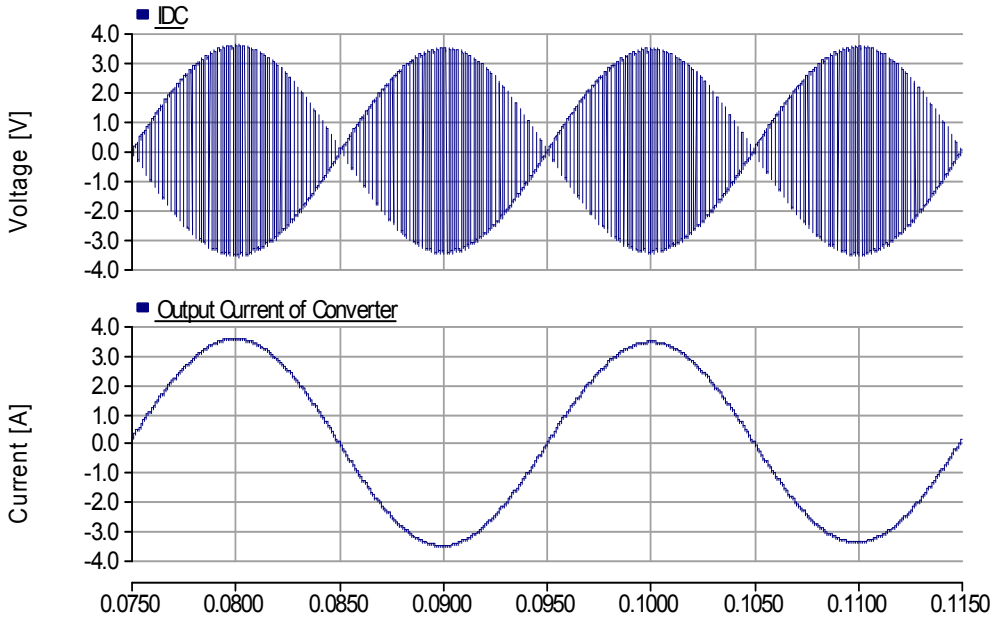


Fig.4.29: DC link current and output current of the converter in the capacitive injection mode

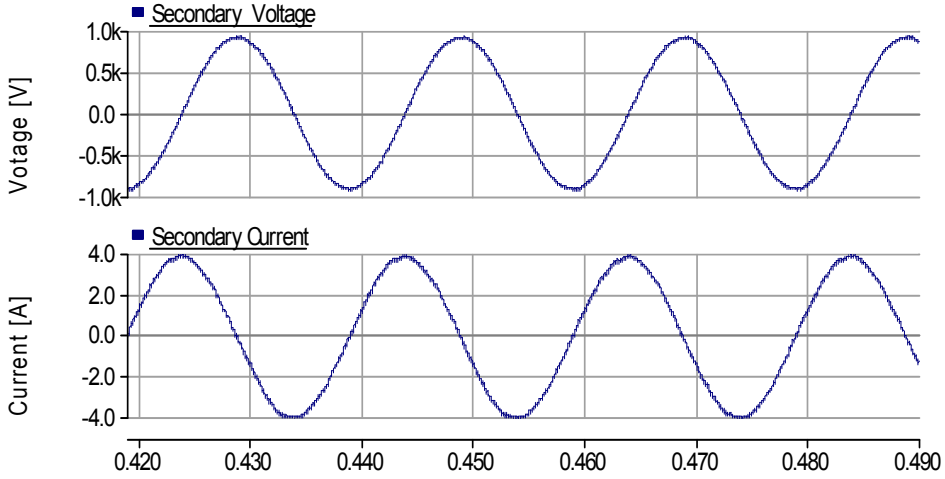


Fig.4.30: Voltage and current in the power electronics side of the STT in the capacitive injection mode

The injected voltage through the line is shown in Fig.4.31. It can be seen that the voltage is leading the line current, and it is a capacitive injection. In order to investigate the consequences of capacitive voltage injection by DSSC modules, three different voltages value at 0V, 0.6Vand 1.4Vper each module have been injected. These voltages are corresponding to 0%, 20% and 50% compensation of phase reactance by DSSC in the studied power system. Fig.4.32 shows the compensation in three steps. At first there is no voltage injection, the system is in normal operation and phase current remains

unchanged. In the second step the DSSC modules compensate 20 % of the phase reactance. In order to obtain such compensation it is necessary to inject 12 volts. In the next step the modules are required to compensate 50% of the reactance, therefore they inject 28 volts. At the final stage the compensation returned back to 20% and it shows that the modules can increase or decrease the percentage of compensation.

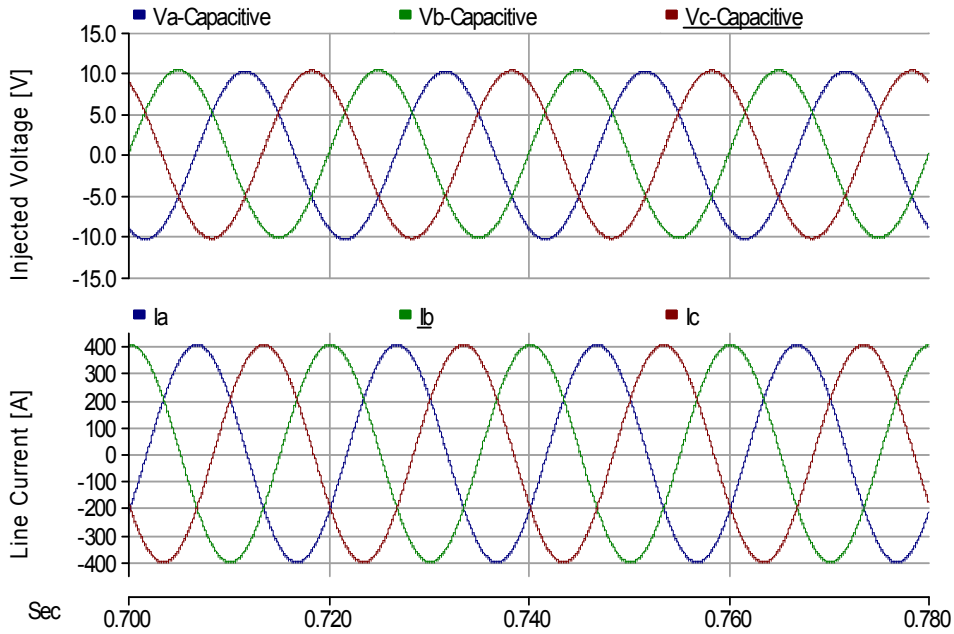


Fig.4.31: Capacitive injection and voltage is leading the current

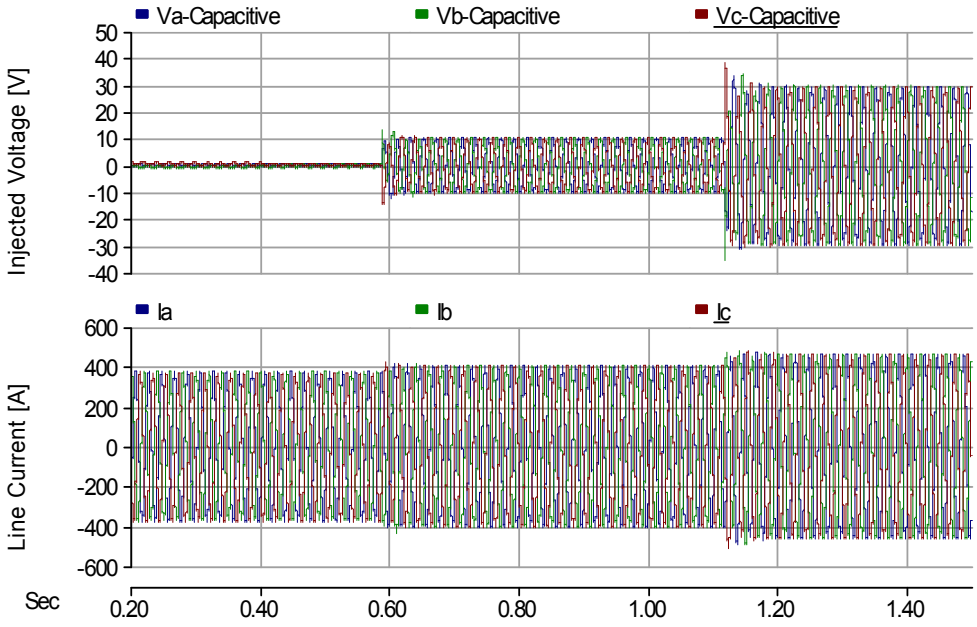


Fig.4.32: Capacitive injection in three different levels

The consequence of different levels of compensation can be seen in the current of the compensated line. With injection of capacitive voltage it is expected that the virtual capacitor to be inserted through the line. This leads to reduction of the reactance of the line. Less reactance means increment in the line current.

4.6.2 Inductive injection

DSSC modules are able to inject inductive voltage as well because they can effectively increase the line reactance. This feature is useful in the power flow control when the operator wants to push away current from a specific line. To do so the final injected voltage through the line must lag the line current. However the output voltage of the converter is a pulse voltage and its polarity is changing in different switching condition and it is shown along with the input current of the converter in Fig.4.33.

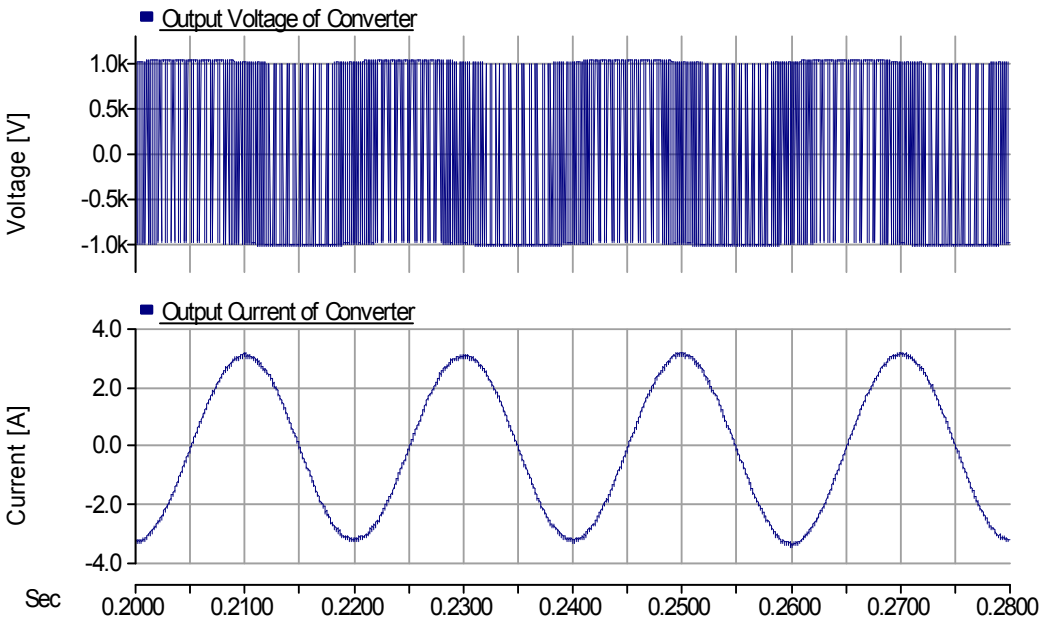


Fig.4.33: Output voltage of the converter along with the input current

The DC link current (current passing through the DC capacitor) along with output current of the converter is shown in Fig.4.34. The flow direction of the current through the link is being changed frequently to regulate the DC voltage.

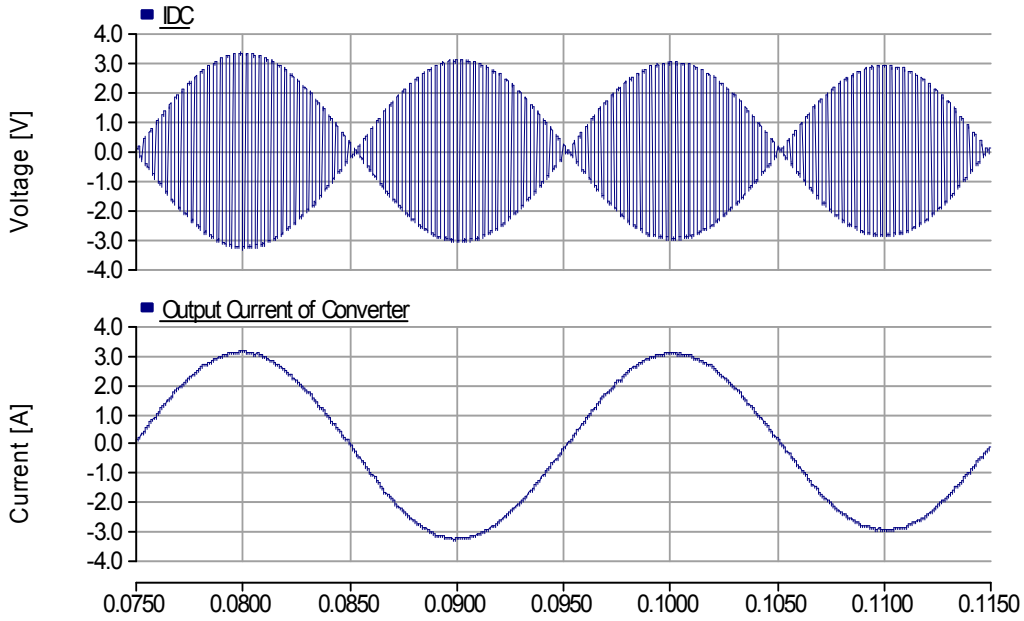


Fig.4.34: DC link current and output current of the converter in the inductive injection mode

Align with the changing of the flow direction of current in the DC link the polarity of the output voltage is being changed to synthesize the required voltage at the output of the converter. The generated voltage (pulse voltage) by the converter is being filtered by the LC filter. Voltage and current in the secondary side of the STT is shown in Fig.4.35. This voltage is injected through the line using STT (same as the capacitive injection mode) and it is shown in Fig.4.36. It shows that the injected voltage is lagging the line current and the DSSC is capable of injecting of inductive reactance when the proposed controller is being applied.

In order to examine the inductive injection capability of the DSSC in the test network, the line reactance is purposely increased by 0%, 20% and 50%. In order to achieve this compensation levels, lagging voltages of 0V, 12V and 28V have been injected respectively, as shown in Fig.4.37. In this firstly there is no injection but soon after in the second time interval the DSSC modules injects 12 V with the purpose of inserting 20 % inductive reactance through the line.

The reduction of the line current shows that the impedance of the line has been increased as result of the injection. Furthermore in the next time interval the DSSC modules insert 50 % more inductive reactance and consequently the line current reduces further. At the final stage again there is no injection and the line current returns back to the normal, clearly indicating that with voltage injection removed the compensation line will back to the normal conditions. This shows that the adding capacitive or inductive

reactance through the line can be easily achieved. Even the amount of compensation can be easily altered.

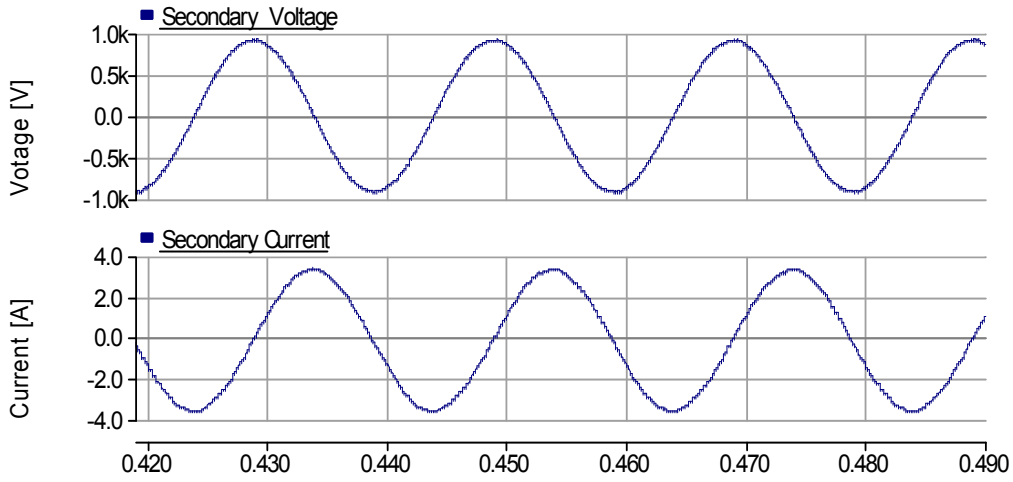


Fig.4.35: Voltage and current in the secondary side of the STT in the inductive injection mode

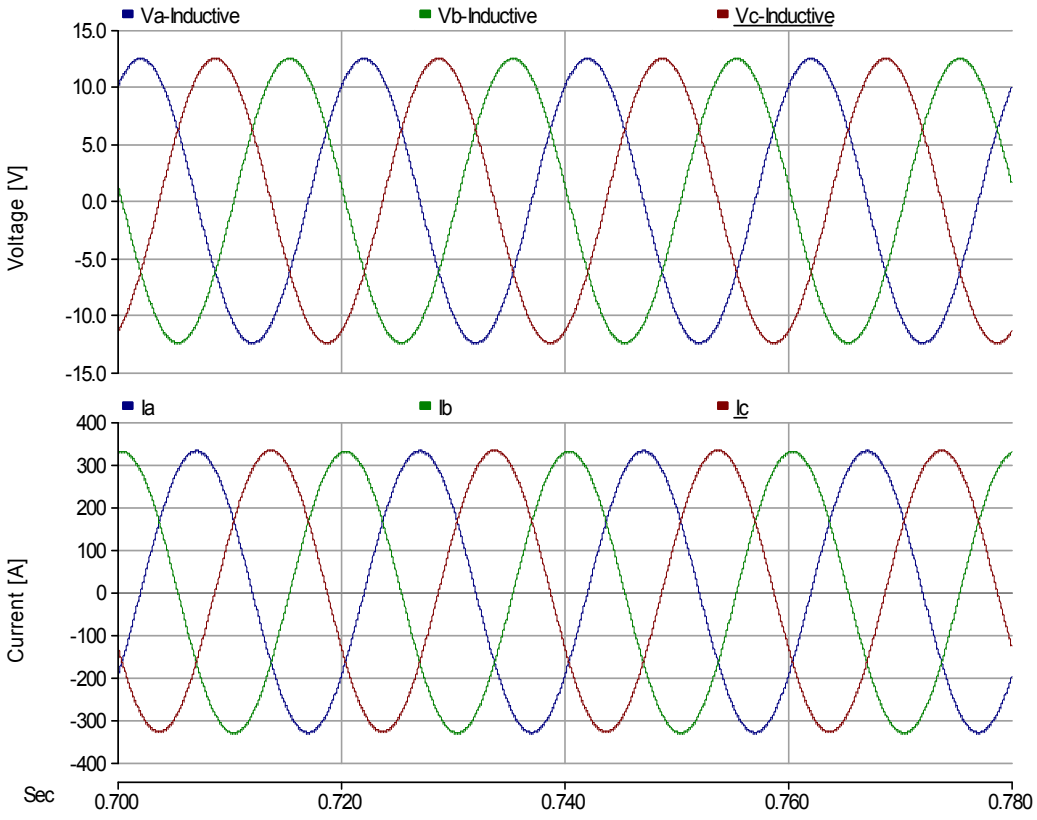


Fig.4.36: Inductive injection of DSSC modules

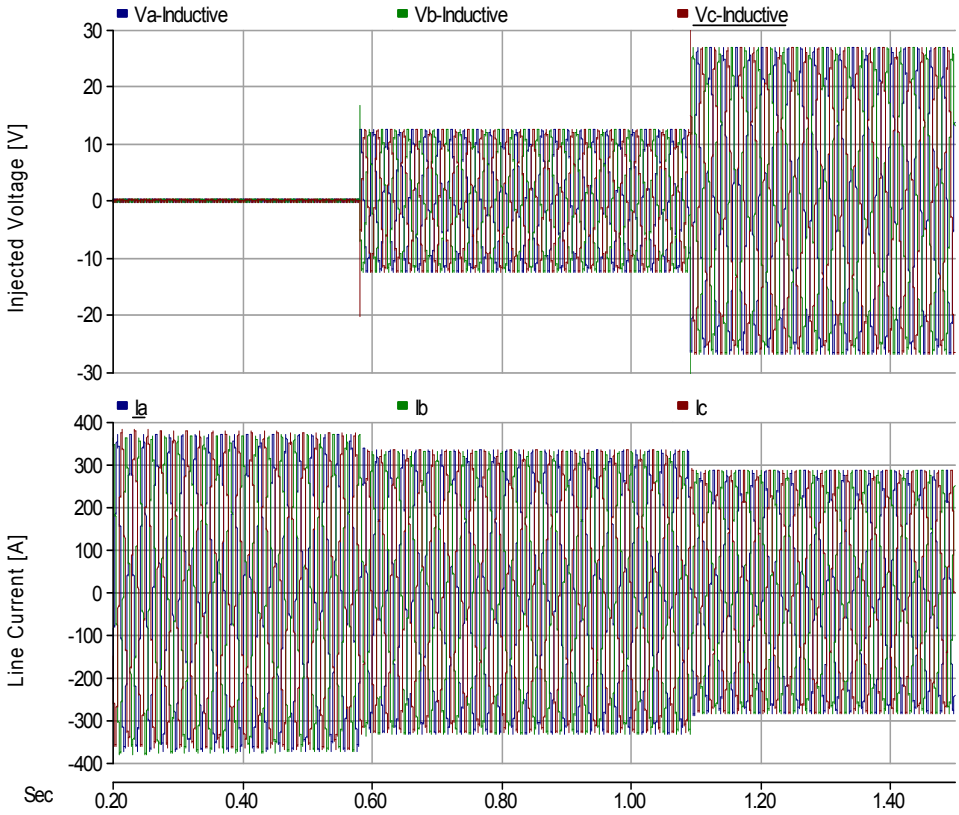


Fig.4.37: Different level of inductive injection

Line1 and line2 are in parallel therefore by increasing the inductance in line1 the current in this line will decrease and consequently line2 current will increase.

4.7 Comparing performance of proposed controller with 90° phase shift based controller

Performance of the proposed controller has been compared with 90° phase shift based controller and dq based controller. The 90 degree phase shift method is used as a control strategy in the simulation of functionality of DSSC. The phase difference between line current and injected capacitive voltage is plotted in Fig.4.38. The phase angle using this controller is -86.85 degree which is different from 90 degree. In this example, the deviation of 3.15 degree is needed in order to make the system become stable. The deviation angle shows that there are some losses within the DSSC device and the angle is diverted from 90 degree to hold DC voltage in the desired value.

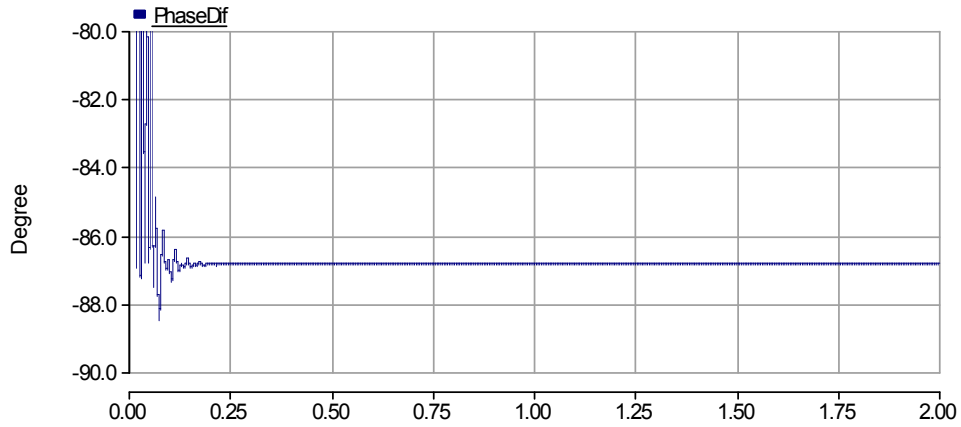


Fig.4.38: Phase difference in capacitive injection mode using the 90° phase shift controller

It must be noted that if the voltage is not injected with a right angle then it will affect the absorbed active power. If the absorption of active power becomes more than ohmic losses then the DC voltage will increase. But in the same time voltage regulator will initiate an error signal to return back the voltage. Consequently the converter needs to switch between the charge and discharge modes more rapidly in order to maintain the DC voltage. This dissipates the absorbed power, and additionally, increases amplitude of the ripples on the DC link voltage.

Losses (or the absorbed active power) inside the DSSC module for 90° phase shift method is plotted in Fig.4.39 using active power measurement block within the PSCAD. In this simulation the aim is to compensate 20 % of the line reactance but DSSC device absorbs active power.

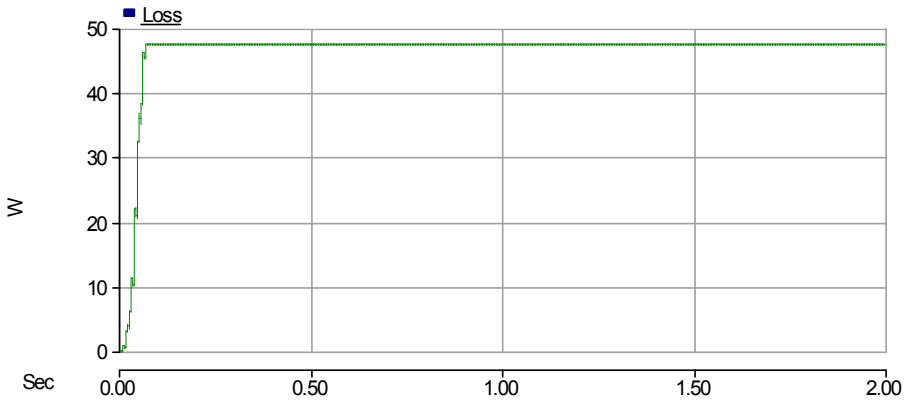


Fig.4.39: Power loss in each DSSC module using the conventional control system

Each DSSC module using the proposed controller consumes 20.33W in order to compensate the internal power losses while in total all of the modules providing 863.34 VAr to contribute toward the line compensation. However with conventional method power loss in DSSC module becomes 47.43 watt. System parameters are tabulated in Table 4.6.

Parameter	Value
System voltage	11kV
Line current	575A
Power Line resistance	2.368Ω
Power Line reactance (rated)	5.175Ω
DC link voltage	1.05kV
Number of DSSC device	20
Switching frequency	5kHz

Table 4.6: System parameters

Line current is shown in Fig.4.40. Current, passing through the DC link and the current is being fed into the converter are shown in Fig. 4.41. The converter current, as shown in this figure, is sinusoidal and proportional to the line current. The DC link current clearly, as shown in Fig.4.41, shows effect of switching action. This current is being chopped frequently to change the flow direction and charge or discharge the capacitor in order to hold the voltage in a desired value.

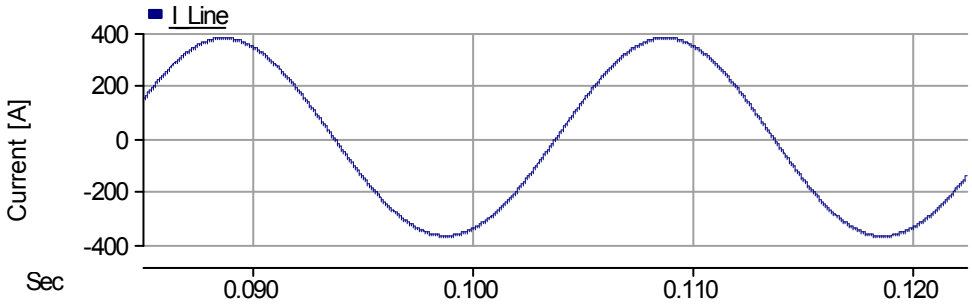


Fig.4.40: Line current

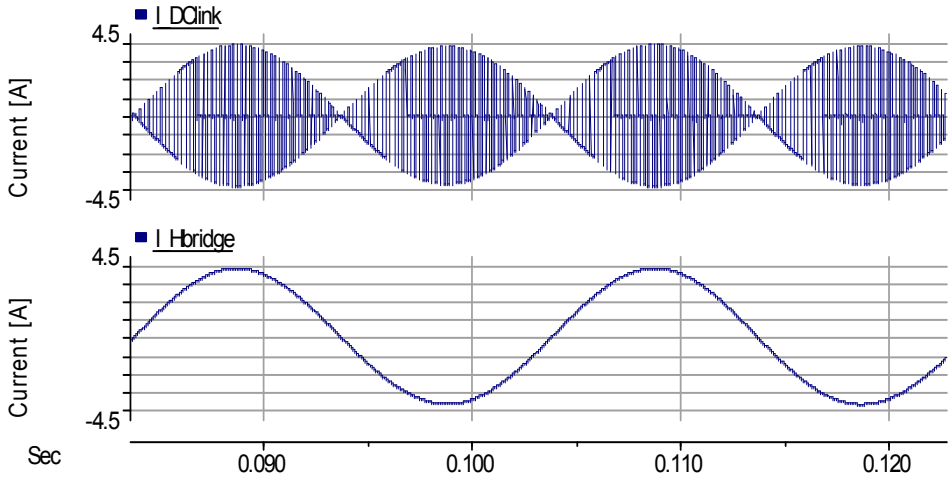


Fig.4.41: Converter current and DC link current

The injection angle is an important factor in regulating the DC voltage across the capacitor and maintaining the stability of whole system. With the intention of presenting the difference in the regulated voltages across DC link when using the conventional approach the DC voltage is shown in Fig.4.42 in more details. Using the 90° phase shift method the ripple in the DC voltages is 4% which is result of erroneous injection angle. With the conventional method the peak value is 1130 volts with respect to 1100 volts. This emphasizes that the method is not more effective in reducing the percentage of ripples.

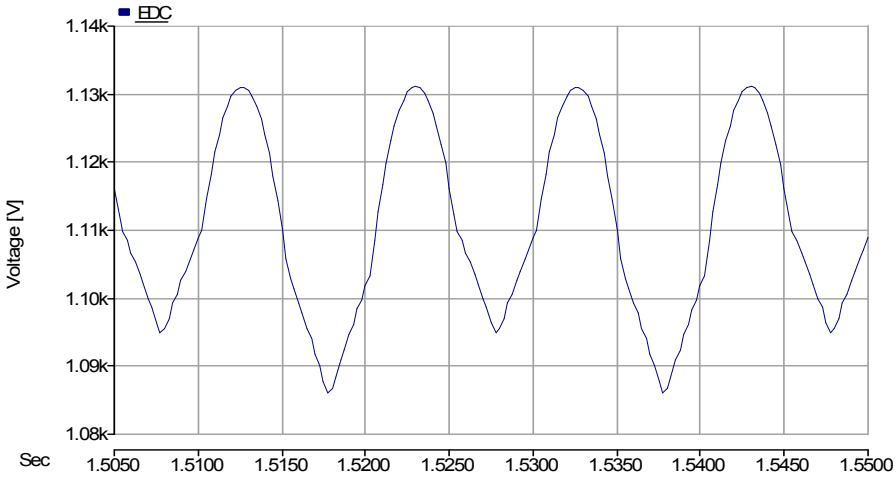


Fig.4.42: Ripple of DC voltage (with the conventional method)

With the conventional method, the harmonic analysis of the injected voltage however reveals that there are 16% of second order harmonic and 3% of third harmonic along with the fundamental injected voltage which is shown in Fig.4.43. In this figure the fundamental voltage is in blue; the green line represents the second harmonics and the brown one shows the third harmonics.

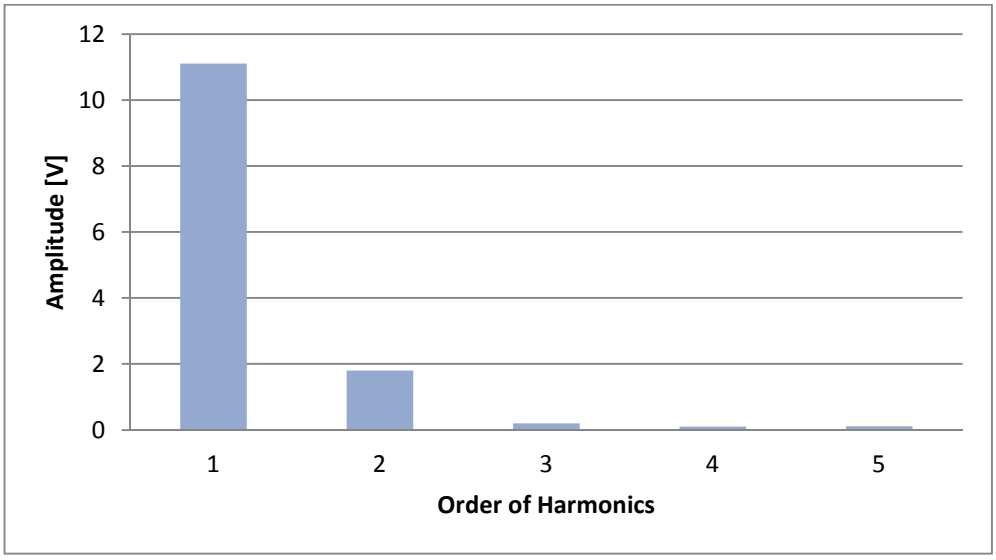


Fig.4.43: Harmonic analysis of injected voltage using the conventional control method

The proposed controller can optimize the injection phase angle. Supporting for this feature, the angle of injected voltage with respect to the line current has been investigated in order to check the accuracy of the controller. The phase difference between line current and injected capacitive voltage by using the proposed controller is plotted in Fig.4.44.

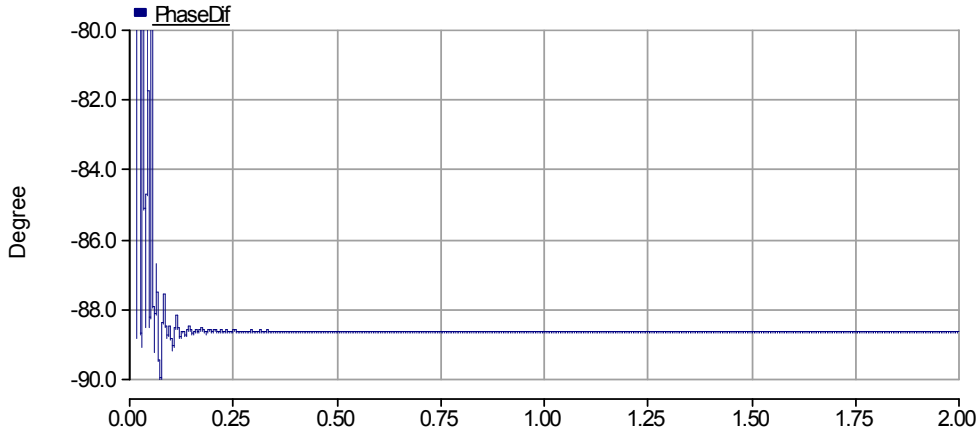


Fig.4.44: Phase difference in capacitive injection mode using the proposed controller

The phase angle using the proposed controller is -88.65 degree and -86.85 degree with the conventional control strategy. Comparison between Fig.4.38 and Fig.4.44 shows that, the angle in using the proposed controller is closer to -90 degree. It must be noted that if the voltage is not injected with right angle then it will affect the absorbed active power. If the absorption of active power becomes more than ohmic losses then the DC voltage will increase. But in the same time voltage regulator will initiate an error signal to return back the voltage. Consequently the converter needs to switch between the charge and discharge modes more rapidly in order to regulate the DC voltage. This dissipates the absorbed power, and additionally, increases amplitude of the ripples on the DC voltage.

Losses (or the absorbed active power) inside the DSSC module for the proposed control strategy is plotted in Fig.4.45. In both cases the aim is to compensate 20 % of the line reactance but different control system absorbs different active power.

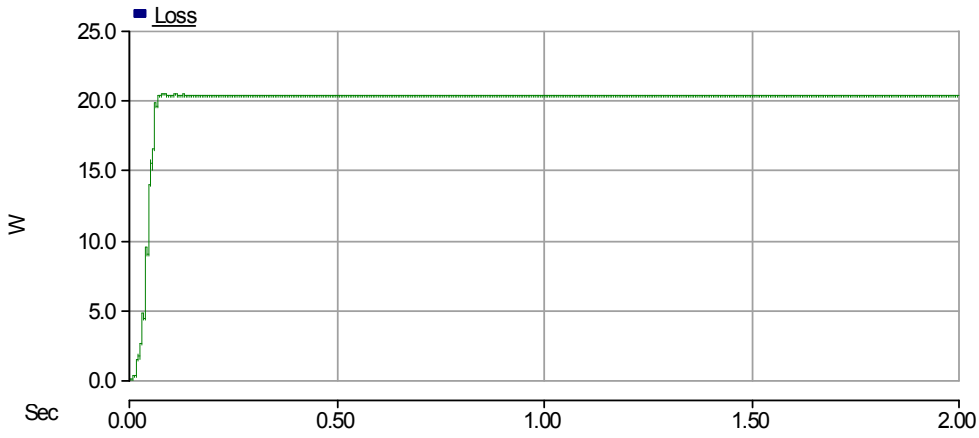


Fig.4.45: Power loss in each DSSC module using the proposed control system

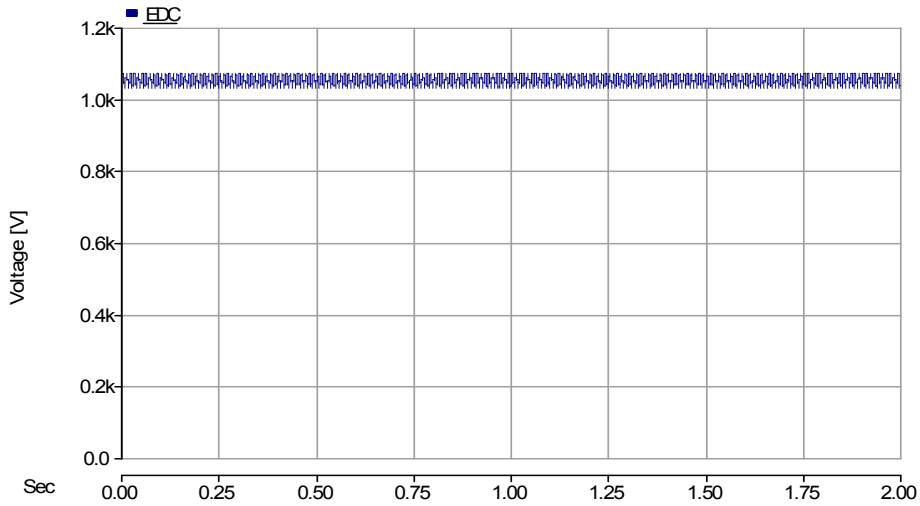
The losses within the DSSC modules are measured by using active power measurement block in the PSCAD software. Each DSSC device using the proposed controller consumes 20.33W in order to compensate the internal power losses while in total all of the modules providing 863.34 VAr to contribute toward the line compensation. However with conventional method power loss in DSSC module becomes 47.43 watt, which is much higher than that in the proposed method, while they both provide same reactive power to the system. A summary of above figures including the power losses, injection phase angle, injected reactive power and percentage of losses in comparison with the amount of injected reactive power are given in the Table 4.7.

Simulation Results	20% Compensation	
	Conventional Method	Proposed Method
Reactive Power Injection	864.12 VAr	863.34 VAr
Power Loss	47.43 W	20.33 W
Phase angle	-86.85	-88.65
Loss percentage	5.4 %	2.3 %

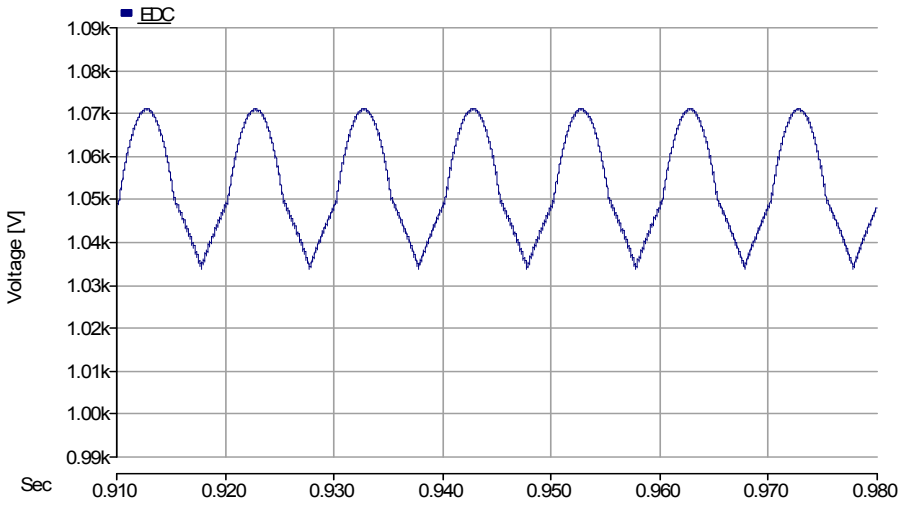
Table 4.7: Summery of power loss and phase angle study

From the table it can be concluded that, in order to inject almost same amount of reactive power, the proposed method helps to reduce losses from 47.43W to 20.33W per module, i.e. by 3.1%, when compared to the conventional one.

The injection angle is an important factor in regulating the DC voltage across the capacitor and maintaining the stability of whole system. With the intention of presenting the difference in the regulated voltages across DC link when using the new control method is shown in Fig.4.46 in more details. Using the proposed method the ripple in the DC voltages is 3.2 % of the peak value, which is 1.05kV. This shows the peak value is 60 volts less than that in the conventional method. This emphasizes that the proposed method is more effective in reducing the percentage of ripples compared to the conventional one.



a) DC voltage across the DC link (with proposed controller)



b) Ripple of DC voltage (with proposed controller)

Fig.4.46: Ripple of DC voltage

With harmonic analysis of the injected voltage as shown in Fig.4.47, it is realized that there is no significant harmonic voltage injection when the proposed method is used.

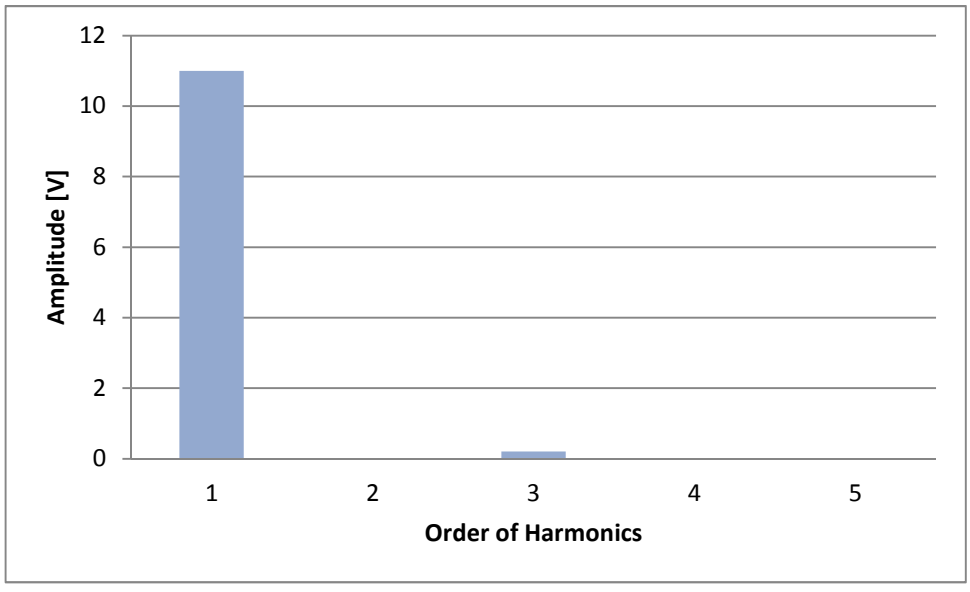


Fig.4.47: Harmonic voltage injection (using the proposed control method)

Earlier in this chapter it has been claimed that the controller is immune against presence of harmonics in the power system. This capability has been examined by simulating a system which is shown in Fig.4.48. In this system V_1 is representing the main source with the fundamental frequency and V_2 is demonstrating the harmonic source.

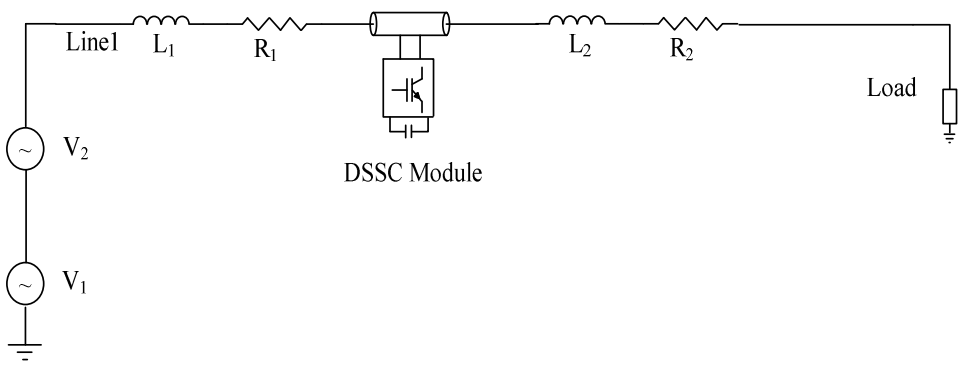


Fig.4.48: System including harmonics

L_1 and L_2 are representing the line inductance and the resistance of the line is shown by R_1 and R_2. The line current is shown in Fig.4.49 and it includes 5% of fifth harmonic. The harmonic analysis of the line current is shown in Fig.4.50 and in this figure amplitude of the fundamental current and fifth harmonic come in blue and pink respectively.

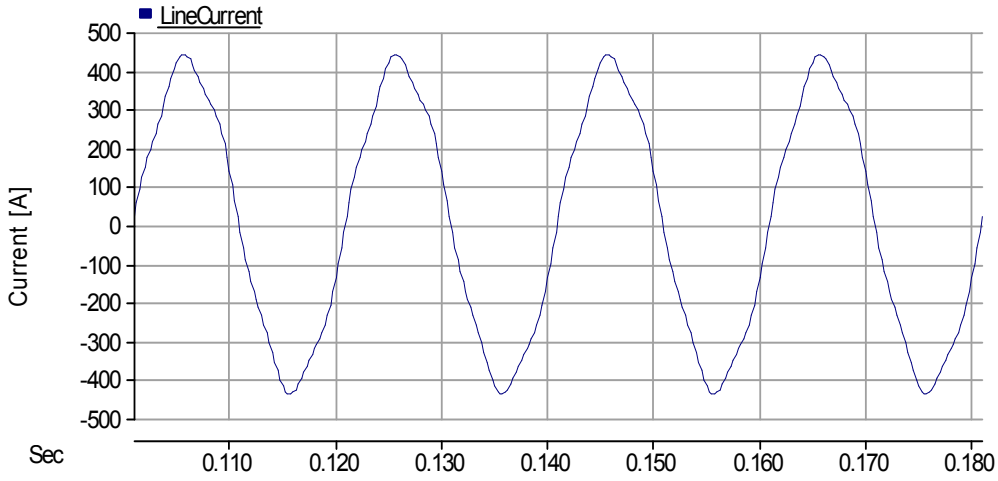


Fig.4.49: Line current including 5% of fifth harmonics

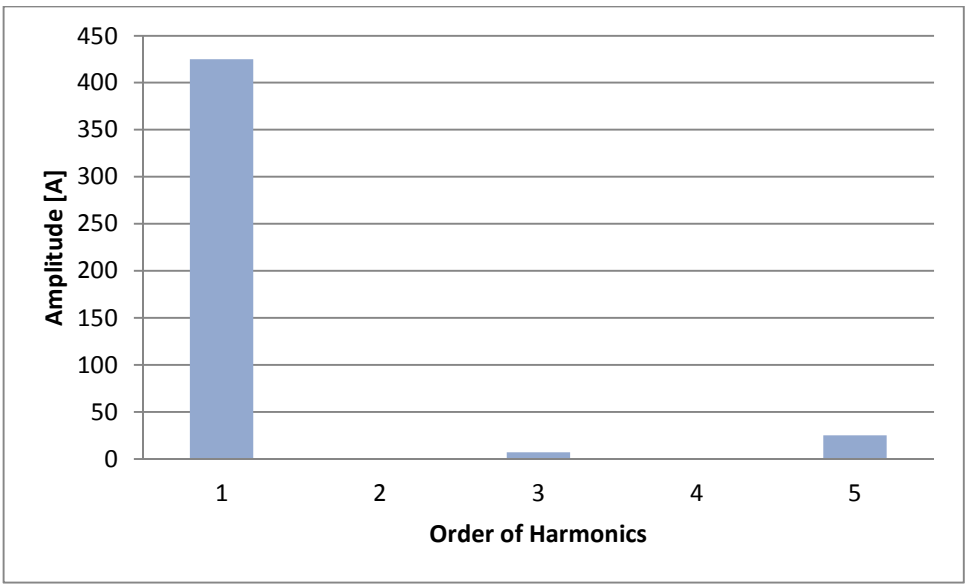


Fig.4.50: Harmonic analysis of the line current

The exchanged power between the DSSC device and the AC power system is shown in Fig.4.51. It can be easily observed from the figure that the AC signal is still symmetrical and even the DC signal is zero. These show that with presence of harmonics the controller still works properly, filtering out the polluting harmonics.

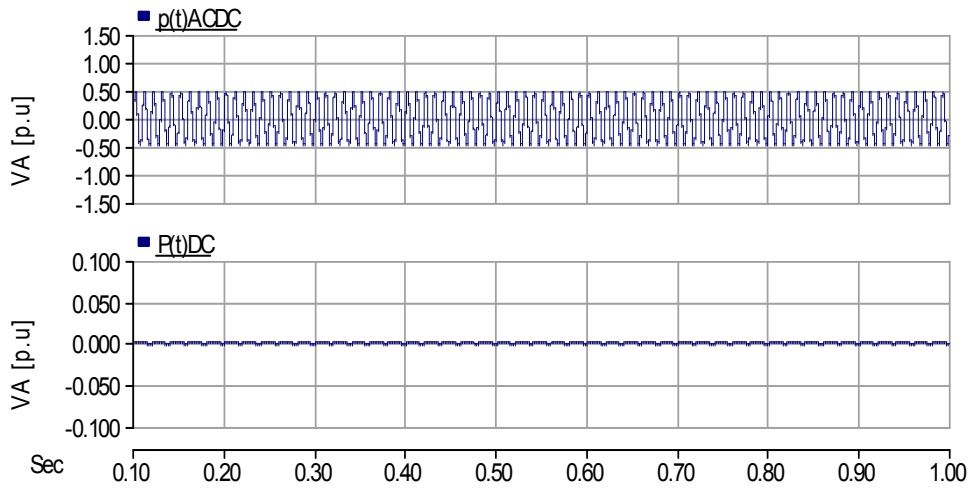


Fig.4.51: p(t) ACDC and p(t)DC in presence of 5% 5th harmonic

More extensively, in order to study the probable effect of the harmonics in highly polluted power systems the functionality of the controller is tested with the presence of

10 % fifth of harmonic, plus 5% of third harmonic. The simulated results are shown in Fig.4.52.

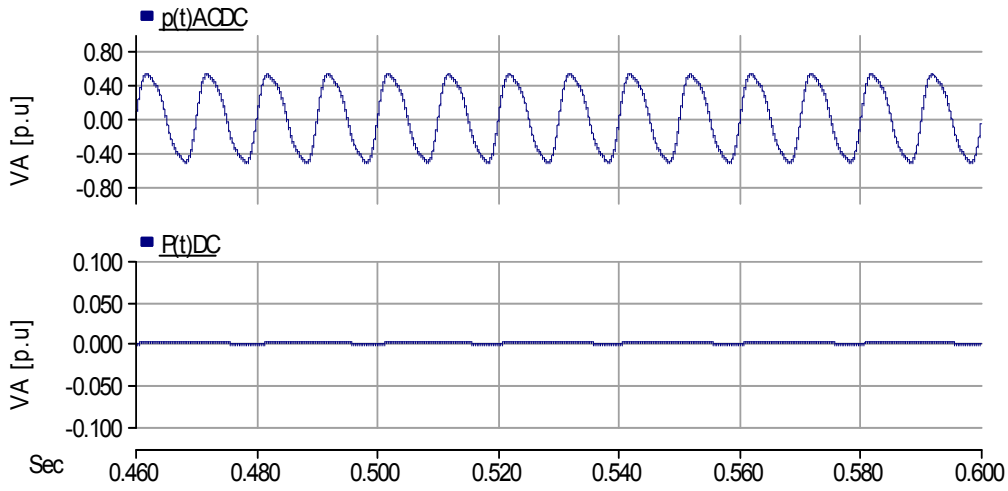


Fig.4.52: p(t)ACDC and p(t)DC in presence of 5% 3rd harmonic and 10% 5th harmonic

The above figure shows that the waveform of the AC signal includes harmonics and based on the equation (4.12) the harmonics are defiantly higher than 2nd harmonic. In the same time the filter is tuned to pass the low frequency signals (below the 2nd harmonic and nearly dc signal) then consequently the high order harmonics will be bypassed. Actually, by comparing Fig.4.51 with Fig.4.52 it can be clearly observed that the DC signal remains unchanged. From all results obtained above, it can be concluded that the harmonic pollution is not an affecting parameter for the proper operation of the controller. In other words, the proposed control is immune against harmonics.

4.8 Comparing performance of proposed controller and dq based controller

In the proposed single phase controller each phase has been controlled independently. However, dq based controller is a three phase controller and three phases are not independent from each other. In an unbalance three wire three phase system there is no zero sequence in the line current and the current can be decomposed to positive and negative sequences using control strategy presented in Fig.2.52.

4.8.1 Performance of proposed controller within three phase system

The proposed controller which is designed earlier in section 4.3 (The controller is comprised of a PI controller and a feedback from multiplication of line current and

injected voltage which is passing through a low pass filter as described in controller design section) and presented in equation (4.22) has been applied within a distribution network. The parameters of the employed distribution power system are tabulated in Table 4.6 (power system parameters). In this subsection the performance of the proposed controller in terms of its capability in regulating the DC voltage and injecting compensation series voltages have been investigated. Control system in each DSSC module produces its own reference signal without involving with other modules. Fig.4.53 shows that three DSSC modules employed in three different phases are capable of regulating the DC voltage within the required value.

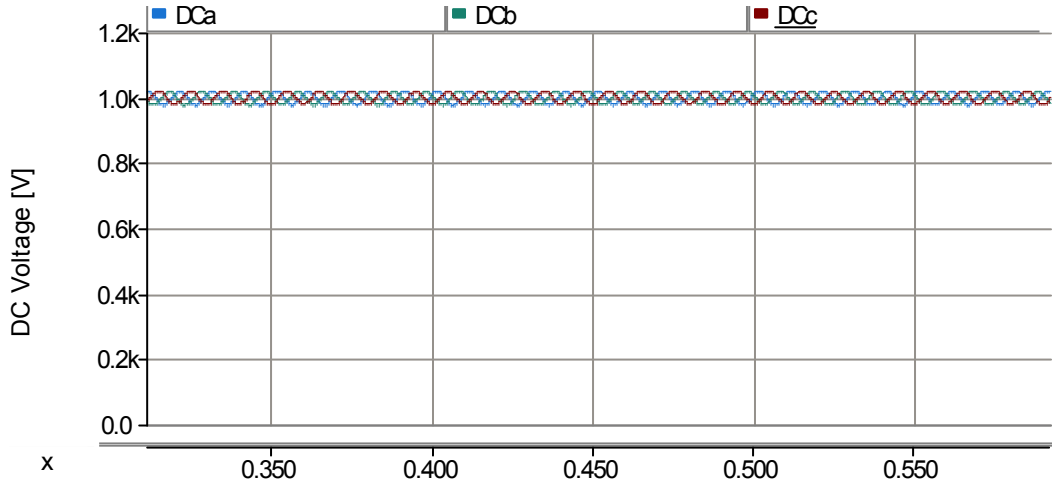


Fig.4.53: Voltage across the DC link within DSSC modules employed in three different phases

In order to compare performance of system in supplying balanced load and unbalanced load these two setups have been investigated. The examined three phase system is supplying a three phase balanced 6MW load. The line currents and injected voltages by DSSC devices are shown in Fig.4.54. The figure shows that line currents are balanced and the injected voltage in each phase is orthogonal to the line current. The reference signals of injected voltages are shown in Fig.4.55 and they are provided by their own modules independently. The aim of each controller within DSSC module is to provide an injected voltage which is orthogonal to the line current and in the same time hold the DC voltage in desired value. These two requirements have been met by the single phase controller within three phase system. The simulation results presenting the injected voltage and their corresponding reference signals have been shown in figure Fig.4.54 and Fig.4.55 respectively.

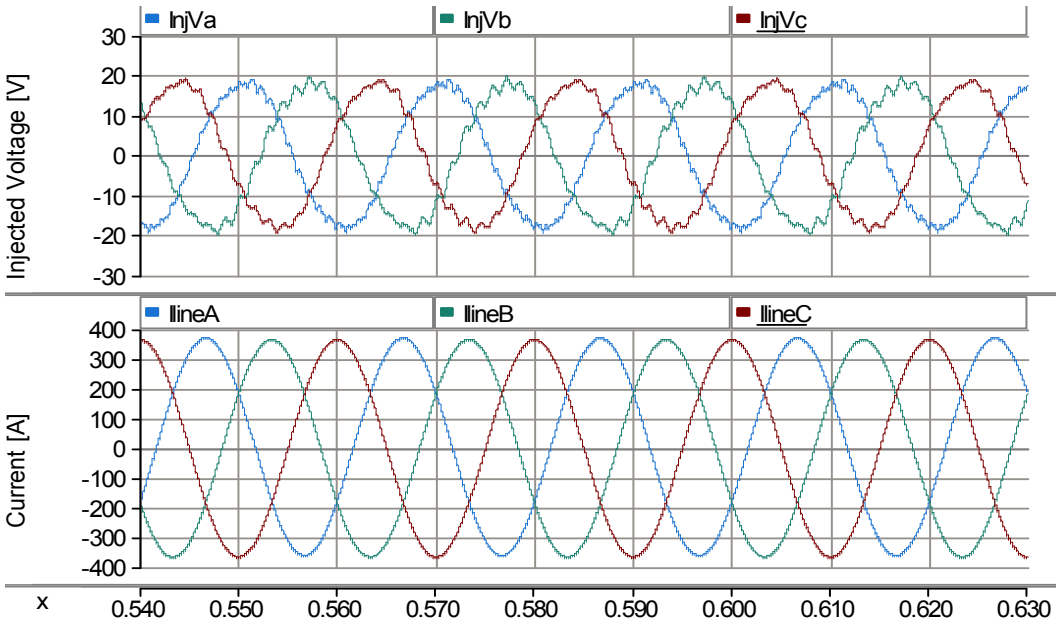


Fig.4.54: Injected voltages by DSSC devices in each phase and three phase line currents

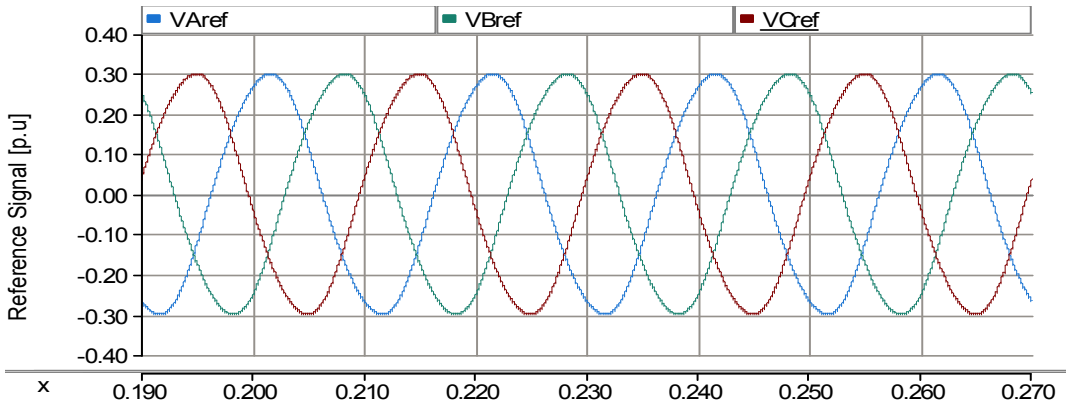


Fig.4.55: Reference signals of injected voltages provided by each DSSC modules separately

However, the above figures show the performance of the controller when the three phase system is balanced. In this case the direct and quadrature component of the line currents (I_d and I_q) shown in Fig.4.56 are smooth. This is an indication for a balanced three phase system. In this figure also the amplitude of the line current is shown by I_{dqLine} which is equal to:

$$I_{dqLine} = \sqrt{I_d^2 + I_q^2} \qquad (4.24)$$

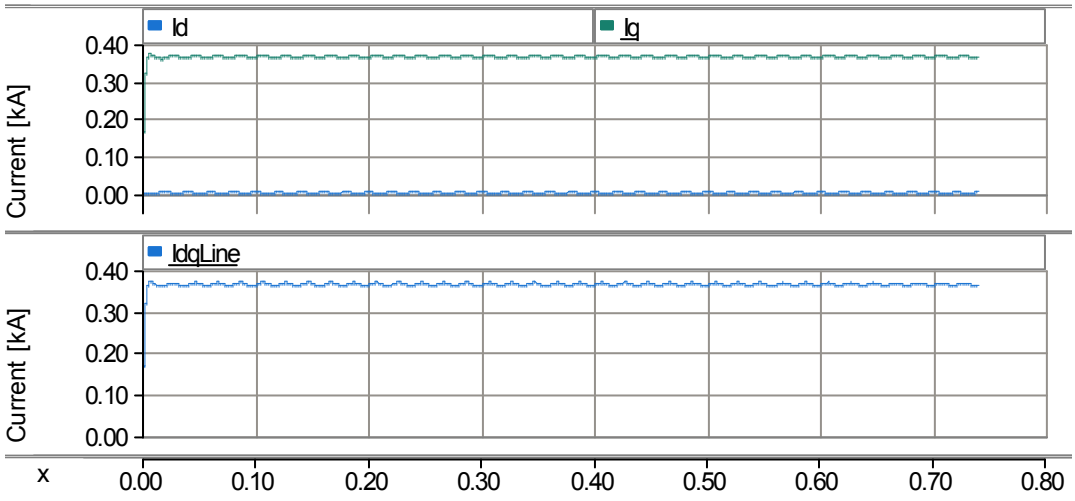


Fig.4.56: Id, Iq and amplitude of the line current

4.8.2 An unbalanced three phase system with no series compensation

An unbalanced load comprises of a 6MW three phase balanced load and a 1MW single phase load connected to the phase "b" of three phase distribution system which its parameters are tabulated in Table 4.6 (the table represents parameters of each phase) has been simulated. The DSSC devices have been bypassed and the lines are uncompensated. The injected voltages and line currents are shown in Fig.4.57. It shows that the injected voltage is zero and line current in phase "b" is higher than the other two phases. This allows observing the status of distribution system in terms of its dq components of line current without compensation.

PLL of series compensators are always locked to the line current. However with unbalance line currents the dq components can be distorted. The I_d and I_q components of line current without compensation along with the amplitude of the line current is plotted in Fig. 4.58. It can be clearly observed that dq components are oscillatory.

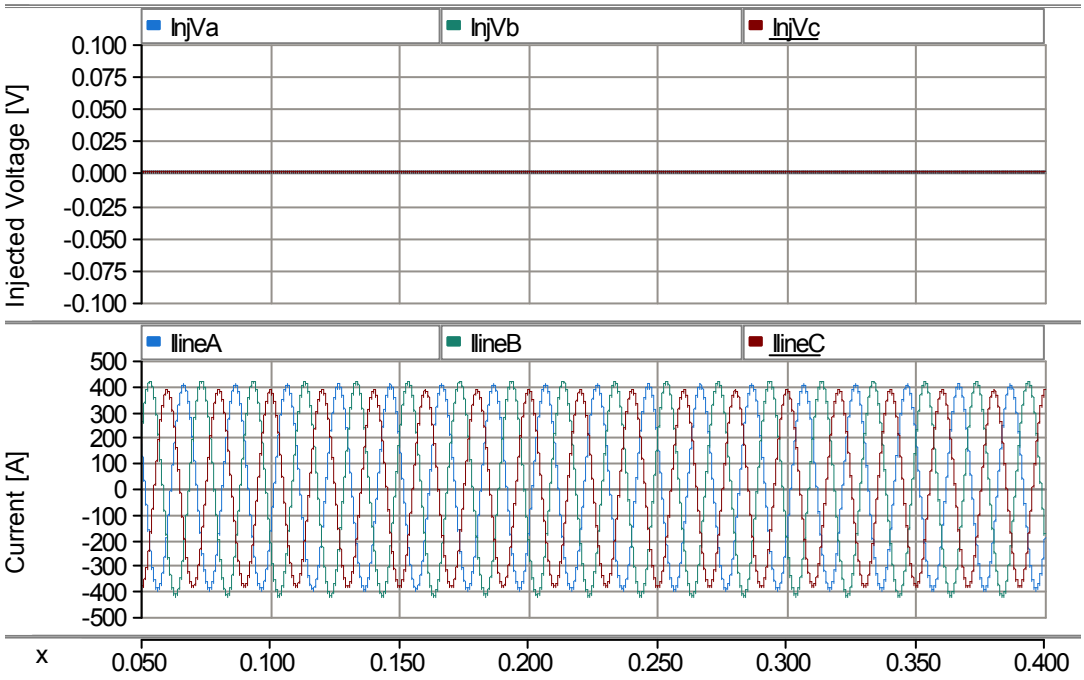


Fig.4.57: Injected voltage and line currents when the three phase system is unbalanced

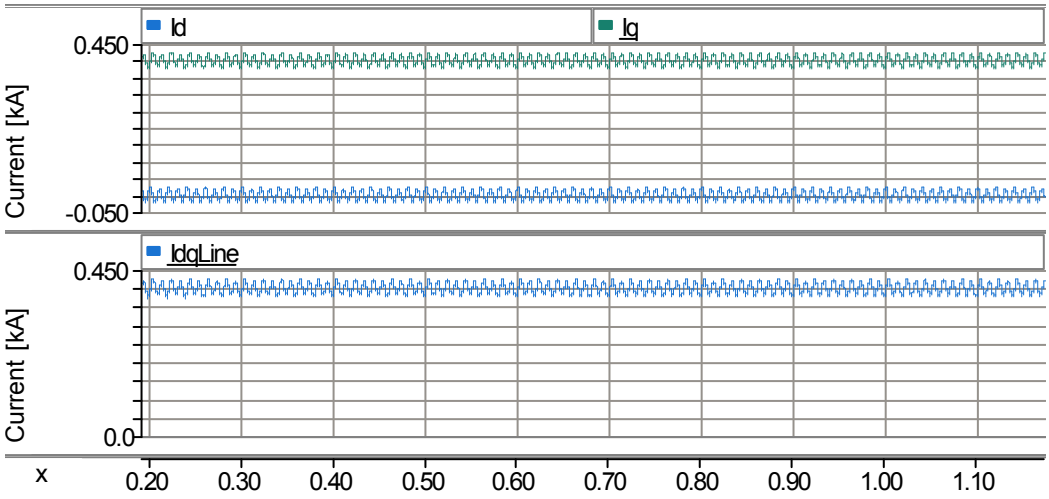


Fig.4.58: The Id and Iq components along with the amplitude of the line current

4.8.3 Performance of propsed controller within unbalanced three phase load

In the previous subsection it has been shown that in the presence of unbalanced load the line currents are unbalanced and dq components are distorted. However simulation results show that the performance of the single phase controller is not affected by unbalance of the system. Voltages across the DC link are illustrated in Fig.4.59 and it shows that the voltage regulation by single phase controller has been satisfactorily achieved in each phase.

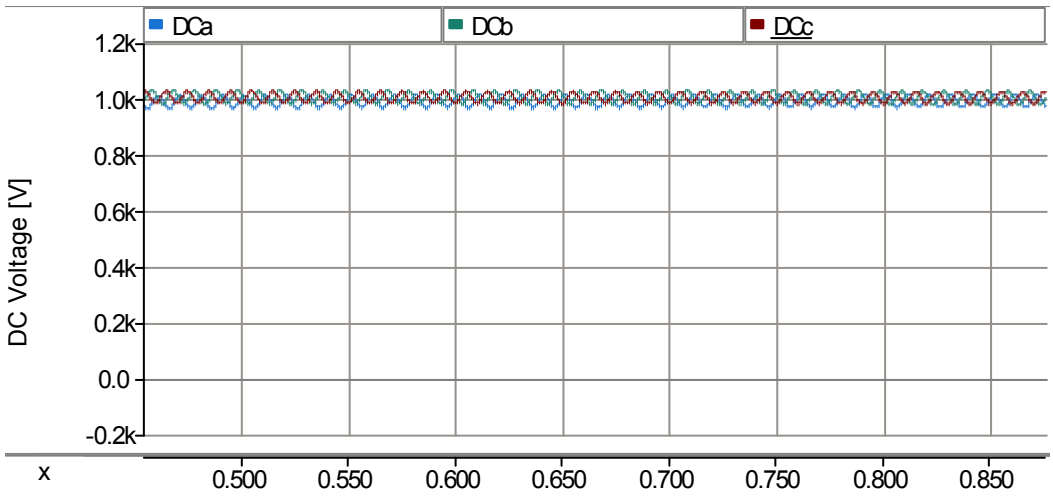


Fig.4.59: DC Voltages

Fig.4.60 shows the reference signals generated by controller within DSSC devices in different phases. The signals are generated independently and they are not affected by the unbalanced currents.

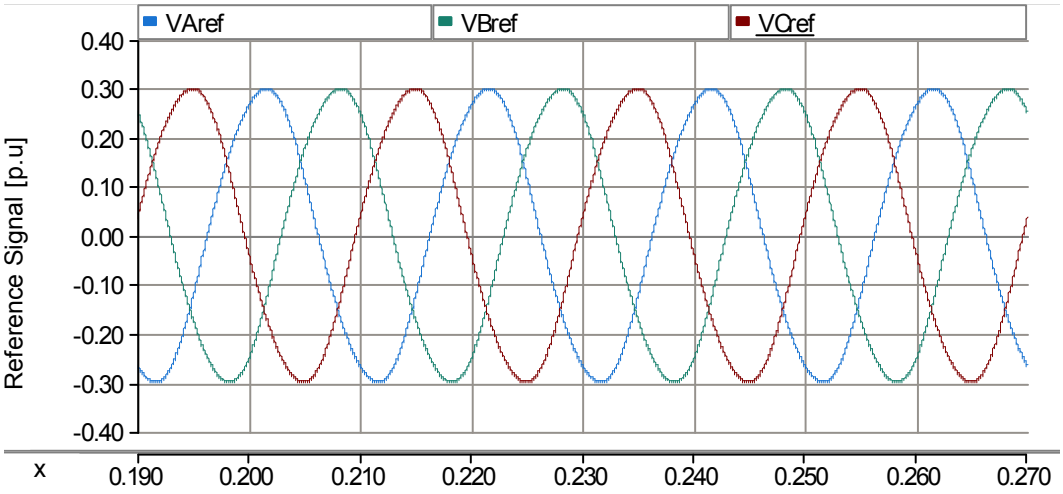


Fig.4.60: Reference voltages

The injected voltages by the DSSC devices through the three phase system and the corresponded line currents are plotted in Fig.4.61. It can be observed that in order to provide the required compensation the injected voltages only slightly vary depends on the line current. When the line current is less then injected voltage is high.

The proposed controller is a single phase controller and three phases are completely independent from each other. In this method each controller in each phase has no connection to the other phases and it does not sense or control three phase related components such as zero sequence component.

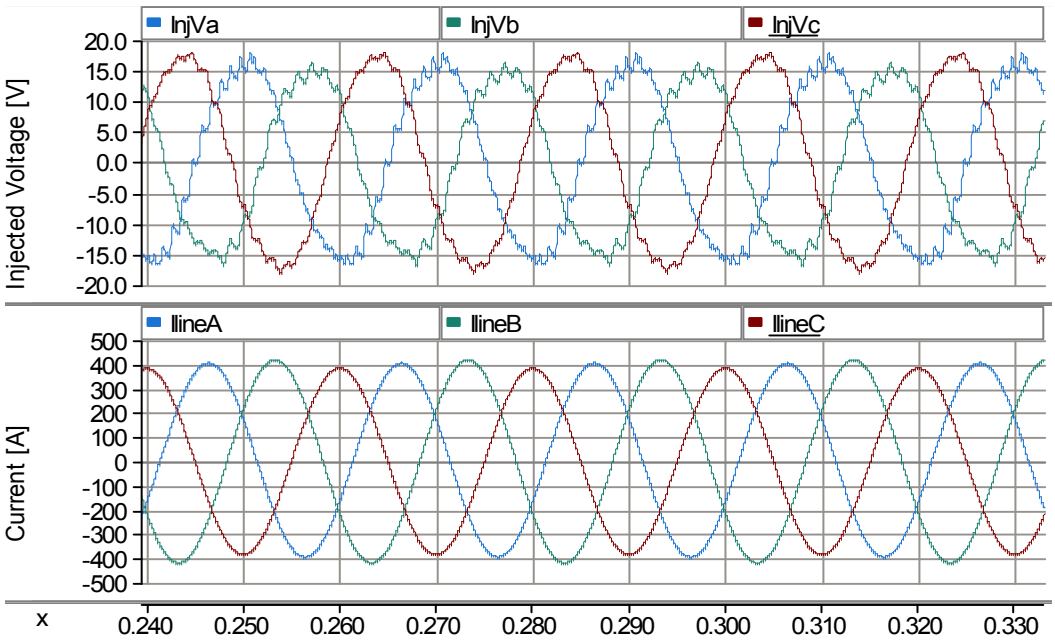


Fig.4.61: The injected voltages by DSSC devices and line currents

Injected harmonics by DSSC devices in each phase is demonstrated in Fig.4.62. Amplitude of injected 3rd harmonics is indicated below each figure. It can be observed that there are some other high order harmonics as well, however their amplitude is significantly low in comparison with the fundamental frequency.

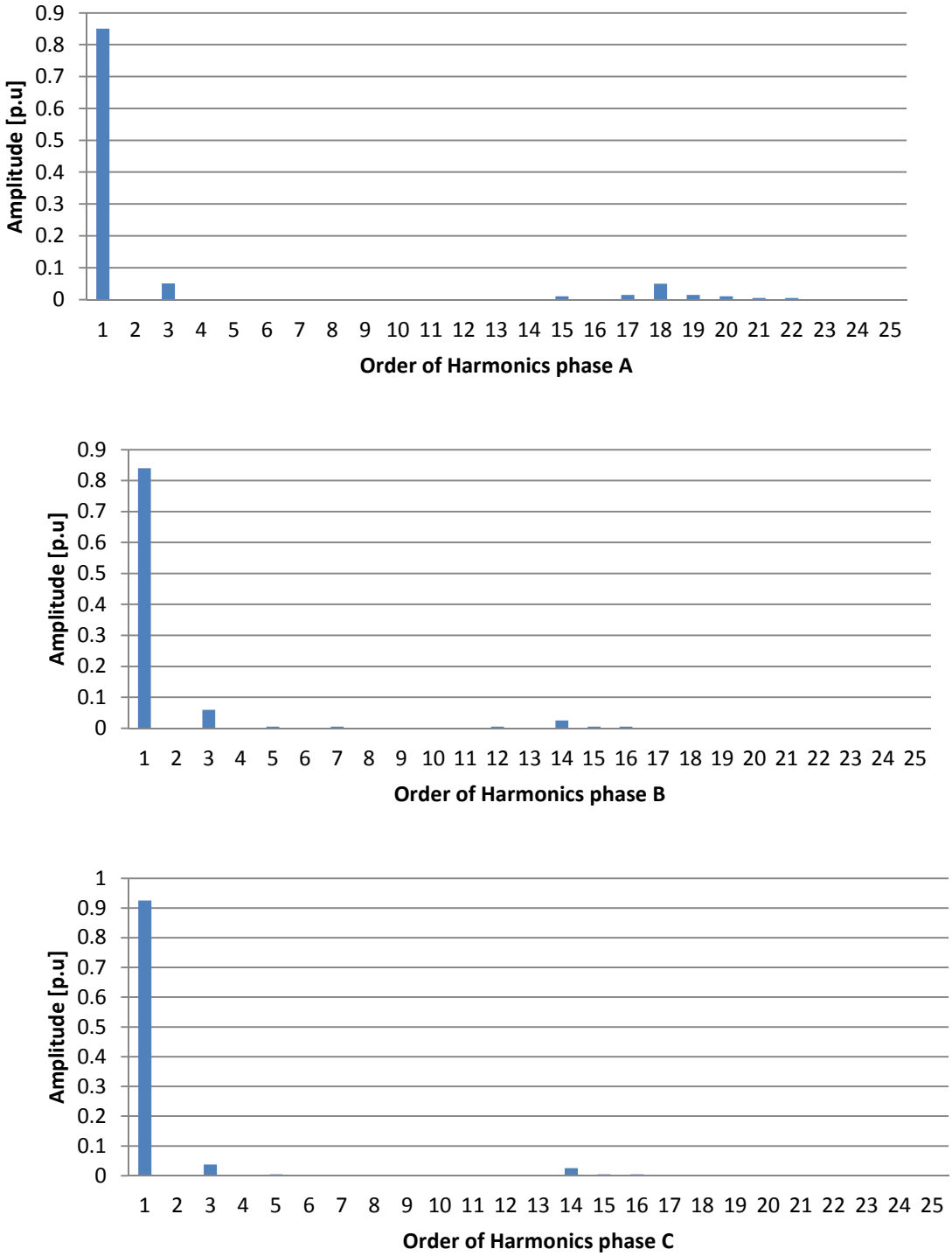


Fig.4.62: Injected harmonics in three phase

4.8.4 Performance of dq based controller within unbalanced three phase load

With the same three phase power system (including the same unbalance load as per pervious section) conventional dq controller has been employed within the DSSC devices.

PI controller dq based controller is designed and the obtained control parameters are tabulated in Table 4.8. The designed PI controller is used in the unbalanced three phase system regardless of percentage of system unbalance.

Parameters	Value
k_p	150
k_i	200
Time constant	0.005

Table 4.8: Control parameters

The regulated DC voltages in each phase, shown in Fig.4.63, are slightly different. It can be observed that the DC voltage in phase "a" is slightly lower than the voltage in phase "b" and "c".

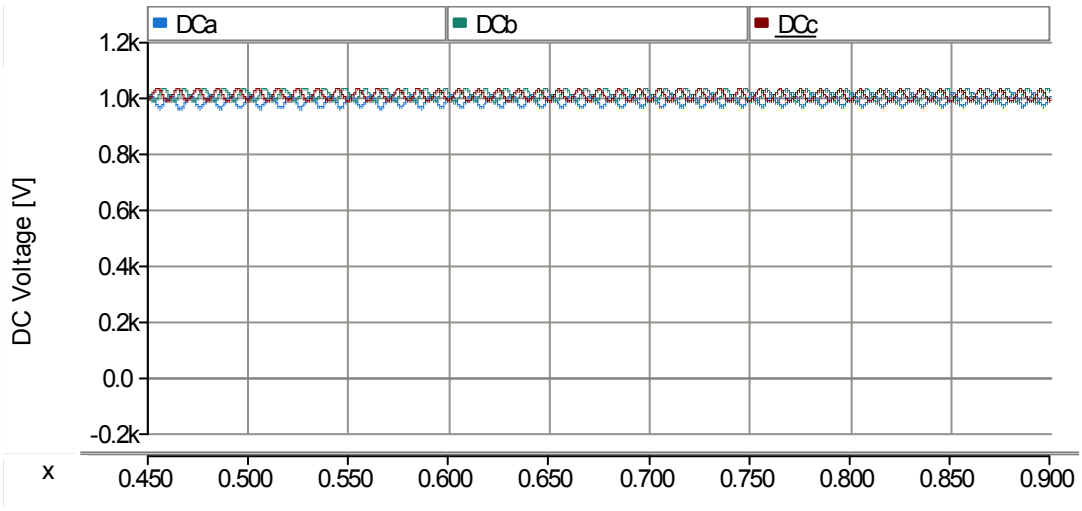


Fig.4.63: DC voltages in each phase

The dq components of line currents are shown in Fig.4.64. These components are oscillatory because the three phase system is unbalanced. Also I_{dqLine} which is calculated by (4.24) from dq components of three phase line currents is oscillatory. The dq components of the line current are used in producing reference signals by dq based controller. The generated reference signals for the three phases are shown in Fig.4.65. This figure shows that the amplitude of signals are different from each other and they have unbalanced amplitud.

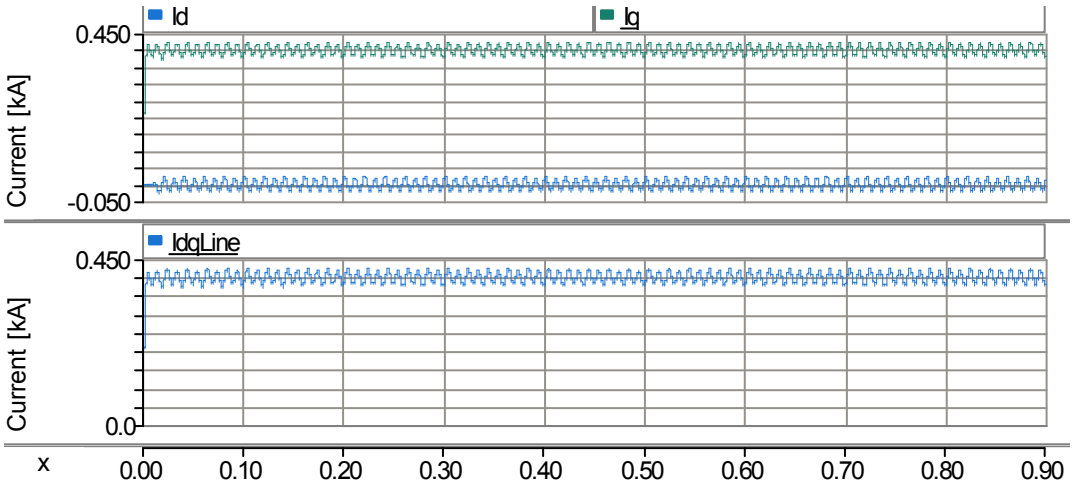


Fig.4.64: dq components and amplitude of the line current

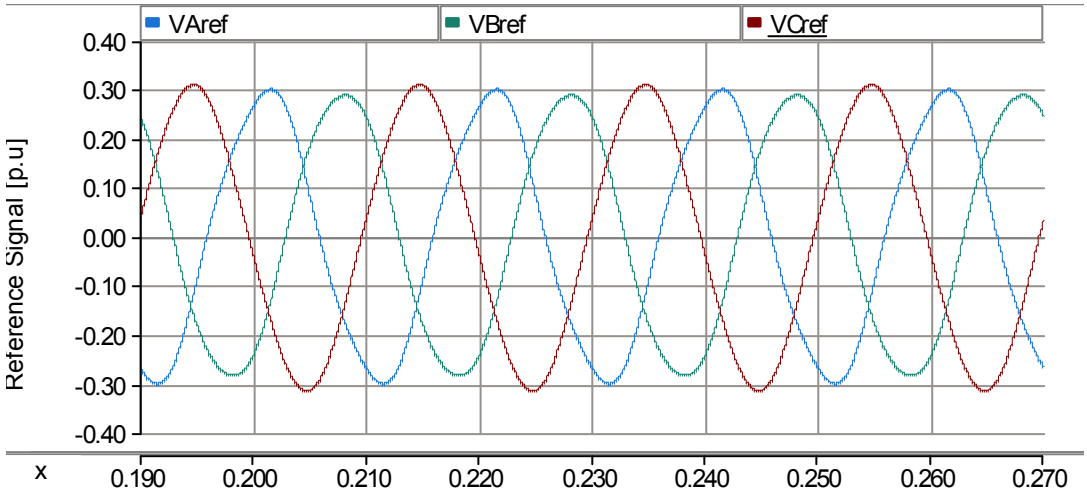


Fig.4.65: Reference signals generated by the dq based controller

The three injected voltages by DSSC devices using dq based controller in three different phases are shown in Fig.4.66. These voltages are unbalanced and distorted. For example injected voltage in phase “c” is higher in comparison with the other phases. This is an unbalance injection and it increases the unbalance of system. In another example injected voltage in phase “a” is more distorted than the injected voltage in other two phases.

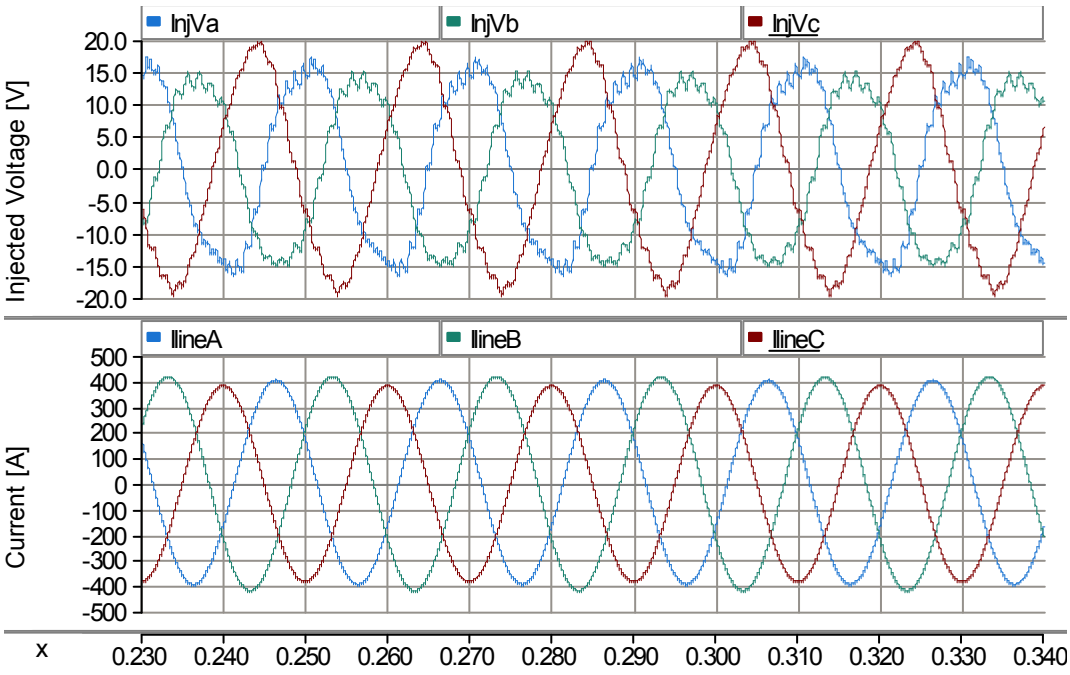
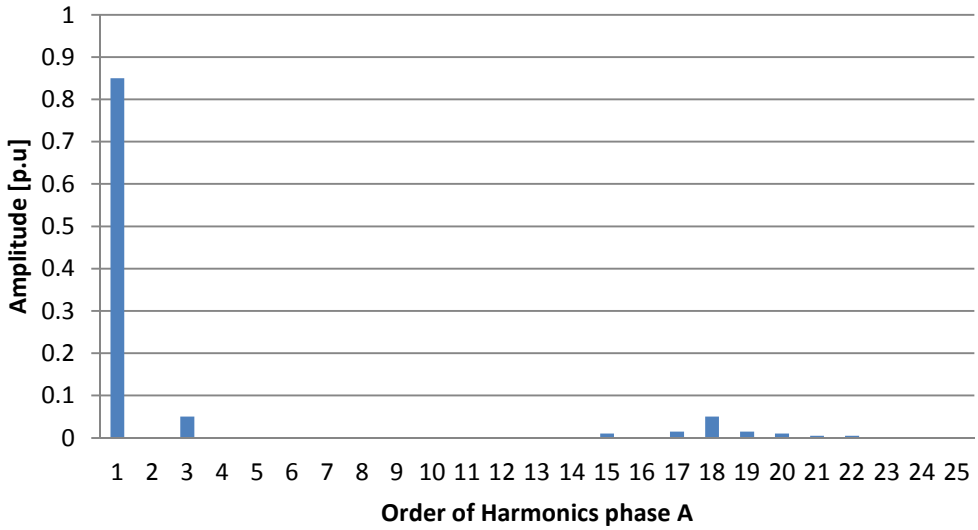


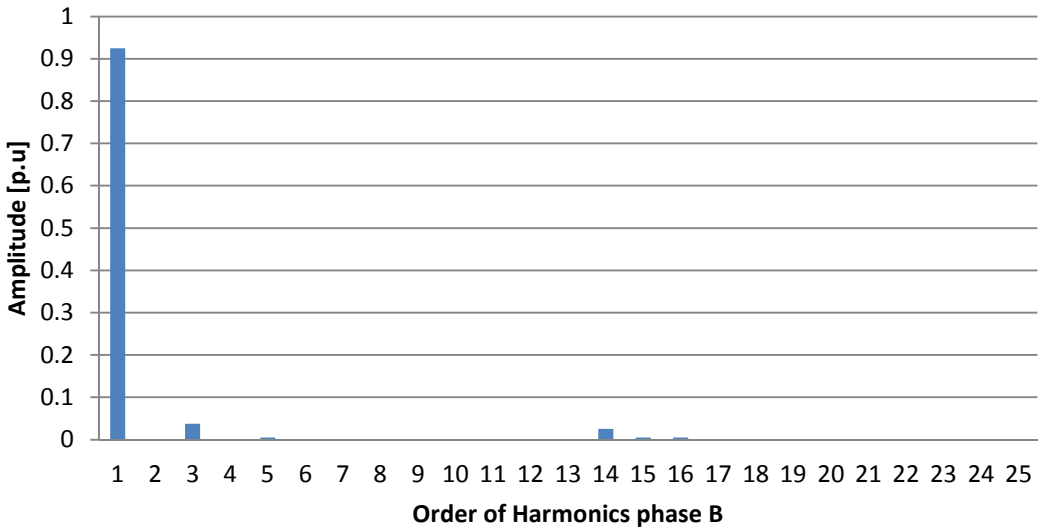
Fig.4.66: Injected voltage and line currents

The injected harmonics by the dq based controller in presence of unbalanced load is shown for each phase in Fig.4.67. The amplitude of injected 3rd harmonics is indicated below each figure. The presented value is compared with injected 3rd harmonics using a single phase controller (shown in Fig.4.62). Comparison between Fig.4.62 and Fig.4.67 shows that the amplitude of the harmonics is increased by almost 52%. For example in the case of phase "a" it is 1.01V in Fig.4.61 and it is 1.94V in Fig.4.67.
The controller uses dq component of three phase system and it does not sense or control zero sequence component.

When performance of dq based controller is compared with the proposed controller the followings difference can be identified:

- The reference signals in the proposed controller are not affected by the unbalance load while they are affected in the dq based controller.
- The injected voltage in the dq based controller is unbalance
- Amplitude of injected harmonics in the dq based controller is high (i.e. 3rd harmonic almost doubled)





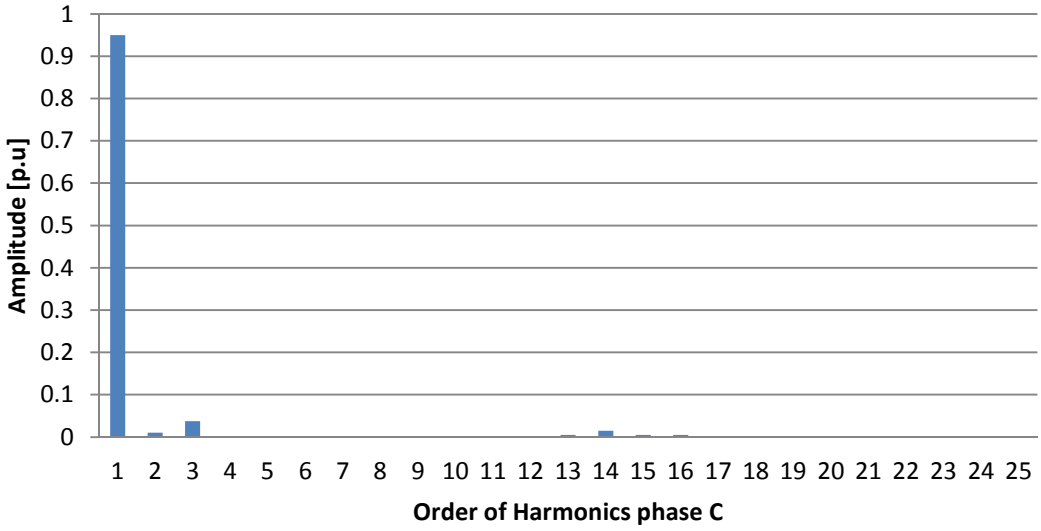


Fig.4.67: Injected harmonics in three phase

4.8.5 *Performance of proposed controller in presence of unbalance three phase system*

Performance of the proposed single phase controller has been investigated within an unbalance three phase system. The amplitude of voltages, as shown in Fig.4.68, are different in each phase and the system is supplying a 6MW balanced load.

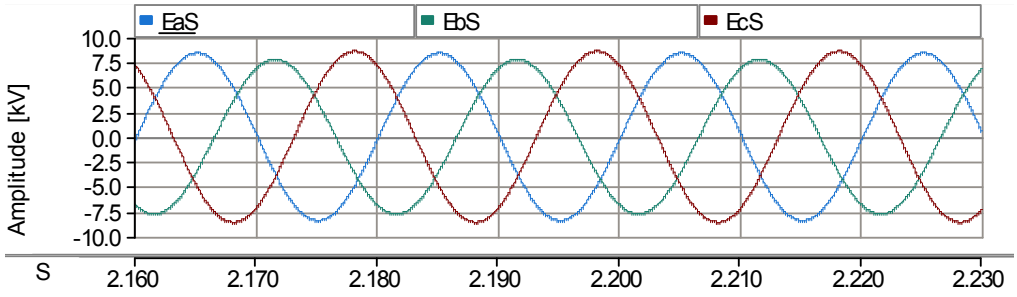


Fig.4.68: Amplitude of each phase in the unbalance system

Despite a balance load (in the previous section effect of unbalance load has been investigated) the supplied current become unbalance and this is shown in *dq* representation of load current in Fig.4.69. In this plot it can be observed that there is an oscillation in the I_d and I_q which is an indication for an unbalance system. Amplitude of I_{dqLine} is calculated by root square of I_d plus I_q (dq component of three phase line current) and it is shown by in Fig.4.69.

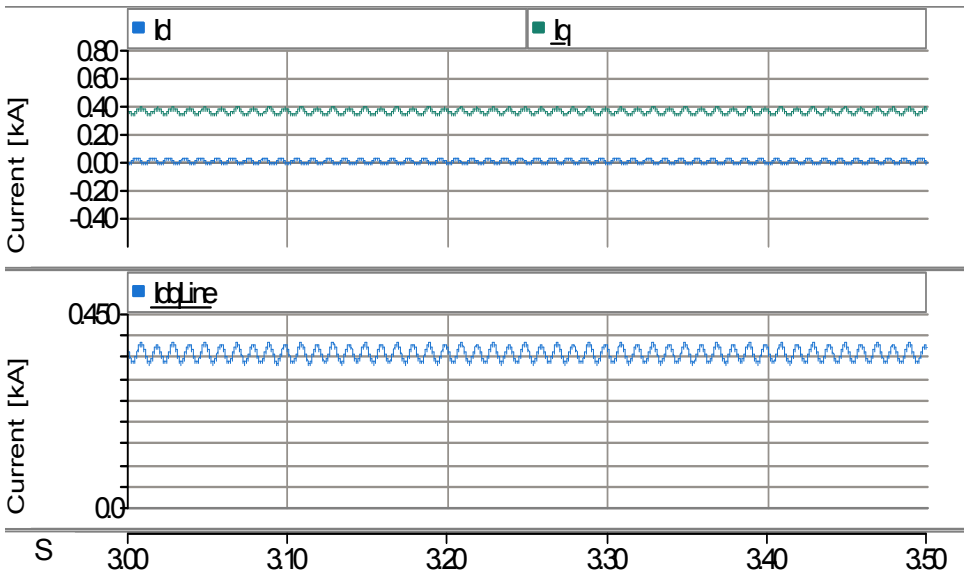


Fig. 4.69: dq representation of load current

Calculated reference signals by single phase controllers in each phase are shown in Fig.4.70. Despite the unbalance system voltage and unbalance load current the generated signals are identical.

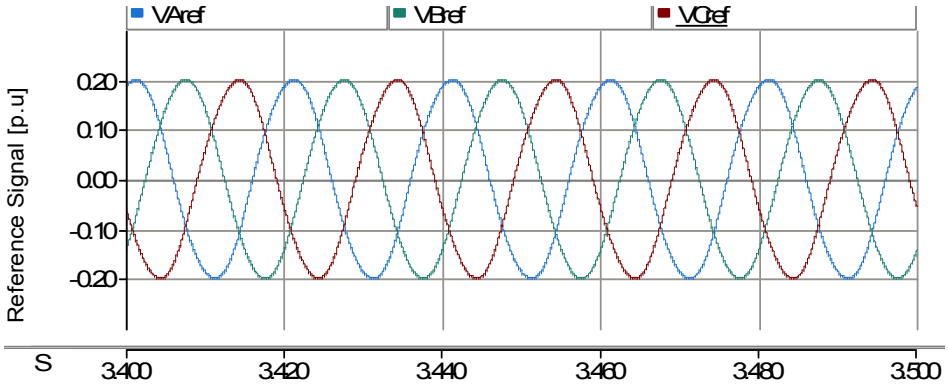


Fig.4.70: Reference signals generated by single phase controller

Injected voltage by DSSC and line current is shown in Fig.4.71. This figure shows that regardless of unbalance current and voltages in the three phase system, DSSC is able to inject same voltages in each phase. This shows that the DSSC device in each phase can execute reference signal without involving with two other phases.

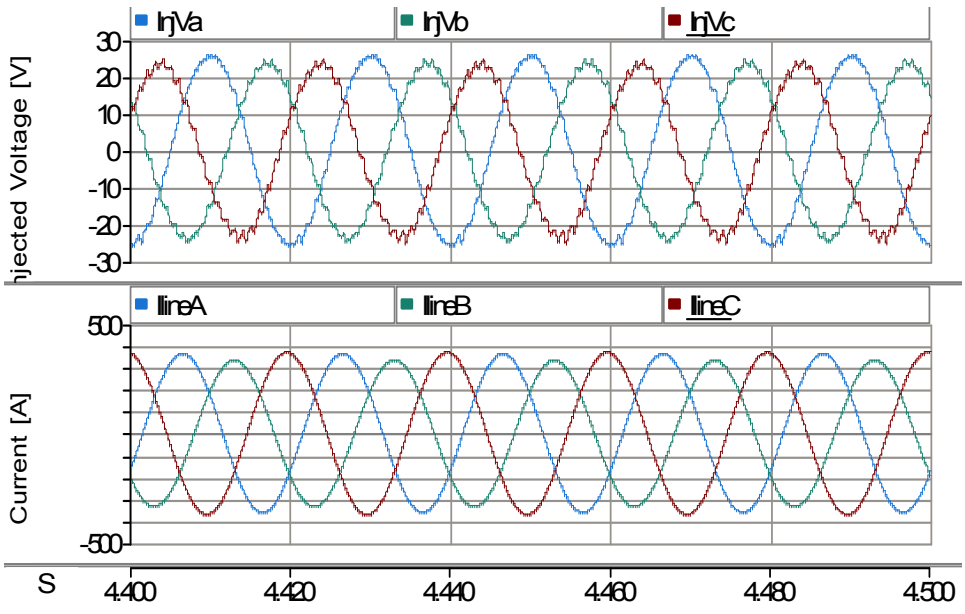


Fig.4.71: Injected voltage by DSSC and line current within unbalance system.

Each DSSC device can hold the demanded DC voltage across its own DC capacitor independently. This is shown in Fig.4.72 for each phase of system.

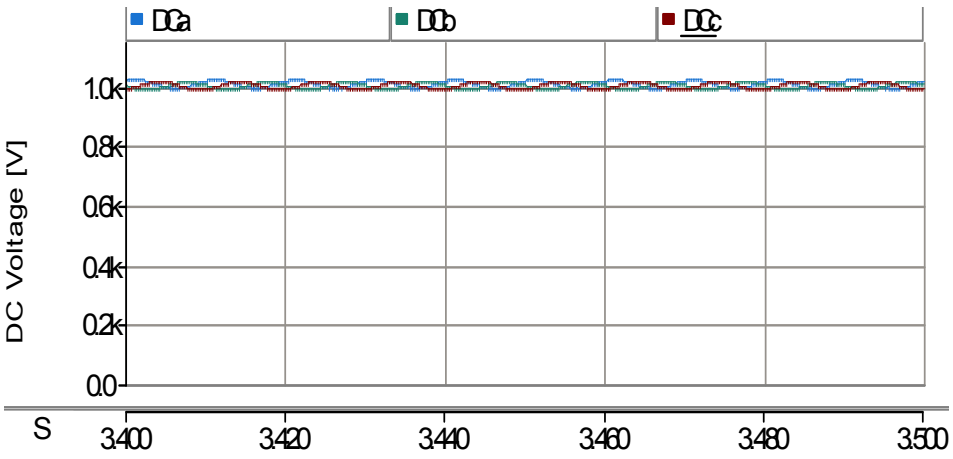


Fig.4.72: Voltages across DC capacitors

Injected harmonics by each DSSC in three phases are shown in Fig.4.73 for phase “a”, “b” and “c”. The spectrums of harmonics show that the injected harmonics are almost same.

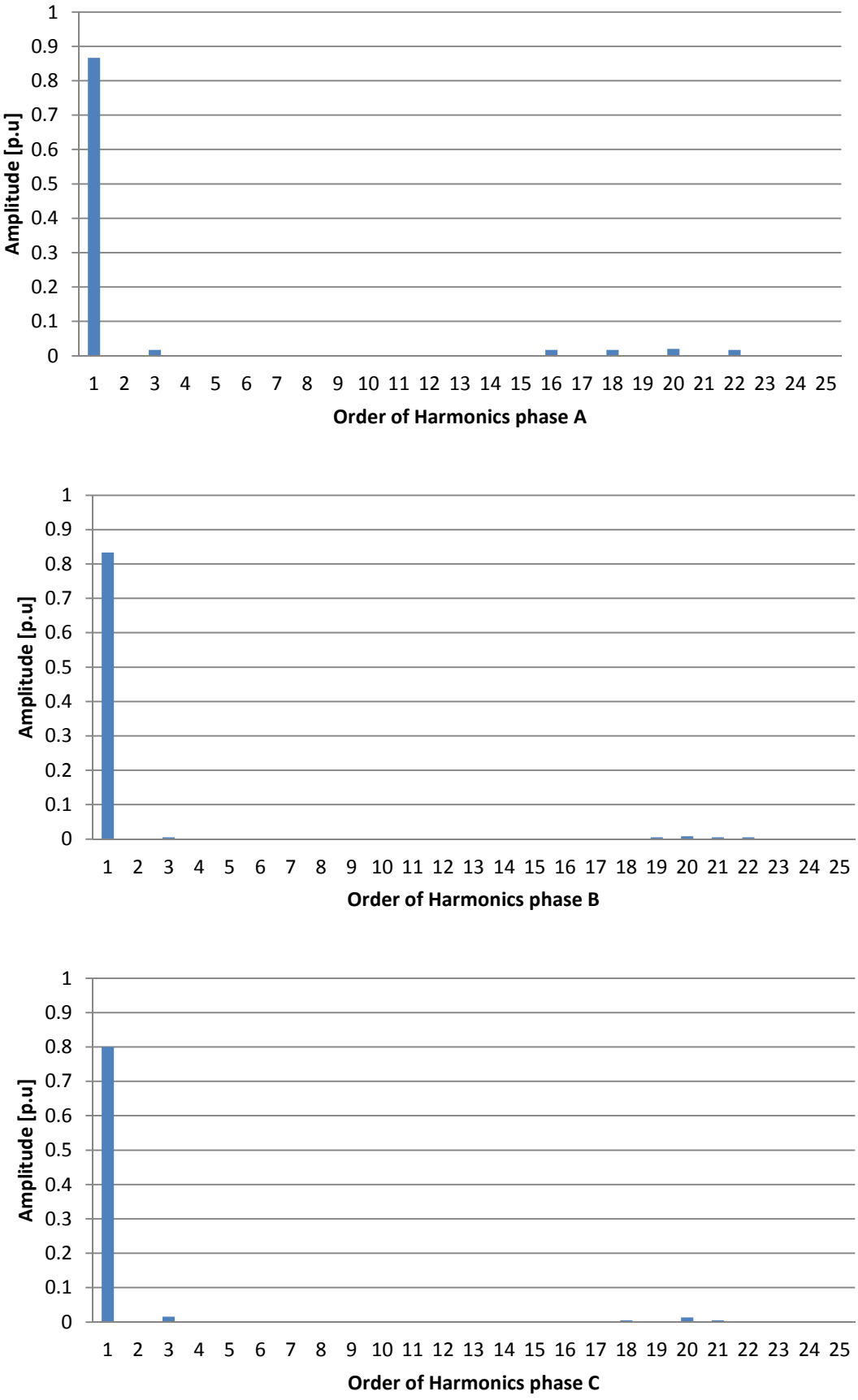


Fig.4.73: Spectrums of injected harmonics by single phase controller in an unbalanced system

4.8.6 *Performance of dq based controller in presence of unbalance three phase system*

Performance of *dq* based controller has been examined in presence of an unbalanced system. This is the same three phase system which has been used in pervious subsection which performance of the single phase controller has been investigated with. Voltage of three phase system is shown previously in Fig.4.68 it shows that system has three different voltages in each phase. Furthermore, *dq* components of the three phase line currents because of presence of unbalance are oscillatory as shown in Fig.4.69.

Generated reference signal by the *dq* based controller is shown in Fig.4.74 and unbalance of three phase voltage can be observed easily.

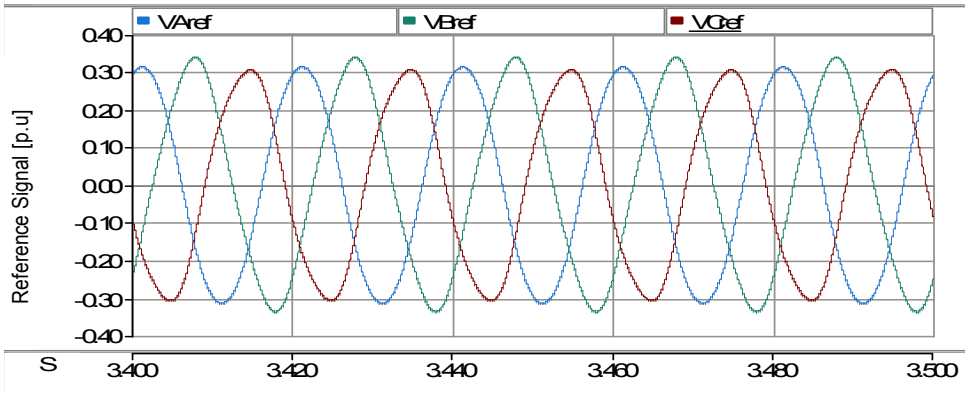


Fig.4.74: Generated reference signal by the dq based controller

Fig.4.74 shows that generated reference signal is affected by unbalance of system. However in pervious subsection by using proposed single phase controller the generated reference signals, as shown in Fig.4.70 are identical.

Injected voltage by DSSC and line current when *dq* based controller has been used are shown in Fig.4.75. This shows that injected voltage is unbalance and its value for each phase is different.

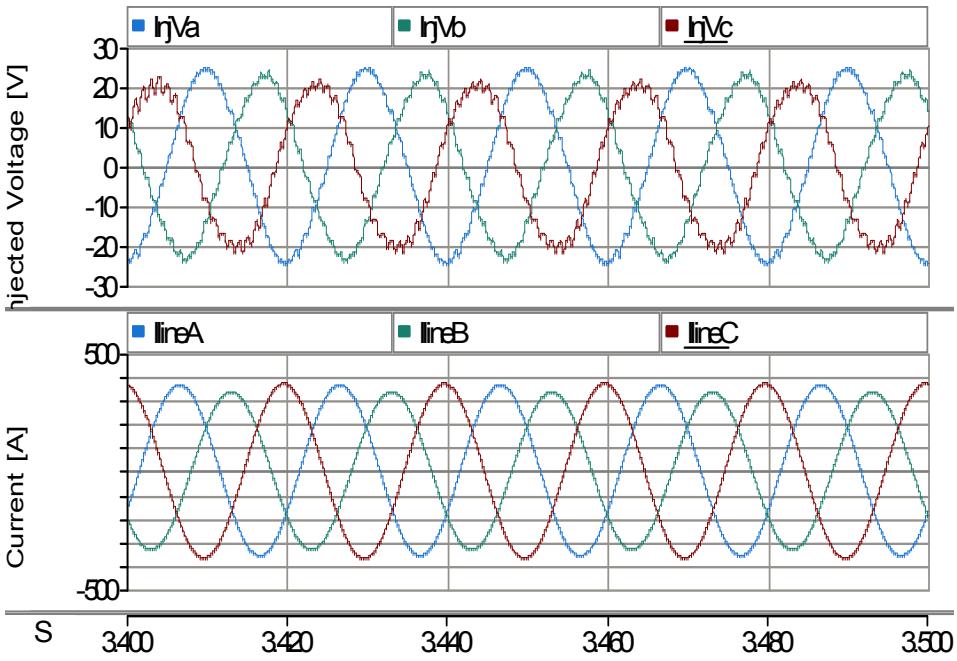


Fig.4.75: Injected voltage by DSSC using dq based controller

Injected voltage by DSSC using *dq* based controller is different for each phases while it is almost identical (as shown in Fig.4.71) when the proposed single phase controller has been employed.

Using the *dq* based controller in an unbalanced system is able to regulate the voltage across the DC capacitor as shown in Fig.4.76.

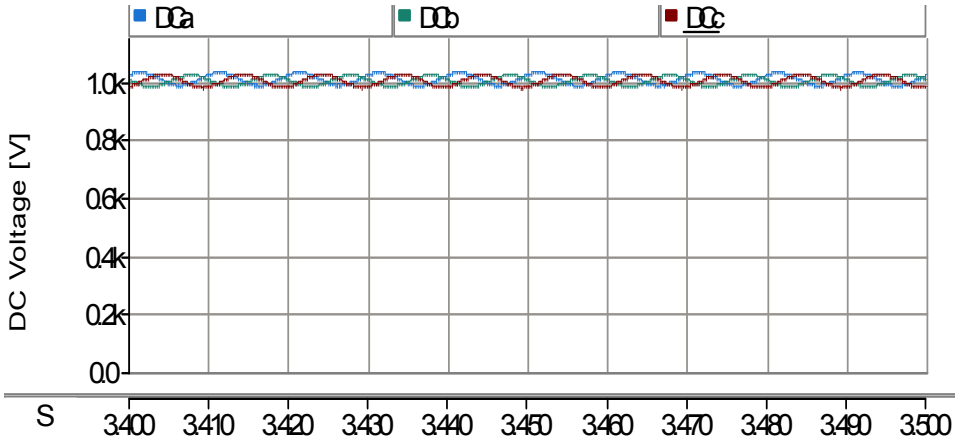
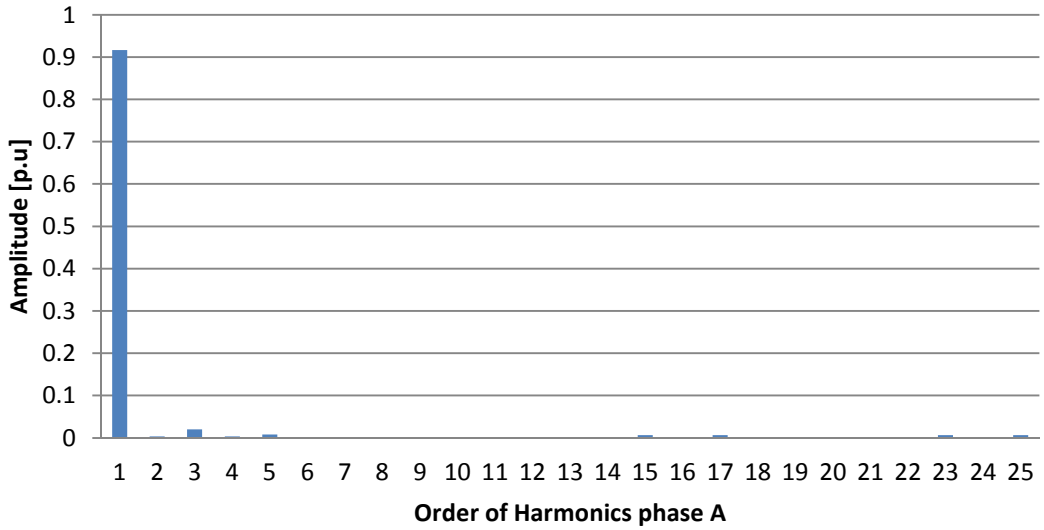
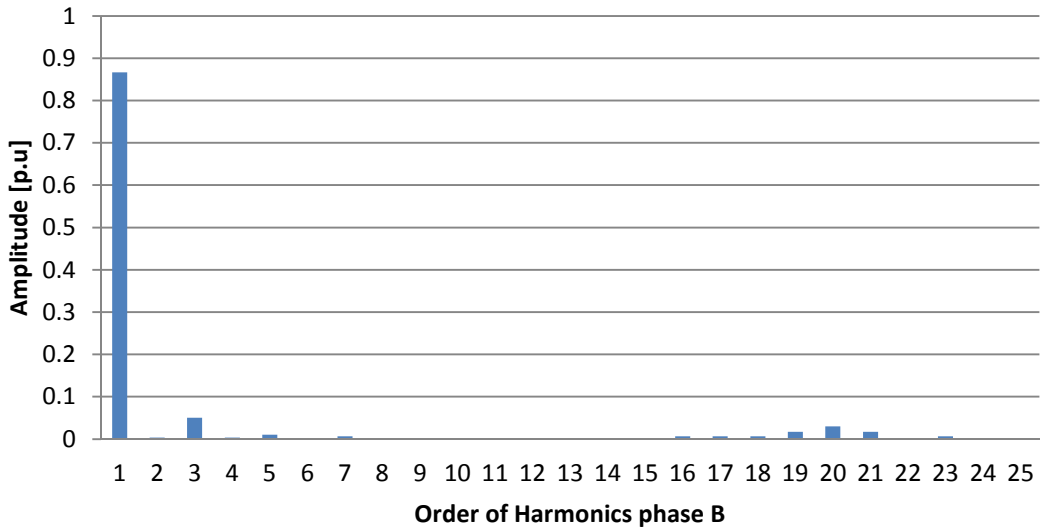


Fig.4.76: Voltage across the DC capacitor using the dq based controller in an unbalanced system

Comparing Fig.4.72 with Fig.4.76 shows almost no difference between the regulated voltages across the DC capacitor when single phase controller and *dq* based controller has been used respectively.

Injected harmonics for three different phases by DSSC when a *dq* based controller has been used are shown in Fig.4.77.





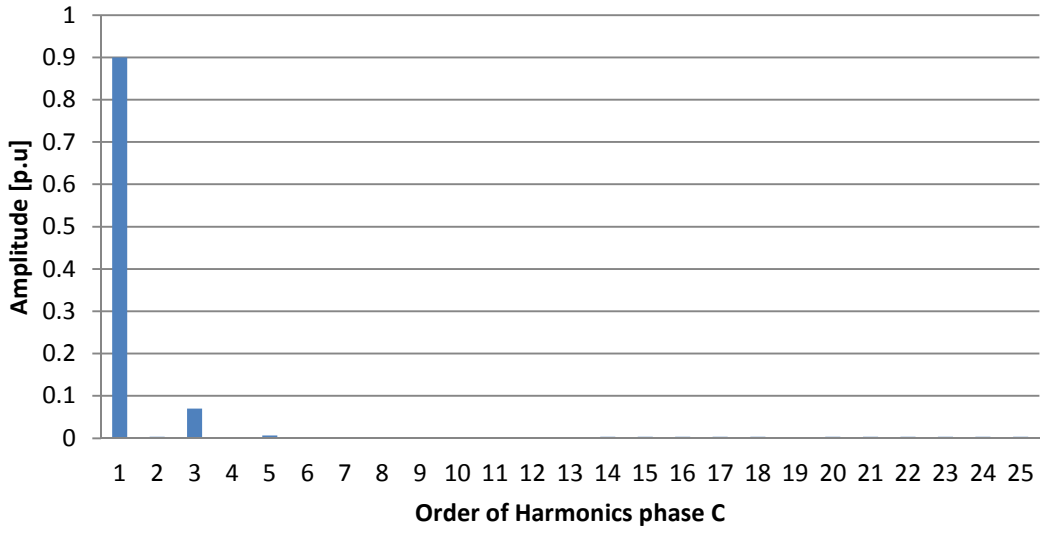


Fig.4.77: Spectrums of injected harmonics by dq based controller in an unbalanced system

Comparing spectrums of injected harmonics by two controllers shows that amplitude of third harmonics using *dq* based controller is boosted almost ten times in phase B and four times in phase C.

4.9 Comparing the performance of proposed controller with using only a DC link voltage controller

Performance of DSSC using only DC voltage controller and proposed controller has been compared. In Fig.4.78 concept of both controllers have been presented and it has been shown that only one controller can be selected in a time by using contrller selector. This figure provides blockdiagramatic comparsion between the two controllers. As it can be clearly observed that conventional controller (only DC voltage controller) recieves only error of DC voltage as an input and consequently it controls only this parameter. However in proposed controller (located inside the green dasht line) in order to provide reference signal not only the error of DC voltage is being taken into account but also the error of injection angle has been considered. It means that proposed controller, controls both injection angle and DC voltage. The proposed controller in absense of phase difference signal is the same as the convetional controller. The conventional controller alone can adjust the DC voltage however the injection angle can be sacrifised. This is because it controls only the DC voltage and tries to keep the DC voltage as close as possible to refrence value. In this approach injection angle is not in priorety and it is used by DC voltage controller to provide required active power to hold the DC voltage.

However the injection angle itself in DSSC device is required to be kept fixed and as close as possible to 90° and it needs to be considered by the controller. By adding the phase difference (which is shown in green in Fig.4.78) in the proposed controller both DC voltage and injection angle will be considered.

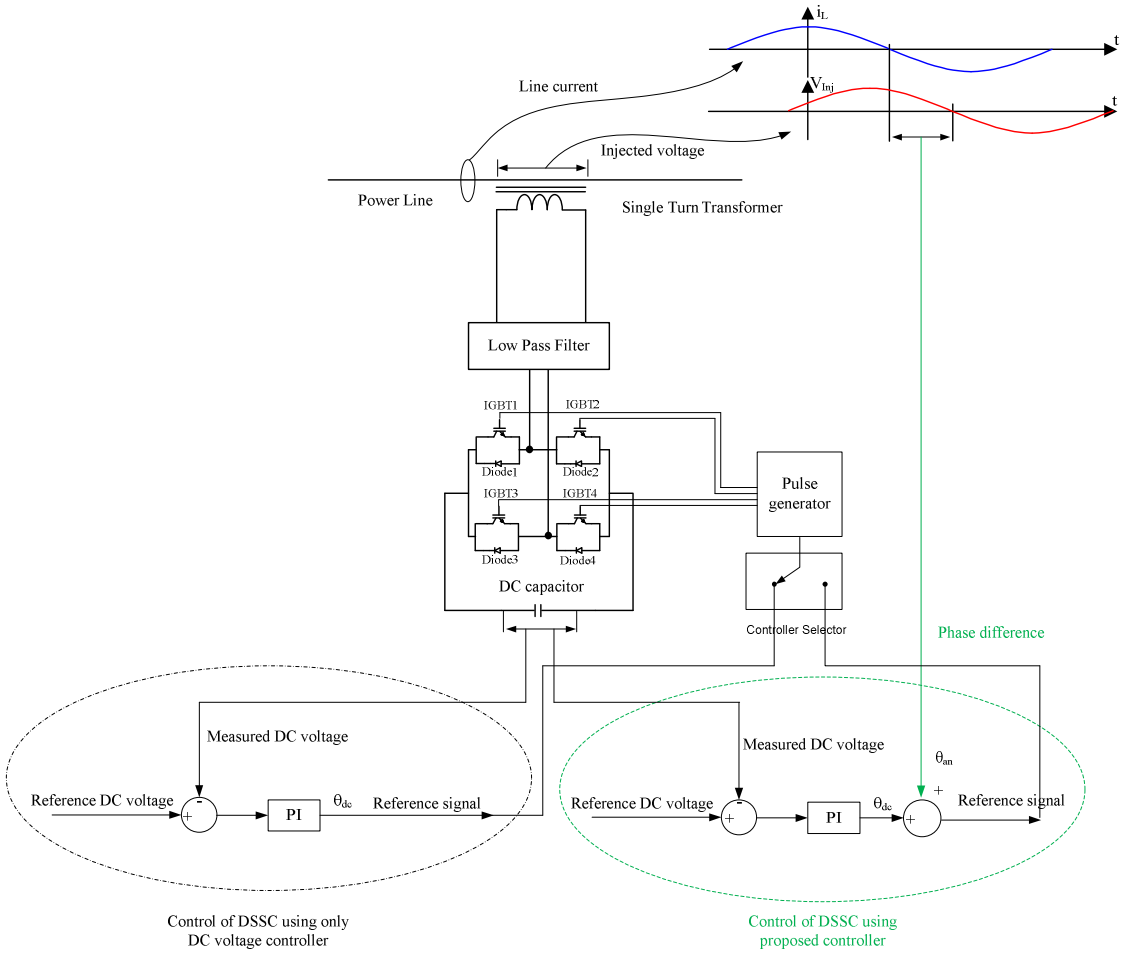


Fig.4.78: Comparison between the proposed controller and DC voltage (only) controller

4.9.1 Performance of the device using voltage regulator only

DC regulator alone can be used to hold the DC voltage in DSSC device and inject series voltage through the line. DC voltage controller is an optimaly tuned PI contoller using root locus approach.

In the DC voltage controller as shown in Fig.4.1 controller regulates the voltage across the DC capacitor. Transfer function of DSSC device is shown by *G* in the block diagram and it is represented in (4.25)

$$G = \frac{V_{cdc}}{u} = \frac{1.6e^{-7}S}{3.2e^{-15}S^4+1.2e^{-7}S^2+1} \qquad (4.25)$$

Root Locus diagram of *G* is shown in Fig.4.79. There are two branches that move to the positive side and the system is unstable.

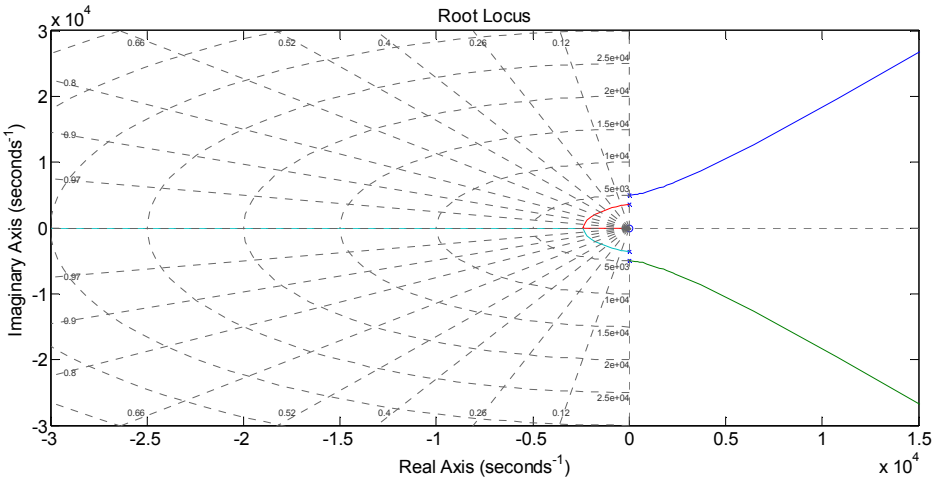


Fig.4.79: Root Locus diagram of G

A controller is needed to be designed to stabilize the system and meet the requirements which are tabulated in Table 4.9. The requirements in this table are chosen in a way to be consistent with other designed controllers in this chapter.

Parameter	Value
Overshoot	Less than 5%
Damping	0.9

Table 4.9: Requirements for the designed controller

By inserting a zero and pole the Locus is changed as shown in Fig. 4.80. The change of Locus is not guaranteeing that the controller is meeting the requirements. The step response of the system needs to be seen in order to evaluate the system performance. The step response is plotted in Fig. 4.81 and it shows high oscillation in response.

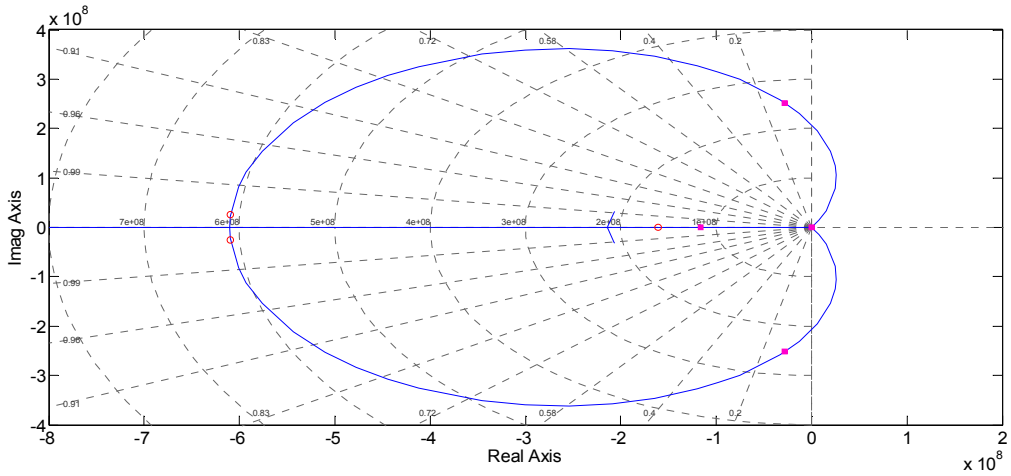


Fig. 4.80: Root Locus with inserted zero and pole

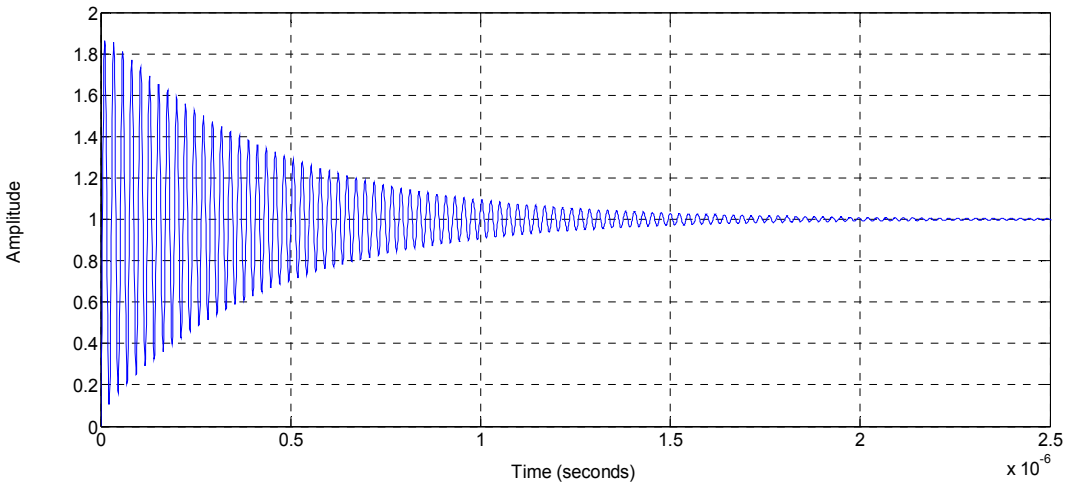


Fig. 4.81: Step response with inserted zero and pole

In order to eliminate the oscillation the inserted zero needs to be relocated in a way to improve the step response. To do so, inserted zero is moved further right to -1.34 and the corresponding Root Locus diagram is plotted in Fig. 4.82.

For overshoot of less than 5% and damping factor of 0.95 the corresponded gain of 150 can be obtained from Root Locus in Fig. 4.82. By including the selected gain in the controller the corresponding step response of the system is plotted in Fig. 4.83. It can be observed that peak of overshoot reaches to 1.04 and there is no oscillation before settling down and reaching steady state.

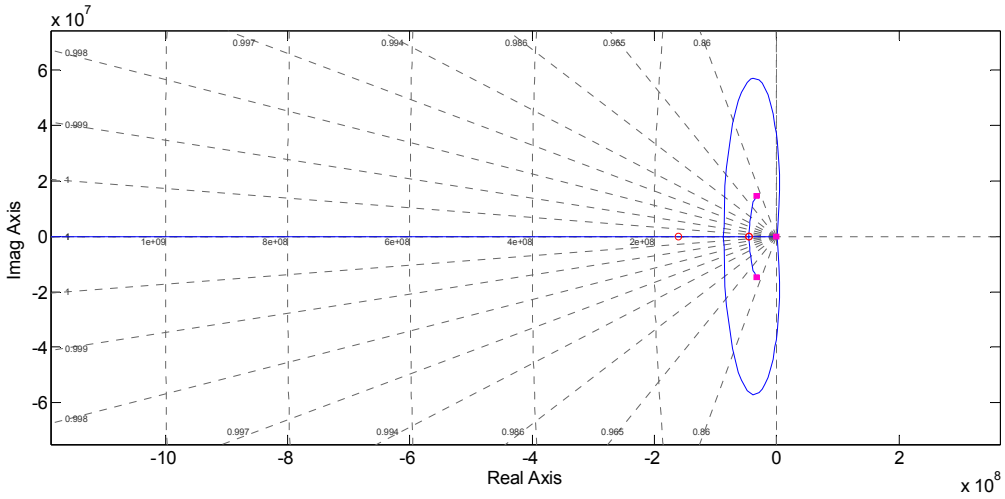


Fig. 4.82: Root Locus when inserted zero is moved further to the right

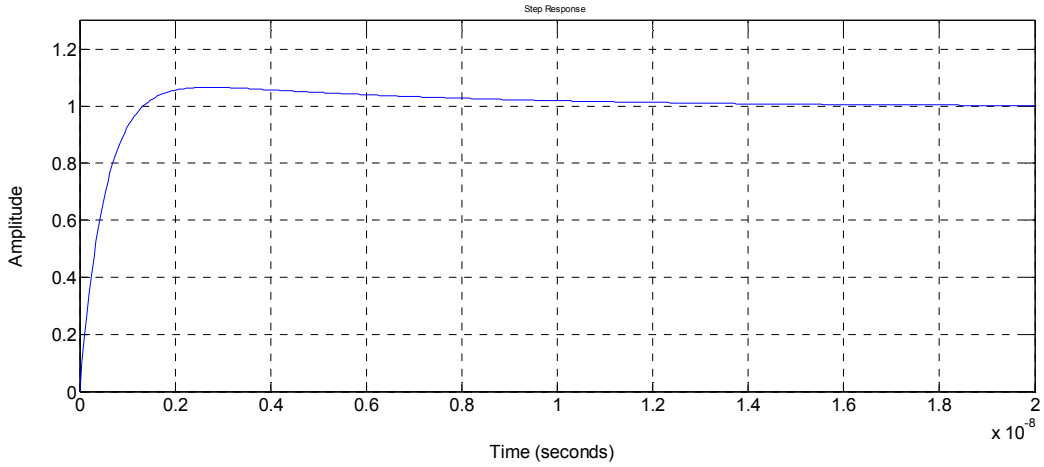


Fig. 4.83: Step response of the system when inserted zero is moved further to the right

Parameters of the PI controller are calculated in (4.26) by comparing the inserted pole and zero with the transfer function of controller. The inserted zero and pole are -1.34 and 0 respectively and the gain is 150 (from Root Locus).

$$\frac{150(s+1.34)}{s} = \frac{(k_p s+k_i)}{s} \qquad (4.26)$$

From (4.26) k_p and k_i are obtained 150 and 200 and tabulated in Table 4.10.

Parameters	Value
k_p	150
k_i	200

Table 4.10: Parameters of PI controller

The injected angle (phase difference between injected voltage and line current) in each phase by DSSC devices is presented in Fig. **4.84**. The angle is varying in order to regulate the DC voltage and for phase "A" the variation is around 95.85°. It means that it is deviated from 90° by 5.85°.

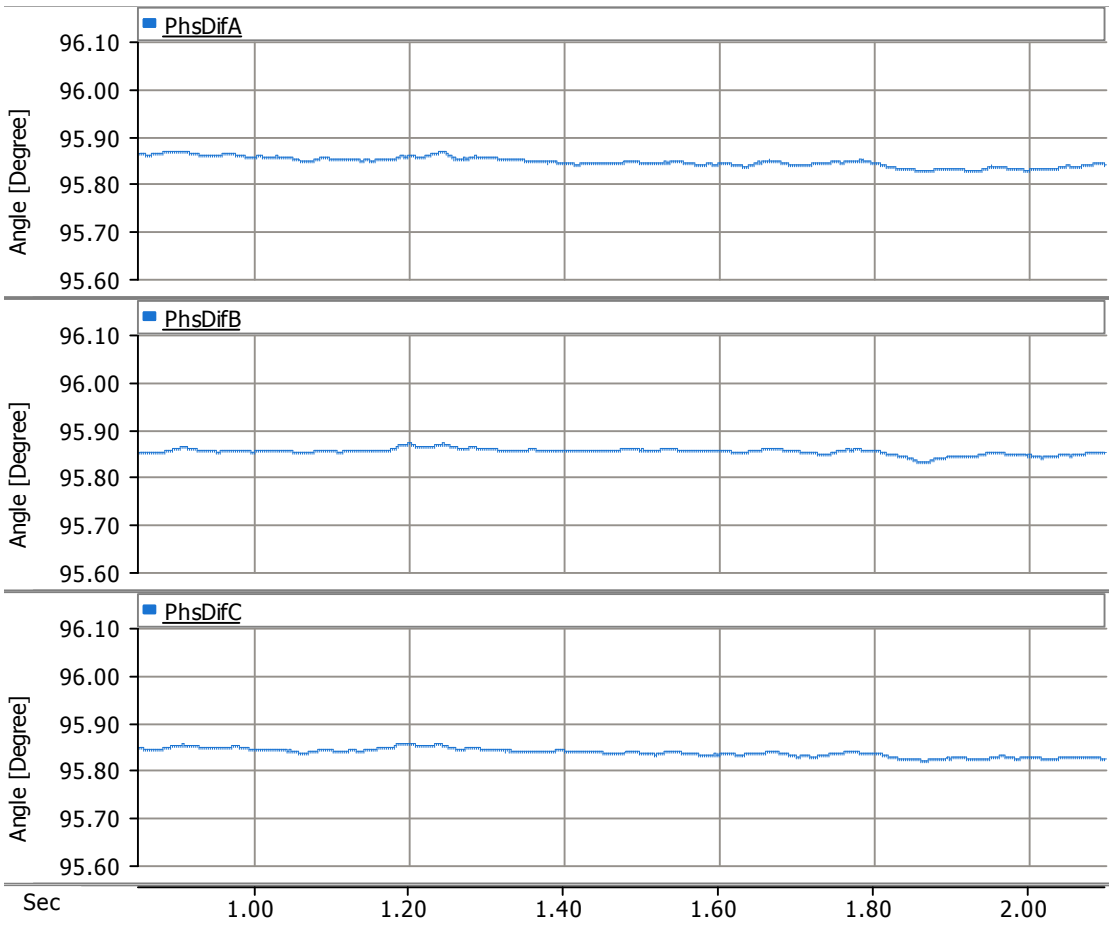


Fig. 4.84: Phase difference between injected voltage and line current in each phase

Obviously, the aim of this controller is just to adjust the voltage across the DC link and it has no direct control on the angle of injected voltage.

The DC voltage using voltage regulator only, is plotted in Fig.4.85 for three different phases. In steady state the voltage in DC link of each DSSC devices varies between 977V and 1020V and amplitude of rippel is 43V.

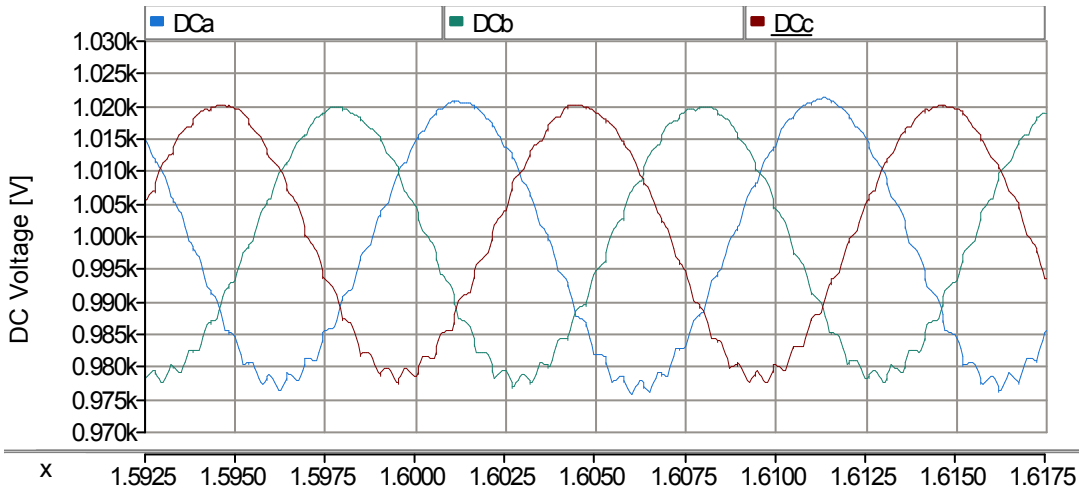
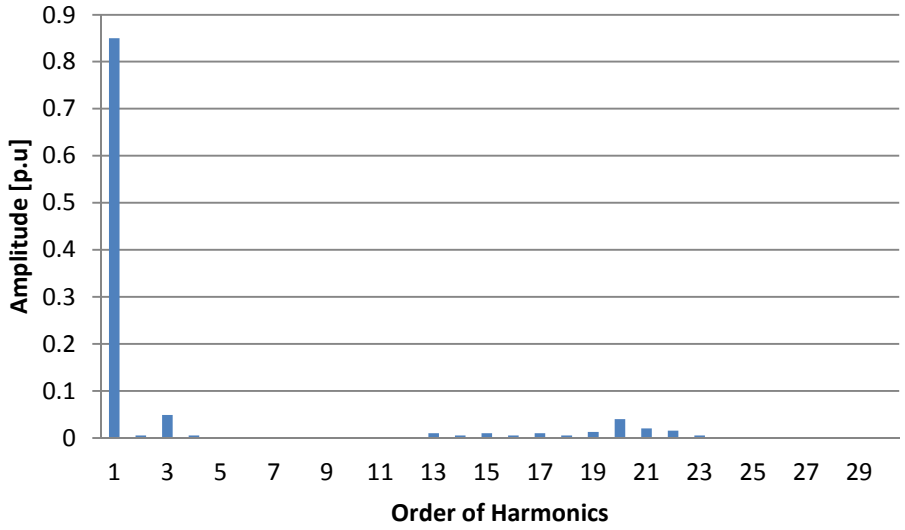
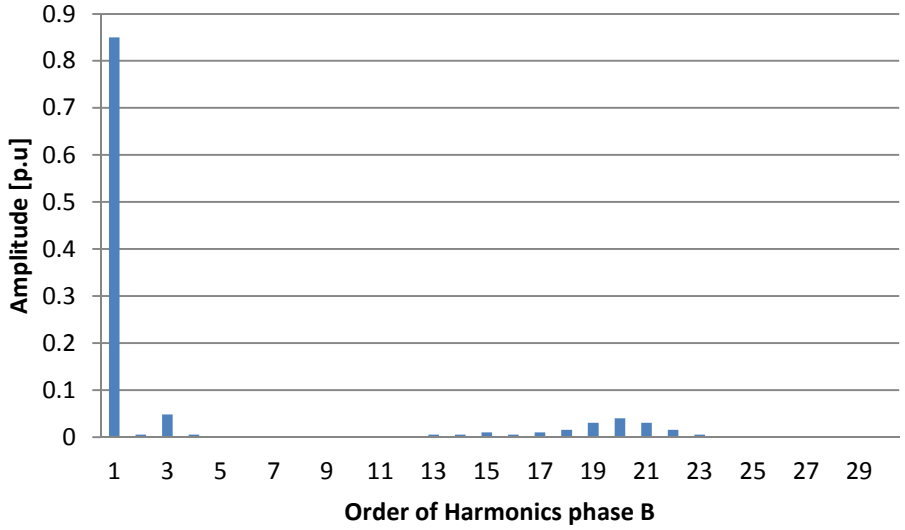


Fig.4.85: DC voltages in three different phases

The injected harmonics by DSSC device are plotted in Fig.4.86. The harmonic spectrum shows that, along with the fundamental frequency the device injects some other harmonics such as 3^{rd} and 20^{th}. Total harmonic distortion (THD) of injected voltage is 5%.

Amplitude of the 3^{rd} harmonics is indicated below each harmonic spectrum for each phase. For example in phase "A" amplitude of 3^{rd} harmonic is 0.98V.





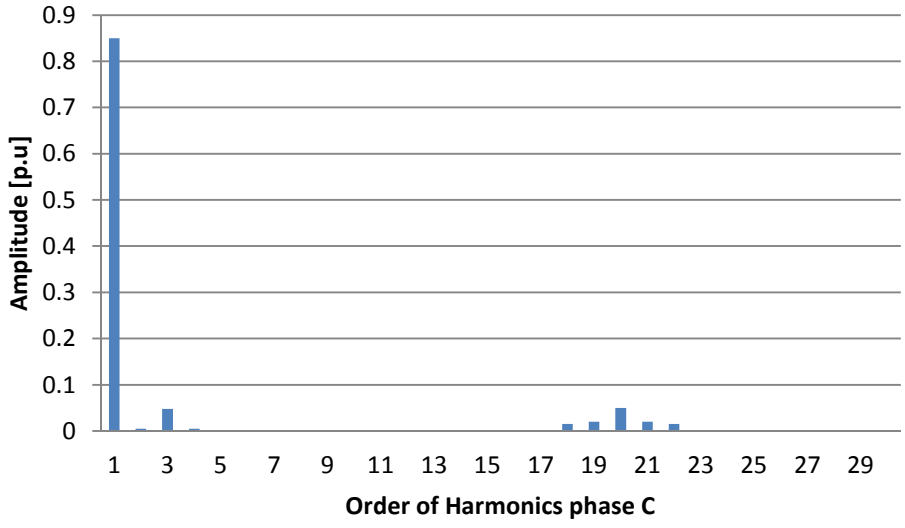


Fig.4.86: Injected harmonics by DSSC device

The PI controller gain is changed at different values around the optimally obtained value (150 as per Table 4.10) in order to investigate the effect of different gains on the performance of system. The changes in the gain values affect the ripples of DC voltages and the injected angle. Depends on if the gain is increased or decreased the obtained results can be different. Fig. 4.87-Fig.4.94 show the obtained results for ±10% change of the gain.

In Fig. 4.87 the voltage across the DC link has been increased as the gain of PI controller is increased by 10%. The peak voltage increased from 1.02 kV to 1.03 kV and the ripple is 75V. The increment of ripples amplitude as a result of increasing the gain is not a desirable effect.

The injection angle is presented in Fig. 4.88 and it shows that the angle is improved as result of higher gain when it is compared with Fig. 4.84. The angle is reduced from 95.9° to 95.7° and it is a desirable effect.

The injected harmonics by DSSC device is represented in Fig. 4.89. By comparing the amplitude of harmonics with the harmonics plotted in Fig.4.86 it can be observed that amplitude of injected harmonics is slightly increased and THD is obtained 5.2%.

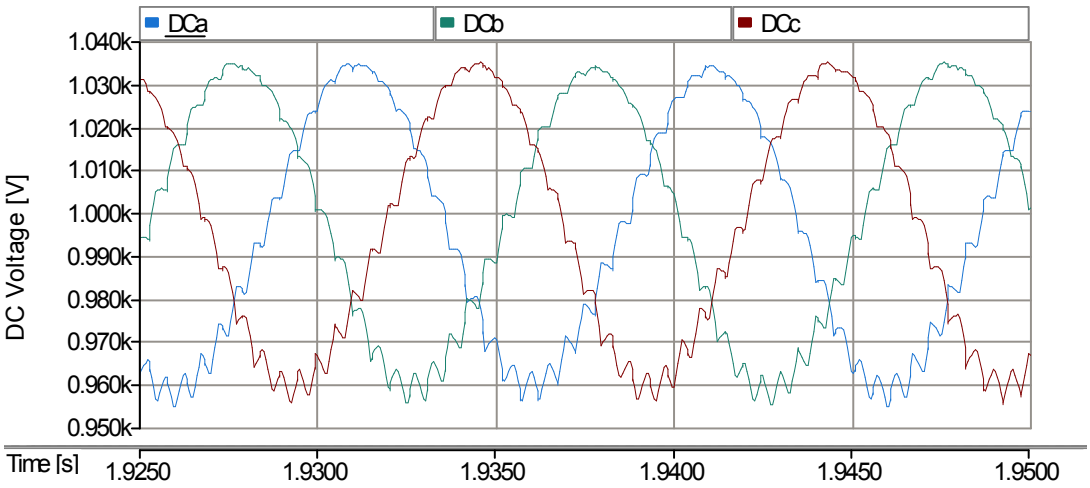


Fig. 4.87: Voltages across the DC capacitor when the PI gain is increased

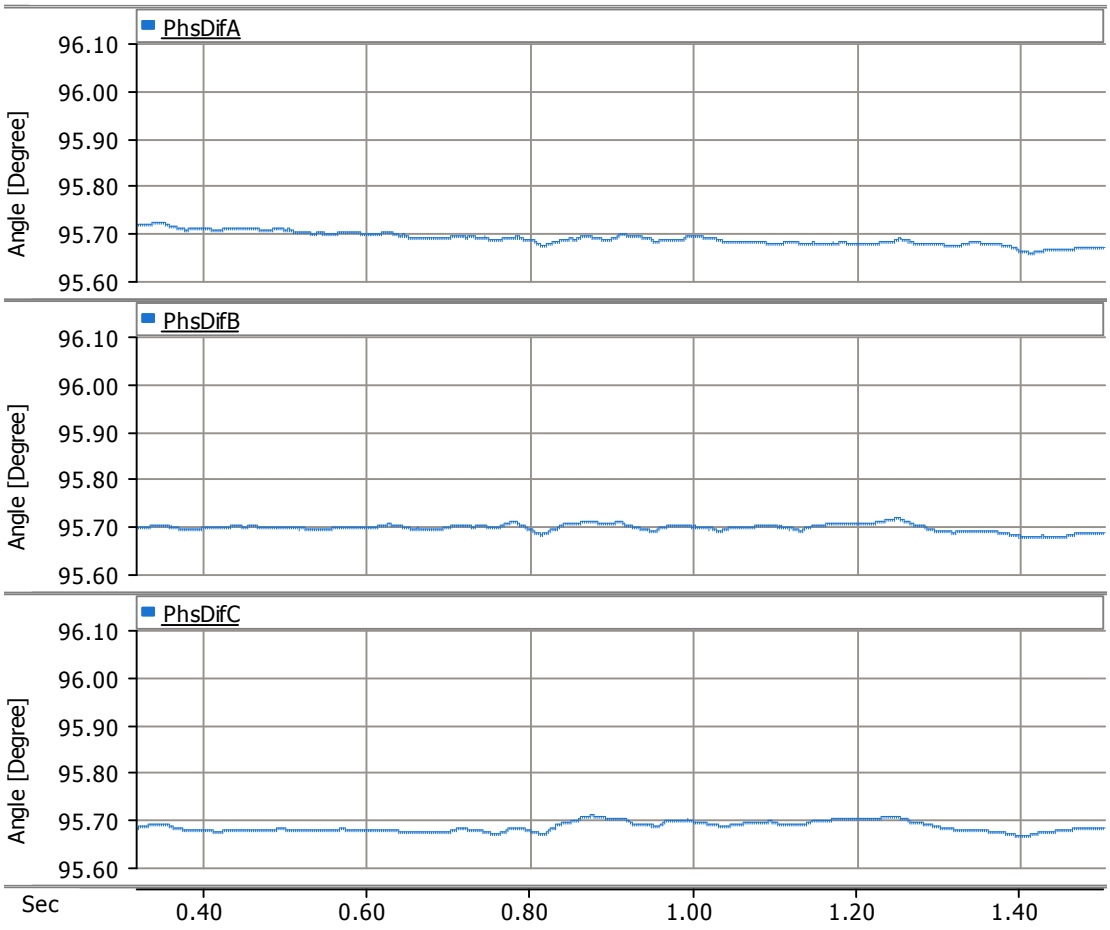
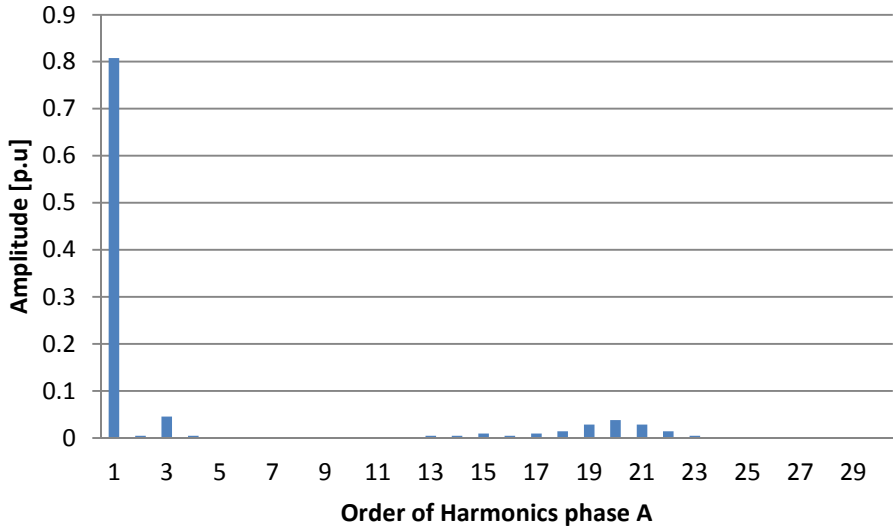
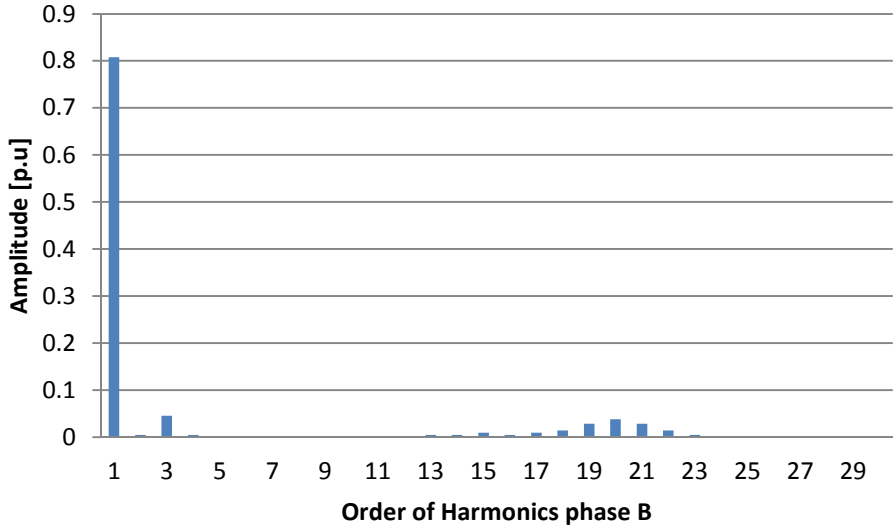


Fig. 4.88: Injection angle when gain in the PI controller is increased





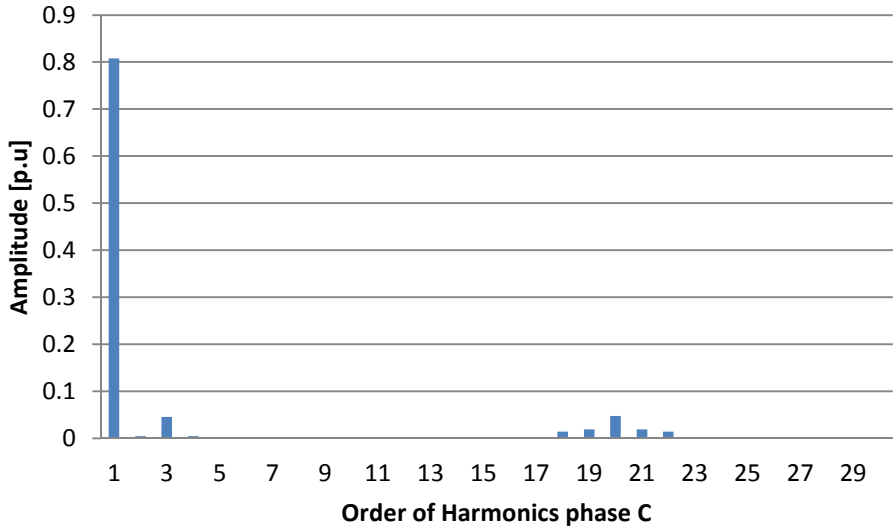


Fig. 4.89: Order of harmonics when gain of controller is reduced

In order to investigate the effect of reducing of the gain in the PI controller the gain has been reduced by 10%. The ripple of DC voltage is reduced and the reduction is noticeable when it is compared with the DC voltage presented in the Fig. 4.90. The peak of ripples is reduced from 1.02kV to 1.009 kV and the ripple is 19V.

In addition, the reduction of gain also can affect the injection angle of voltage. The angle is show in Fig. 4.91 and in comparison with Fig. 4.84 it can be observed that it is increased from 95.85° to 95.93°.

The injected harmonics by DSSC device is shown in the Fig. 4.92. Comparing the amplitude of the harmonics with corresponding one in Fig.4.86 shows slightly improvement in the injected harmonics and THD is 4.85%.

Studying the change of gain demonstrate that it can improve voltage or injection angle but it does not grantee to enhance both in the same time.

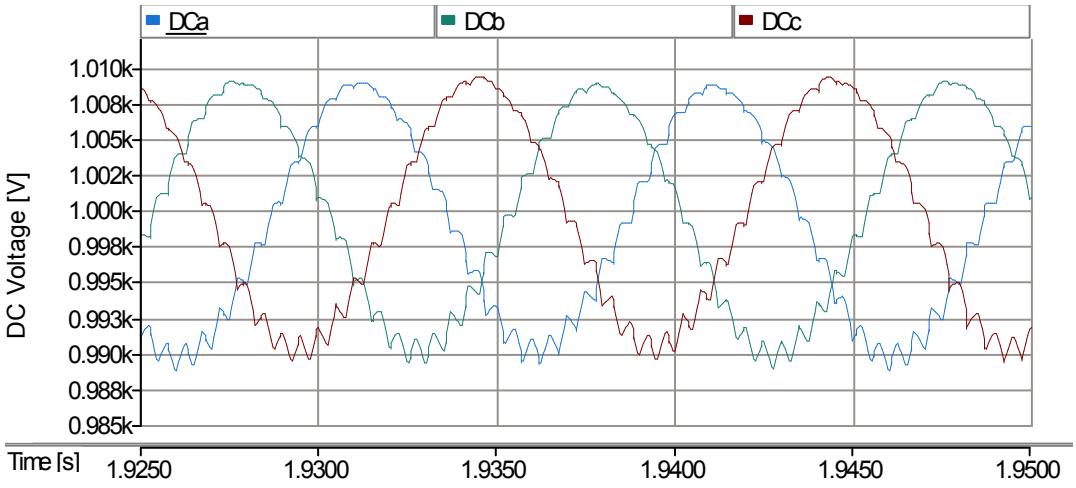


Fig. 4.90: Voltages across the DC capacitor when gain the PI controller is reduced

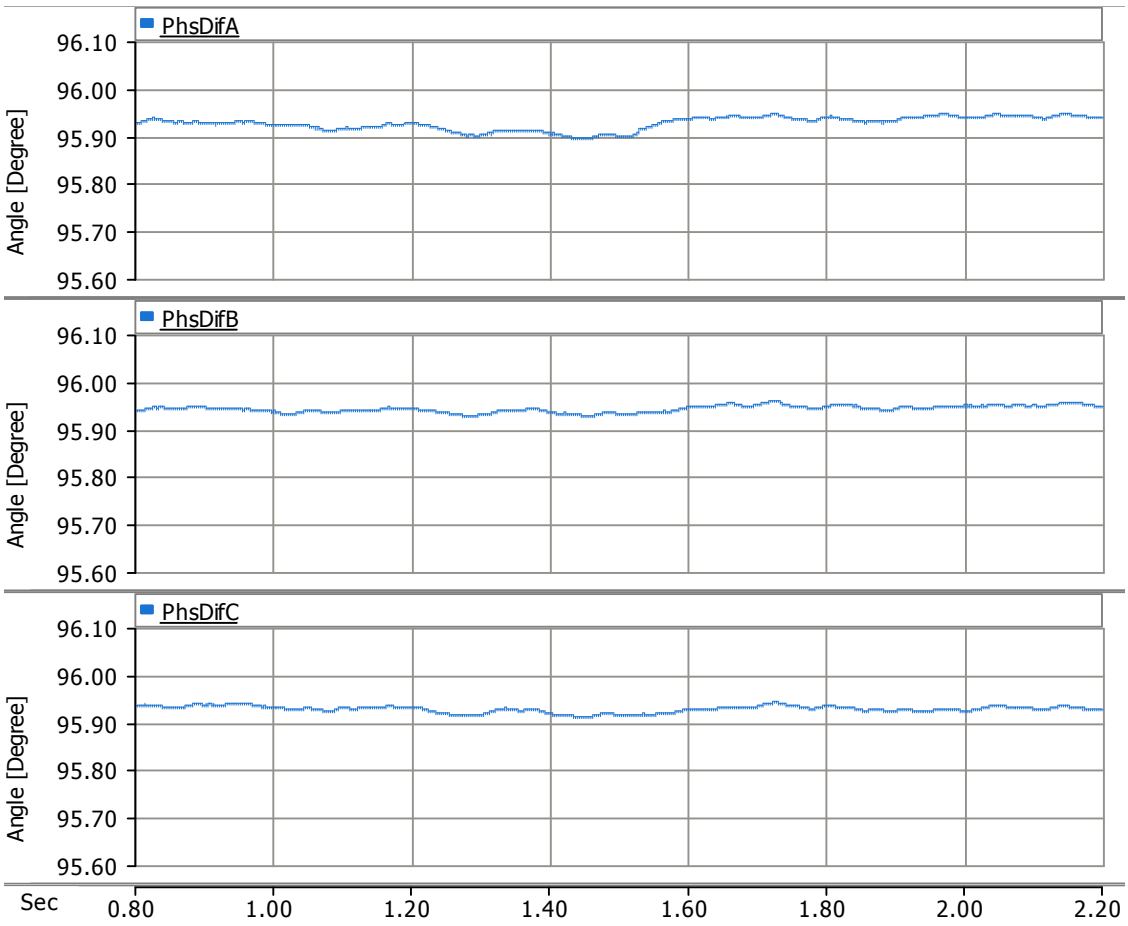


Fig. 4.91: Injection angle when gain the PI controller is reduced

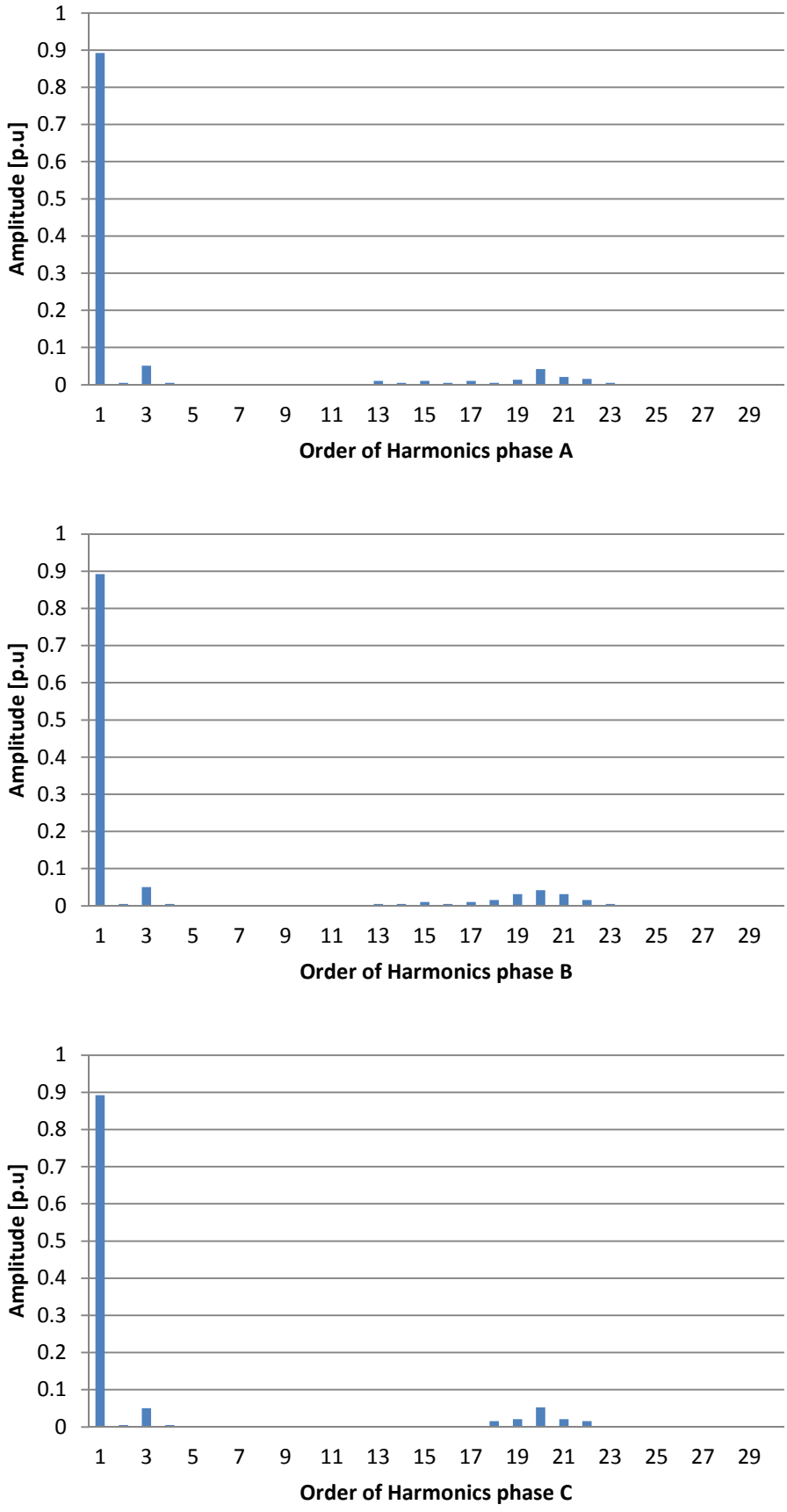


Fig. 4.92: Order of harmonics when gain of controller is increased

4.9.2 *Performance of the device using proposed controller*

DC voltage controller can be re-tuned (fine tuning) to improve ripples or reduce deviation of injection angle. This requires fine tuning parameters of PI controller however proposed controller considers both DC voltage adjustment and angle of injection in the same time. It is expected that the ripple of voltages to be lower and angle of injection to be closer to the 90° by employing the proposed controller. By further tuning the proposed controller it can be observed that the angle of injection is reduced to 95.05°. The angle of injection in each phase is plotted in Fig.4.93.

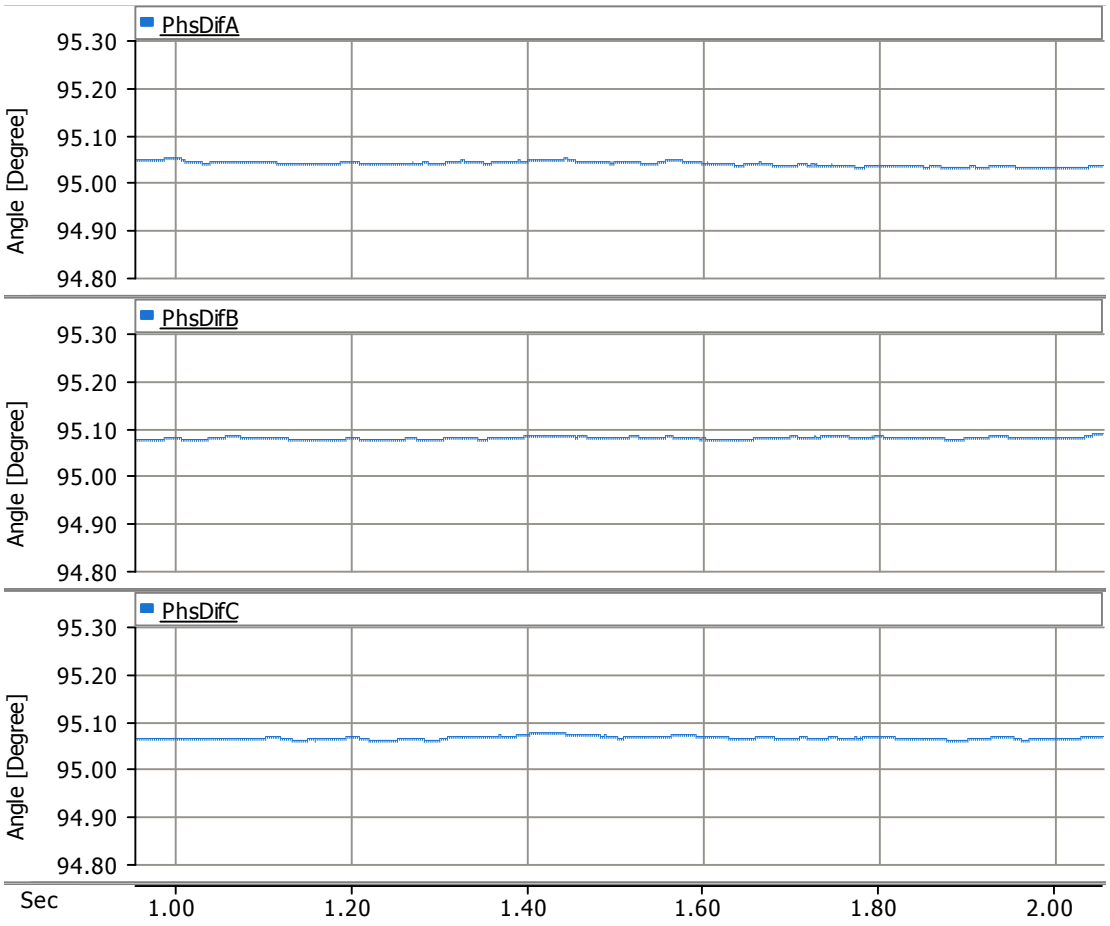


Fig.4.93: Injection angle

In the same time DC voltage ripple become 15V and the voltage oscillates between 987V and 1002V. The boundary of oscillation is reduced by 65 % in comparison with DC voltage shown in Fig.4.85. The boundary of oscillation is 43V (using only DC voltage controller) in Fig.4.85 while it is 15V in Fig.4.94. The DC voltage adjusted by each DSSC devices in three different phases is plotted in Fig.4.94.

The importance of the proposed controller becomes dominant when accuracy of injection angle come high priority.

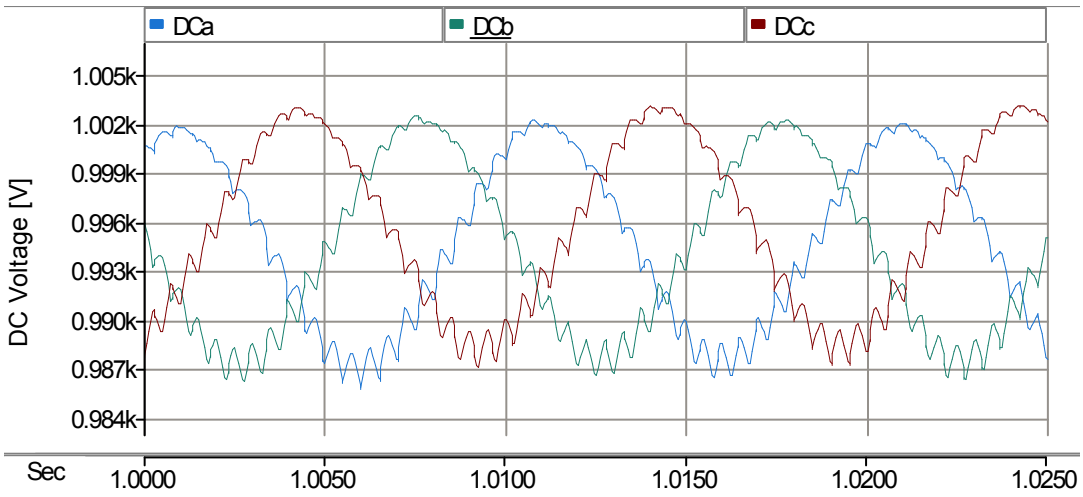
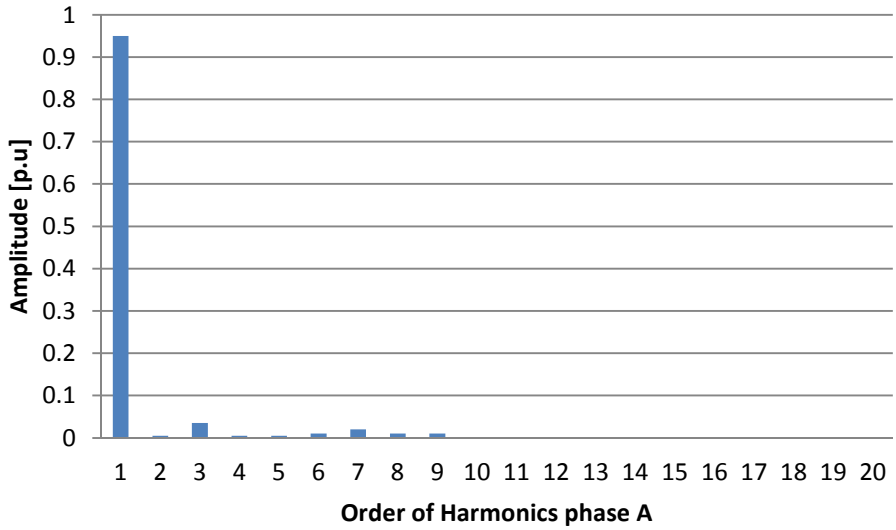
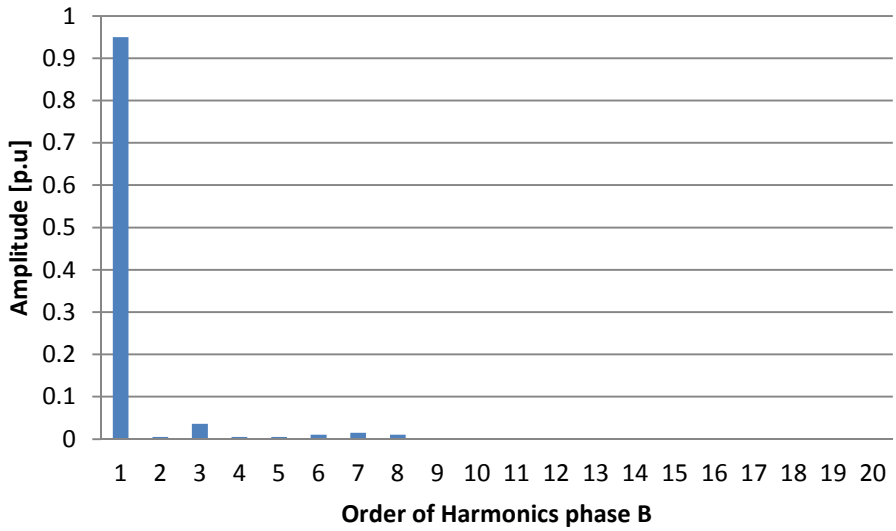


Fig.4.94: DC voltage using the proposed controller

The spectrum of injected harmonics using the proposed controller is presented in Fig.4.95 for three different phases. Amplitude of injected 3rd harmonic through phase "A" is 0.71V which in comparison with its value represented in pervious figure is reduced by 27%. THD of injected voltage is 4.1%.





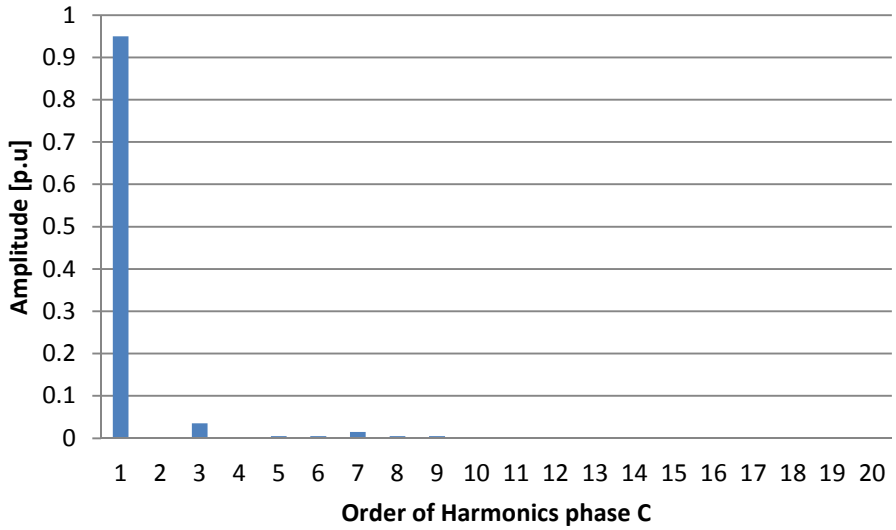


Fig.4.95: Injected harmonics using the proposed controller

4.9.3 Summarized results of conventional and proposed controller

In the conventional controller when gain increases, it affects the voltage ripples, THD and the angle of injection. Amplitude of ripples and angle of injection respond differently to the change of gain. Increment of gain improves the angle while increases the amplitude of ripples and THD. It means that improving one the factors (i.e injection angle) sacrifices the other one.

However, when gain is reduced it reduces the amplitude of ripples and THD, but increases the injection angle. It can be observed that reducing gain does not improve all factors in the same time.

Proposed controller can improve ripples, THD and injection angle in the same time as it receives continuously feedback from both angle of injection and DC voltage. These improvements (as shown in the previous subsection) have been achieved by further tuning the proposed controller. The ripple is reduced to 15V and angle of injection is reduced to 95.05°.

Table 4.11 summarizes the simulation results for the further tuned conventional and proposed controller.

Controller	kp	ki	Ripple	Angle	THD
Conventional controller	150	200	43V	95.9°	5%
Conventional controller with increase gain	165	200	75V	95.7°	5.2%
Conventional controller with reduced gain	135	200	19V	95.93°	4.85%
Proposed controller with further tuning	142	200	15V	95.05°	4.1%

Table 4.11: Summarized results of further tuned conventional and proposed controller

4.10 Investigation of the change of the system parameters on the performance of the proposed controller

In electrical networks (including distribution feeders) some of the system parameters such as line voltage, connected load and network configuration can be changed with different loading conditions. For example, voltage drop can often happen in heavily loaded distribution networks and in another example, amplitude of line current can be altered by changing loads in the system. However, it is expected that the functionality of

DSSC which is governing by the proposed controller not to be affected by these changes.

4.10.1 Performance of the DSSS with no changes in system parameters

An 11Kv distribution feeder supplying a three phase load is equipped with DSSC devices have been used in simulation. Impedance of the line comprises of 0.03 H reactance and 1 Ω resistance. DC voltage as shown in Fig. 4.96 has been regulated at 1kV by each DSSC devices in their own DC link.

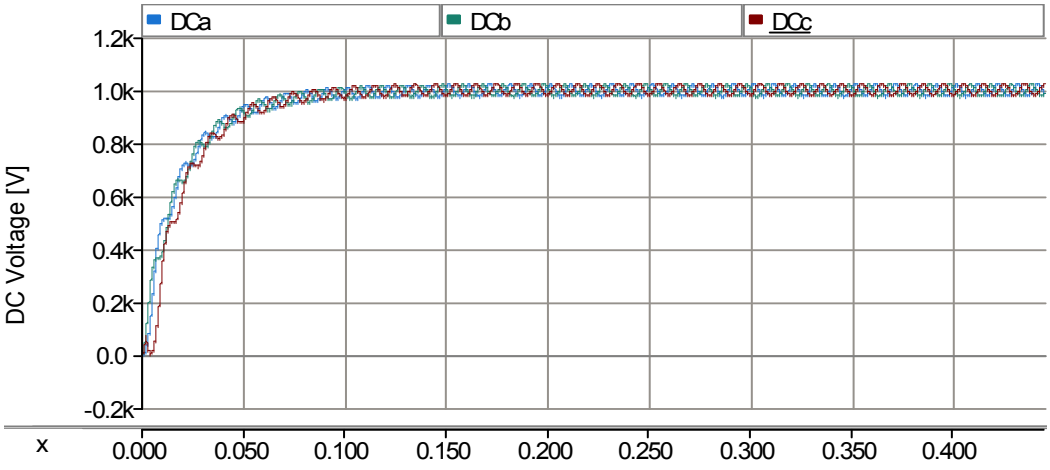


Fig. 4.96: DC voltage when line impedance includes 0.03 H reactance and 1Ω resistance

Injected voltage and line current is shown in Fig.4.97 and it shows the orthogonal injection of voltage through the line and peak amplitude of line current flowing through the STT is 380A.

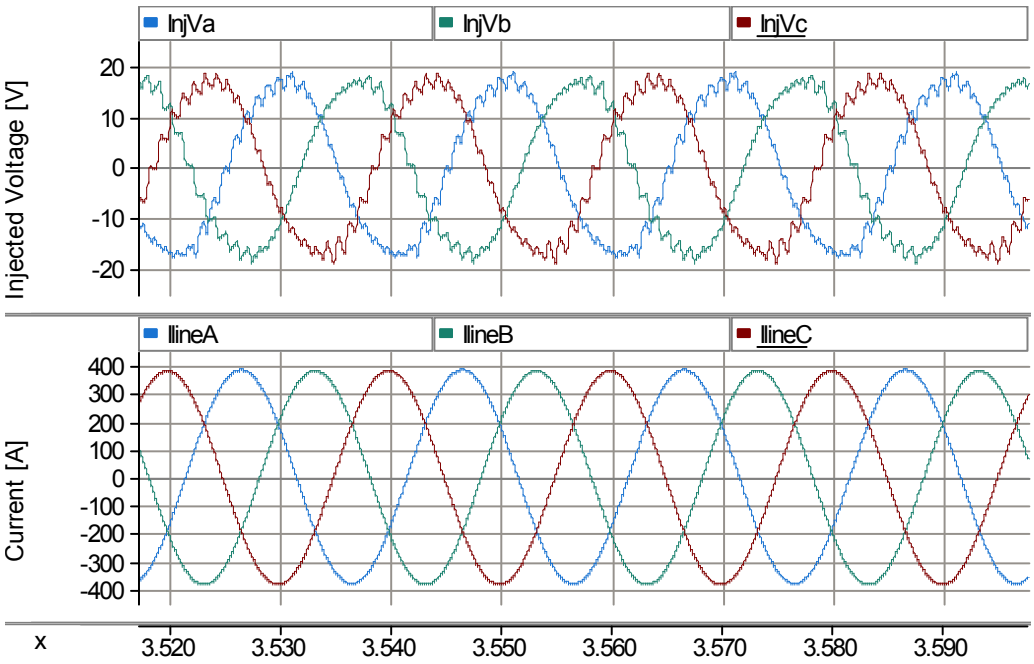


Fig.4.97: Line Current and injected voltage when line impedance includes 0.03H reactance and 1Ω resistance

Load angle between the sending end and receiving end is show in Fig.4.98. The angle is 23.8° when the line peak current is 380A. It can change depends on the impedance of the line and this is shown in the next subsection.

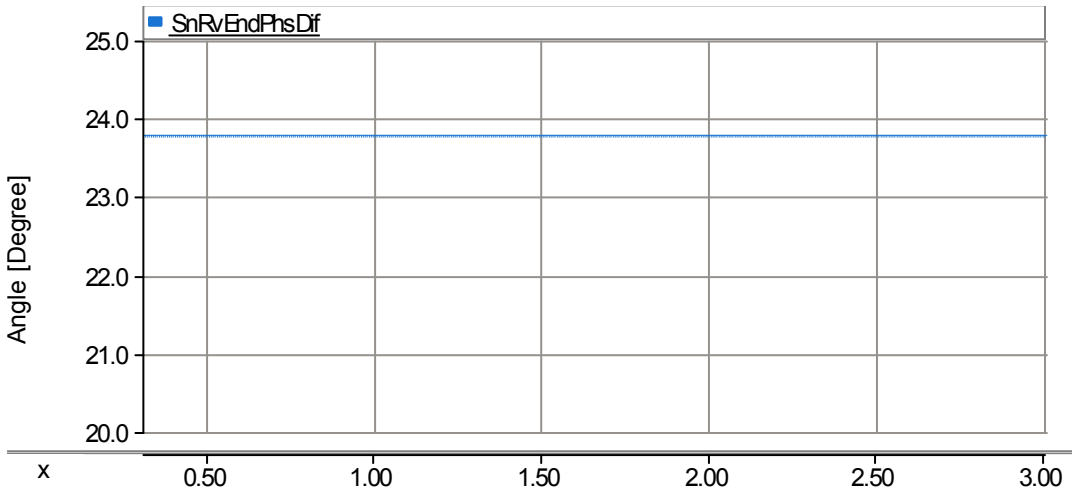


Fig.4.98: Load angle when line impedance includes 0.03 H reactance and 1Ω resistance

4.10.2 Performance of the DSSS when resistance of the line is altered

Line resistance reduced by 90% from 1Ω to 0.1Ω in order to investigate the effect of change of the line resistance on the performance of the DSSC. As a result of reduction

of the line resistance, current is increased from 380A to 400A. This increment can be realized by comparing Fig.4.99 and Fig.4.97.

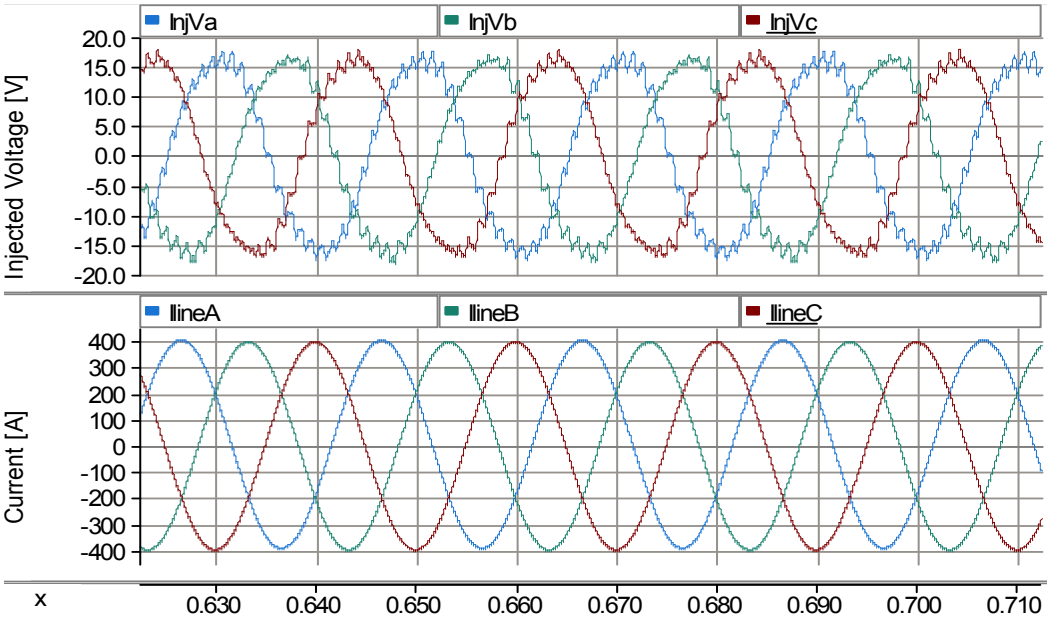


Fig.4.99: Line Current and injected voltage when resistance of the line is 0.1Ω

Fig.4.99 shows that injected voltage is orthogonal to the line current and it has not been affected by change of line current.

The load angle is shown in Fig.4.100 and due to the reduction in the resistivity of the line, load angle is increased by 1° from 23.8° to 24.8°.

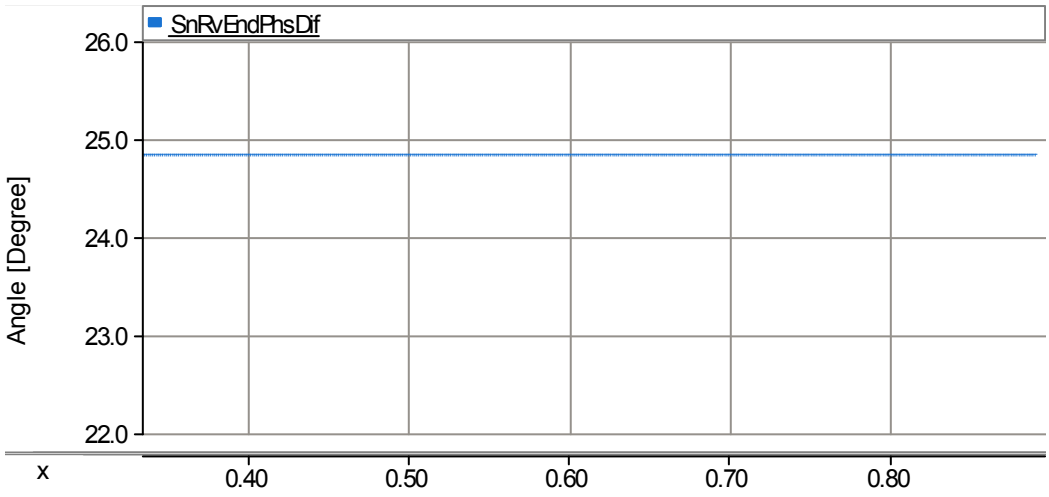


Fig.4.100: Load angle when resistance of the line is 0.1Ω

Despite the changes in the line current, line impedance and load angle the proposed controller has regulated the voltage across the DC link at 1kv (desired value). DC voltages are plotted in Fig.4.101 and it shows that performance of the controller has not been affected by the aforementioned changes.

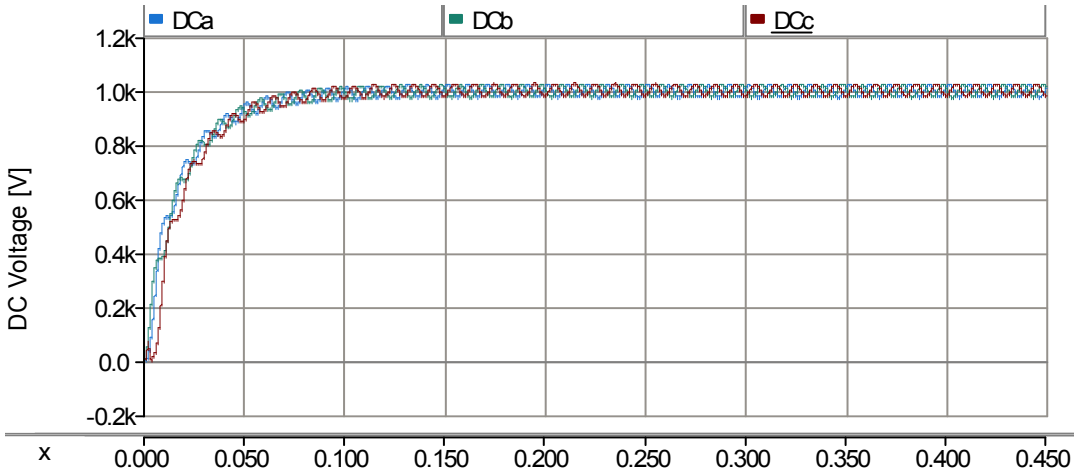


Fig.4.101: DC voltage when resistance of the line is 0.1Ω

4.10.3 Performance of the DSSS when load is reduced in half

Variation of the load occurs most frequently in the electrical networks especially in the distribution networks. DSSC models employed in the networks need to be compatible with such changes. It means that employed controller must operate in presence of different loads and be able to regulate the DC voltage in a required value and inject orthogonal voltage with respect to the line current. Fig.4.102 shows the voltage across the DC link when the supplied load is halved. It can be seen that the voltage is regulated in 1kV and it remains stable in steady state regardless of load reduction.

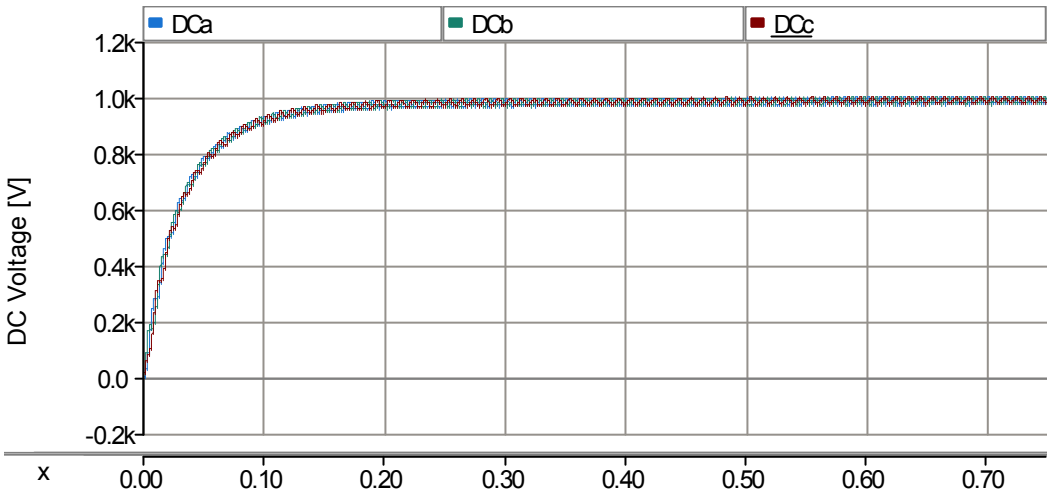


Fig.4.102: Voltage across the DC link when the supplied load is halved

With load shading line current as shown in Fig.4.103 has been reduced almost by 50% from 400A to 200A. However as it can be observed the DSSC modules are still able to inject orthogonal voltage through the line. This shows that operation of controller is not dependent on the line current and it can operate satisfactorily with different line currents.

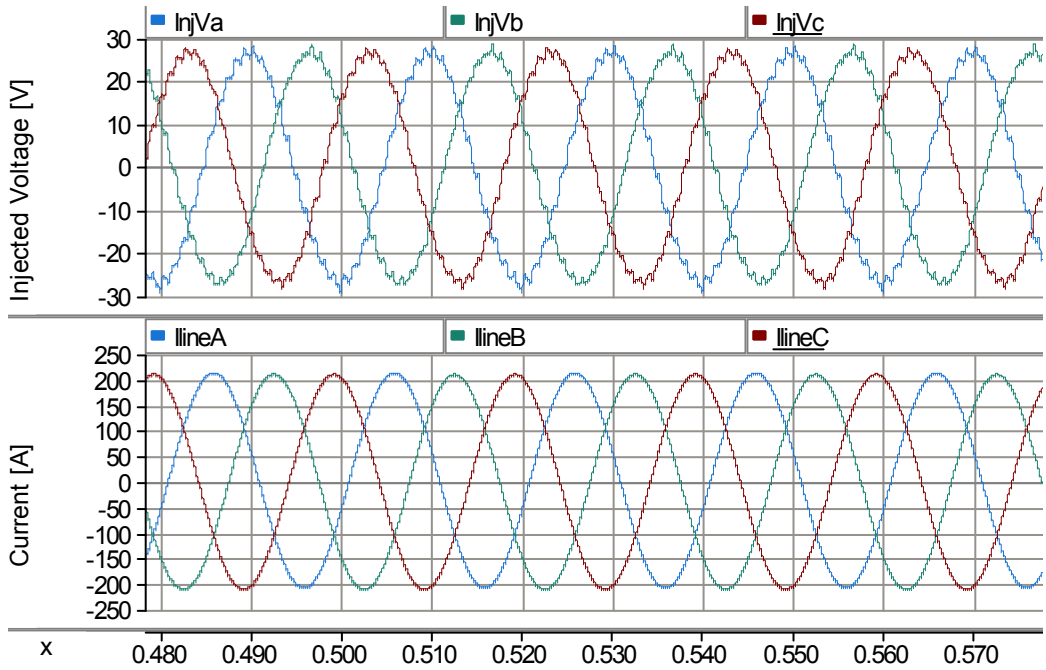


Fig.4.103: Line current and injected voltage when the supplied load is halved

However, the load angle has been changed by change of the connected load at the receiving end and it is shown in Fig.4.104. Comparison between this figure with the corresponding one shows that load angle has been decreased by 45% from 23.8° to

12.9°. The reduction of load angle is consistent with the lessening of load however this is not endangering the functionality of DSSC and its controller.

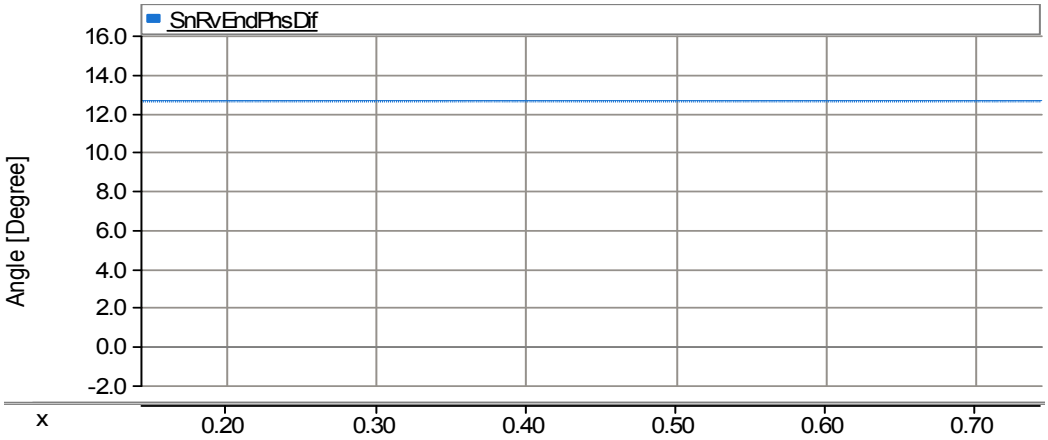


Fig.4.104: load angle when the supplied load is halved

4.10.4 Performance of the DSSS in reconfigured network

Reconfiguration of the electrical network is one of the events which can change the load angle and line current in the meshed and parallel networks. In order to investigate the probable effects of the reconfiguration of the network on the performance of the operation of DSSC modules another line is connected in parallel with the existing line to supply the same load. One of the notable changes is variation of the load angle which is shown in Fig.4.105. By connecting another line in parallel the new load angle has become 20.5°. This shows 3.3° reduction in the load angle as it was 23.8° in absence of parallel line.

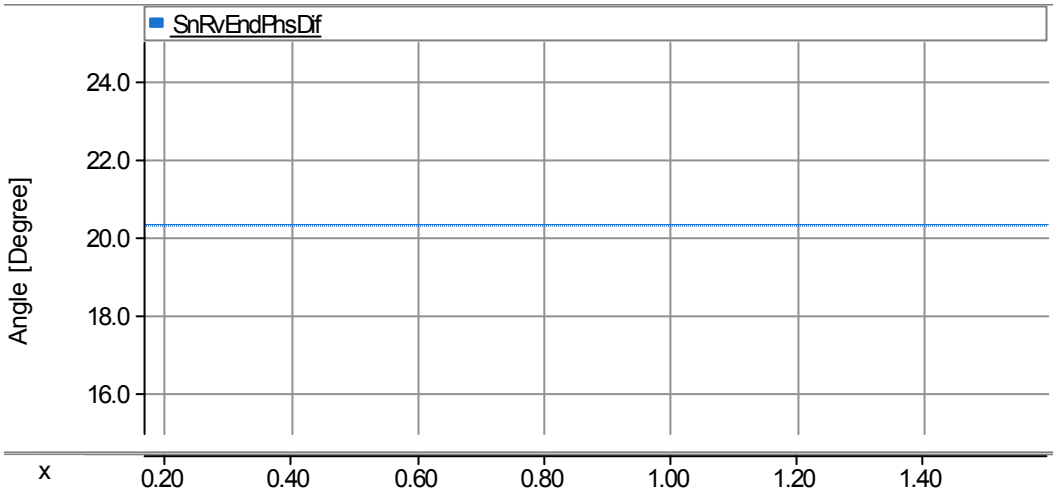


Fig.4.105: load angle when another line is connected in parallel

Line current has been decreased as the load current is divided between two parallel lines. Fig.4.106 shows the line currents and injected voltages in the line equipped with

DSSC modules. Line current was 400A when a single line was supplying the load (see Fig.4.88) however by connecting another line in parallel, line current becomes 260A. Although line current and load angle (as it is discussed earlier) has been changed but satisfactory orthogonal voltage injection plotted in Fig.4.106 shows the performance of the controller has not been affected.

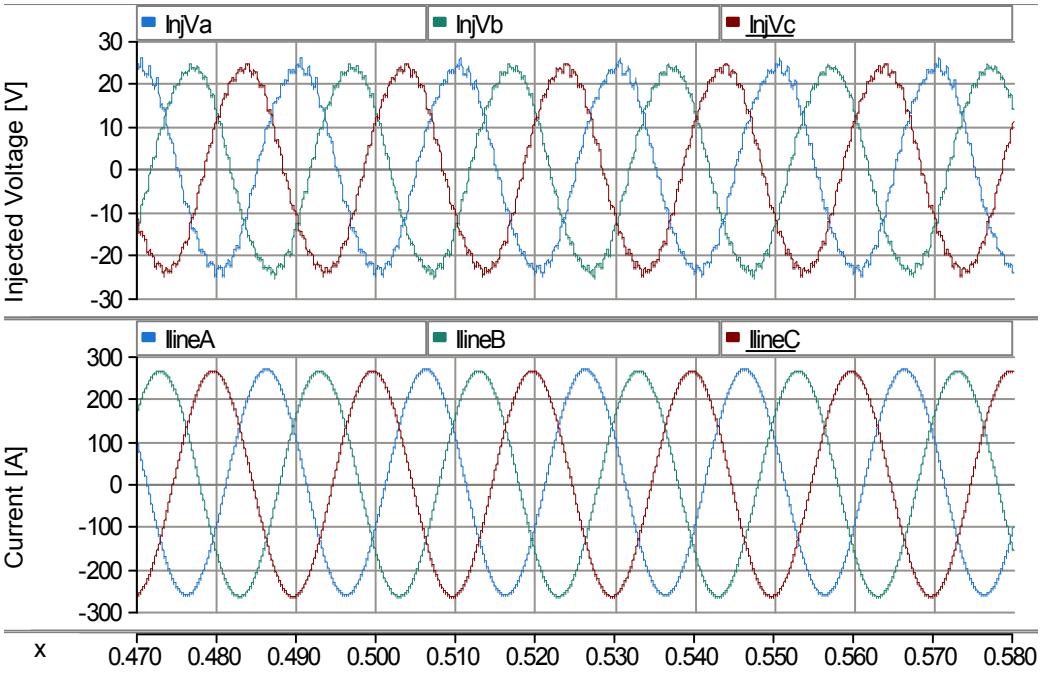


Fig.4.106: Line Current and injected voltage when another line is connected in parallel

Voltage across the DC link is shown in Fig.4.107 and it shows that despite change of load angle and line current controller is able to regulate the DC voltage at 1kV. Voltage remain stable in steady state and its amplitude is not affected by the changes in the power system.

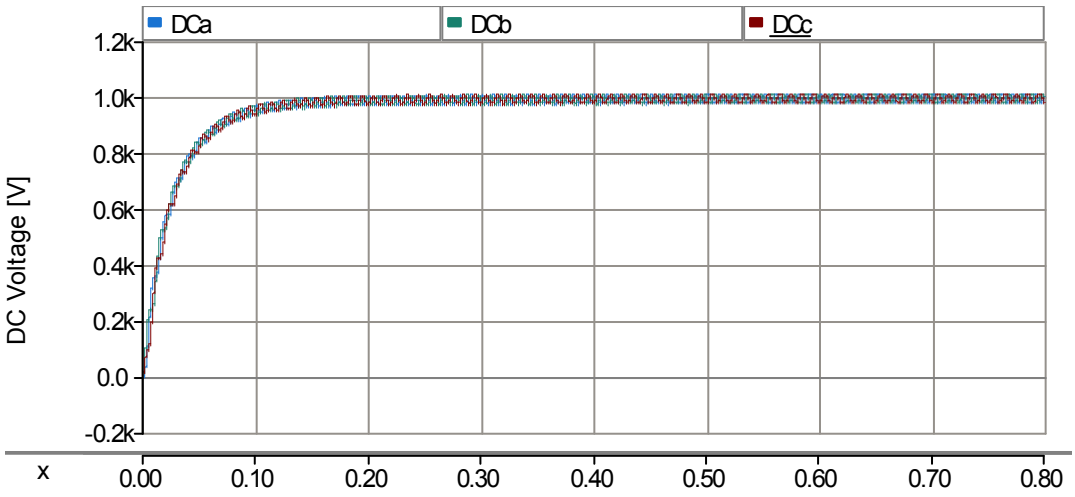


Fig.4.107: DC voltage when another line is connected in parallel

4.10.5 Performance of the DSSS in sag swell of the line voltage

Voltage drop and over voltage in the electrical networks can affect other electrical parameters of the system such as line current or load angle. In order to investigate the possible effects of the change of voltage on the performance of the DSSC two different scenarios has been examined. In one scenario the line voltage has been increased by 10% and in another scenario it has been reduced by 10%. The rms value of sending end line voltage is plotted in Fig.4.108 and it shows 10% over voltage.

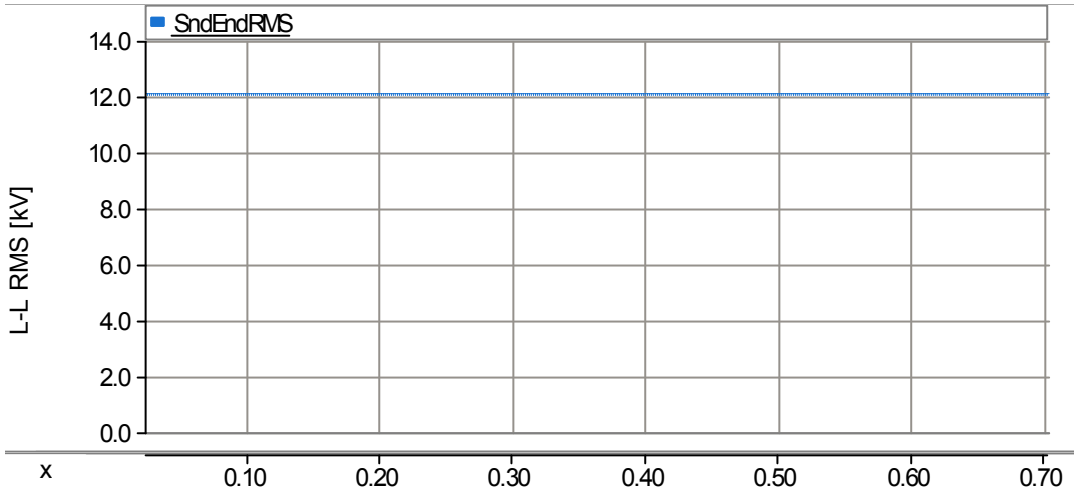


Fig.4.108: Sending end line voltage when there is 10% over voltage

As the line voltage increases the line current increases as well however functionality of DSSC devices as shown in Fig.4.109 remains unaffected. This figure shows that line is

increased by 10% from 400A to 440A and DSSC devices injecting orthogonal voltage in respect to the line current.

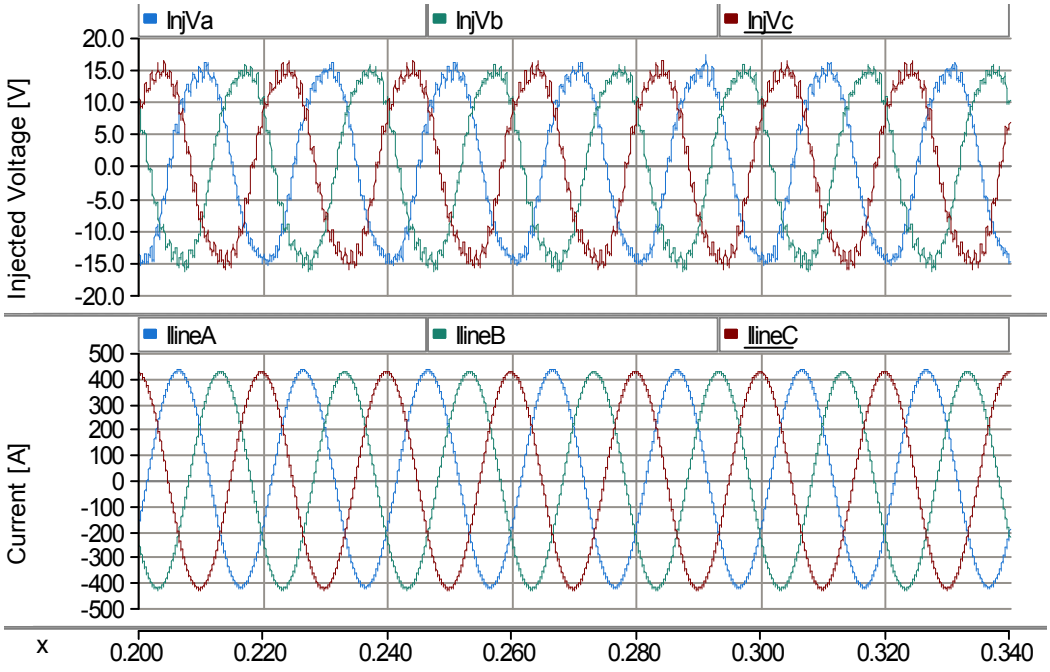


Fig.4.109: Injected voltage and line current in presence of 10% over voltage

When there is a 10% change in the line voltage, DC voltage is regulated in 1kV by DSSC device across the capacitor as shown in Fig.4.110. This shows that the voltage reaches to steady state and remains stable at 1kV.

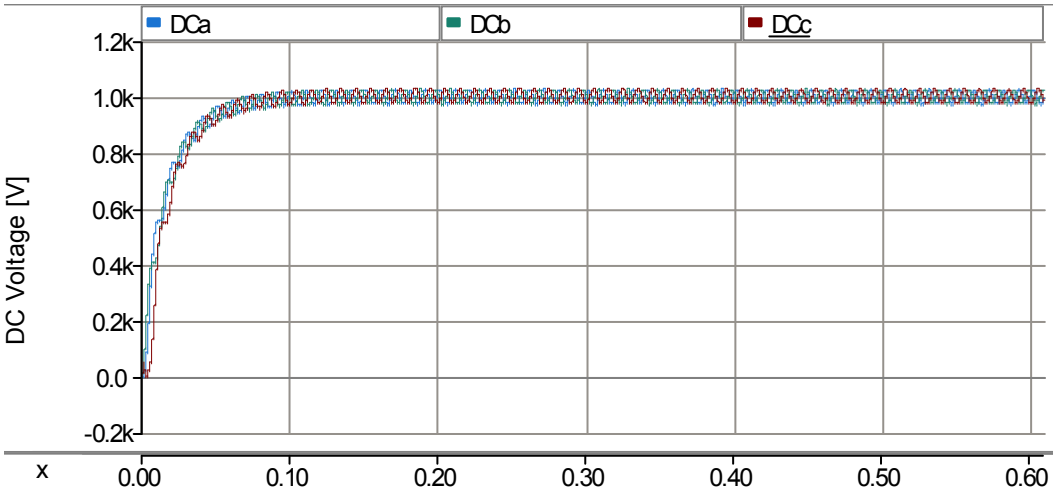


Fig.4.110: DC voltage across the capacitor when there is 10% change in the line voltage

Fig.4.110 shows that regulating the DC voltage across capacitor is successfully achieved in presence of 10% change in the line voltage. The change can be either rise in

the voltage or drop in the voltage. For example, Fig.4.111 shows rms value of voltage (10kV which is 10% less from 11kV) at the sending end bus of the line however the adjusting of the DC voltage remains unaffected as it is shown in Fig.4.110.

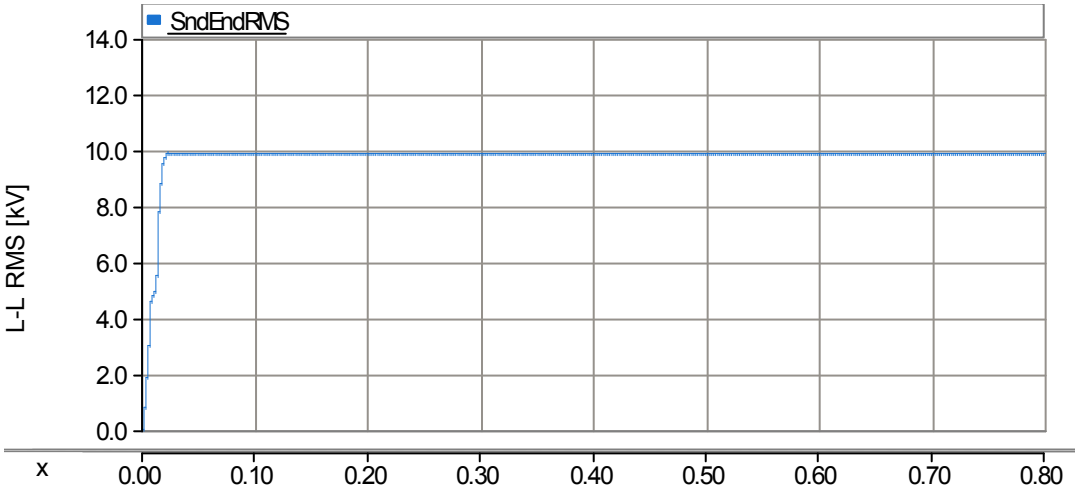


Fig.4.111: rms value of voltage at the sending end

When there is a 10% voltage drop in the line voltage line current is decreased as well and it is dropped to 360A as shown in Fig.4.112. However, this figure shows that still the DSSC module injects orthogonal voltage in respect to the line current and the functionality of DSSC has not been affected.

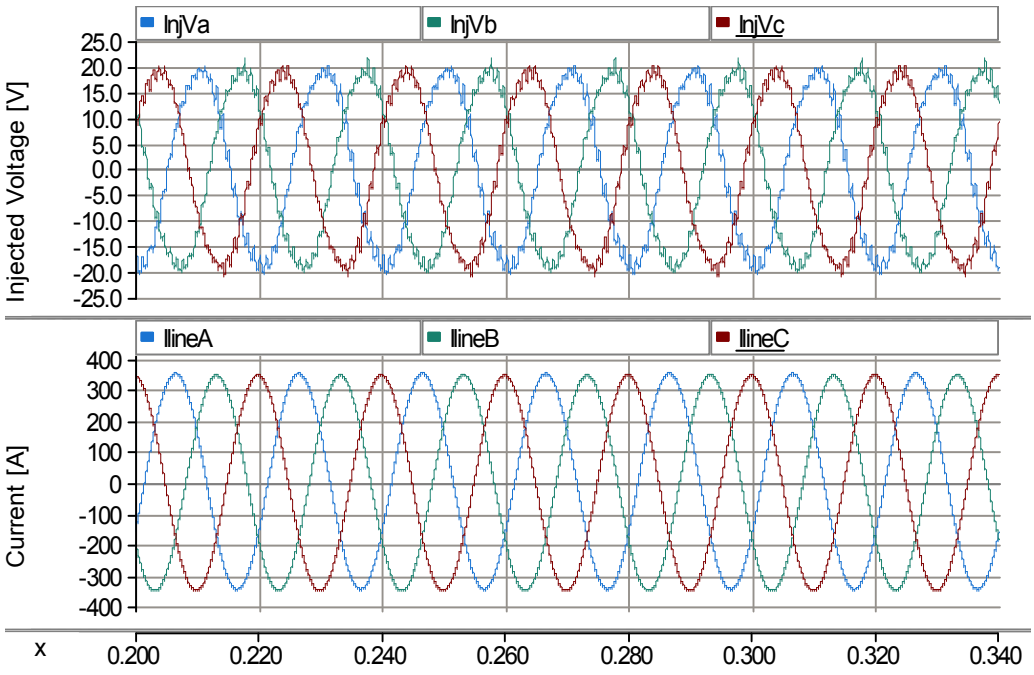


Fig.4.112: injected voltage and line current when there is a 10% voltage drop at the sending end bus

4.11 Fault Management Study

DSSC devices are series through the lines and in the case of short circuit events in the power lines a high current is expected to flow through the STT. Fig.4.113 shows rms value of current feeding the fault in occurrence of single phase to ground fault in phase "A". Current increases in the corresponding line as it is shown in Fig.4.114. This figure shows the line current when it is not compensated with DSSC and line is just supplying a lumped load at the receiving end.

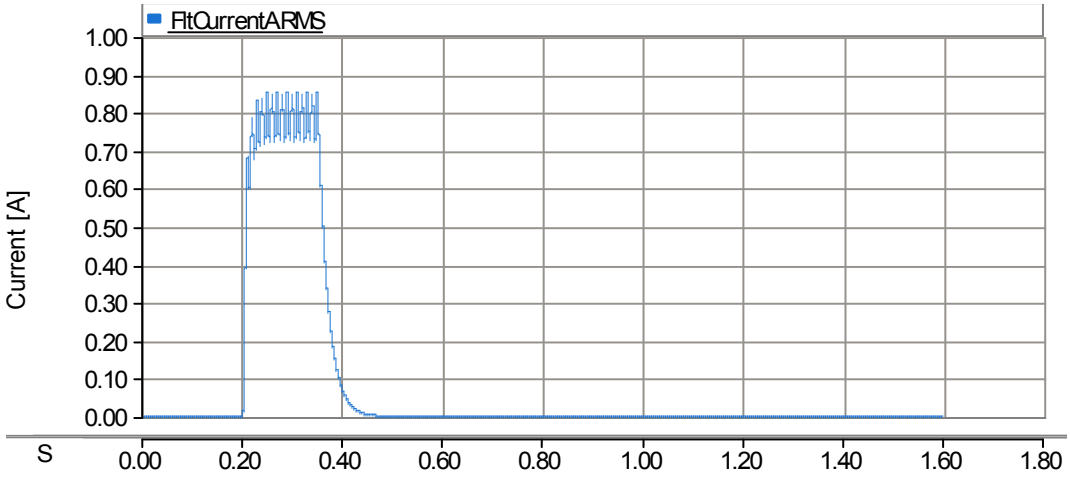


Fig.4.113: rms value of fault current

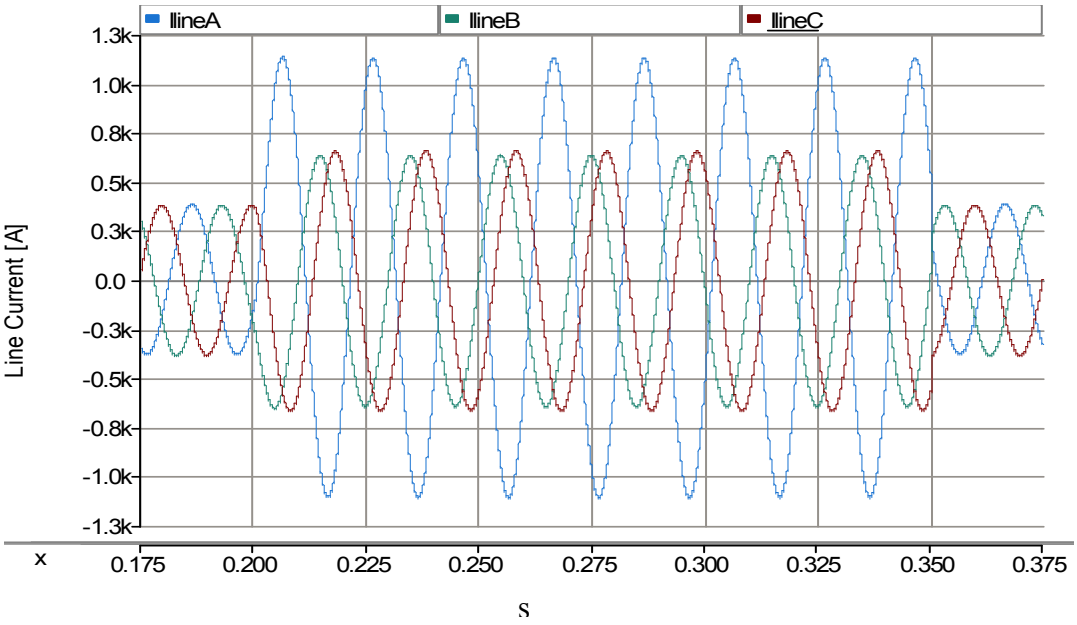


Fig.4.114: Three phase line current with single phase to ground fault in "A" phase

However, if the line becomes equipped with DSSC modules, there will be high current in the secondary of STT. Fig. 4.115 shows the current passing through the DC link

inside the DSSC in the case of single phase to ground fault. As it can be observed clearly from Fig. 4.115 the peak of current is increased dramatically by 300% by jumping from 50A to 150A.

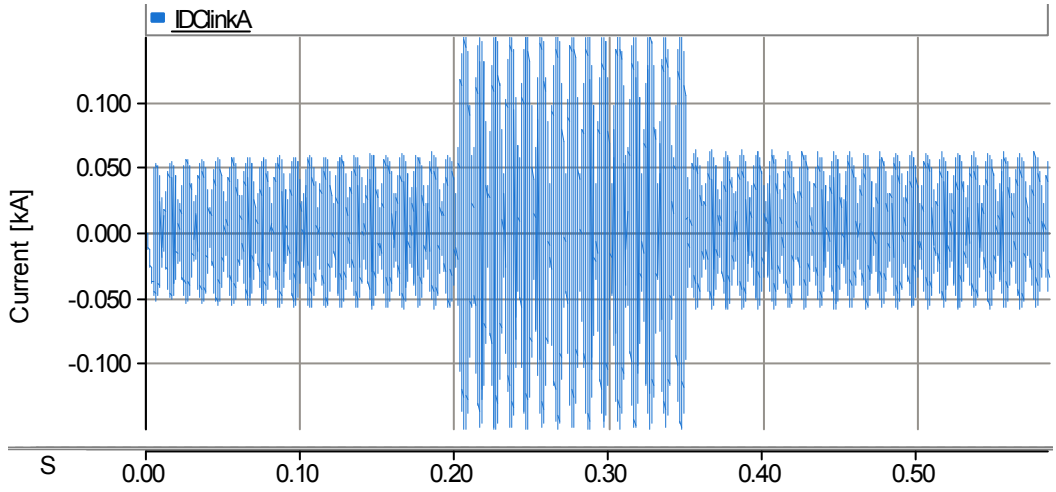


Fig. 4.115: Current flowing through the DC capacitor in the DSSC device

The current flowing through the power electronic devices can damage the components. In order to protect the DSSC devices some protection action need to be taken. The possible protection actions and strategies have been studied in the following subsections.

4.11.1 STT is bypassed

In the occurrence of the single phase fault to ground one of the possible actions which can be taken is bypassing the STT in the secondary side (converter connected side). By doing so, the induced current in the secondary side will circulate in the transformer and the bypass switch. This is desired as it is stopping the current flowing through the converter. Fig.4.116 shows the current within the DC link it shows that the high current through the link is stopped immediately after bypassing the STT.

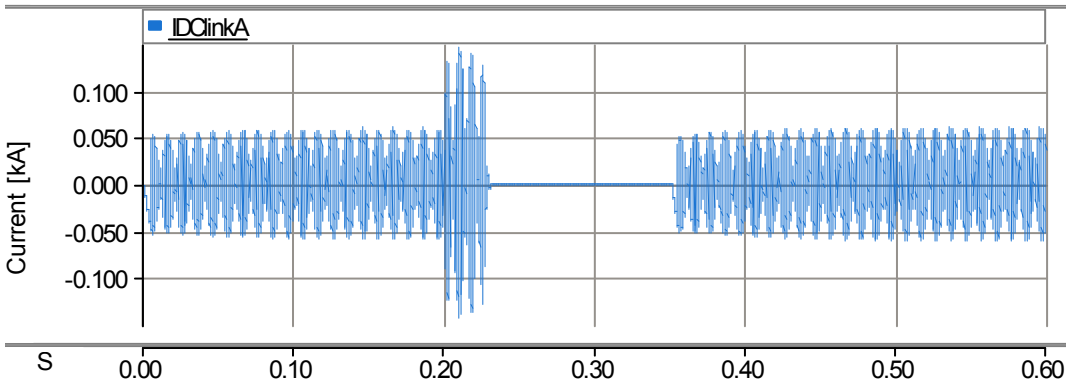


Fig.4.116: Current through the DC link when STT is bypassed

The injected voltage by DSSC device and line current is shown in Fig.4.117. Bypassing the STT reduces amplitude of injected voltage in the faulty phase. It has almost no effect on the line current and this can be distinguished by comparing line current shown in Fig.4.117 and Fig.4.114. Having almost same fault current with DSSC and without DSSC denotes that the fault level is remaining unaffected.

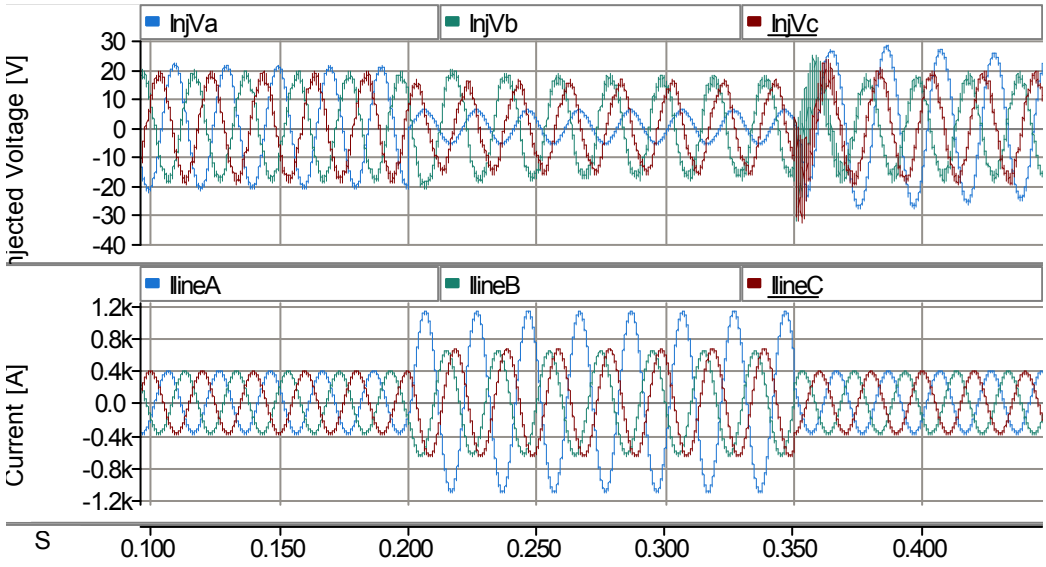


Fig.4.117: Injected voltage and line current when the STT is bypassed

Bypassing the STT in the secondary side discharges the DC capacitor and immediately after clearing the fault the capacitor starts to be charged up. Voltage across the DC link in DSSC device in phase "A" is shown in Fig.4.118. Voltage is zero during the fault and it reaches 1kV by clearing the fault.

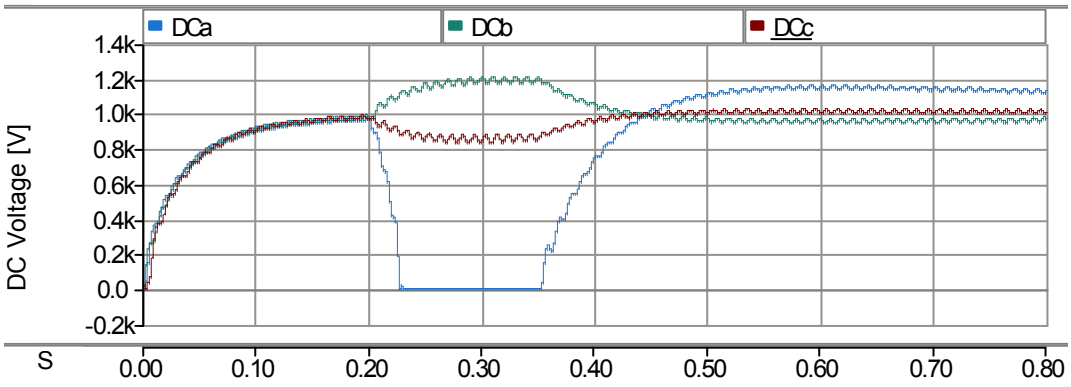


Fig.4.118: DC voltage across the capacitor when STT is bypassed during the fault

Bypassing the STT in the secondary side helps to circulate the current between the secondary and the bypass switch. This mitigates DC link current and discharges the capacitor. Mitigation of DC link current is desired however discharge of the capacitor is a disadvantageous.

4.11.2 STT is bypassed and converter is blocked

In order to save DC voltage during fault DC capacitor needs to be isolated from bypass switch. This can be achieved by blocking the converter. Blocking the converter disconnects the path between the capacitor and the bypass switch. Fig.4.119 shows the voltage across the DC capacitor in DSSC for three different phases when STT is bypassed and converter is blocked in occurrence of fault. Phase "A" is the faulty phase and it can be observed that during the fault the voltage stays flat and immediately after fault recovery converges to 1kV.

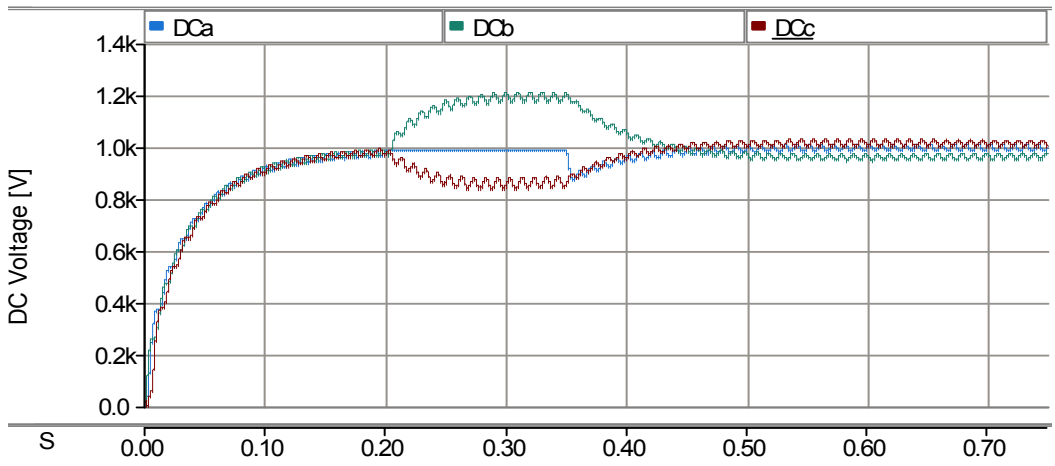


Fig.4.119: Voltage across the DC capacitor when converter is blocked and STT is bypassed

The injected voltage and line current in the case of bypassing the STT and blocking the converter is shown in Fig.4.120. It is expected that, injected voltage or line current not to be affected by blocking converter and bypassing STT. Comparing Fig.4.120and Fig.4.117 shows that there is no difference in the injected voltage or the line current and this is satisfying the expectations.

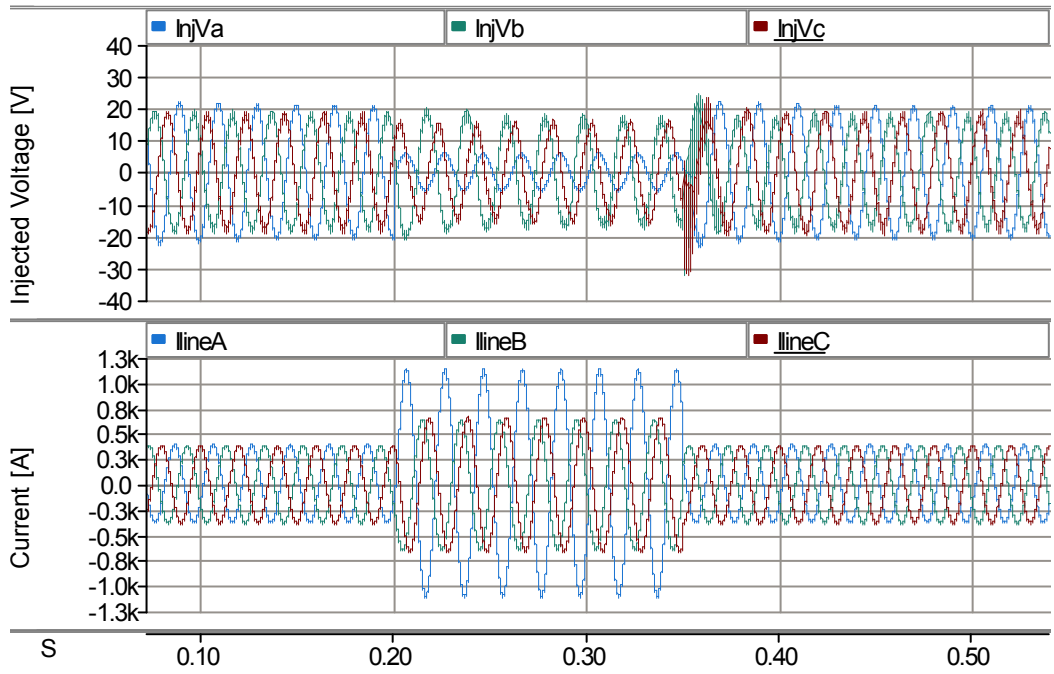


Fig.4.120: Injected voltage and line current when converter is blocked and STT is bypassed

Blocking the converter and bypassing STT in the same time stops current flowing through the DC link. Fig.4.121 shows DC link current and It can be seen that current is zero immediately after blocking the converter and it resumes after deblocking.

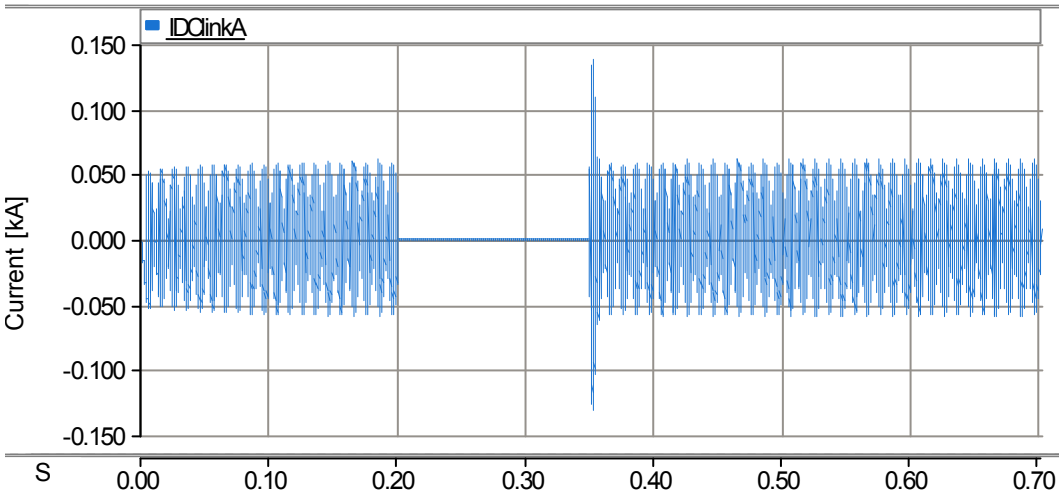


Fig.4.121: DC link current when converter is blocked and STT is bypassed

4.11.3 STT is opened

STT can be open circuit in the secondary side instead of being bypassed in occurrence of short circuit fault in the power line. In order to take this action a series switch needs to be located between converter and STT. By opening the switch converter will be isolated from the STT and consequently from the power line. DC link current shown in Fig.4.122 falls down below the steady state value and it slowly decays.

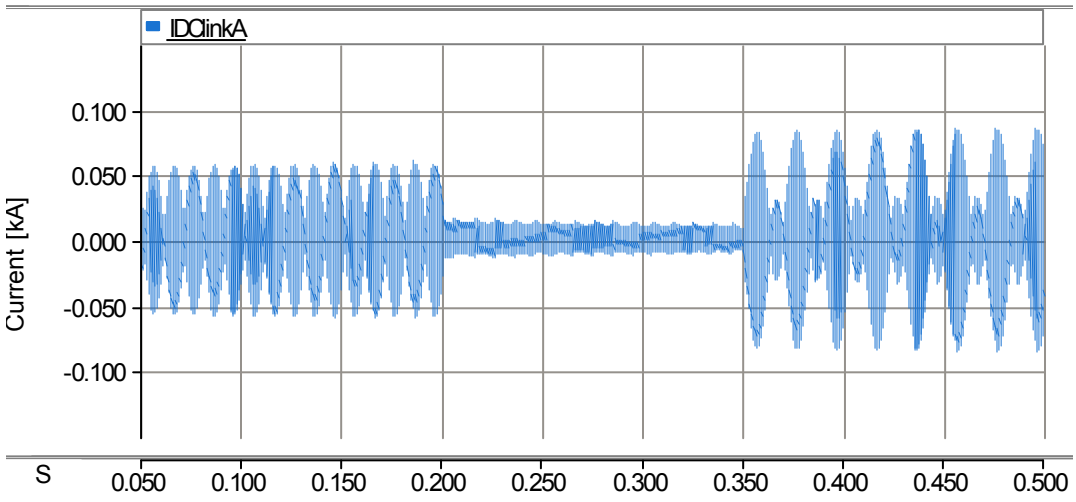


Fig.4.122: DC link current when STT is open circuit

Decaying current discharge DC capacitor and reduces the DC voltage. Voltage across the DC capacitor inside the DSSC device in three different phases is shown in Fig.4.123. DC voltage in phase "A" decreasing during the fault but it recovers again by clearing the fault.

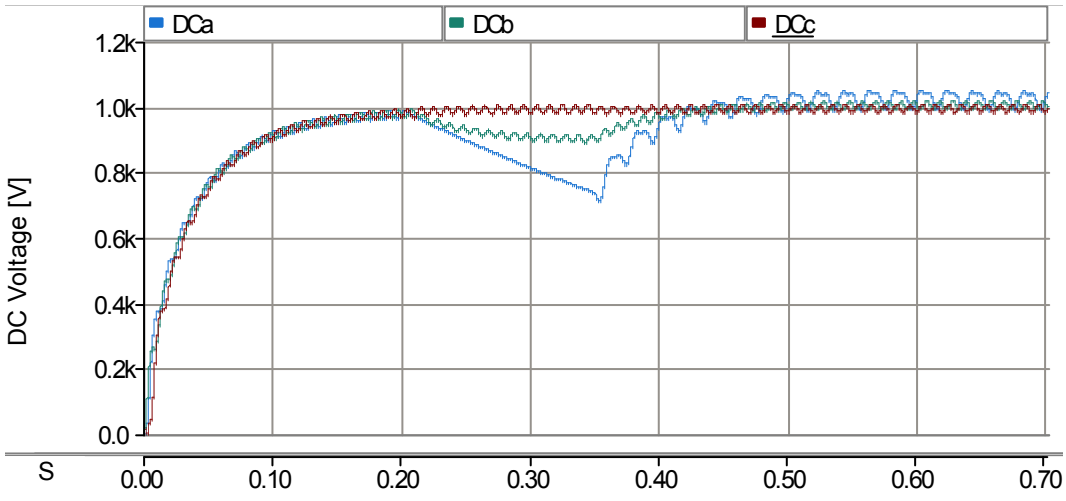


Fig.4.123: DC voltage inside DSSC when STT is disconnected from the converter

Disconnecting the STT from the converter makes an open circuit in the secondary side of STT. Consequently, it inserts series impedance through the line and limits the fault current even below the steady state value as shown in Fig.4.124. Opening the STT can be more beneficial as it limits the line short circuit current however, practically it is impossible to be employed. Opening the circuit induces a high voltage in secondary side of the STT which can endanger the insulations and related equipments. For this reason in the presence of fault opening of the STT must be avoided.

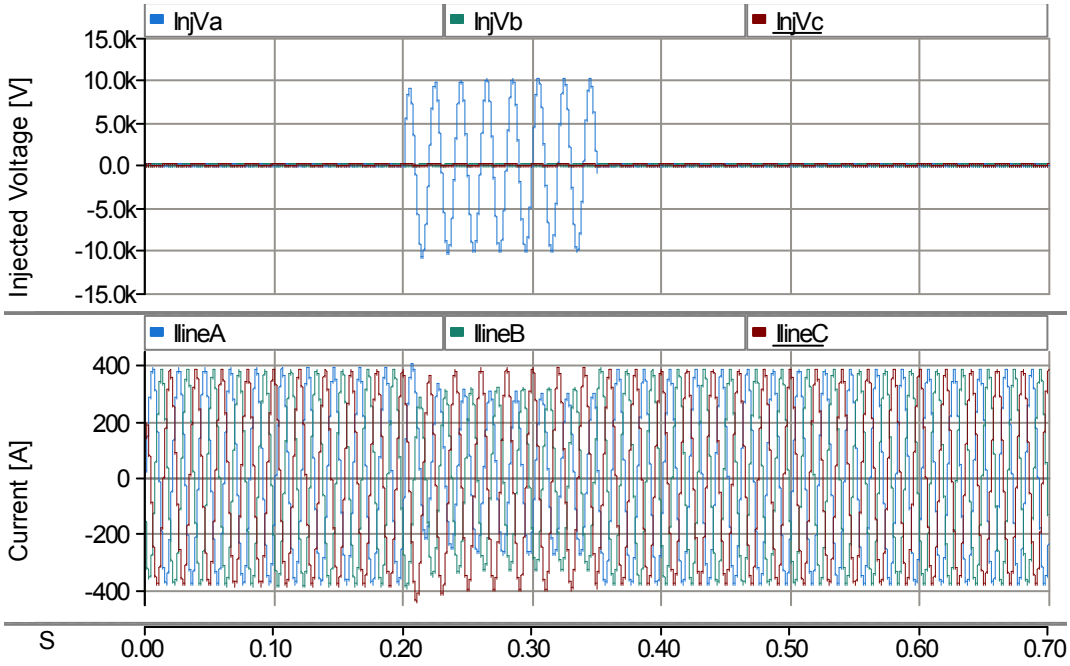


Fig.4.124: Injected voltage by DSSC and line current STT is isolated from converter

4.11.4 Converter is blocked

Blocking the converter disconnects DC capacitor from STT and stops converter from functioning. To achieve this, the control system stops sending firing pulses to the IGBTs and IGBTs become an open circuit. Current flowing through DC link in steady state and during the fault is shown in Fig.4.125. It shows that current is increased slightly in one direction (diodes conducting direction) and id stopped in the reverse direction (diodes are not conducting).

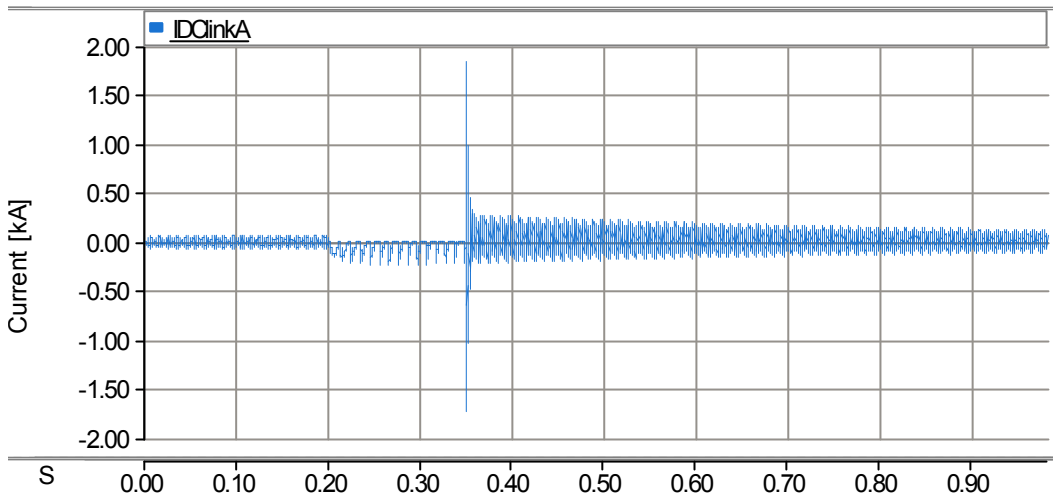


Fig.4.125: Current through DC link when only converter is blocked

In addition, blocking converter means losing control over the voltage across the secondary of the STT. Consequently, a high voltage will be induced in either side of the STT (with respect to the turn ratio of the STT they will be different in amplitude) which as discussed in pervious subsection it can endanger the insulations and equipments. Injected voltage by STT and line current in three different phases is shown in Fig.4.126. In this figure the induced voltage is high and it continuously grows but short circuit current through the line also remains high.

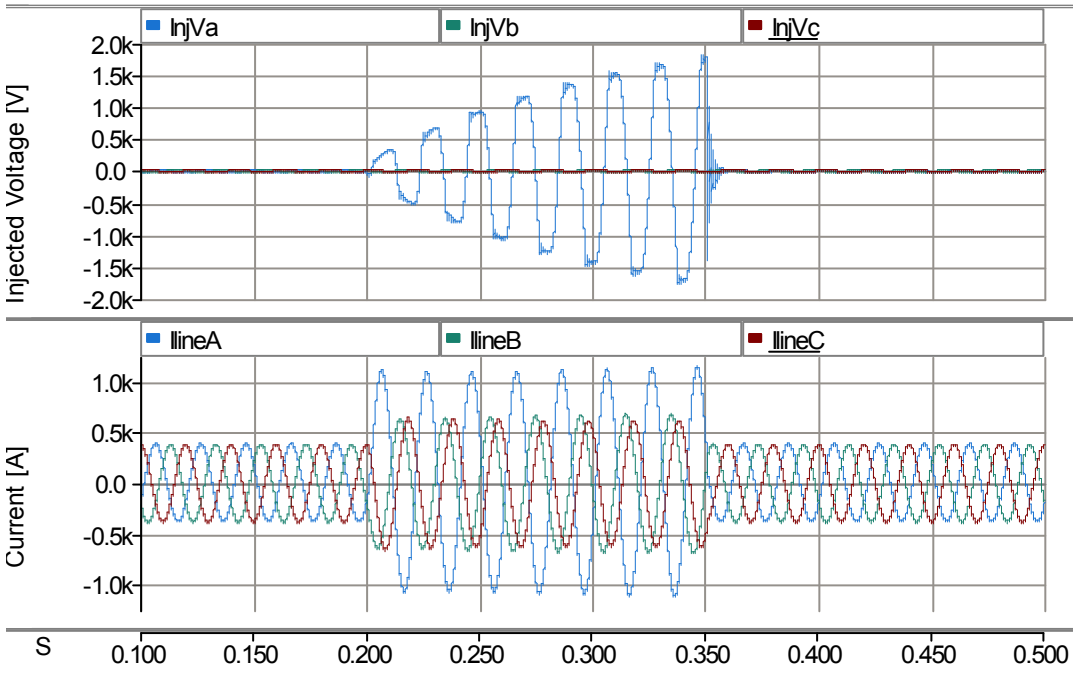


Fig.4.126: Injected voltage by STT and line current in three different phases when only converter is blocked

Although converter is blocked however DC capacitor still can be charged up through diodes and as there is no control on the capacitor voltage then it can exceed the limits. For example, Fig.4.127 shows the voltage across the DC link when converter is blocked. In this figure capacitor voltage continuously is increasing during the fault and as soon as the converter is deblocked then voltage start to become under control.

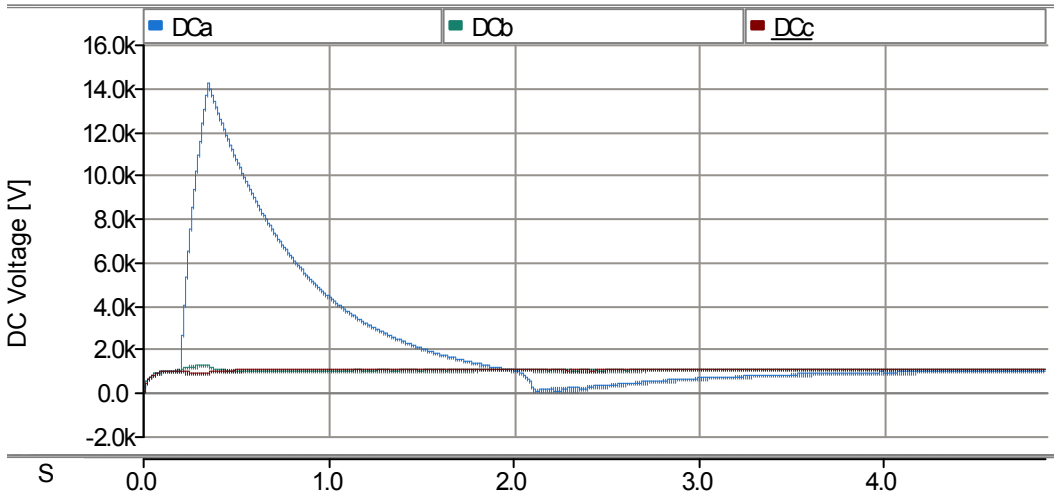


Fig.4.127: Voltage across the DC link when converter is blocked

4.11.5 Concluded fault strategy

During the fault all components need to be protected from high voltage or current. For this reason different fault recovery strategies have been investigated. For example, when only converter is blocked DC voltage can exceed the limit which is not desired. In another scenario, when STT become open circuit -regardless of blocking or deblocking of converter- there will be high AC voltage in either side of the STT which makes this solution to be unpractical. Among the examined fault recovery strategies, bypassing the STT tends to be an acceptable option to be employed. It can avoid inducing a high voltage in the STT however, it comes with disadvantage of discharging the DC capacitor. Blocking the converter along with bypassing the STT holds the DC voltage in pre fault value and avoids a high voltage in the STT in the same time. This is the solution which is proposed to be taken. Also with this solution, short circuit current through the faulty line remains unaffected and it is not affecting the fault level of the power system.

As regard as protecting the switches before detecting the fault and taking the proposed actions concern, it must be noted that the switches must be rated for the maximum

possible over-currents and overvoltages. The switches also can be protected against overvoltages by employing surge arresters in parallel to bypass the switches when the voltage across them exceeds the maximum withstand voltage. However, the switches definitely must be rated to the maximum over-current which can occur in the worth condition.

In addition to the switches components of the LC filter needs to be protected against the transients. They need to be designed in a way to withstand the worth scenario of over current and in the same time they need to be protected by surge arresters against the possible overvoltages.

4.12 Simulation of LC filter

The LC filter is designed to be employed in the experimental tests is simulated in PSCAD using the selected values of RL in order to observe the performance of the filter. Having carrier frequency of 1kHz for the PWM pulse generator the output voltage of the converter, as it can be clearly observed in Fig.4.128 (blue bars), contains high order harmonics. Some of the major dominant generated harmonics are 18, 20, and 22. However by using the designed low pass filter the mentioned harmonics have been eliminated, as it can be seen in Fig.4.128 (black bars). Now only the fundamental frequency has passed through the filter. In spite of this along with the fundamental frequency some other low order harmonics with negligible amplitude has been observed but they are not effective.

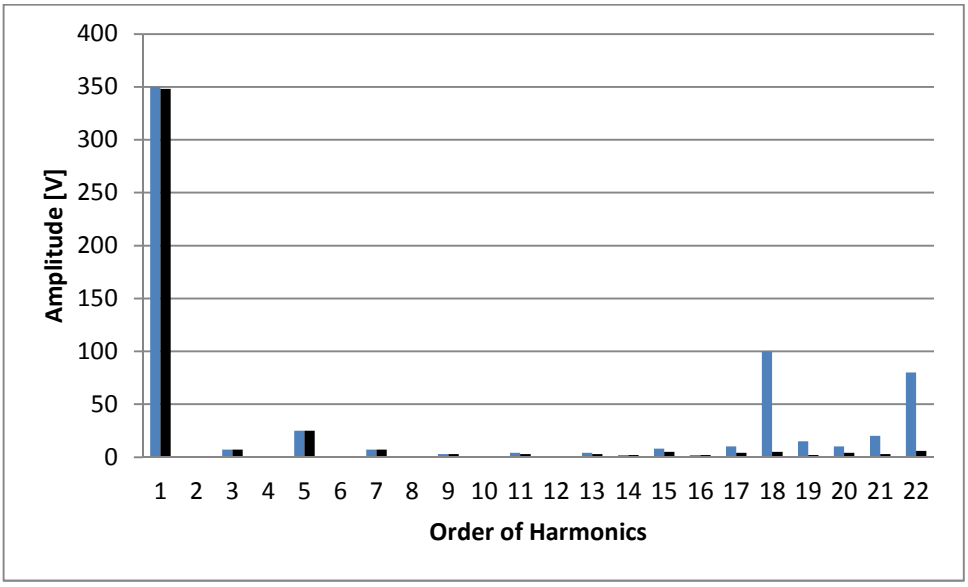


Fig.4.128: Harmonics at the input and output of the RLC low pass filter

Fig.4.129 presents the output of the filter and output voltage of the converter along with the related PWM switching pattern. This figure shows that the output voltage of the converter is a chain of pulses with amplitude of ±500 V which are consistent with the switching pattern generated by the PWM generator. Meanwhile the output of the filter is a sinusoidal waveform.

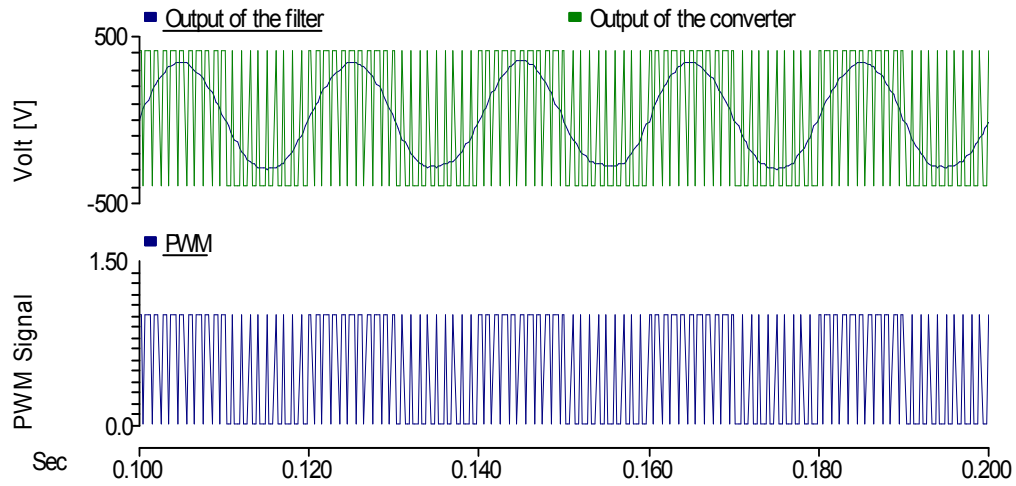


Fig.4.129: Output voltage of the filter and converter along with the switching pattern

The output voltage of filter and the output of the converter are also represented in Fig. 4.130 and Fig.4.131 for 5 cycles. The observation of these two waveforms shows the satisfactory operation of the filter. However it requires a proper tuning of the filter. Tuning of the filter is a key factor in achieving satisfactory results. The output of the converter must be carefully monitored and a harmonic analysis must be conducted in order to have a good evaluation of the existing harmonics. In order to avoid any resonance and at the same time to eliminate the harmonics, the cut off frequency of the filter is chosen smaller than the frequency of first dominant harmonic which must be eliminated. In this study the frequency of first high harmonic is 900 Hz which has order of 18th and the cut off frequency is set to 112 Hz. The selected cut off frequency is smaller than the dominant harmonic and will eliminate all the higher harmonics.

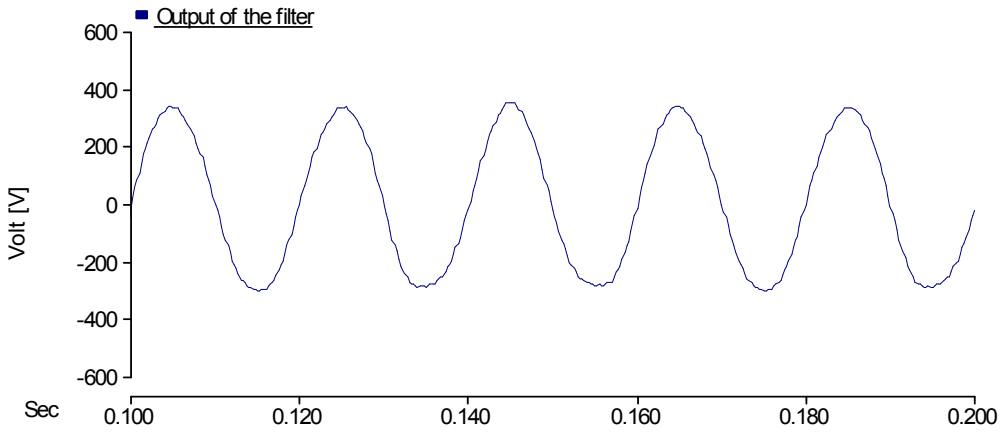


Fig. 4.130: Output voltage of the filter

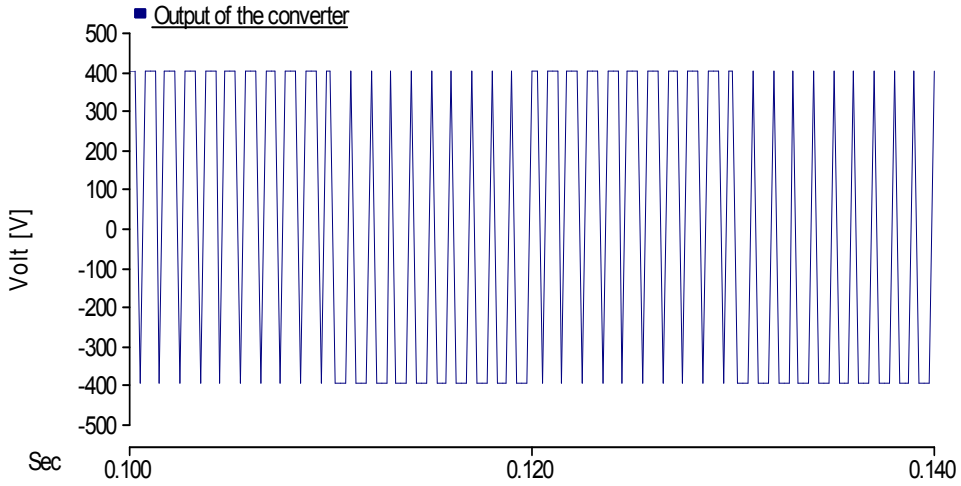


Fig.4.131:Output voltage of the converter

4.13 Summary

In this chapter, in order to avoid using dq conversion and provide a compensation which is independent from line current a new closed-loop control strategy based on the exchange of instantaneous power is proposed. The control guarantees an orthogonal injection of voltage with respect to the line current. It also optimizes the active power absorption by the DSSC device and holds the DC voltage at desired value at the same time.

The DSSC device was modelled by dividing its modes of operation into two categories. In mode 1 IGBT's 1 and 4 within the DSSC device are conducting and IGBT's 2 and 3 are off. In mode 2 IGBT's 1 and 4 are switched off and IGBT's 2 and 3 are conducting. Based on these two modes of operation and considering equivalent impedance of the system in each mode, transfer function of system was obtained.

The obtained transfer function is used in designing of a controller. The controller stabilizes system by inserting zeros and the proper location of the zeros are found using SISTOOLS of MATLAB. Stability study is conducted using step response of the closed loop system when the designed controller is employed. In addition, effect of change of system parameters on the performance of the designed controller has been investigated. Change of system parameters includes change in the capacitance of DC capacitor, AC capacitor (filter capacitor) and inductance of filter. These parameters do not put stability of system at risk as long as their changes are limited to 10%. In sensitivity analysis, effect of adding a low pass filter to the proposed controller was investigated. Bode diagram of filter was plotted and it has been observed that filter does not have any attenuation or phase delay in the DC and the data which is being used by controller is in the DC.

The performance of the DSSC and the proposed controller has been studied using PSCAD. This study employs, an 11kV distribution network comprised of two parallel lines are connected to an 11kV substation at one end and supplying a lumped load at another end. The amount of compensation as a percentage of line reactance can be determined by adjusting the amplitude of the injected voltage. This study has demonstrated that the applied control system is capable of injecting both capacitive and inductive reactances through the line.

In comparison with 90° phase shift approach the proposed controller has managed to reduce the phase angle difference of injected voltage with respect to the line current. In the same time reduces the level of injected harmonics through the line by DSSC when

proposed controller has been used.

Comparison of performance of the proposed controller with dq based controller demonstrates independency of the proposed controller from the unbalance currents of three phase power system. Reference signal in the dq based controller is affected and their amplitude are not same. Then DSSC device can provide compensation which is differed from the demand. However, proposed controller shows that regardless of unbalance current and voltages in the three phase system, DSSC is able to inject same voltages in each phase as per demand.

The proposed controller in comparison with the controller which is using only DC link voltage regulator demonstrates better performance with respect of injection angle. When only DC voltage regulator has been used the injection angle is diverting from the target (90°) and it is oscillating. Diversion from the target angle means the capacitive or inductive injection is not purely reached.

Sensitivity of controller with respect to the change of power system parameters has been studied. This study includes power system parameters changes such as line resistance, voltage sag swell and reconfiguration of the network. The results show satisfactory performance of controller in injection of the series voltage through the line and regulating of the DC voltage.

A fault management study has been conducted in order to find best fault recovery solution in occurrence of fault within the system. When only converter (within the DSSC) is blocked DC voltage can exceed the limit which is not desired. In another scenario, when STT become open circuit -regardless of blocking or deblocking of converter- there will be high AC voltage in either side of the STT which makes this solution to be unpractical. Blocking the converter along with bypassing the STT holds the DC voltage in pre fault value and avoids a high voltage in the STT in the same time.

5 Experimental Results

Although the proposed control and its performance is well simulated using PSCAD/EMTDC, however, a laboratory test bench is needed in order to conduct experimental tests and validate the simulation results. To do so, based on the available lab facilities in the Upper Ground (UG) lab at Newcastle University, a low voltage test bench is designed and implemented. The overview of the test bench is shown in Fig.5.1. As can be seen, it includes DSSC device and low voltage power system.

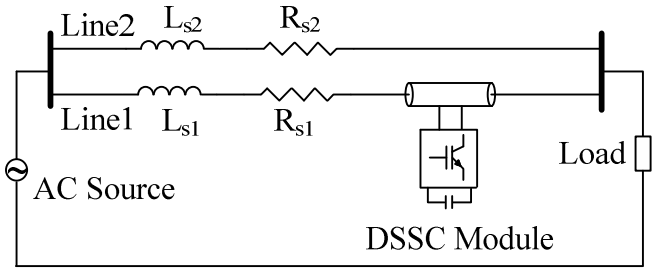


Fig.5.1: The overview of the inside of the test rig

The power circuit of the DSSC device comprises of a voltage source H-bridge converter (VSC), a single turn transformer, a DC capacitor serving as a DC link, an LC filter. The control electronics is digitally implemented using dsPIC33F microcontroller, electronic measurement, control boards and a DC power supply. In this device, a 500µF capacitor, rated at 1.5 kV is used as a DC link to hold the DC voltage provided by the converter. Converter itself is a full H-bridge IGBT module, which is connected between DC link and LC filter. The LC filter is located between the converter and a single turn transformer. It is built up of a capacitor and an inductor. The filter is a low pass filter, designed to eliminate high order harmonics generated by the converter. As a result, it can provide a non-distorted sinusoidal waveform at the secondary of the STT.

The single turn transformer is a cylindrical shape transformer. Its primary winding has just one turn and it is the power line itself. In the compensated electrical networks it is supposed to be suspended from the lines.

The dsPIC33F microcontroller is used to process the incoming signal from the system and to run the control algorithms. The incoming feedback signals from the system, have been provided by the electronic measurement boards. Also another electronic board has been designed serving as an interface between the output signals from the controller and the converter.

The 11 kV power distribution feeder is modelled by a 50 volts power system. This low voltage is chosen according to the maximum voltage permissible by the rules and regulation of health and safety in the UG lab. The system comprises of a 30mH inductor representing the inductance of the line and in series with a 6 Ohm resistance demonstrating the ohmic resistance of the line. The power system is supplied by a 220:50 transformer with a maximum current of 15A. The galvanic isolation between the test rig and the main power supply in the lab is achieved by supplying the 220:50 transformer with a unity-ratio isolation transformer. This will protect the main power supply in the lab from any probable fault which may occur during the experimental tests.

The power system as shown in Fig.5.1 is a single phase line and there is only one DSSC device connected in series with it. At the end of the line there is a load through which the line current is passing. Also, in order to demonstrate that the DSSC module is operating correctly, contributing toward the power flow control in the system, there must be another parallel line to supply the load. This extra parallel line will facilitate this by changing the reactance in the compensated line to be able to change the amount of current passing through the compensated line and consequently in the parallel line. For this reason another parallel line, exactly with the same characteristics as the first one is also provided in the test rig. As stated earlier, the parallel line will only be used in the power flow control test.

Having designed and built of the test rig the proposed control strategy implemented on the microcontroller and it is executed to conduct experimental tests to validate the simulation results. The capability of control system in generating capacitive and inductive injected voltage is examined in this chapter. In addition its efficiency is compared with the traditional control method.

5.1 H-Bridge Voltage Source Converter

The main power electronics device in the DSSC unit is the H-bridge voltage source converter. The converter as shown in the Fig.5.2 comprises of four IGBT and four anti-parallel diodes. The dc side of the converter is connected to the DC capacitor, whereas the AC connection points are connected to the LC filter. The maximum current passing through (when IGBT is conducting) and the maximum continuous voltage across the IGBT (when it is off) needs to be considered carefully. In the same time its power rating is also important parameter in the selection of IGBT.

The selected DC capacitor is rated at 1.5 kV, therefore in the worst case the maximum voltage of the DC link will be controlled not exceeding 1.5 kV. For this reason the maximum continuous voltage across each IGBT will not exceed 0.75 kV in steady state. However, Transient Over Voltage (TOV) can be higher. Regarding to the rated current, the nominal current of the 220:50transformer connected to the power system is 15A. As a result the resistors including the connected load to the system has the same range of nominal current. The current in the secondary side of single turn transformer depends on the turn ratio of the STT, let say n, and it will be n times smaller than line current. It is obvious that normally n is a number between 1 and 100 and that the current in the secondary side, not only cannot exceed 15A, but also it will be much less than current in the primary side.

Another important factor in the selection of IGBT in the design process is the I_C (collector current of IGBT) versus V_{CE} (voltage across the collector-emitter of the IGBT) curve for different V_{GE} (voltage across the Gate-Emitter). This curve normally is provided by the manufacturer and it is shown and explained in appendix B [91].

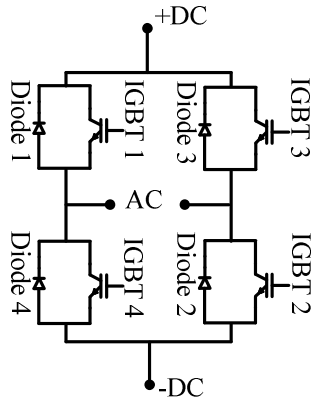


Fig.5.2: H-bridge voltage source converter

In the design of DSSC device, based on the aforementioned ratings for voltage and current, the IGBT module SK20GH123, manufactured by Semikron, is chosen for building up the converter used in the DSSC.

It can be deducted from I_{CE}-V_{CE} curve which is well explained in appendix B that the IGBT can initiate a current flow even with V_{GE}=7 volts but the current will not exceed 3A. For this reason and in order to reach the rated current flow, high V_{GE} is required.

In order to meet all these requirements in the design of gate driver board, the turn-on voltage for the IGBT's inside the SK20GH123 device is set to 15 volts. Additionally, a negative gate voltage is required to turn off the switch and provide immunity against

dv/dt. The lowest range of turn-off voltage for the selected IGBT is -20 V. However lower gate voltages, similar to higher turn-on gate voltage, can cause a permanent damage to the device and at the same time low negative gate voltage can be problematic as well. Because there is a series resistance inside the gate of IGBT and low gate voltage can lead to a slow switching.

In order to turn on the IGBT and let current flows from the collector to the emitter there must be a positive voltage across the collector-emitter and gate-emitter terminals. Referring to the data sheet [91] of the selected IGBT, $V_{GE\ (th)}$ is in the range of 4.5 V - 6.5 V and the typical voltage is 5.5 volts. Moreover the details of gate leakage current and other parameters in general and especially for the selected IGBT can be found in [91] and appendix B. The IGBT cannot be turned on or off directly by the controller itself, hence there must be buffering interface between them. The interface board, not only provides proper voltage and current to drive the IGBT, but also isolates the power switches, IGBT's, electrically from the microcontroller.

5.2 Gate Driver Board

Gate driver board is mainly employed to convert control signals such as switching pattern to a proper voltage or current in order to turn on or off the IGBTs. At its output, it must provide the required turn on or turn off energy for the related IGBT. To do so, the outer level power supply and the series resistor (gate resistor) must be chosen carefully in order to provide a current with proper amplitude to charge or discharge the IGBT with minimum possible time. A gate driver board is composed of two different parts and a typical plan of this board is shown in Fig.5.3. The first part is called *Buffer* which is directly connected to the microcontroller and the second part is called *Gate Drive* and is located between buffer and IGBT. Four buffers provide the required current for the gate drive, otherwise it is not possible for the microcontroller itself to feed all of the gate drives.

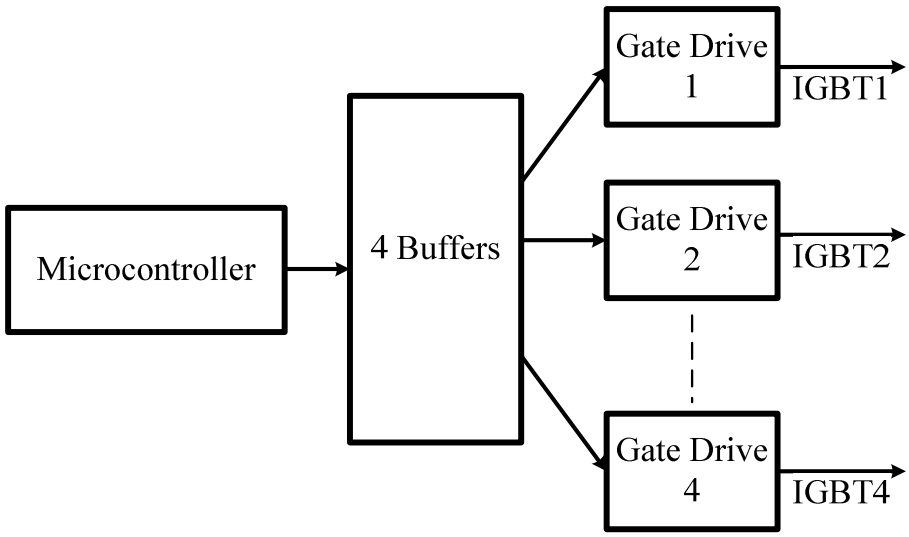


Fig.5.3: Typical layout of Gate Drive Board

In order to guarantee high impedance between microcontroller and the gate driver a proper buffer is required to avoid sinking too much current from the microcontroller. To do so, based on the output voltage of the microcontroller, 5 volts, and input voltage of the gate drive, 5 volts, the chip SN74AHCT125N is selected for its current sinking capability [92]. Also it is compatible with a supply voltage of 5 V which can easily be provided by many of the ordinary DC power supplies and will avoid a need for special DC source.

In [93] the range of supply voltage is specified between 0.5 and 7 volts however the recommended supply voltage is given between 4.5 V and 5.5 V. For this reason, V_{CC}, is defined to be 5 volts.

Another important component in the gate drive board is gate driver. It provides the turn-on and turn-off voltages directly. In most of the designs for IGBT, it also provides the adequate amount of power to charge and discharge the gate of IGBT. Additionally, gate drive must isolate the signal level from the power circuits and usually this can be achieved by an integrated opto-coupler within the gate drive. It must be well-matched with the carrier frequency of PWM pulse generator in order to transfer the generated signals to power converter and to be fast enough to correspond to the changes in the input. Some electrical features such as input and output voltages and currents must be compatible with the related parameters in the connected device.

For example when output voltages of the bufferSN74AHCT125N, is 5 V and its output is an input to the gate drive, then the input of the selected gate drive needs to be 5 Volts. Similarly, the input current of the selected device must not exceed the 12 mA limit

which is the designed output current for the buffer as explained earlier in part 6.3.1. In addition, the PWM signal frequency depends on the different test scenarios and is expected to vary between 1 KHz and 10 KHz and the gate drive must have enough bandwidth to deal with the generated signals.

It is also required that the supply voltage feeding the device can easily be provided by normal DC power supplies. Based on all of the aforementioned requirements, the opto-coupler HCPL-3180 device is selected. Its features and further technical data can be found in Appendix B.

However gate drive (gate drive component) needs an "isolated power supply" in order to provide the required voltage for turn-on and turn-off of the IGBT. It is like a DC power supply which can provide voltage and reference ground. This is because firstly the output voltage of the gate drive is less than 15 V and this will not be able to force IGBT to conduct fully. Then there is a possibility that the flow of current through the device not to reach the rated current. Secondly, in the H-bridge converter two IGBTs (IGBTtop and IGBTbot) are connected in series in such a way that the emitter of top IGBT is connected to the collector of the bottom IGBT. For this reason the voltage of emitter will be depend on the ON or OFF status of the bottom IGBT. In order to avoid floating voltage across the gate-emitter, the use of an independent power supply is necessary to guarantee the required voltage across the gate-emitter.

Based on the electrical requirements specified in the appendix B in terms of input, output currents and voltages, the NMF0515S isolated power supply is selected to be employed in the board. It converts 5 volts at the input to 15 volts at the output. Since the isolated power supply is a DC/DC converter and is connected to the power circuit, it must have sufficient insulation for high voltages in order to operate safely in such voltages. Additionally, it is necessary that the selected device has enough isolation capacitance in order to avoid any dv/dt issue. The NMF0515S power supply, the selected device, is isolated for 1000 V, which is much higher than the expected DC voltage across the DC link in the converter [94].

Another important consideration in the design is the maximum peak gate current. Refer to appendix B and data sheet of selected component [94] the gate current must not exceed 2.5 A; however practically because of negligible impedance of output circuit of the gate drive it is not possible. Therefore, the current must be controlled by adding a series resistor between the gate drive and IGBT. The resistance can be calculated as follow:

$$R_G = \frac{\Delta V}{I_{Peak}} \quad (5.1)$$

where R_G is the resistance of series resistor between the gate drive and IGBT, Ipeak is the maximum peak output current of gate drive. The ΔV represents the variation of the required gate-emitter voltage for turning on and off of the IGBT. For the SN74AHCT125N the maximum output current is 2.5A and for the IGBT the ΔV is 30V. Therefore:

$$R_G = \frac{30}{2.5} = 12\ \Omega$$

R_G, under any conditions, must not be smaller than 12 Ω otherwise the peak current will exceed the permissible output current of gate drive. However, practically the impedance of the gate drive circuit is not zero and it will contribute toward the R_G and the peak current will be less than 2.5 A. Furthermore this current will decay as the gate capacitance in the IGBT charges up. But the value of peak current is a key factor in charging up time of the gate circuit in the IGBT. This is because with higher peak current the charge up time will be less and this will increase the efficiency of the switching and will reduce the switching power losses. This is because with smaller resistor the gate capacitance will charge and discharge quickly and switching will take less time.

On the other hand, the smaller external resistor will increase the immunity against the dv/dt in the gate circuit. However smaller value of external resistor can increase di/dt stress through the free wheel diodes in the converters which are connected to an inductive loads. This can create a transient over voltage across the switches also it can generate an oscillation. In order to solve this problem, a higher external resistor value is required but it will increase the switching losses. In each switching event current flows through the resistor and increasing the resistance will increase the losses. For this reason sometimes having two different external resistances, one for charging the gate capacitance in the IGBT and the other one to discharge the gate capacitance are used. In order to have two different external resistors the gate drive itself must have two different outputs but this can increase the complexity of design and implementation of the gate drive board which is not necessary in most of the cases. Especially when the switching frequency is quite low then there is no need to have separate charge and discharge gate circuits.

5.2.1 *Design of gate drive board*

Detail of the design is presented in Fig.5.4 and it can be clearly observed that the input signals are first fed into the buffer, SN74AHCT125. Then the related output signals are connected to four gate drives, HCPL-3180, via series resistors and the resistors are controlling the current flowing between buffer and gate drive. The gate drives are supplied by isolated power supply, NMF0515S, and they operate like a DC-DC converter and always provide a fixed voltage of 15V volts between P3 and P5.

This voltage appears at the output of gate drive, between pins 8 & 6 or between 5 & 6, and provides the gate-emitter voltage via a series resistor.

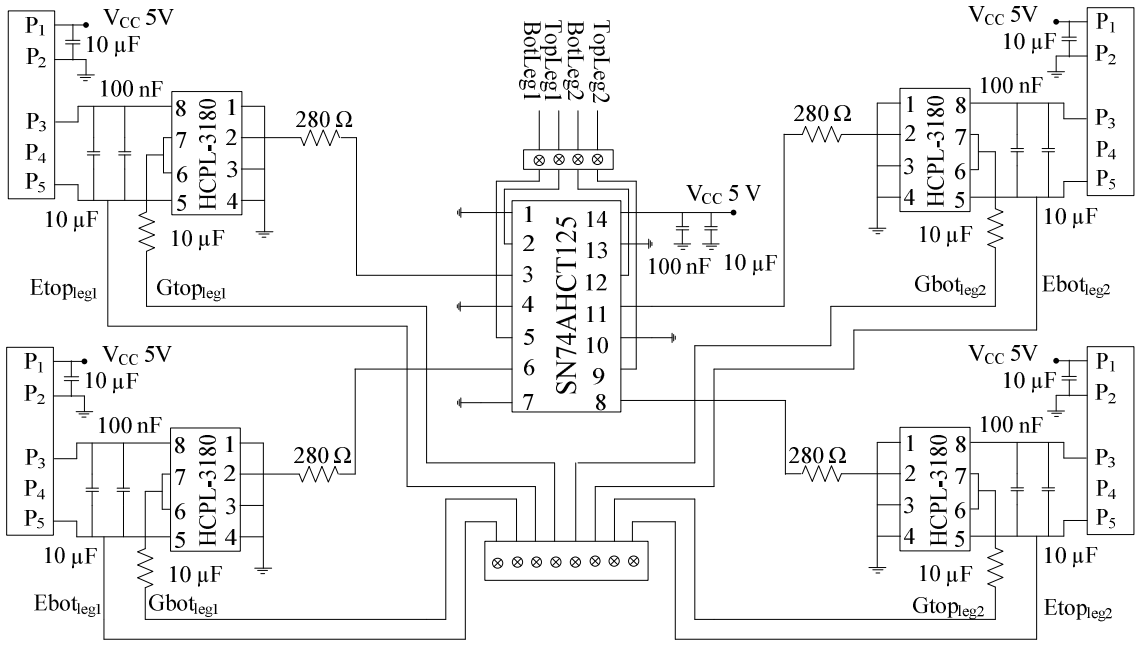


Fig.5.4: Design of the gate drive board

5.3 Voltage Measurement Board

Generally measurement is a key factor in the control systems especially when the measured parameters are used as feedback signals in the control blocks. The capability and performance of the controller can be affected by accuracy of the measurement. In the proposed control strategy, instantaneous value of DC voltage and injected AC voltage are two important inputs along with the instantaneous line current for the controller.

To provide these two voltage inputs for the controller two voltage measurements have been designed and implemented. The voltage measurement board includes two main

different parts. The first part is a voltage transducer (VT) which is connected in the primary side in parallel with the target points to measure the potential between them. The second part is a combination of op-amp circuits that are providing desirable signal to the microcontroller. The selection of the VT depends on the expected maximum and minimum voltage between the points that VT will be connected and also the accuracy of measurement which is demanded by the control system.

Each VT, like any electrical equipment, has rated values for certain input and output voltage and current which specified by the manufacturer. In the same time the mentioned parameters must be matched with the expected measured voltages. For example the DC voltage across the DC link and AC voltage across the secondary side of the single turn transformer (STT) in the laboratory prototype DSSC module is not expected to exceed 500 volts (however the employed capacitor is rated up to 1.5kV in order to withstand to transient over voltages). For this reason, in the voltage measurement board design the nominal primary voltage is planned to be 500 volts. Based on the design requirements and the available VT in the market and having considered their accuracy, the voltage transducer LV 25-P has been selected [95].

Refer to the device data sheet [95] and appendix B the optimum accuracy of the device can be achieved if the primary input current in the measuring of the nominal voltage become 10 mA. In order to obtain such accuracy in our design the external resistors in DC voltage measurement board and AC voltage measurement board have been selected so that when measuring 500 V and 200 V respectively the corresponding currents to be 10 mA. To do so, Re the external resistor, can be calculated as follow:

$$R_e = \frac{V_{PN}}{I_{PN}} \qquad (5.2)$$

In equation (5.2) V_{PN} is the measured voltage and I_{PN} is the primary current in the input of transducer. Considering the maximum peak value of injected voltage by DSSC in the prototype system, the voltage is expected to not exceed 200 volts in the power electronic side. This is the voltage that needs to be measured by AC voltage measurement then the V_{PN} in this board is 200 volts. For example, with substituting this value and 10 mA as input current in equation (6.2), R_e is calculated as follow:

$$R_e = \frac{200\ \text{V}}{10\ \text{mA}} = 20\text{k}\Omega$$

R_e is selected to be 20kΩ and similar calculation can be done for $R_e$used in DC voltage measurement board. In this board the nominal measured voltage is assumed to be 500V then the Re is calculated to be 50kΩ. Then with having 20kΩ and 50kΩ resistance at the

input of the VT the accuracy of the measurement refer to appendix B will be 0.8 % in both boards.

Another element which is used more frequently in both DC and AC voltage measurements is Operational amplifier (Op-amp).In order to alter some electrical features of measured signals using specified circuits and provide the desired electrical signals. However care must be taken in selection of Op_amp because a device with poor slew rate can generate a nonlinear effect in the circuit. For this reason especially in the measurement circuits design the slew rate of the employed devices becomes more important because any nonlinearity in the measurements can cause instability in the system. In the voltage measurement board, the LMC660CM is selected to be used in the design. Because typical slew rate of the LMC660CM is 1.1 V/µs; however refer to the data sheet of the device [96] and appendix B a minimum slew rate of 0.8 V/µs is guaranteed at the ambient temperature.

5.3.1 Design of voltage measurement board

The voltage measurement board includes electronics circuits and a voltage transducer (VT). VT is located between the electronics part and power circuit and isolates these two parts electrically. As a part of the design process an external resistor needs to be used to limit the input current which is explained earlier in pervious subsection. By having 10mA input current the output current of the VT, considering the turn ratio of 2500:1000, will be 25mA. Considering Kirchhoff Current Law at the output of the VT the KCL equation can be written as follow:

$$i_O = i_1 + i_4 \quad (5.3)$$

where i_O is the output current of VT and i_1 and i_4 are the current passing through R_1 and R_4 in Fig. 5.5.It is noted that i_1 is almost negligible because the input impedance of the op-amp is high and in ideal condition the current passing through it is zero. Substituting i_1 equal to zero in equation (6.3) it can be concluded that:

$$i_O = 0 + i_4$$

$$i_O = i_4$$

It means that the output current of the VT wholly passes through the R_4. As a result there will be a voltage drop across the R_4 which can be calculated as follow:

$$v_O = i_4 * R_4 \quad (5.4)$$

Using the corresponding values V_O can be found as follow:

v_O= 25 mA * 100 Ω= 2.5 V

In the circuit the output of the VT is connected to a low pass filter which can smooth the measured signal by bypassing the high frequency signals. The gain for the low pass filter can be written as follow:

$$v_{Out} = -v_{in}\frac{X_{C_1} \| R_2}{R_1} \quad (5.5)$$

where V_{Out} and V_{in} are the output and input of the filter, X_{c1} is the reactance of the capacitor. As the frequency of the input signal goes high then the reactance of the capacitor will go to the zero and then the gain will be zero. When the frequency of the signal goes down the reactance of the capacitor will go high and then only R_2 will affect the gain. So, for the low frequency signals the gain will be:

$$v_{Out} = -v_{in}\frac{R_2}{R_1} \quad (5.6)$$

As it can be clearly observed from equations (5.5) and (5.6) the designed low pass filter is inverting (180 degree phase displacement) the signal as well. Therefore the signal needs to be inverted once again in order to return it back to the original phase. In the same as the measured voltage is an AC voltage then it has positive and negative amplitude repeatedly during each cycle. However the microcontroller requires a positive signal between 0V and 3.3 volts. In order to meet these conditions the final signal must vary between the mentioned voltage bands. To do so, after low pass filter circuit another circuit is needed while inverting the signal gives the required offset and adjust the amplitude of the final signal. For this reason an inverting op-amp circuit along with the offset bias circuit is added immediately after low pas filter circuit in this design. However there could be other solutions which can avoid using multiple Op-amp circuits. The bias circuit is just adding up some value on top of the signal in order to guarantee that the final signal will not go to negative. The added value can be calculated as follow:

$$v_{bias} = \frac{VSS * R_7}{R_8 + R_7} \quad (5.7)$$

where V_{bias} is the added value. Substituting the corresponding values into equation (5.7) the V_{bias} can be calculated as follow:

$$v_{bias} = \frac{12*1}{13+1} = 0.85$$

However gain of the inverting Op-amp circuit along with V_{bias} is:

$$v_{Out} = -v_{in}\frac{R_6}{R_5} + 0.85 \quad (5.8)$$

and substituting the corresponding values, V_{Out} can be calculated as follow:

$$v_{Out} = -v_{in}\frac{10\,\text{k}}{10\,\text{k}} + 0.85 = -v_{in} + 0.85$$

After this op-amp circuit there are two protective diodes which they are connected between final output and ground and a node with potential of 3.3 volts. The aim is that if with any reason the amplitude of output signal becomes less than 0 V or greater than 3.3 V then the related diode will conduct and consequently the microcontroller will be protected. All of the aforementioned circuits can be seen in the Fig. 5.5. This figure shows the design of voltage measurement board which is obtained using Multisim software.

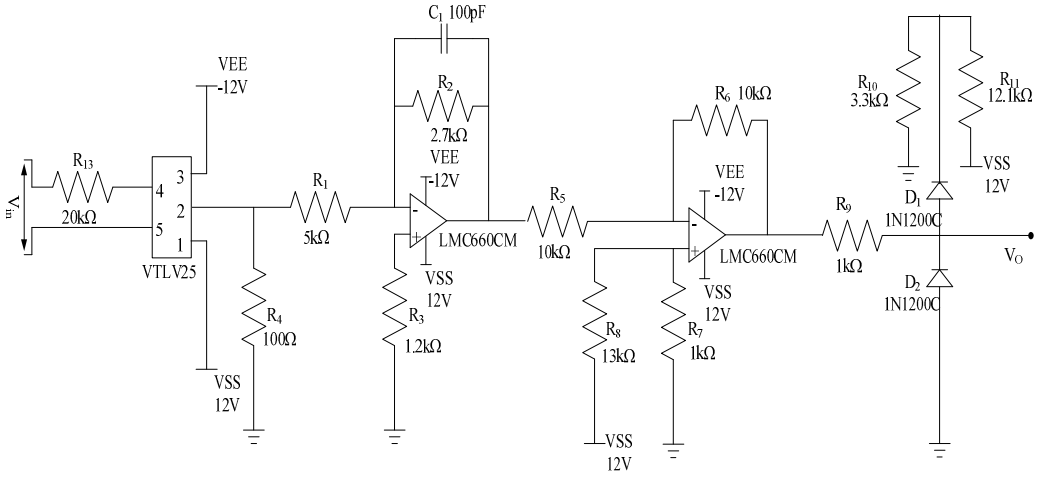


Fig. 5.5: Design of Voltage Measurement Board

5.4 Current Measurement

Current measurement board is used to monitor current waveform through the power line. As the DSSC current is linked to the power line current via a single turn transformer then the monitored current waveform includes the instantaneous information of the current inside DSSC as well. However based on the proposed control strategy the injected voltage must be in orthogonal with the line current. For this reason, the line current itself is directly monitored and fed to the microcontroller so that it can be used by control algorithm.

The accuracy and precision of the current measurement board becomes more important which must be considered in the design process of the board. It comprises of a Current Transducer (CT) and an electronic circuit. The CT is fed by the measured current and provides a voltage type signal at the output. This voltage is fed to the electronic circuit and the circuit provides a proper signal at the output.

One of the major criteria in the selection of CT is the maximum primary current that CT can take at the input. However in the designed prototype test rig based on the UG lab

facilities, the maximum current in the power line will be 15 A then in terms of the maximum input current any CT with input current above 15 A will be fine. In terms of required supply voltage of CT, it is desirable to be in the standard voltage range then it can be easily provided by the standard DC power supplies. Also, it is required that the selected CT be mountable on the PCB board in order to facilitate its employment along with the electronic board within one PCB board.

The most important feature of CT is its accuracy as it can affect the proper operation of control system. Considering all the aforementioned futures the LTS 25-NP Current Transducer has been selected for the current measurement board. More information regarding the selected CT and check against the required design criteria can be found in the appendix B.

The selected CT has capability of measuring current of up to 25 A which is enough for our purposes [97]. Also it requires 5 volts as supply voltages which can be provided by most of ordinary standard DC power supplies.

The output voltage can be defined as [72]:

$$V_{out} = 2.5 \pm (0.625 * I_P/I_{PN})V \quad (5.9)$$

where V_{out} is the output voltage and I_P and I_{PN} are the primary current and nominal primary currents, respectively. The current measurement board is designed for nominal current of 25 A then by substituting I_{PN} with 25 A the equation (5.9) can be rewritten as:

$$V_{out} = 2.5 \pm (0.025 * I_P)V \quad (5.10)$$

From equation (5.10), it can be clearly argued that the output voltage has offset of 2.5V. That means even with zero input current the output voltage is 2.5 volts and it must be considered in the design.

5.4.1 Design of electronic circuit of current measurement board

Electronic circuit of the current measurement board comprises of different op-amp circuit which are in cascade connection. The first part, as shown in Fig.5.6, is a Non-Inverting Amplifier. It is the first point of connection to the CT. As explained in section 5.4 the output voltage of the CT includes 2.5V DC voltage and it must be bypassed in order to pass the alternating part of the output voltage. Actually only the alternating part of the voltage includes information about the measured current for this capacitor C_1 is located between the Op-amp circuit and CT and it bypasses the DC voltage.

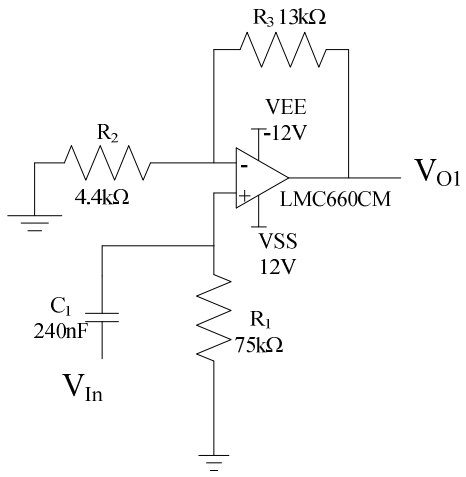


Fig.5.6: Non-Inverting Amplifier

The output voltage of the amplifier, shown in Fig.5.6, can be calculated as

$$V_{O1} = \frac{R_2+R_3}{R_2} * V_{in} \quad (5.11)$$

where V_{O1} is the output voltage of the amplifier and V_{in} is the input voltage. Substituting R_2 and R_3 in equation (5.11) with 4.4kΩ and 13kΩ the equation (5.11) can be rewritten as

$$V_{O1} = 3.95 * V_{in} \quad (5.12)$$

Equation (5.12) shows that the gain of amplifier is 3.95. Considering the input voltage margin of 0.375 V for the maximum input current of 15 A the V_{Out} will be 1.48 V.

It means that V_{O1} will vary between -1.48V and 1.48V. However the negative voltages are out of the acceptable input voltage margin of the microcontroller. In order to bring signal into the acceptable margin some other op-amp circuit are required. The complete electronic circuit of the current measurement board is shown in Fig.5.7. In this circuit, after the Non-Inverting Amplifier there are two cascaded Inverting Amplifiers. The first one is just inverting the signal and the relation between its output and input can be written as

$$V_{O2} = -\frac{R_5}{R_4} V_{i2} \quad (5.13)$$

where V_{i2} and V_{O2} are the input and output of the first inverting amplifier. Equation (5.13) is a general formula, thus it can be applied to all inverting amplifier circuits. With substituting values of R_5 and R_4 into (5.13) it can be rewritten as

$$V_{O2} = -V_{i2} \quad (5.14)$$

The second inverting amplifier includes some DC offset while it is inverting the signal. The relation between its output and input can be written as

$$V_{o3} = \frac{R_9}{R_6} V_{i3} + V_{DC} \quad (5.15)$$

where V_{i3} and V_{O3} are the input and output of the second inverting amplifier circuit and V_{DC} is the DC offset. The DC offset is just shifting up the signal in order to avoid appearing any negative signal at final output of the measurement board. V_{DC} is provided by a voltage divider and can be calculated as

$$V_{DC} = \frac{R_8}{R_8 + R_7} * 12 \quad (5.16)$$

Substituting the values of R_8 and R_7 into equation (5.16) the V_{DC} becomes 1.6V. In continue in equation (5.15) by replacing the values of R_9 and R_6 and VDC it will become

$$V_{o3} = -V_{i3} + 1.6 \quad (5.17)$$

It is argued earlier that the V_{O1} will vary between -1.48 and +1.48 then by using these values in V_{O2} and V_{O3} the final output V_O will be as

$$V_O = \pm 1.48 + 1.6 \quad (5.18)$$

$$V_O = 3.1 \quad Or \quad V_O = 0.1 \quad (5.19)$$

Based on equation (5.19) the final output voltage of the measurement board is located in the permissible margin of the input voltage of the controller, which is between 0 V and 3.33 Volts. However a protection for the microcontroller input is needed just in case the output voltage goes beyond the safe margin. To do so, two diodes are connected the output and they will conduct if the output voltage become more than 3.2 V or less than -0.6 V. In the former D_1 and in the latter D_2 will conduct.

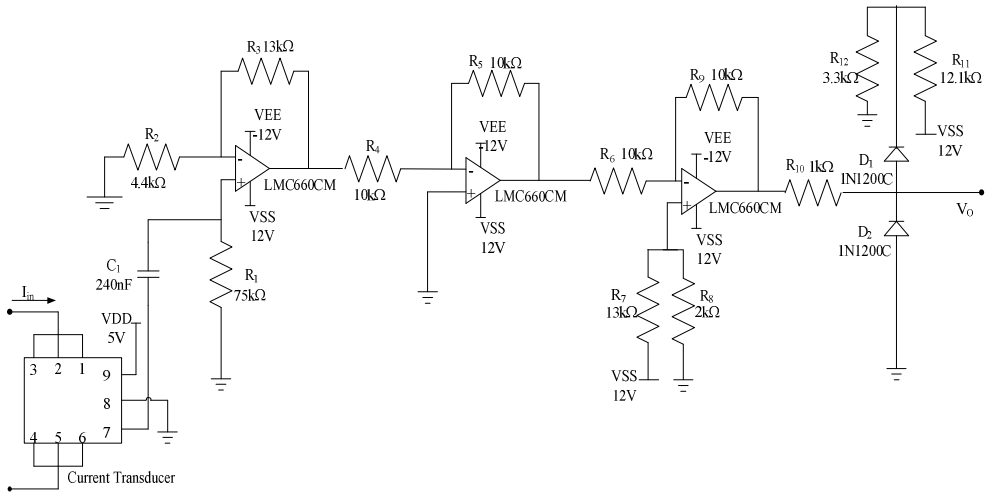


Fig.5.7:Full circuit of the current measurement board

5.5 Single Turn Transformer (STT)

Single turn transformer mainly consists of a cylindrical core and a secondary winding. The primary winding is the power line itself which is passing through the cylindrical core. The core is made of two parts, clamped to each other to make a complete cylinder. This makes the mounting and dismounting of device to be simple. However in the practical design there is an air gap between the parts and will be included in the magnetic path of the flux.

The secondary winding is wound on the core, as shown in Fig.5.8. This winding is coupled to power line like a conventional transformer. As the current flowing through the power line it induces current in the secondary winding. However the induced current is much lower than the line current. Actually it is reduced by the turn ratio of transformer, let say 1:100, and even in the case of short circuit just small proportion of current can pass through the power electronic circuits before bypassing the STT in the secondary side by mechanical switches.

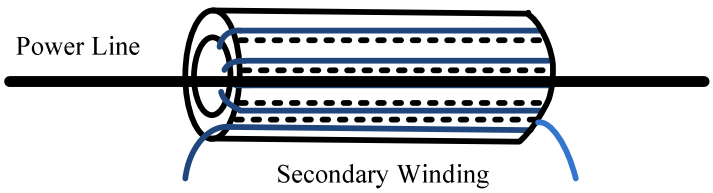


Fig.5.8: Single Turn Transformer

The STT can operate in two different modes of functionality. First mode of operation occurs when the secondary side is bypassed by a mechanical switch. By shortening the secondary side secondary voltage will be zero and the induced voltage at the primary will be zero. In this case, there is no injection in the primary side except the injection of leakage inductance which is negligible and has no effect on the proper operation of the power system. In the second mode of operation, the secondary winding is connected to the converter via a low pass filter and the generated voltage by the H-bridge converter is injected by STT. Because the injected voltage can lead or lag the line current then as a result of injection inductive or capacitive reactance can be induced through the line.

The maximum reactance which DSSC can be injected through the power line depends on the magnetizing inductance, X, of the STT. The magnetizing inductance is equal to the self-inductance of the power line (or primary winding) and is related to the reluctance of the core of STT. In cylindrical core distribution of the air gap between

line and core is identical around line and reluctance in different points of the core can be calculated as follow:

$$\mathcal{R} = \frac{2\,\pi r_1}{\mu(\,r * l)} \qquad (5.20)$$

In equation (5.20), r is the thickness of the core as shown in Fig. 5.9 and r_1 is the distance of the calculated point from the centre of the cylinder. In this equation, l is the length of the cylinder and μ is representing the permeability of the material of the core.

The reluctance of magnetic path in the core is highly dependent on the permeability of the material. For this reason by introducing air gap in the magnetic path the reluctance can be increased. Air gap in magnetic path of STT is unavoidable and it has been introduced by gap between the two parts of the core. These two parts are clamped to each other in order to create a circulation path for the flux. However increasing the reluctance of the magnetic path in presence of air gap is desirable. Because in the transmission and distribution lines the flowing current can be very high and consequently the core can be easily saturated which can affect the proper operation of the DSSC.

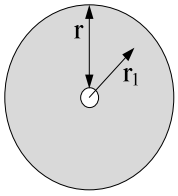
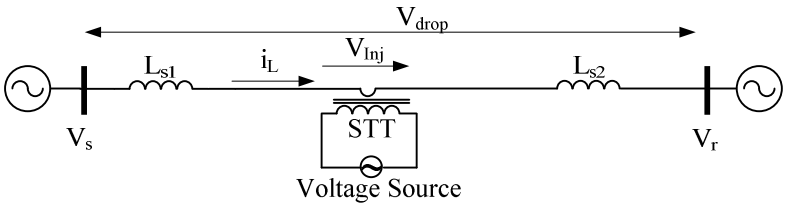


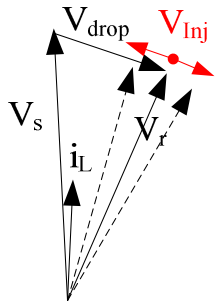
Fig.5.9: Cross section of the STT core

By creating an air gap the magnetizing inductance of STT can be tuned to the desirable value. In spite of this, in the design of laboratory prototype model of STT the air gap is not considered. Because it is used only in the laboratory test rig and there is no need of to be made of two parts in order to ease off the mounting and dismounting the device through the power line. Additionally, as the applied current in the power system in the test rig is considerably low and will not exceed 15A then with the intention of increasing flux density in the core the STT is made of just one cylindrical core. However, full design steps of the single turn transformer that can be used for an 11kV distribution network is explained later in this chapter.

The connection of DSSC device and relations between the current and voltages are shown in Fig.5.10.



a) STT is injecting a voltage source through the line



b) Relation between the voltages in a compensated power system

Fig.5.10: The connection of DSSC device and relations between the current and voltages

The maximum voltage that STT can inject highly depends on the design of its magnetic core. The magnetic permeability of core must be high enough in order to provide proper reluctance for the generated magnetic flux by the power line. This will increase the coupling of the transformer and efficiency of the device. The core chosen is made of non-oriented silicon steel laminations, which is called M33035A, with maximum flux density of B= 1.5 T.

The induced voltage by single turn transformer can be calculated as follow:

$$V_{inj} = 4.44\,\hat{B}ANf \qquad (5.21)$$

where V_{inj} is the injected voltage and $\hat{B}$ is the flux density in the core. Also A is representing the net cross-sectional area of the core and N is the number of turns of the winding around the core. In this equation, f is the frequency of the injected voltage and it is same frequency of the line current which is equal to 50 Hz. To induce 6V, V_{Inj}=6 V (fundamental), in the primary side with substituting B= 1.2 T, f=50 Hz and N=1 in equation (5.21) the cross sectional area for the STT, A, can be calculated as

$$A = \frac{6}{4.44 * 1.2 * 50} = 0.0225\ m^2$$

In order to meet the cross sectional area of A=0.0225 m2 one of the possible options is using value of r= 0.075 m and l= 0.3 m as represented in the Fig.5.11 and can be calculated by equation (5.22).

$$A = r * l \quad (5.22)$$

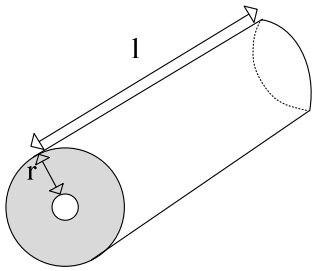


Fig.5.11: Core of STT

However, the thickness, r, and length, l, of the core can be different values but at the end the required cross sectional area must be provided. In the same time volume of cylinder should bare minimum in order to minimize its weight. Having considered this in the final design, r is chosen to be 0.06 m and l is decided to be 0.3 m. With having these values the related cross sectional area is calculated to 0.018 m^2. So in order to induce 6 V in the primary side with the calculated A= 0.018 m2 the required flux density can be calculated using equation (5.21) as follow:

$$\widehat{B} = \frac{6}{4.44 * 0.018 * 1 * 50} = 1.5 \text{ T}$$

The calculated flux density, 1.5 T, is in the margin of magnetic saturation of the employed magnetic lamination in the core. Moreover, B=1.5 T, will be required when the injected voltage is expected to be 6 V however in the experimental studies using the implemented test rig the injected voltage will not reach to 6 V. Then the saturation of the core is guaranteed because of lower than 6 V injected voltages.

The magnetic field strength in the core, H, depends on the magnetic permeability of the material which the core is made of and the flux density in the core. The relationship between the field strength and flux density can be written as follow:

$$H = \frac{\widehat{B}}{\mu} \quad (5.23)$$

where H is the magnetic field strength, B is the flux density and μ is the magnetic permeability.

On the other hand, magnetic field strength in the different distances from the centre of the core is different and it decreases by increasing the distance. However, H also has a relationship with the magnitude of electrical current flowing through the wire in centre of the core as well. In this case by increasing the current the H is increasing as well. H can be formulated as

$$H = \frac{NI_l}{l} \quad (5.24)$$

where I_l is the magnitude of current flowing through the power line and N is the number of turns in the primary winding. In this equation, l is representing the length of distance that magnetic flux needs in order to close the loop. For example at the distance of 0.04 m from the core centre the length is equal to 2*π*0.04= 0.25 m. For the selected core material μ is approximately equal to 0.015 and for the designed core B=1.5 T and with substituting these values in the equation (5.23) H can be calculated as follow:

$$H = \frac{1.5}{0.015} = 100$$

With substituting H=100, l=0.25 and N=1 in the equation (5.24) the required current for generating flux density of 1.5 T in the distance of 0.4 from the centre of the core can be calculated as follow:

$$I = \frac{H * l}{N} = \frac{100 * 0.25}{1} = 25\ A$$

It can be concluded that the designed core for injecting 6 V in the primary side needs 25 A current passing through the centre of the core. However practically through the experimental studies the injected voltage is not exceed 2 V. Because, first of all from the health and safety regulations of the UG lab the secondary side voltage must not exceed 50 V and with considering high turn ratio of the STT, 1: 25, the primary side voltage can be restricted to 2 V or less. Secondly, because of low rated facilities of the UG lab such as supply transformer and even reactance and load practically it is not possible to exceed 15 A current in the power system in the test rig. Then, although the designed single turn transformer has capability to inject 6 V in the primary side through the power line but practically because of the aforementioned restrictions the injected voltage is not reached to the nominal value.

The designed STT consists of secondary winding. However this winding is not a fixed winding and can be easily replaced by another winding with different turns in order to provide injected voltages with different voltage magnitude. For example, through the experimental tests the turn ratios of 1:25, 1: 50 and 1:75 have been used in different test scenarios. All the windings are wounded around the designed core which has 30 cm length. By dividing the length of cylinder (30cm) with the thickness of each laminate (5mm) the required numbers of laminates obtains 600. The core is built up by stacking 600 laminations of M33035A with thickness of 0.5mm together in order to provide the required length of 30 cm. The laminations are bolted to each other in three different points. The location of bolts in the cross section of core is shown in Fig.5.12.

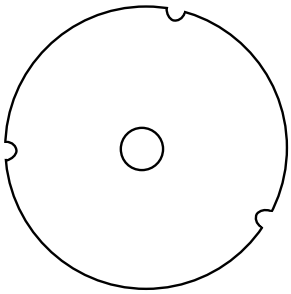


Fig.5.12: The location of bolts in the cross section of core

The holes in three different locations are made far from the centre of the core with intention of saving the material close the centre. The density of flux close to the centre is higher than that in the outer layer of the core. Therefore losing the material in the centre can lead to early saturation of core. The laminations are made of non-oriented silicon steel which has same magnetic property in all direction. This reduces the flux density in the core but it must be noted there is no air gap in the design and this will help to avoid the magnetic saturation of the core.

In the oriented silicon steel the magnetic properties are in one direction and if it matches with the direction of flux then the flux density can increase. However if this kind of lamination is used then the air gap and having two part core is recommended. Otherwise, as the permeability of the core is much higher than the air then the flux will concentrate through the core rather than the air path. Both the air and magnetic paths are in parallel and of course the flux will pass through the way that has low magnetic resistance. But if there is an air gap between the two parts of the core then the reluctance of air gap will be in series with the reluctance of the core and consequently the resultant reluctance will be higher than reluctance of pure magnetic path of one part core.

5.6 Design steps of single turn transformer to be employed in an 11kV distribution feeder

Line parameters of a typical overhead line (employed in an 11kV distribution network) are tabulated in Table 5.1[77]. Design of STT can be customised for specific requirements. For example in this design, DSSC is assumed to compensate 10% of line reactance. In order to provide such compensation, DSSC should insert a reactance of 0.0312Ω/mile in series with the line. This compensation can be achieved by injecting a voltage of 10.8V/mile. This voltage can be calculated by multiplying the reactance by

the maximum allowed current through the line. Multiplying the injected voltage by the maximum line current of 345A, the transformer rated is obtained as 3.7kVA.

Here it is assumed that a single-turn transformer (STT) is installed at each mile of the distribution line. In order to insert a reactance of 0.0312 Ω per mile.

Type	Cross section	Current capacity	R	L
FeAl234	234mm^2	345A	0.143 Ω/mile	0.996 mH/mile

Table 5.1: Typical line parameters in an 11kV distribution system

The single turn transformer should provide the equivalent inductance calculated from equation (5.25).

$$L = \frac{X_{inj}}{2\pi f} \quad (5.25)$$

where X_{ing} is the inserted reactance, L is the required inductance and f is the power frequency. By substituting X_{inj} with 0.00996 Ω in (5.25) the inductance becomes 99.3μH.

Flux within the STT is calculated in equation (5.26)

$$\phi = Li_L \quad (5.26)$$

where L represents the target inductance of STT and i_L is the line current. By substituting L with the calculated value of 99.3μH and i_L with line current of 345A the generated flux will be about 0.034 Webber.

Grain-oriented silicon steel with flux density of up to 1.7 T and relative permeability of 23335 is used in the calculations and design process of the STT [81], [98]. The transformer is designed such that the core will not be saturated by the flux generated by the maximum line current. Hence, the upper range of flux density is considered to be 1.6 T. The relationship between flux and flux density is written in equation (5.27).

$$\phi = BA \quad (5.27)$$

where ϕ is the flux, B is the flux density and A is the core cross sectional area of the STT . Using the flux density of 1.6 T (to avoid from saturation) and the calculate flux of ϕ= 0.034Wb, the core cross sectional area is obtained as 0.0215 m^2.For a rectangular cross section (as shown in Fig.5.13), the area is calculated as $A = d \times l$, where d and l are core thickness and length, respectively.

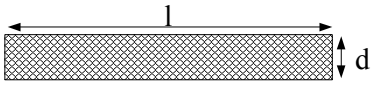


Fig.5.13: Rectangular cross section

Assuming a length of *l*= 1.15 m, a thickness *d* of 0.0186m is obtained.

The inner diameter of the core should be bigger than the outer diameter of the line conductor. Hence, the radius r_1 in Fig.5.14 should be selected to be larger than the conductor radius.

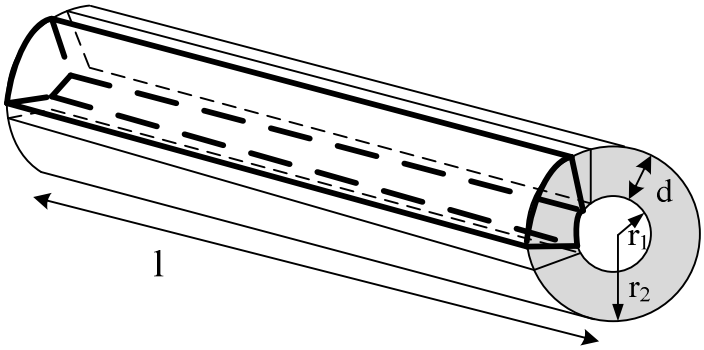


Fig.5.14: Designed STT for an 11kV distribution system

Considering the data in Table 5.1 the inner radius is selected to be 0.87cm to allow the power line pass through. With a thickness of 1.86cm calculated above, the outer radius r_2 will be 2.73cm.

For installation considerations, the core is designed to be comprised of two separate semi-cylindrical sections, which are clamped together and close the magnetic path. There are two air gaps between the two sections as shown in Fig.5.15 which increase the magnetic reluctance of the core.

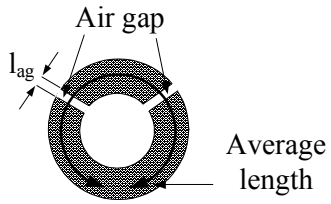


Fig.5.15: Air gap

The air gap reluctance can be calculated using the equation (5.28).

$$\mathcal{R}_{ag} = \frac{l_{ag}}{\mu_0 A_{ag}} \qquad (5.28)$$

where $\mathcal{R}_{ag}$ is the reluctance, μ_0 is the permeabilityof air ($4\pi\times10^{-7}$ H/m). A_{ag} and l_{ag} represent the cross sectional area and length of the air gap, respectively. The total air gap length l_{ag} is assumed to be about 0.1mm. Substituting for those values, the total air gap reluctance will be $3701.3H^{-1}$

Reluctance of the core can be calculated in the same way. However, but l_{ag} must be replaced with l_{eff} (effective length) and μ_0 should multiplied with relative permeability of the core which is 23335 [81].The effective length, l_{eff}, includes the average distance within the core that flux flows through minus the air gap length and its calculated value is 0.1126m. By substituting the related values in (31.4) reluctance of magnetic path of the core, $\mathcal{R}_{core}$, become 0.1787.

The total reluctance $\mathcal{R}_{total}$ is the summation of reluctance of the core and air gap and it is equal to 3701.4787. Inductance can be calculated from equation (5.29) as follow

$$L = \frac{N^2}{\mathcal{R}} \tag{5.29}$$

where N is the number of turns and in here it is 1. Then L becomes inverse of reluctance and the total inductance of the core including the air gaps becomes equal to 2.7μH. This means that adding air gap reduces the core inductance. Hence, in order to achieve the previously calculated inductance of 99.3μH (total target inductance) the cross section of the core must be increased. (Because of early saturation possibility of core material their flux density is considered in the calculations. This consideration provides the cross section of the core and the cross section shapes air gap. It means that core material has the priority in calculations of the cross section. Having provided the cross section of the core, reluctance of air gap can be calculated.)

The new cross section of the core can be calculated using equation (5.30).

$$A_{new} = \frac{L(without\ air\ gap)}{L(with\ air\ gap)} \times A(without\ air\ gap) \tag{5.30}$$

By replacing the respective values in (5.30), A_{new} is obtained as $0.079m^2$. Therefore, the new transformer core thickness will be

$$d = \frac{0.079}{1.15} = 6.86cm$$

New outer radius is obtained 7.73cm by adding the thickness of the core to the inner radius. Summary of the design is tabulated in Table 5.2.

Inductance (L)	Inner radius (r_1)	Outer radius (r_2)	Thickness (d)	Length (l)
2.7 µH	0.87 cm	7.73cm	6.86 cm	115 cm

Table 5.2: Summary of transformer design

5.7 Microcontroller

In order to execute the control strategy, a microcontroller is needed to be employed in the test rig. The microcontroller is a digital signal controller which uses the incoming signals and produces the outgoing signals by executing the control algorithm. To do so, some major units such as, CPU, I/O, Direct Memory Access (DMA) and Analogue to Digital Converter (ADC) are required. Some of these units such as ADC can be provided externally but obviously some others like CPU must be included within the microcontroller.

There are large numbers of different microcontrollers available in the market that they can be employed in the design. However, with intention of reducing the complexity and easing off the design, it is decided to use a microcontroller that can provide all of the aforementioned units. For example, dsPIC33FJ family is one of the possible options which meet the requirements and the feature of dsPIC33FJMC710 from this family matches with the requirements of the design.

For example, it comes with built in ADC then the output signals of the measurement boards can be fed directly into the controller. It includes 8 channel fitted hardware DMA which permits exchanging data between RAM and ports without interrupting the CPU. Otherwise CPU itself must be involved in the managing the data transfer which requires interruption and takes some clock cycles to do so. Also it has its own internal oscillator and there is no need to provide externally. The oscillator is much needed to generate the clocks (time steps) in the system management which can include interrupt controller unit, timer, PWM generator, I/O etc.

One of the most useful features of the employed dsPIC is its built in PWM generator. Obviously in order to trigger the IGBT's we need a PWM generator to produce the required pulses from the reference signal. Having this capability, there is no need to write a code and add complexity to the algorithm.

Considering all the above mentioned requirements a dsPIC33FJ256MC710 is selected to be used in the test rig with an embedded board. This board includes two different communication ports connecting the board to the PC. One of them is ICD 2 port and the other one is a USB port. The board can communicate with a PC using the ICD 2 port

only when it is connected via a MPLAB ICD2 device. This device, as explained in the appendix C, uses RS-232 or even USB protocol to connect the board to a PC. In the designed test rig the RS-232 communication protocol has been employed.

As already mentioned, the embedded board includes a USB port as well which can be used to communicate with PC via the USB port. In this case there is no need to use the MPLB ICD 2. However, it needs a specific application to be installed in the PC and be coordinated with MPLAB. The application adds the complexity of the transferring data and uploading the code. This port is not used for the communication.

In order to introduce the source code being used to execute the proposed control strategy some of the most important configurations within the dsPIC are briefly explained in the appendix C or [99]. These configurations include the followings:

- Direct Memory Access (DMA) [100]
- PWM Generator
- Analogue to Digital Converter (A/D) [101]
- I/O Ports

5.8 LC Filter

Output of the converter is just a chain pulse of the DC capacitor voltage. However the injected voltage must be a sinusoidal waveform. Then a low pass filter is needed to be employed in order to eliminate high order harmonics and provide the required sinusoidal waveform at the secondary side of the single turn transformer (STT).

5.8.1 Different types of low pass filters

Different types of filters can be employed in grid connected power converters to eliminate the harmonics (basically harmonics in the range of switching frequency). Configuration of filters and their performance are key factors which have been considered in the filter design. In the same time cost and weight of components are also other requirements which must be respected in the filter design [102].

Different types of filters which can be used in the grid connected converters mainly include L filter, LC filter and LCL filter. These configurations are shown in Fig.5.16 and they come with different advantages and disadvantages.

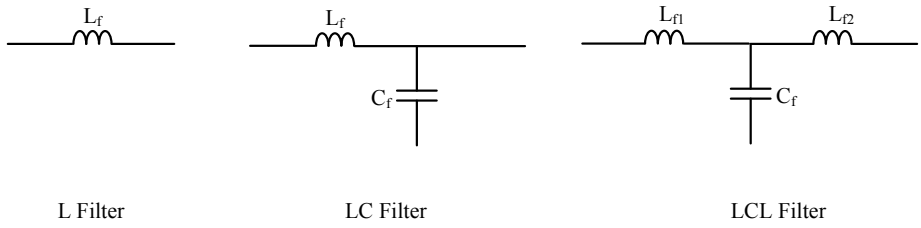


Fig.5.16: Different types (configurations) of filters

For example, L filter comes with very simple topology as it comprise of only an inductor which is located between the converter and transformer in the grid connected converters. However, it requires big inductor in order to eliminate the harmonics and mitigate the current ripple in the same. This can increase the size, weight and cost of the design [103], [104]. Especially the increasing weight of filter in DSSC devices can be more problematic as these devices are supposed to be suspended from the line. Another disadvantage of application of the L filter is the voltage drop across the inductor. With the intention of eliminating the higher frequencies, normally higher inductance required and this can insert big impedance in series. Additionally, such a design can attenuate the fundamental frequencies as well which is not desired.

In order to overcome the aforementioned problem LC filter can be employed. Cut off frequency for this filter is calculated in equation (5.31).

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{5.31}$$

where f_c is cut off frequency of the filter and L_f, C_f represents the inductance and capacitance of the employed inductor and capacitor. Refer to equation (5.31) with higher capacitance implemented in the filter, required inductance will be reduced. Reduction of the inductance means lessening of the fundamental frequency voltage drop across the inductor. However, higher capacitance brings another issue by reducing through the capacitor. Practically this can lead to a high inrush current and it must be avoided and the capacitance should be moderated [105].

Another filter topology which is used in the literature is the LCL filter. However, with LCL filter still the aforementioned disadvantage exists but in spite of this, LCL filter has some other advantages. For example, current ripples are mitigated by L_{f1} and C_f, and L_{f2} is just smooth out the remaining ripples and provide decoupling impedance between the AC power system and converter [105].

Decoupling impedance becomes more important when the impedance of the AC system affects the performance of the converter and filter [106]. However, in the case of the

DSSC, the device is connected in series with the line via a single turn transformer with high impedance in the converter side. The change of the impedance of the line can only affect the amplitude of the current flowing in the converter side of the STT. This can only affect the amount of compensation provided by DSSC and the effect can be easily equalized by making available and settable set points for the controller. Then this advantage of LCL filter is not attract attention in the low pass filter deign for DSSC device. However, LCL filter is a third order system which can unnecessarily add complexity to the system and affects the performance of converter within the DSSC device [107], [106], [103].

5.8.2 Performances of the filters

Transfer functions of the filters presented in Fig.5.17 are stated in equation (5.32) [104].

$$tf_L = \frac{1}{sL_f} \tag{5.32}$$

$$tf_{LC} = \frac{1}{L_f c_f s^2 + 1}$$

$$tf_{LCL} = \frac{1}{s^3 L_{f1} L_{f2} c_f + (L_{f1} + L_{f2})s}$$

where tf_L, tf_{LC} and tf_{LCL} represent transfer function for L, LC and LCL filter respectively. In (5.32) L_f, L_{f1}, L_{f2} and C_f are representing the employed inductance and capacitance in the filters as shown in Fig.5.17. Bode diagrams of three different types of filters have been plotted in Fig.5.17 using equation (5.32) and typical parameters. In this figure bode diagram of L, LC and LCL filter is shown in green, blue and red respectively.

Performances of all three types of filters in terms of magnitude are quite similar in the frequencies below the cut off frequency. However in frequencies above the cut off frequency LCL provide more attenuation than LC and L filter. This is an advantage for the LCL filter in comparison with the other two filters. However, in terms of phase angle, LCL filters come with -90° for frequencies below the cut off frequency and -270° for frequencies above the cut off frequency. Phase delay for fundamental frequency (included in the low frequencies) is not desirable and will weaken the dynamics of system.

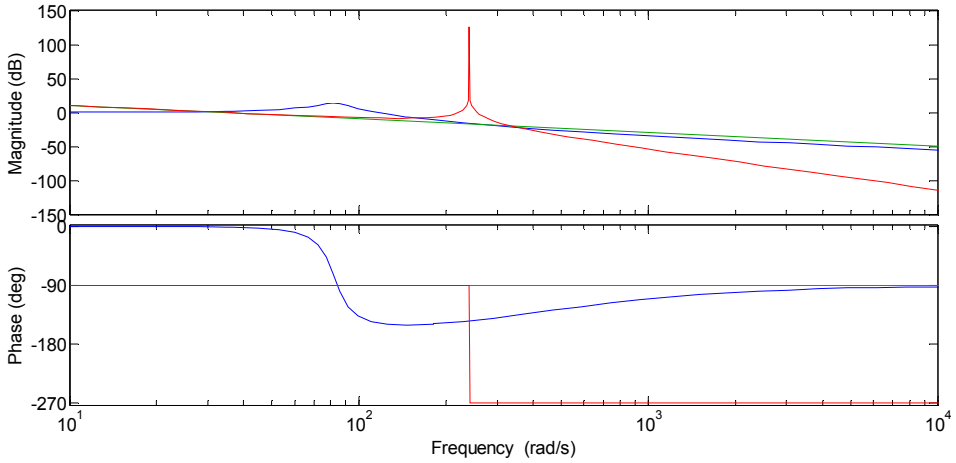


Fig.5.17: Bode diagrams of three different types of filters

It can be observed that in Fig.5.17 phase delay generated by LC filter for harmonics below the cut off frequency is smaller in comparison with the other two filters. In the same time, in terms of attenuation for higher frequencies LC filter provides middle range attenuations (higher than L filter lower than LCL). LC filter has been chosen to be employed in the DSSC device because it can provide required attenuation for higher frequencies without having the aforementioned disadvantages of the L and LCL filter. More importantly, its moderate simplicity reduces the complexity and cost of the DSSC device.

5.9 Design of LC filter

Low pass LC filter provides great attenuation for high frequency waveforms and passes through the low frequency waveforms. Power topology of employed LC filter within the DSSC device is presented in Fig.5.18.

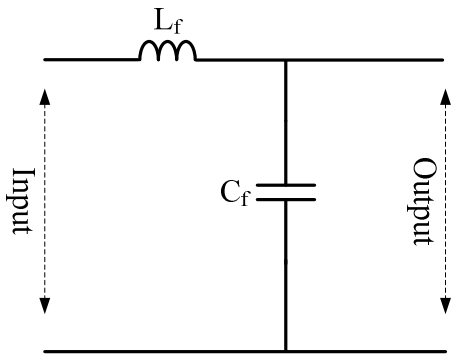


Fig.5.18: Designed and employed low pass filter

Transfer function of the filter is provided in equation (5.33).

$$tf_f = \frac{1}{l_f c_f s^2 + 1} \tag{5.33}$$

Operating switching frequency of voltage source converter within the DSSC device is 15kHz and the output voltage is expected to be polluted with high order harmonics. In order to eliminate the harmonics a low pass filter with cut off frequency of lower than switching frequency is needed. Considering the switching frequency and first dominant harmonics, a cut off frequency of 12kHz has been considered and it can be calculated using equation (5.34).

$$f_c = \frac{1}{\sqrt{l_f c_f}} \tag{5.34}$$

where f_c is the cut off frequency of the employed low pass LC filter and l_f and c_f are the inductance and capacitance of the filter.

Small value of inductor is more desirable as it will reduce the losses and voltage drop across the inductor. In addition small inductor comes with small size and less weight which in turn makes application of DSSC more feasible in the distribution networks. In order to achieve smaller value of inductance higher capacitance is required. With assuming capacitance of 500e-6F and considering required cut off frequency of 12kHz, calculated inductance using equation (5.34) will be 80e-6H. Design value of the LC filter is summarised in Table 5.3.

Parameter	Value
c_f	12KHz
l_f	80µH
c_f	500µF

Table 5.3: Summery of design value

With substituting the design parameters in equation (5.33) transfer function of the designed filter to be employed in the DSSC device is stated in equation (5.35).

$$tf = \frac{1}{6.9e^{-9}s^2+1} \quad (5.35)$$

The filter is expected to attenuate harmonics above the 12kHz and in order to observe the expected attenuation, bode diagram of the filter using (24.3) is plotted in Fig.5.19. In this figure it can be clearly seen that the filter has no attenuation on the fundamental frequency. In addition phase delay for low frequencies (frequencies below the cut off frequency) is very small and in the fundamental frequency is negligible.

Bode diagram shows phase margin of 141° which is inside the safety margin. The designed phase margin is an assurance for stability of the filter.

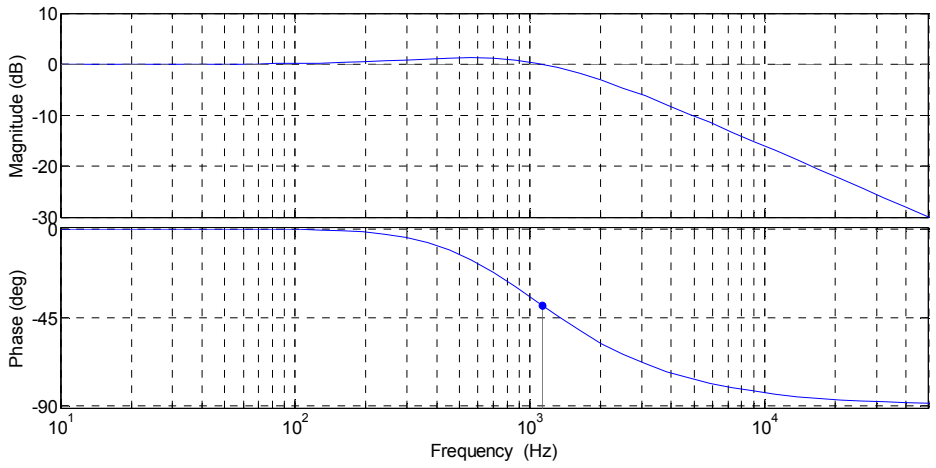


Fig.5.19: Bode diagram of the designed low pass LC filter

5.9.1 Implemented RC filter

In the implemented prototype, DSSC module in the lab employed low pass filter (as shown in Fig.5.20), which comprises inductor and capacitor.

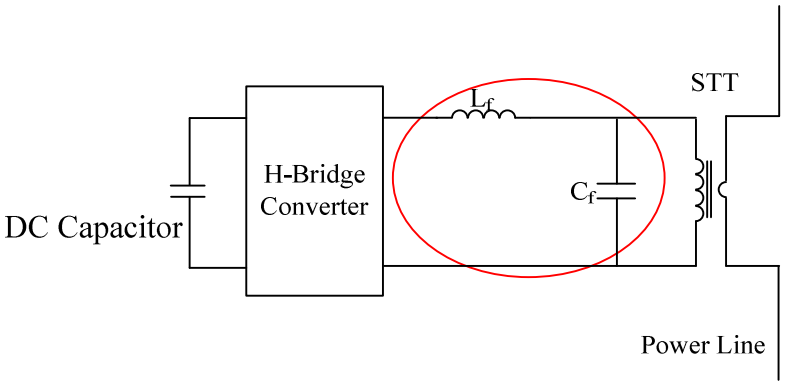


Fig.5.20: H-Bridge converter, RLC Filter and STT

It must be bear in mind that the output voltage of the converter is the input voltage of the filter and the output voltage of the filter is the secondary voltage of the single turn transformer.

In the implemented control system the switching algorithm is using carrier-based pulse width modulation (PWM) pulse generator to generate the final desired switching pattern. The employed PWM technique is well explained in [108]. The output voltage of the inverter includes high level of the harmonics. To smooth out the filtered signal and eliminate most of the harmonics the cut off frequency must be smaller than the switching frequency. With switching frequency of 1kH, cut off frequency must be between 50Hz (fundamental) and 1kH. The cut off frequency can be calculated using equation (5.34) and its value must be chosen from frequencies near to the first dominant harmonic from the harmonic spectrum of output voltage of the converter. In this case study the first dominant frequency is 900Hz.

In addition, filtering down to the fundamental frequency (which is 50 Hz in this study) normally requires big inductor and capacitor that can make the hardware implementation difficult and costly. For these reasons and considering available inductance in UG lab to be employed in the test rig implementation, cut off frequency of 112 Hz found to be achievable. Substituting cut off frequency (f_C) of 112 Hz into equation (5.34) and L_f of 20mH capacitance of C_f is obtained 100uF.

5.10 Validation of proposed controller

With validation purpose for the simulation results the proposed control method was examined using the scaled down prototype DSSC module. The test rig includes a power system, which comprises two parallel feeders supplying a load. The power system is a single phase system and the line to ground rms voltage of the AC source at sending end bus is 50V. This voltage level is defined based on the health and safety regulations of the UG lab at the Newcastle University. The parallel lines include a 20mH inductance and a 1Ω resistor to model a 20km, 11kV distribution feeder. The DSSC device connected in series with the line1 via a single turn transformer with turn ratio of 1:100.

The H-bridge converter is built using a 4-pack IGBT, SK20GH123, which is providing four IGBT along with four anti parallel diodes in one pack. The proposed control method is implemented using C code in dsPIC33FJ256MC710. The injected voltage, along with the line current, DC link voltage and DC link current, are shown in Fig.5.21.

In this figure the injected voltage comes in blue and the line current is in green. The yellow and the pink lines represent the current through the DC link and the DC voltage respectively. The leading voltage in Fig.5.21 is representing a capacitive injection. In this figure line current and injected voltage comes in blue and green respectively. DC link current is shown in yellow.

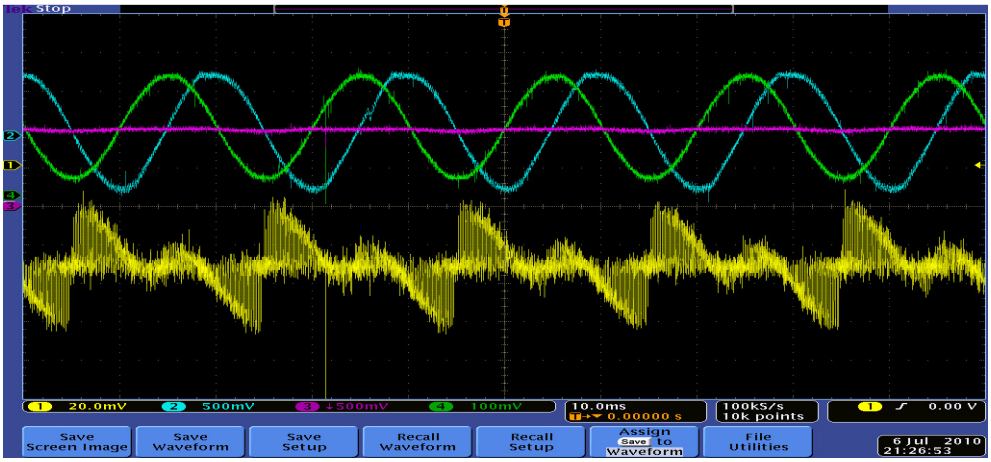


Fig.5.21: Capacitive voltage injection (snapshot of the screen of oscilloscope)

In the experimental tests the result data has been extracted from oscilloscope and plotted using Excel. Capacitive injection of the DSSC is represented in Fig.5.22. The figure

shows the capability of the proposed controller in capacitive injection through the power line.

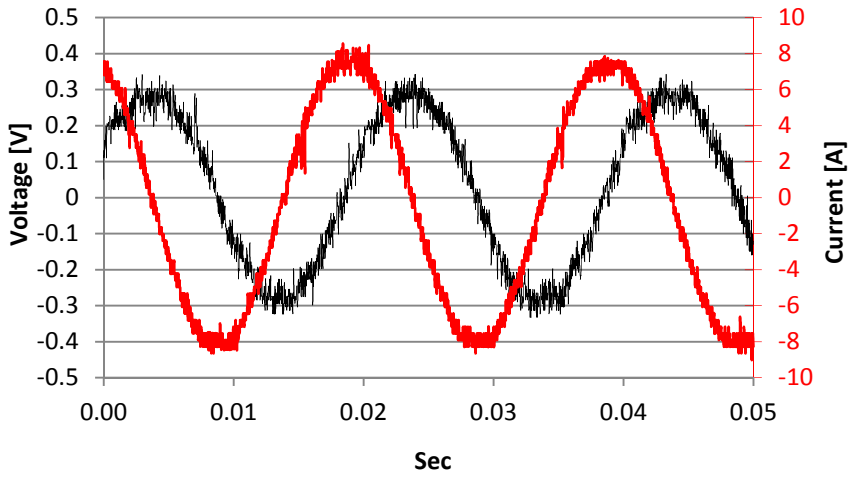


Fig.5.22: Capacitive injection

Inductive injection capability of the system has been examined and the result is shown in Fig.5.23.The figure shows the capability of the proposed controller in inductive injection through the power line.

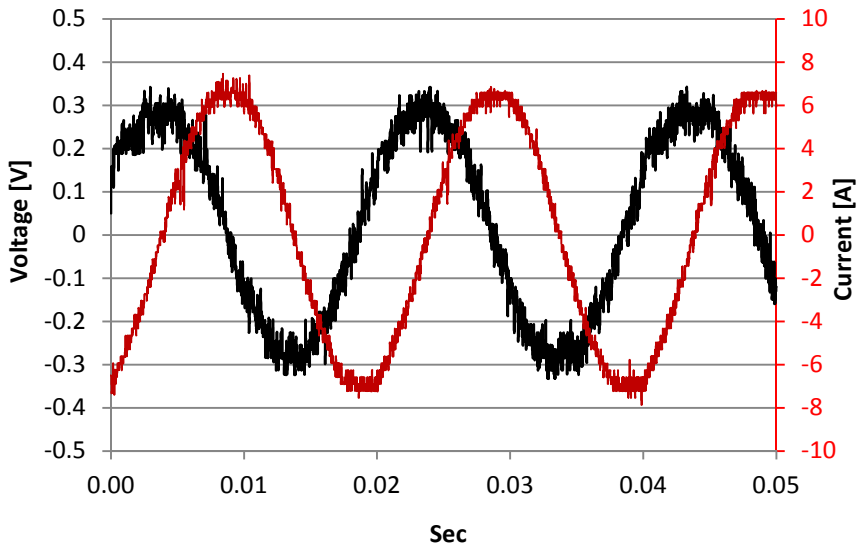


Fig.5.23: Inductive injection

The phase difference between injected capacitive voltage and line current based on the extracted data when the injection is capacitive becomes -87.98 degree. The angle is almost identical to the angle which is achieved by PSCAD simulation and is presented

in chapter 4. Along with the phase angle of -87.98 degree the whole losses for DSSC module, which is measured using YOKOGAWA power analyzer, is 1.99W. While using the conventional control method the angle is -85.23 degree and the losses become 4.65W for comparison.

The injection with proper angle can reduce the ripple amplitudes because of less absorption of active power. Using the proposed control method the peak amplitude of ripples in DC link, as shown in Fig.5.24, become 32.5 volts while this voltage with the conventional control system, shown in Fig.5.25, is 34 volts.

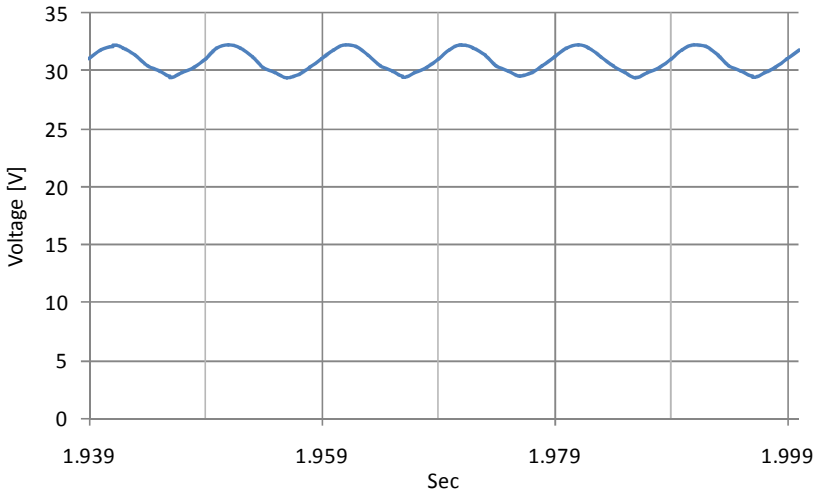


Fig.5.24: DC link ripples with proposed control

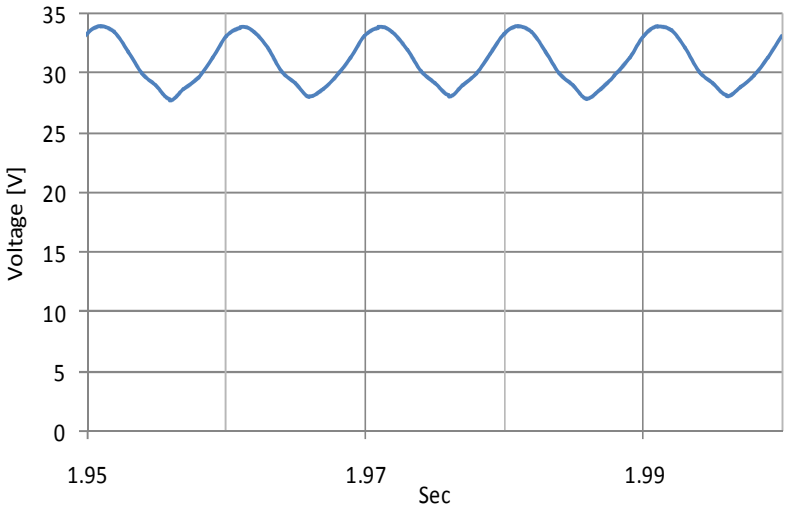


Fig.5.25: DC Link ripples with conventional control

It can be noted that the percentages of the ripples can be calculated using equation (5.36)

$$v_r = \frac{\Delta v}{V_{dc}} \times 100 \qquad (5.36)$$

where v_r is representing the percentage of the ripple and V_{dc} is the peak amplitude of the voltage. In this equation Δv represents variation of voltage from minimum to maximum. Using the conventional controller and replacing the corresponding values in (5.36) percentage of the DC voltage ripples is obtained as 20.5%. However the ripples become 12.3% when proposed controller is employed. The percentage of ripples is reduced from 20.5% to 12.3%, i.e by 8.2 %. This is reduced because in the proposed controller both DC voltage and injected angle are controlled in the same time. This can avoid deviation of injection angle from the target value and consequently the exchanged active power is reduced. As result of reduced exchanged active power percentage of ripples are reduced. Table 5.4 summarizes the above tests and compares the experimental results for both control methods while DSSC compensating of the parallel lines.

Experimental Results for Capacitive Injection	Using Proposed Method	Using Conventional Method
Losses [W]	1.99	4.65
Phase angle [Degree]	-88.65	-85.98
DC Link Voltage Ripples [%]	12.3	20.5

Table 5.4: experimental results for both control methods

Effect of compensation of only one line in a bus with two parallel lines has been investigated. Assuming that line1 is being compensated by DSSC and line2 is remain uncompensated. Obviously, sending end bus current via two parallel lines is equal to sum of the currents in the line1 and line2 before and after the compensation of line1. The line current in line1, as a result of compensation, has been increased and in the same time current in the line2 has been decreased. This can be identified in Fig.5.26 which is showing the practical results of the compensation of line1.

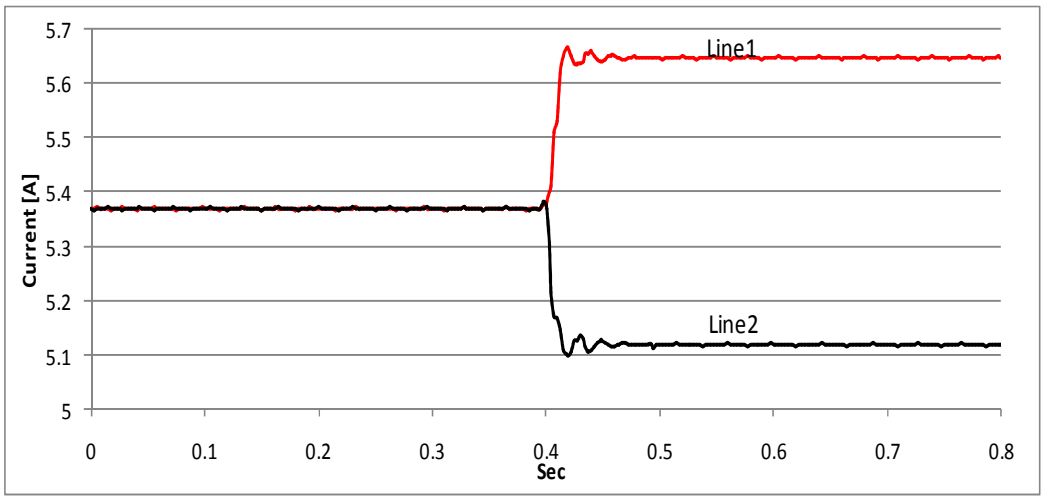


Fig.5.26: Practical rms value of line current

5.11 Summary

In this chapter, the hardware implementation of the prototype DSSC device has been explained. The device was designed and built in the UG lab at Newcastle Upon Tyne University. The operating voltage of power system inside the test rig is 50 volts and the maximum expected current is below 15 A. The design and build of test rig includes all electronic board, single turn transformer, programming of the microcontroller and RLC low pass filter.

The electronic boards include two voltage measurement boards (one for AC voltage and one for DC voltage), a current measurement and a gate drive board. The related PCB board is designed using Ultiboard software and was assembled and soldered in the UG lab. One of the most important electronic boards which is designed and implemented in this project is the gate drive board. This is an interface board between the microcontroller and power converter.

The single turn transformer used in the prototype consists of mainly a cylindrical core and a secondary winding. The primary winding in this case is the power line itself which is passing through the cylindrical core. As the current flowing through the power line it induces current in the secondary winding. The current is fed into the LC filter and VSC converter.

The maximum voltage that STT can inject highly depends on the design of its magnetic core. The magnetic permeability of core must be high enough in order to provide appropriate reluctance for the generated magnetic flux by the power line. The core is

chosen to be made of non-oriented silicon steel laminations, which is called M33035A, with maximum flux density of B= 1.5 T.

Full design steps of single turn transformer that can be used for an 11kVdistribution network have been explained. The required inductance of the demanded compensation is calculated based on the rated current of the power line. For the calculated inductance cross section of STT core is obtained. Practically the core comprised of two parts and it comes with air gap and inserts a magnetic resistance in the in the circulating path of the flux. The resultant reluctance was included and the new inductance is obtained considering the requirements. The obtained inductance requires recalculation of the cross section. Having done the recalculation the new cross section the thickness of the core is obtained 6.89cm and the length of the STT becomes 115cm.

Different types of low pass filters and their performance in mitigating harmonics have been studied. In terms of amplitude they provide quite similar attenuation in the frequencies below the cut off frequency. However in frequencies above the cut off frequency LCL provide more than the other two. As regard as phase angle concerns, LCL filters generate -90° phase delay for frequencies below the cut off frequency and -270° for frequencies above the cut off frequency.

Phase delay generated by LC filter for lower frequencies is smaller in comparison with the other two filters and for higher frequencies LC presents middle range attenuations. Based on this study and in order to avoid complexity of LCL filter, LC has been employed in the DSSC device. Design process of LC low pass filter is explained and proper inductance and reactance have been selected.

Microcontroller, dsPIC33FJ256MC710, was selected for being employed in the implementation of the prototype. The microcontroller has its own A/D, DMA and PWM generator which decreases the complexity of hardware implementation.

Ultimately, all of the equipment and devices are located inside an aluminium cage, as presented in this chapter, with a wooden floor and net metal lid. This cage includes the power system as well and the operator has not have access to inside the cage during the test (operation). This is because the lid of the cage is equipped with a protection switch. As soon as the lid is opened the power system will cut off immediately. In addition the test rig comes with an emergency STOP switch which can cut off the power in all equipment immediately in an emergency case.

The proposed controller was examined using the designed test rig. The experimental results show that the controller is capable of injecting both capacitive and inductive

voltages and alter the reactance of the line. In a power system, including two parallel lines, as result of the capacitive injection, current increases in the compensated line and decreases in the other one. In the same system by injecting inductive reactance in the compensated line, current is pushed away from the line and pulled into the uncompensated parallel line.

Experimental results using the conventional and the proposed controller have also been compared. It has been noted that the loss is reduced using proposed controller in comparison with the 90° phase controller. In this study it has been demonstrated that diversion of injection angle from the target value is improved. In addition, the percentage of ripples in the DC voltage has been reduced from 20% to 12.5% when the proposed controller has been used instead of 90° phase shift based controller.

6 Conclusions and Future Work

Investigations in relation to distributed static series compensator (DSSC) are concluded in this chapter. The conclusions includes an overview of all types of series compensator solutions and discusses feasibility of application of DSSC devices in the existing distribution feeders investigating mechanical withstand capability of the feeders. This is followed by reviewing the advantages and disadvantages of existing control algorithms and developing a new control strategy to overcome some of the drawbacks.
Conclusion of achieved simulation and experimental results proposing the utilization of proposed control system are then discussed. Finally, the contributions and published papers are listed and future work is discussed.

6.1 Conclusion

Fixed capacitors in series through the power lines is one of the series compensation solutions can be employed electrical networks. However it comes with some disadvantages which encourages looking for alternative solutions. Power electronic based series compensators are introduced to overcome to the disadvantages. SSSC and DSSC are power electronic based series compensators which are using VSC to inject a series voltage through the line.
DSSC is a single phase device and it is more reliable as it uses a STT to inject voltage through the line and in case of fault in the system just a small current passing through the power electronic devices. As it is just suspended from the line then even failure of device does not disrupt the power in power line. In addition it can be easily assembled and disassembled from the line by clamping the STT. Finally there is no need for customized design and thus these could be mass produced in effect lowering the costs.

The capability of existing distribution overhead lines to withstand the suspension of DSSC devices from the lines has been studied and presented in Appendix D. Between each two poles there was one suspended DSSC device from the power line. The mass of the DSSC device generates an extra mechanical load through the line. The added load increases the line mechanical inertia and helps to stop the low amplitude horizontal oscillations (Galloping) however as soon as the oscillation is started its suppression will be difficult. The vertical vibration (Aeolian) was not dependant on the mass of the line and so remains unaffected by adding the DSSC device.

In most of the cases the total weight of the wire plus weight of the DSSC was in the acceptable margin. However it is recommended that installation of device some part of the feeder with long span such as river crossing to be avoided. The study of the mechanical withstands capability of the feeders show that the application of DSSC in the distribution networks is feasible however this cannot be generalized for all feeders and it is recommended that their capability to be investigated individually before any installation of the DSSC devices.

Two different control strategies, 90° phase shift and dq conversion based controller have been employed in literature review. Practically, the DSSC device needs to compensate its own internal losses and this requires angle of injected voltage to be diverted slightly from 90° with respect to line current. The slightly diversion of phase angle over the time period can be different and it requires an adaptive control to take the changes into account.

In most of the control strategies employed with SSSC, the dq conversion has been applied. However, it has been shown that in presence of unbalanced AC system the accuracy of dq conversion can be affected and the resultant dq components can be inaccurate.

In order to overcome the aforementioned drawbacks a single phase controller which is providing a dynamic injection angle has been developed. The angle was being adjusted to reduce exchange of active power. It has been shown that the controller monitors DC voltage and the injection angle in the same time and regulates both of them.

Performance of proposed controller was compared with conventional controller (only DC voltage controller). In the conventional controller changing the gain affects amplitude of ripples, THD and angle of injection in different ways. For example, increasing the gain improves the angle but deteriorates the amplitude of ripples and THD. However, reducing the gain reduces the amplitude of ripples and THD, but increases the injection angle. The results show that always improving one the factors, using conventional controller, can sacrifices the other one.

Proposed controller enhances ripples, THD and injection angle all in the same time, as it receives continuous feedback from both angle of injection and DC voltage. The simulation result show that proposed controller was reduced amplitude of the ripples, THD and angle more than the conventional controller (only DC voltage controller).

Using the proposed controller the exchanged active power and ripple of DC voltage are reduced. These are mainly achieved because the new controller reduces unnecessary charge and discharge of DC capacitor around the desired voltage level. The simulation results have proven that the controller was capable of injecting both capacitive and inductive reactance through the line.

DSSC devices were employed in an 11kV distribution networks and it was improved electrical parameters such line reactance or voltage profile. It has been demonstrated that with X/R ratio of one (or in the vicinity of 1) capacitive injection can decrease the transmission capability of the power line. More interestingly in these lines (with lower X/R ratio) inductive injection can increase the line capacity.

It has been shown that, the amount of compensation that each DSSC module can deliver was calculated by dividing the injected voltage with line current. DSSC device can be designed to inject voltage with different amplitudes and the number of modules is highly depends on the capability of each module and required compensation to be achieved. The required compensation per mile was a key parameter in the design of each device. The number of devices can be obtained by dividing the required compensation with the compensation that each device can deliver.

It has been demonstrated that using DSSC devices, which were controlled using a new control strategy, power flow can be controlled in parallel power lines. It has been shown that load flow can be diverted partially from either of the lines to the other one by injecting capacitive and inductive reactance. It means that by inserting capacitive reactance the line reactance was reduced and it can transfer more power.

In another application DSSC has been used to improve voltage profile through the line. In this application the injected capacitive reactance by the DSSC compensates the line inductive reactance and the voltage drop. It also injects reactive power to boost up the line voltage and provides part of the consumed reactive power.

A controller using the achieved transfer function and considering specific requirements such as overshoot percentage of step response has been designed. The controller guaranties stability of the system by inserting zeros at the proper location of the zeros poles map.

A sensitivity analysis has been conducted and it shows the designed controller was immune against system parameters changes. The changes include variation in capacitance of DC link, capacitor and inductance of low pass filter. It has been found that stability of system will not be at risk as long as the changes are restricted to 10%.

The impact of adding a low pass filter to the designed controller was also examined.

The performance of the proposed controller employed within a DSSC device has been compared with the traditional controllers when DSSC was being used in an 11kV distribution network. The proposed controller shrinks phase angle of injected voltage in comparison with 90° phase shift method. Also it mitigates the injected harmonics more than 90° phase shift method.

When a dq based controller was used in the control of DSSC dependency of reference signal on to the line current has been observed. This was because reference signal in the dq based controller was calculated based on the dq component of line current. However the proposed controller demonstrates independent performance from the line current as it provides a reference signal for each phase.

When only DC link voltage regulator was being used, the angle of injection was more oscillatory. The proposed controller demonstrates better performance with respect to this controller. Using the proposed controller the injection angle was diverting less from the target.

In another sensitivity analysis performance of the DSSC which employs proposed controller against system parameters change has been examined. Change of parameters includes change in line resistance, voltage, and figuration of the network. The simulation results present satisfactory functioning of controller.

A fault recovery strategy has been developed based on the studying different fault scenarios. This was to identify an approach to be taken in the occurrence of fault in the power system. It has been found that, by blocking only converter (H-bridge converter inside DSSC) voltage across the DC link can exceed its limit. However, when fault occurs and STT becomes open circuit regardless of blocking or not of the converter- a high AC voltage will be generated in either side of the STT. In order to avoid these issues converter was blocked and STT was bypassed. This hold DC voltage in the pre fault value (within the limit) and keep away STT from experiencing a high voltage in its terminals.

A full design step of STT for an 11kV application in distribution network was included. STT was required to provide appropriate inductance in order to meet the demanded compensation. The inductance was calculated from required compensation reactance and the calculated inductance determines the cross section of STT. Practically the STT

core was a combination of two parts which are clamped to each other. The air gaps between two parts insert a magnetic resistance in the flux path and changes the reluctance which was obtained from the calculations. The cross section was calculated based on the inductance which includes reluctance of the air gaps as well. Considering the calculated cross section of the core thickness of 6.89cm and the length 115cm were obtained for STT.

DSSC also requires a low pass filter to mitigate the harmonics. Different topologies of low pass filters (including L, LC and LCL) and their performance in connection with grid connected power converters have been studied. Based on the conducted study the provided attenuation by filters for frequencies below the cut off frequency are quite similar. Conversely in higher frequencies LCL attenuates more than the other two filters. In terms of phase angle, LCL creates -90° delay for lower frequencies and generates -270° phase delay for higher frequencies (Higher frequency means above the cut off frequency and lower frequency means below cut off frequency).

In using LC filter the created phase delay for lower frequencies was smaller when it was compared with phase delays which were generated by other two filters. The attenuation provided by LC filter for higher frequencies was middle range. In this study LC filter presented satisfactory performance and it has been used in the DSSC device. Thereafter a low pass LC filter has been designed for to mitigate the harmonics above the cut off frequency.

A laboratory test rig has been designed and implemented in the lab and it has been used to execute the control algorithm. The implemented device using the proposed controller was capable of injecting both capacitive and inductive voltage through the line. The designed STT was used to inject the voltage and the experimental voltage injection results prove its proper functionality.

In an experimental test with a power system with two parallel lines capacitive and inductive reactance injected in the compensated line in order to investigate the load flow capability of the device. In the capacitive injection current pulled into the line and pushed away from the other line. Additionally, in an inductive injection current was diverted to uncompensated line. These were demonstrating the load flow control capability of the device.

Using the experimental test rig performance of the proposed controller was compared with the traditional controller. In this study proposed controller reduces the losses when

it was compared with the performance of 90° phase controller. Furthermore, the proposed controller reduces diversion of injection angle from 90°. It has been found that ripples in the voltage of DC link reduce to 12.5% when the proposed controller has been employed within the DSSC device while it was 20% when 90° phase shift controller was in use.

6.2 Contributions

The conducted study includes research, design, experimental implementation (experimental results) and feasibility study. The author contributions have been listed in the following bullet points:

- An overview of compensation in electrical networks is obtained.
- An overview of series compensations and the related control strategies have been provided which can be used as a reference document for the research works conducted in this field.
- Novel application of DSSC in distribution system has been introduced. This includes application of DSSC to improve voltage profile in a distribution network and novel application of DSSC in load flow control in distribution network. It has been shown that using DSSC in distribution networks voltage profile can be improved and load flow can be controlled. Improving voltage profile in a novel idea which introduced in this research work.
- It has been found that as X/R ratio decrease ATC of line will decrease too. A novel idea has been developed that with systems with low X/R ratios inductive series injection by DSSC can increase ATC
- A novel single phase controller for control of DSSC based on the instantaneous exchange of complex power has been developed. This is an alternative approach to the fine tuning of conventional controller to improve functionality of DSSC.
- A novel fault recovery strategy has been developed for DSSC device to be taken in occurrence of fault.
- Full design steps of a STT (to be employed in an 11kV distribution system)has been provided.

Three cited conference papers have been published from the research work as listed follow:

- "New Control Method For Distribution Network, Distributed Static Series Compensator" *Oral presentation in: PEMD, Brighton UK, 2010*
- "Distributed Static Series Compensation for Distribution Network Line Voltage Profile Improvement" *Oral presentation in: IEEE PES ISGT (Smart Grid Conference), Manchester, 2011,*
- "Feasibility study of application of DSSC in distribution networks" *Oral presentation in: CIRED Conference, Stockholm, 2013*

6.3 Future work

This study is focused on the DSSC itself and its control algorithm. The algorithm reflects on the control system of the converter inside the DSSC and does not consider the relationship between the all modules throughout the compensated system. The DSSC is a novel idea and needs lots of work to be carried out to become mature technology. For example the following topics came across during the research which was out of the scope of this research but they are important issues and they need to be investigated in the future works

6.3.1 Design consideration

The DSSC is a special device and it is supposed to be suspended from the overhead lines in the electrical networks. It must be designed so that it has capability to withstand in extreme weather conditions. For example in the icy, rainy and windy condition the normal operation of the system needs not to be affected. In addition the functionality of DSSC must not be affected in presence of large corona or electromagnetic waves which are generated around the power lines. Furthermore, in order to industrialize the DSSC the reliability of the solution must be found out carefully. DSSC must be designed in a way so that mounting or dismounting can be done easily in a live system within the minimum time. The recommended research work needs to be conducted in properly equipped laboratories in order to simulate the environmental conditions and provides high voltage and high current facilities.

6.3.2 High level control and managing the modules in the network

The DSSC modules through the network must be controlled by a high level control. Each module has own program and control strategy inside which can deliver the demanded compensation. However the demand itself is an important factor which can be defined by operator or an intelligent program. For example the program can provide

an up to date and online demand plan for the modules based on the dynamic of the power system. For instance it can consider the stability of the whole network and based on that repeatedly updating the demand for compensation. In another example it can contribute toward the peak shaving in the network. This can be achieved by change the reactance of a feeder which is connecting peak area to the network that has available generation capacity.

Customized software is needed to be developed in order to receive online information about the parameters of system from all over the network and analyse the data.

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Appendix A: dq Conversion

A.1 Introduction

dq conversation is a mathematical conversion of a three dimensional system to a two dimensional system. Both systems are synchron and they share a same angular frequency. The two dimension system is so-called dq system and "d" is the direct component and the "q" is the quadrature component of the system. In an ideal system the angle between "d" and "q" is 90°. In appendix A the dq conversion is explained and the related formulas have been represented. In addition the definition of the unbalanced AC system is denoted in this appendix.

A.2 dq conversion

dq conversion has been used widely in the literature reviews of previous research in the field of SSSC. It is mainly used to convert a three-phase system to a two dimensional system, which is rotating synchronously with the three-phase system. This conversion reduces the volume of calculations in the power system studies and also it reduces the complexity of the analysis. The conversion matrix is shown as

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(wt) & \cos(wt-\frac{2\pi}{3}) & \cos(wt+\frac{2\pi}{3}) \\ -\sin(wt) & -\sin(wt-\frac{2\pi}{3}) & -\sin(wt+\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad \text{(A.1)}$$

where w is the angular frequency of the three-phase system, which must be updated using a PLL that is locked to the power system. The equation (A.2) shows the conversion of V_{abc} to the V_{dq} using the matrix shown in equation (A.1):

$$\begin{bmatrix} V_d \\ V_q \\ V_o \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(wt) & \cos(wt-\frac{2\pi}{3}) & \cos(wt+\frac{2\pi}{3}) \\ -\sin(wt) & -\sin(wt-\frac{2\pi}{3}) & -\sin(wt+\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad \text{(A.2)}$$

consequently, the parameters V_d and V_q can be calculated as

$$V_d = \sqrt{\frac{2}{3}}\left(\cos(wt)\,V_a + \cos\left(wt - \frac{2\pi}{3}\right)V_b + \cos\left(wt + \frac{2\pi}{3}\right)V_c\right) \quad (A.3)$$

$$V_q = -\sqrt{\frac{2}{3}}\left(\sin(wt)\,V_a + \sin\left(wt - \frac{2\pi}{3}\right)V_b + \sin\left(wt + \frac{2\pi}{3}\right)V_c\right) \quad (A.4)$$

and

$$V_o = \frac{1}{\sqrt{3}}(V_a + V_b + V_c) \quad (A.5)$$

In the above calculations, the V_q parameter is orthogonal to the V_d parameter and they are so-called the quadrature and direct components of the conversion. The V_0parameter is supposed to be zero in this conversion. However, the non-zero value of the V_0 parameter shows that the three-phase system is not a balanced system. This is because in an ideal case and in a balanced system, the V_a, V_b and V_c parameters are as follows:

$V_a = V_{max}\text{Sin}(wt)$ (A.6)

$V_b = V_{max}\text{Sin}(wt + 120)$ (A.7)

and

$V_c = V_{max}\text{Sin}(wt - 120)$ (A.8)

where if the equivalent values of V_a, V_b and V_c from equations (A.6), (A.7) and (A.8) be substituted in equation (A.5), then equation (A.5) can be rewritten as

$$V_o = \frac{1}{\sqrt{3}}(V_{max}\text{Sin}(wt) + V_{max}\,\text{Sin}(wt + 120) + V_{max}\,\text{Sin}(wt - 120)) \quad (A.9)$$

however, the following equality must be observed where

$$V_{max}\text{Sin}(wt) + V_{max}\,\text{Sin}(wt + 120) + V_{max}\,\text{Sin}(wt - 120) = 0 \quad (A.10)$$

The equation (A.10) can then be argued that in balanced power systems, the dq conversion of V_{abc} will result in V_d and V_q only and that the V_o parameter will be zero. Equation (A.2) can then be rewritten as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(wt) & \cos(wt - \frac{2\pi}{3}) & \cos(wt + \frac{2\pi}{3}) \\ -\sin(wt) & -\sin(wt - \frac{2\pi}{3}) & -\sin(wt + \frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (A.11)$$

Furthermore, in most of the applications after the conversion of V_{abc} to V_{dq}, the calculations and control strategy take place in the dq domain and thereafter, the provided signals must be reconverted to the abc format. To do so, the inverse conversion matrix is needed, which is denoted as

$$T^{-1} = \begin{bmatrix} \cos(wt) & -\sin(wt) \\ \cos(wt - \frac{2\pi}{3}) & -\sin(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) & -\sin(wt + \frac{2\pi}{3}) \end{bmatrix} \quad \text{(A.12)}$$

By applying the equation in (A.12), the V_{abc} parameter can be calculated from V_{dq} as

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \cos(wt) & -\sin(wt) \\ \cos(wt - \frac{2\pi}{3}) & -\sin(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) & -\sin(wt + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad \text{(A.13)}$$

In all of the above calculations, it is assumed that the dq axes are synchronised with the abc axes as shown in Fig.A.1. This means that the d-and a-axes are in the same direction (aligned). However, this is not necessarily needed because there can be a phase difference between them in some specific applications. For example, in SSSC or DSSC applications, the introduced phase angleθ can be ±π/2 in order to create 90 degree phase shift. The shifted dq axes are shown in red in Fig.A.1.

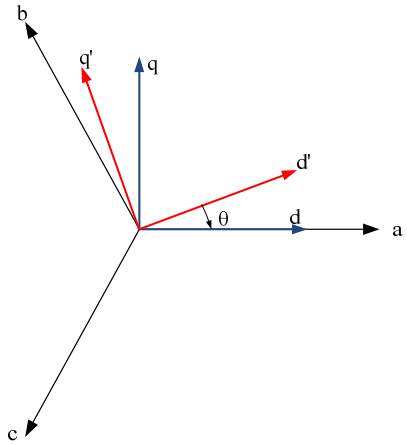


Fig.A 1: abc to dq

Considering the phase angle θ, equations (A.11) and (A.13) can be rewritten as

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(wt \pm \theta) & \cos(wt - \frac{2\pi}{3} \pm \theta) & \cos(wt + \frac{2\pi}{3} \pm \theta) \\ -\sin(wt \pm \theta) & -\sin(wt - \frac{2\pi}{3} \pm \theta) & -\sin(wt + \frac{2\pi}{3} \pm \theta) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad \text{(A.14)}$$

and

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \cos(wt \pm \theta) & -\sin(wt \pm \theta) \\ \cos(wt - \frac{2\pi}{3} \pm \theta) & -\sin(wt - \frac{2\pi}{3} \pm \theta) \\ \cos(wt + \frac{2\pi}{3} \pm \theta) & -\sin(wt + \frac{2\pi}{3} \pm \theta) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad \text{(A.15)}$$

In equations (A.14) and (A.15), the parameter θ represents the initial phase angle, which will be useful when the dq axes needs to either lead or lag the abc axes.

A.3 Unbalanced Three Phase AC System

A typical unbalanced three-phase system is shown in Fig.A.2(a), which can be compared with a three-phase balance system in Fig.A.2(b).

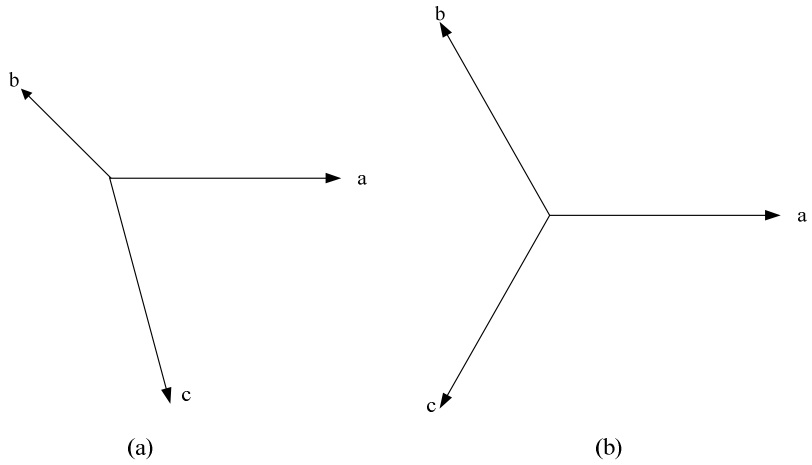


Fig.A 2: a) Unbalance three-phase system b) Balance three-phase system

In Fig.A.2 (a) the phase angles between the phasors in the unbalanced system are not identical and their amplitudes are different. However, in a balanced system as seen in Fig. A.2 (b), the angle is indistinguishable and the amplitudes are the same.

Furthermore, the unbalanced system disturbs the dq conversion and can lead to an incorrect calculation. The unbalance of a three-phase system is defined by the percentage of difference from the average voltage. This can be calculated as

$$\text{Percentage of Unbalance} = \frac{100 * \text{Max } \Delta V}{V_{Ave}} \quad \text{(A.16)}$$

where Max ΔV is the maximum difference from the average voltage and V_{Ave} is the average voltage.

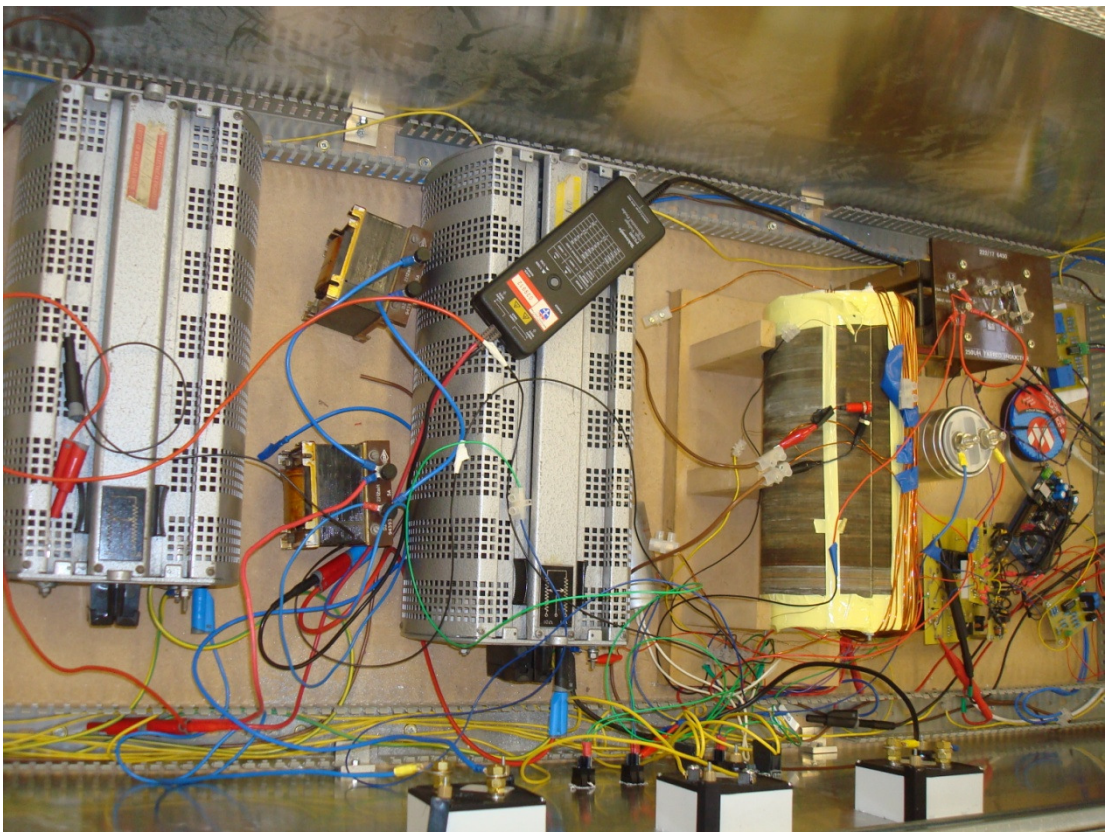
Appendix B: Technical Characteristics of Components

B.1 Introduction

Technical characteristics of components and test rig are represented in appendix B. It includes the components and electronics boards which are employed in the implementation of the electronic and power electronics boards. The design process is explained in chapter 4 then appendix B includes only the technical specifications and in some cases the input and output layouts of the components and the related photo.

The test rig includes 220:50 transformer, DSSC device and all of the electronic boards which are located inside an aluminium cage, as shown in Fig.B.1 a and b, with a wooden base and net cover.

a) Aluminium cage of test rig



b) Inside test rig

Fig.0.1: Designed and implemented test rig

B.2 H-Bridge Converter

In the design of power electronics converter SK20GH123has been selected which is a H-bridge compact module has been used. It can be easily secured to a top-mounting copper heatsink with just one screw. It has well matched IGBT's and diodes inside in terms of rated voltage and current. Its I_C-V_{CE} curve for different V_{GE} voltages is shown in Fig. B.2. Based on the design the rated maximum voltage between collector and emitter, V_{CE}, in the off mode is 1.2 kV and the rated collector current, I_C, is 23A at the ambient temperature of 25°C. This current rating could go down to 15A at the temperature of 80°C. The rated current for the freewheeling diode is 24A and 17A at temperatures of 25°C and 80°C respectively [91].

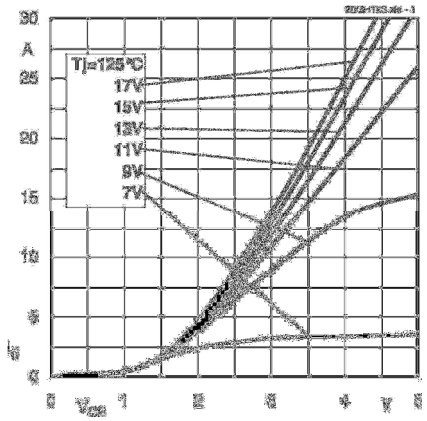


Fig. B. 2: IC versus VCE curve

The SK20GH123 device, as shown in Fig.B.3, comes with 16 pins. These pins provide access to different points of the H-bridge converter and IGBTs. Moreover, the corresponding points of connection inside the SK20GH123 for pin numbers 1,2, 5, 7, 8, 9, 13 are shown in Fig. B.4 but the rest of pins including 3, 4, 6, 10, 11, 12, 14, 15 are left unconnected, i.e. they are not applicable.

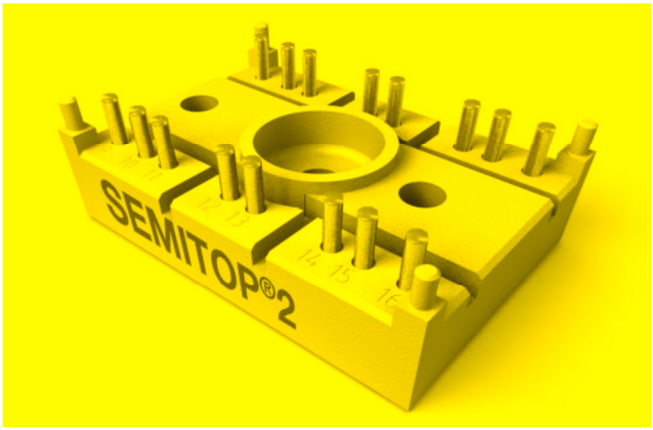


Fig.B.3: SK20GH123 device

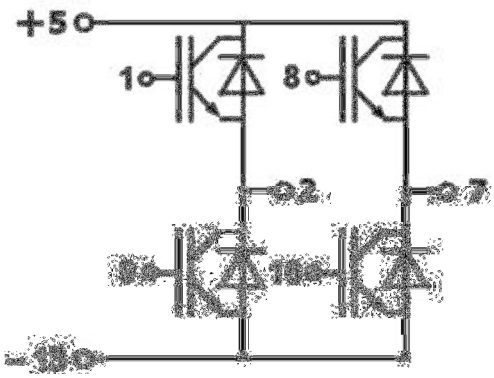


Fig.B.4: The pin-configuration of SK20GH123 device

B.3 Buffer

SN74AHCT125 has been used in the gate driver board design. This device has 14 pins, as shown in Fig.B.5, including four inputs, four outputs and four output-enabling ($\overline{OE}$) inputs[93].

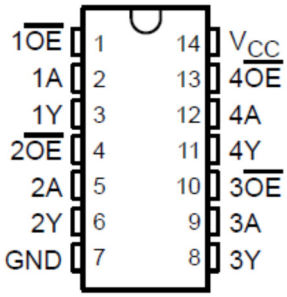


Fig.B.5: SN74AHCT125

The $\overline{OE}$ input can disable or enable the output by being high or low respectively. If the output is enabled then it will follow the input. It means that the output will be equal to the input. The relationship between input and output of each buffer is represented in Table B.1.The logical diagram representing the functionality of the device along with the related pin numbers is depicted in Fig.B.6.

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Table B.1: Function table for each buffer

In this device, the high level output is equal to V_{CC} and the minimum high level input is 2V while its maximum low level is 0.8 V. The input values between 0.8 V and 2 V will not be recognised and the related output for these inputs will not be reliable but in the gate driver the inputs will be 0V and 5V for the low level and high level input values respectively. In order to disable one of the outputs, the related $\overline{OE}$ is connected to V_{CC}, +5V, and irrespective of input the output will have no values. However, if $\overline{OE}$ is connected to ground (zero volt) then the related output will be active and with

connecting the associated input to the 5 volts the output will be 5 volts. Also having 0 volt in the input will make output zero as well.

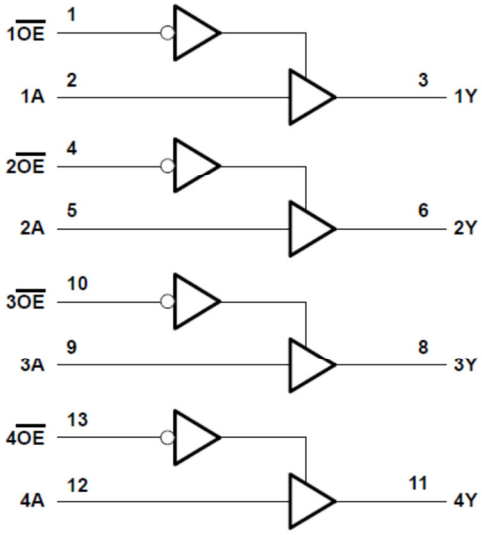


Fig. B. 6: Logic diagram of the SN74AHCT125

B.4 Gate Drive

The HCPL-3180 device includes an integrated GaAsP LED which is providing optical coupling, as shown in Fig.B.7, between input and output. This device comes with 8 pins where pin numbers 1 and 2 are not connected; pin number 2 and 3 are connected to anode and cathode respectively. Pin number 8 and 5 are used for VCC and VEE connection. Pin numbers 7 and 6 are connected to the V_O jointly [109].

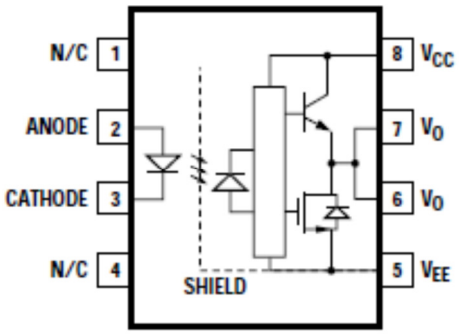


Fig. B. 7: Functional diagram of HCPL-3180

With reference to the data sheet [68] there must actually be a minimum positive voltage of 1.2V across the anode-cathode in order to trigger the GaAsPLED. The recommended voltage in data sheet is 1.5 V therefore, the forward voltage of diode is considered as 1.5V in the design. On the other hand the output voltage of the buffer is 5 V and the voltage across the resistor will be 3.5V and referring to the data sheet [109] the

minimum required input current for the GaAsP LED must be 10mA. Then the highest resistance between the buffer and gate drive must not exceed 350 Ohm in the same time the lowest resistance also must be below 280 Ohm. Moreover in order to select a standard resistance, a 320 Ohm resistor is selected as a series resistance connected in series with the anode of the gate drive.

In continue the calculations to select a proper resistor using equation (B.1) are presented as follow:

$$V_{OB} - V_{IG} = I_{IG} * R_S \quad \text{(B.1)}$$

where V_{OB} is the output voltage of the buffer and V_{IG} is the input voltage of the gate drive. Additionally, R_S is the series resistance, located between the gate drive and buffer, and I_{IG} is the input current of the gate drive passing through the R_S. In the design procedure the following is assumed:

V_{OB}= 5 V

V_{IG} = 1.5 V

I_{IGmin}= 10 mA and I_{IGmax}= 12 mA

R_S can then be calculated as follow:

$5 - 1.5 = 10 * R_S \rightarrow$ the Max R_S will be 350 Ω

$5 - 1.5 = 12 * R_S \rightarrow$ the Min R_S will be 280 Ω

Electrical specifications of HCPL-3180 and associated required parameters are given in table B.2.

Parameters	Specified	HCPL-3180
Opt coupler isolation	Required	Provided
Bandwidth	Max 10 kHz	250 kHz
Input current (ON)	12 mA	10 mA
Input voltage (OFF)	0.8 V	0.8 V
Input forward voltage	<5 V	1.5 V
High level output current	12 mA	0.5-2 A
High level output voltage	5 V	V_{CC}-4

Table B.2: Electrical specifications

A PCB board has been designed using Ultiboard software and printed at Newcastle University. The PCB is built using a one layer copper board and the components have been soldered at bottom copper layer. Fig.B.8 and Fig.B.9 show the design of PCB and the final assembled board respectively. The outputs of the gate drive are connected to the gate and emitter of the related IGBT's by using 8 coaxial and shielded wires. It is very important that the shields in the wires to be connected to the ground the system;

otherwise noise can be induced through the wire and it can generate unwanted switching. Even the length of the wire must be as short as possible in order to avoid any possible induced noises.

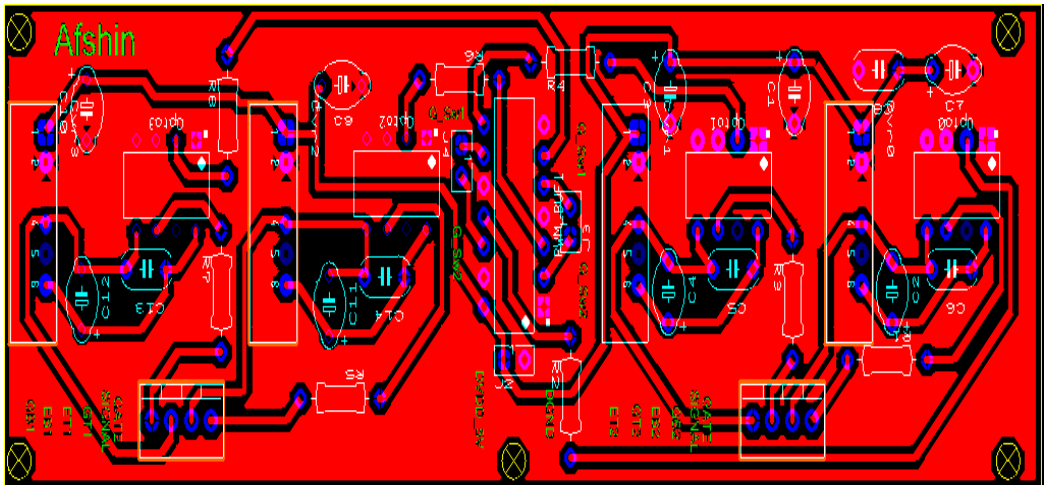


Fig.0.8: Design of PCB Gate Drive Board

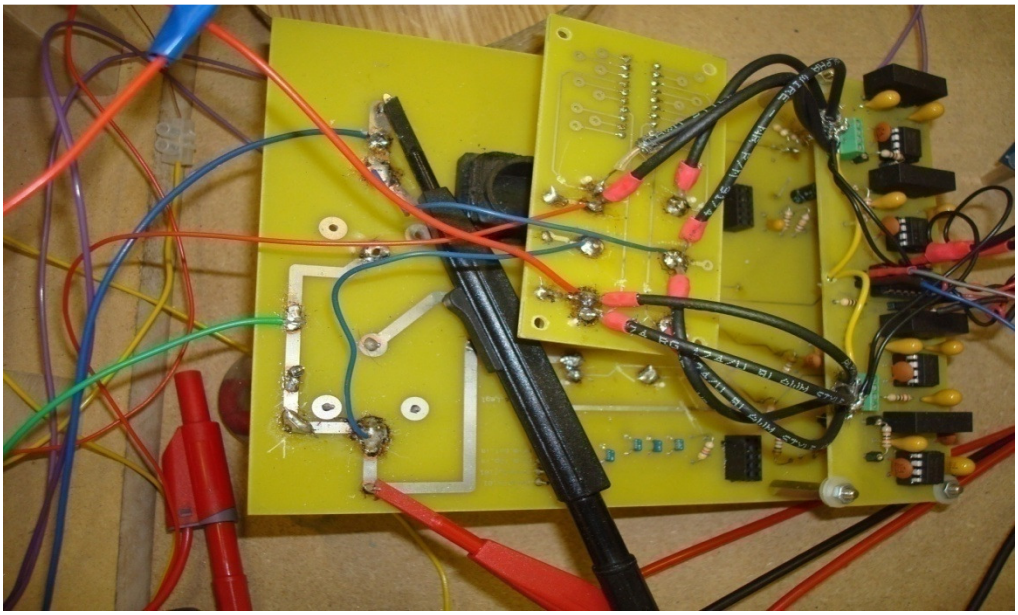


Fig.0.9: Implemented Gate Drive Board

B.5 Isolated power supply

Isolated power supply provides isolation between electronic signals and power circuit. This device, NMF0515S, is shown in Fig.B.10 which is a DC/DC converter [94].The device comes with 5 pins where pin numbers 1 and 2 are connected to the supply voltage of 5 V.Pin numbers 3 and 5 provide the output voltage of 15V. Its rated output

power is 1 Watt and requires no heat sink. It also can provide output current of 67 mA [94].

Fig. B. 10: NMF0515S DC/DC converter

Its output power capacity may reduce by an increase in the operating temperature. The reduction in output power starts from 70° and up to this point it can deliver 100% of the rated power. After this point, the output reduces linearly with an increase in the temperature. For example at 100° the output power is halved. Moreover when the temperature reaches 125°, the output converges to zero. The safe operation zone is shown in Fig. B.11 [94].

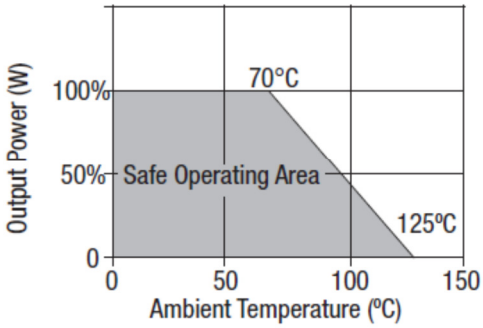


Fig. B. 11: Safe operation zone and out power of MNF0515S at different ambient temperatures

In general, switching ON and OFF of IGBT consumes some energy which must be provided by the gate drive and gate drive power supply. The amount of required energy depends on the gate charge characteristics of the selected IGBT and the switching frequency. The average current which must be supplied is given as follow:

$$I_{Ave} = Q_G * f_O \quad (B.2)$$

where f_O is the operation frequency and Q_G is the total gate charge. The operating frequency in this experimental study is about 1 KHz and the total gate charge can be found from gate charge characteristics curve which comes with data sheet of the IGBT. For SK20GH123 IGBT the gate charge characteristics is depicted in Fig.B.12 and can

be easily observed that for the IGBT, in order to reach its nominal current, it requires 90 nC energy. Therefore the average current will be:

$I_{Ave} = 90 * 1000 = 0.9$ mA

and the required power which must be provided is calculated as follow:

$$P_{req} = I_{Ave} * \Delta V \quad \text{(B.3)}$$

where P_{req} is the required power to turn on the IGBT so that the current through collector-emitter to reach its nominal value. Also ΔV is the range of change of the gate-emitter voltage from OFF to ON status or vice-versa. The gate-emitter voltage changes from -15 to 15 so the ΔV will be 30 volts. Therefore P_{req} is calculated using (B.3) as

$P_{req} = 0.9 * 30 = 27$mW

Referring to the data sheet of the gate drive isolated power supply [94], its output power is 1W, enough to supply the gate drive to turn ON and turn OFF the IGBT. In addition, referring to data sheet of the gate drive, its output power is 600mW which is enough to provide P_{req} as calculated above.

Furthermore, it must be noted that the experimental studies are conducted in order to prove the validity of the proposed control idea which is discussed earlier in chapter 4. However in these studies the collector-emitter current in ON status of the IGBT due to the restriction on the equipment and the available facilities in the UG lab is designed not to exceed 15 A. But yet full P_{req} is required in order to force IGBT to fully conduct the current. For this reason, although the collector-emitter current will rarely reach 15A, but the gate-emitter voltage is designed to be 15V and the P_{req} will be 27mW.

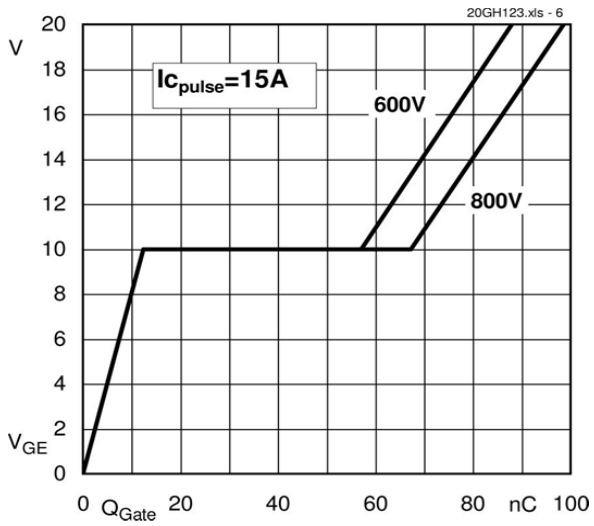


Fig.B.12: Gate charge characteristics of SK20GH123

Despite a small amount of power is required to turn on and turn off the IGBT, a considerable high peak current is required in order to provide an efficient switching. This is because having sufficient current, the required energy will be supplied quickly and the switching will be performed faster. To do so, the gate current must be increased up to the specified permissible value. This value is determined mainly by the output current of the gate drive which is 2.5 A for the HCPL-3180.

B.6 Voltage Transducer (VT)

Voltage transducer is a key component in the voltage measurement board. The LV 25-P VT is shown in Fig. B.13. The measurement of voltage can be achieved by passing a current through the transducer which is proportional to the measured voltage and can be controlled by an external resistor. In the calculation of the resistance it must be noted that the optimum accuracy of the device can be achieved if the primary input current in the measuring of the nominal voltage become 10 mA [95].

Fig. B.1: LV 25-P the selected voltage transducer

In addition the accuracy of VT depends on the value of input current and refer to the data sheet of the LV 25-P [95] its accuracy is 0.8% for I_{PN}=10 mA and 1.5% for I_{PN}=5mA. Furthermore, the turn ratio of the transducer is 2500:1000 and with nominal current at the input the nominal output current will be 25 mA. In order to convert the output current to the voltage and make it useable by the electronic circuit a resistor, RM, needs to be connected between output pin and ground of the electronic board in the measurement board. The connections of the VT and related pins are shown in Fig.B.14. In this device +HT and –HT are positive and negative polarity of connections of the input voltage. +VC and –VC are the supply pins. The output is shown by M and it must be connected directly to the RM resistor.

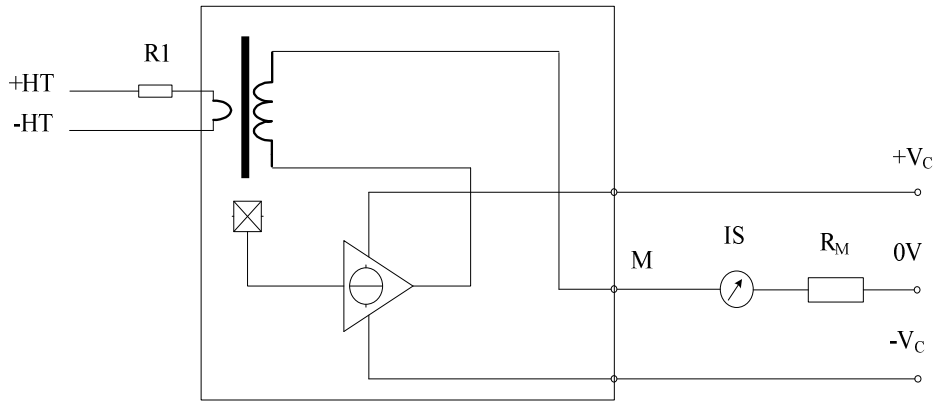


Fig. B.2: Connections of VT

As a part of the hardware design and implementation, a PCB board which is shown in Fig.B.15 is designed using Ultiboard software. The designed PCB is printed in the Newcastle University and afterward the other devices are populated. After implementation, the board itself was tested and validated using fixed AC and DC voltage sources. The final implemented voltage measurement board is shown in Fig.B.16.

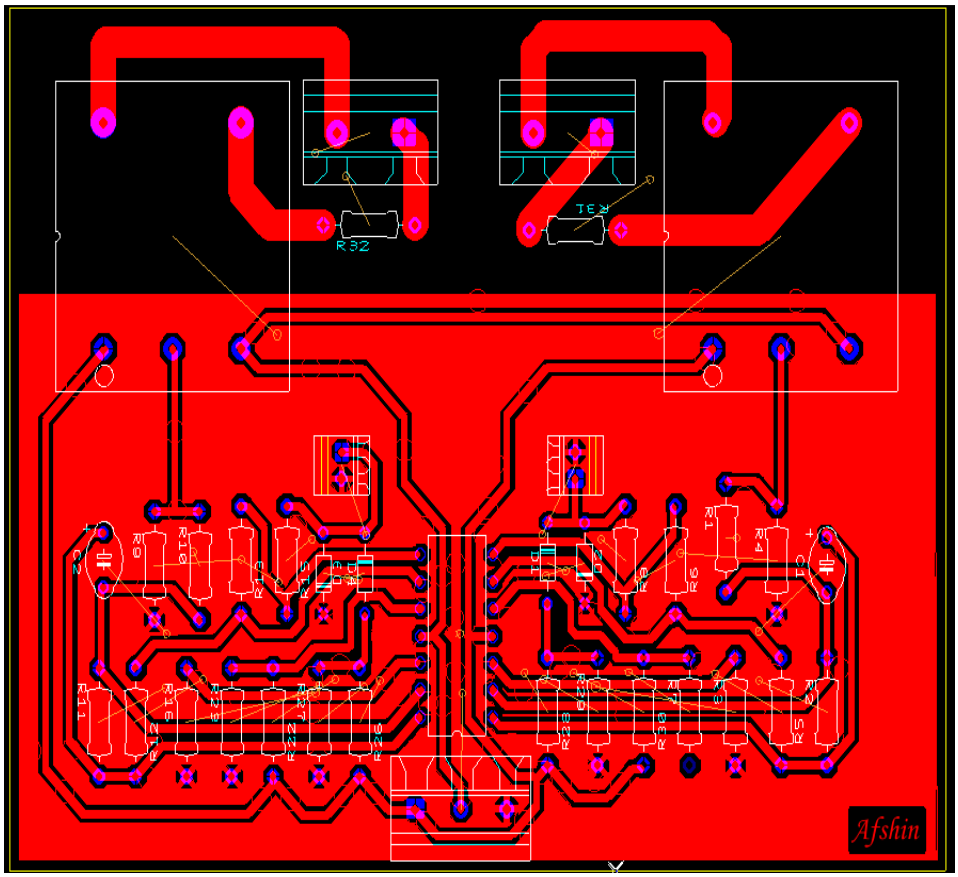


Fig.B.15: PCB designed voltage measurement

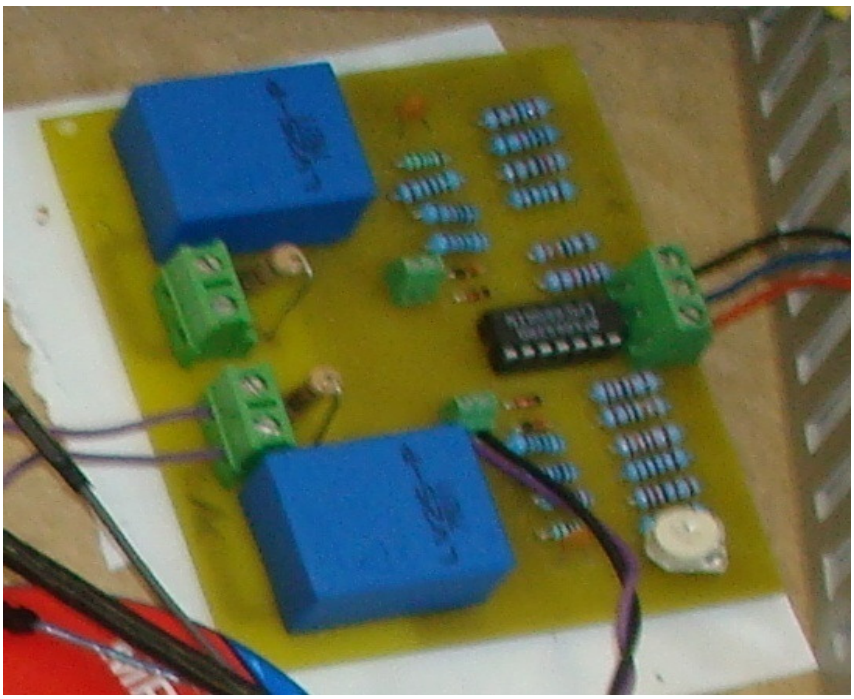


Fig.B.16: Implemented voltage measurement board

B.7 Op-Amp

LMC660CMOp-amp chip is used in the voltage and current measurement boards. It is used to boost up the main signals (i.e. voltage or current) and eliminate the unwanted signals. It includes four Op-amps and its connection diagram is shown in Fig.B.17. As long as its electrical features concern it must be noted that it has rail to rail output swing therefore, the output voltage can dynamically vary between VSS and VEE [96].

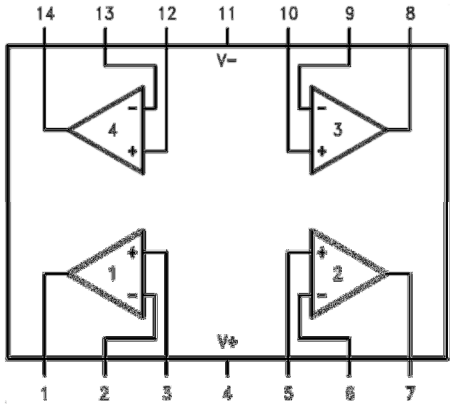


Fig. B.3: Connection diagram of the LMC660CM

B.8 Current Transducer

Current transducer LTS 25-NP shown in Fig.B.18 is employed in the current measurement board. Its accuracy is ±0.2 % at nominal input current and temperature of 25°C [97].

Fig.B. 4: LTS 25-NP Current Transducer

The I-V characteristic of the CT presented in Fig.B.19 shows that for input currents above the absolute value of I_{Pmax} the output voltage remains unchanged, i.e. gets saturated. The output voltage for input currents above I_{Pmax} will retain in the fixed value of 4.5 volts and for currents less than $-I_{Pmax}$ will remain in 0.5 volts. I_{PN} (nominal input current) for this current transducer is 25 A then with the nominal input current the output voltage will be 3.125 V. It can be concluded that the permissible output voltage margin to measure the currents between 0 up to 25 A is 0.625 V.

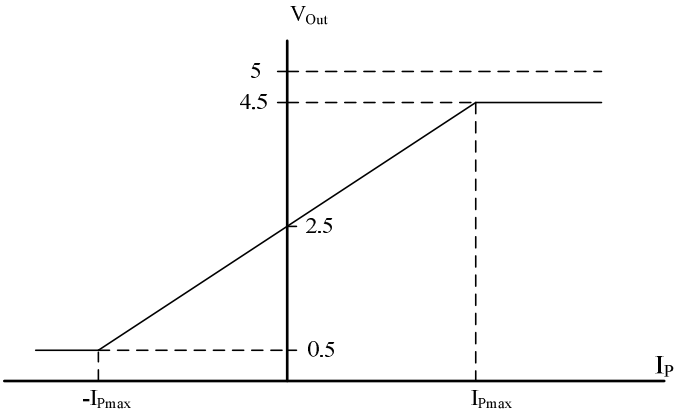


Fig.B.5: I-V characteristic of LTS 25-NP Current Transducer

However if the CT is supposed to be used to measure lower currents then different configurations of the input can be used in order to achieve the accuracy of 0.2 %. To do

so, three different configuration of CT can be used as depicted in Table B.3. For example, for input currents about 25 A it is recommended that pin numbers 1, 2, 3 to be connected together and pins 4, 5, 6 also to be tied together as well then the turn ratio of 1 will be selected in the transducer.

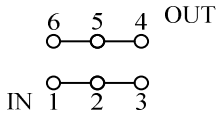
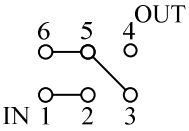
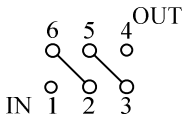
Number of Primary Turns	Primary Nominal Current rms I_{PN} [A]	Nominal Output Voltage V_{Out} [V]	Recommended Connections
1	±25	2.5±0.625	
2	±12	2.5±0.600	
3	±8	2.5±0.600	

Table B.3: Different configuration of CT with different turn ratio

The connection of LTS 25-NP is shown in Fig. B.20. It shows that the CT can be supplied by 5 V DC and the ground is shared between supply voltage and output voltage. In this diagram, the input current is shown by ±IP which can be shared between input pins 1, 2, 3 and output pins 4, 5, 6. The turn ratio of CT can be changed by choosing one of the connections in Table B.3.It is noted that if the direction of input current is from pins 1, 2, 3 to 4, 5, 6 the polarity of the output voltage will be positive. If the direction of input current changes then the polarity of output voltage will be negative. Despite of this the output voltage is still positive (minimum 0.5 volts) because there is 2.5V offset at the output. However the change of direction must be considered in the calculations.

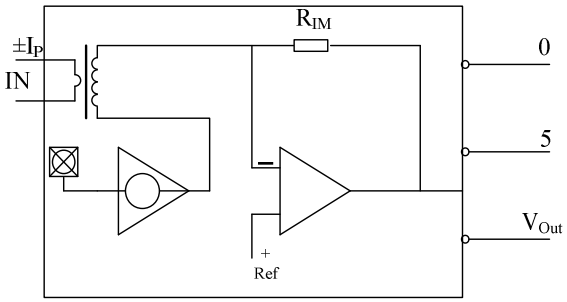


Fig. B.20: Connection in LTS 25-NP Current Transducer

A PCB is designed for the current measurement board using Multisim and Ultiboard software. The designed PCB is printed at Newcastle University and it layout is shown in Fig.B.21.

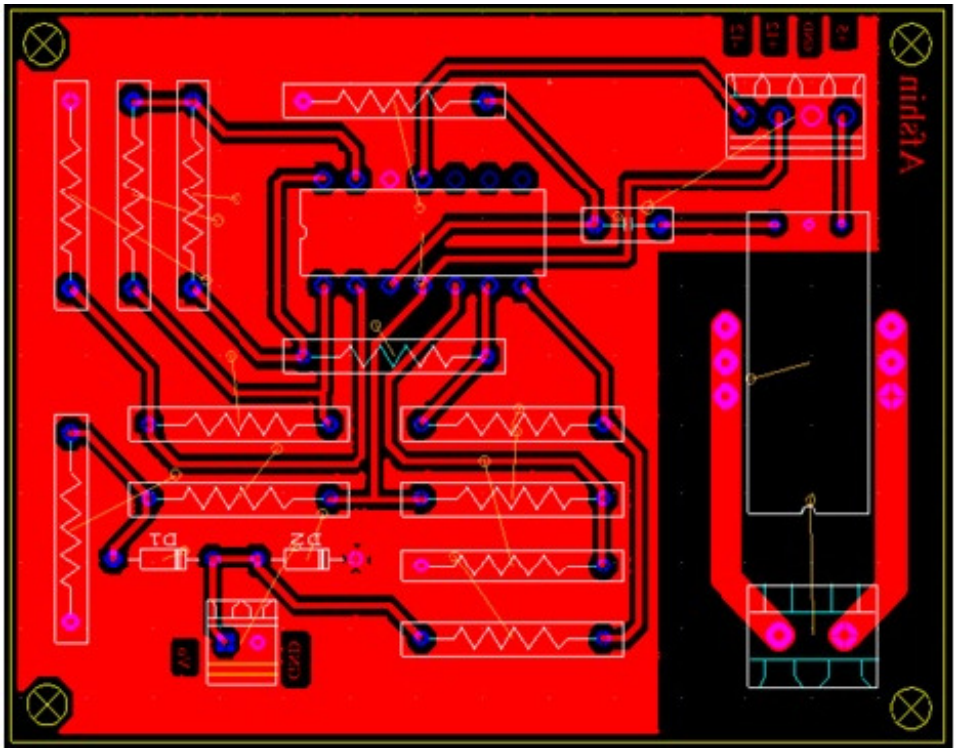


Fig.B.21: layout of designed and printed PCB for current measurement board

After printing the PCB, other components including p-amps, CT, resistors etc... have been soldered in the UG lab as a part of the implementation process. The final completed current measurement board is shown in Fig.B.22.

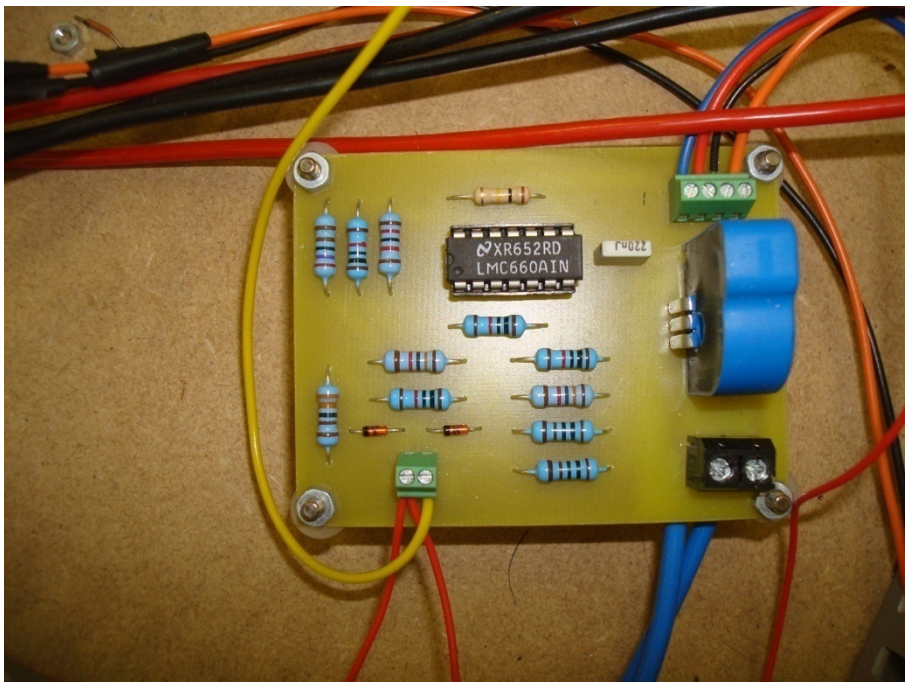


Fig.B.22: The current measurement board

Appendix C: Microcontroller

C.1 Introduction

A microcontroller is needed to run the control algorithm. The algorithm is being executed by CPU which is the main part of a microcontroller. However a CPU sends commands and receives information by importing and exporting of data. Then a microcontroller needs to provide a proper input and output (I/O) ports in order to be able to run an algorithm and control a plant. The received signals are in an analogue format and their configuration needs to be converted to digital. This is achieved with an analogue to digital (A/D) converter within the microcontroller. The digital data is handled using data memory access (DMA) in the microcontroller and this can avoid involvement of CPU in data management. In addition the control algorithm of the DSSC includes a PWM generator. This functionality either can be provided by the microcontroller itself as an embedded function or it can be written in a code and executed by the CPU.

In appendix C the employed microcontroller, dsPIC33FJ256MC710, in the implementation of test rig is explained. The microcontroller comes with embedded board and it includes its own PWM generator, A/D, I/O ports and DMA.

C.2 Microcontroller

The selected board is shown in Fig.C.1 with description of different parts. The microcontroller (dsPIC) itself needs to be supplied by 3.3 V, which comes from a robust on-board power supply. This power supply is well regulated for 9V-36V input voltage range. Other different voltage levels for the different parts of the board are provided internally. Even the polarity of the input voltage of the board is not important and a voltage between the permitted margins can be used in the input. Robustness of the embedded board in terms of using wide range of voltages, no matter what polarity they have, makes the embedded board flexible and easy to use. In the designed test rig, the embedded dsPIC board is supplied with + 9V via a DC power distribution feeder which is built to supply the electronic boards within the test rig. Additionally, the dsPIC can be supplied externally via available connectors and the reference voltage for the ADC can be altered and provided externally [110].

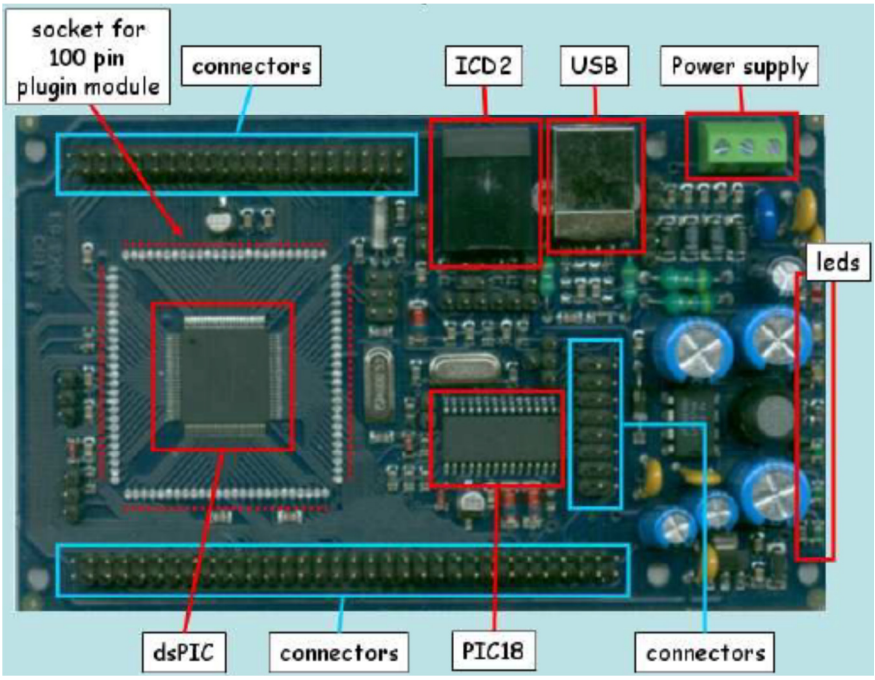


Fig. C. 1: dsPIC33FJ256MC710 within an embedded board

It can be observed from Fig.C.1 that the board comes with six different LEDs. They facilitate monitoring different status of operation of the board. Different operation mode of the board is indicated by the related LEDs which they come in different colour in different operation mode. More details of each LED and related colour can be found in table C.1 [110].

LED	Colour	Function
DL1	Green	Input power supply
DL2	Green	Internal +5V power line activity
DL3	Green	Internal +5V power line activity
DL4	Yellow	dsPIC (R) DSC controlled led (e.g., debugging purposes)
DL5	Yellow	Internal PIC18 controlled led
DL6	Red	USB cable connection monitor

Table C.1: Colours of LEDs indicating different functionality of the board

As soon as the power supply is connected, the DL1 becomes green indicating input power supply is on.

The dsPIC's pins are available at the connectors which are shown in the Fig.C.1 [92]. The connectors assign easy access to all the pins in the microcontroller. The signals coming from the measurement boards, as well as the signals going to the gate drive board, are connected to the dsPIC via these connectors. The pin configuration of the dsPIC33FJ256MC710 is shown in the Fig.C.2 which is a Thin Quad Flat Pack (TQFP) 100 pin chip. Pin numbers 93 (PWM1L), 94 (PWM1H), 98 (PWM2L) and 99 (PWM2H) are used as PWM outputs. Pin numbers 25 (AN0), 24 (AN1) and 23 (AN2) are used as analogue inputs for two voltage signals and one current signal coming from the measurement boards. All pins are accessible by sockets provided in the board. This facilitates direct access to the dsPIC.

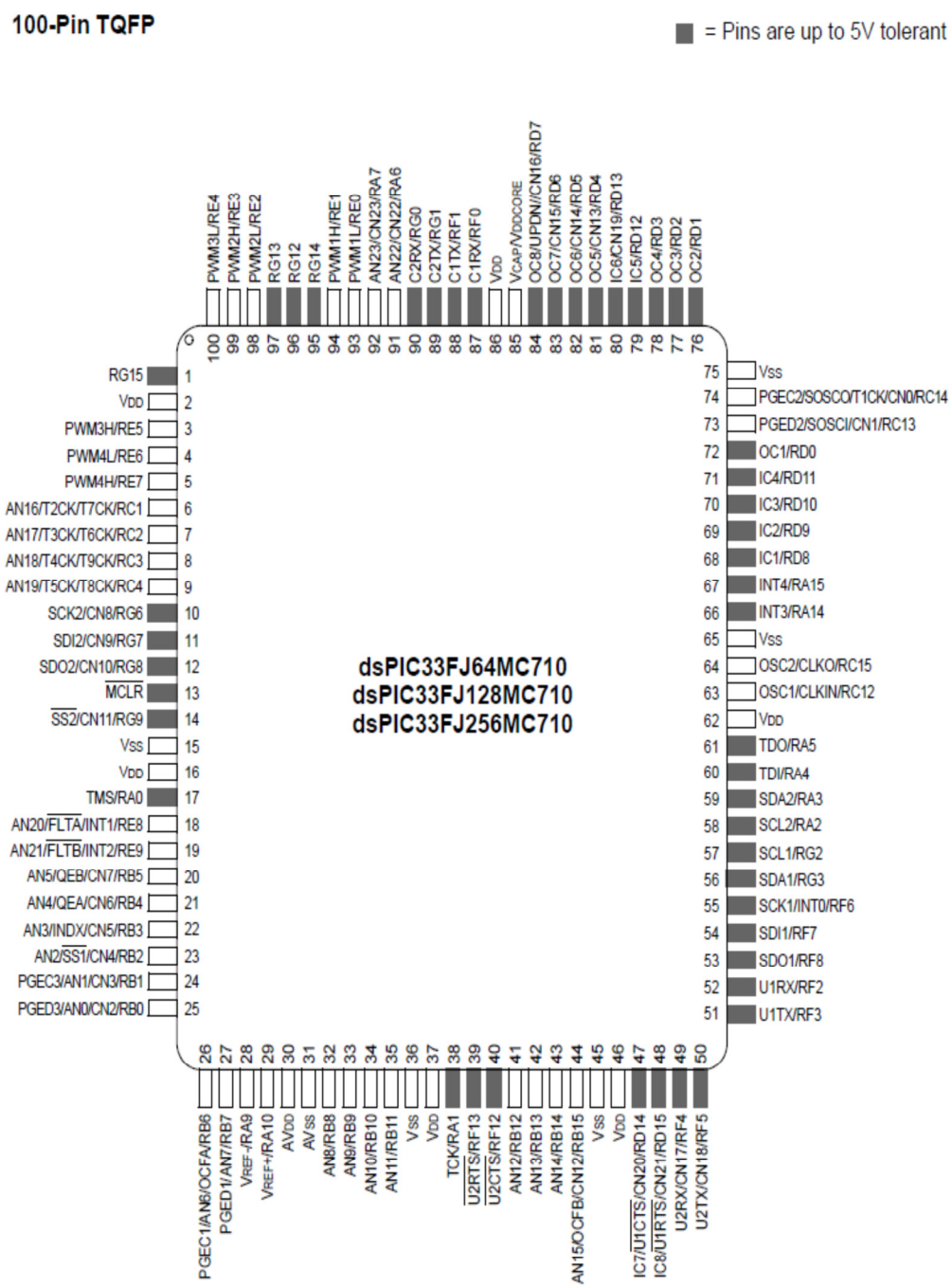


Fig.C.2: Pin diagram of dsPIC33FJ256MC710

It operates like an interface and must be used along with MPLAB software installed in the PC. It gives the opportunity for the programmer to see the status of the registers in the breakpoint [74]. The program written in C code is then compiled using MPLAB software and uploaded to the controller via MPLAB ICD 2 (shown in Fig. C.3). Once running the program in the microcontroller, the status of the variable and registers can be downloaded to the PC again using the MPLAB ICD 2. This communication even

allows amending the value of registers which can be very useful in debugging the program [99].

Fig. C. 3: MPLAB ICD 2

C.3 Direct Memory Access (DMA)

Direct Memory Access (DMA) is used to manage data between the CPU and other peripherals in the dsPIC. This helps the CPU not to be involved in transferring data between the registers. The peripherals which are involved with DMA in this project are [93]:

- ADC
- Input Capture
- Output compare

Each DMA must be configured properly to carry out specific functions. There are six different registers in the DMA controller which need to be set to certain values. For example, DMAxCON configures channel x to carry out a certain mode of operation. Also Enabling or Disabling the channel is done by this register. As another example, DMAxCNT deals with the numbers of requests from DMA which must be set in DMA controller.

In this project, DMA is set for peripheral indirect mode and continuous, not Ping-Pong mode. The related code is as follow:

```
void initDma0(void)
                {
                DMA0CON = 0x0000; // no increment
DMA0CONbits.AMODE = 0; // Config DMA for Peripheral indirectmode
DMA0CONbits.MODE  = 0;// Config DMA for Continuous no Ping-Pong mode
                DMA0CNT=3;    // 4 DMA request
                DMA0REQ = 13;         // 0001101 = ADC1 – ADC1 Convert
```

```
DMA0PAD=(int)&ADC1BUF0;
DMA0STA = __builtin_dmaoffset(DMA0_buffer);
DMA0CONbits.CHEN=1;    // Enable DMA
IFS0bits.DMA0IF = 0; //Clear the DMA interrupt flag bit
IEC0bits.DMA0IE = 1; //Set the DMA interrupt enable bit
DMA0CONbits.CHEN=1; // Enable DMA
}
```

C.4 PWM Generator

ThedsPIC33FJ256MC710 has four PWM generators. Each of them can be configured independently. In this project two of them have been employed in order to trigger four IGBT's in the H-bridge converter. Each PWM generator has two outputs, high and low, which can be in complimentary or independent mode. For example, in the complimentary mode if the high value output has logic "1" then the low value output definitely is "0". However, in the independent mode the low value output is not necessarily "0" and can be "0" later on.

The PWM generator can be configured to insert dead time in the transition from low to high or high to low status. This is a very useful capability of the PWM generator when generating two outputs from one single PWM signal in order to trigger two IGBTs in one leg. If two IGBTs in one leg of the converter conduct at the same time then it will create a short circuit, thus will discharge the DC capacitor. By introducing dead time between the switching times of the IGBTs there will be no short circuit in the related phase.

Output of PWM can operate in different modes as follow [112]:

- Single Event PWM Operation
- Edge Aligned PWM Mode
- Centre Aligned PWM Mode
- Complimentary PWM Output Mode

The Centre Aliened PWM mode has been used in this project then only this mode is explained here and further information regarding the other modes of operations can be found in [96].The centre aligned PWM mode, as shown in Fig.C.4,usesPxTMR, PxDC and PTPER parameters to generate PWM pulses. For example in half period when the PxTMR reaches to the PxDC value the related PWMxH output becomes zero (low level). The output value is zero till the second half period when the PxTMR again

becomes equal to the PxDC and the output becomes “1”. The change of value of output happens each time PxTMR become equal to the PxDC.

However this change depends on the mode of PxTMR. For example, when PxTMR is in up counting mode then the output value will change from “1” to “0”. There will be other way around when the PxTMR is in down counting mode. The mode of PxTMR changes when the value of PxTMR reaches the PxTPER. This event happens twice per period as it is explained in continue. Initially, the PxTMR value is zero then it starts to count up until it reaches the PxTPER value. This time interval is equal to half period and at this point PxTMR starts to count down. After another half period the PxTMR reaches to zero which is the time again to switch to up counting mode.

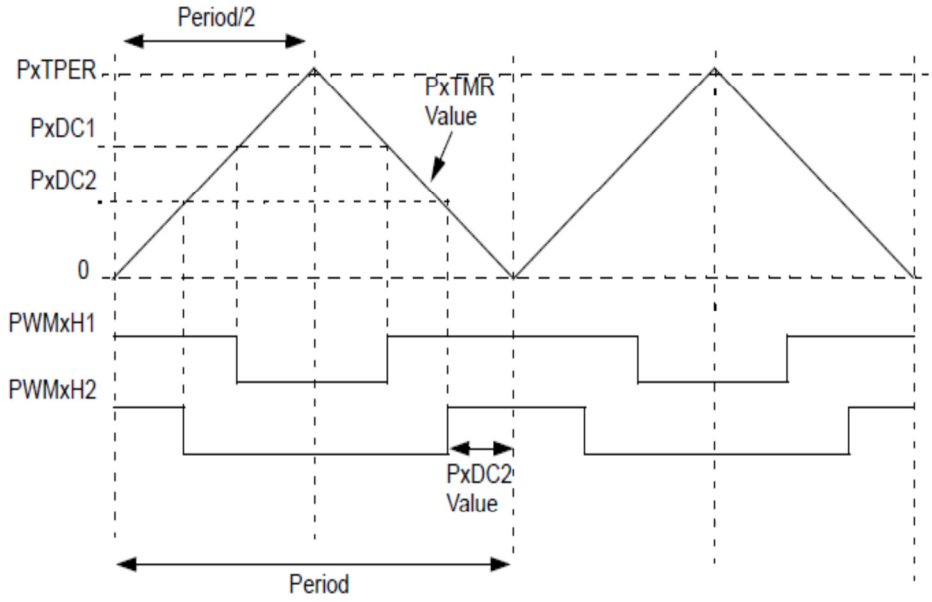


Fig. C. 4: Centre aligned PWM mode

In dsPIC33FJ256MC710 each PWM generator can produce two PWM pulses with different duty cycles but with the same frequency. This can be obtained by using different PxDC values; each of them can generate different pulses in the corresponding output. The value of PxDC is updated by the reference signal at each clock. With new value of PxDC then the generated pulse will be different and of course updated. This process makes the producing of the demanded waveform (in our project a sinusoidal voltage which is orthogonal to the line current) become possible by the converter. The value of PxTPER determines the frequency of carrier signal in the PWM generation. This is so called chopping frequency in the PWM and it can be increased or decreased by decreasing or increasing the PxTPER, respectively.

The PWM generator can be configured to operate in different mode with different functionalities. Such a configuration is represented in the following code. For example, the PWM outputs can be selected to operate in pair or single mode. Having the pair mode selected, the pin pairs can be either in the Independent output mode or in Complementary output mode. In the independent mode each of pin pairs can hold either values of "0" or "1". It means that both in the same time could have value of "1" or "0". In complementary mode if one of them is high the other is necessarily low.

In the DSSC prototype project the complementary mode is selected. This is because in H-bridge converter there are two series-connected IGBTs in each leg of converter and if they are triggered at the same time then there will be a short circuit in the DC bus. In order to avoid such a failure they must be protected against being "ON" at the same time.

After selection of the mode of operation for the outputs, the outputs themselves must be activated. This is activated by Enable/Disable bit for the corresponding output in the configuration register of the related PWM generator. For example, in order to enable the "HIGH" output of the PWM1 the "PWM1CON1bits.PEN1H", as it is represented in the following code, must be set to "1".

As explained earlier the PxTPER is employed in PWM generator to achieve the desired chopping frequency. Normally this frequency remains unchanged during the operation. The PxTPER can be calculated as

$$\text{PxTPER} = \frac{\frac{\text{FCY}}{\text{FPWM}} - 1}{2} \qquad \text{(C.1)}$$

where PxTPER is related to half of the period of the carrier signal, FCY is the instruction clock of the dsPIC. This FCY determines the speed of operation of the device. With dsPIC33FJ256MC710 operation frequency of 40 MHz can be achieved. FPWM is the chopping frequency of the carrier signal. For example, if using FCY of 20 MHz in order to achieve PWM frequency of 20 kHz, PxYPER can be calculated as

$$\text{PxTPER} = \frac{\frac{20\text{MHz}}{20\text{kHz}} - 1}{2} = \frac{999}{2} = 499.5 \cong 499 \qquad \text{(C.2)}$$

The PxDC, the duty cycle of the pulses, are changing all the times during the operation. Source of changes is the reference signal itself. For this reason, there is a facility in the PWM generator which provides opportunity to update the PxDC immediately after any change within the reference signal. Also, the update can be taken place at the end of each clock. In the prototype implementation, the update is set to be taken into account at the end of each clock in order to avoid disturbances.

```
voidinit_PWM()
{
P1TCONbits.PTCKPS = 0b00;
P1TCONbits.PTOPS = 0b0000;  //<3:0>: PWM Time Base Output Postscale Select bits
P1TCONbits.PTMOD = 0b11;    //<1:0>: PWM Time Base Mode Select bits ---11 = PWM time base operates in a Continuous Up/Down mode with interrupts for double PWM updates
PWM1CON1bits.PMOD1 = 0;
PWM1CON1bits.PMOD2 = 0;
PWM1CON1bits.PMOD3 = 0;   // PWM I/O Pair Mode bits
FPOR1bits.HPOL=0 ;//1 = PWM I/O pin pair is in the Independent Output mode
//0 = PWM I/O pin pair is in the Complementary Output mode
PWM1CON1bits.PEN1H =1;
PWM1CON1bits.PEN1L = 1;
PWM1CON1bits.PEN2H = 1;
PWM1CON1bits.PEN3H = 1;
PWM1CON1bits.PEN2L = 1;  // PEN4H=1 PWMxH4 I/O Enable bits(1,2)
PWM1CON1bits.PEN3L = 1;
PWM1CON2bits.IUE = 0;    //IUE=1 Immediate Update Enable bit
PWM2CON2bits.IUE = 0;
PTPER = 6500;        /* PTPER = ((1 / 400kHz) / 1.04ns) = 2404, where 400kHz
//PTPER = 1000; // is the desired switching frequency and 1.04ns is PWM resolution. */
/*~~~~~~~~~~~~~~~~~~PWM1Configuration ~~~~~~~~~~~~~~~~~~~~~~*/
PDC1 = 640;                      /* Initial Duty cycle */
/* Clock period for Dead Time Unit A is TcY */
/* Clock period for Dead Time Unit B is TcY */
P1DTCON1bits.DTAPS = 0b00;
P1DTCON1bits.DTBPS = 0b00;
/* Dead time value for Dead Time Unit A */
/* Dead time value for Dead Time Unit B */
P1DTCON1bits.DTA = 8;
P1DTCON1bits.DTB = 5;
/* Dead Time Unit selection for PWM signals */
/* Dead Time Unit A selected for PWM active transitions */
```

```
P1DTCON2bits.DTS3A = 0;
P1DTCON2bits.DTS2A = 0;
P1DTCON2bits.DTS1A = 0;
P1DTCON2bits.DTS3I = 1;
P1DTCON2bits.DTS2I = 1;
P1DTCON2bits.DTS1I = 1;
P1TCONbits.PTEN = 1; // PWM Time Base Timer Enable bit Enabling PWM Pulse Generation
 //1 = PWM time base is on
 //0 = PWM time base is off
}
```

C.5 Analogue to Digital Converter (ADC)

Analogue signals come from the measurement boards need to be converted to the digital format and this is achieved in microcontroller through means of an ADC. In the laboratory prototype DSSC test rig, the employed microcontroller, dsPIC33FJ256MC710, includes an integrated ADC. The block diagram of the ADC module is shown in Fig.C.5, where it comes with 32 analogue inputs connecting to pins AN0 AN1...AN31.These inputs can be selected by using the control bits to be connected to a sample and hold devices. This will provide an opportunity to control the incoming signals and decide to connect the desired signal within a proper timing to the ADC. It means that all of the inputs eventually can be connected to the ADC but this can happen only if the related control bit becomes “1”[94].

One of the key features of the ADC module is that it can take an external reference signal instead of an internally provided one. This feature can be used to manipulate the conversion resolution. However in the DSSC prototype implementation the internal reference signal has been employed in order to avoid complexity. Also the ADC module supports DMA which allows the data to be stored in the memory without using CPU. This attribute of ADC saves time and consequently speeds up the operation of device.

The ADC module, like other parts of the dsPIC33FJ256MC710, has its own configuration registers. These registers allow selecting different configuration of the module. For example, the analogue input channel s can be selected and configured using these registers. Even the “ON” and “OFF” mode of ADC can be controlled by allocating “1” or “0” to the associated register. In the DSSC prototype inputs AN1, AN2

and AN3 are allocated as analogue inputs. These three inputs receive analogue signals from current and two voltage measurements.

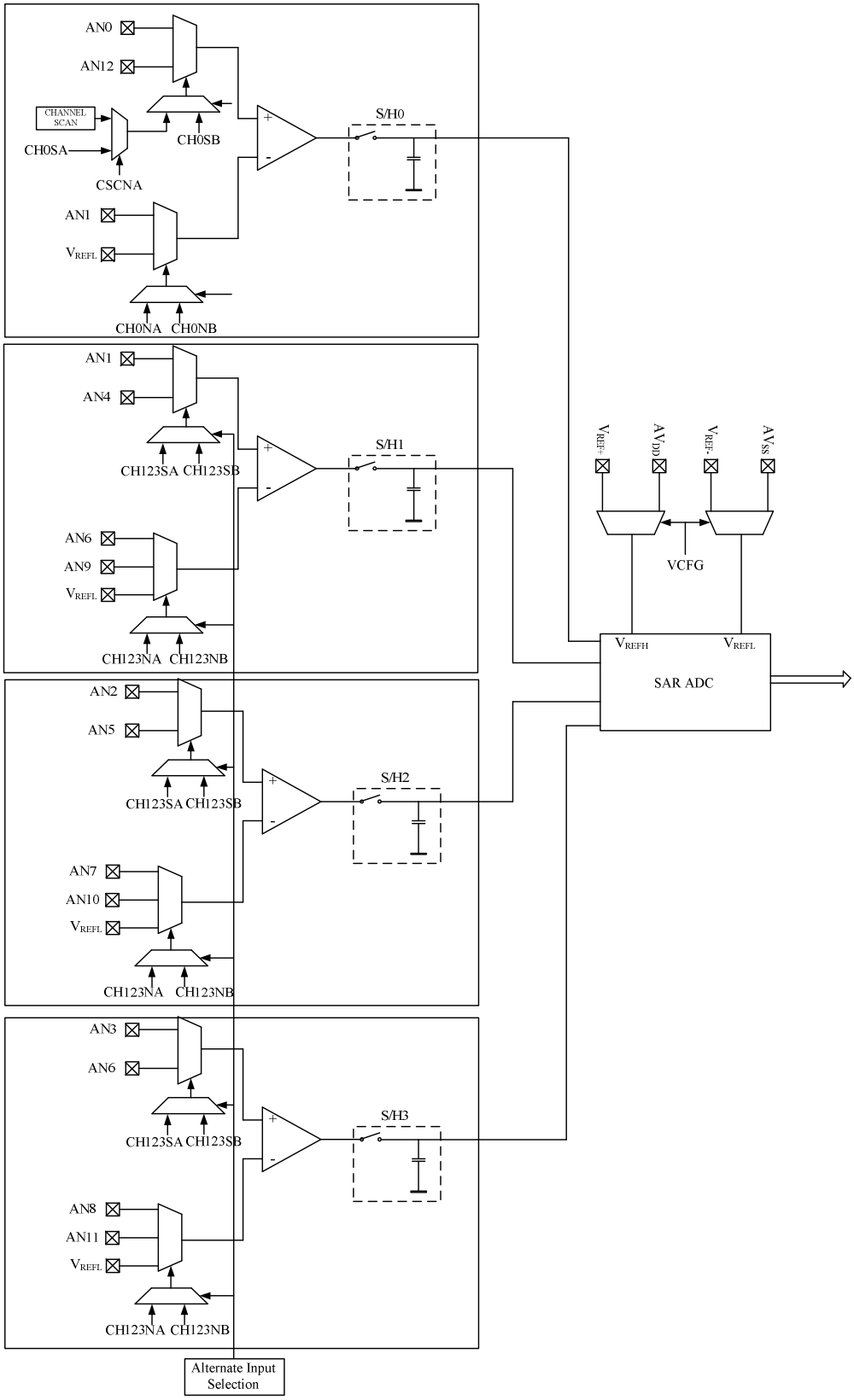


Fig.C.5: The block diagram of the ADC module

C.6 I/O Ports

I/O ports are used to send or receive data in order to monitor and control the other devices. In the dsPIC33FJ256MC710 all the pins can be employed as I/O ports except pins for supply (such as VDD or VSS) and the pins used for clock and oscillator (OSC1/CLKL). A dedicated port model is shown in Fig.C.6 where each port can be configured to be “Input” or “Output” [92].

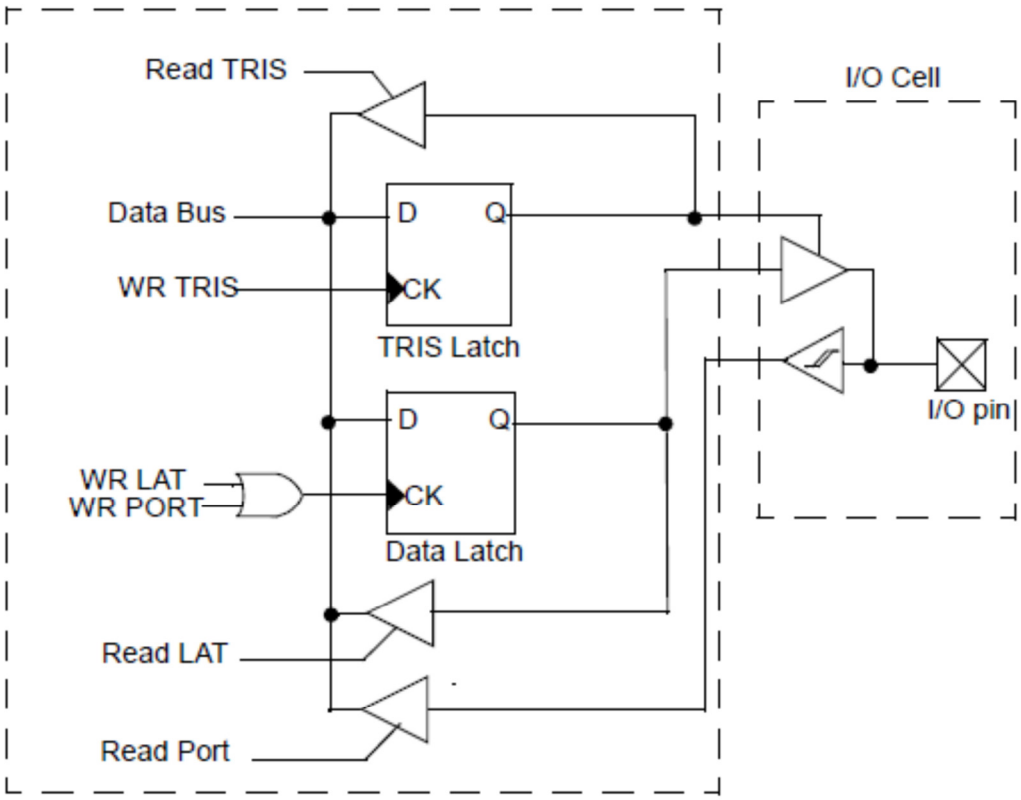


Fig.C.6: A typical block diagram of I/O port

Each I/O port needs four registers namely, TRIS, PORT, LAT and ODC in order to be set to operate in desired mode. For example, the TRIS register defines the flow direction of data by enabling the I/O port to be “Input” or “Output”. When the TRIS register (for the corresponded I/O port) is set to “0” it means that the port is an “Output” while “1” in the TRIS register shows that the corresponded port is an “Input”. “PORT” register allows reading or writing of the corresponding I/O pin. To do so, some instructions like “BSET” or “BCLR” are needed to be used. For instants, the example code for “BSET” can be as follow:

```
BSET      PORTA,   #0              ; Set pin 0 on Port A to ‘ 1’
```

```
BSET    PORTA,  #1          ; Set pin 1 on Port A to ‘ 1’
```

In the above code, the “BSET” instruction sets value of “1” to the port “A”. However, reading from and writing into the port can be problematic if the read and write follows each other (so-called “Read-Modify- Write” mode). The problem can occur when these instructions want to be executed one after each other while the voltage in the corresponding pin has not reached to the target level. In occurrence of this problem, wrong data will be presented in the I/O pin. In order to avoid the fault the “LAT” register must be employed. In the “Read-Modify-Write” operation the data can be red from the port latch and is written in the I/O port pin. The following code shows the writing on the I/O port using LAT register.

```
BSET    LATA,   #0          ; Set pin 0 on Port A to ‘ 1’
BSET    LATA,   #1          ; Set pin 1 on Port A to ‘ 1’
```

There is no difference between LAT and PORT register when they are used to write to the I/O port. However, using these two registers to read from I/O port can result in different values. For instance, LAT reads the previous value which was held in the port but PORT reads values which are currently on the port.

Appendix D: Application of DSSC in Distribution Networks; Feasibility Study

D.1 Introduction

Feasibility of DSSC application in the existing 11kV distribution networks, in terms of their mechanical withstand capability, has been studied. The study includes overhead line design considerations and evaluation of the strength of poles. The study identifies important mechanical factors which must be considered in application of DSSC in the electrical networks. The study focuses mainly on the existing networks and employed equipments within their design. For example, the poles used in the construction of low voltage overhead lines are not as strong as transmission line towers and they can be made of different type of wood or metal. The overhead line wires can also be made of a wide range of conductors and materials. In addition, the effect of environmental conditions such as wind and the consequence oscillations has been studied.

D.2 Overhead Line Design Consideration

The mechanical construction of an overhead line, and its maintenance, requires a lot of attention in the design process of the line. Generally the most likely element to fail in an overhead line is the conductor and this can happen because of high winds or overloading of the line due to ice. For example, most of the reported overhead line failures in 11kV distribution circuits are related to line breakages [113]. Long spans increase the possibility of conductor clashing and may cause some damage at the contact points. This will weaken the strength of the wires and increase the likelihood of a break down in windy or bad weather conditions. For these reasons, care must be taken to ensure that the extra weight presented by the suspension of DSSC devises from the line conductors is fully taken into account when considering the application of DSSC.

D.2.1 Restricted vibration

Vibrations in an overhead distribution line can be divided into two categories. The first is an oscillation with large amplitude and low frequency referred to as Galloping and is generated by winds with speed of 5-10 miles/s. This type of vibration usually occurs in locations with long spans, for example where lines cross rivers or highways. The second

type is referred to as Aeolian vibrations and is a vertical vibration with low amplitude and normally with the frequency of about the natural frequency of the line.

With regard to the Galloping, the suspension of DSSC from existing lines acts like added inertia and will initially contribute toward damping of any small amplitude weak oscillations in the line. However, as the large amplitude oscillation starts, for example as a result of strong wind, the extra weight of the DSSC device will boost the oscillation and may lead to a clash between the lines.

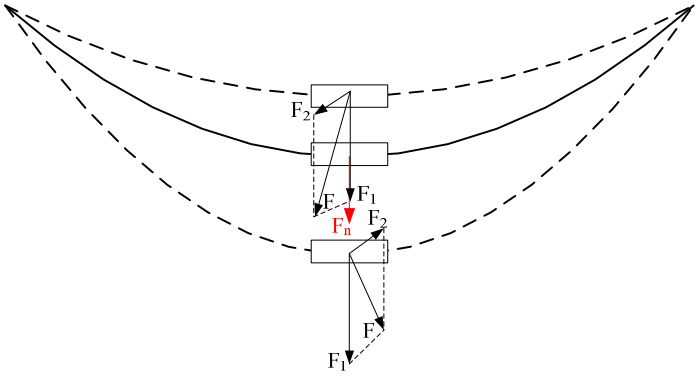


Fig.D.1: Decomposition of mechanical forces

The decomposition of mechanical forces in a DSSC compensated line is shown in Fig.D.1. In the figure, F is a mechanical force pointing toward the ground due to the mass of the line and the DSSC device. Under normal conditions, i.e. no oscillation, F_2 is zero and F_1 is equal to F. However, as the line moves to the side as a result of Galloping F will be decomposed into the two orthogonal forces F_1 and F_2 with F_2trying to force a return back to the pervious conductor location. Thus, and in accordance with Newton laws of motion, it may be concluded that the extra mass of the DSSC device will help stop the initialisation of Galloping. However if as result of strong winds Galloping is initiated, the extra mass means that it may become more difficult to stop. Therefore where there is a likelihood of Galloping, in areas like river or highways crossings (in locations with long span), the installation of DSSC is not recommended in those sections of the line. Because of the distributed nature of the compensation, however, this will have a minimal effect on the performance of the line as a whole.

Aeolian vibration on the other hand is not directly related to the weight of the wire and will not be significantly affected by the presence of DSSC devices in the power lines. This kind of vibration is caused by continuous wind and the margin for this movement is similar to the wire dimensions.

D.2.2 Conductor tension

Conductor tension is generated by the line mechanical load which is a combination of wind force and weight of the conductor. The former is mainly horizontal and is referred to as the Maximum Conductor Pressure (MCP), while the latter is a vertical load and is referred to as the Maximum Conductor Weight (MCW). The maximum permissible tension of the conductor is the tension which the conductor can stand at a temperature of −5.6°C, considering the effects of all loads including wind pressure and weight. The maximum tension of the conductor must of course be within certain safety limits. The suspension of DSSC modules, however, means that there is a possibility of the resultant tension exceeding the existing safety margins as a result of the extra weight of the modules.

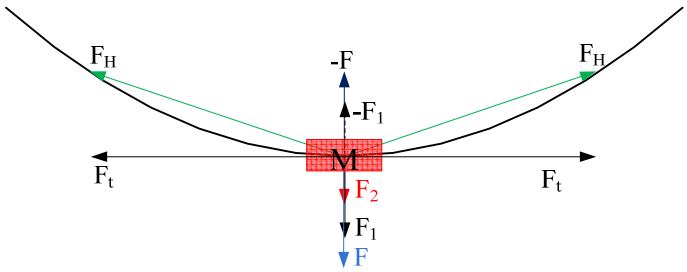


Fig.D.2: Interaction between the forces in a compensated distribution line

Fig. D.2 shows the forces generated by the mass of the line, the mass of the DSSC module and the forces generated in the line to counter the resultant force. In the figure, F_2 is generated by the mass of the DSSC module and is equal to $m_D g$, where m_D is the mass of the DSSC device and g is the gravitational acceleration. F_1 represents the force generated by the mass of the line and is equal to $m_l g$ where m_l is the mass of the line section between two poles. F is the sum of the two forces F_1 and F_2. In order to counter the effect of F, the line generates the force F_H, which may be decomposed into two orthogonal components, −F and F_t, as shown. The force −F has exactly the same magnitude as F but acts in the opposite direction while F_t is the force which creates tension in the wire. The line tension will therefore increase with any increase in F. For this reason the effects of adding the external weigh represented by the DSSC modules must be carefully studied.

The tensions withstand capability of a power overhead line varies from line to line depending on the dimensions, materials and geometry of the wires. The characteristics

of Aluminium alloy, as a commonly used conductor for 11kV overhead lines, is selected for investigation in this study. A conductor with a cross sectional area of 180.7 mm^2 has a mass of approximately 497 kg per km, with a calculated breaking load of 50.65 kN [60]. Assuming that each DSSC module has a mass of approximately 50 kg (typical weight of DSSC as mentioned in [50]) and considering the mass of 0.4 km section of the line (the maximum span length for medium class poles) then the wire must be able to withstand (0.4*497+50) kg. The force produced by such a mass is around 2.4kN and is less than the calculated breaking load for the wire. So, in this case suspension of DSSC modules from the wire may not be problematic in terms of the calculated breaking load. Using another example of a standard aluminium alloy stranded conductor (with a cross sectional area of 30.10 mm^2 and an approximate mass of 82 kg/km) the calculated breaking load is 8.44 kN. By adding the weight of the DSSC device, the total load will be 82.8 kg which produces a force of 0.8 kN, still less than the breaking load of the conductor. However, as the cross sectional area of the wire becomes smaller the ratio of breaking load to the resultant load becomes smaller and care must be exercised when considering the implications of DSSC.

Cross sectional area	Mass per kilometer	Calculated breaking load	Total load with DSSC	Ratio of breaking load over the total load
30.10 mm^2	82 kg	8.44 kN	0.8 kN	10.55
47.84 mm^2	131 kg	13.4 kN	0.99 kN	13.26
59.87 mm^2	164 kg	16.80 kN	1.11 kN	18.73
180.7 mm^2	497 kg	50.65 kN	2.4 kN	21.10
211.0 mm^2	580 kg	59.10 kN	2.72 kN	21.73
362.1 mm^2	997 kg	101.5 kN	4.33 kN	23.44

Table D.1: Results for different standard aluminium alloy stranded conductors

Results for different standard aluminium alloy stranded conductors are presented in Table D.1.The results show that installing DSSC modules into distribution feeders is possible with the lowest ratio of breaking load to the total load in all cases being 10.55. However, the wires used on each feeder are different and even it can even be different with different parts of one feeder. For this reason, the characteristics of feeder in terms of the breaking load of the wires must be studied carefully before installing the DSSC modules.

D.2.3 Cross-arm

Cross-arms on top of the overhead line poles in distribution feeders are used to hold the line conductors and the related insulators. In terms of their mechanical design, the cross-arms must be able to support two different types of vertical and horizontal loads. Vertical loads include the weight of the wire and an extra load of about 225 lb [85], [114] which is the approximate weight of a line worker. The horizontal load is generated mainly by wind. Wire tension in most cases is negligible because the generated tensions from both sides of the cross-arm are equal. Generally, both vertical and horizontal loads depend on the characteristics of the conductor, the span, ice load and wind load. The vertical load can be calculated [114] as follows:

$$T_v = [W_w + 0.913 * \pi * il\,(il + dw)10^{-3}] \qquad \text{(D.1)}$$

In equation (D.1)$T_v$is the vertical load on the cross-arm (Fig. D.3), while *il* and *dw* represent the cross section of ice load and wire, respectively. W_w is the weight of wire and this will be increased by the additional weight of the DSSC modules. This will increase T_v for each cross-arm but the new load should not cause any immediate problems since the mass of the DSSC device (at less than 50 kg) [114] is less than the extra design weight margin representing the weight of a line worker. The many varieties of cross-arm designs as well as different quality of the materials used in their construction are key parameters that must be carefully considered before the inclusion of DSSC modules in distribution feeders. As discussed earlier they have some margins to with stand extra load but this cannot be generalized for all networks Because the weight margins can be different from one cross-arm design to another, it is recommended that each circuit should be investigated individually on a case by case basis in order to obtain a certain level of confidence, reliability and safety.

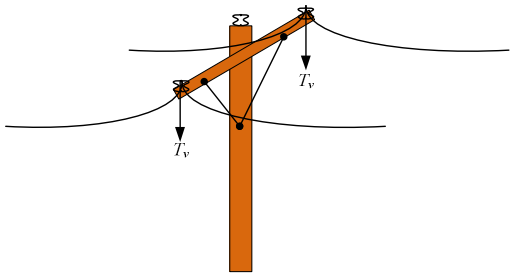


Fig.D.3: Vertical load on cross-arm

The horizontal load will be different for cross-arms which are located through the feeder from those which are at the begging or at the end of the feeder. For a cross-arm not

located at either ends of the line (Fig. D.4), the horizontal load is calculated [114] as follow:

$$T_{t_1} = (P_w * d * 10^{-3})S_w \quad (D.2)$$

whereT_{tl} (kg) is the horizontal force of wind and P_w(k/m^2) is the wind pressure. d represents the cross sectional diameter of the wire and S_w is the effective length of the span. The additional weight of a DSSC module does not affect any of these parameters. Therefore, no extra horizontal load is imposed by the suspension of the DSSC modules.

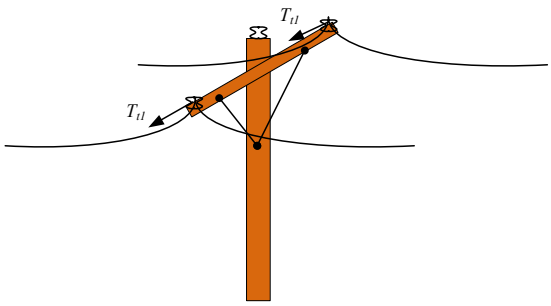


Fig.D.4: Horizontal load on cross-arm

However, at locations where there is a bend in the feeder an additional force due to the angle of the bend is added to the horizontal load of the cross-arm. In this case, the resultant force is the combination of wind force and the angle force and can be calculated [114] as follows:

$$T_{t_2} = 2H_{ten}\mathrm{Sin}\frac{\gamma}{2} + (P_w * d * 10^{-3}) * S_w \quad (D.3)$$

where$T_{t2}$is the resultant horizontal force and H_{ten} is horizontal tension in the line. In this equation, H can be affected by the weight of the DSSC modules. This may be mitigated by using supportive joints, etc. However, because of the distributed nature of DSSC, the connection of DSSC modules in such sensitive locations can simply be omitted.

A similar situation can be found at the beginning or at the end of the feeder. At these locations, the line tension on the two sides of the cross-arm is not equal. Normally, the line tension from the substation side is negligible and the total horizontal force is the combination of two orthogonal forces, one generated by the wind and the other generated by the line tension in the direction of the conductor. These forces are shown in Fig.D.5.

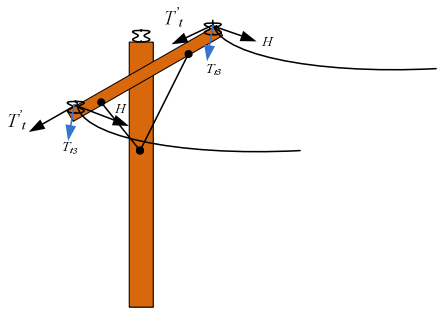


Fig.D.5: Horizontal loads at the corners

In this situation, the total load, T_{t3}, is calculated as follows:

$$T_{t3} = \sqrt{H_{ten}^2 + T_t'^2} \quad \text{(D.4)}$$

In this equation T_t' as discussed earlier cannot be affected by the weight of the DSSC device, however, H_{ten} must be considered [114]. If the inclusion of a DSSC module at the beginning or at the end of the feeder becomes necessary for any reason, then the cross-arm must be supported mechanically by a supportive structure.

Two other parameters must be considered in the cross-arm design process, the phase to phase distance and the phase to pole distance. The phase to pole distance is the minimum space between the closest wire to the pole or its connection and can be calculated [62] as follows:

$$L_{min} = 125 + 5 * (V - 8.7) \quad \text{(D.5)}$$

where L_{min} (mm) is the minimum distance between line and pole and V is the line voltage. For example, for an 11kV feeder this must be at least 136.5 mm, however other issues such as birds sitting on the wires or maintenance requirements mean that this distance is larger in practice. In equation (D.5) L_{min} is function of V only, and is not affected by the additional weight of the DSSC modules. So, it can be stated that series compensation of a line using DSSC will not change the minimum distance required between pole and line. The minimum distance between two phases PC (needed to make sure that they are electrically isolated) is calculated [114] as follows:

$$PC = K_e\sqrt{f_{max}} + L_I + \frac{V}{150} \quad \text{(D.6)}$$

where V is the line voltage and L_I represents the insulator string length. In this equation the maximum depth of span is represented by f_{max} and K_e is a parameter which is determined by type of wire, its material and cross sectional area. These parameters are not going to be affected by suspending the DSSC modules from the line. However, it is recommended that the modules are connected to the three conductors in different

locations between each two adjacent poles. The suggested configuration is shown in Fig.D.6.

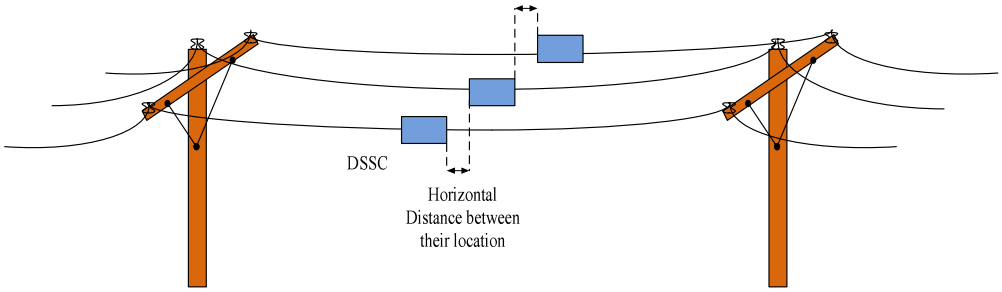


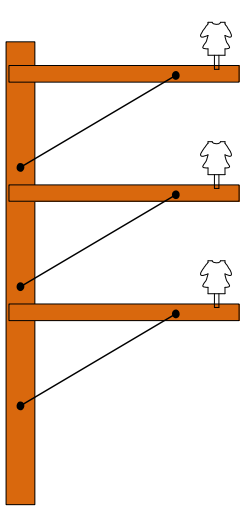
Fig.D.6: Connection of DSSC modules in different locations

The configuration and structure of the cross-arm is an important parameter in the distribution of mechanical loads. Different types of cross-arm are shown in Fig D.7 and their advantages/disadvantages given in Table D.2.The selection of a given cross-arm design depends on environmental conditions, the length of the span, depth of the span and the line voltage. Based on the type of their connection to the pole and the way they hold the wires, the cross-arm designs are given names like flag shape arm, double circuit arm, triangle shape arm, L shape arm, buck arm and double arms as shown in Fig.D.7.

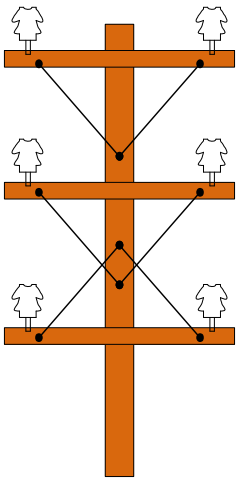
The materials with which the cross-arms are made and the way that insulators are connected to the arms may be different for different designs. For example, the insulator can be implemented on the arm or alternatively it can be suspended from the arm. Moreover, the arms can be made of wood, metal or composite material depending on environmental conditions and the mechanical loads that the arms needs to carry.

Nameof cross arm	Description
Flag shape	This cross-arm needs a small space and can be employed when there is a difficulty in providing enough safety margin in terms of electrical clearances. Long depths of span can be achieved with this design. As each individual wire has its own independent arm, the weight of each added DSSC module will rest on one arm. This will avoid having the weight of all three modules on one arm.
Double circuit	The cross-arm carries two sets of three phases and can be employed with long spans between poles. Normally it comes with pin insulators. However, adding two sets of three DSSC modules can present a heavy total load.
Triangle shape	This cross-arm uses three pin insulators to hold the wires which and are located at the three points of a triangle so that the phases are relatively close to each other. This limits the possible depth and length of span between two poles.
L shape	Using this cross-arm in the distribution feeders will limited the depth of the span between two poles. This design is used when there is a small space for electrical clearances.
Single arm	This design is employed in areas where there is heavy ice and pollution. As it needs a large space for the required electrical clearances, it is most commonly found in the countryside and in mountainous areas where the distance between the two poles are long. They are usually designed to withstand large mechanical loads, so the implementation of DSSC modules on this type of cross-arm will not be problematic.
Buck arm	Is used when two line cross each other. There will be two orthogonal loads vertically and horizontally and extra support wires may be needed in some cases.
Double arm	This is essentially the same as the single arm design, reinforced by another arm in parallel. The second arm is added to manage the high mechanical loads in heavily loaded feeders with big heavy wires.

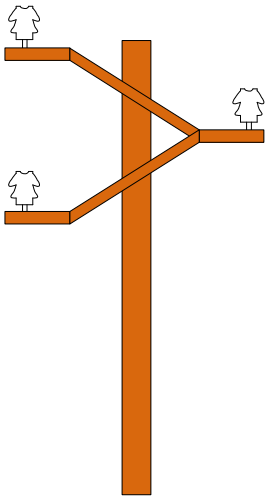
Table D.2: Different cross-arm designs



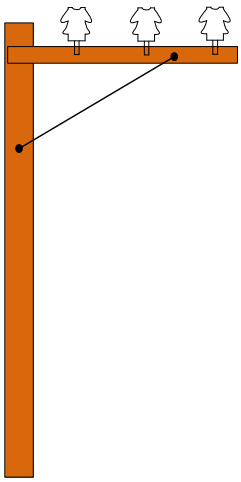
A) Flag Shape



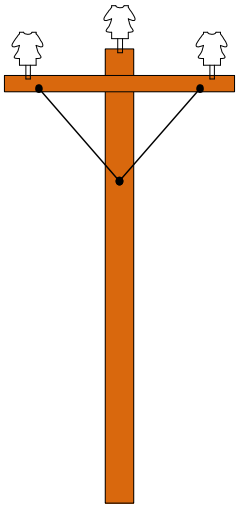
B) Double Circuit



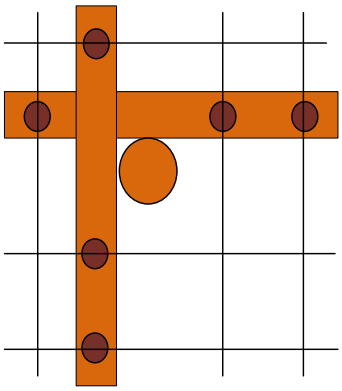
C) triangle



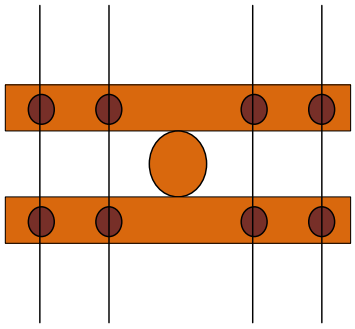
D) L Shape



E) Single Arm



F) Buck Arm



G) Double Arm

Fig.D.7: Different possible type of cross-arm in the distribution feeders

D.2.4 Poles

The pole is a major item of equipment in an overhead line distribution network. It holds the mechanical loads of the cross-arms and wires and other vertical loads due to wind, ice, and the resultant tension in the conductors. In most cases, the resultant wire tension generates only a vertical force in the direction of the pole itself (uplift or downlift) and the horizontal effects are negligible (horizontal tensions at either end cancel each other out). The vertical force acting on the pole is equal to the total weight multiplied by the length of span and can be expressed as:

$$F_v = w \times S_l \quad \text{(D.7)}$$

where F_v is the vertical force on to the pole, w is the total weight of the wires, ice, etc. and S_l is the length of span. It can be clearly observed from equation (D.7) that *w* will be increased by introducing the DSSC modules into the system. This force, F_v, is directed at the foundations of the pole and do not affect the pole itself.

Poles must also withstand another horizontal force generated by the wind. This force depends on the length of span the wind blows through and the strength of the wind and can be expressed as:

$$F_{WH} = S_w * (W_{mf} * \rho) \quad \text{(D.8)}$$

where F_{WH} is the horizontal force generated by the wind through the wire and directed to the pole, W_{mf} is the maximum wind force through one meter of the wire, S_w is the length of span which the wind blows through and ρ is a parameter defined by environmental parameters. Adding a DSSC module will not have any effect on the horizontal force because the parameters in equation (D.8) will remain unaffected. Based on equations (D.7) and (D.8) it can be concluded that if the mechanical load of the DSSC modules is balanced on both sides of the pole, there will not be any extra load on the poles themselves. For this reason it is recommended that the number of added DSSC devices must be equal on both sides of the pole.

Poles are made of different materials including concrete, wood and steel and their mechanical properties will differ in term of their load carrying capabilities. In distribution networks, and especially in 11kV networks, poles are mainly made of wood or concrete and metal poles are rarely used. For this reason, only wooden and concrete poles are considered in this study.

Concrete poles are made of reinforced concrete and they have some advantages that encourage utility companies to employ them widely in their networks. For example, they do not need any maintenance, are fire proof and do not decay for years and years.

They can be made in a variety of different sizes, heights and dimensions [114], [115] and this gives designers a lot of freedom in the planning stage. Table D.3 gives the maximum mechanical load for different lengths of some common, widely used concrete poles. The selection of the height of the pole and its' mechanical strength depends on environmental factors and the weight of the conductors.

Length of pole [m]	9	9	9	9	12	12	12	12	12	15	15	15	15
Maximum mechanical load [kgf]	200	400	600	800	200	400	600	800	1200	400	600	800	1200

Table D.3: Different design of concrete poles

In Table (D.3) maximum mechanical load is the load that the pole can withstand under normal conditions measured in kilogram force (1kgf being equal to the force generated by a mass of 1kg). Table D.4 gives the mass of different conductors and of the DSSC modules [116]-[118]. The conductors are called All Aluminium Alloy Conductors (AAAC) and widely employed through the 11kV distribution networks. They are made of copper and aluminium. Table 3.4 includes the calculated total weight of wire and a DSSC module through the span. In this calculation the length of span is assumed to be 0.4 km and the weight of one DSSC device to be 50 kg. Each wire includes one DSSC device and between two poles there are three devices suspended from the wires.

Code Name	Conductor Cross sectional area	Mass per kilometer	Calculated weight of span and DSSC (0.4 km)
Almond	30.10 mm2	82 kg	82.8 kg
Fir	47.84 mm2	131 kg	102.46 kg
Hazel	59.87 mm2	164 kg	114.88 kg
Ash	180.7 mm2	497 kg	248.4 kg
Elm	211.0 mm2	580 kg	281.52 kg
Upas	362.1 mm2	997 kg	448.15 kg

Table D.4: calculated weight of conductors and DSSC modules

Wooden poles are also employed widely in distribution networks, and especially in older, aging circuits. The wood poles decay with time is and this can reduce their strength, so they need to be maintained and kept in good condition. The strength of the poles throughout a feeder becomes more of a concern when the feeder is proposed to be compensated by DSSC and the poles must be checked and tested against rot and weakness. There are two commonly employed methods to check the strength of wooden poles.

One approach is to use the Sibert drill method in which the pole is drilled using a tiny drill, 1milimeter in dimension, at quite high speed of say 7000 rpm [85]. The sample will generate data which is then analysed to check for any signs of rot. Another method is to simply check the pole visually or by using the Mattson bore approach. Mattson bore approach is a kind of visual check however in this method a tool is screwed into the pole. This will provide some sample from inside the pole which can be checked and analysed visually. The collected data can then be analysed to check the condition of the pole.

Table D.5 shows different types of wood poles with their related fibre stress and circumference taper [119]. The fibre stress represents the average strength of the pole and along with the circumference defines the pole class. For example, Cedar western red an specie of wood pole comes in different class mentioned in Table D.6 [120].The length and load capacity of each pole class is given in Table D.6 [119]. The table shows that each pole has a limited load capacity which must not be exceeded under any circumstances. Then introduction of the DSSC modules must be carried out based on the values given in these Tables to avoid exceeding the permissible load capacity of the pole.

Species	Fiber Stress(Ib/in^2)	Circumference Taper (inch/ft)
Cedar, western red	6,000	0.38
Pine, ponderosa	6,000	0.29
Pine, jack	6,600	0.30
Pine, lodge pole	6,600	0.30
Pine, red	6,600	0.30
Cedar, yellow	7,400	0.20
Douglas-fir (interior north)	8,000	0.21
Douglas-fir, coast	8,000	0.21
larch, western	8,400	0.21
Southern Pine	8,000	0.25

Table D.5: Different type of wood pole with related fibre stress

Pole class	Horizontal load (lb)	Length range (ft)
H5	10,000	45-125
H4	8,700	40 -125
H3	7,500	40-125
H2	6,400	35-125
H1	5,400	35-125
1	4,500	35-125
2	3,700	20-125
3	3,000	20-90
4	2,400	20-70
5	1,900	20-50
6	1,500	20-45
7	1,200	20-35
8	740	20-30
9	370	20-25

Table D.6: Length and load capacity for different pole classes

D.3 Summery

This study, investigates main parameters of overhead line design in an distribution feeder which may be affected by suspending an external mechanical load from the power lines. For example, the effect of adding DSSC modules on the horizontal and vertical vibrations through the lines is studied. It is comprehended that the additional mechanical load represented by the DSSC modules can even help suppress Galloping (horizontal oscillations), but does not affect Aeolian (vertical vibrations).

Furthermore, braking load of some commonly used conductors (the most vulnerable part of the system to failure) in electrical distribution networks is also analysed. It has been concluded that the additional DSSC devices directly increase the tension in the conductor. Afterward, study recommends suspension of DSSC devices to be avoided where the feeder is crossing a river, road or where it has a very long span.

In general, it was concluded that compensating distribution lines using DSSC devices is a feasible proposition in terms of the mechanical load capacity of the feeder. However this statement cannot be generalized for all feeders and all networks. For this reason and before adding the modules through the line, the capability of the line must be carefully studied.