Newcastle University

Reduced DC-Link Capacitor Drives for More-Electric Aircraft Applications

Manas Khatre

A thesis submitted for the degree of
Doctor of Philosophy

September 2009

School of Electrical, Electronic
and Computer Engineering

Some text bound close to the spine.

ABSTRACT

As the race towards More Electric Aircraft continues in the aerospace industry, the demand is rising for reliable yet cheap flights. The increasingly power hungry aircraft system puts even greater pressure on designers to replicate the performance of conventional hydraulic aircraft systems by all electrical means. At present one of the heaviest and most size dominating components of aircraft electrical actuator drives is the dc-link capacitor.

Today the most advanced passenger aircraft such as the Airbus A-380 employ Fly-by-Wire techniques but still rely on electro-hydraulic actuators (EHA) for the critical primary control surface actuation. Non-hydraulic alternatives using electro-mechanical actuators are the subject of much current research for applications in primary control surface actuation but as yet are not able to meet their critical safety standards. The research work presented here follows previous work in the authors Research Group on secondary flight control surfaces in which fault tolerant drive arrangements were used to meet the required reliability figures mostly because of the lack of reliability of the dc-link capacitors. This research shows that much smaller dc-link capacitors are possible by modifying the control methods. Smaller capacitance requirements make much more reliable capacitor technology viable and hence may allow the required mean time between failures to be met from much simpler non-fault-tolerant conventional three phase drives.

A new drive with a switch estimation based control is proposed here with the potential to operate at much lower dc-link capacitor values. As part of the analysis a complete simulation of a three-phase 3.6 kW permanent-magnet synchronous machine (PMSM) with a PWM rectifier-inverter drive for a full electrically powered flap for a mid-sized aircraft like an Airbus A-320 is presented. The effect of the size of the capacitor is examined and ground rules to establish minimum acceptable size are derived exploiting the knowledge of the exact switching states in the rectifier and inverter. Measurements on an experimental rig are used to validate the simulation.

CONTENTS

LIST OF FIGURES

ACKNOLEDGEMENTS

Firstly I would like begin by thanking the ORS scholarship committee for partly funding my tuition fee without which I would not have started this study. I would also like to thank the Electrical Electronic and Computer Engineering Department's Scholarship Committee for Fund the rest of my tuition fee.

I feel extremely exhilarated to have completed this PhD thesis under the supervision of Professor Alan Jack. Professor Jack always helped and encouraged me from the initial funding up until the painstaking work of checking this thesis. In addition without Alan's recommendation and also the support given by Professor Satnam Dlay that helped secure the ORS award, this research would not have got off the ground. Thanks are due to Dave Atkinson for his timely review of my work and giving valuable suggestions for specific problems. I would like to thank Damian Giaouris for providing constructive feedback during the annual review of my work.

I acknowledge sincere thanks to all the technical staff in the department for their cooperation during my stay in the department lab. Specific thank goes to Jack Noble, Allan Wheatley and Stephen Mitchell for always agreeing to help on short notice. I am also thankful to my UG lab colleagues, Glynn A., Matthew A., Yutana C. and Zaid for sharing ideas and knowledge throughout the duration of study.

I owe immense debt to my wife Pushpita, without her love, support and sacrifice I would never have realized my full potential & my parents Ashok Khatre and Prabha Khatre with my brother Pawas for their unconditional love and encouragement. I wish to thank my uncle Pramod Soni and aunt Sangeeta Soni for treating me like their own son and caring for me through life. I am grateful to my friends Amit, Kartik, Dharmendra, Sanjay, Deepak and Shweta, who were always on my side whenever I needed them.

Finally I want to dedicate this work to my beloved grandfather Late.Shrikrishna Khatre and my uncle Late.A.K.Mukhopadhyay who both passed away during this time but are always my source of inspiration in life.

NOMENCLATURE

FBW	Fly-by-Wire
PBW	Power-by-wire
MEA	More Electric Aircraft
HA	Hydraulic Actuation
EMA	Electro-magnetic actuator
EHA	Electro-hydrostatic actuator
PDU	Power Drive Unit
MCU	Machine Control Unit
VF	Variable Frequency
VSI	Voltage source inverter
CSI	Current source inverter
TUHH	System Engineering of University of Hamburg
SRM	Switched Reluctance Motor
PM	Permanent Magnet
PMM	Permanent Magnet Motor
PMSM	Permanent magnet synchronous motor
FCU	Flight Control Unit
FCC	Flap Control Computer
PWM	Pulse Width Modulation
DSVPWM	Differential Space Vector Pulse Width Modulation
IGBT	Insulated-Gate Bipolar Transistor
EMI	Electro-magnetic interference
SVM	Space Vector Modulation
rpm	Revolution per minute
MC	Matrix Converter
TIMES	Totally Integrated More Electric System
THD	Total harmonic distortion
UPF	Unity power factor
PCB	Printed circuit board
C.F	Compensation factor

L-L	Line to Line
L-N	Line to Neutral
V	Voltage
A	Ampere
M	Motor
V_{ref}, V_R	Reference Voltage
V_c	Carrier voltage
A_c	Carrier wave amplitude
A_r	Reference wave amplitude
V_{out}	Output Voltage
V_{dc}	DC-link Voltage
D,d1,d2	Duty cycle
C	Capacitor/dc-link capacitor
P or W	Power
P_{mech}	Mechanical power
I_d, i_d	d-axis current
I_q, i_q	q-axis current
i_c	dc-link capacitor current
i_{rect}	Rectifier output current
i_{dc}	dc-link output current
i_o	Output current
V_d, v_d	d-axis voltage
V_q, v_q	q-axis voltage
L	Inductance
L_d, L_q	d-q axis inductances
L_s	Supply phase inductance
$\overline{SW}$	Switching Function

ω	Angular speed (ω_e -eletrical speed, ω_m -mechanical speed)
rect.	Rectifier
m/M	Modulation depth
T_e	Motor Torque
p	Motor pole pair
R	Resistor
ψ	Field flux linkage
ψ_m	Magnet flux
emf	Electromagnetic field
E	Back E.M.F
θ_e	Electrical Angle
V_α, V_β	Clark transformation voltages
J	Motor inertia
$V_1 ... V_8$	Voltage vectors
k_t	Torque constant
T,t	Time duration
Sr,Sy,Sb	Switching logic
*	Used as superscript for demand values
ref	Used as subscript for reference values

Note: Wherever possible the meaning of each symbol/abbreviation is given in this thesis when it is first used.

CHAPTER 1

INTRODUCTION

It is clear that there have been huge changes in air transport since the Wright brother's first flight in 1903 (Fig.1). However all of the major technologies of modern passenger jets were already in use in the 1930's – gas turbine engines, stressed skin construction and flight surfaces using sweep to approach as near as possible the speed of sound. It took another 20 years for these technologies to reach commercial aircraft but arguably since the De Havilland Comet first flew in 1949 there has been nothing essentially new in type of transport aircraft if the short-lived and arguably non-commercial supersonic Concord programme is not considered. The huge increase in drag associated with supersonic flight coupled to the difficulties associated with the opposing design goals of combining both low and high speed flight means that most attention continues to be given to improving subsonic transports. In this area large advances have been made in the efficiency of engines using larger and larger fans to provide thrust and having only a small proportion of the engine intake air passing through the turbine. In addition the thrust available from the largest engines has risen sharply and engine efficiency has also improved and this has allowed bigger and bigger aeroplanes and lower and lower seat per mile costs. The result is that new designs offer lower overall costs than keeping older airframes which has thereby stimulated onward development. The trend is clearly shown in the Boeing 737 which first flew in 1967 using low bypass ratio engines (i.e. most air goes through the turbine). To a casual observer it appears just like the Airbus A380 excepting that this aeroplane which first flew in 2005 is very much larger and has a large number of less obvious differences. The 737 has been extensively modified in an attempt to keep it competitive receiving newer more efficient high bypass ratio engines on two occasions and having a new wing with increased span and added wingtip aerodynamic features. The result is large numbers of first generation 737's being retired before their fatigue life was reached. The last three decades of technological advancements in the field of aerospace engineering have therefore mostly concentrated on economic issues rather than simply trying to fly faster.

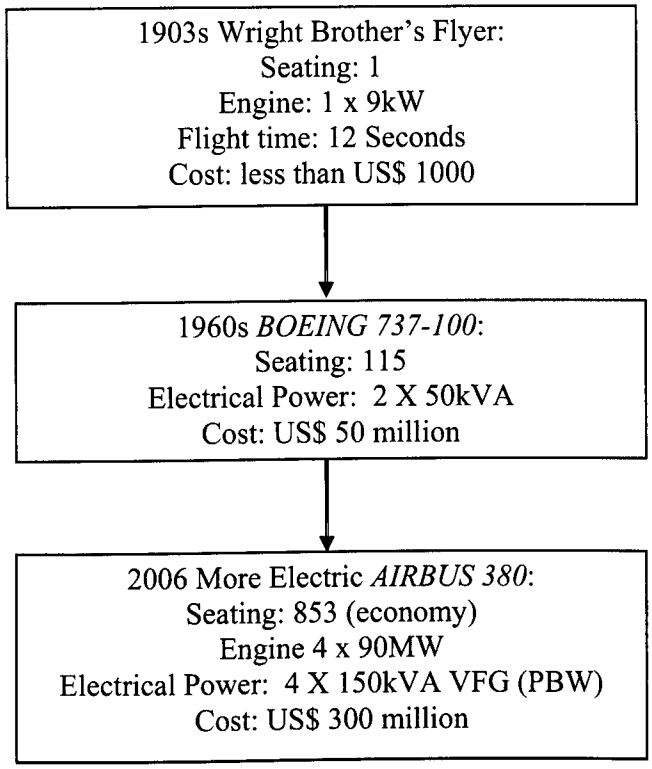


Fig.1. Development in air transportation in last ten decades.

Whilst improving engines, bigger aeroplanes and better aerodynamics are the foreground of development, lighter, more reliable and more controllable systems can also markedly improve seat per mile costs. Recently a good deal of attention has been paid to the possible advantages of using electrical systems to replace hydraulic systems for surface and undercarriage actuation and engine-bleed-air systems for cabin pressurization/temperature control and deicing. The A380 shows partial implementation of this trend with electro-hydraulic actuation backing up hydraulics for aileron and elevator actuators, electric motors backing hydraulic motors for slat movements and backup electro-hydraulic actuators for rudder and some spoiler actuation. In other words the trend is now for a ''More Electric Aircraft'' (MEA) which increasingly replaces the conventional ways of powering and controlling the aircraft systems. The use of electric systems has the potential to significantly reduce the complexity, weight and cost of flying and maintaining an aircraft. The use of electrical power for aircraft actuation is not new and has been around since well before World War II but the high power and force density coupled with the natural fault tolerance offered by hydraulics is far from easy to compete with and competitive electrical solutions are pushing the state of the art. The scope of this thesis only includes the actuator drives which are required to control the high lift

aircraft surfaces. To achieve efficient power transfer from the aircraft engine to the control surface, a distributed electrical approach has proved a successful in recent aircraft like the A380 where the actuator drive is placed close to the control surface. This type of drive configuration now imposes stringent safety requirements resulting in the need for fault tolerance and redundancy but they also demand very high reliability to force down flight dispatch failures and their concomitant costs.

The research work presented in this thesis focuses particularly on reducing the complexity of the actuator drive by proposing a new drive configuration which allows reduced dc-link capacitor size. Literature studies discussed in following chapters suggest that that the dc-link capacitor is one of the weakest links in terms of reliability and it is both bulky and heavy. If its capacity can be reduced a more reliable capacitor technology can be used. In the prototype flap drive developed in University of Newcastle Upon Tyne which forms the background to this project, the fault tolerance in the drive was introduced with the primary aim of improving system reliability to meet flight dispatch requirements i.e. a safety aim. In this prototype flap drive, the power-off brakes were employed to give the failsafe feature of the flap system rather than any redundancy in the drive. Figures for the reliability of a smaller and thereby better technology for the dc-link capacitor suggest that fault tolerance in the drive is no longer necessary which further reduces the size and complexity of the converter.

In a more general non-aerospace context a reduced dc-link capacitance makes for reduced costs provided the extra complexity of the drive does not more than compensate.

1.1 Aims and Objectives

The main aim of this thesis is to contribute knowledge in the area of reduced dc-link capacitor size in drives for use in high reliability applications. The aims and objectives of this research are:-

- To understand the basic actuator technology for aircraft control surface actuation.
- To understand the detailed function of the various building blocks of control surface actuator drives.
- To establish the factors affecting the size of control surface actuator drives.
- To study previous research work related to dc-link capacitor size reduction.

- Propose a new drive structure and control method to achieve reduced dc-link capacitance in the aircraft actuator drive to achieve cost and size savings.
- To create a full simulation of an existing permanent magnet machine drive using MatLab and verify the results using experimental data.
- To study in the dc-link size affecting parameters such as supply phase inductance etc.
- Design and simulate the new control method to demonstrate that dc-link capacitor reduction is possible.

1.2 Thesis Overview

The work presented in this thesis is split into three parts: background information, the development of an adequate simulation and its experimental verification and finally the new control structure and its simulation. The first part (Chapter 1 and Chapter 2) aims to provide a detailed background behind this research. The study of previous research establishes the need for a new control method for actuator drives to achieve weight and cost savings. The literature review provides a background for the various building blocks of an actuator drive.

The second part deals with developing a drive simulation that is able to explore the issues associated with the dc-link capacitance size (Chapter 3) and validating the simulation using measured results from an existing (conventional) dc-link drive (Chapter 4).

The third part deals with an investigation of the parameters affecting the dc-link capacitor size and from this a new control structure is developed (Chapter 5) exploiting the advantages of using a fully switched rectifier converter. It is demonstrated via simulation that very low dc-link capacitor size is necessary and it is argued viable using the proposed converter structure and control. Finally the limitations of the proposed method are examined and from this recommendations are made for future work and conclusions drawn (Chapter 6).

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In the area of aircraft actuation systems, the design and particularly the drive system are currently being intensively researched. Conventional actuation of control surfaces in aircraft is based on a direct hydraulic link with the aircraft control system. The recent advances in power electronics offers new systems that are replacing these hydraulic links with electrical ones. This means it is now possible to generate signals from the cockpit that will go directly into a computer controlled electrical drive whose output supplies the actuator that moves the aircraft control surface. The current flight control actuation system can be considered to involve two main technological areas: Fly-by-Wire (FBW) and Power-by-Wire (PBW) *[1]*.

FBW technology deals with the electronics involved in the flight control system. There is a properly designed architecture (centralised or distributed) which is designed to meet fault tolerance and load requirements. A distributed control architecture offers great advantages like pilot workload reduction, alternate means of supply for the actuators and reductions in weight.

On the other hand PBW technology deals with the load itself, which means the design and development of actuators for flight control surfaces. PBW includes modifications and design of new motors and their drives that are capable of controlling the flight control surfaces with high standards of reliability & safety. This research concentrates on the PBW technology which includes the actuator configurations, electric motors and high precision electronic drives.

This section of the thesis aims to provide background information about the aircraft actuation technology and the selection of the various building blocks of a control surface actuator drive. Further into chapter two possible alternatives to actuator drive are discussed

and a possible drive configuration is proposed which has a smaller dc-link capacitor. This chapter also provides some analysis of previous research carried out towards reducing dc-link capacitance.

2.2 Selection of Drive for Control Surface Actuation

2.2.1 Actuators for Drive

Control surfaces in aircraft allow the pilot to control and adjust the altitude of the aircraft. Early aircraft had fixed wings, but once in air the aircraft was uncontrollable. The development of control surfaces in aircraft allowed controlled and stable flight. Each control surface require separate and precise control in timely fashion, so the actuators need to be very reliable and should be able to produce sufficient torque to move the control surfaces under all flight conditions. The main control surfaces of a fixed wing aircraft are shown in Fig.2.1.

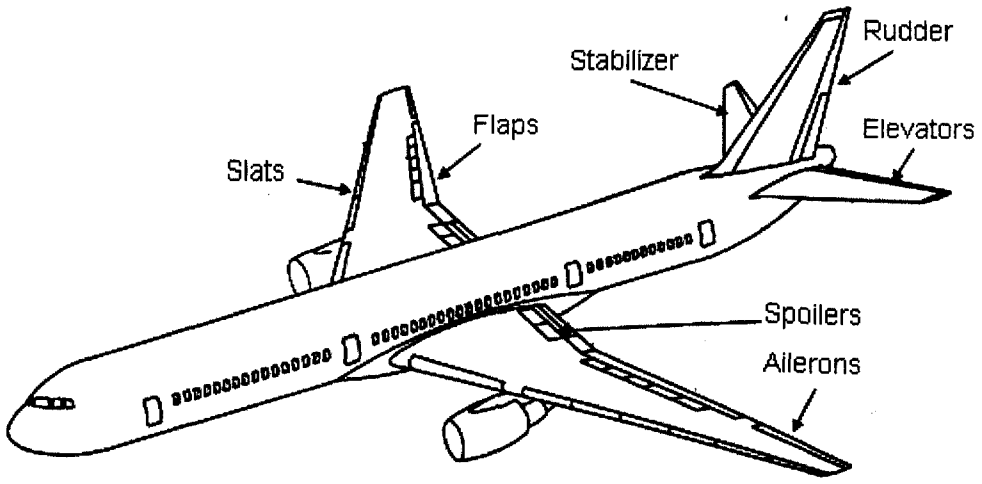


Fig.2.1. Aircraft control surfaces

The performance requirements (such as accurate synchronization) of these control surface actuators require very accurate drive system behind them. Unlike conventional actuation techniques, the "More Electric Actuation" will have less (or no) hydraulic motor or actuator embedded in the actuator itself, to drive the control surfaces of aircraft. The actuators can be categorised (depending on the link with the load) as:-

[A] Hydraulic Actuator [HA] – Hydraulics naturally have high power per unit weight and very high torque or force per unit weight and can hold very large static loads with no power consumption. In addition the control input can be at very low power levels. These attributes make them natural choice for flight surface control. Centralised and independent hydraulic systems deliver high pressure to the hydraulic actuator local to flight surface under control *[2]*.

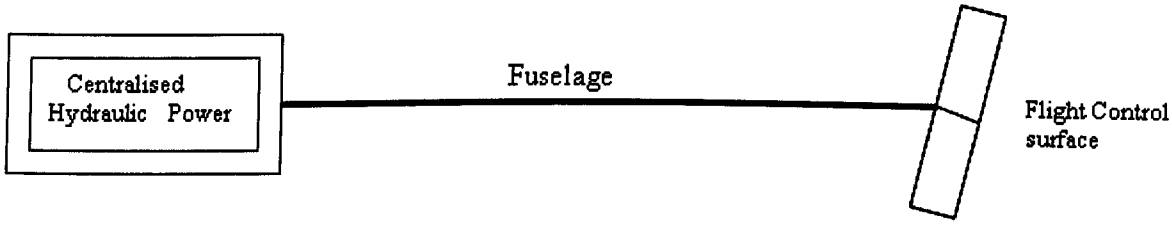


Fig.2.2. Basic HA operation.

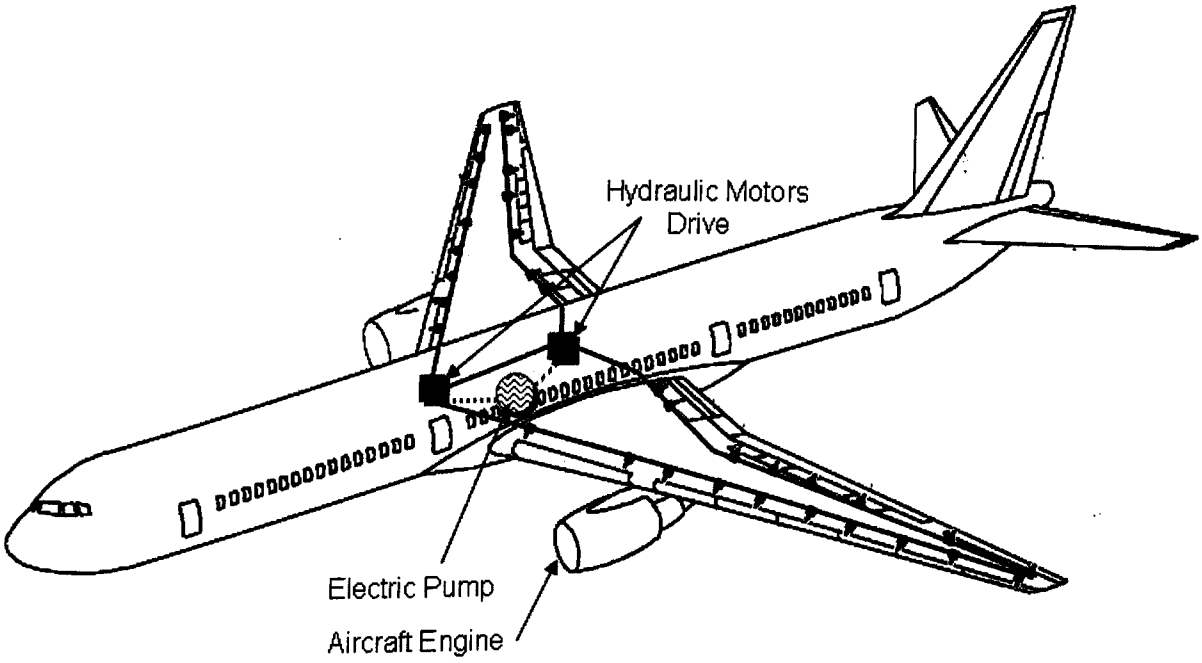


Fig.2.3. Conventional Hydraulic Actuation

As shown in Fig.2.3, the high lift system of civil aircraft generally uses a hydraulic motor drive and single drive shaft across both wings to control the flaps/slats. The other advantages of HA includes easy active-standby or active-active configurations of the actuator and less sensitivity to load fluctuations. If a failure of a high lift surface is detected then all the surfaces are locked into the position of the failed surface to avoid uncontrolled movement of the surfaces. In the case of primary flight controls they cannot be locked and the typical arrangement is to have dual actuators either of which can control the surface in the event if the

surface failed to lock. The problem with HA is that it is prone to fire and corrosion as the fluid continuously travel through pipe work to reach the flight surface under control. There are also problems of complicated and extensive mechanical linkage, disconnection from the aircraft hydraulic supply and fluid bleeding during maintenance and reinstallation *[1]*. However the biggest disadvantages of this type of actuation are the heavy hydraulic plant and the very low power density transmission across the aircraft. The rapid development of control and power electronics means control with high safety is possible and more electrical means of control leads to research into the electromagnetic actuators (EMA) and electric/hydraulic actuators (EHA).

[B] Electromechanical Actuator (EMA) – An EMA is the result of completely removing all hydraulics from the HA actuation system. As the name suggest the coupling provided between flight control surface and the driving motor is purely ''mechanical'', which is achieved for instance by means of a gearbox/ball screw system as shown in Fig. 2.4.

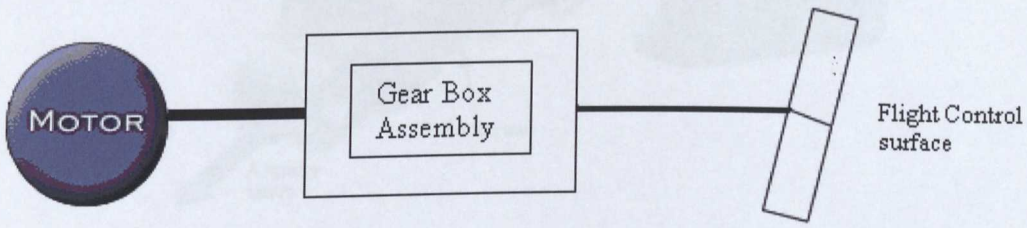


Fig.2.4. Basic EMA operation

Centralised electrical power can be distributed to electric motors driving actuators via different gearing combinations. Motor speed, direction and torque are translated directly into speed, direction and load in the actuator. The mechanical coupling makes this type of actuator more susceptible to mechanical jamming and more wear. The above problems associated with EMA can be avoided to some extent by additional devices and arrangements (like second drives or redundant phases) which add complexity, cost and most importantly weight to the overall system. In addition electric drives struggle to compete with hydraulic systems on force per unit weight (especially in holding long term large static forces). This is the reason why (so far at least) EMA are not suited for Primary Flight control surfaces (Aileron, Rudder, and Elevator) which require fast and precise dynamic response to command input. However secondary flight control surfaces (flaps, slats and spoilers) which require relatively slow dynamic response to command input and have a low duty cycle during a flight) can more easily accommodate EMA. The most effective way of reducing the weight of an EMA is to increase the speed of the motor which in turn means higher ratio gearboxes. In addition

converter weight and size is important and in this case the static energy storage components (i.e. capacitors and inductors) are the dominant components and research into reducing their size is important. It is also more difficult to lock a failed EMA and that leads to geometries which naturally lock or the requirement of the increased use of power-off brakes. These developments in EMA are starting to lead to proposals for primary flight controls as for instance in Fig. 2.5.

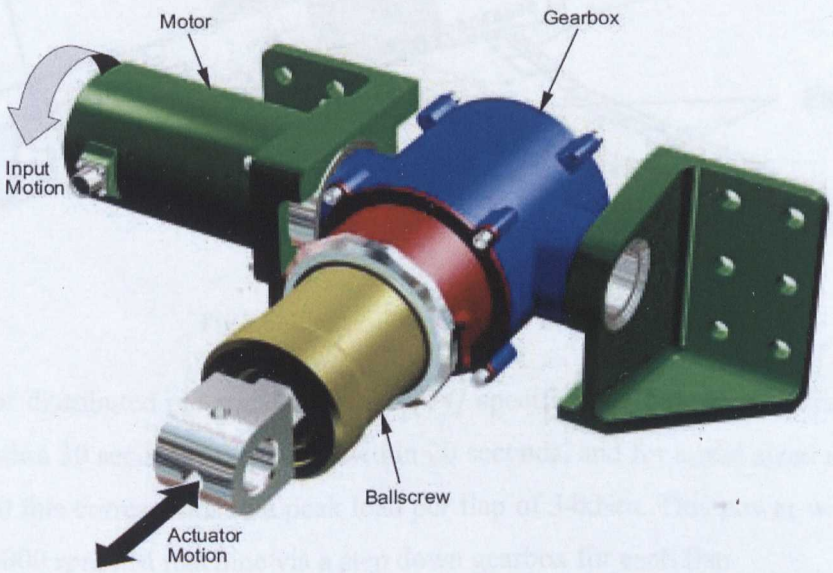


Fig.2.5 Large EMA for High-Power Flight Controls *[1]*

As discussed previously in conventional hydraulic actuation, in the case of a failed actuator it is locked in position. Bennet et al in *[13]* came up with a replacement of an HA which utilised localized electrical actuation of individual secondary control surfaces using an EMA and power-off brakes as shown in Fig. 2.6.

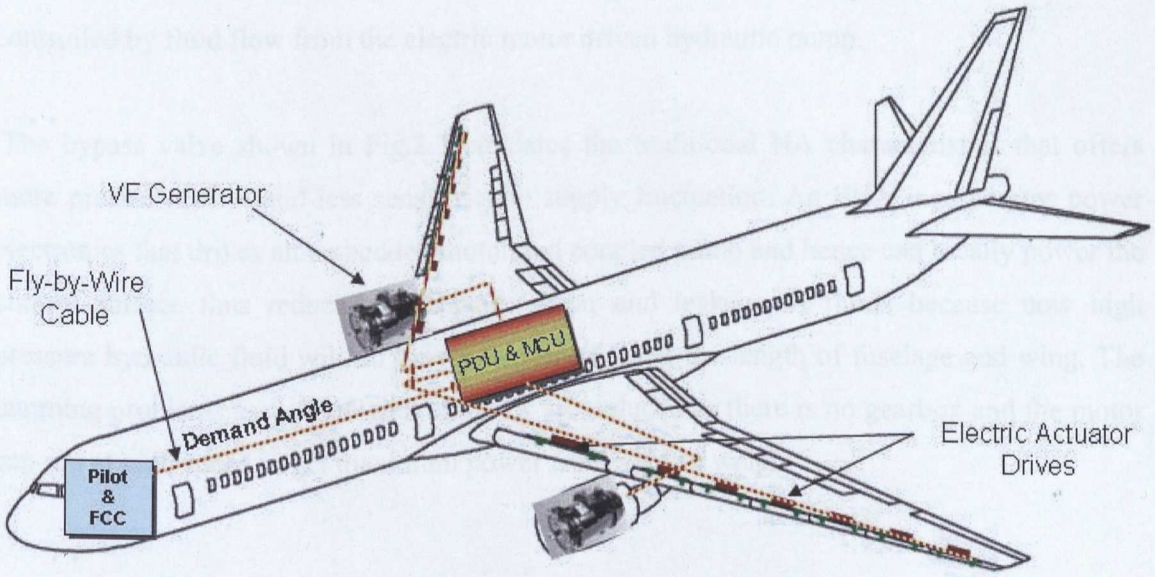


Fig.2.6. Electrical Actuation of Control Surfaces

This type of distributed electrical actuation *[14]* specification requires the flaps to be fully extended within 30 seconds and retract within 20 seconds, and for a mid sized aircraft like an Airbus A320 this corresponds to a peak load per flap of 34kNm. This power was supplied by a 3.5kW 10,000 rpm PM machine via a step down gearbox for each flap.

EMA technology eliminates the hydraulics and many of its disadvantages but it introduces a problem that is similar to a hydraulic actuator, HA's are prone to corrosion and leakage in the fluid route but on the other hand EMA's have gearing systems that are prone to gearbox failures. A more distributed arrangement of actuators helps to reduce the impact of failures. This type of EMA is being heavily researched but as yet not all actuation is viable using EMA's and hence that leads to locally electrically powered hydraulic actuation or EHA but this time the hydraulic system is miniaturised and the motor/pump is embedded locally.

[C] Electro-Hydrostatic Actuator (EHA) – The first breakthrough for use of an EHA for commercial aircraft control surfaces was made by the Airbus 380 aircraft. EHA's solve most of the problems associated with EMA's and HA's whilst still offering the characteristics of a traditional HA and therefore require minimum change in system identification. An EHA uses a motor to rotate a fixed displacement hydraulic pump which eventually moves the hydraulic piston jack and thus the aircraft surface under control.

The motor can be made bidirectional for changes in direction. Speed and direction are controlled by fluid flow from the electric motor driven hydraulic pump.

The bypass valve shown in Fig.2.7 emulates the traditional HA characteristics that offers more precise control and less sensitivity to supply fluctuation. An EHA incorporates power electronics that drives an embedded motor and coupled pump and hence can locally power the control surface thus reduce maintenance, wear and leakage of fluids because now high pressure hydraulic fluid will no longer be routed along the length of fuselage and wing. The jamming problems associated with an EMA are reduced as there is no gearbox and the motor can run at high speed to get maximum power from a given weight

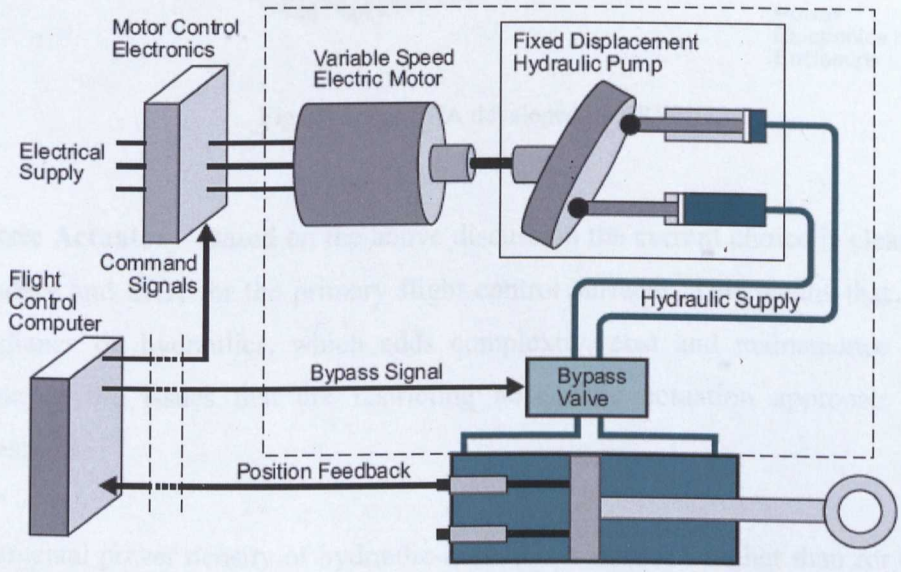


Fig.2.7. Basic EHA Control. *[1]*

Some advantages of EHA compared to EMA and HA can be summarised as:-

- Removes the requirement of a centralised pump.
- Fluid also provides cooling.
- Low power consumption during standby operation.*[1]*
- Less sensitive to power fluctuation.
- AC as well as DC compatible.
- Faster time response.

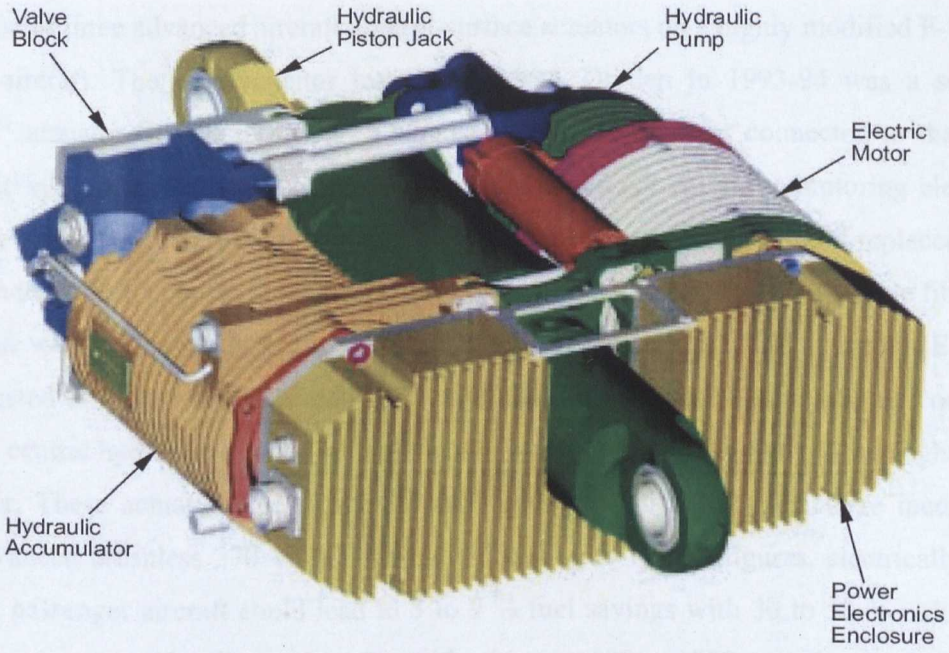


Fig.2.8 Large EHA developed by TRW. *[1]*

[D] All Electric Actuator – Based on the above discussion the current choice is clear: EMA for the secondary and EHA for the primary flight control surfaces. This means that there is still some reliance on hydraulics, which adds complexity, cost and maintenance for the aircraft. Some of the issues that are restricting all-electric actuation approach can be summarised as:-

- Fundamental power density of hydraulic-motors can be much higher than for electro-magnetic motors *[2]*.
- All-Electric approach could be more sensitive to power surges than the hydraulic approach of actuation.
- Compared to an equivalent hydraulic approach of actuation, the All-Electric configuration would generate considerably more localized heat. There could be a possibility of heat dissipation in airframes but it wouldn't be a safer option. Heat dissipation could also be achieved by forced air but the aerodynamic penalty and installation complexity would restrict its use and so the electric actuator has to rely on natural convection within the local environment for cooling *[1]*.

Researchers at NASA's Dryden Flight Research Centre recently concluded the flight validation of three advanced aircraft control-surface actuators on a highly modified F-18 Hornet aircraft. The first actuator tested by NASA Dryden in 1993-94 was a so called ''Smart'' actuator. It was by-design a standard hydraulic actuator connected to the central hydraulic system and was supplied with a self contained control and monitoring electronics unit. The benefit of these Smart actuators over a traditional system was that it replaced a large wire bundle (which connects the flight control computer to actuator) with a simple fibre-optic cable pair which allows significant weight savings. The second and third actuators (EMA and EHA) tested in 1998 were fully power-by-wire devices that means there was no connection with the central hydraulic system and commands were electronic direct from the flight control computer. These actuators use similar control and electronics units and were incorporated with advanced brushless 270 V DC motors. According to NASA figures, electrically driven actuated passenger aircraft could lead to 5 to 9 % fuel savings with 30 to 50 % reduction in ground equipment and military aircraft could achieve a 600 to 1000 pound reduction in take-off weight *[3]*.

Based on the above discussion the possible all electric actuator design for any flight control surface without any hydraulics might require a much more complex drive and control. One possibility could be a modified EMA which could serve the purpose of an All-Electric actuator for primary flight control. Possible modifications could be in the gear assembly or in the EMA design itself. Researchers at the Institute of Aircraft System Engineering, University of Hamburg (TUHH) Germany came up with an idea of hybrid actuation that is to use an EMA for flight critical control surfaces along with an EHA which is used for load application. The test rig employing an EMA for primary flight control under research in TUHH is shown in Fig.2.9.

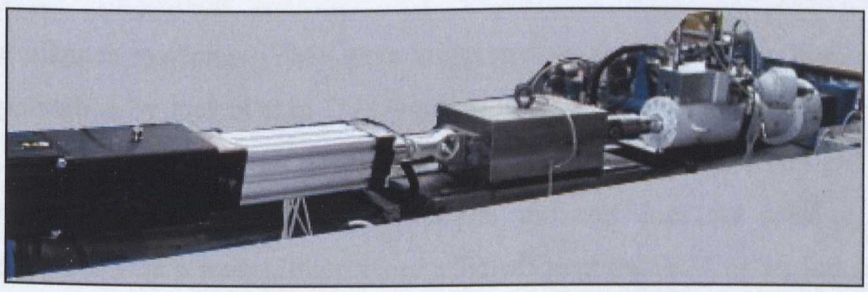


Fig.2.9. EMA test rig at TUHH Germany.*[Ref:TUHH]*

Key possible advantages of All Electric actuation can be summarised as:-

- Lesser maintenance of aircraft.
- Quick and easy fault diagnosis.
- Easy re-configuration and modification.
- Improved flight safety.
- Weight and cost savings (especially those accruing from weight reduction).

2.2.2 Motor Selection for the Drive

Considering the merits and demerits of different types of machines which might be suitable for high performance aerospace applications, there are three obvious contenders induction motors, switched reluctance motors and permanent magnet motors. Induction motor as an option was explored by *[15]* aiming for a fault tolerant machine. The induction machines require extensive magnetic coupling between phases to produce a rotating field and in addition they produce high rotor losses at low speed which makes them a poor choice for fault tolerant applications. The choice of motor for an actuator drive is always driven by the requirements of fast response and tight positional control and a very accurate control is required especially at low speed to track position. In this respect brushless DC motors offer better performance than switched reluctance motors (SRM) *[5]*. On the other hand the inherent fault tolerance characteristics of the SRM also make them a tempting choice for high-performance aerospace applications *[6]-[10]*. Since actuator applications require full torque production at all rotor positions and one phase of an SRM can only contribute to one half of a cycle or less, this prevents the SRM being the best choice unless it has large number of phases otherwise failure of one phase will produce regions with far less than full torque.

Permanent magnet machines (PM) were suggested as the option for high-performance aerospace application by Jack et al in *[11]* with a similar degree of fault tolerance to an SRM. Their high torque density makes them an ideal solution to achieve weight savings in aerospace applications. Also in PM machines the armature does not need to supply any magnetizing current which makes them more efficient than an SRM or an Induction motor. The introduction of fault tolerance into a PM machine causes a small reduction in the torque capability but the intelligent modular design of the machine can achieve the best of both

issues. The modular design of the PM machine requires minimal electric, magnetic and thermal interaction between phases of the drive which are naturally present in an SRM *[6][9] [12]*. The comparison between PM and SRM given by Jack et al in *[12]* predicts that the PM machine was able to produce 29% more torque than the equivalent SRM for the same temperature rise. Based on the above discussion PM motors are chosen in this research as the actuator motor for simulation as well as for experimentation purposes. Further attention is restricted to drives for high lift surfaces (flaps and slats) as these drives are already viable using EMA's.

2.2.3 Drive Topologies

The choice of drive topologies for high lift aircraft actuator drives is heavily affected by the requirement of drive fault tolerance and reliability factors. The flap actuator drive must be able to meet reliability requirements of less than 10^{-9} failures per hour which corresponds to a mean time between failures of over 100,000 years. This requirement is beyond what any standard electrical actuation system can achieve on its own. Use of power-off brakes which operate in case of a failure and lock the actuation system reduces the reliability requirements to 10^{-5} failures per hour which in fact mostly relates to the economics of not be able to dispatch aircraft.

A conventional electrical drive still cannot meet these reliability requirements *[17][18]*, hence fault tolerance and redundancy has been used by *[16]* in the motor and drive to allow the system to operate with a single fault. To achieve fault tolerance, a drive must be able to produce full torque at all rotor positions when a fault has occurred in either the motor or the power electronics controller. The above requirement was achieved in *[16]* using a modular approach for the drive. Each module was comprised of a single phase winding and was driven from a voltage fed inverter. Although the phases of the machine were contained within a single housing, each phase was thermally, magnetically, mechanically and electrically isolated from the other modules. Each module could be driven either by a single phase bridge or a set of three phases supplied from a 3-phase bridge. Finally in *[13]* the authors came up with the conclusion that the best combination of component count, converter size and machine size occurs with either 2+1 or 4+1 phases, each supplied from a single phase bridge (where for

instance 2+1 means that 2 phases are enough to meet the drives output requirements). For the drive construction and research purposes, Bennet et. al *[16]* used a three-phase modular system because it gives a good compromise between the level of redundancy and drive complexity. The drive schematic for the above work is shown in Fig.2.10.

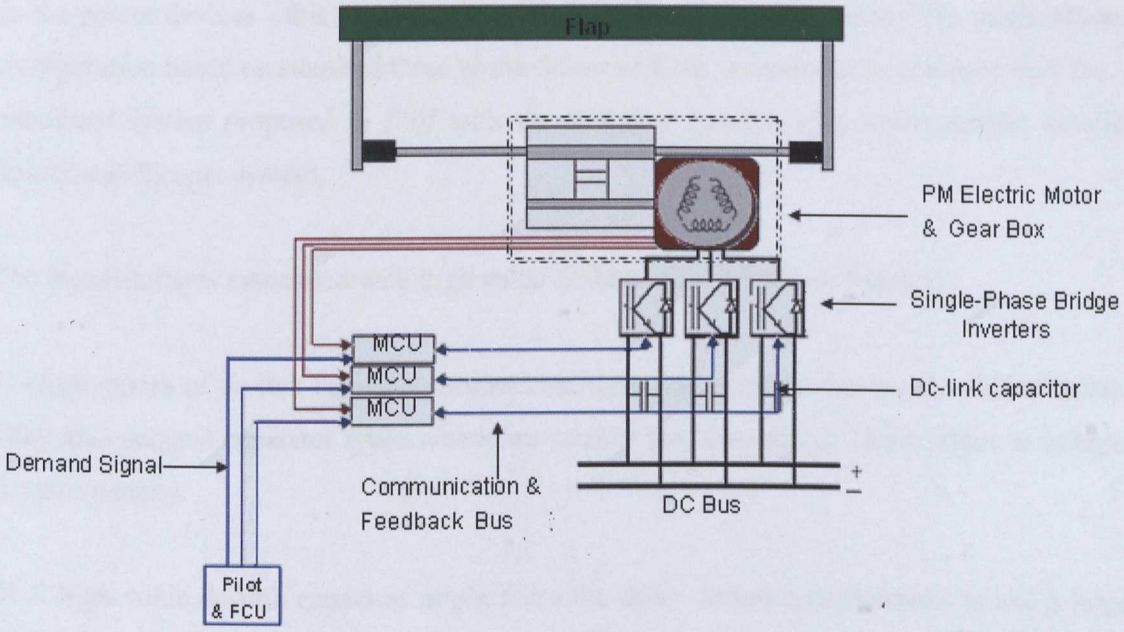


Fig.2.10 Modular drive for full electric actuator flap drive *[16]*

A single electrical drive is used to move each flap. To deliver the high load torque at low speeds a highly geared system is coupled to the motor. A 10000 rpm 3.4Nm electric motor was connected to a 10000:1 step down gearbox supplying 34kNm to the flap. Each motor phase was driven by a completely isolated electric drive which interacts with each other through a machine control unit (MCU) and then to a flap control computer (FCC). The dc-link capacitor used in each of the inverter bridge was 950 μ F. Using this type of triplex control architecture arrangement the failure is proved to be below 10^{-5} per hour (even without using the fault tolerance of the drive) corresponding to a mean time between failures of 11 years when coupled to power-off breaks this meets the system requirement of 10^{-9} per hour. The power –off brakes utilizes a jaw type clutch coupled to an electrical solenoid through a ball spline mechanism to prevent asymmetry between individual surfaces *[58]*. Power-off brakes are also sometimes referred as wing tip brakes or no-back brakes which provide braking with the solenoid de-energized and allow free rotation with solenoid energized. This mechanism is fail safe, if the power is lost the brake will lock the flap transmission.

In *[16]* the drive was configured to be fault tolerant in order to achieve required flight dispatch specifications. The flight dispatch figures are related to economics rather than safety. As the dc-link capacitors are the least reliable component of the drive, it can be argued that the required reliability to meet flight dispatch can be achieved if the dc-link capacitor can be replaced by a high reliability small dc-link capacitor and by close control of operating stress on the power devices - this is the key aim of this research. In other words this might allow a configuration based on standard three phase drives without redundancy to compete with the redundant system proposed in *[16]* with the attendant benefits of a much simpler smaller, lighter and cheaper system.

The disadvantages associated with high value dc-link capacitor are as follows:

1) High values of dc-link capacitor demand multiple capacitors increasing the risk of failure. They also suggest capacitor types which are smaller but have higher failure rates to mitigate the size penalty.

2) A high value dc-link capacitor might force the drive design specifications to use a larger inductor in conjunction with such a capacitor to avoid high current flowing into the inverter causing weight increase and poor power factor.

3) A large dc-link capacitor needs a high power rating rectifier to push the high levels of currents to charge the capacitors. Such a drive capacity is only required during the starting period and is unnecessary during normal times.

4) After the power is switched off, it is required to discharge the dc-link capacitors the higher the value of capacitor the bigger this problem is.

5) The dc-link capacitors significantly dominate the overall size (and hence weight) of the drive.

Although the six pulse diode converter would be more reliable than the fully switched converter (because of more devices in fully switched converter), a smaller (and more reliable) dc-link capacitor with fully switched converter (with better voltage control) could allow the drive to achieve higher reliability figures, reduce size, weight and cost and yet meet flight

dispatch specification as per the system shown in Fig.2.11. The front end converter could be either a three-phase diode rectifier or a fully switched IGBT converter. With a diode rectifier the problems associated with a six times supply frequency dc-link voltage ripple, increased power losses and EMI interference are all present therefore a fully switched PWM IGBT rectifier is a clear choice also giving a higher input power factor and a regenerative capability. The PWM rectifier produces a low dc-link ripple and responds rapidly to reversal of power flow and thus allows low energy storage components in the dc-link.

The following advantages are related to the selection of a voltage source inverter (VSI) drive configuration as compared to a current sourced inverter (CSI).

1) A VSI configuration offers lower reactive component size weight and cost because of less interactive with load. The filter component values depend only on switching strategy used.
2) Unlike CSI which exhibit inherent four-quadrant operation, VSI can offer alternative control and lower harmonics in the input and output currents.
3) Unlike CSI, VSI can easily operate at no load.

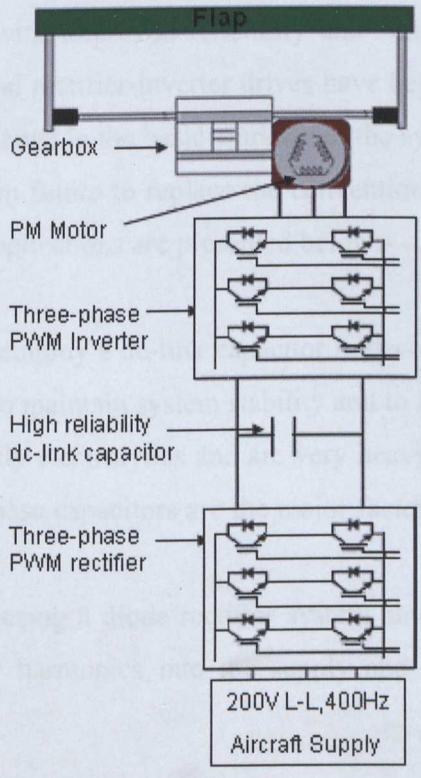


Fig.2.11 Proposed three-phase all electrical flap actuator drive with small dc-link

Considering the high-lift actuator drive requirements and actuator motor specification of *[16]* the proposed drive system specification can now be summarised as:-

Table-2

Flap load requirement	34kNm
Gearbox:	10000:1
PM motor	10000 rpm, 3.4Nm, 3.6kW, 5 pole pair
Inverter	Three-phase 20 kHz PWM/SVM Vector control, IGBT
Rectifier	Three-phase 12 kHz PWM/SVM UPF control, IGBT
Aircraft power supply	200V L-L, 400Hz Three-phase AC

2.2.4 Matrix Converter Drives

This section aims to give a basic understanding of Matrix converter technology and will discuss the advantages and constraints related to its use. So far dc-link single phase and three phase inverter systems to supply the actuator PM motor have been examined, now alternatives to replace the conventional dc-link inverter system in the aircraft actuator drive so as to minimise weight and cost with improved reliability and simplicity need to be considered. Since the 1970's conventional rectifier-inverter drives have become the de facto standard and there has been hardly any change in the basic working of the system. Some of the key reasons why there might be a need in future to replace the conventional drive arrangement specially for military and aerospace applications are presented below:-

- Conventional drives employ a dc-link capacitor to decouple the switching of the input and output systems, to maintain system stability and to filter the rectifier supply. These capacitors are typically electrolytics and are very heavy, space consuming and have a limited life. In fact these capacitors are the major factor that determines the life of the drive.
- Conventional drives using a diode rectifier system have the problem of feeding high level, low frequency harmonics into the supply and thus have a very poor power factor.

- Using a single end supply there is one energy flow path from rectifier to inverter to motor in conventional drives and during braking there is a waste of energy that has to be dissipated in heavy resistors which are also heavy and space consuming.

All the above mentioned problems forced engineers to think about alternative means of supplying the actuator motor especially where there is need to reduce the weight, losses and improve the reliability and efficiency. Based on the above, a power conversion arrangement can be thought of as:-

- First issue: The bulky dc-link capacitor can be eliminated by converting directly AC to AC. The vital decoupling can be moved (and combined with the filtering role) to the start or end of the drive. The argument being that with fast switches the decoupling function does not require large static components and hence the overall static component budget falls.
- Second issue: A Direct AC to AC conversion system does not have a diode rectifier and hence only small filters are required to deal with the high frequency harmonics. This advantage is of course shared with a full switching input bridge.
- Third issue: The AC-AC system is capable of bi-directional power flow and the power from the machine is able to flow back in to the supply so as to improve the power factor and the efficiency of the drive. Again this advantage is shared with a full switching input bridge.

The so called ''Matrix Converter'' has the potential to provide a solution to all of the above mentioned issues if precise control and switching is designed. A three-phase matrix converter circuit is shown in Fig.2.12 where the bidirectional power flow is achieved by means of a switch cell which is capable of blocking voltage and conducting current in both directions.

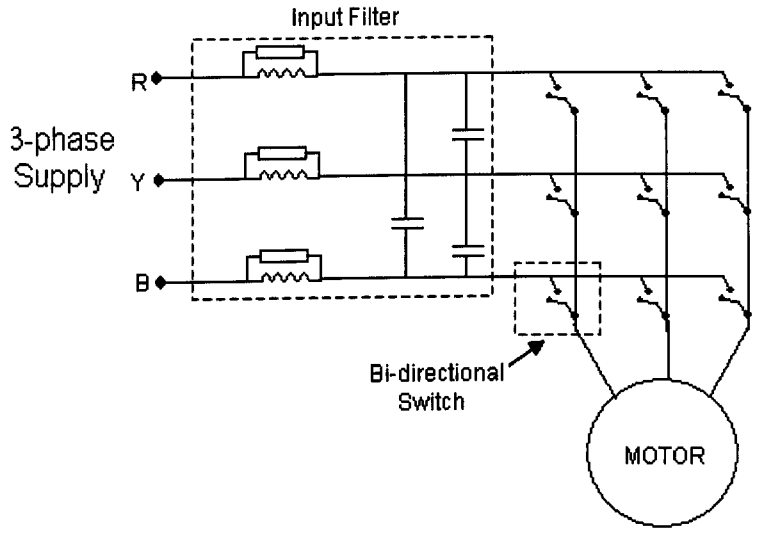


Fig.2.12 Three-phase Matrix Converter

The realisation of this AC-AC direct converter Matrix Technology was demonstrated by the work of Venturini and Alesina *[20] [21]*. It was shown that it is possible for the machine to draw (near) sinusoidal current through the supply lines if the three supply lines are directly connected to the three-phase motor terminals through a matrix web of bidirectional switches provided the switching is controlled precisely using multistep commutation strategy. So in the Matrix converter at any time one of the input lines is chosen as having the most appropriate voltage for the output line. The output could be taking positive or negative current and could provide positive or negative voltage once the switch is turned off and this reveals the need for a switch capable of blocking voltage and conducting current in both directions. Up till now no such device is available and so it is constructed by use of discrete power devices as shown in Fig.2.13. Among them are diode bridge, common emitter and common collector arrangement. Diode bridge arrangement has the advantage of only one gate driver, with the disadvantage of uncontrolled direction through the switch. In common emitter arrangement the two diodes provide reverse blocking capability. Advantages with common emitter include reduced conduction losses (only two devices in conduction at anytime) and independent control of direction of current. Disadvantage of common emitter switch include requirement of isolated power supply for gate drives for each bidirectional switches.

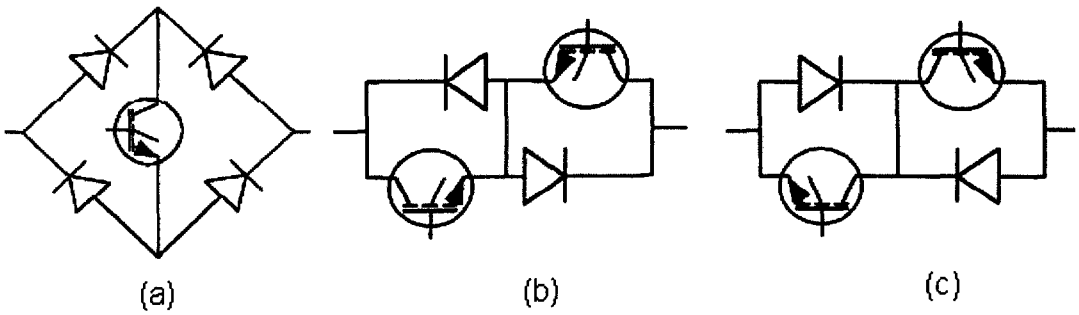


Fig 2.13 Bi-directional switch for MC (a) Diode Bridge (b) Common Emitter switch (c) Common Collector switch

Common collector arrangement is similar to common emitter only difference the IGBTs are arranged in common collector mode. Switching losses for common collector switch is similar to common emitter switch. In common collector switch only six isolated power supplies are needed to supply gate drive signal, however, in practice other constraints such as minimizing the stray inductance means that operation with only six isolated supplies is not generally viable. Therefore common emitter is generally preferred for creating matrix converter bidirectional switches *[59]*.

Switching of Matrix Converters:- As noted the basic idea of a matrix converter drive is to eliminate the dc-link and thus it does not offer any natural path for the circulating (freewheeling) currents. This is the reason the commutation process for a MC is much more complicated and proper operation is more difficult to achieve than in traditional dc-link converters. If a more detailed view is taken of the circuit of the MC in Fig.2.12 it can be concluded that to avoid any short circuit between output and input phases no more than two bidirectional switch can be switched ''On'' at any one time. Also it can be concluded that all the bidirectional switches in any one phase cannot be turned off at the same time because that would result in large voltages as the inductive load current would be suddenly blocked. This was the problem that hindered the development of MC's for a long time.

Basic Commutation: - The commutation technique adopted to switch a MC is a compromise between complexity and the issues mentioned above. The commutation techniques breaks the above mentioned rules and allows a short commutation overlap to create a short circuit between phases and the resulting current rise is limited by extra circuitry to avoid destruction of the converter. In this overlap technique an incoming cell (i.e. a bidirectional switch) is fired

before the outgoing cell is switched off. The use of extra circuitry includes inductors which are undesirable because they are large and expensive and also because the switching time for each commutation is greatly increased which in turn may cause control problems. For the switch timing please refer to Fig.2.14 (a) and Fig.2.15.

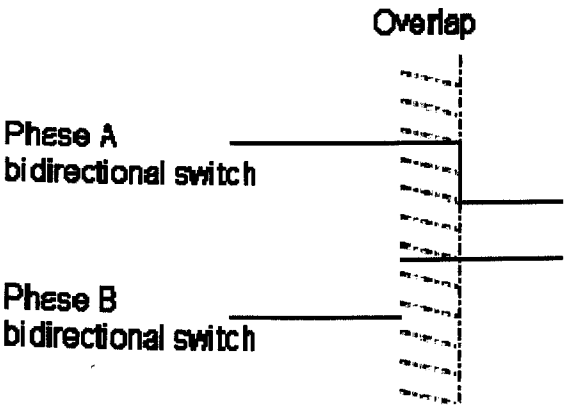


Fig. 2.14(a) Overlap commutation

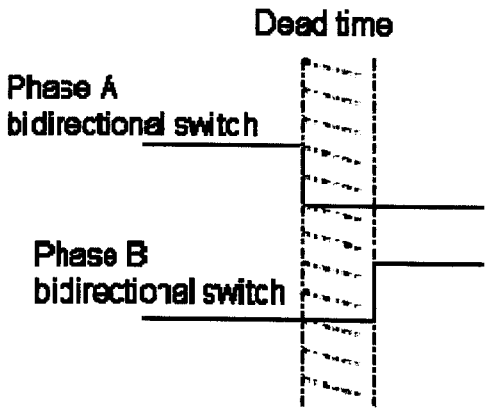


Fig.2.14 (b) Dead-time Commutation

The opposite of this overlap commutation is "dead time" commutation where no switch is fired thus causing a momentary open circuit and hence an overvoltage. Snubbers and clamping devices are needed to control this overvoltage and provide a (temporary) load current path. This method is also undesirable since energy is lost in every commutation moreover the snubber and clamping circuitry adds complexity and weight which mitigates against the advantages of Matrix converter - smaller and lighter. This style of timing is shown in Fig.2.14 (b).

Semi-soft Commutation: - An alternative method of commutation which obeys the rules of a MC is a four-step commutation in which the direction of current in each switch is controlled. For example take a phase where it is desired to switch off cell A and switch on Cell B without any momentary short circuit or open circuit of the phases. It is assumed here that load current towards the load is positive.

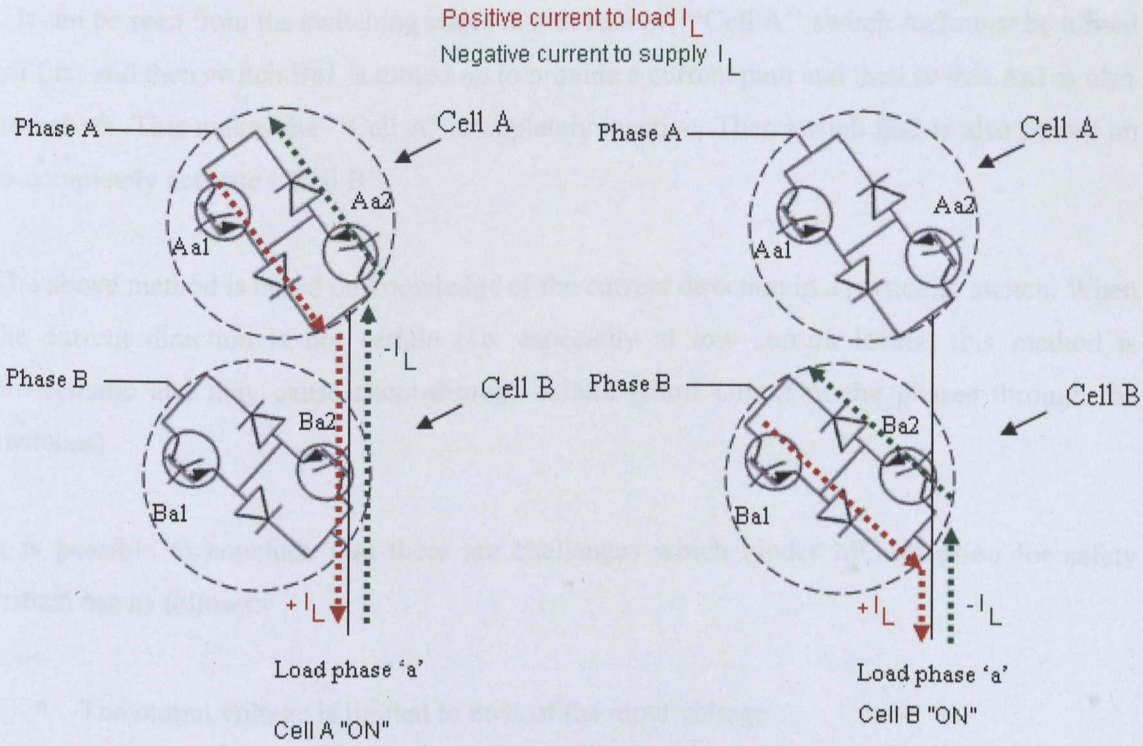
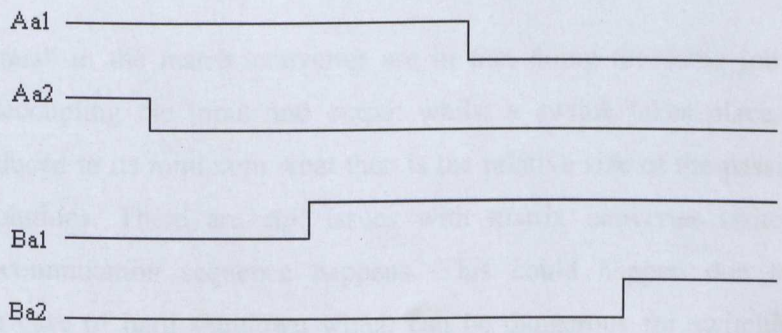


Fig.2.15. Soft-Commutation of a Matrix Converter phase.

(Note: Switch 'Aa' means the lines connecting the input terminal of the MC 'A' to output 'a' of the MC which is input terminal of the load. Similarly for switch 'Bb')

Referring to Fig.2.15 the soft-commutation strategy is actually providing a path for the load current through the second cell which is to be turned on. So during turn off of ''Cell A'' the load current path is provided by a switch in ''Cell B''. In steady state both the devices in the active bidirectional switch are gated to allow bidirectional current flow. The switching sequence for four step semisoft current commutation is shown in Fig.2.16.



(Note: Upper States are ON and lower states are OFF)

Fig.2.16 Soft-Commutation switching states.

It can be seen from the switching states that to turn off ''Cell A'' switch Aa2 must be turned off first and then switch Ba1 is turned on to provide a current path and then switch Aa1 is also turned off .This makes the ''Cell A'' completely inactive .Then switch Ba2 is also turned on to completely activate ''Cell B''.

The above method is based on knowledge of the current direction in a particular switch. When the current direction is not certain (i.e. especially at low current levels) this method is problematic and may cause shoot-through failure (short circuit of the phases through the switches).

It is possible to conclude that there are challenges which hinder MC adoption for safety critical use as follows:-

- The output voltage is limited to 86% of the input voltage.
- The need for a large number of fast high-power switches increases the cost and reduces the mean time between failures.
- Complex control algorithms.
- Determination (sensing) of current direction in the bidirectional switches is very difficult and complex.
- As there is no dc-link the pulse width modulated supply to the matrix converter which is actually a discontinuous power flow poses problems during commutation of the switches which is reflected into the input terminals of the drive as supply harmonics. This problem is solved by using input filters but still it adds cost and complexity.

The "input filters" in the matrix converter are in fact doing the same job as the dc-link capacitor in decoupling the input and output whilst a switch takes place. If the dc-link capacitor is reduced to its minimum what then is the relative size of the passive components in the two solutions. There are still issues with matrix converter switching when an inappropriate commutation sequence happens. This could happen due to current sign detection or in case of hard shutdown which can be dangerous for switching devices. To rectify this issue requires an over voltage protection system *[60]*.A diode clamp protection circuit with a capacitor is often used *[61]* but this solution is expensive and bulky. Some other solutions were proposed to address this issue including varistors *[62]*, active clamping *[63]* or

shutdown commutation sequences *[64]*. All above solutions are not in harmony with the aims of this research to achieve simplified reduced capacitor for actuator drive converter. Considering above arguments, further investigation of this aspect is not necessary and out of scope of research work presented here but it might at least provide a better background against which to judge the two systems.

Despite all of the limitations mentioned above the potential of Matrix converters in terms of reduced weight and adequate reliability cannot be ignored. Current research is towards reducing the switching complexity of MC's which might make them more adoptable for safety critical use.

Recent research and development work done by Smiths Aerospace into using Matrix converters for flight critical control surface includes a 3kW Matrix converter to drive an EHA for an Airbus A320 Aileron *.22]*.They have developed a Totally Integrated More Electric System (TIMES) using a Matrix converter driving an actuator motor. The aileron actuator is shown in Fig.2.17.

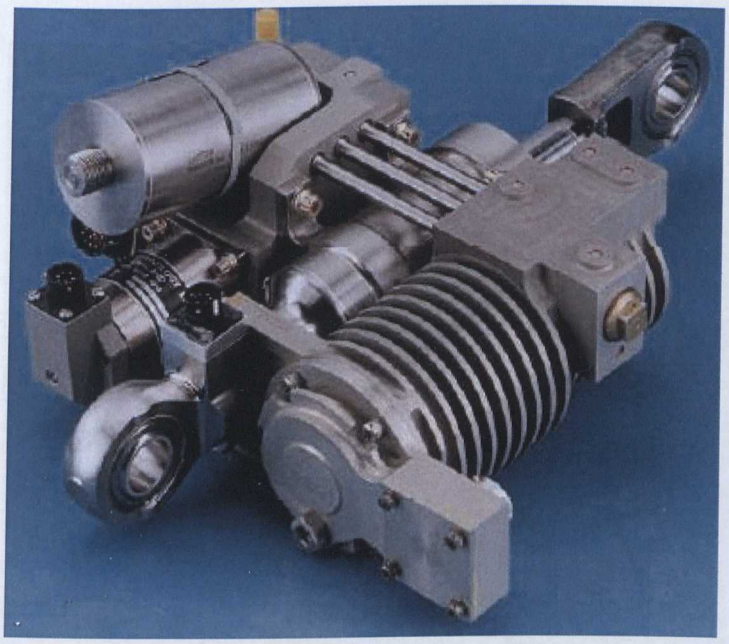


Fig.2.17.Airbus A320 Aileron actuator by Smiths Aerospace.*[22]*

A bidirectional switch module was used for the matrix converter made by Eupec *[22]* and this is shown in Fig.2.18. The module uses 18 IGBTs and 18 Diodes with a rating of 7.5 kW (1200V and 35A.). The EHA operates from an 115V L-N three-phase supply providing a usable line to line voltage of about 160V.

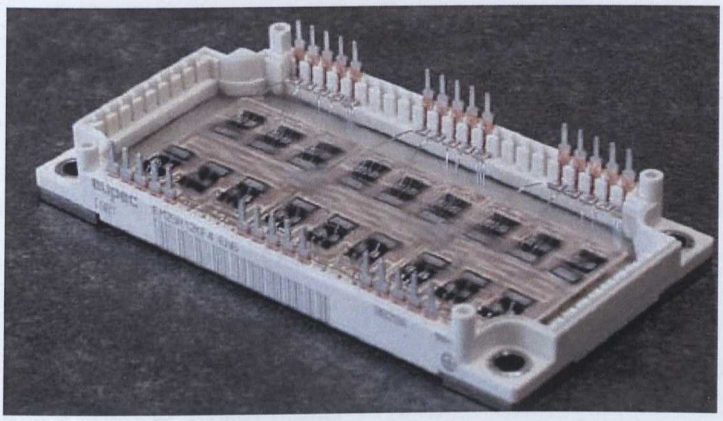


Fig.2.18. Fully Integrated Eupec bidirectional switch module for the Matrix Converter Drive. *[22]*

The complete matrix converter module is shown in Fig.2.19.

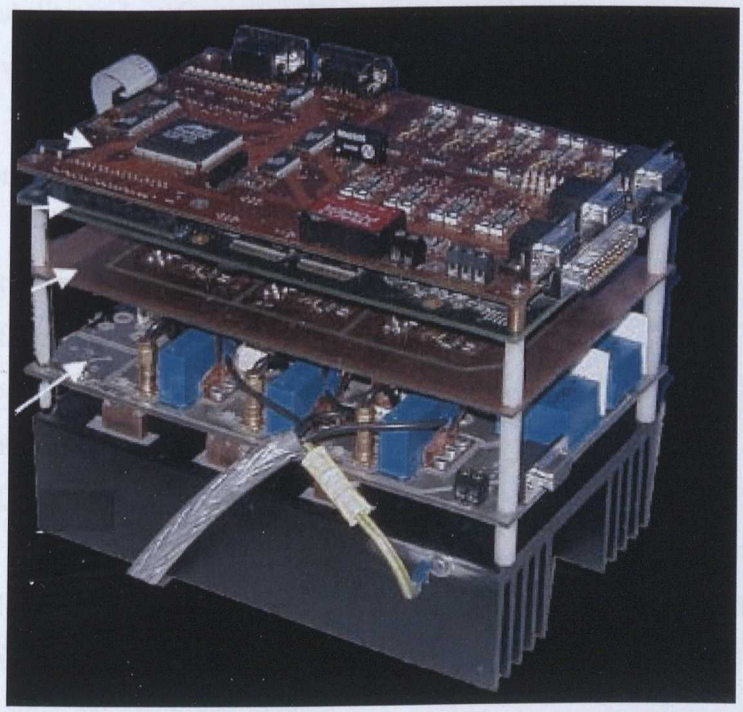


Fig.2.19 Totally Integrated More Electric System (TIMES) using Matrix Converter Drive *[22]*

It is worth noting again here that even the Matrix converter presented above is not completely free from filtering components. Although it eliminates the capacitors from the dc-link it introduces filtering capacitors on the supply side to filter out incoming harmonics as well as to provide a freewheeling path to load current as evident from Fig.2.12. Also the reliability comparison analysis done by Smiths Aerospace *[22]* shows that the six pulse rectifier topology for an actuator drive would give the highest reliability.

2.2.5 Capacitor Technology Overview

The main features to consider while selecting a dc-link capacitor for converter applications can be summarised as *[103]*:-

- Low ESR (equivalent series resistance) and ESL (equivalent series inductance) in order to achieve reduced circuit losses.
- High ripple current capability at high frequencies.
- High insulation resistance to achieve near constant DC voltage levels.
- Sufficiently enough capacitance value to achieve smoothing of dc-link voltage.
- Thermal and electrical stability of the capacitor.
- High reliability and performance during product life time.
- Size and weight considerations for specific application.

Various capacitor technologies for use in dc-link drives can be considered are as follows:-

- Electrolytic Capacitors
- Polymer Film Capacitors
- Ultra Capacitors or Supercapacitors
- Solid Tantalum Capacitors
- Ceramic Capacitors

There is no single capacitor technology which can satisfy all above mentioned requirements *[103]* as each one has its own merits and demerits. From dc-link point of view, these capacitor technologies are discussed here:-

Electrolytic Capacitors: - So far the electrolytic capacitors were the most common choice for dc-link converter applications. This trend can be attributed to the requirement of high capacitance that can be achieved with this technology. The electrolytic capacitor uses the dielectric properties of aluminium corrosion. To achieve good specific energy the aluminium foil is pitted and this limits the maximum nominal voltage of this type of capacitors (500-600Volts). Due to limited maximum nominal voltage, electrolytic capacitor bank arrangement is required in higher voltage applications. Electrolytic capacitors are prone to failures near 100 °C operating range. The strict higher reliability and stability requirements under high temperatures are forcing the way forward for film capacitors in precision applications.

Polymer Film Capacitors: - The thin metallic layers are coated on the dielectric in such a way that they can volatilize to isolate the defect. So when the dielectric breakdown strength increases at any local weak point in film capacitor, the dielectric breakdown occurs. This dielectric is transformed in to highly compressed plasma and tries to force its way out. At the same time the metallisation near the channel evaporates and insulate the region. This process allows the capacitor to regain full functionality and thus enhances reliability during its lifetime. This self healing property of polymer film capacitors also allows increase in the voltage gradient. These capacitors can withstand twice rated voltage without significantly reducing lifetime and therefore user only needs to take account of nominal voltage that is required for a particular application.

Unlike the electrolytic technology, the film technology is more benefiting in low capacitance value applications. Due to their low dielectric loss factor, the polypropylene film capacitors were first choice in film capacitor technology. But now the polyester film capacitors with low ESL and ESR are also proving competitive against polypropylene types. Because of polyester's higher dielectric constant, much higher capacitance values can be produced giving more volumetric efficiency *[55]*.

Recent advances in semiconductor technology can allow direct mounting of dc-link capacitors onto the IGBT modules. The connection lead between the IGBT and dc-link capacitor is no longer required, forcing the stray inductance to decrease dramatically. This helps to limit over voltage due to semiconductor commutation.

There are several companies involved in developing high temperature and high reliability film capacitors. AVX TPC has already demonstrated life expectancy of 100,000 hours for this capacitor technology under nominal electrical and environmental conditions for traction applications *[54]*. In order to achieve this high lifetime, the capacitor was hermetically sealed by a polyurethane resin in an aluminium box. The film capacitor types can also allow use of different types of terminals for example large copper plate terminals.

The AC polycarbonate capacitors were developed by TRW under NASA research programme *[53]* and subjected to 5000 hour, 400Hz test over a range of voltage and temperature. Various designs for both metalized film and film-and-foil types of construction were studied for temperatures up to 120°C and two designs were demonstrated with no failures up to this temperature range. No correlation between increase in the capacitor failures with increase in voltage at temperatures up to 125°C was found. It is important to note here that the term ''capacitor failure'' or end of life refers to decrease in capacitance value of 2% *[54]*.

Researchers in *[56]* have developed ionic polymer metal composite capacitor (IPMCs) that meets typical aerospace design constraints of high reliability, robustness, light-weight as well as high temperature (up to 300°C) operation. The IPMCs were fabricated as flexible thin films that can be shaped and scaled in any size, even around the devices. The IPMCs developed so far can offer up to 1 mF cm-2 or 40mF/g for a 100 μm thick polymer substrate *[56]*.

It is clear that capacitors which use polycarbonate film as dielectric medium have advantage in ac power aerospace applications because of low dissipation factor, good dissipation stability and high temperature capability.

Ultracapacitors or Supercapacitors: - Supercapacitors are also known as ultracapacitors or electric double layer capacitors. Compared to a conventional capacitor, the ultracapacitor offers very high energy density and small size. Capacitance values up to 400 F in a single packaging are available with this technology. Due to their high capacitive density these capacitors can be used in place of batteries in some applications. The construction of supercapacitors is based on carbon (nanotube) technology. The carbon technology used in these capacitors creates a large surface area between the two electrodes separated by a dielectric material. Unlike other capacitor technologies, the dielectric in supercapacitor is actually an electric field generated by a physical barrier of activated carbon. Thickness of this

dielectric is as thin as a molecule. Extremely large surface area of activated carbon later yields several thousands square meters per gram allowing absorption of large amount of ions. The charging/discharging takes place in an ion absorption layer formed on the electrodes of activated carbon. The activated carbon electrodes are impregnated with an electrolyte where positive and negative charges are formed between electrodes and impregnant. This way the electric double layered capacitor becomes an insulator until large enough voltage is applied across it *[100]*.

Supercapacitors have applications in consumer electronics (PC cards, cameras etc where extremely fast charging is required), hybrid electric vehicles (regenerative braking) and as replacement of batteries. Power density of supercapacitors (in commercial use) by manufacturers such as Maxwell, NessCap, Eposis and Econd is around 4-7kW/Kg.

Advantages associated with supercapacitors are high efficiency, long life cycle, rapid charging, low impedance, environment friendly, wide temperature range and simple charge methods. On the other hand they also have limitations such as high self discharge and linear voltage discharge. In dc-link converter applications, the main limitation of supercapacitors is its low individual cell voltage (0.9-3.3V), meaning a series connection of many supercapacitor cells is required to obtain higher voltages *[101]*. In series formation any unequal distribution of cell voltage will affect the performance and life time of the cell. To overcome this problem an additional voltage balancing control strategies are suggested in *[102]*.

Solid Tantalum Capacitors: - Tantalum capacitors are manufactured from a powder of pure tantalum metal. Depending on the particle size of this powder, the surface area and thereby the capacitance can be controlled. Due to their dry design and volumetric efficiency, the tantalum capacitors are increasingly replacing their aluminium electrolytic counterparts.

Due to their low leakage and high capacity, the tantalum capacitors are frequently used in sample and hold circuits to achieve long hold duration. Tantalum capacitors are replacing electrolytic capacitors for applications which require high reliability and high temperature operation. But for kW range dc-link voltage converter applications such as the one presented in this thesis, the tantalum capacitors are not commercially available.

Ceramic Capacitors:- The non-polar ceramic capacitors are in widespread use in electronic equipments for past many decades as a low cost, small size and high capacity alternative to other low value capacitor types. Ceramic capacitor is made up of alternative layers of metal and dielectric ceramic material. The ceramic capacitors can be categorised in three different types depending on their temperature characteristics.

Class I type ceramic capacitors are the most stable type available and have a predictable temperature coefficient. They are made up of non ferro-electric material and often used in resonant circuit applications but at the same time offer lowest volumetric efficiency. For circuit coupling applications where stability of capacitor characteristics is not important, ferro-electric Class II type ceramic capacitors are used. Class II type ceramic capacitors offer higher volumetric efficiency but less stability. Class II ceramic capacitor's characteristics are affected by temperature, voltage and time.

Class III type ceramic capacitors are general purpose capacitors used for coupling or other applications where dielectric losses, stability of capacitance characteristics are of little importance. Class III capacitor type offers highest volumetric efficiency but poorest stability of any type.

A very limited research work is published for use of ceramic capacitors in dc-link applications. Although the ceramic capacitors are extremely reliable but are only commercially available in very small sizes and thus can not be considered for kW range dc-link converter applications.

As discussed in this section features such as high current capability, low inductance, flexible design, different mounting options, thermal stability, reliability and long service life makes film capacitors the preferred choice for reduced dc-link capacitor drive applications. The film capacitors can clearly replace other capacitor types to achieve high reliability, cost and weight savings in the proposed drive of Fig.2.11. Micro farad range dc-link film capacitors for power electronic applications are already commercially available from EPCOS which can deliver mean life expectancy figures of up to 100000 hour *[57]*.

2.3 DC-Link Reduction Previous Research

Two decades of developments in semiconductor research have facilitated electrical engineers to obtain huge improvements in cost and performance of electrical drives. Modern research and development is more focused on high frequency power electronics devices and control electronics but there is lack of research and development on passive components of the drive. Research published by *[4]* have illustrated the impact of capacitors and inductors on the overall size and weight of power conditioning equipment in more electric aircraft applications and is shown in Fig. 2.20.

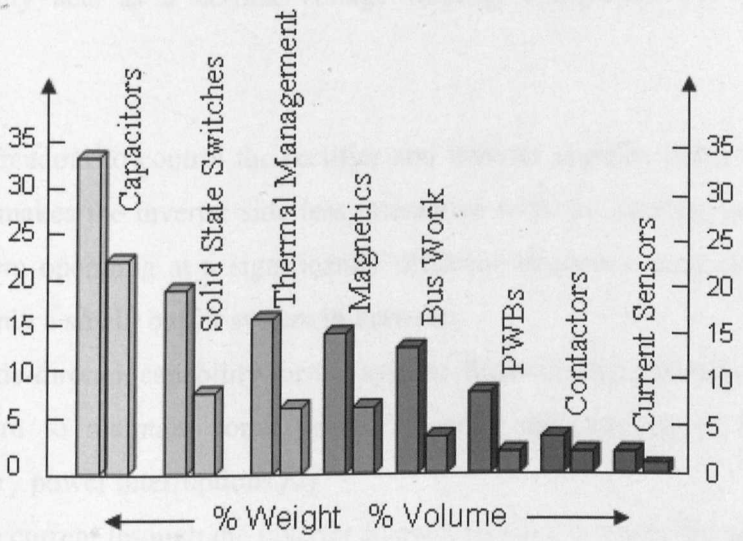


Fig.2.20 Power conditioning weight and volume *[4]*

As stated above, one of the major aims of this research is to reduce the size and cost of the drive system by reducing the filtering components involved. One of the most unreliable and bulky parts of any variable frequency drive system using a dc-link is the capacitor in the dc-link. There is numerous research publications later discussed further in this chapter which deal with the problem of achieving a minimum acceptable dc-link capacitor value for a particular drive performance.

In a typical AC drive the AC supply can be converted to DC voltage by means of a standard diode rectifier or a fully switched pulse width modulated IGBT rectifier. A capacitor is used to hold this DC voltage and it can then be converted into a variable frequency AC pulsed

voltage for a load motor. Using a three-phase diode rectifier as the inverter input, the dc-link output of the rectifier will have its lowest frequency ripple at 6 times the supply frequency. The dc-link peak is determined by the supply voltage and the ripple voltage magnitude depends on the dc-link capacitor value. Higher values of dc-link capacitor result in small dc-link voltage ripple and better input and output currents. In cases where the inverter is supplied using a fully switched IGBT rectifier, the dc-link performance not only depends on the value of dc-link capacitor but also on the switching frequency of the rectifier. If the rectifier can match the inverter/load requirements at all instances then no dc-link capacitor is required in theory but because the modulation and control is not in perfect synchronisation and there is a one-step PWM delay, a certain amount of capacitor is required to act as a buffer. The dc-link capacitor not only acts as a dc-link voltage filtering component but also offers other advantages:-

- It gives freedom to control the rectifier and inverter systems independently. In other words it makes the inverter side less interactive with the rectifier, as otherwise these two system operating at a significantly different frequency range tend to interact if there is only a small buffer system in between.
- It adds ride-through capability for the system .Ride-through capability is the ability of the system to maintain some degree of order and control of the drive during momentary power interruptions.*[2]*
- When the current through the inverter freewheels back towards the supply, the dc-link capacitor provides a path for it and thereby helps the power factor and the efficiency of the overall system.

In the last ten years there have been many publications related to the reduction and even elimination of the dc-link capacitor. This section will discuss the previous dc-link related research in detail and categorize it based on its applicability to this research. For a better understanding of the dc-link research a typical AC-DC-AC drive is considered as shown in Fig.2.21.

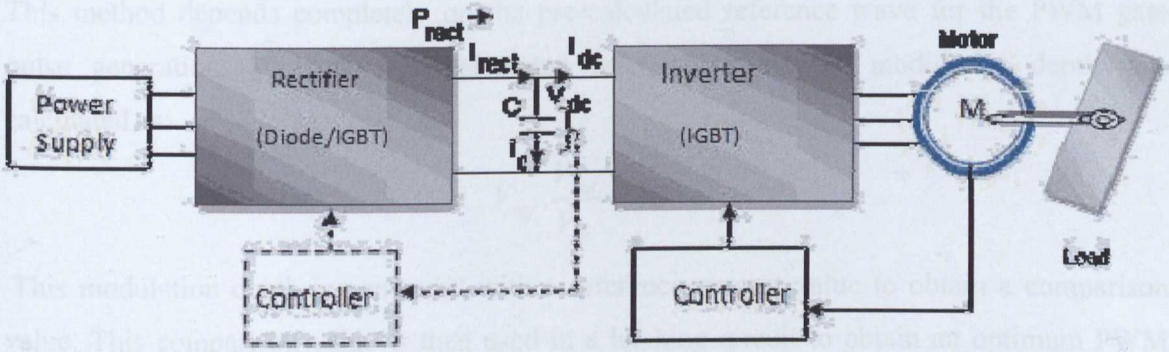


Fig.2.21 Typical AC-DC-AC drive

The earliest research work in reducing the size of the dc-link capacitor was reported in *[18]* with active and passive converter bridges. The control method involved voltage compensation by implementation of triangular comparison pulse width modulation. The dc-link research published in the last decade is summarised below along with discussion about their contributions and demerits.

[1] AC to AC conversion without a dc-link capacitor: This patent filed in 1996 aimed for AC to AC conversion without the use of a dc-link capacitor *[19]*. This technique is based on the measurement of the dc-link voltage and compensation for its ripple content. The patent concept is shown in Fig.2.22.

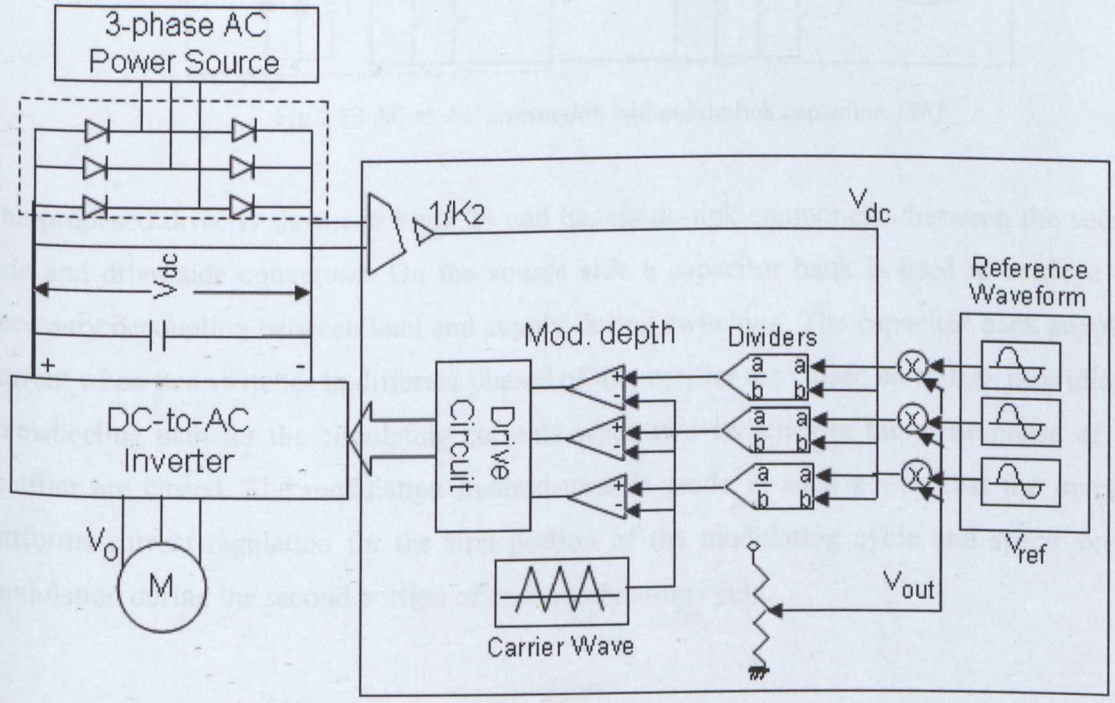


Fig.2.22 Conceptual AC to AC conversion without dc-link capacitor patent *[19]*.

This method depends completely on the pre-calculated reference wave for the PWM gate pulse generation. With this pre-calculated reference value the modulation depth was calculated as:

$$V_{ref} \cdot \frac{V_{out}}{V_{dc}} = M$$

This modulation depth is compared with a reference current value to obtain a comparison value. This comparison value is then used in a latching circuit to obtain an optimum PWM pulse pattern to compensate the dc-link voltage ripple. This patent relies completely on the pre-calculated reference information and therefore cannot adapt to dc-link variations. The pulse pattern output is fixed as a result of the fixed reference.

In 2005 Honeywell *[28]* came up with a patent for AC to AC conversion without a dc-link capacitor for a compressor motor drive in aircraft applications.

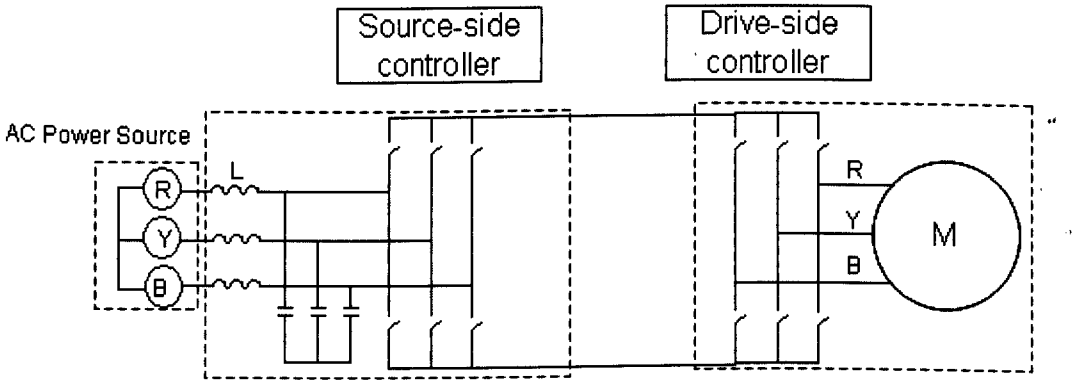


Fig.2.23 AC to AC conversion without dc-link capacitor. *[28]*

The proposed drive is shown in Fig.2.23 and has no dc-link components between the source side and drive side converters. On the source side a capacitor bank is used to achieve the necessary decoupling between load and supply during switching. The capacitor bank supplies current when two switches in different phases of the rectifier are closed as well as providing a freewheeling path for the circulating currents when two switches in the same phase of the rectifier are closed. The modulation method used is made in such a way that the inverter performs current regulation for the first portion of the modulating cycle and space vector modulation during the second portion of each modulating cycle.

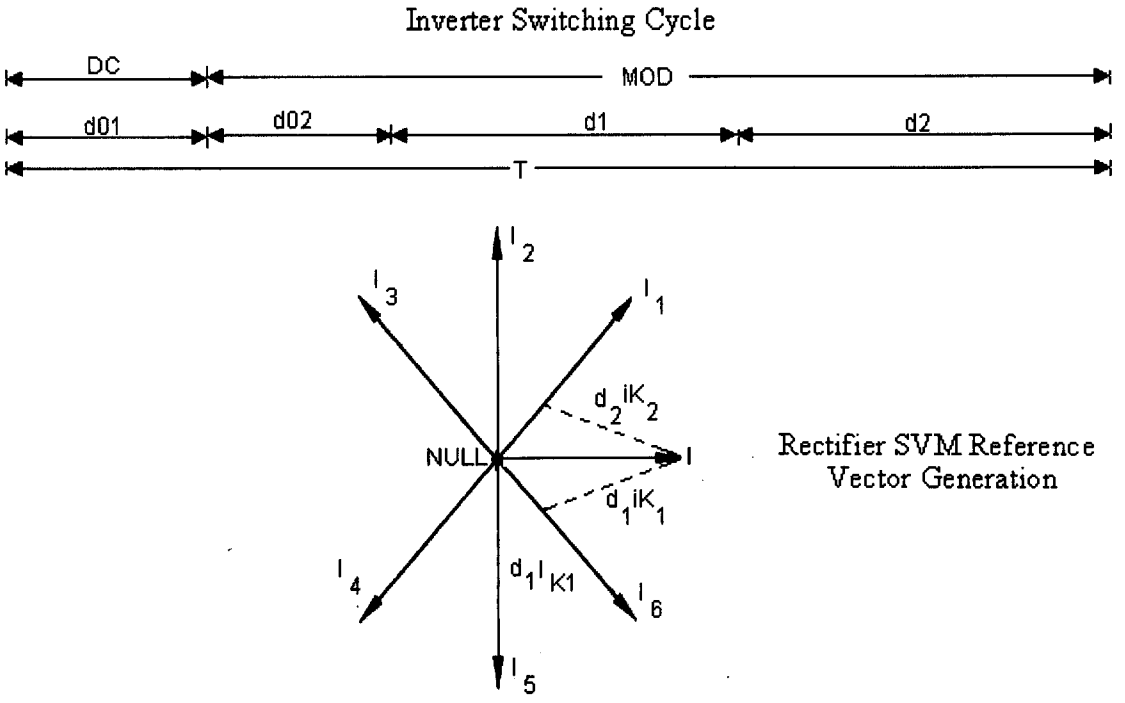


Fig.2.24. Switching technique for rectifier and inverter modulation *[28]*.

In Fig.2.24 the inverter switching cycle (where T is PWM period) is shown where DC represents the current regulation period (d01) which is required to control the current in the dc-link. During this period one leg of the rectifier is shorted with the dc-link. In the next switching period MOD (as shown in Fig.2.24) is calculated so as to extract fundamental frequency currents from the supply side. On the other hand rectifier modulation varies the duty cycle d1 and d2 to create the rotating current vector I. This reference current vector ensures the capacitor bank is connected and disconnected to maintain a ripple free dc-link current.

Another piece of research from *[30]*, is in principle, similar to that presented in *[28]*. Here the dc-link is also eliminated by putting a high frequency filter capacitor on the supply side as shown in Fig.2.25. These filter capacitors absorbs incoming harmonics and provide smoother dc-link voltage.

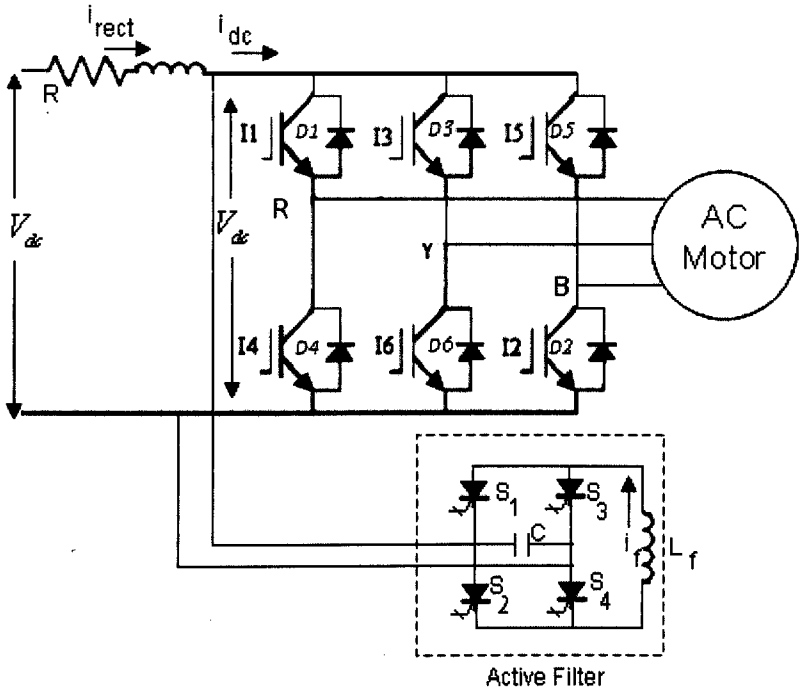


Fig.2.25 Elimination of dc-link capacitor by front end filter capacitor bank *[30]*.

Despite claiming to eliminate the dc-link capacitor this research uses a small capacitor (C) for device commutation purposes and an inductor (L) to offset the dc current levels. Moreover this method also relies on the direct dc input supply.

In 1993 Minari, Y. et al published their research *[34]* for rectifier-inverter drive without dc-link components based on a filtering LC circuit on the supply side. To achieve reduced filtering requirements the rectifier is PWM controlled. The research claims to have no dc-link components while the input filters absorb the inverter switching ripples. But the feasibility of this configuration has applications at only low power level.

There is also the similar work presented in *[41]* where the dc-link capacitor, input inductor and braking chopper are replaced with a front end filter.

Research work presented by Kim, J.S et al. *[33]* in 1993 relies on the principle of power balance on both sides of the converter-inverter system. Unlike previous approaches based on other filtering components this method is based on an active power balance between bridges regardless of the load variation in real time as shown in Fig.2.26.

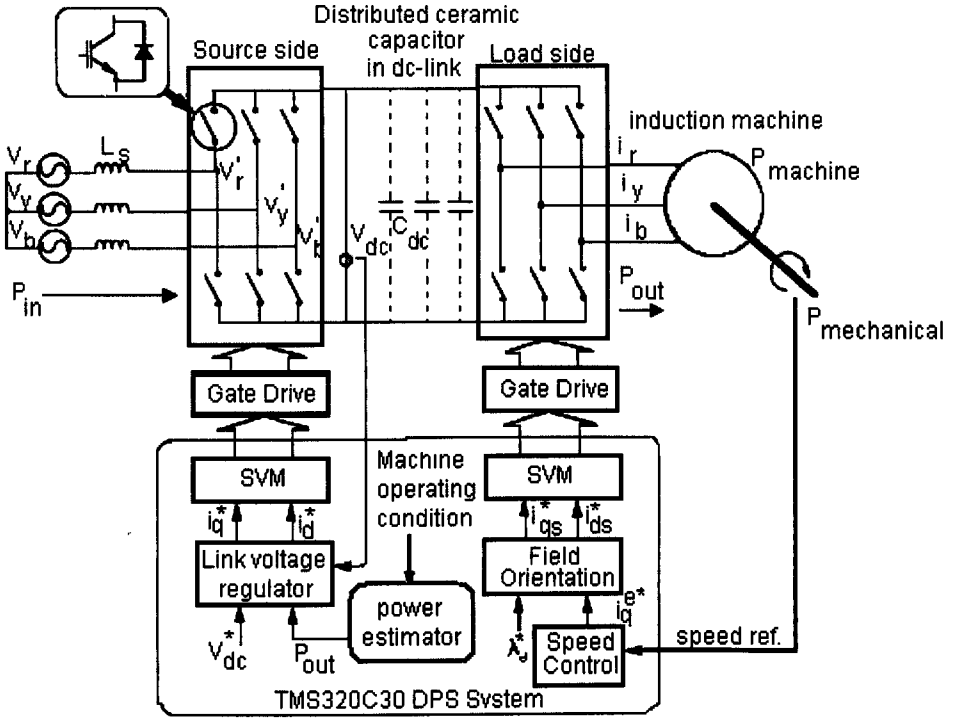


Fig.2.26 Reduction of dc-link capacitor by power balance *[33]*.

The above method ensures load balance by measuring instantaneous power delivered to the load and aiming to provide exactly that power from the rectifier to the dc-link. Power estimation is done by summing up the mechanical power output and the power loss in the machine. Hence:

$$P_{(machine)} = P_{(mechanical)} + P_{(machine\ loss)}$$

Power output from inverter can be written as:

$$P_{(out)} = P_{(machine)} + P_{(inverter\ loss)}$$

Another estimated power is the inverter loss power P(inverter loss). There are inevitable switching losses and conduction losses in the power electronic switching devices which are not insignificant but their exact estimation if not possible. This method based on estimation of inverter power losses which are assumed to be proportional to phase currents at constant frequency as:

Inverter Losses = Switching losses + Conduction losses.

So $$P_{(\text{inverter loss})} = (V_{drop} + V_{CE})(i_r + i_y + i_b)$$

Where conduction losses are simply the product of collector voltage V_{CE}, the switching losses are attributed to blocking voltage V_{drop} which is a function of dc-link voltage.

By applying a power balance principle between output power $P_{(out)}$ and input supply power $P_{(in)}$ as :-

:

$$P_{(out)} = P_{(in)}$$

Where output power is given as:

$$P_{(out)} = \frac{3}{2}.(V_q i_q + V_d i_d)$$

Here $\frac{3}{2}$ multiplier is park transformation factor. For vector controlled inverter we have i_d=0, so,

$$P_{(out)} = \frac{3}{2}.V_q i_q$$

The input controller current reference is formulated as the combination of feedback term (dc-link voltage error) and feedforward term (output power). The rectifier controller demand for unity power factor operation (based on output power) is obtained using the above analysis as:

$$i_q^* = \frac{2.P_{(out)}}{3.V_{dc}}$$

The above research provides a very good basis for reducing dc-link capacitor but there are a few assumptions made in this research which might make it difficult to achieve in practice. The controller is implemented with a voltage regulating deadbeat control loop so it is sensitive to machine parameter variations. Another assumption made is that the rectifier side is perfectly operating at unity power factor at all times and hence oscillating components of power associated with non-unity power factor are not taken in to account which might thereby create incorrect instantaneous values using the power balancing equations.

Extending the above research work the authors integrated a resonant circuit into the drive *[42]*. As shown in Fig. 2.27, the resonant circuit consists of two additional switches to allow the bridge devices to operate with zero switching losses.

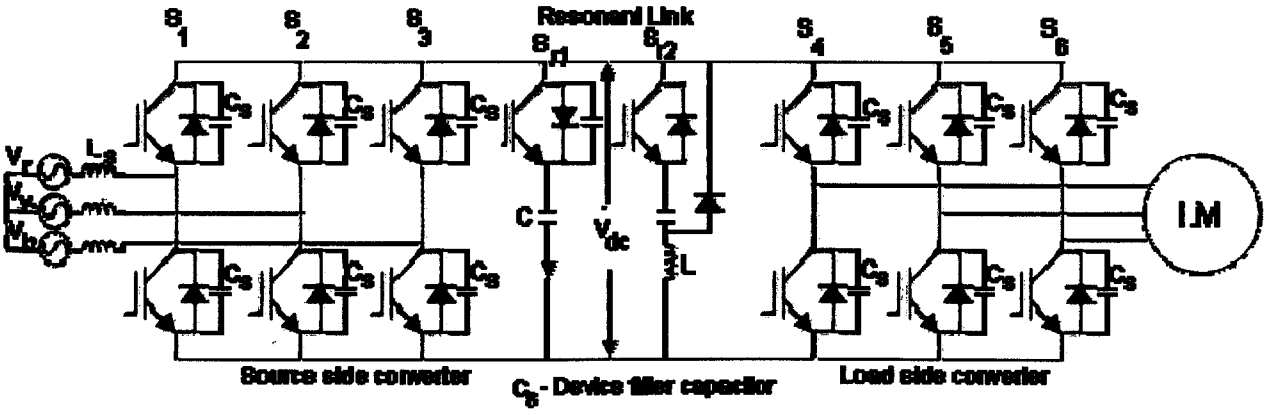


Fig.2.27 Integrated resonant circuit in AC/DC/AC drive to achieve low losses *[42]*.

The control methodology presented for both the front and back end converters is aimed to compensate for machine parameter changes. The source and load side parameters are measured and a single control signal used for the switching of both converters at the same time thus allowing for zero state switching and reduced losses. This addition of resonant link adds even more complexity to the whole system and thus only power balancing part of this work is useful for research presented in this thesis.

Continuing the trend of power balancing techniques to reduce the dc-link storage, K.Nam et al. in *[43]* presented a fast dynamic control scheme. In their work the inverter power dynamics is measured and fed into the rectifier to produce an exact amount of power that is required for the inverter. Previous methods of dc-link control do not consider the inverter dynamics and hence are ineffective in cases when the motor speed changes suddenly. This method relies on the calculation of the inverter power using the output voltages and currents in real time. This type of master-slave arrangement uses the inverter dynamics of $\frac{dP_{inv}}{dt}$ to find the transfer function of the controller to keep the dc-link voltage constant. This method shows no performance degradation during high frequency operation unlike conventional methods which degrades as the frequency goes up.

More publications such as *[37]* adopted a PWM rectifier front end to achieve small dc-link energy storage requirements. They also rely on the principle of power balancing to achieve small supply current distortion and high power factor. Most of these methods require measurement of the load side dc-link current which is not an easy task since at the same time it is important to reduce the stray inductance of the bus bar system between the capacitors and the IGBTs.

[2] Cancelling dc-link voltage ripple: The patent filed by Texas instrument in 2001 *[26]* is based on a modification of the space vector modulation method to reduce the dc-link voltage ripple and thus the size of the dc-link capacitor A dc-link voltage measurement feedback method allows a high speed DSP to generate constantly adapting PWM IGBT gate pulses so as to cancel the dc-link voltage ripple as shown in Fig.2.28.

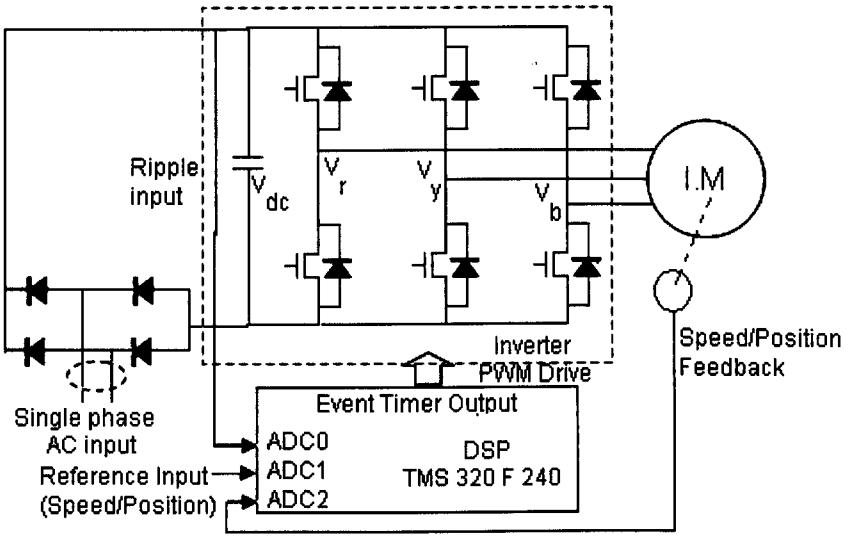


Fig.2.28 Conceptual dc-link capacitor reduction patent by modification of SVM. *[26]*

The reduction in dc-link voltage ripple and thus the necessary capacitor size allows the use of high reliability small size capacitors. The switch dependent inverter fundamental output voltages ($V_{n=r,y,b}$) assuming constant dc-link voltage can be described as:

$$V_n = \begin{vmatrix} V_r \\ V_y \\ V_b \end{vmatrix} = V_{dc} \times \overline{SW} \tag{2.1}$$

Where $\overline{SW}$ is switching function and can be described as:

$$\overline{SW} = \begin{vmatrix} SW1 \\ SW2 \\ SW3 \end{vmatrix} = \begin{vmatrix} \sum_{n=1} A_n \sin(\omega_e.t) \\ \sum_{n=1} A_n \sin(\omega_e.t - 120^\circ) \\ \sum_{n=1} A_n \sin(\omega_e.t + 120^\circ) \end{vmatrix}$$

Here A_n (n = r,y,b)is the peak fundamental inverter terminal voltage and ω_e is the electrical angular speed in rad/sec.

To understand the ripple effect this research first assumes that the dc-link voltage is not ripple free and contains a sinusoidal component of frequency ω_i of magnitude $k.V_{dc}$ .Now the input dc-link voltage becomes:

$$\overline{V_i} = V_{dc} + k.V_{dc} Sin\omega_i t = V_{dc}(1 + k.\sin\omega_i t)$$

Now by use of equation (2.1) the above expression can be re-written as:

$$\overline{V_n} = V_{dc}(1 + k.\sin\omega_i t).\overline{SW} \tag{2.2}$$

It is evident from the above expression that the dc-link ripple has a significant effect on the inverter output. Based on equation (2.2) the research in this patent aims to introduce a counter modulation in the inverter control. So the "counteract" modified switching function would now be:

$$\overline{SW_{new}} = \frac{1}{(1 + k.\sin\omega_i t)}\overline{SW} \tag{2.3}$$

The new inverter output voltage can now be written as:

$$\overline{V_i} = \overline{SW_{new}}.(1 + k.\sin\omega_i t).V_{dc}$$

Putting the value of $\overline{SW_{new}}$ from equation (2.3) the inverter output voltage becomes:

$$\overline{V_i} = \overline{SW}.V_{dc} \tag{2.4}$$

Equation (2.4) shows that the inverter output voltage is changed by the same ripple factor and after introducing the counter modulation in the inverter control the inverter output becomes the same as without the ripple in equation (2.1).This research shows that by suitably altering the frequency, immunity to dc-link ripple can be achieved. This research was extended for power conditioning equipment for space applications *[27]*. The author stated that a 20-30% reduction in the dc-link capacitor had been achieved.

Following the previous tradition of power balancing schemes with a switched front end *[40]* aims to achieve a faster response in dc voltage regulation. Fig. 2.29 shows the drive arrangement.

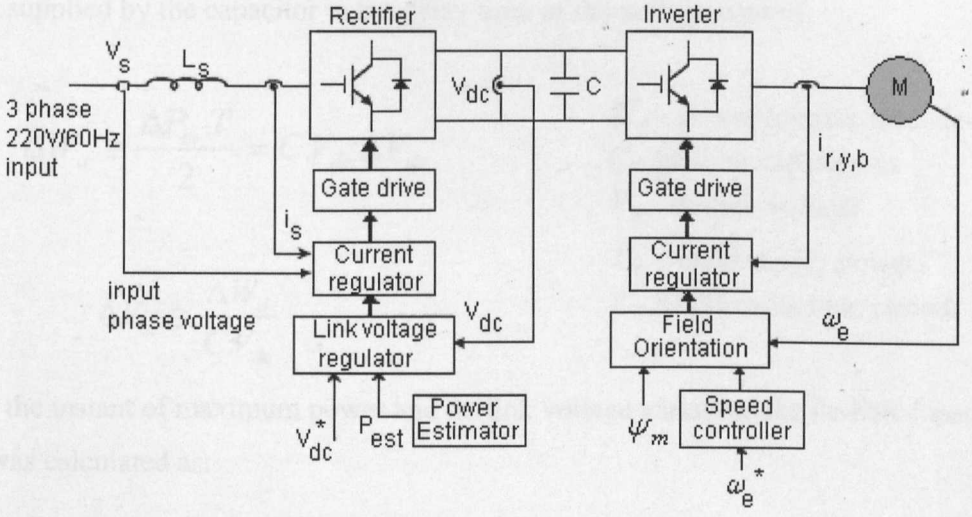


Fig.2.29 Block diagram of quasi-direct ac/dc/ac converter *[40]*

The above scheme depends on power estimation using the dc-link voltage and output current. To achieve better regulation of the dc-link current, a calculated fraction of the input power is injected into the dc-link.

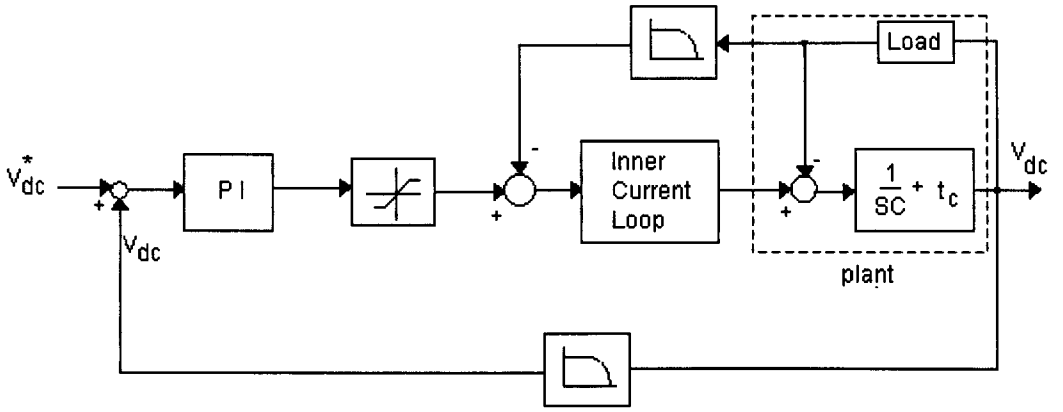


Fig.2.30 Control block for dc-link voltage regulation. *[40]*

Along with achieving a dc-link capacitor reduction, the authors also suggested ways to get unity power factor by generating the current demand in the controller using the input voltage signal. The expression for the determination of the dc-link was carried out based on the energy supplied by the capacitor in the delay time of the voltage control.

So $$\Delta W_d \cong \frac{\Delta P_{in}.T}{2} = C.V_{dc}.\Delta V_{dc}$$

So

$$\Delta V_{dc} \cong \frac{\Delta W_d}{C.V_{dc}}$$

W_d – power transfer from dc-link
C – dc-link capacitance
V_{dc} –dc-link voltage
P_{in} – input supply power.
T – PWM cycle time period.

So for the instant of maximum power and dc-link voltage variation, the dc-link capacitor value was calculated as:

$$C \geq \frac{\Delta P_{in}.T}{2.V_{dc}\Delta V_{dc\max}}$$

Values satisfying the above expression do not always hold true and above all this expression assumes the variation of power flow to be constant in every switching period which is not the case for all the switching periods of the complete cycle. Capacitor technology plays an important role in determining the size of the capacitor as analysed in *[40]* using metalized polypropylene film capacitors.

[3] Other approaches for dc-link reduction: Research work presented in *[31]* proposes a dc-link substitution with three-phase bank of filter capacitors on supply side. So the arrangement hardly provides any benefits in terms of a size reduction for the whole system. On the other hand another research group *[32]* proposed electrolytic-capacitor-less PWM inverter drives where the electrolytic capacitor was replaced with a smaller size AC capacitor. This scheme could be used for higher frequency (above 16 kHz) three-phase sinusoidal PWM converter applications but for applications of a few kHz or a quasi-square wave mode or in single phase inverters, this scheme is not particularly useful. Using higher frequencies are mainly limited by controller reference voltage (and thus lowest possible output voltage when converter starts skipping pulses), reduction in converter efficiency and increased heat dissipation *[65]*. Clearly there is tradeoffs and limitations in designing high frequency converter and is not considered as alternative means to achieve dc-link capacitor size reduction.

To achieve minimum energy storage research published in *[35]* uses the same carrier wave for the PWM signals of both the rectifier and inverter thus synchronizing the vector controlled switching. A reference signal from the load side is extracted and added to the output of the dc-link voltage controller. Now control action on the load side will immediately cause a change in the line side thus minimising the power fluctuation in the dc-link and thus the necessary capacitor size. An important suggestion given by this publication was the correlation between the dc-link capacitor size and the control and modulation methods used.

In 1994, the research works published by Wheeler *[36]* were based on a fully switched front- end rectifier and inverter to achieve power regenerative capability as well as a high power factor. This topology offers sinusoidal current extraction from the supply side at nearly unity power factor. This results in the PWM rectifier producing low ripple and the dc-link voltage rapidly responding to power reversal and this means that low energy storage is required in the dc-link. Unlike diode rectifier which requires a series inductor to control dc-link ripple this PWM rectifier topology does not require a series inductor. The above research links the size of the series inductor and dc-link capacitor to acceptable supply side harmonics, dc-link loop stability and transient response.

The dependencies of reactive components in the dc-link were established by *[38]*. An expression for the r.m.s values of the input current and voltage ripple as a function of reference signal were derived. The author suggests that the reference signal to drive the

modulation switching is a function of the load power factor. Also it is shown here that the r.m.s value of inverter input current doesn't depend on the shape of the reference signal. It is also suggested that the addition of harmonics other than the third into the sinusoidal reference signal is neither useful nor necessary.

In the area of multilevel converters the idea proposed in *[44]* relies on the injection of third harmonics in the output voltage of the inverter. The injection of third harmonics results in the production of second and fourth harmonic dc-link current components. The signal requires injection of a suitably computed third harmonic component in the output phase voltage to reduce second harmonics and thus additional control requirement at the cost of fourth harmonics. For the over-modulation region the dc-link harmonic components requires additional filtering. However the method presented here is only successful if the modulation is linear and thus it has limited application.

As noted above one of the major size deciding factors for the dc-link capacitor is the ripple current rating and voltage holdup time during power interruptions. Voltage ripple would automatically be reduced if the previous two conditions are satisfied and thus it is not a primary factor in sizing. In *[45]* Lipo et al. investigated a method to reduce the ripple current in a constant voltage/hertz pulse amplitude converter drive. The rectifier side ripple current contribution to the dc-link can be reduced by using a supply side reactor. The ripple current contribution in the dc-link from the inverter side is a function of the load angle and the modulation depth. Lipo et al suggested that a current source rectifier can be used to provide a buck function with unity power factor and a lower dc-link ripple. This also allows an alternative mode of controlling the drive with a combined pulse amplitude modulation and pulse width modulation. The reduction of dc-link voltage ripple and an increase in the modulation depth causes a change in the magnitude and distribution of harmonics and thus a decrease in the ripple current. A reduction in ripple current results in a reduction of the power loss in the capacitor.

A change in the switching pulse pattern and thus an optimisation of the modulation wave was suggested in *[46]* to control the dc-link harmonics with a view to reduce capacitor size without significantly increasing the dc-link voltage ripple. To better understand the selection of the dc-link capacitor and the relationship to dc-link harmonics a simplified equivalent model of the dc-link was used. A transfer function between dc-link voltage and current was established and a bode plot was plotted for different values of dc-link capacitor as shown below.

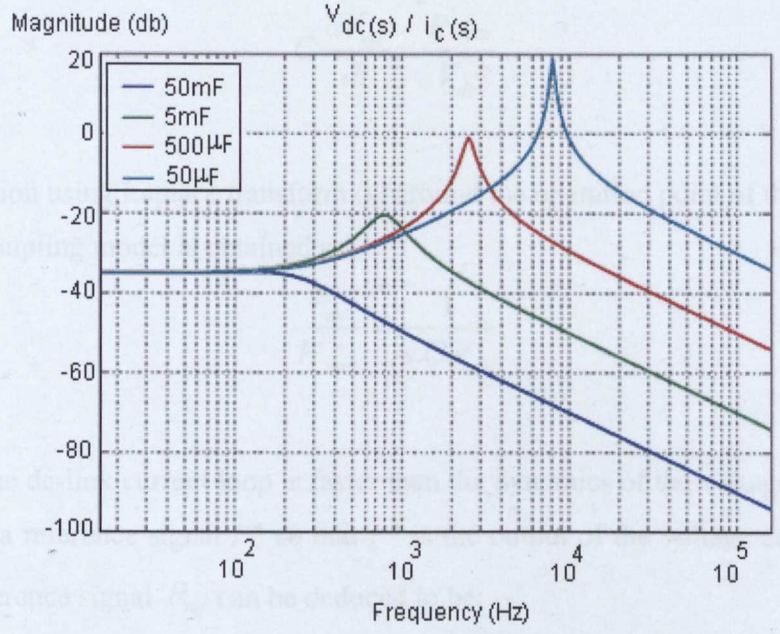


Fig.2.31 Effect of reducing dc-link cap on Bode diagram *[46]*

As the bode plot above shows, the magnitude at the resonant frequency increases as the dc-link capacitor is reduced. So in order to avoid the voltage ripple this range of unwanted harmonics has to be avoided. It means increasing the dc-link capacitor does not necessarily help to reduce the dc-link voltage ripple. This research uses selective harmonic elimination PWM (SHEPWM) that was used traditionally for phase voltage harmonic cancellation. The purpose of SHEPWM is to determine the optimal commutation sequence in order to cancel both dc-link current and voltage harmonics. This method also uses pre-estimation of the switching sequence in order to avoid resonance of the dc-link.

A study of the effect of load variation on the dc-link voltage was presented in *[47]* with an aim to reduce the dc-link capacitor. The idea was to compensate load variation via rectifier control so that the dc-link voltage becomes almost insensitive to it. As the dc-link voltage depends on the rectifier as well as the inverter commands, this study aims to decouple them by introducing a decoupling matrix as feed-forward control. The above mentioned decoupling control model was obtained as (Fig.2.21):-

$$i_c = C\frac{dV_{dc}}{dt} = i_{rect} - i_{dc} = \frac{P_{rect}}{V_{dc}} - i_{dc}$$

Introducing a new variable $P'_{rect} = P_{rect} - V_{dc}.i_{dc}$ to the equation above gives:

$$C\frac{dV_{dc}}{dt} = \frac{P'_{rect}}{V_{dc}}$$

After linearization using Laplace transform (s) around the operation point of the above equation a decoupling model is obtained as:

$$\frac{V_{dc}}{P'_{rect}} = \frac{1}{s.C.V_{dc}}$$

By assuming the dc-link current loop is faster than the dynamics of the voltage loop P'_{rect} can be replaced as a reference signal P^* so that P^* is the output of the voltage controller. So the decoupling reference signal P_{ref} can be deduced to be:

$$P_{ref} = P^* - V_{dc}.i_{dc}$$

A similar feed-forward signal derived from the machine controller is used by *[51]* to control the dc-link voltage in a VSI drive. Unlike linear controllers which cannot keep up with the dynamic transient nature of the dc-link voltage, this method uses predictive control with an active front end converter to allow a minimum dc-link capacitor. The dc-link voltage is predicted one step ahead and if it exceeds the desired value, the reference voltage vector of the rectifier is modified to keep the dc-link voltage within limits.

K.Nam et al. in *[48]* came up with an expression of the theoretical lower bound dc-link capacitor value in a converter-inverter drive system. The theoretical lower bound capacitance value is the one that prevents a voltage rise above a certain threshold value. The expression for this lower bound value is deduced based on the assumption that if power in and out of the dc-link is equal then the dc-link capacitor voltage will remain constant and would require minimum value capacitance. On equating the rectifier and inverter power an expression for capacitor current can be derived as a function of the d-q axis input and output currents:

$$i_{cap} = 1.5\frac{i_{d1}V_{d1} - i_{q2}V_{q2}}{V_{dc}}$$

A voltage compensation transfer function can be obtained from the above expression and the algorithm works out the minimum capacitor value required for all possible combinations of

converter/inverter duty cycle. Continuing their work in *[49]* the authors implemented the algorithm along with a feed-forward compensation term to null the capacitor current. Unlike existing methods, this method is intended to compensate the inverter current at the voltage node bypassing the current controller. This type of control requires a differentiator and offers much higher bandwidth with better dc-link regulation.

In *[50]* Saren et al. used over-modulation to increase the voltage output of the PWM converter. They suggested that a VSI with high over-modulation is less sensitive to dc-link fluctuation. Less dc-link fluctuation allows for lower line side current harmonics and thus a smaller dc-link capacitor.

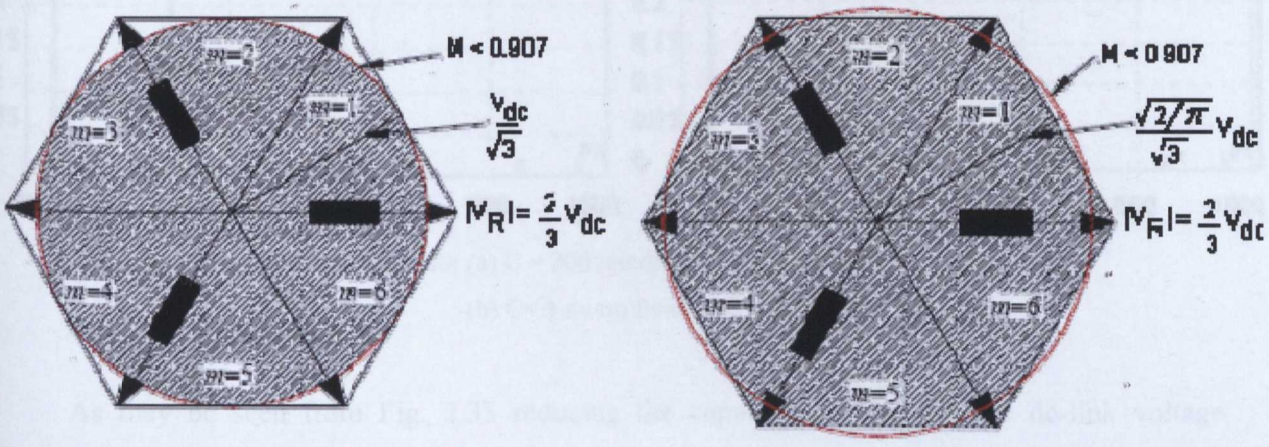


Fig.2.32 (a) Conventional modulation vectors (b) Over-modulation vectors *[50]*

Unlike conventional modulation as shown in Fig.2.32 (a), over-modulation allows for an increased stator voltage vector up to the maximum value but at the cost of a distorted reference signal. This maximum overvoltage follows a hexagon shape. In this constant amplitude over-modulation method the vector that is closest to the amplitude can be found from the angle of the vector from the middle of the space vector sector.

A small change in power electronic hardware was considered in *[52]* introducing a small metalized polypropylene film capacitor (MPFC). This change has a significant impact on frequency converter dynamics and the motor control algorithm. The small dc-link capacitor now doesn't require a pre-charge circuit but at the cost of increased line current harmonics. The effect of MPFC is shown in Fig. 2.33.

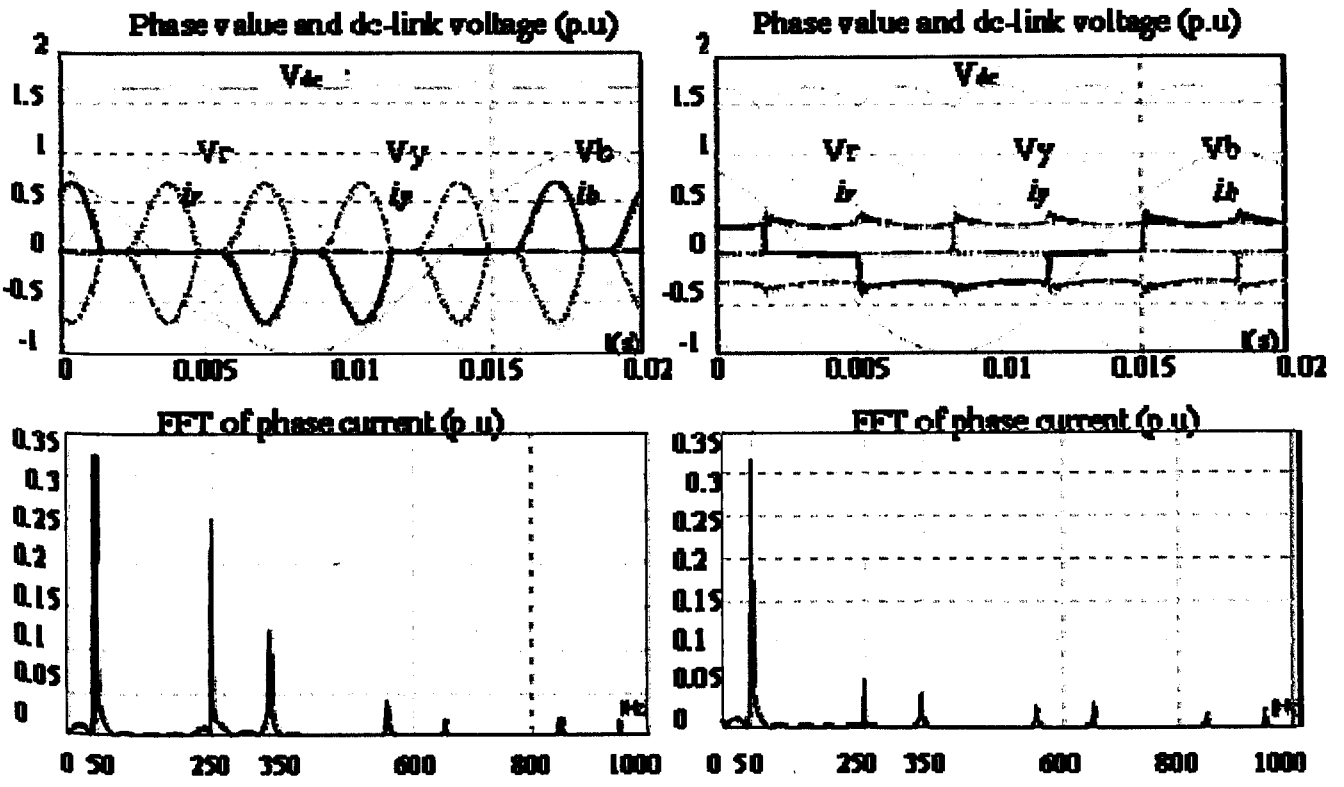


Fig.2.33. DC-Link performance for (a) C = 200 micro farad, AC side inductor = 4mH *[52]*
(b) C= 1 micro farad, AC side inductor = 0.4 mH

As may be seen from Fig. 2.33 reducing the capacitor means that the dc-link voltage fluctuation is increased but the line side current harmonics are improved. The dc-link fluctuation can be compensated by modulation using dc-link feedback control. The new modulation method used is a differential space vector pulse width modulation (DSVPWM) to allow better utilisation of the dc-link and faster converter control. The DSVPWM is suggested to be able to compensate heavily fluctuating voltages and produces the correct average voltage vector with high accuracy.

The drive of Fig.2.11 was proposed with an aim to achieve dc-link capacitor reduction with minimum change in the system hardware and control. It can be argued that the publications discussed before do not offer a complete solution to achieve small dc-link capacitor without asking for significant changes in system hardware and control. Techniques are suggested that allow complete dc-link elimination. They rely on a fix pulse pattern and therefore could not adapt for dc-link variations and that is why it would not be suitable for the application under consideration here. Much research work relies on eliminating the dc-link by using source side

filtering, but the source side filter is now doing the job for the dc-link capacitor and does not offer a low capacitor drive solution.
As discussed before another common method used for dc-link reduction is to have additional hardware to apply dc-link ripple cancellation. This additional control hardware is used to modify space vector modulation to modify IGBT pulse patterns. The scheme proposed in *[26]* was to modify the switching pattern based on switching function *SW* and dc-link voltage. The inverter voltage was then modified by applying counter modulation. This type of power balancing scheme was used in future in this research to gain significant dc-link reduction compared 20-30% achieved in *[26]*.

The dc-link current sensing for use in close-loop current control of front end rectifier were used in *[66]* and *[67]* to recreate three phase supply currents but it will be shown later in the thesis that why this can be relied upon for rectifier controller.

To achieve a very small dc-link capacitor a power balancing scheme could be assisted by a switch estimation logic which would predict the real time gate pulse status in both converters of Fig.2.11. The proposed balancing scheme for Fig.2.11 is similar in concept to the one presented in *[40]* where a small fraction of power is injected into the dc-link, but instead in the proposed method this would include a combined power difference contributed by the inverter and rectifier at the same time. The combined control would allow compensation for load as well as supply changes. Any other method for example harmonic injection and special control modulation methods were not considered in this research but rather effort is made to create a generic solution which could be applied to conventional systems without significant modification.

2.4 Conclusions

This chapter started by presenting background to the growing use of electrical actuation in aircraft and the latest research done in this area. This chapter went on to analyse different options for the various actuator drive applications and components such as actuator motor, converters and drive topologies. The chapter attempted to demonstrate that reducing the dc-link capacitance was a valuable goal in improving aircraft actuation systems size and weight. The contributions of this chapter are summarized below:

1) The introduction of this chapter provided brief introduction and differences between power-by-wire and fly-by-wire actuation technologies.

2) Further this chapter attempts to give an insight into the various types of actuation technologies (HA, EMA, EHA) and compare their merits and demerits.

3) A comparison of various motors was done to suit actuation specifications. From this it was shown that high lift surface actuation is now an application well suited to a totally electromechanical actuator and that this was a good target for the developments described in this thesis.

4) Based on fault tolerance and reliability requirements of actuator drives for high lift surfaces two main drive topologies – dc-link and matrix converter were presented and the dc-link drive configuration was proposed as a the best current solution. It was shown that a conventional multiphase inverter with a lower dc-link capacitance might match flight dispatch figures at lower size and cost than the fault tolerant architectures currently suggested.

5) Brief details of Matrix Converter technology option were presented and compared with conventional rectifier-inverter drives from which it was concluded that current reliability figures for matrix converters could not match the dc-link architecture.

6) The advantages of dc-link system were discussed and it was pointed out that the most unreliable and bulky part of the system are the capacitors in the dc-link.
7) Various previous research efforts to reduce the size of dc-link were discussed in detail.

8) Among all discussed techniques, the power balancing schemes offers a simple solution for reducing the dc-link but the previous research does not offer significant size reduction. A new power balancing scheme could be devised based on switch estimation control logic for drive specification of Table-2. The determination of switching status would offer better power balance around the dc-link and thus a much smaller capacitor. The control method proposed in brief here would allow a small dc-link capacitor in conventional drives with a small control modification.

CHAPTER 3

DESIGN, MODELLING AND SIMULATION OF A THREE-PHASE ACTUATOR DRIVE

3.1 Introduction

In order to be able to observe and analyze the parameters affecting the choice of the dc-link capacitor in an actuator drive, a detailed drive simulation model is necessary. This chapter will describe the modeling and simulation of a three phase AC-DC-AC drive for a mid-size commercial aircraft flap/slat actuator. A reduction in dc-link capacitance is likely to lead to the drive becoming unstable and this poses a risk to the converters and the rest of the drive system so as a first step it is clearly valuable to study proposed changes using a simulation. The major components of the actuator drive simulation need to include the actuator motor and its load, fully switching models of the inverter and rectifier converters and their controllers and finally the aircraft supply as shown in Fig.3.1.

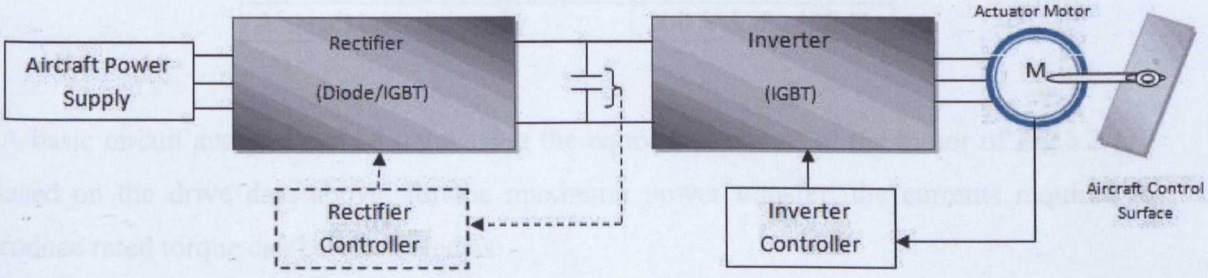


Fig.3.1 Basic structure of actuator control surface drive

Later in this chapter various alternatives of rectifier and the switching schemes used for the converter(s) will be discussed in detail with the simulation results. The chapter will conclude with a complete simulated model of a three-phase PMSM actuator dc-link inverter drive. The results from the simulation system will be compared in Chapter 4 with measurements taken

from a drive in operation. This provides a validation process for the simulation and allows confidence in the new drive schemes proposed and simulated in Chapter 5.

3.2 Actuator Motor Model Simulation

As discussed in Chapter.2, the advantages associated with permanent magnet synchronous motors make them the preferred choice for an aircraft control surface actuator. A mid-sized commercial aircraft like an Airbus 320 requires the flap to be fully extended or retracted within 30 seconds which corresponds to a peak power per flap of approximately 3.5 kW and a torque of 3.4k Nm (at the flap arm). This torque is supplied using a PMSM operating at a rated speed of 10,000 rpm via a step down gearbox *[16]*. The PMSM parameter selection for the above purpose is taken from *[16]* and is shown in Table.1:-

Table I
Actuator Drive Parameter

Motor power rating P_{mech}	3.6 kW
Rated speed ω_r	10000 rpm.
Rated torque T_e	3.4 Nm
Pole pair p	5
Stator resistance (per phase) R	0.156 Ω
Stator inductance (per phase) L	1.27 mH
Peak flux linkage ψ	0.0258 V-s
DC-Link voltage V_{dc}	460 V
Aircraft power supply	200 V L-L, 400 Hz

A basic circuit analysis can be done using the equivalent circuit of the motor of Fig.3.2 (a). Based on the drive data above, for the maximum power transfer, the currents required to produce rated torque can be calculated as:

$$T_e = \frac{3}{2}.p.(\psi.i) \tag{3.1}$$

So

$$i = \frac{3.4 \times 2}{3 \times 5 \times \sqrt{2} \times 0.0256} = 12.4\,\text{A}$$

The voltage drops in the motor phase windings (inductance and resistance) can be calculated as:

$$i \times L \times \omega_e = 12.42 \times 0.00127 \times (10000 \times 5 \times \pi/30) = 82.58 \text{ V}$$

$$i \times R = 12.42 \times 0.156 = 1.94 \text{ V}$$

The electrical speed ω_e of the machine is calculated from mechanical speed ω_m as:

$$\omega_e \text{ (rad/sec)} = \omega_m \times p \times (\pi/30)$$

The back e.m.f (E) generated by the PMSM at rated speed can be calculated as:

$$E = \omega_e \times \psi \tag{3.2}$$

$$E = (10000 \times 5 \times \pi/30) \times 0.0365 = 191.11 \text{ V}$$

The voltage required at the motor terminals to produce the motor's rated currents can hence be calculated as:

$$V = i.R + ji.L.\omega_e + E \tag{3.3}$$

The phasor diagram representation of the above equations is shown in Fig.3.2 (b).

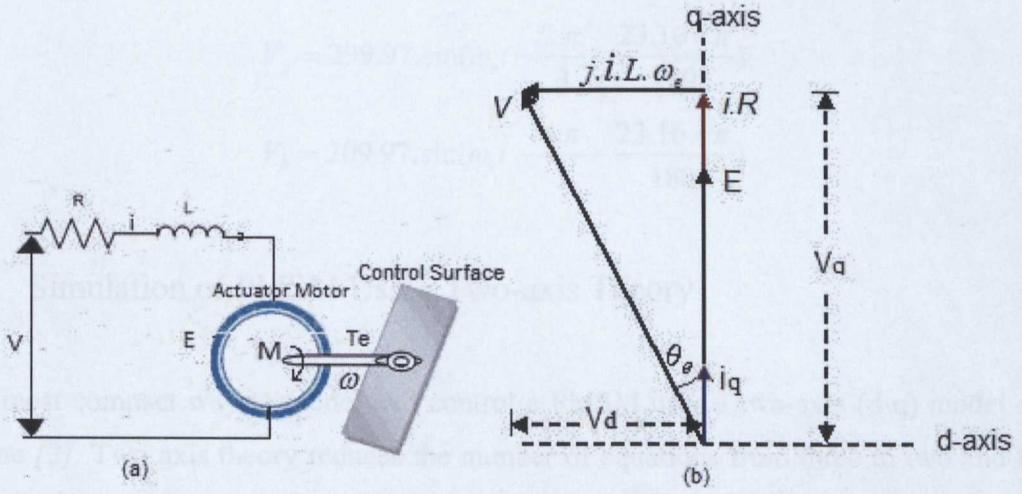


Fig.3.2 (a) Basic equivalent circuit representation of machine.
(b) Phasor diagram of PMSM machine under maximum power transfer condition.

The three-phase line currents & back e.m.f for the actuator motor model can be written as:

$$i_r = 12.42.\sin(\omega_e t) \tag{3.4}$$

$$i_y = 12.42.\sin(\omega_e t - \frac{2.\pi}{3})$$

$$i_y = 12.42.\sin(\omega_e t - \frac{4.\pi}{3})$$

And back e.m.f as:

$$E_r = 191.11.\sin(\omega_e t) \tag{3.5}$$

$$E_y = 191.11.\sin(\omega_e t - \frac{2.\pi}{3})$$

$$E_b = 191.11.\sin(\omega_e t - \frac{4.\pi}{3})$$

The load angle between the terminal and induced voltages can easily be calculated from the phasor diagram of Fig.3.2 (b) as $\theta = 23.16°$. The three-phase theoretical voltage required at the motor terminals to produce a torque of 3.4 Nm at 10000 rpm can easily been determined from phasor diagram of Fig.3.2(b) and eq.(3.3) as :-

$$V_r = 209.97.\sin(\omega_e t - \frac{23.16 \times \pi}{180}) \tag{3.6}$$

$$V_y = 209.97.\sin(\omega_e t - \frac{2.\pi}{3} - \frac{23.16 \times \pi}{180})$$

$$V_b = 209.97.\sin(\omega_e t - \frac{4.\pi}{3} - \frac{23.16 \times \pi}{180})$$

3.2.1 Simulation of PMSM Using Two-axis Theory

The most compact way to model and control a PMSM uses a two-axis (d-q) model of the machine *[2]*. Two axis theory reduces the number of equations from three to two and fixing the axes with respect to the magnet makes all parameters invariant with position even in the presence of saliency. In control terms the controlled variable is constant with time in the steady state and the response of the system is quasi-linear in the most common circumstance

where the speed varies far slower than the electrical quantities and magnetic saturation is not dominant. Two axis theory makes sinusoidal 1st harmonic only assumptions but these are not a severe approximation is the vast majority of machines. The rotor-reference frame d-axis and the q-axis voltage equations for a PMSM can be written as:-

$$V_d = i_d.\mathrm{R} + \frac{d\psi_d}{dt} - \omega_e.\psi_q \tag{3.7}$$

$$V_q = i_q.\mathrm{R} + \frac{d\psi_q}{dt} + \omega_e.\psi_d \tag{3.8}$$

Here ω_e is the "electrical speed" (in other words the rate of change of electrical angle) of the machine in *rad/s*.

The corresponding d-axis and q-axis flux linkages can be calculated as:

$$\psi_q = L_q.i_q$$

&

$$\psi_d = L_d.i_d + \psi$$

where ψ is the peak magnet mutual flux linkage of the PMSM. Implicitly the assumption is being made here that L_d, L_q and ψ are all constants i.e. there is no magnetic saturation. In the general sense this is not a good assumption and in this case the simplest procedure is to have maps of ψ_d and ψ_q against i_d and i_q. However in this particular case the target motor is a servomotor which is designed to have rather little saturation even at overload and hence the assumption is reasonably valid.

The voltages at the machine terminals are in the three-phase stator reference frame which needs to be transformed in to *d-q* axis voltages for the PMSM model using the following Clarke and Park transformations:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_r \\ V_y \\ V_b \end{bmatrix} \tag{3.9}$$

And

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} -\cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3.10}$$

The electrical angle θ_e of rotation for the PMSM model is determined from:

$$\theta_e = \int \omega_e . dt \tag{3.11}$$

The d-q axis voltages along with the speed information can be used to calculate the instantaneous *d-q* axis flux values using equations (3.7) and (3.8) as:

$$\psi_d = \int (V_d - i_d . R + \omega_e . \psi_q)\, dt \tag{3.12}$$

$$\psi_q = \int (V_q - i_q . R - \omega_e . \psi_d)\, dt \tag{3.13}$$

Now the resulting load currents (i_q , i_d) can be obtained using the inductances and magnet fluxes. Using the flux linkages as the electrical state variables is much more numerically stable than using the currents in this role when saturation is present and hence this model can be easily modified for use when saturation is more significant.

The electromagnetic torque produced from these current and flux values can now be written as:-

$$T_e = \frac{3}{2} . p . (\psi_d . i_q - \psi_q . i_d) \tag{3.14}$$

The current in the *d-q* rotor reference frame can be converted back to the three-phase stator frame using following reverse transformations.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \tag{3.15}$$

And

$$\begin{bmatrix} i_r \\ i_y \\ i_b \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.16}$$

The complete model of the PMSM based on the above equations using MatLab/Simulink is shown in Fig.3.3. Here it is assumed that the machine's leakage inductance is equal in the d

and q axes. Also it is assumed here that the induced back e.m.f profile of the motor is sinusoidal.

The mechanical arrangement of the test system on which these models are to be validated consists of two directly coupled servo drives, one acting as a motor and the other acting as a brake (i.e. generating). The shaft system is very stiff in comparison to the load it carries and hence the shaft angle between load and drive can be considered zero and the total inertia lumped into a single value. The speed to torque conversion within the PMSM model can then easily be done using the motor's dynamic equations as:

$$T_e = T_L + B.\omega_m + J.\frac{d\omega_m}{dt} \tag{3.17}$$

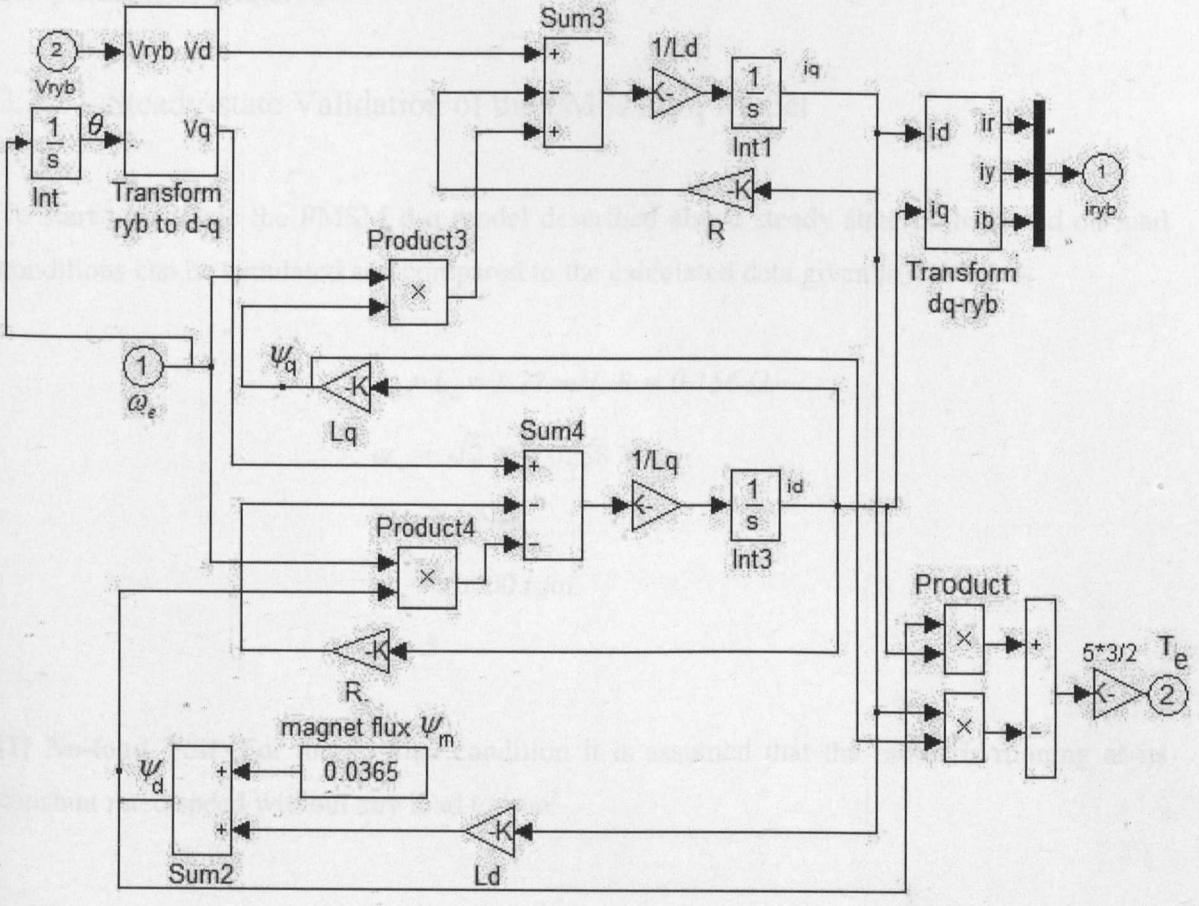


Fig.3.3. PMSM simulation model using two-axis (d-q) theory.

The simulated mechanical motor dynamics of eq. (3.17) is shown in the Fig.3.4.

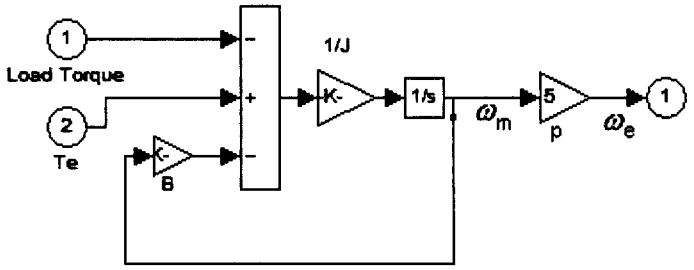


Fig.3.4. PMSM dynamic equation model.

In the case of a model for a full flap actuation system it is necessary to have a more complex mechanical model if sudden lock situations are to be considered but for this thesis such complexity is not required.

3.2.2 Steady-state Validation of the PMSM d-q Model

To start to validate the PMSM d-q model described above steady state no-load and on-load conditions can be simulated and compared to the calculated data given in Table.1 :-

$$L_d = L_q = 1.27\ mH,\ R = 0.156\ \Omega,$$

$$\psi_m = \sqrt{2} \times 0.0258\ \text{V s}$$

$$T_e = 3.4\ \text{Nm},$$

$$\omega_m = 10000\ \text{rpm}.$$

$$p = 5$$

[1] No-load Test: For the no-load condition it is assumed that the motor is running at its constant rated speed without any load torque:

$$i_q = i_d = 0$$

Using these conditions in the motor's flux equations (3.12-3.13) gives:

$$\psi_q = 0$$

And $\psi_d = \psi_m = 0.0365$ V s

The d-q axis voltages can be computed for the no-load condition using eq. (3.7-3.8) as:

$$V_d = 0$$

& $$V_q = \omega_e . \psi_d$$

$$V_q = 1047.2 \times 5 \times 0.0365$$

$$V_q = 191.1 \text{ V}$$

This voltage (V_q) is the back e.m.f of the actuator motor at no load and rated speed. Putting these flux and current values in equation (3.14) gives the torque output of the motor equal to zero as we expected for no load condition.

So $T_e = 0$ Nm

The simulation results are shown in Fig.3.5. In this simulation the model is run with the speed fixed with the initial values of the flux linkages set to zero. As may be seen the flux linkages and currents follow an initial transient before settling down to their expected constant values with $\psi_q = i_q = i_d = T_e = 0$ and $\psi_d = 0.0365$ Weber as per the earlier calculations thus successfully starting the verification process. The transient shown in Fig.3.5 is purely artificial because in real life the d axis flux linkage must have an initial value equal to the magnet flux but it does demonstrate that the simulation of the motor is stable as required.

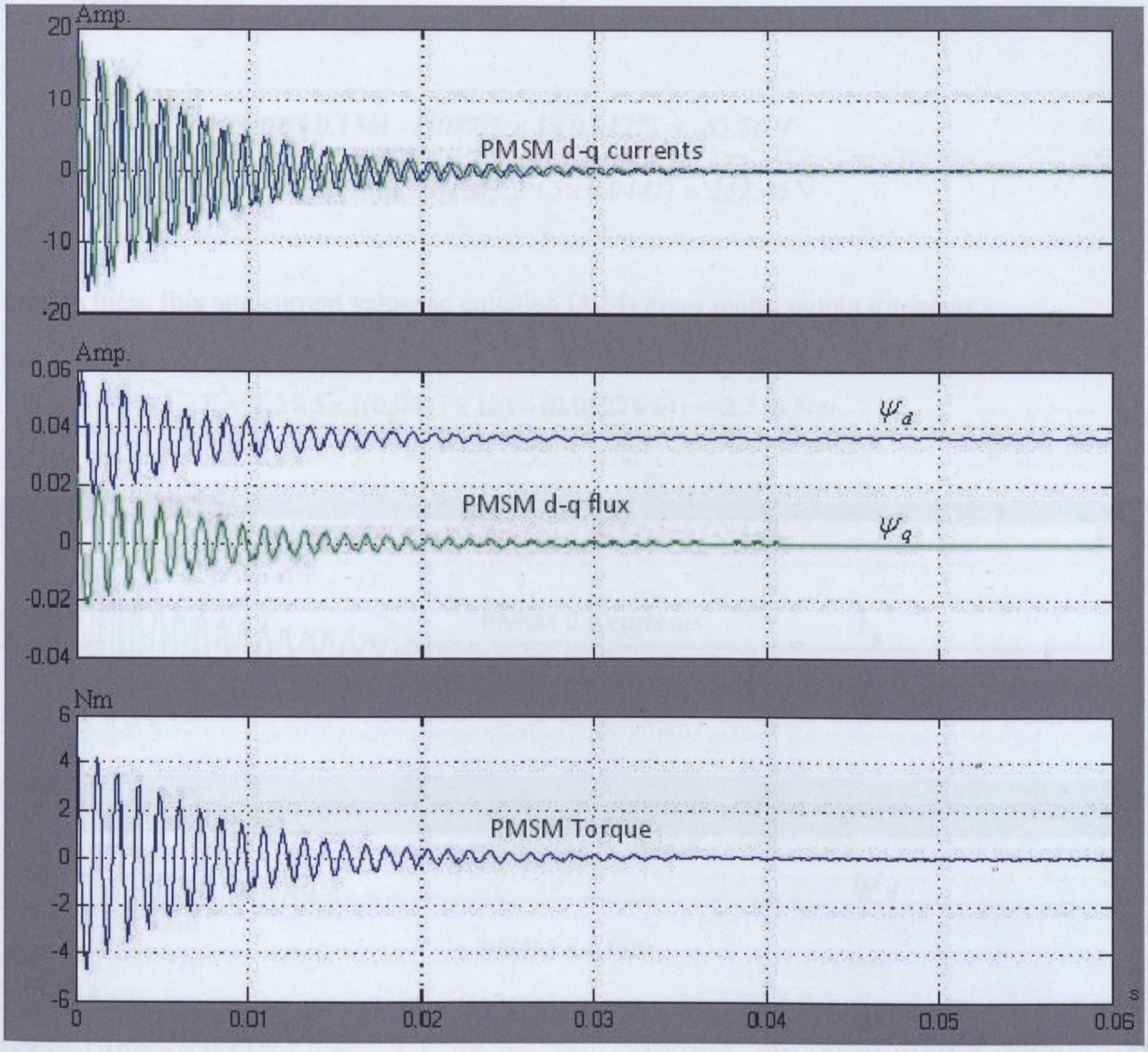


Fig.3.5 Current, flux and torque response of PMSM two-axis model for No-load test.

[2] Load Test – Here the intention is to set up a steady load case for which currents, flux linkages and torque can be easily calculated and compared to the simulated results. The load test is done with the PMSM running at its rated speed of 10000 rpm, and for the example case where the load current values are $i_d = 6$ A & $i_q = 10$ A. In the steady state the input d-axis and q-axis voltages required to produce these currents can be calculated using motor's flux equations - (3.12) & (3.13):

$$\psi_q = 0.00127 \times 10 = 0.0127 \text{ V s}$$

&

$$\psi_d = (0.00127 \times 6) + 0.0365 = 0.0441 \text{ V s}$$

The steady state d-q axis voltages can be calculated using motor's dynamic equations (3.7-3.8) as:

$$V_d = (6 \times 0.156) - (1047.2 \times 5 \times 0.0127) = -65.56 \text{ V}$$

$$V_q = (10 \times 0.156) + (1047.2 \times 5 \times 0.0441) = 232.46 \text{ V}$$

Putting these flux and current values in equation (3.14) gives motor output torque as:-

$$T_e = 1.5 \times 5 \times \{(0.0441 \times 10) - (0.0127 \times 6)\} = 2.736 \text{ Nm}$$

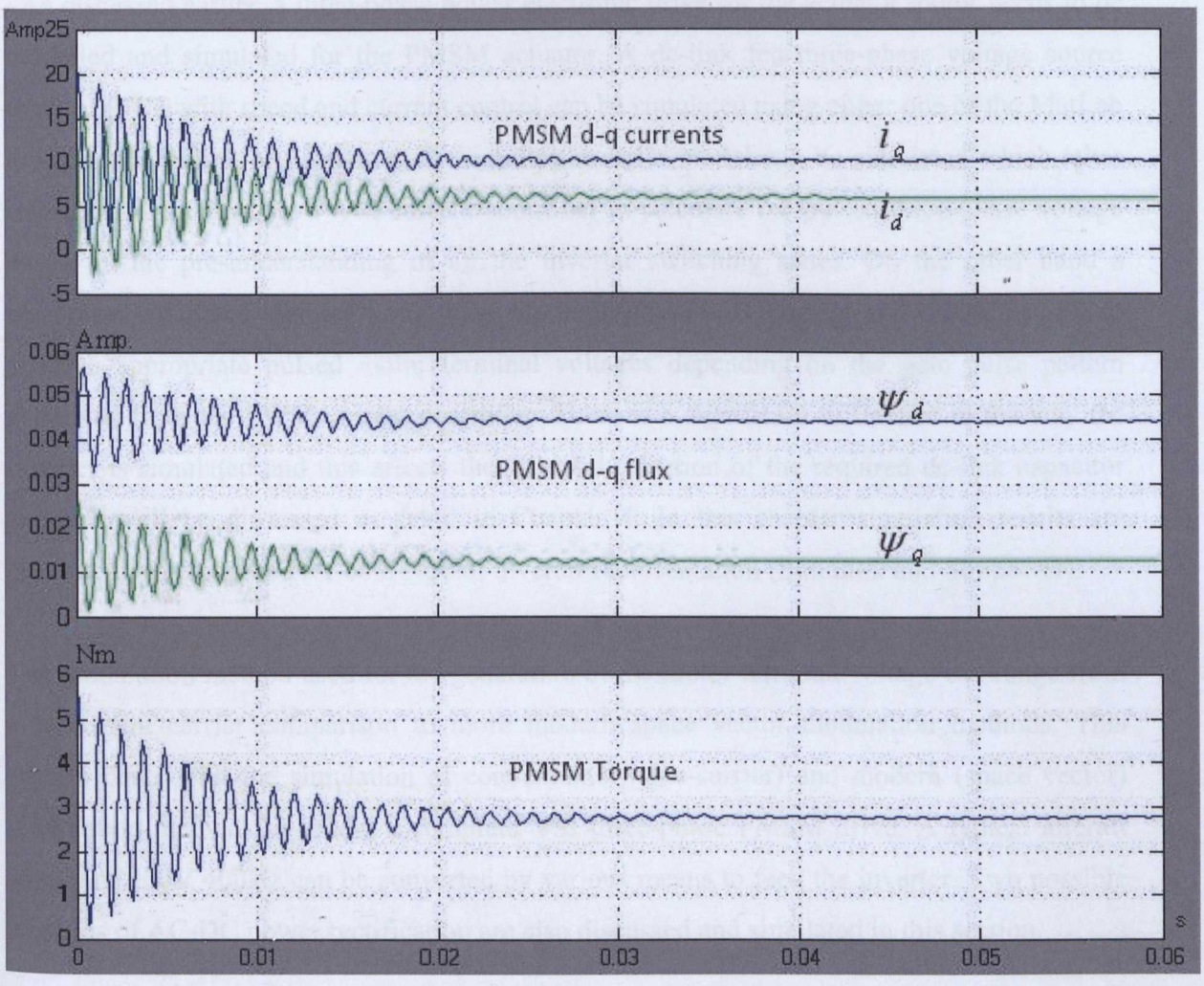


Fig.3.6 Current, flux and torque response of PMSM two-axis model for Load test.

The simulation is run with the calculated d and q axis terminal voltages and speed imposed on the model. The resulting current, flux and torque values from this simulation are shown in Fig. 3.6. As for the no-load case the initial values for the state variables ψ_d and ψ_q are zero

and hence the simulation must work through an initial transient to reach the steady state values of 0.0441 and 0.0127 Weber respectively are as per the calculated values above. The torque is also seen to match with the calculated value (2.736 Nm) as do the currents for direct and quadrature axes (6A and 10A). The comparisons above lend some confidence to the PM machine model and this allows the design/simulation of the PWM inverter and rectifier systems to supply this PM synchronous machine actuator.

3.3 Power Electronic Drive and Converter Simulation

As discussed earlier, a three-phase power electronic drive for the actuator motor needs to be modelled and simulated for the PMSM actuator. A dc-link fed three-phase voltage source inverter (VSI) with speed and current control can be simulated using either one of the MatLab toolboxes Simulink or Simpower. A Simulink inverter model can be simulated which takes reference input from the PWM current controller to calculate the pulsed three-phase voltage based on the pre-understanding of all the inverter switching states. On the other hand a Simpower simulated inverter would have the three-phase IGBT bridge and should be able to produce appropriate pulsed motor terminal voltages depending on the gate pulse pattern generated from the PWM current controller. There is a significant difference in the way the inverter is simulated and this affects the size and selection of the required dc-link capacitor and this will be discussed in detail in Chapter 4. In this chapter simulation results are presented and compared for both type of inverter representation (Simulink and Simpower).

The modulation method used for the generation of the motor terminal voltage can range from a basic sine-carrier comparison to more modern space vector modulation methods. This section deals with the simulation of conventional (sine-carrier) and modern (space vector) modulation methods to model a complete VSI three-phase PMSM drive. A typical aircraft supply of 200V 400Hz can be converted by various means to feed the inverter. Two possible methods of AC-DC power rectification are also discussed and simulated in this section.

3.3.1 Simulation of Three-phase Inverter for an Actuator Motor Drive

3.3.1.1 Three-phase Simulink Inverter Simulation

The basic principle of voltage source inverters (VSI) is to convert a DC voltage to an AC voltage of variable frequency and amplitude. Each leg of a standard three-phase VSI consist of two series connected IGBTs with back to back reverse recovery diodes. The input DC voltage is obtained by rectification of the available aircraft three-phase ac supply. The circuit diagram of a three-phase inverter connected to the equivalent circuit of the actuator motor is shown in Fig.3.7.

The three-phase bridge is supplied by a dc-link voltage V_{dc} using a dc-link filter capacitor. The actuator motor is considered to be star connected so the sum of the three stator currents is zero:

$$i_r + i_y + i_b = 0$$

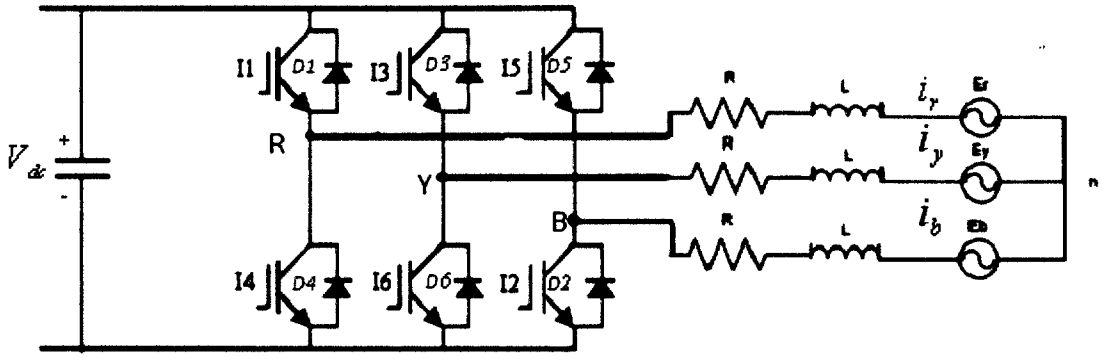


Fig.3.7. Three-phase equivalent circuit of IGBT Inverter connected to PMSM equivalent circuit.

In Fig3.7 the IGBTs are shown as $I_1, I_2 \ldots I_6$ and the corresponding diodes are $D_1, D_2 \ldots\ldots D_6$. In order to avoid any short circuits in the inverter, both the switches in any one leg cannot be turned "on" at the same time, thus the nature of the switches in any one leg is complimentary.

So

$$I_1 + I_4 = 1 \tag{3.18}$$

$$I_3 + I_6 = 1 \tag{3.19}$$

$$I_5 + I_2 = 1 \tag{3.20}$$

To produce the desired output load currents, these 6 IGBTs need to be switched in a specific manner. To simulate the inverter using Simulink, it is very important that there is an exact knowledge of all of the possible switching combinations of the IGBTs. Depending on the way the three phases are connected to the positive and/or negative dc-link rails there are 8 switching combination of the IGBTs that are possible. So for example if phase R is connected to the positive dc-link rail and phase Y & B are connected to negative rail then the inverter state is termed ''100''. The 8 possible combinations of IGBTs with the corresponding phase-neutral voltages are shown in Fig.3.8. As can be seen in Fig.3.8 two of the inverter states produce zero AC line voltage and the line currents freewheels through either the upper or lower IGBTs.

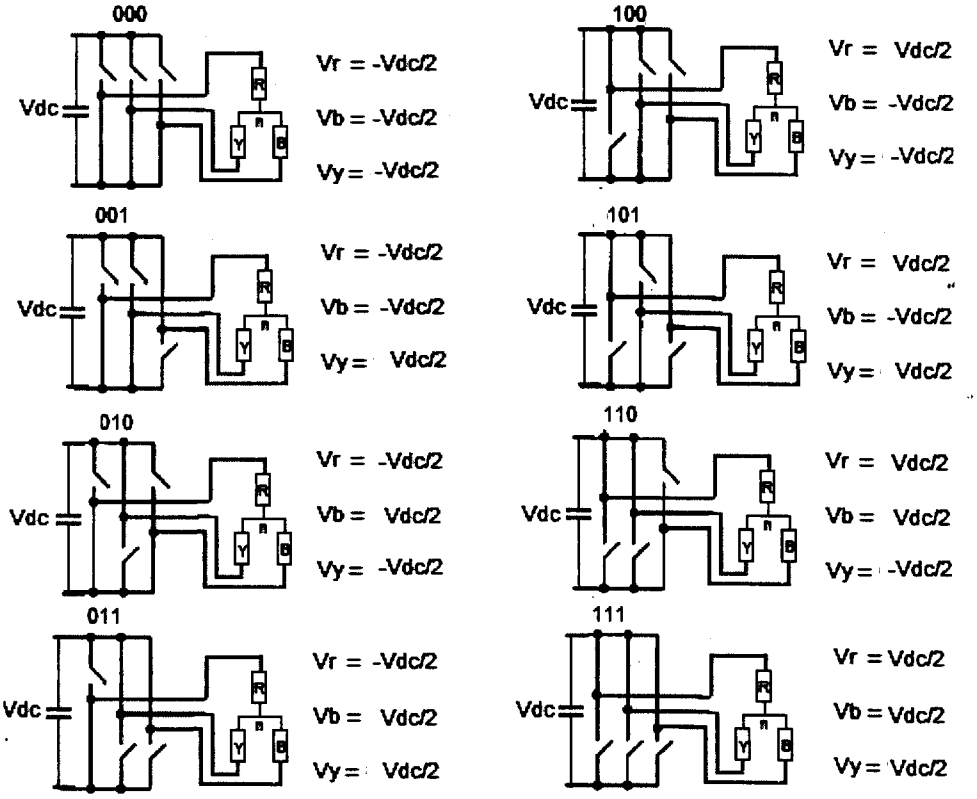


Fig.3.8. Inverter switching states

It is important to note here that for simulation purpose the existing switch model in Simulink does not consider dead times and current takeover from one switch to other is instantaneous. The selection of the inverter states, in order to generate a specific terminal voltage, is ensured by the modulation technique and equations (3.18-3.20). The state dependent terminal voltages can now be represented as:

$$V_r = \frac{V_{dc}}{2}(I_1 - I_4) \tag{3.21}$$

$$V_y = \frac{V_{dc}}{2}(I_3 - I_6) \tag{3.22}$$

$$V_b = \frac{V_{dc}}{2}(I_5 - I_2) \tag{3.23}$$

Sine-Carrier Modulation: To generate the above voltages, the modulator compares the three-phase signal of the desired frequency with a high frequency carrier signal. The two signals produce a high for the time when the reference signal is higher than the carrier wave and vice versa. This phenomenon is generally known as pulse-width modulation and will be discussed in detail later. A three-phase inverter Simulink simulation for a carrier modulation method is shown in Fig.3.9.

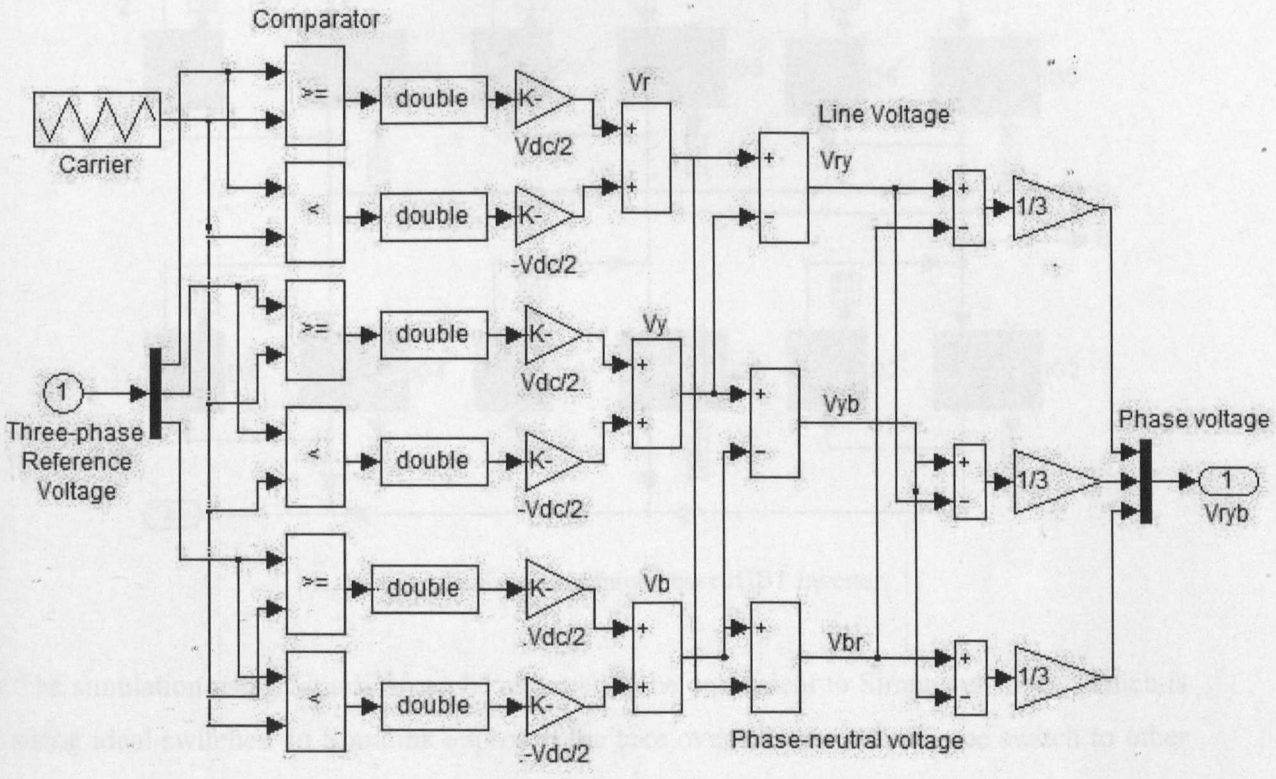


Fig.3.9. Simulink sine-carrier PWM Inverter simulation for generating motor terminal voltage.

For comparison purpose the simulation results of this inverter model will be presented later with the Simpower inverter simulation results.

3.3.1.2 Simpower Inverter simulation

As discussed earlier the inverter shown in Fig.3.7 can also be simulated using Simpower. The complimentary switch relationship of equations (3.18)-(3.20) still needs to be satisfied and the switching states of Fig.3.8 still holds true but this time not necessarily in the same sequence as before. The three-leg inverter simulated using Simpower uses 6 IGBTs and 6 diodes blocks which are inbuilt in the Simpower library. To generate the PWM output voltage, these IGBTs needs to be supplied with appropriate gate pulses. The IGBT gate pulses can be generated in similar fashion to the Simulink model (Fig.3.9) by comparing a high frequency carrier with the reference voltage of the current controller. But this time instead of calculating the phase-neutral voltages, the output voltages are generated by switching the individual IGBTs in the inverter.

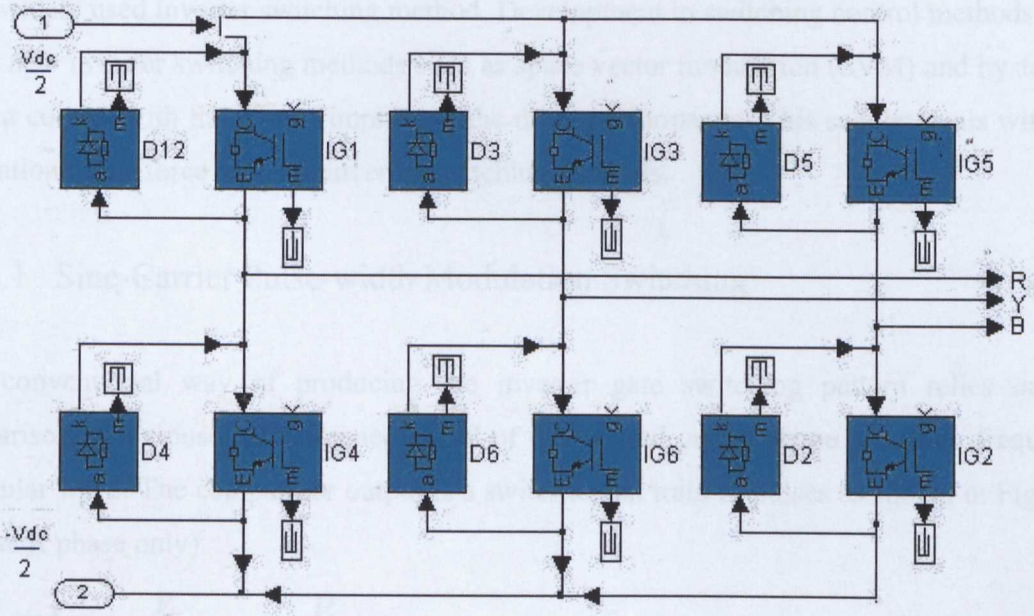


Fig.3.10 Simpower three-phase IGBT Inverter.

The simulation using Simulink can be assumed to be equivalent to Simpower model which is using ideal switches. In Simulink approach the take over of current from one switch to other will be in zero time as there is no device impedance. On the other hand in Simpower approach there will an overlap during current commutation from one device to other as the device model consist of impedance in series. For these reasons the simulation results of Simulink and Simpower can not match. A three-phase VSI simulated using inbuilt switching devices from

MatLab/Simpower library is shown in Fig.3.10. The Simpower default parameters for the IGBTs and the diodes are tabulated below:

IGBT Parameters:-	Diode Parameters:-
Resistance= 0.01 Ω	Resistance= 0.02 Ω
Inductance= 1e-6 H	Inductance= 0 H
Forward Voltage= 1 *V*	Forward Voltage= 0.8 *V*
Current 10% fall time= 1e-6 s	
Current Tail Time= 2e-6 s	

3.3.2 Simulation of Inverter Control Switching

Simple six-step inverters offer inferior performance at low speeds and this had led to the development of pulse width modulation (PWM) techniques. Currently the PWM system is the most widely used inverter switching method. Development in switching control methods have led to new inverter switching methods such as space vector modulation (SVM) and hysteresis current control with the aim of improving the drive performance. This section deals with the simulation of the three possible inverter switching methods.

3.3.2.1 Sine-Carrier Pulse-width Modulation Switching

This conventional way of producing the inverter gate switching pattern relies on the comparison of a sinusoidal reference signal of the desired output shape to a high frequency triangular wave. The comparator output is a switched flat train of pulses as shown in Fig.3.11 (for the R phase only).

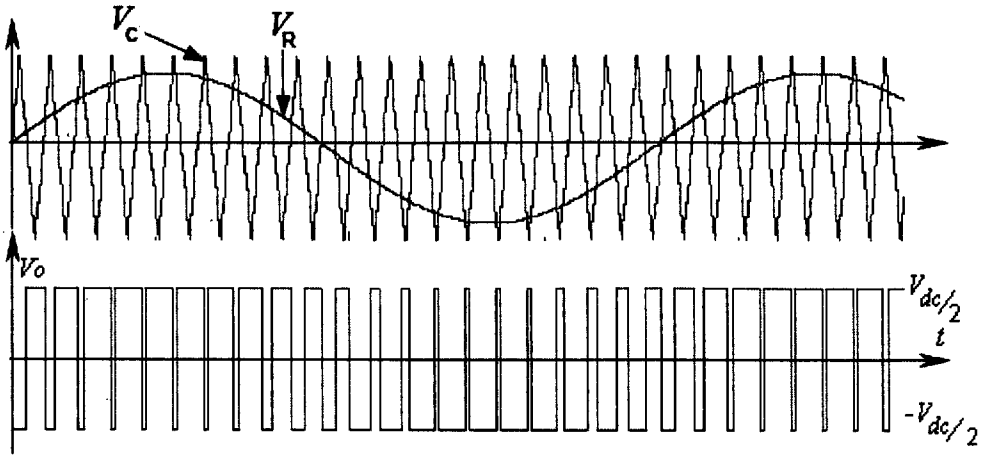


Fig.3.11 Carried based Pulse Width Modulation (Bipolar)

The amplitudes of the carrier triangular wave V_c and reference wave V_R determine the amplitude of the fundamental inverter output V_o. The fundamental frequency of the output is the same as that of the reference signal V_R. The output voltage V_o is nothing but the reference signal V_R converted into a set of high frequency pulses, the frequency of which is decided by the frequency of the carrier signal V_c.

As shown in the Fig3.11 the inverter output line voltage is governed as:

- When $V_R \geq V_c$, *then* $V_o = V_{dc} / 2$

- When $V_R \leq V_c$, *then* $V_o = -V_{dc} / 2$

Where V_{dc} is the dc-link voltage. Now if the amplitude of the carrier signal V_c is "A_c" and the amplitude of the reference signal V_R is "A_r" then the modulation depth of the PWM can be calculated as:

Modulation depth $$M = \frac{A_r}{A_c} \tag{3.24}$$

& the amplitude of the fundamental inverter output V_o is given by:

$$V_o = M . \frac{V_{dc}}{2} \tag{3.25}$$

For a dc-link voltage input measurement of V_{dc} = 460 V, and taking a carrier wave of amplitude A_c = 450 V then to achieve a fundamental output peak of V_o = 209.97 V (as per equation (3.6) the modulation depth can be calculated using equation (3.25) as:

$$M = \frac{2.V_o}{V_{dc}} = 0.91$$

So

$$A_r = A_c . M$$

$$A_r = 450 \times 0.91$$

$$A_r = 410.8 \text{ V}$$

Thus the ideal reference required to produce the 209.97 V peak fundamental inverter output (equation 3.6) can be calculated using equation (3.24) as:

Or
$$V_{R.r} = 410.8.\sin(\omega_e t - \frac{23.16 \times \pi}{180}) \tag{3.26}$$

$$V_{R.y} = 410.8.\sin(\omega_e t - \frac{2.\pi}{3} - \frac{23.16 \times \pi}{180})$$

$$V_{R.b} = 410.8.\sin(\omega_e t - \frac{4.\pi}{3} - \frac{23.16 \times \pi}{180})$$

The sine-carrier comparison pulse-width modulation logic of Fig.3.11 is simulated and shown in Fig.3.12 and this is used to give 6 gate pulses for the 6 IGBTs of the inverter. Note that the comparison of phase-R reference with V_c will result in the gate pulse for I_1 (Fig.3.10) and the negative phase-R reference comparison will result in gate pulse for I_4 to ensure their complimentary switching pattern.

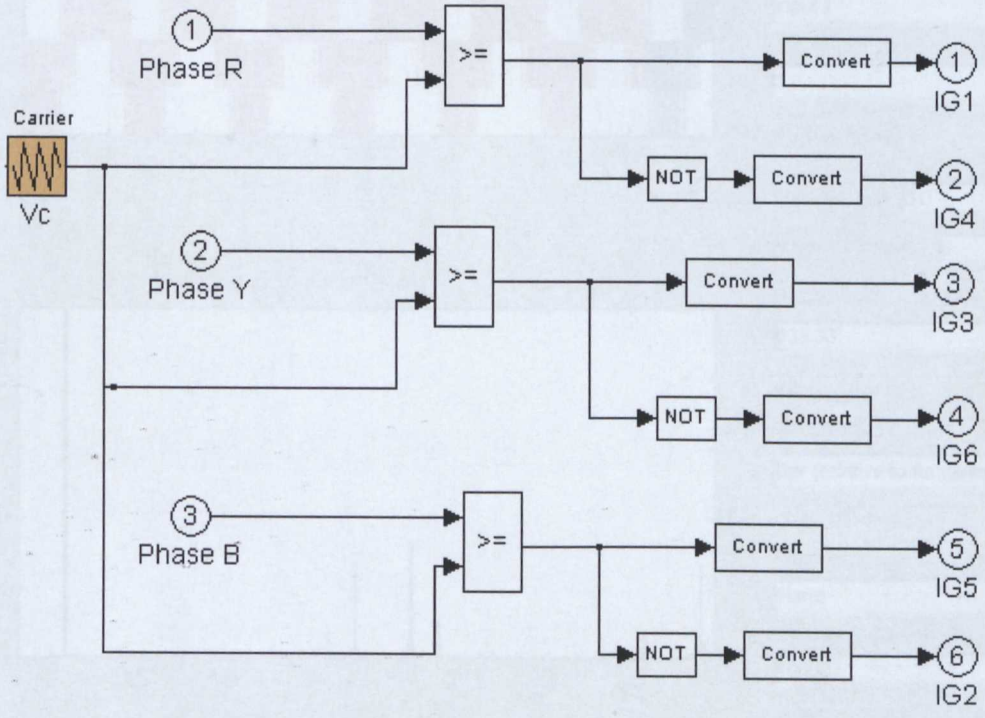


Fig.3.12. Carrier based PWM gate pulse generation simulation

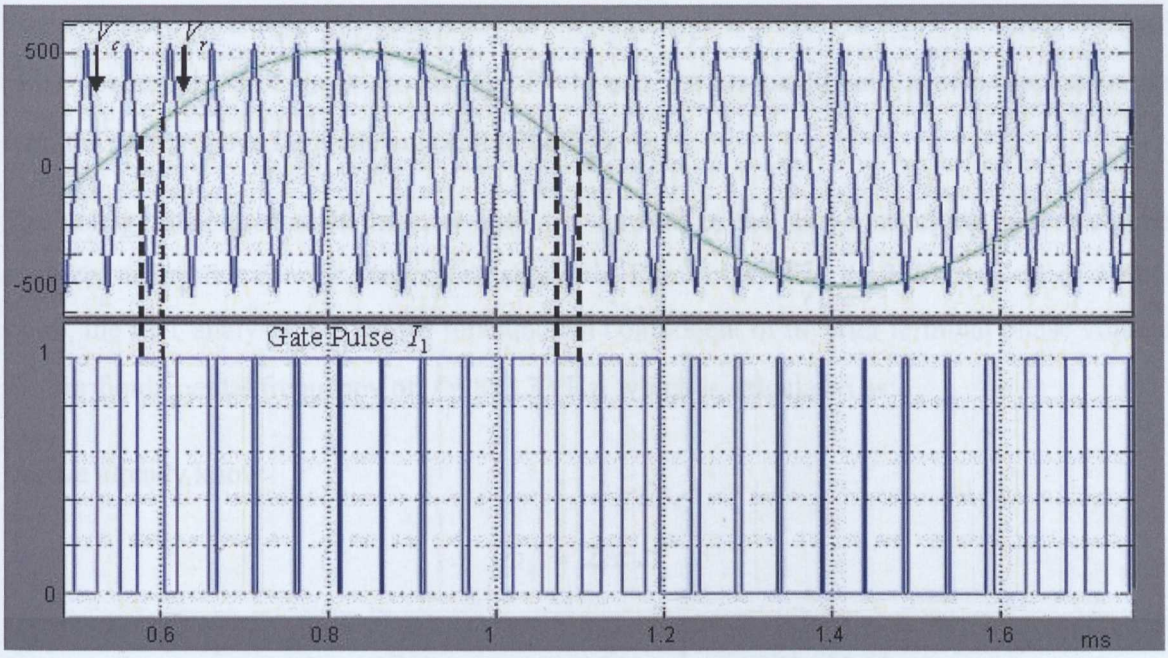


Fig.3.13. Gate pulse generation using carrier based PWM simulation

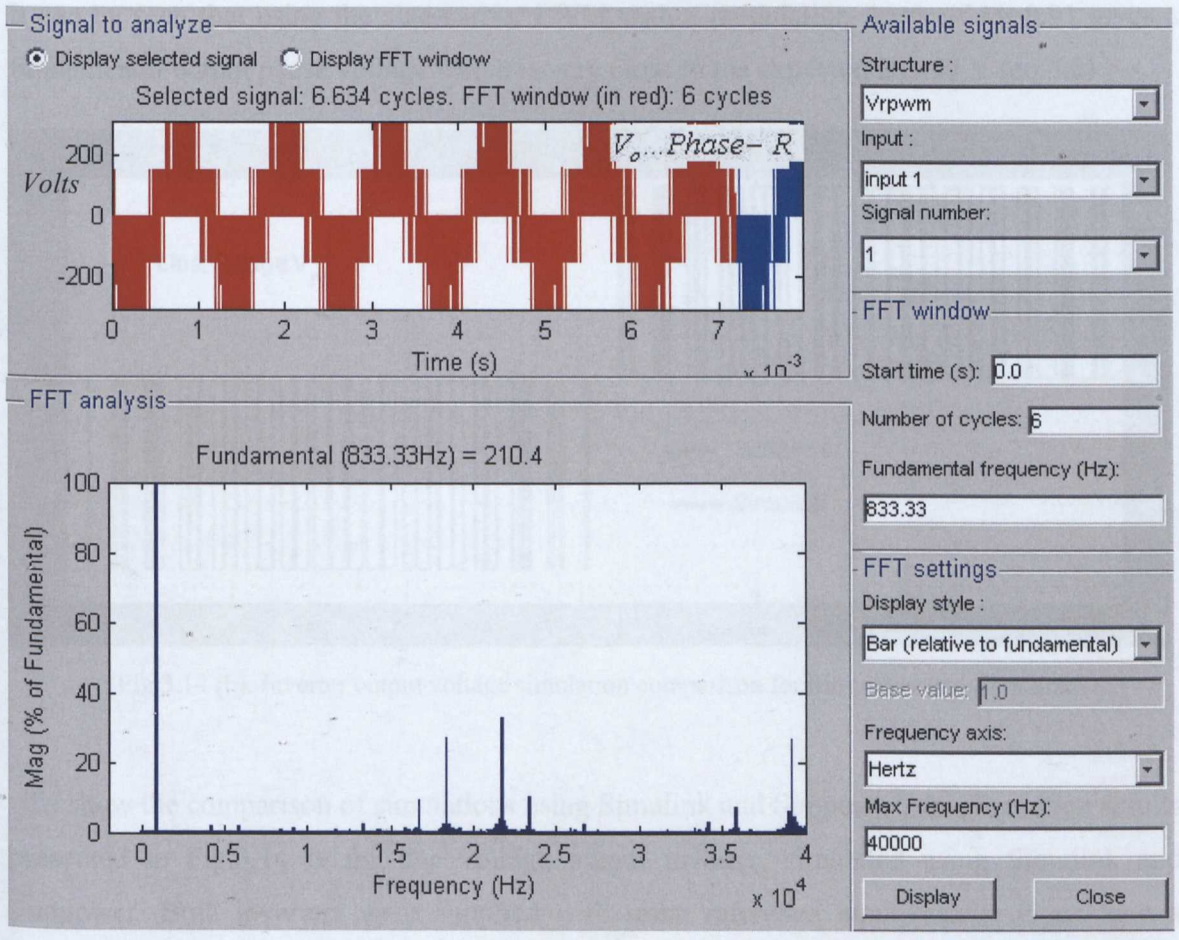


Fig.3.14(a). Fast Fourier analysis of the output inverter voltage (phase-R) for sine-carrier PWM

The simulated results for this carrier based PWM scheme is shown in Fig.3.13 where the gate pulse generation for I_1 is as shown. The PWM scheme discussed here is of a bipolar nature with the carrier wave frequency chosen to be 20 kHz.

The voltage generated at the inverter output as a result of the above switching pattern can be analyzed using fast-fourier analysis as shown in Fig.3.14(a). For the motor speed of 10000 r.p.m, the FFT analysis is done for fundamental component of inverter terminal phase voltage V_r for fundamental frequency of f= 833.33 Hz, which is calculated as:

As we already know

$$\omega_e = 2.\pi.f$$

So $$f = 10000 \times 5 \times (\pi / 30)\frac{1}{2.\pi} = 833.33\,Hz$$

It can be seen that using the sine-carrier PWM with a modulation depth of M=0.91 gives a fundamental output phase voltage which is very close to the expected 209.97 V (eq.3.6).

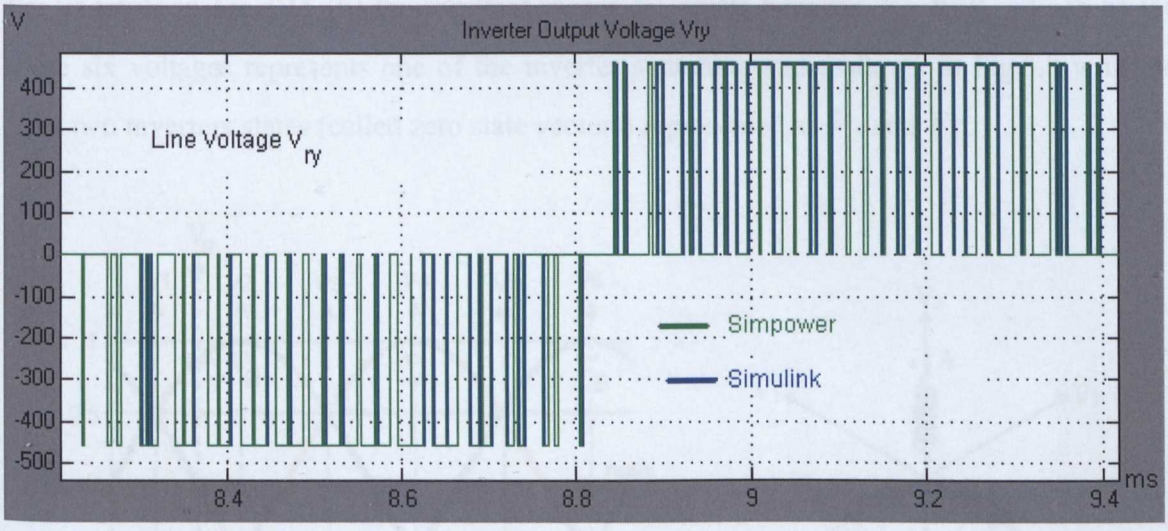


Fig.3.14 (b). Inverter output voltage simulation comparison for Simpower and Simulink

To show the comparison of simulations using Simulink and Simpower, the simulation results presented in Fig.3.14 is for line voltage output inverter, simulated using Simulink and Simpower. Both inverters were supplied with same reference input, carrier signal and a constant dc-link voltage input supplying identical resistive load. It is clear that the voltage pulse from Simpower is delayed from the one from Simulink.

3.3.2.2 Space Vector Modulation Switching

Unlike the previously discussed sine-carrier pulse-width modulation, the space vector modulation (SVM) does not have separate modulators for each phase. In this more recent method of modulation a single reference vector is used to determine the switching states of the inverter bridge. When the three-phase windings of an AC machine are fed with balanced three-phase currents, it produces three flux vectors oriented along their respective winding's axis. The magnitude of these three vectors alternates but the magnitude of the resultant rotating flux vector remains constant.

To explain the generation of the resultant voltage vector, consider a three-phase balanced set of voltage shown in Fig.3.15 (a) applied to the stator winding of Fig.3.15 (b). The three-phase waveform of Fig.3.15 (a) can be considered, as if it consists of six instances when one of the phase voltages has positive or a negative peak. The voltages at these instants are named as V_1 to V_6 and are known as the active vectors. At any instant the resultant voltage vector V_R could be anywhere between or upon these six individual vectors.

For example in Fig.3.15 (b) the resultant vector V_R exists between V_1 & V_2. Each of the these six voltages represents one of the inverter switching states shown in Fig.3.8 with the final two inverters states (called zero state vectors) represented as V_7 and V_8.

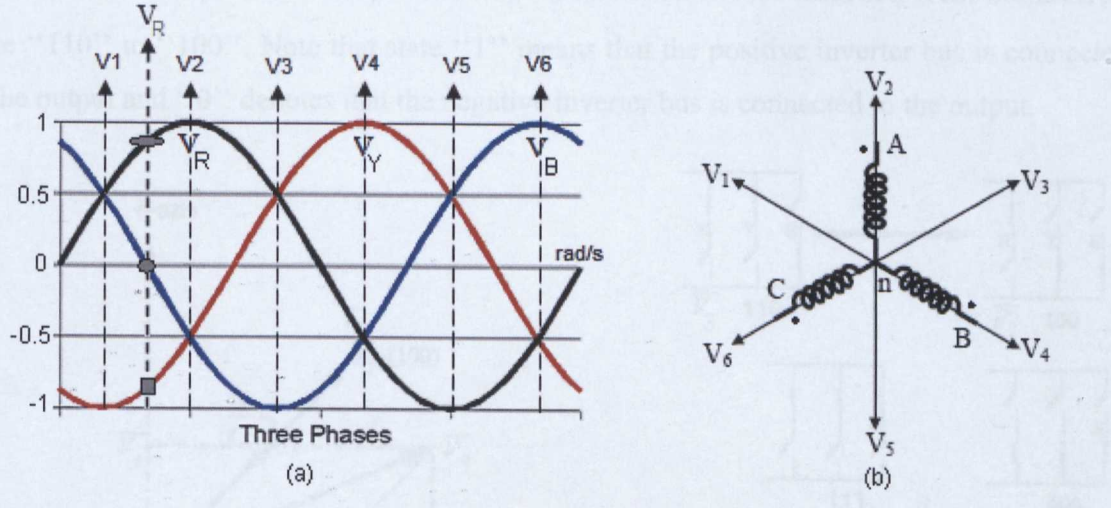


Fig.3.15. Principle of Space Vector Modulation

Fig.3.15(a) shows a three-phase balanced motor terminal voltage and in this ideal case the resultant space vector moves in space with constant magnitude and frequency. However due

to the switching nature of the inverter, the voltage space vector changes its direction abruptly in multiples of 60 electrical degrees. The active vectors V_1 to V_6 have a magnitude of V_{dc} / 2 and point along a fix direction, the zero vectors (V_7 and V_8) on the other hand have zero magnitude. Fig.3.16 shows the voltage space vector plane with the zero vectors at the centre of the hexagon.

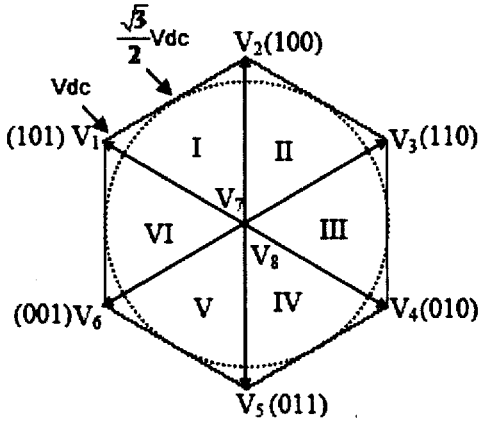


Fig.3.16 Voltage space vector hexagon

The resultant space vector V_R can be expressed as a resultant of two adjacent vectors V_3 & V_2 (of duration t_1 & t_2 respectively) which are in line with the nearest active and zero vectors of a particular sector in the SVM hexagon as shown in Fig.3.17 for sector-II. In this case the resultant space vector V_R is rotating in an anticlockwise direction from the inverter state ''110'' to ''100''. Note that state ''1'' means that the positive inverter bus is connected to the output and ''0'' denotes that the negative inverter bus is connected to the output.

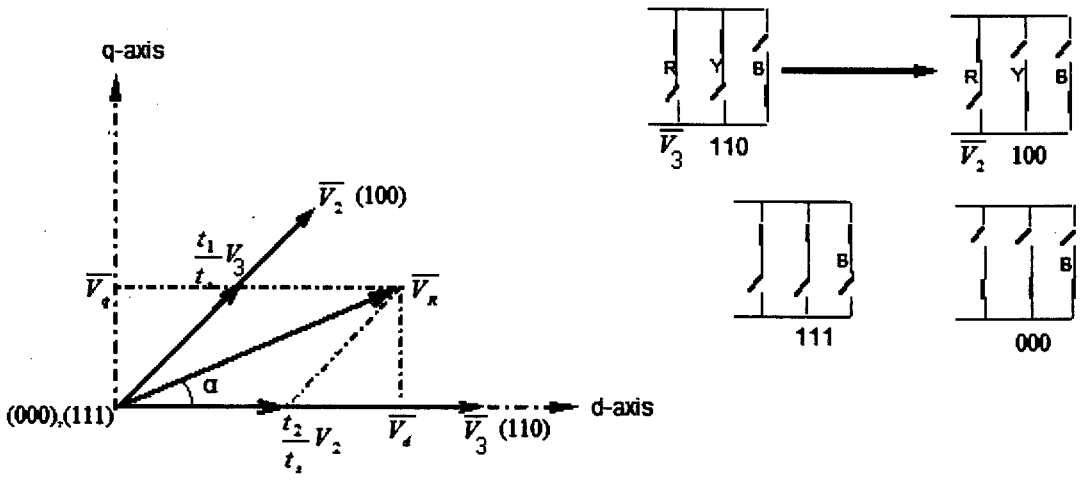


Fig.3.17 Principle of space vector calculation and switching states for sector-II

In the SVM hexagon there is a limit to the absolute length of the resultant vector. If the resultant vector lies along an active vector, it has a magnitude equal to the dc-link voltage V_{dc} as shown in the Fig.3.16. However the maximum amplitude of the output voltage is limited to the circle within the hexagon which is:

$$\overline{V}_{Line-Line.\max} = V_{dc}.\cos\ 60^{o} = \frac{\sqrt{3}}{2}.V_{dc} \tag{3.27}$$

(Modulation depth $M_{\max}$ =1)

So the corresponding limit in the phase voltage is:

$$\overline{V}_{phase.\max} = \frac{2}{3}.\overline{V}_{Line-Line.\max} = \frac{1}{\sqrt{3}}.V_{dc} \tag{3.28}$$

At any particular instant the resultant reference vector can be expressed as in Fig.3.17:

$$\overline{V_R} = \frac{t_1}{t_s}\overline{V}_3 + \frac{t_2}{t_s}\overline{V_2} \tag{3.29}$$

Here t_s represents the duration of one PWM cycle. To determine the exact position of the resultant space vector $\overline{V_R}$, it is very important to calculate the real-time angular position of $\overline{V_R}$ with respect to the nearby active vector. As shown in Fig.3.17, to find the angle α, $\overline{V_R}$ can be decomposed in d-q components such as:

$$\left|\overline{V_R}\right| = \sqrt{\overline{V_q}^2 + \overline{V_d}^2} \tag{3.30}$$

And so,

$$\alpha = \tan^{-1}\left|\frac{V_q}{V_d}\right| \qquad (0 \le \alpha \le 60^{o}) \tag{3.31}$$

The time of the application (t_1, t_2) of the active vectors and the zero voltage vectors (t_7, t_8) can be calculated from Fig.3.17 as:

$$t_1 = \frac{|V_R|}{|V_3|}.t_s.\frac{\sin(\frac{\pi}{3}-\alpha)}{\sin(\frac{\pi}{3})} \tag{3.32}$$

$$t_2 = \frac{|V_R|}{|V_2|}.t_s.\frac{\sin(\alpha)}{\sin(\frac{\pi}{3})} \tag{3.33}$$

& so $$t_0 = t_7 + t_8 = t_s - t_1 - t_2 \tag{3.34}$$

Here t_7 & t_8 are the duration of the zero vectors and their inverter states are (111) & (000) respectively. The above calculation was done considering only sector-II of the SVM hexagon, the expression for the switching durations for any sector (say the n^{th}) can be derived as:

$$t_1 = \frac{|V_R|}{|V_3|}.t_s.\frac{\sin(\frac{\pi}{3}-\alpha+(\frac{n-1}{3}).\pi)}{\sin(\frac{\pi}{3})} \tag{3.35}$$

& $$t_2 = \frac{|V_R|}{|V_2|}.t_s.\frac{\sin(\alpha-(\frac{n-1}{3}).\pi)}{\sin(\frac{\pi}{3})} \tag{3.36}$$

& again $$t_0 = t_7 + t_8 = t_s - t_1 - t_2$$

Where, n varies from 1 to 6 for the relevant SVM hexagon sectors. The real-time values of sector n can be found using the Simulink model shown in Fig.3.18.

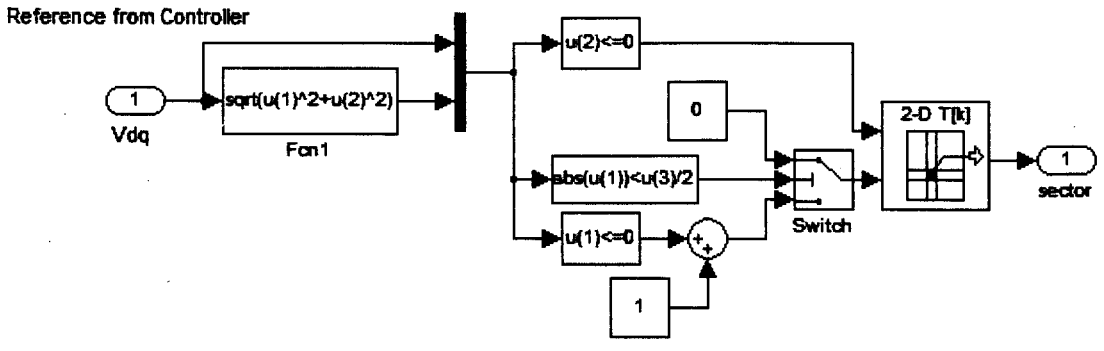


Fig.3.18 Sector value calculation from reference signal

The above discussed calculation of the time durations of the active and zero vectors is shown in the Simulink model of Fig.3.19.

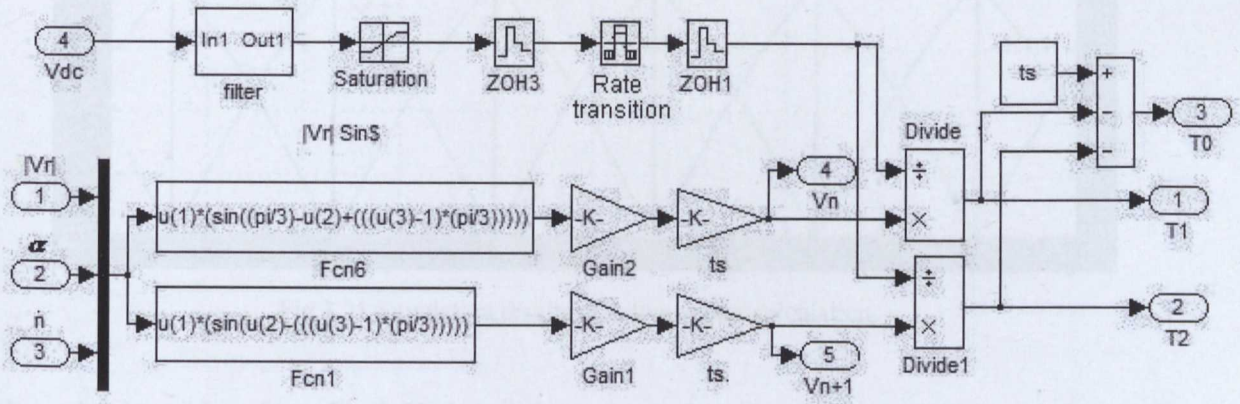


Fig.3.19.Switching duration calculator for SVPWM cycle.

Simulation results of the switch durations for ideal reference input of equation (3.26) are shown in Fig.3.20.

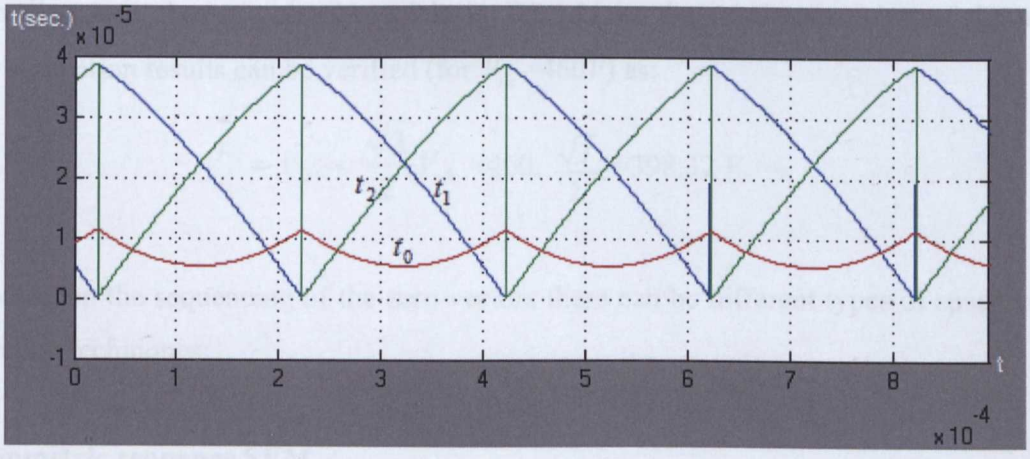


Fig.3.20. Switching duration simulation results for SVM.

The use of ''Zero order hold (ZOH)'', ''Rate transition'' and ''Delay'' blocks throughout the thesis is purely to eliminate simulation errors which appear due to different sample times (for inner and outer control loop) and continuous states of various parameters.

The instantaneous vector simulation result for the ideal reference input of equation (3.26) is shown in Fig.3.21.

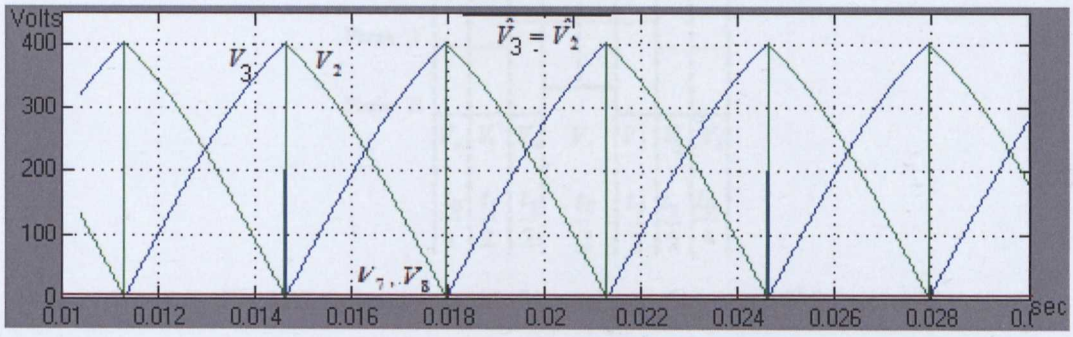


Fig.3.21 Simulation results of active vector calculation.

It is clearly evident from Fig.3.21 that at the instant when the resultant vector goes from one hexagon sector to another, there is an abrupt change in its active vector magnitude. For example in Fig.3.16 when the resultant vector V_R lies on the vector V_3, the instantaneous value of vector V_2 is zero. When the resultant vector V_R rotates 30^o towards vector V_2, the instantaneous values of the active vectors becomes $V_R = V_3 = V_2 = \frac{\sqrt{3}}{2}.V_{dc}$ and so on. The pattern discussed above is clearly visible in Fig.3.21 as the maximum value of the active vector simulation results can be verified (for V_{dc}=460V) as:

$$\hat{V}_3 = \hat{V}_2 = \frac{\sqrt{3}}{2}V_{dc} = 460.\ \frac{\sqrt{3}}{2}. = 398.37\ V.$$

Depending on the sequencing of the zero vectors there can be different types of space vector modulation techniques:

[1] Symmetric sequence SVM

This is the standard SVM switching method and it has symmetry in the switching waveform i.e. zero vectors (V_7 or V_8) before and after the active vector sequence as shown in Fig.3.22 for sector-II for the three phases (R,Y,B). The individual vector durations are calculated in the same manner as discussed above using equations (3.32)-(3.34).

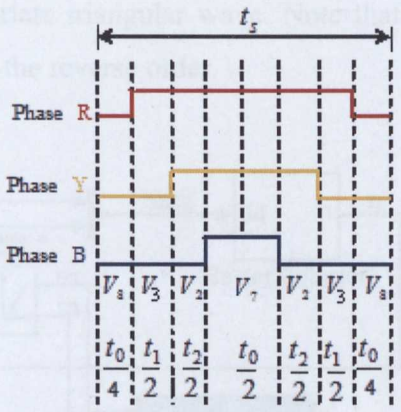


Fig.3.22 Switching pattern for symmetric sequence SVM sector-II

Based on the above switching pattern, the switching duration of each of the devices (I_1 to I_6) for sector-II can be calculated as:

$I_1 = t_1 + t_2 + \frac{t_0}{2}$	$I_4 = \frac{t_0}{2}$
$I_3 = t_2 + \frac{t_0}{2}$	$I_6 = t_1 + \frac{t_0}{2}$
$I_5 = \frac{t_0}{2}$	$I_2 = t_1 + t_2 + \frac{t_0}{2}$

The above switching states can be put into matrix form for each of the six sectors of the SVM hexagon. By selection of the appropriate sector the reference vector can also be calculated as:-

$$\overline{V_R} = \frac{t_1}{t_s}\overline{V_3} + \frac{t_2}{t_s}\overline{V_2} + \frac{t_0}{t_s}(\overline{V_7} + \overline{V_8}) \tag{3.37}$$

Or in matrix form as:

$$[V_R] = [\frac{t}{t_s}].[V] \tag{3.38}$$

The complete simulation model of the symmetrical sequence SVM for all six sectors with a three-phase SVM reference generation signal is shown in Fig.3.23. The switching pulses of the above calculated duration can easily be generated by comparing this three-phase SVM

reference signal to an appropriate triangular wave. Note that in every next PWM cycle the switch pattern repeats itself in the reverse order.

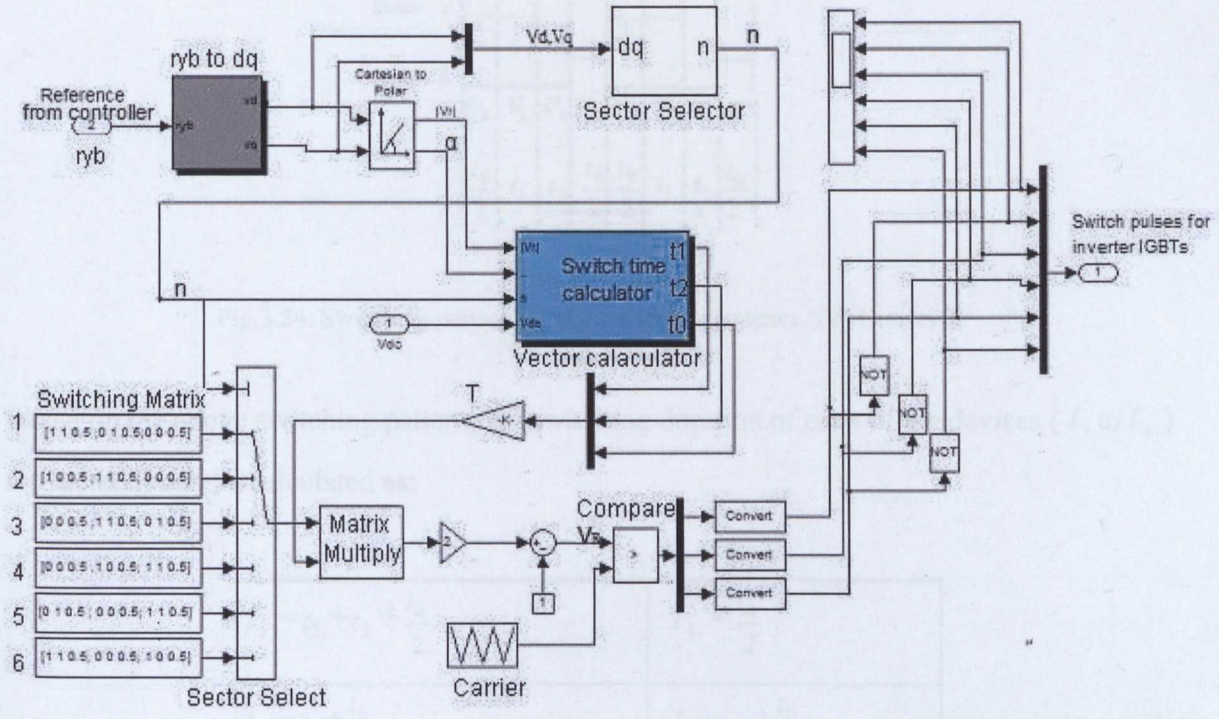


Fig.3.23 Symmetric sequence SVM switching generation

[2] Right Aligned Sequence SVM

Like the previously discussed symmetrical SVM, the right-aligned sequence SVM also has zero vectors (V_7 or V_8) arranged before and after the active vectors(V_1 - V_6) but unlike the symmetric sequence SVM this right-aligned SVM does not repeat itself in the reverse order in the next modulation cycle instead the sequence is repeated in exactly the same order. The right-aligned sequence SVM gate pulse pattern is shown in Fig.3.24 for sector-II for all three phases (R, Y, B). The individual vector durations are calculated in the same manner as previously discussed using equations (3.32)-(3.34).

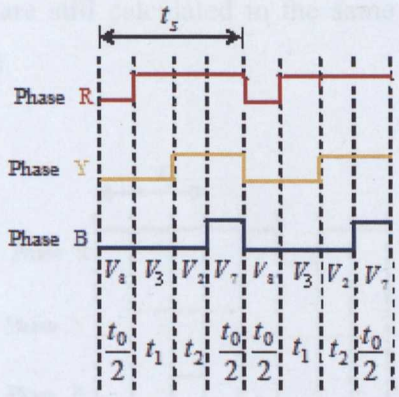


Fig.3.24. Switching pattern for right-aligned sequence SVM sector-II

Based on the above switching pattern, the switching duration of each of the devices (I_1 to I_6) for sector-II can be calculated as:

$I_1 = t_1 + t_2 + \frac{t_0}{2}$	$I_4 = \frac{t_0}{2}$
$I_3 = t_2 + \frac{t_0}{2}$	$I_6 = t_1 + \frac{t_0}{2}$
$I_5 = \frac{t_0}{2}$	$I_2 = t_1 + t_2 + \frac{t_0}{2}$

Note that the IGBT time durations for this SVM are the same as that of the symmetric-sequence SVM but now there are only 4 commutation states in any PWM cycle. The above switching states can be put into matrix form for each of the six sectors of the SVM hexagon and by the selection of the appropriate sector the reference vector can be calculated using equation (3.38).

[3] Alternating Zero Vector Sequence SVM

As the name suggest in this type of SVM method the zero vectors (V_7 or V_8) are used alternatively in adjacent cycles so that the effective frequency is halved The alternating zero sequence SVM pulse pattern is shown in Fig.3.25 for sector-II for all three phases (R,Y,B).

Individual vector durations are still calculated in the same manner as discussed previously using equations (3.32)-(3.34).

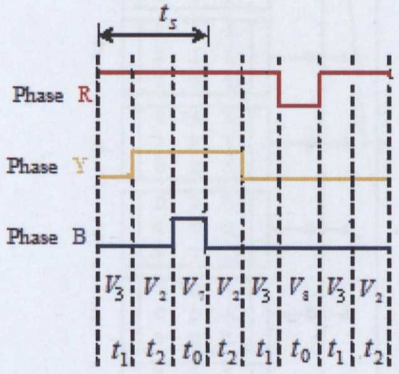


Fig.3.25 Switching pattern for Alternating Zero Vector Sequence SVM for sector-II

Based on the above switching pattern, the switching duration of each of the devices (I_1 to I_6) in the inverter bridge for sector-II can now be calculated as:

$I_1 = 2(t_1+t_2)+t_0$	$I_4 = t_0$
$I_3 = 2t_2+t_0$	$I_6 = 2t_1+t_0$
$I_5 = t_0$	$I_2 = 2(t_1+t_2)+t_0$

The above switching states can be put into matrix form for each of the six sectors of the SVM hexagon and by the selection of the appropriate sector the reference vector can be calculated using equation (3.38).

The SVM reference generation simulation remains the same as Fig.3.21 except for the way the switch timing is calculated as shown in Fig.3.26.

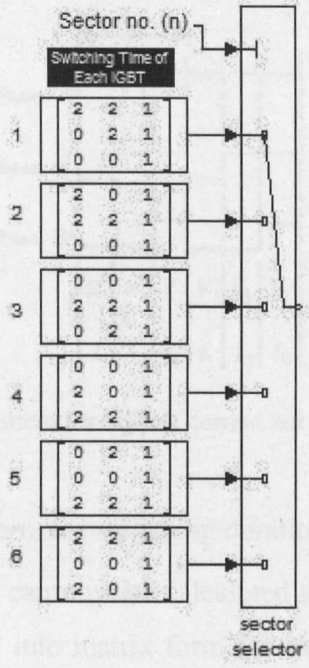


Fig.3.26 Switching timing calculation for Alternating Zero Vector Sequence SVM

[4] Highest Current Not Switched Sequence SVM

Device switching losses in the inverter are the most significant losses in the inverter. These losses are directly related to the current flowing through the switching device. Hence it may be argued that by avoiding the switching of the inverter leg that is carrying the highest current the switching losses might be reduced.

The ''highest current not switched SVM'' type of modulation method is based on the above argument of avoiding switching the phase which carries the highest current with the aim to reduce switching losses. This can be implemented because every adjacent active vectors (V_1 to V_6) differ in only device state. Hence by using only one zero vector (V_7 or V_8) within a given switching sequence of a particular sector, one of the legs doesn't have to be switched at all. The switching sequence pattern of this type of SVM is shown in Fig.3.27 for sector-II for all three phases (R,Y,B). The individual vector durations are still calculated in the same manner as discussed previously using equations (3.38).

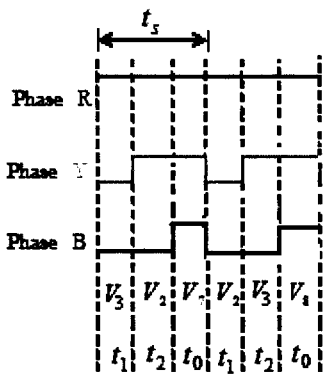
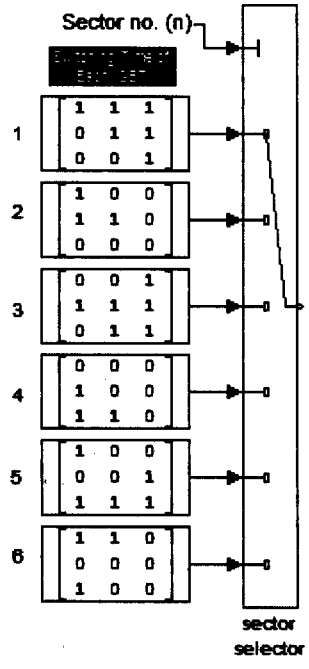


Fig.3.27. Switching pattern for highest current not switched SVM for sector-II

Based on the above switching pattern, the switching duration of each of the devices (I_1 to I_6) in the inverter bridge for sector-II can now be calculated and this is shown in Fig 3.28. The above switching states can be put into matrix form for each of the six sectors of the SVM hexagon and by the selection of the appropriate sector the reference vector can be calculated using equations (3.32) & (3.34). The SVM reference generation simulation remains the same as in Fig.3.21 except for the way the switch timing is calculated as shown in Fig.3.28.



$I_1=t_1+t_2+t_0$	$I_4=0$
$I_3=t_2+t_0$	$I_6=t_1$
$I_5=t_0$	$I_2=t_1+t_2$

Fig.3.28 Switching timing calculation for highest current not switched SVM

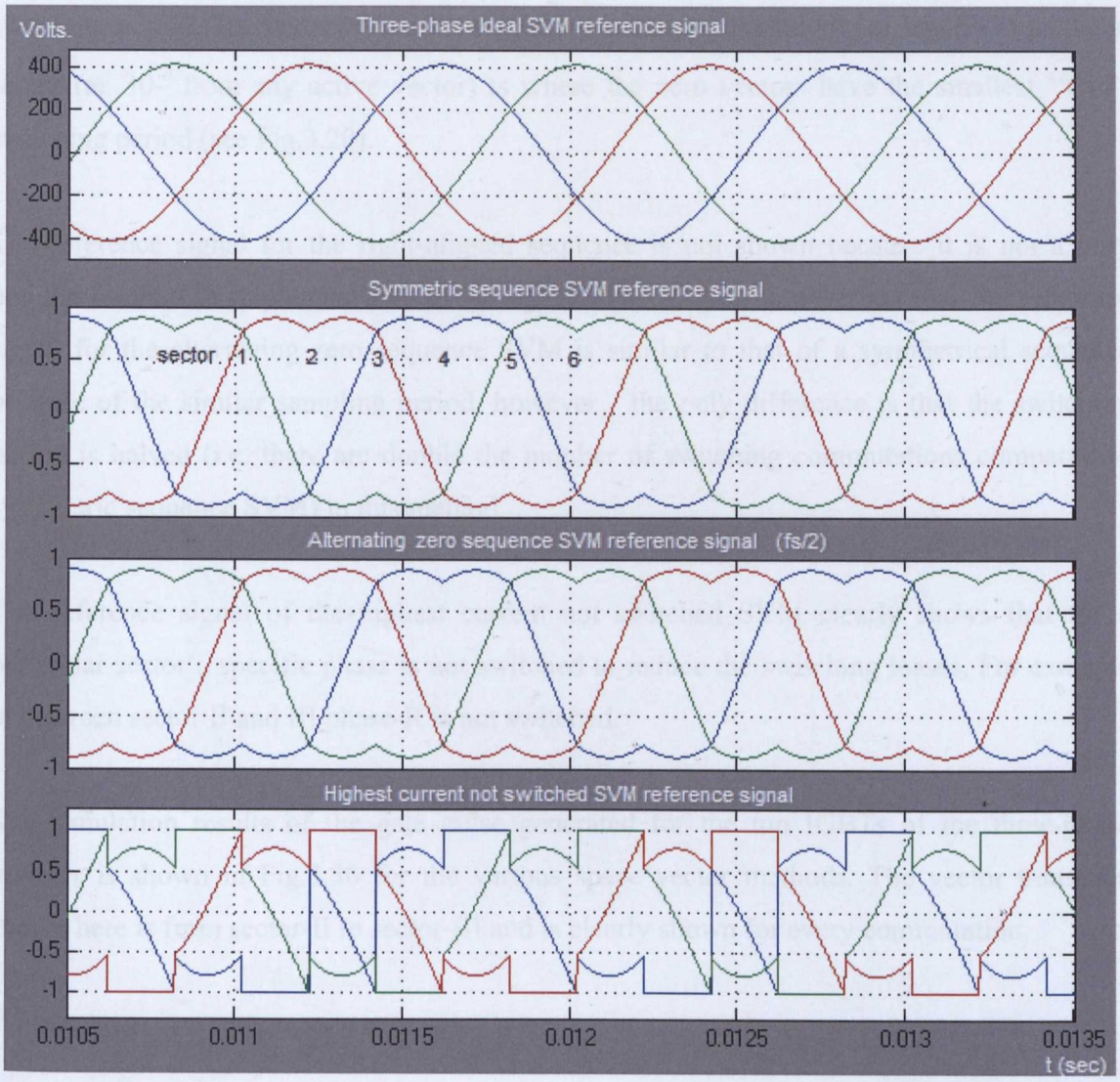


Fig.3.29 SVM reference signal for various SVM types.

The most important aspect of this switching scheme is the selection of the zero vectors for a particular sector. However it is not always possible to avoid switching the phase with the highest current because the choice of the zero vectors is based on the desired output voltage as well as on the load dependent current. In this case the phase carrying the second highest current is not switched and the switching losses can still be kept low.

The reference signal generated from all the SVM methods discussed above is shown in Fig.3.29. Compared to the first ideal reference three-phase sinusoidal signal, the symmetric sequence reference signal has a dip instead of peaks. This dip signifies the transition of the reference vector V_R from one SVM hexagon sector to another. The jump from one sector to another in the SVM hexagon is the instant when the zero vector has its longest ''ON''

switching period. The instant when the resultant vector is in the middle of any SVM hexagon sector (at 30^{o} from any active vector) is where the zero vectors have the smallest ''ON'' switching period (see Fig.3.20).

The reference signal for the right-aligned sequence is not shown because it is not a very popular method to implement due to its higher THD. It can be observed that the reference signal for the alternating zero sequence SVM is similar to that of a symmetrical sequence because of the similar sampling period, however the only difference is that the switching period is halved (i.e. there are double the number of switching commutations compared to symmetric sequence SVM) in this method.

The reference signal of the highest current not switched SVM clearly shows that for a particular sector a specific phase is not switched to reduce the switching losses. For example in between sector II and III phase-R is not switched.

The simulation results of the gate pulse generated for the top IGBTs of the three-phase inverter is shown in Fig.3.30 for the various space vector methods. The vector transition shown here is from sector-II to sector-III and is clearly shown for every commutation.

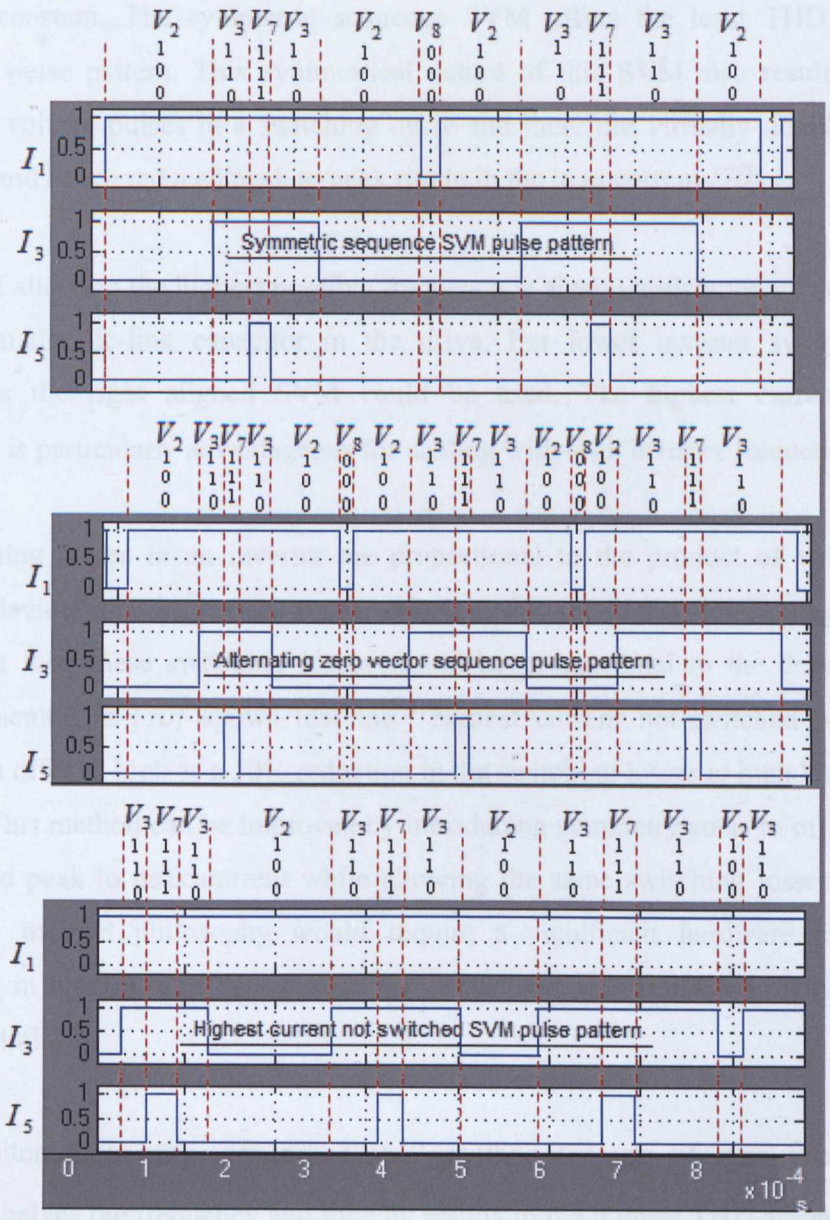


Fig.3.30 Gate pulse pattern simulation results for various SVM types.

Modulation algorithms such as hysteresis are simple to implement but are not considered here because they use non-adjacent space vectors and produce higher THD and switching losses. To decide which method is best suited for achieving a reduced dc-link capacitor it is important to compare the above discussed methods. A detail comparison analysis is presented in *[70]* based on switching loss, THD and peak to peak ripple currents. The result presented in *[70]* shows that the THD decreases with increase in modulation depth for all the SVM methods. This is because the increase in modulation depth causes an increase in the fundamental current/voltage component while the other harmonic components remain

relatively constant. The symmetric sequence SVM offers the least THD because of its symmetric pulse pattern. This symmetrical nature of this SVM also results in double the number of voltage pulses in a switching cycle and therefore virtually doubling the inverter frequency and hence reduced peak to peak ripple in the load current *[70]*.

The idea of allowing the highest possible frequency is always welcomed by designers so as to allow a smaller dc-link capacitor in the drive. For lower inverter switching frequency applications the right aligned SVM could be used. The highest current not switched application is particularly advantageous for dealing with high inverter frequency applications.

The switching losses in an inverter are proportional to the product of voltage across the switching devices and the current at that switching instant. If a dc-link voltage is assumed to be constant then these switching losses would be proportional to the device current. The results presented in *[70]* shows that the ''highest current not-switched sequence'' SVM method can offer as high as a 50% reduction in the switching losses at high load power factors (>0.866). This method can be improved by introducing symmetry so as to offer reduced THD and reduced peak to peak current while allowing the same switching losses. Improving the modulation method philosophy would require a significant hardware change and add complexity in control, and therefore is not considered as a preferred method to achieve a smaller dc-link.

In the ''alternating zero sequence SVM'' method the use of zero vectors (V_7 or V_8) effectively halves the frequency and thereby results in the highest THD amongst all the SVM methods but it offer lowest switching losses at the same time. Similarly ''symmetric sequence SVM'' offers lower THD but at the cost of higher switching losses. This requirement forces designers to consider a tradeoff between the size of heat sink and the size of filters. The work presented in this thesis is concentrated on the size of dc-link capacitor therefore the ''symmetric sequence SVM'' is considered as the preferred method for further analysis.

3.3.3 Three-Phase Rectifier Simulation

The three-phase inverter discussed in the previous chapter was assumed to be supplied with a constant dc-link voltage but in practice the dc-link voltage for the actuator inverter comes from the rectified aircraft AC power supply (200V L-L, 400Hz). The rectification of the aircraft AC power supply could be done using a three-phase diode rectifier or a fully controlled front end PWM rectifier. Both methods have their own merits and demerits depending on the application and performance requirements, and they will be discussed in this section with the aim of achieving smaller capacitor requirements in the dc-link.

3.3.3.1 Three-phase Diode Rectifier

Before discussing the rectifier in detail, it is necessary to calculate the effective load which the rectifier needs to supply in order to emulate the performance as if it is connected to an actuator motor load. The approximate actuator motor load power requirement (ignoring inverter losses) can be calculated using eq.(3.4) and Table-1 as:

$$P_{load} = P_{mech} + P_{copper\ .loss} \tag{3.39}$$

So $$P_{load} = 3500 + \frac{3}{2}(12.42)^2.(0.156)$$

So $$P_{load} = 3.596\ \text{kW}$$

For ease of understanding the operation of a fully switched rectifier, this load is assumed to be effectively resistive and can be calculated as:

$$R_{load} = \frac{V_{dc}^{\ 2}}{P_{load}} = \frac{460^{\ 2}}{3596} = 58.84\Omega$$

A simulation model of a three-phase diode bridge rectifier connected to a 400 Hz aircraft power supply (L_s selected for 0.1 p.u drop) and a resistive load (with C=1000 μ F) is shown in Fig.3.31. This is probably the most extensively used rectifier topology for low (5-50 kW) to moderate (up to few kW range) applications.

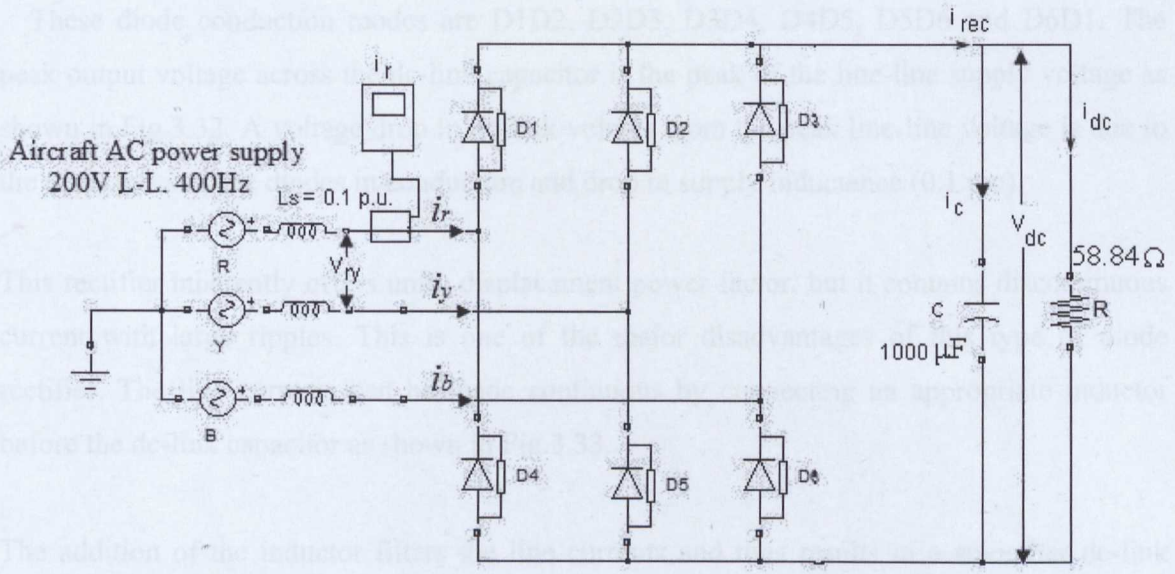


Fig.3.31 Three-phase diode bridge rectifier simulation with resistive load.

The top group diodes (D1, D3, D5) allow the largest of the three phase voltages V_{rn}, V_{yn}, V_{bn} to appear at the positive DC bus. Similarly the bottom group of diodes (D4, D6, D2) allows the most negative of the three phase voltages to appear at the negative DC bus. The output voltage at any instant is thus the largest of the six line voltages $V_{ry}\ V_{yb}\ V_{br}\ V_{yr}\ V_{by}$ and V_{rb} with one diode from the top group and one from the bottom group conducting at any instant. Thus the rectifier has six different input to output conduction modes that each last for 120^{o}.

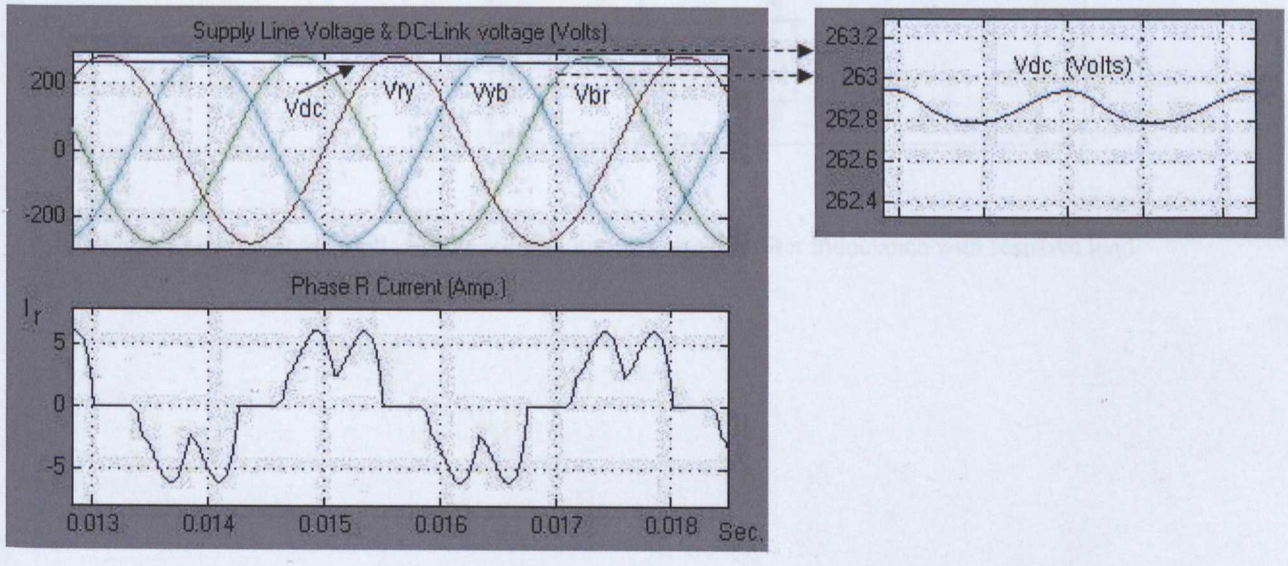


Fig.3.32 DC-Link voltage, line-line voltage and phase-R current of the diode bridge rectifier.

These diode conduction modes are D1D2, D2D3, D3D4, D4D5, D5D6 and D6D1. The peak output voltage across the dc-link capacitor is the peak of the line-line supply voltage as shown in Fig.3.32. A voltage drop in dc-link voltage from the peak line-line voltage is due to the resistances of the diodes in conduction and drop in supply inductance (0.1 p.u).

This rectifier inherently offers unity displacement power factor, but it contains discontinuous current with large ripples. This is one of the major disadvantages of this type of diode rectifier. The line currents can be made continuous by connecting an appropriate inductor before the dc-link capacitor as shown in Fig.3.33.

The addition of the inductor filters the line currents and thus results in a smoother dc-link voltage. Adding an inductor may significantly increase the size, weight and cost of the drive.

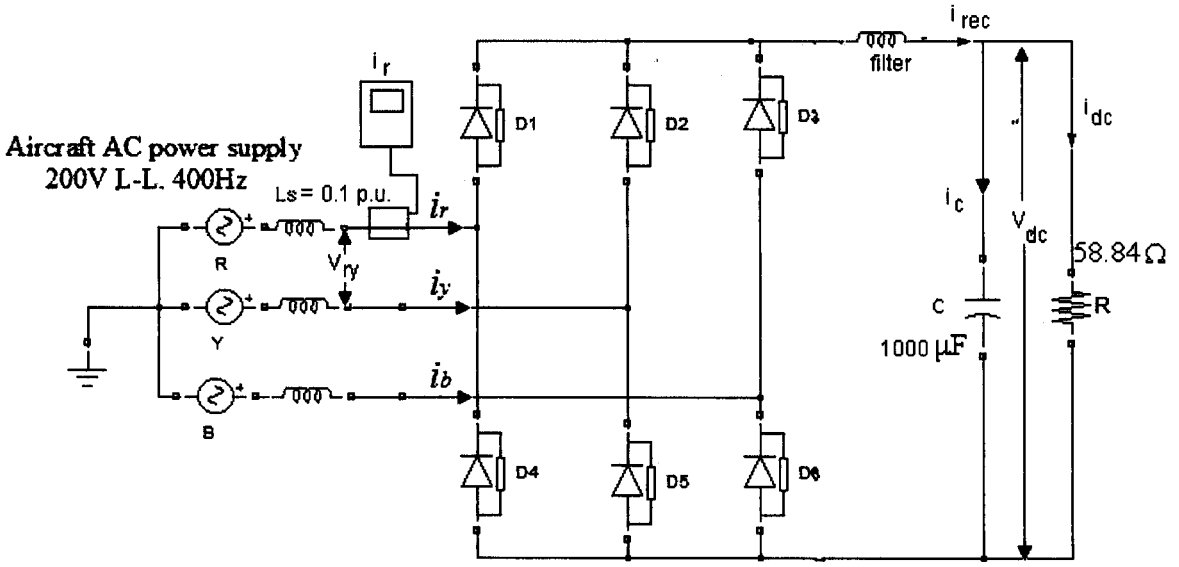


Fig.3.33 Three-phase diode bridge rectifier simulation with filter inductance with resistive load

3.3.3.2 Three-phase PWM Rectifier

A three-phase fully controlled rectifier is preferred when large power is involved and it avoids the use of an autotransformer with a diode rectifier. The use of autotransformer is not considered with diode rectifier in previous section because in terms of reliability of the whole system, PWM rectifier can offer more reliable operation than autotransformer and diode rectifier combined *[22]*.

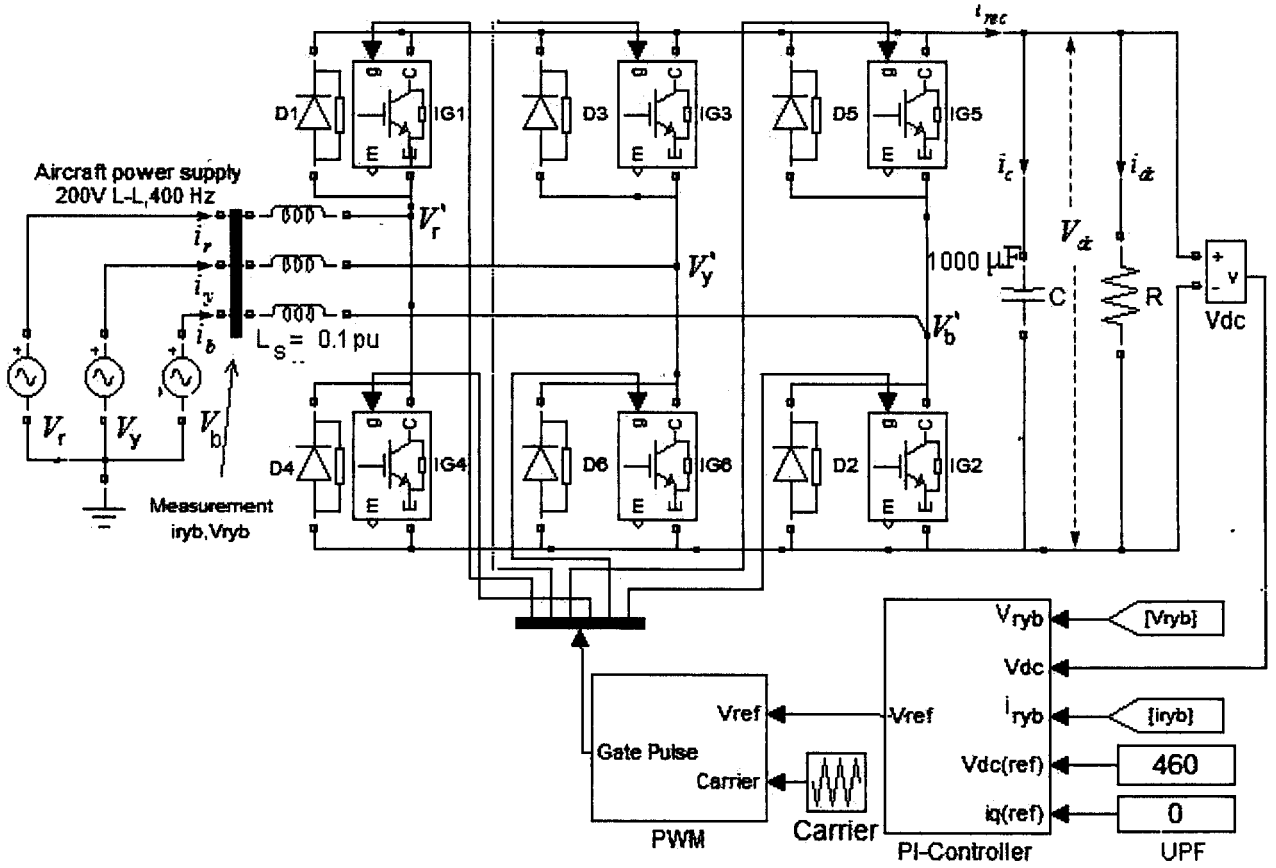


Fig.3.34 Three-phase PWM IGBT rectifier with unity power factor controller.

This type of forced commutated rectifier has the advantage of less harmonic contamination, controlled power factor and power reversal if required. A three-phase IGBT rectifier simulation model with a pulse width modulation control circuit is shown in Fig.3.34.

The basic operating principle of the above rectifier is based on maintaining the desired constant dc-link voltage close to the reference value using a feedback control loop. To achieve

this goal, the dc-link voltage is measured and compared with a reference value to generate an error signal as shown in Fig.3.35. A PI controller converts this error signal into a d-axis current reference signal which is later compared with the corresponding measured supply current component. To achieve unity displacement power factor operation (taking the d-axis as reference), a zero value q-axis current is forced by the controller. The current PI controller converts these current and voltage error signals into a set of reference voltage signals, which are required to achieve the desired dc-link voltage and unity displacement power factor operation. The three-phase reference signal is used in the PWM block to produce the gate pulses for the six IGBTs of the inverter. The pulse width modulation method can be any of the methods discussed previously from carrier wave comparison to space vector modulation. The carrier wave comparison modulation method for dc-link voltage control is discussed in detail below.

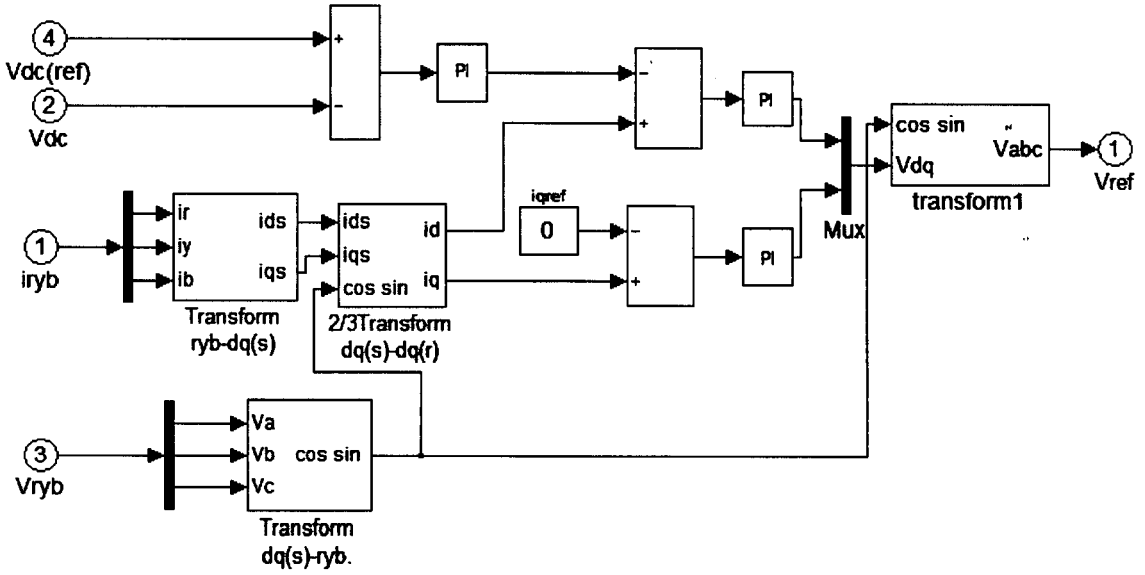


Fig.3.35 Voltage source voltage controlled dc-link controller

The desired rectifier output voltage is obtained by controlling the gate pulse width and thus the input rectifier terminal voltages (V_r', V_y' V_b'). To accurately control the dc-link voltage the PWM scheme must "generate" a fundamental input rectifier terminal voltage of the same frequency as the supply.

The interaction between the supply voltage and the terminal voltage can be seen in the phasor diagram of Fig.3.36 for phase-R.

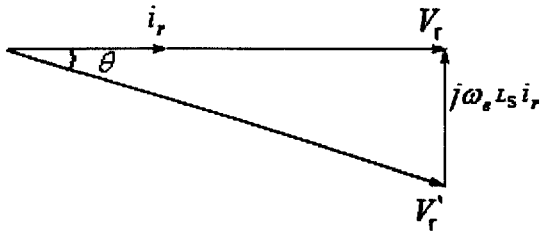


Fig.3.36 Unity power factor operation of three-phase PWM rectifier (phase-R).

Here ω_e is the angular frequency of supply voltages in rad/sec. From the above it is known that the maximum requirement from the rectifier is P_{load} = 3.596 kW. To find the unknown parameters such as i_r and Ls for the rectifier it can be written that:

$$P_{load} = 3.596 \text{ kW} = 3.\ V_r.i_r.\cos\theta$$

For unity power factor operation ($\cos\theta$=1) the peak phase-R supply current can be calculated as:

$$P_{load} = 3.596 \text{ kW} = 3.\ \frac{200}{\sqrt{3}.\sqrt{2}}.i_r$$

So $$i_r = 10.8 \text{ A (rms)} = 14.6 \text{ A (peak)}$$

To limit the fault current on the supply side below ten times the rated value, the supply inductor (Ls) is selected assuming 0.1 p.u. voltage drop in it.

So $$j\omega_e.L_s.i_r = 0.1.\frac{200}{\sqrt{3}} = 16.3 \text{ V}$$

and $$L_s = 0.44 \times 10^{-3} \text{ H}$$

From the phasor diagram of Fig.3.36 the peak phase-R terminal voltage can be computed as:

$$V_r' = V_r - j\omega_e L_s i_r$$

So $$V_r' = 164.1 \text{ V}$$

The angle δ can be calculated as:

$$\delta = \tan^{-1}(\frac{16.33}{163.3}) = 5.7^{\circ}$$

Instantaneous values of the three-phase fundamental terminal voltages can be found using the equations below:

$$V_r' = 164.1 \text{ Sin}(\omega_e t - 5.7\frac{\pi}{180}) \quad (3.40)$$

$$V_y' = 164.1 \text{ Sin}(\omega_e t - 5.7\frac{\pi}{180} - \frac{2\pi}{3}) \quad (3.41)$$

$$V_b' = 164.1 \text{ Sin}(\omega_e t - 5.7\frac{\pi}{180} - \frac{4\pi}{3}) \quad (3.42)$$

Where ω_e is the electrical angular frequency of the supply currents in rad/sec.

The target fundamental terminal voltages (V_r', V_y' V_b') for the required dc-link voltage (V_{dc} =460 V) can be expressed in relation to the PWM modulation depth using equation (3.24) and (3.25) as:

Rectifier modulation depth:-

$$M_r = \frac{A_r}{A_c}$$

Here the amplitude of the carrier V_c is " A_c " and the amplitude of the reference signal is A_r .The amplitude of the fundamental terminal voltage V' is related to modulation depth as:

$$V' = M_r . \frac{V_{dc}}{2}$$

For a desired dc-link voltage of 460 V and carrier wave amplitude of A_c = 10 V, the fundamental rectifier terminal voltage peak V' = 164.1 *Volts* can be achieved for a modulation depth of:-

$$M_r = \frac{2.V'}{V_{dc}} = 0.71$$

Thus the ideal reference required to produce the fundamental rectifier terminal voltage V' can now be calculated as:

$$A_r = A_c \,.\, M_r = 10 \times 0.71 = 7.1 \text{ V}$$

So

$$V'_{R.r} = 7.1.\sin(\omega_e t - \frac{5.7 \times \pi}{180}) \tag{3.43}$$

$$V_{R.y} = 7.1.\sin(\omega_e t - \frac{5.7 \times \pi}{180} - \frac{2.\pi}{3}) \tag{3.44}$$

$$V_{R.b} = 7.1.\sin(\omega_e t - \frac{5.7 \times \pi}{180} - \frac{4.\pi}{3}) \tag{3.45}$$

The simulated result of the above PWM rectifier for unity power factor operation is shown in Fig. 3.37. As shown in Fig.3.37 the supply current simulation confirms the calculated peak current value of 14.6Amp and unity power factor.

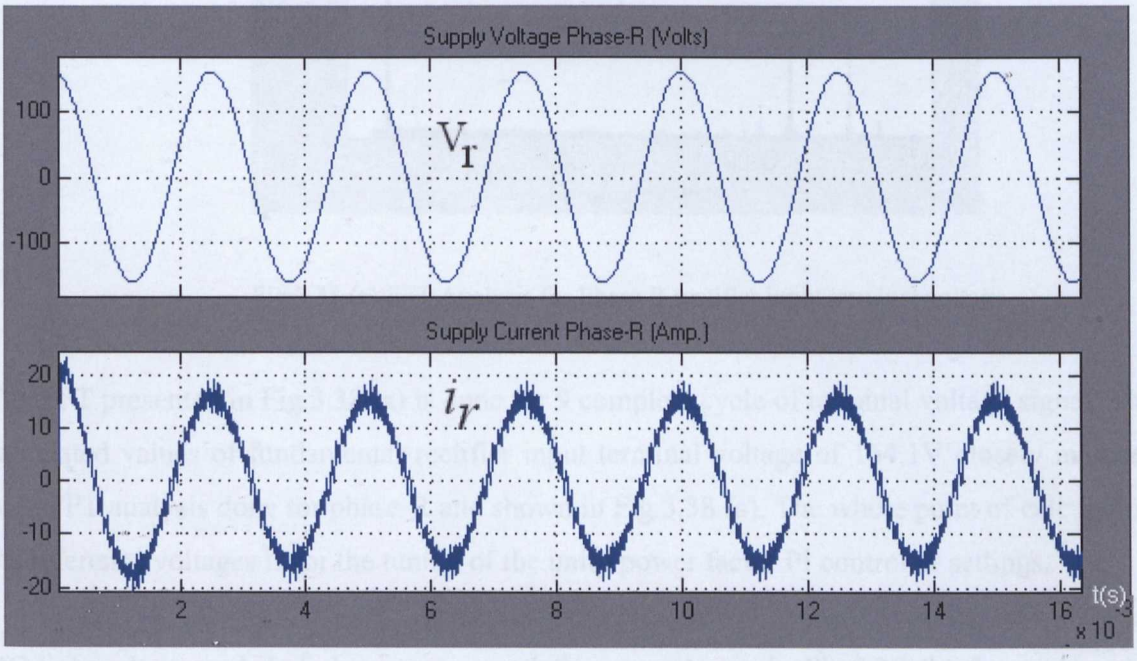


Fig.3.37 Simulation results of unity power operation of 12 kHz sine-carrier PWM rectifier.

The results of Fig.3.32 of diode rectifier can be compared with Fig.3.37 as PWM rectifier draws good sinusoidal currents from supply.

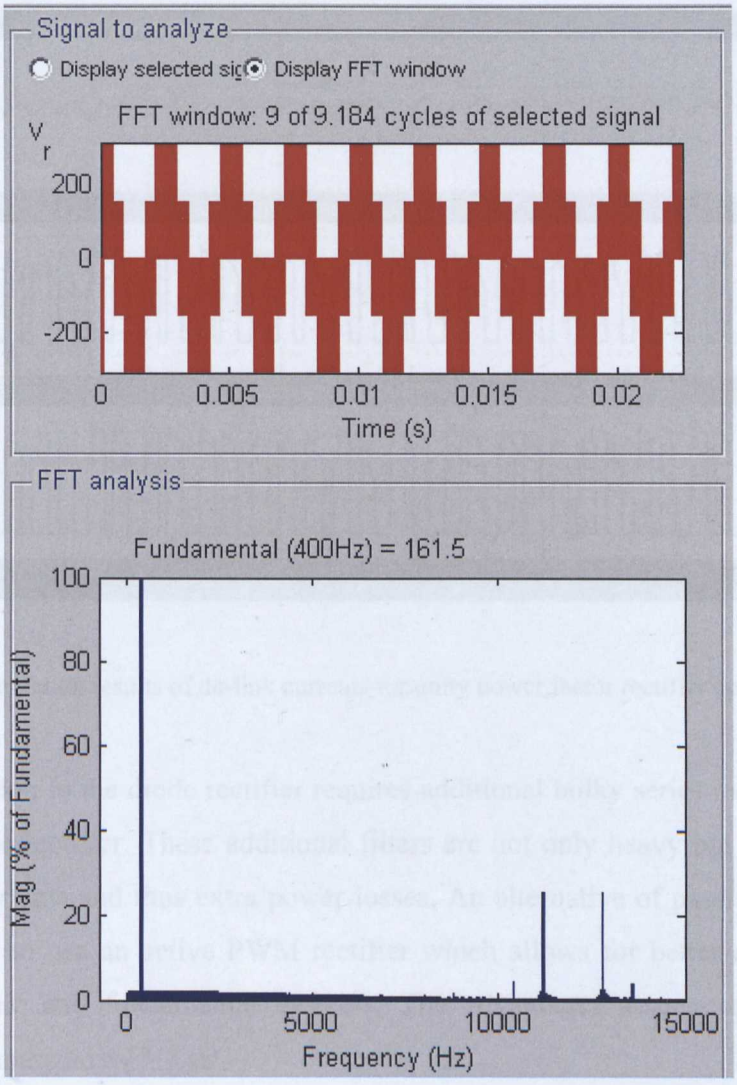


Fig.3.38 (a) FFT Analysis for Phase R rectifier input terminal voltage

The FFT presented in Fig.3.38 (a) is done for 9 complete cycle of terminal voltage signal. The calculated values of fundamental rectifier input terminal voltage of 164.1V closely matches with FFT analysis done for phase-R and shown in Fig.3.38 (a). The whole point of calculating the reference voltages is for the tuning of the unity power factor PI controller settings.

DC-link voltage and dc-link currents simulations are shown in Fig.3.38 (b) for sine-carrier pulse width modulation.

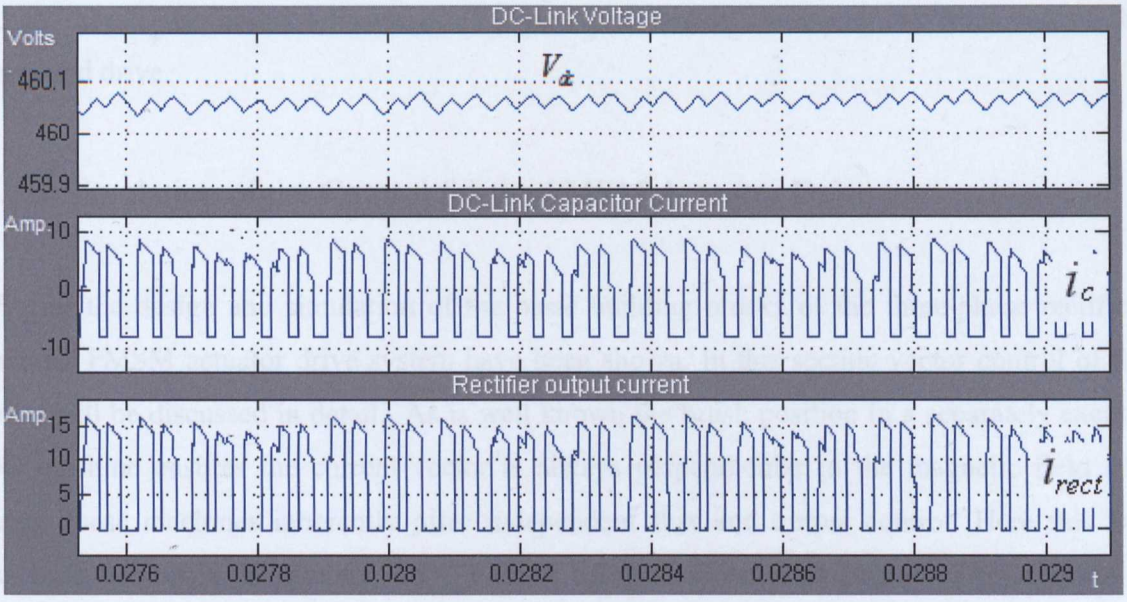


Fig.3.38 (b) Simulation results of dc-link currents for unity power factor rectifier operation

The harmonic reduction in the diode rectifier requires additional bulky series inductors in the input or output of the rectifier. These additional filters are not only heavy but also result in high fundamental currents and thus extra power losses. An alternative of passive filtering in the diode rectifier is to use an active PWM rectifier which allows for better dynamics and controls the harmonic and fundamental currents. The advantages associated with PWM rectifiers can be summarized a *[71]* as:-

- bi-directional power flow,
- near sinusoidal input currents,
- input power factor close to unity,
- lower THD of supply currents,
- control over dc-link voltage,

The EMI regulations require that the PWM rectifier has properly designed low pass filters at the supply side. Although the control of the PWM rectifier is complex and it is less efficient than the diode rectifier, the continuous currents and PWM control allows better control of currents through the dc-link and thus a smaller capacitor in the dc-link. There are various other rectifier topologies that could be considered but the topology shown in Fig.3.34 offers

all the above mentioned advantages *[71]* and therefore is chosen as the front end of the proposed drive.

3.3.4 Simulation of the Control for the PMSM Actuator Drive

So far the design and simulation of the basic building blocks of the three-phase rectifier-inverter PMSM actuator drive system have been shown. In this section vector control of the drive will be discussed in detail. As is well known the brush position in a separately excited DC machine ensures the current vector is always perpendicular to the magnetic field and hence these machines inherently offer independent flux and torque control. Here this DC machine behaviour is emulated in a PMSM using field oriented control. Typical control requirements are constant torque at low speed and flux weakening with constant power for higher speeds. This cross-over depends on the designed rated speed of the motor as shown in Fig.3.39.

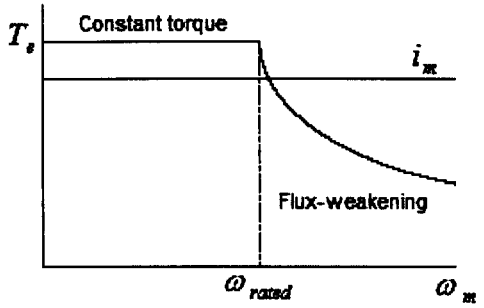


Fig.3.39 Torque versus speed steady state characteristics

3.3.4.1 Vector Control of Three-phase AC-DC-AC drive.

The electric torque T_e of a fully compensated DC machine can be defined as:

$$T_e = K.\psi_m.i_a \tag{3.46}$$

Where K is a machine dependent constant, ψ_m is the instantaneous magnetizing flux linkage produced by the field winding and i_a is the instantaneous armature current.

The DC machine torque control concept says that if the flux linkage ψ_m of the DC machine is kept constant, the electric torque produced by the machine can be fully controlled by adjusting the armature current i_a.

Now applying a similar concept to an AC machine, it is known from equation (3.14) that the PMSM output torque can be defined as vector product of stator flux linkages and stator current as:

$$T_e = \frac{3}{2}.p.(\psi_d.i_q - \psi_q.i_d)$$

The analysis of the machine using a coordinate system (reference frame system), where the coordinate vector rotates synchronously with the flux, enables the separation between the flux linkage and torque producing current component. The q-axis component i_q can be seen as equivalent to the DC machine armature current whereas the d-axis component contributes towards the total flux in the machine, with the major part of the total flux coming from the permanent magnet field (in the direct axis). For this reason the q-axis current is termed here as torque producing current and the d-axis current is called the flux producing current component of the stator current.

[1] Torque control

Here the interest is only in the constant torque region of Fig.3.39 for our three-phase PMSM dc-link actuator drive. Like in a DC machine, to obtain maximum possible torque from the actuator motor the flux producing current component i_d is forced to zero.

From the motor equations:

$$\psi_d = L_d.i_d + \psi_m = \psi_m$$

Thus the maximum torque per ampere (assuming no saliency) becomes:

$$T_e = \frac{3}{2}.p.(\psi_m.i_q) \qquad (3.47)$$

Assuming no cross-saturation (i.e. the magnet flux is not affected by q axis armature current)

$$k_t = \frac{3}{2}.p.\psi_m.$$

The torque can now be represented like equation 3.46 as:

$$T_e = k_t i_q \tag{3.48}$$

The above explanation can be easily understood from the phasor diagram shown in Fig.3.40. By forcing i_d=0, the supply current becomes equal to i_q and at right angles to the flux component which is equal to the magnet flux. It can be inferred from the Fig.3.40 that now the motor back e.m.f is in phase with the supply current (i_q).

The above condition of maximum torque is satisfied here for AC machines by forcing the supply current to lie at right angles to the machine flux and this phenomenon is known as vector control *[69]*.

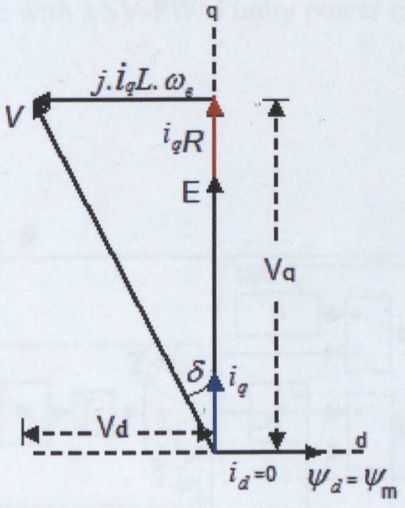


Fig.3.40 Phasor diagram of PMSM machine under vector control

The previously derived equations (3.4)-(3.6) for the maximum torque condition perfectly fits the phasor representation of vector control of Fig.3.40.

[2] Speed control

Controlling the surface actuator requires a precise speed and position control. The speed controller for the dc-link actuator drive can easily be simulated using a speed feedback loop. A properly tuned and designed speed controller should follow the reference speed instructions at any time and minimize any parameter disturbances. A closed loop inverter controller of the type shown in Fig.3.1 consists of a closed loop controller followed by a PWM generator of

either sine-carrier PWM or SVPWM (Fig.3.9 or Fig.3.19). The closed loop controller for speed typically consists of an inner current (thus torque) control loop and an outer speed control loop as shown in the simulation model of Fig.3.41. This is stable in practice because the speed response of the drive is far slower than the torque response and hence the two nested loops do not interact to any significant extent.

The speed and torque controller combined produce a reference signal for the modulator to generate the corresponding gate pulses. The speed controller calculates the real time speed error and generates a reference torque producing q-axis current component. The torque/current controller receives this signal as well as a demand for a zero d-axis current signal to force the field orientation. The inner current loop needs to be much faster than the outer speed loop to achieve good control over currents. A complete SV-PWM vector controlled PMSM actuator drive with a SV-PWM unity power factor rectifier front end is shown in Fig.3.42.

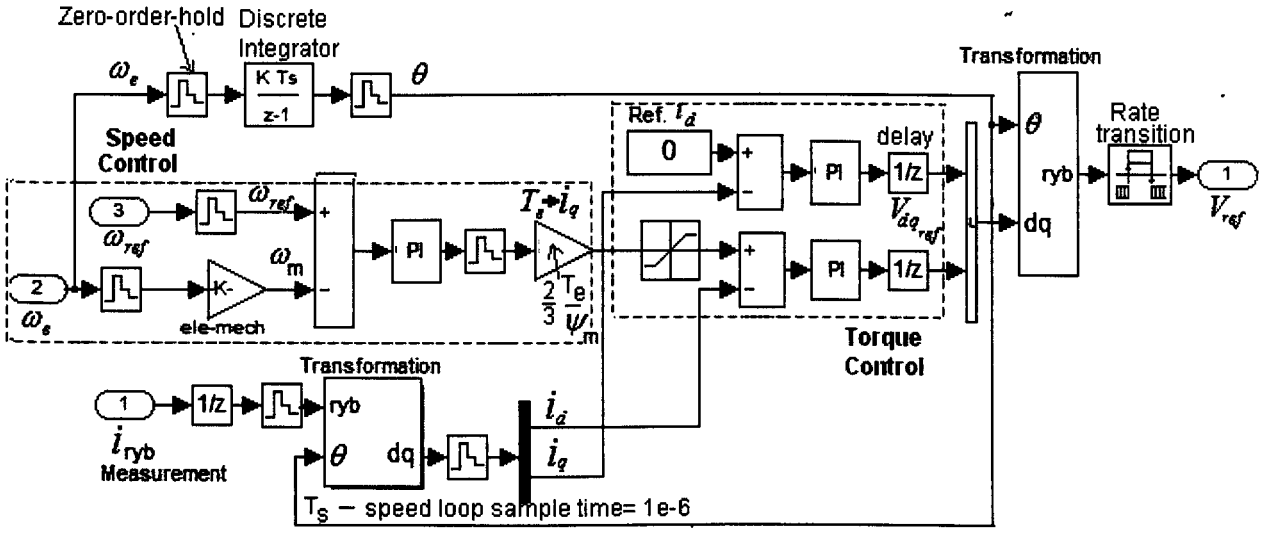


Fig.3.41. Close loop speed and torque controller simulation.

The 34k Nm torque required for the aircraft control surface is supplied via a 10000:1 ratio gearbox. Thus for a 10000 rpm actuator motor the torque producing requirement is just 3.4 Nm. This gearbox feature is simulated in the above drive using a 3.4/10000 load factor gain block to produce a load torque signal for the motor model. The model ignores gearbox backlash and assumes the gear linkage is very stiff and hence the inertia is all transferred to the motor.

As discussed earlier for a typical high lift surface actuator motion of extension and retraction, it is very important that the drive maintains good control and to do this the front end needs to maintain a reasonably stable dc-link voltage with near unity power factor being drawn from the aircraft ac supply.

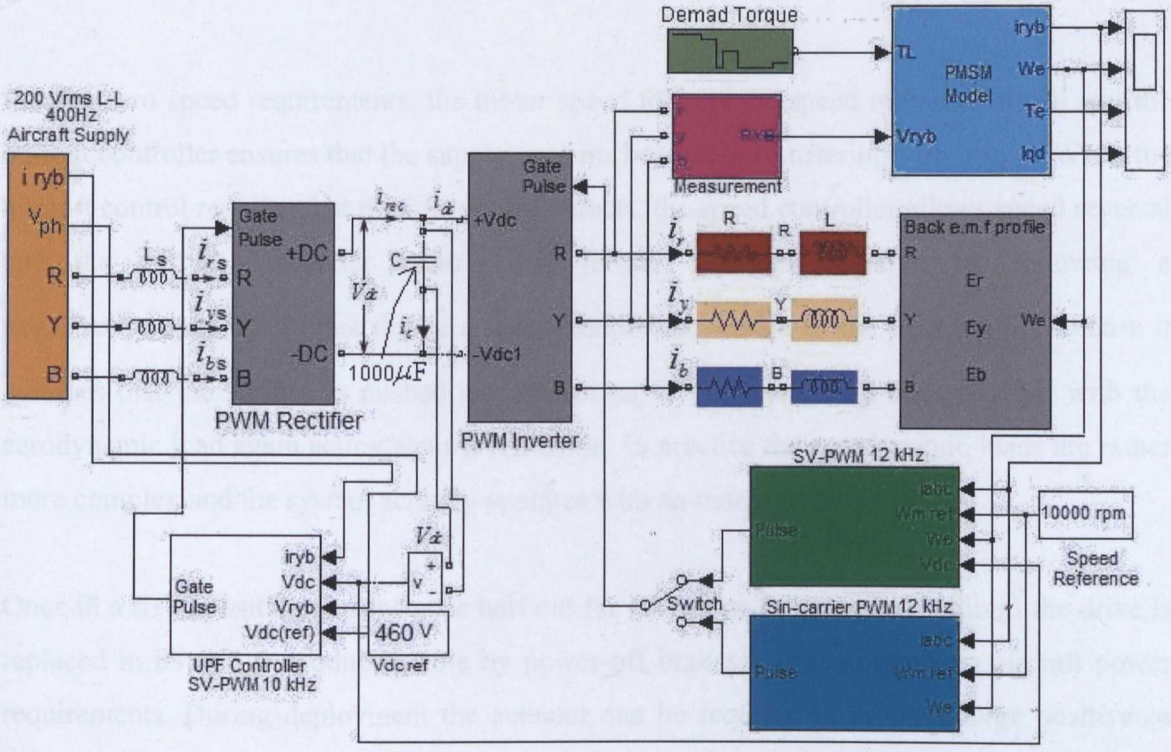


Fig.3.42. PMSM Actuator Drive with SV-PWM vector control and SV-PWM UPF rectifier front end.

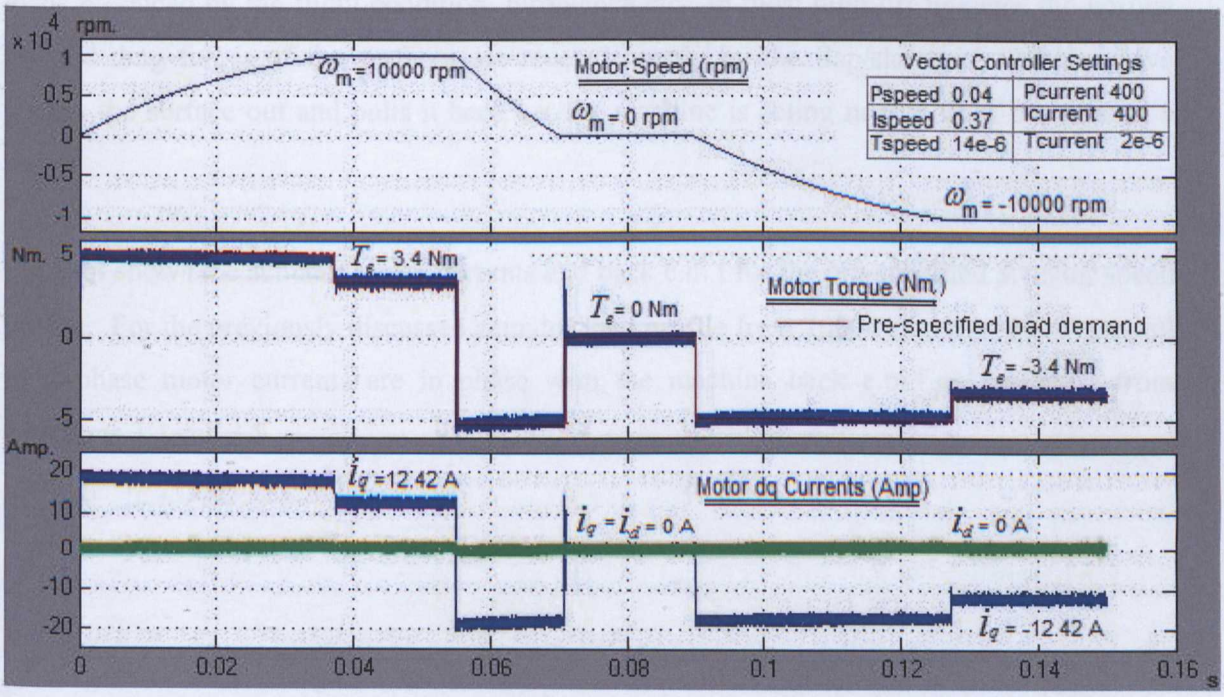


Fig.3.43. PMSM actuator drive speed and current response for a pre-specified load profile.

Fig.3.43 shows the simulation results for the above drive for a typical actuator load profile. It can be inferred from Fig.3.43 that as the actuator motor speed reaches its rated value (10000 rpm) the vector controller is making sure that i_d remains zero at all the times and like a dc machine, the PMSM torque remains proportional to i_q.

For the zero speed requirements, the motor speed follows the speed reference signal and the current controller ensures that the supply currents become zero offering zero torque. When the aircraft control requires that the lift surface retracts, the speed controller allows speed reversal and the current controller ensures the torque becomes negative by following a negative i_q trajectory. In fact this is a rather simplified version of the load profile because it assumes that the surface is pushed out against an aerodynamic load and retracted with the aerodynamic load again acting against retraction. In practice the aerodynamic loads are rather more complex and the system actually operates with an outer position loop.

Once in a fixed position (for instance half out for takeoff or fully out for landing) the drive is replaced in its torque producing role by power-off brakes – thus minimising aircraft power requirements. During deployment the actuator can be required to produce large positive or negative torques depending on the geometry of the actuator linkage and the aerodynamic loads produced by the flight condition, turbulence etc.. In most high lift linkages the normal lift and drag forces of the surfaces are reacted mostly by the flap/slat track and the drive pushes the surface out and pulls it back i.e. the machine is acting nearly all of the time as a motor.

Fig.3.44 shows the actuator motor currents and back e.m.f for the pre-specified actuator speed profile. For the previously discussed actuator load profile from 10000 rpm to -10000 rpm, all three-phase motor currents are in phase with the machine back e.m.f as predicted from equations 3.4 and 3.5.

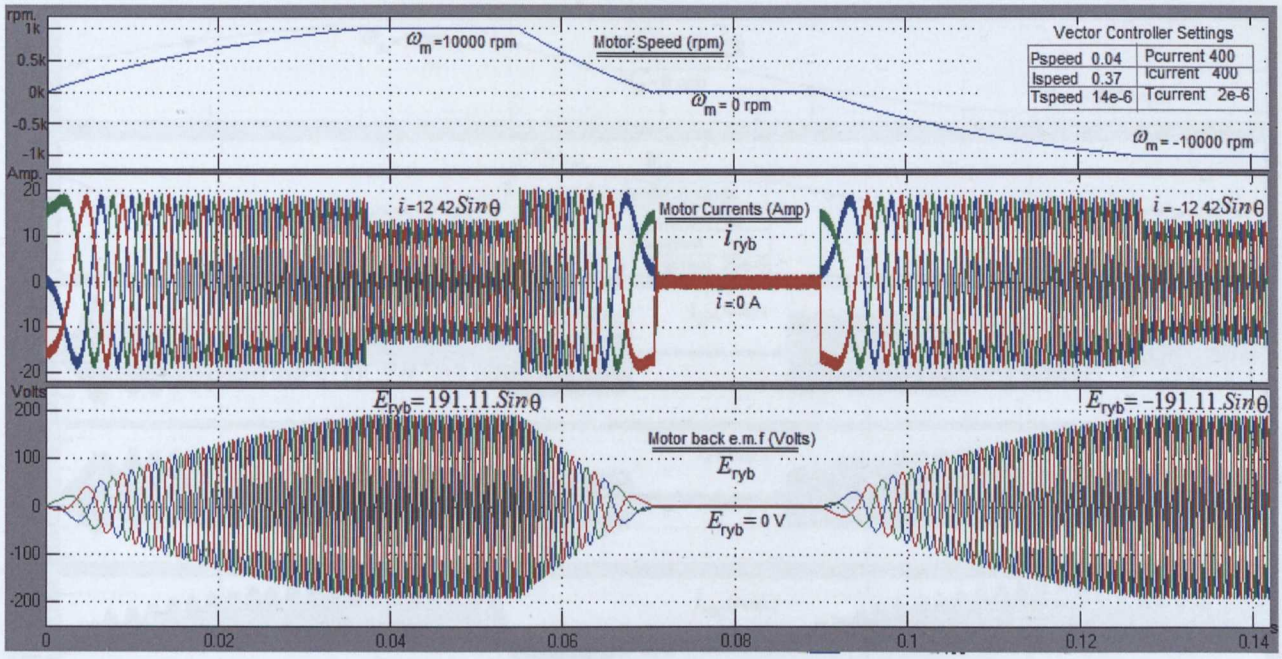


Fig.3.44. PMSM drive current response and back e.m.f profile for pre-specified speed reference

The satisfactory performance of the vector controlled inverter depends to a large extent on the dc-link condition, i.e. on the dc-link capacitor and the voltage control. A three-phase diode rectifier and a sine-carrier controlled UPF rectifier have already been discussed in previous sections for a resistive load. The fully controlled rectifier shown in Fig.3.42 is of space vector controlled PWM type. The space vector principle remains the same as shown in Fig.3.17. The gate pulse generation used is of the symmetric sequence type as shown in Fig.3.23. For the same actuator load profile as discussed above the dc-link quantities are shown in Fig.3.45. Sufficient dc-link capacitance as well as proper tuning of the dc-link voltage PI and unity power factor current PI ensures the stability of the dc-link voltage for no load and speed reversal operations.

Unity power factor operation of the SV PWM rectifier supplying the vector controlled PMSM drive can be seen from the Fig.3.46. The supply voltage remains undisturbed while supply currents respond to load changes. Proper tuning of the PI controllers is done using trial and error method with first to attempt UPF operation (i_{ds}=0) and then increase dc-link voltage proportional gain to meet dc-link voltage demand. It is been observed here that integral gain does not significantly affect the shape of any of signals but only changes the simulation response time. Effect of dc-link control loop proportional gain on dc-link parameters is discussed in detail in Chapter 5.

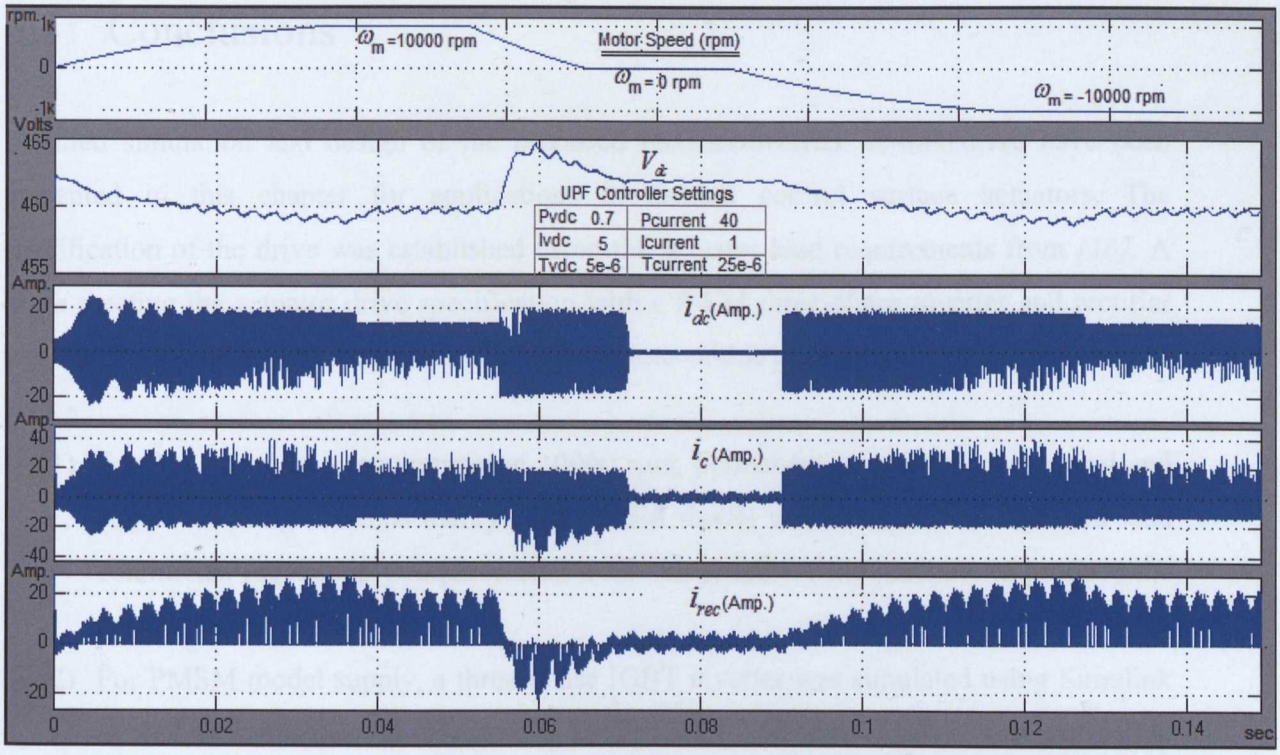


Fig.3.45. Simulation results of SV PWM UPF rectifier dc-link voltage and currents supplying vector controlled PMSM inverter drive.

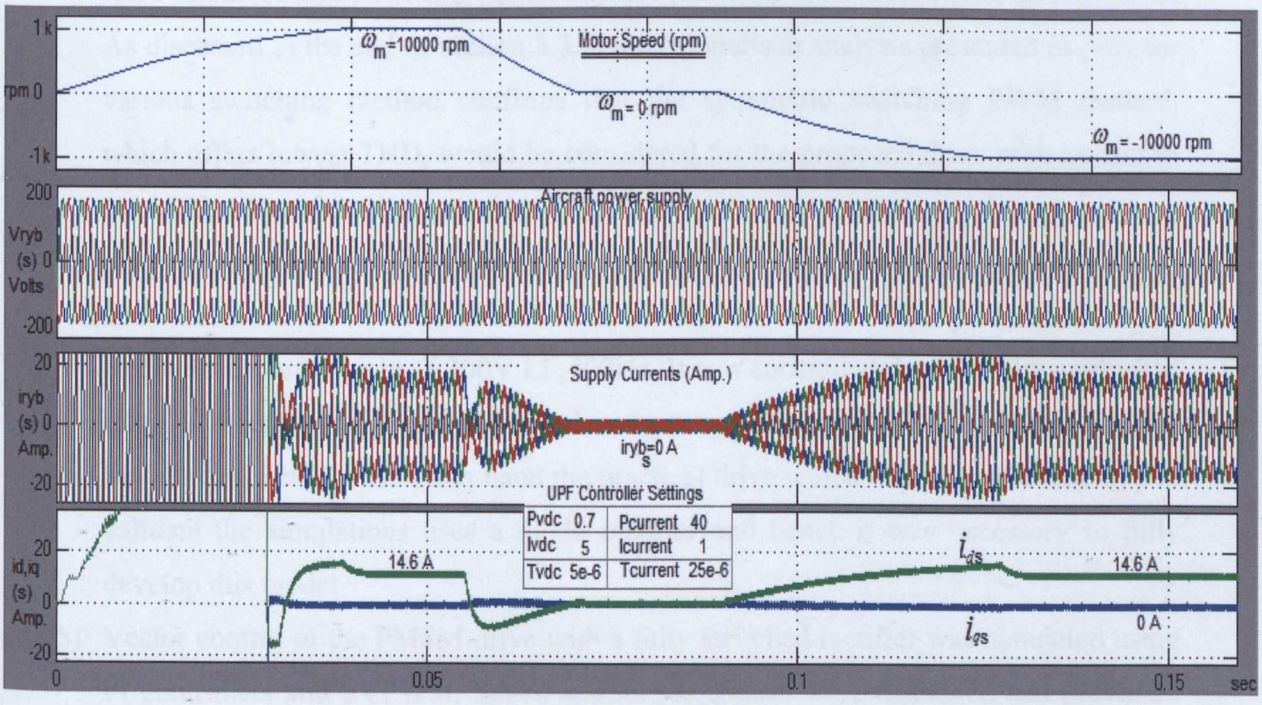


Fig.3.46. Simulation results of SVPWM UPF rectifier supply voltage, supply currents supplying vector controlled PMSM inverter drive.

3.4 Conclusions

Detailed simulation and design of the proposed rectifier-inverter dc-link drive have been presented in this chapter for applications in aircraft control surface actuators. The specification of the drive was established using the actuator load requirements from *[16]*. A drive meeting the actuator drive specification with a PWM three-phase inverter and rectifier was simulated and results presented. The contributions of this chapter are summarized below:

1) For 3.4 Nm torque requirement at 10000 rpm, permanent machine was modeled and simulated using two-axis theory. The PMSM model was tested for no load and load conditions. Ideal supply requirements were calculated for the machine to produce the desired torque and currents.
2) For PMSM model supply, a three-phase IGBT inverter was simulated using Simulink as well as Simpower. As discussed in section 3.3.1.2 Simpower model was required to simulate the non-ideal switching characteristics of practical switching devices.
3) Sine-carrier and space vector switching methods were discussed and simulated to produce appropriate gate pulses for the inverter IGBTs. Various space vector methods were discussed and switching patterns where presented with their merits and demerits. As discussed in the end of section 3.3.2, the comparison analysis presented in *[70]* for various switching method confirms that the symmetric switching PWM method, which offers lowest THD, would be considered for the proposed drive with an aim to reduce the size of dc-link capacitor.
4) Three-phase diode bridges and fully controlled UPF IGBT rectifiers were discussed and simulated for 460 V dc-link and simulation results were presented for the available aircraft supply of 200V LL,400Hz. It was concluded that the fully controlled rectifier offered a large number of advantages not least in respect of minimising dc-link capacitance. On the other hand the practical drive which has been instrumented to validate the simulations uses a diode rectifier and hence it was necessary to fully develop this model
5) Vector control of the PMSM drive with a fully switched rectifier was simulated using PI controllers and SVPWM. Speed and torque control were discussed and presented with the simulation results matching the previously calculated values
6) UPF operation of SVPWM IGBT rectifier was presented with simulation results.

CHAPTER 4

EXPERIMENTAL VALIDATION

It has been shown in Chapter 3 that the proposed drive of Fig.2.11 can be simulated to produce flight profile output from the actuator motor. The output simulation results presented in Chapter 3 (section 3.3.4.1) were based on a $1000\,\mu$F capacitor in the dc-link. Before making any move towards reducing the size of this dc-link capacitor, it is necessary to verify the overall simulation philosophy, for example if the modulation method presented in Chapter 3 is producing the predicted pulse pattern.

Previous research in dc-link current measurement [66][67] relied on recreation of supply phase currents to be used in the rectifier controller. This chapter will show how difficult it is to measure the dc-link currents and will use the simulation of Chapter 3 to explore the possibilities of small dc-link capacitance in the proposed drive. A set of test and load drives is used to emulate the actuator drive on a smaller scale. Two ''Control Technique Unidrives'' *[72]* are used for the purpose of the test and load. In this chapter the test drive setup is simulated and compared with experimental results to validate the simulation and to show why the sensor dependent converter control methods can't be relied upon. To verify the modulation technique used for the proposed drive simulation, gate pulse measurements are performed and compared with the simulation results.

4.1 Unidrive Introduction

Unidrive *[72]* is a trade name for a "universal" AC drive system for use with AC induction and permanent magnet ac motors. The drive can operate as a V/Hz, sensorless vector, closed loop flux vector, servo drive, fully switched front end converter or as a diode bridge rectifier/inverter in back to back formation. The drive control mode and parameter settings can be changed from a small panel on the drive or from a software interface. The drive's microprocessor unit controls the input to the inverter ASIC (application specific integrated circuit) which synthesizes an adjustable carrier frequency PWM *[72]*.

The test and load Unidrives are shown in Fig.4.1. Each of these drives has a diode rectifier front end with a dc-link to the Unidrive inverter supplying the machine. As this experimental work is aiming towards validating the simulation of Chapter 3 and understanding the difficulties of recreating the phase currents using dc-link current measurements, the presence of diode rectifier (instead of PWM rectifier) in the Unidrive setup does not pose any problem.

Fig.4.1 Unidrives for test and load motors

The test drive is set to speed control closed loop servo mode and the load motor is set for the torque control mode. The speed can be directly controlled from the drive panel and load torque can be entered in real time to the load drive. The mode of operation in the tests is to operate the test drive as a motor and the load acts as a brake. A bank of load resistors is connected to the load drive to absorb the power being generated by the load machine.

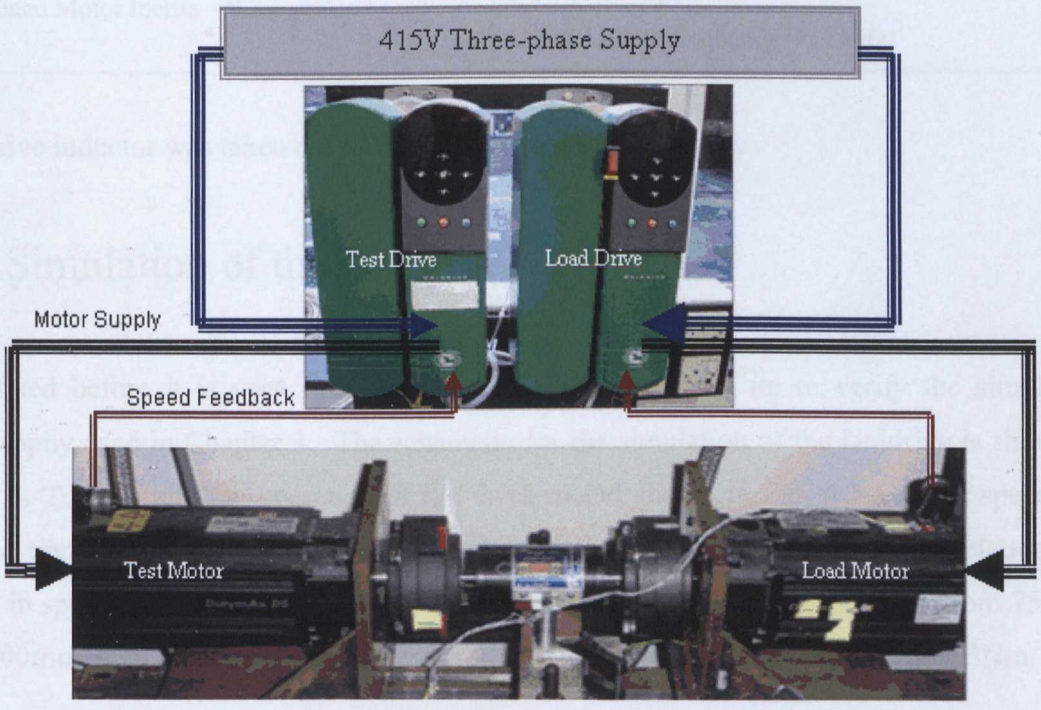


Fig.4.2 Experimental drive setup

The test and load motors are permanent magnet synchronous motors designed for servo applications and they are directly coupled via an inline torque transducer. The test setup is shown in Fig.4.2. The motors have surface permanent magnets (and hence are not salient) and being designed as servomotors they have a near linear torque/ampere characteristic even at 3 times overload (in other words magnetic saturation is not significant in the working range). Again given their servomotor heritage the back e.m.f is very close to a sinusoid and torque ripple is very low. These characteristics make the motors rather simple to simulate and justify the rather simple model used in the validation exercise which is the subject of this chapter. The experimental motor's specifications are as follows:-

Test motor	Load motor
V: 380/480 V	V: 380/480 V
Cont. Torque: 3.3 Nm: 2.06 A	Cont. Torque: 7.7 Nm: 4.81 A
Speed: 3000 rpm	Speed: 3000 rpm
Pole: 6	Pole: 6
Kt: 1.6Nm/A	Kt: 1.6Nm/A

The other information required to simulate the Unidrive is as follows:

DC-link choke = 1.73 mH	Stator Inductance = 43.1 mH
DC-Link choke resistance = 0.5 Ohm	Stator Resistance = 12.6 ohm
DC-link capacitance = 470 μ F	Field flux linkage (r.m.s) = 0.2546 V s
Combined Motor Inertia = 9.3 Kgm^2	DC-link voltage = 600 V
	Inverter PWM frequency = 12 kHz

Unidrive inductor was taken out of the drive to measure its value.

4.2 Simulation of the Unidrive

As stated before it is very important to simulate the test set up to verify the simulation philosophy used in Chapter 3. The schematic for the simulation of the Unidrive is shown in Fig.4.3. To illustrate the operation of the drive model shown in Fig. 4.3 a set of speed and torque transients is simulated and the results are shown in Fig. 4.4. In this simulation two steps in speed are demanded with zero load torque first from 0 to 750rpm then from 750rpm to 1500rpm, then the load torque is increased in three steps from 0 to 1 then 2 then 3Nm.

The system inertia is set very low in these tests (which is a more demanding case for the simulation) and hence the machine accelerates rapidly. As may be seen the drive performs as expected and stably both for speed and torque transients.

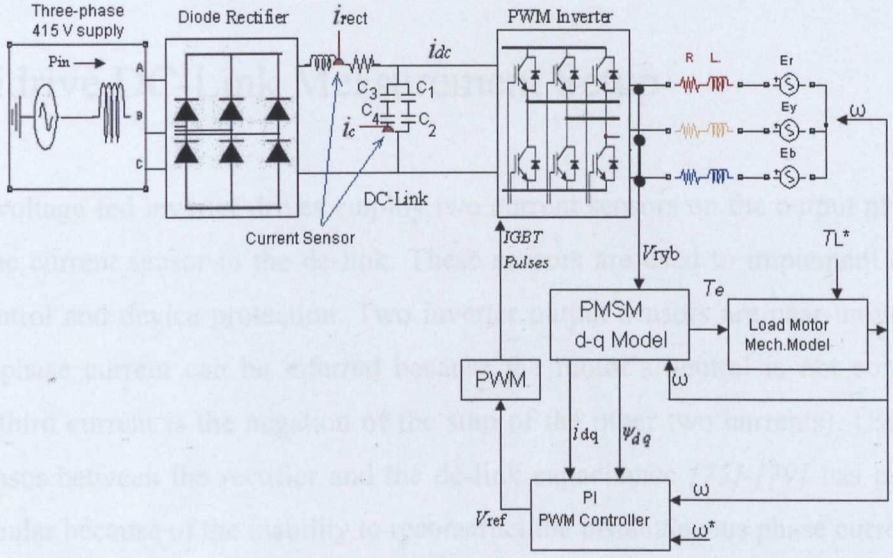


Fig.4.3 Schematic of test set up simulation.

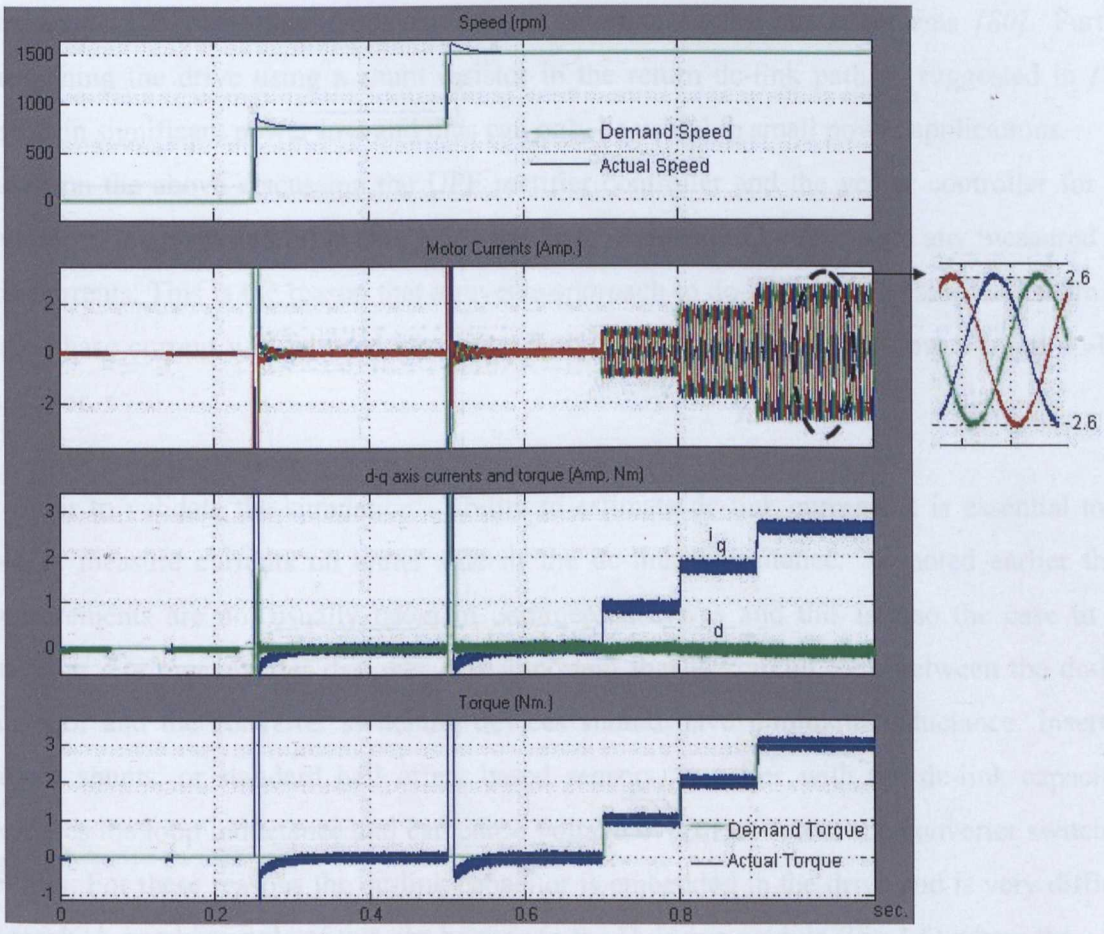


Fig.4.4 Speed, Current and Torque response from test drive simulation for acceleration to 1500rpm

It is important to note here that the Unidrive uses a diode rectifier and a bulky filter choke. The simulation results above use a 470 μF capacitor in the dc-link-the same as the Unidrive dc-link capacitance.

4.3 Unidrive DC-Link Measurement Setup

Typically voltage fed inverter drives employ two current sensors on the output phases and/or perhaps one current sensor in the dc-link. These sensors are used to implement closed loop current control and device protection. Two inverter output sensors are near universal in use (the third phase current can be inferred because the motor's neutral is not connected and hence the third current is the negation of the sum of the other two currents). Using a single current sensor between the rectifier and the dc-link capacitance *[75]-[79]* has proved to be very unpopular because of the inability to reconstruct the instantaneous phase currents.
In addition any closed loop control method which depends on dc-link current measurement has problems caused by the dc-link current containing undesired components such as snubber currents and freewheeling diode currents in addition to the phase currents *[80]*. Further cheapening the drive using a shunt resistor in the return dc-link path as suggested in *[73]* results in significant power loss and thus can only be useful in small power applications.
Based on the above discussion the UPF rectifier controller and the vector controller for the inverter of the proposed drive (Fig.2.11) has been designed to be free from any measured dc-link currents. This is the reason that a reverse approach to dc-link current estimation from the three-phase current will be used in chapter 5 to design a controller to allow a small dc-link capacitor.

In order to validate the simulation's ability to estimate dc-link currents it is essential to be able to measure currents on either side of the dc-link capacitance. As noted earlier these measurements are not usually taken in commercial drives and this is also the case in the Unidrive. For any inverter designer it is important that the circuit loop between the dc-link capacitor and the converter switching devices should have minimum inductance. Inserting current shunts, or standard hall effect based sensors, in series with the dc-link capacitors increases the loop inductance and can cause voltage overshoot across the converter switching devices. For these reasons the dc-link capacitor is embedded in the drive and is very difficult to reach. A good example of this can be seen in the Unidrive module (Fig.4.5) where the

dc-link capacitor leads are only separated by the thickness of the printed circuit board. The diode rectifier is connected to the dc-link capacitors via a choke inductor.

The compact design means that a normal hall based current sensor can only be used if the component is removed and reconnected using a long enough cable which can be passed through the hall sensor. This would mean a significant increase in the circuit inductance between the power devices and the capacitor and is not considered as an option here.

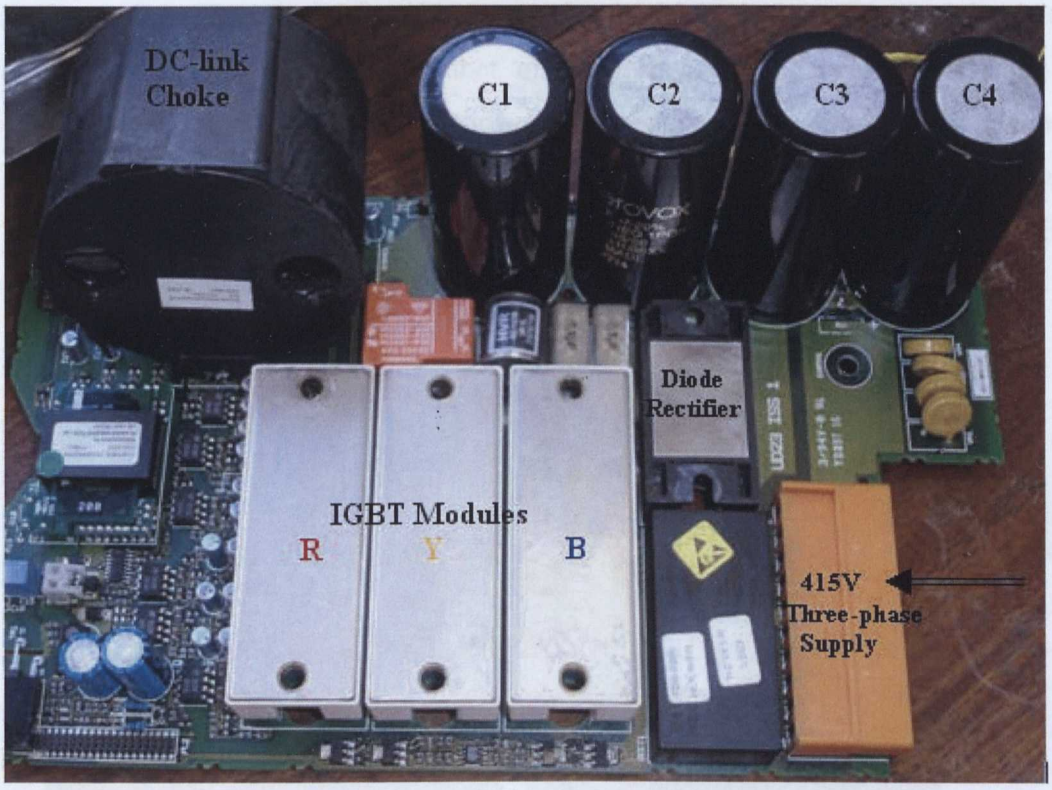


Fig.4.5 Unidrive module showing various components

Initial attempts were made employing flexible Rogowski coils *[82]*. These devices are capable of measuring only short transient dc or ac currents of sufficient frequency because their signal comes from the rate of change of flux linking the coil. The bandwidth of the necessary integrator proved to be too limited to capture all of a typical dc-link "pulse" without significant distortion as shown in Fig.4.13 (b). Perhaps future amplifier developments might allow this type of device to be used and hence allow the advantage of their flexibility to be utilized – for instance it was possible to wrap a Rogowski coil around the leg of a capacitor without disturbing the parent circuit.

A more successful method to measure the rectifier output current and dc-link capacitor currents in the Unidrive was achieved by using an ultra flat open loop integrated circuit current transducer based on the Hall effect principle *[74]*. The drive circuit was modified to allow the use of these sensors in a way that caused a negligible increase in the inductance between the devices and the capacitor. Two miniature current sensors are fitted on main circuit board to measure rectifier output current and dc-link capacitor current. The location of these sensors is shown schematically in Fig.4.3 and physically in Fig.4.6. The rectifier output current measuring sensor is connected by extending the input choke terminals and because it would not significantly affect its number of turns, it barely changes the overall input inductance value. The dc-link capacitor current sensor is connected directly onto the terminal of C4 to minimize the effect of the increased inductance. This capacitor current sensor would only be measuring half the dc-link capacitor current which also helps to minimize the change in the inductance between the capacitors and the IGBT modules.

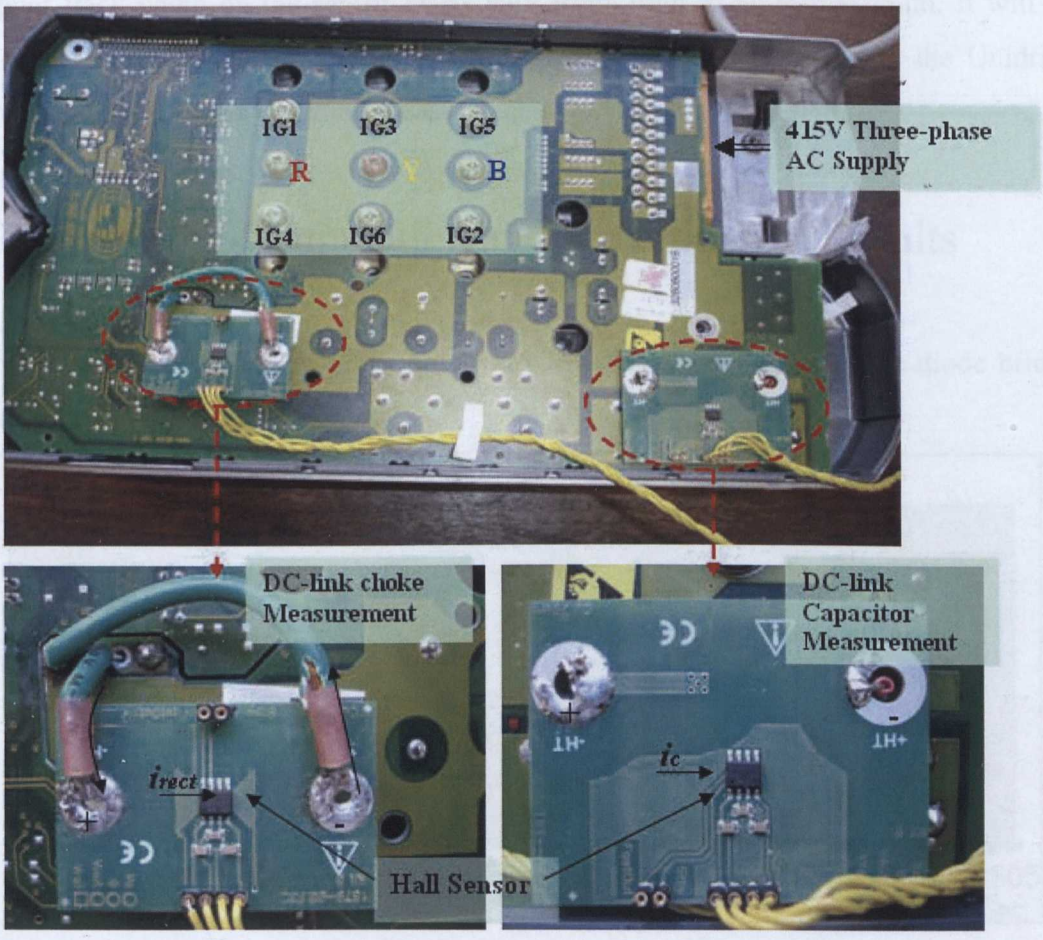


Fig.4.6 Addition of miniature current sensors for rectifier and dc-link capacitor current measurement

The sensor requires an external 5V DC supply and the sensor is mounted directly onto a PCB containing a short element of track. A typical connection arrangement of this current sensor is shown in Fig.4.7.

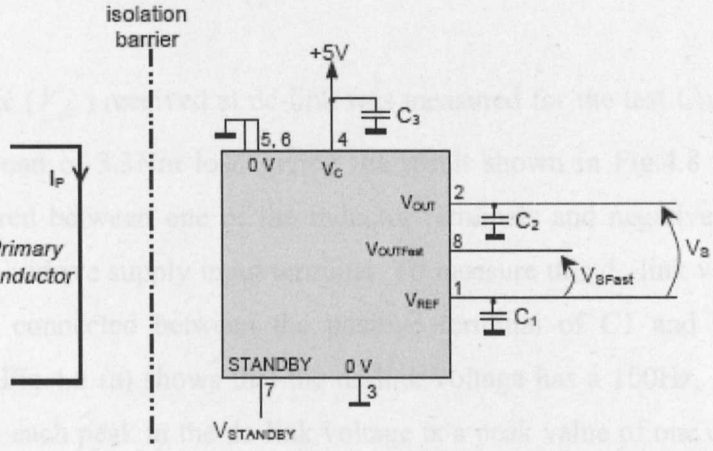


Fig.4.7 Typical connection diagram of current sensor (C1=C3=47nF, C2=4.7nF)

The copper track width on the sensor PCBs vary from 3mm to 8mm maximum. It will be shown in next section that the addition of these two sensors does not affect the Unidrive performance and allows good current measurements.

4.4 Comparison of Simulation and Experimental Results

The three-phase 415V supply voltage is converted to DC using a three-phase diode bridge rectifier inside the Unidrive.

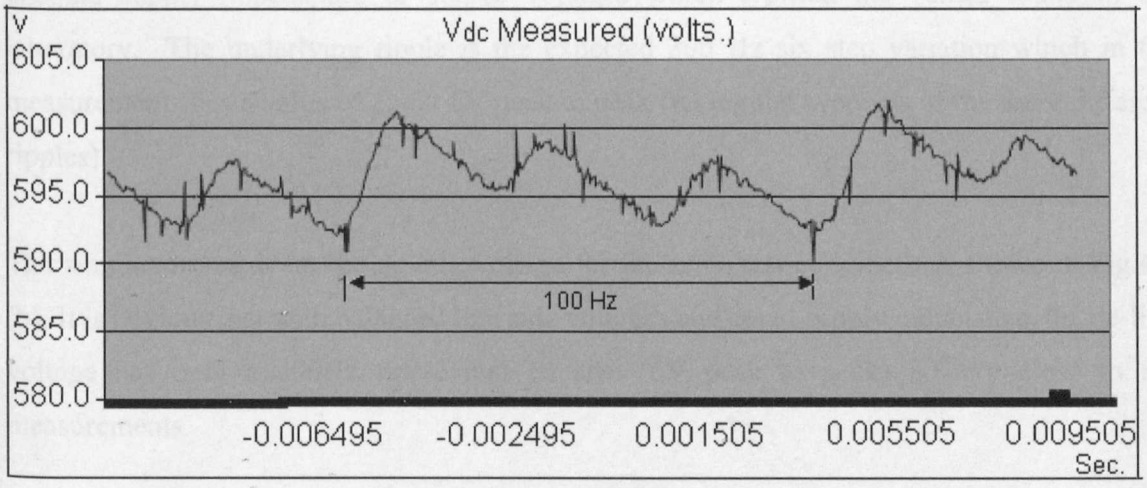


Fig.4.8. (a) DC-Link voltage measurement from test setup [For 3Nm load at 1500rpm]

The peak dc-link voltage is given by

$$V_{dc} = V_{LL} \times \sqrt{2} = 415 \times \sqrt{2} = 586.9 \text{ V}$$

The rectified voltage (V_{dc}) received at dc-link was measured for the test Unidrive running at 1500 rpm, with a load of 3.3Nm load giving the result shown in Fig.4.8 (a). This dc-link voltage was measured between one of the inductor terminals and negative dc-bus terminal which is available Unidrive supply input terminal. To measure this dc-link voltage a standard voltage probe was connected between the positive terminal of C1 and the neutral. The measurement from Fig.4.8 (a) shows that the dc-link voltage has a 100Hz, 10V peak ripple. Or put more simply each peak in the dc-link voltage is a peak value of one of the line to line voltages and the result shows that each peak line to line is different. This ripple could be the result of an unbalanced supply source voltage or unequal supply side phase impedance or both.

At a given load the distinction between unbalanced source voltage or supply impedance is not possible (or relevant). The unbalanced supply is a function of the total instantaneous load in the laboratory at the time of the test and measurement experience showed that the line voltages at the input to the Unidrive had a rather consistent pattern but with constant changes in detail. A decision was made that it would not be possible to exactly replicate the unbalanced supply with any exactitude. The more approximate recourse was to simulate with unequal supply impedances or source voltages which typified the values found in the laboratory. The underlying ripple is the expected 300 Hz six step variation which in the measurements has a value of about 6V peak to peak (taking the averages of the three different ripples).

The simulation result for the dc-link voltage for the same test conditions is shown in Fig.4.8 (b). It is obvious that with balanced line side voltages and equal supply inductance, the dc-link voltage has only a 300Hz ripple and its size (6V peak to peak) is very close to the measurements.

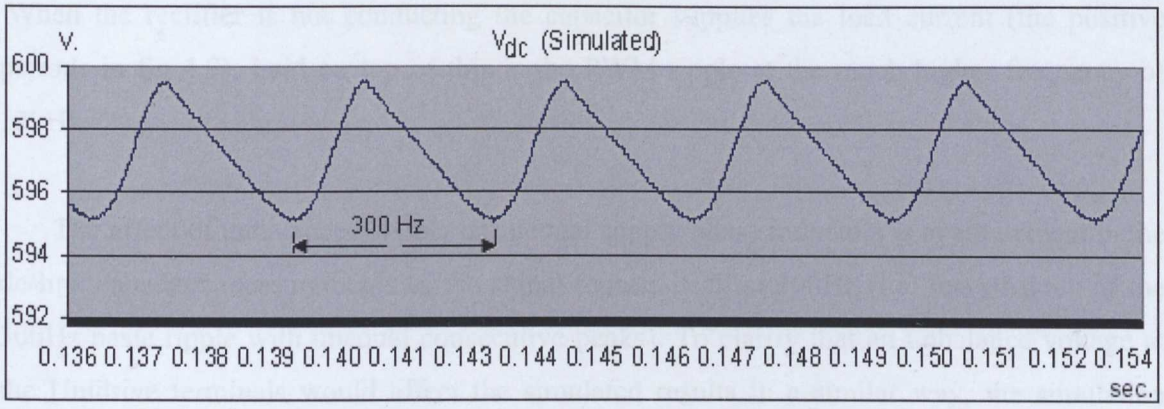


Fig.4.8 (b).Test setup DC-Link simulation results [For 3Nm load at 1500rpm]

To check if unequal supply impedances could result in a similar ripple to the measurements, a simulation with different line inductances on the supply side was carried out. The simulation result (Fig.4.8-c) is very similar to the measurement which confirms that the 100Hz ripple could be because of the differences in the supply side phase inductances.

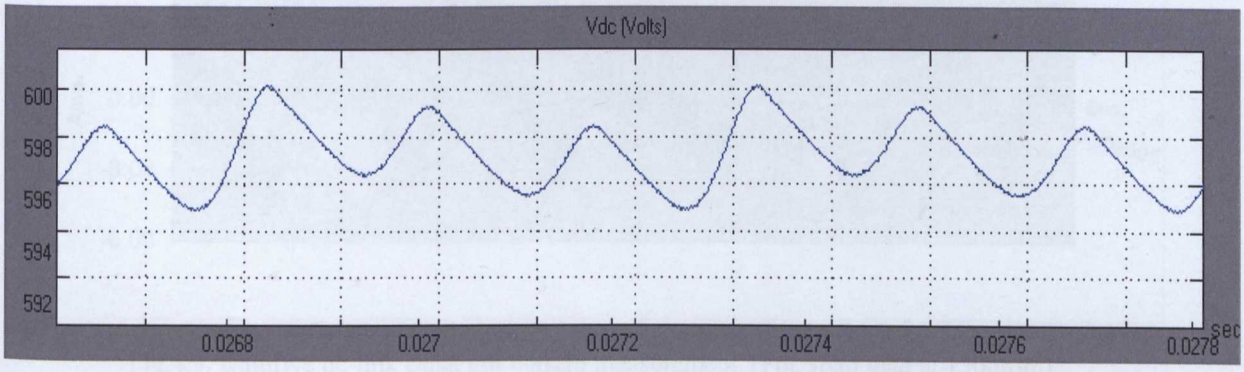


Fig.4.8 (c). Test setup DC-Link simulation results with unequal supply phase inductances [L_R=0.5mH, L_Y=0.8mH, L_B=1mH & 3Nm load at 1500rpm]

The dc-link capacitor current measurement from the current sensors fitted in the Unidrive is shown in Fig.4.9 for a 3Nm load at 1500rpm. In order to help explain the above, following observations can be made. In the steady state the average capacitor current is zero. The (average) DC current being supplied to the load is constant. When the rectifier is conducting the capacitor takes the excess current that is not taken by the load and the capacitor charges (the negative periods in Fig.4.9).

When the rectifier is not conducting the capacitor supplies the load current (the positive periods in fig 4.9). Laid on top of this is the PWM ripple at the much higher frequency of 12kHz.

The effect of unbalanced supply or unequal supply phase inductors is again evident in the dc-link capacitor measurements as the signal repeats itself at 100Hz (i.e. sets of three of the 300Hz basic ripple with unequal consecutive peaks). To clarify that an unbalance voltage at the Unidrive terminals would affect the simulated results in a similar way, the simulation results are presented in Fig.4.10 with supply voltages with unequal peaks. It is clear that just 2V difference in supply voltage peaks can cause a significant change in the dc-link voltage and currents waveforms.

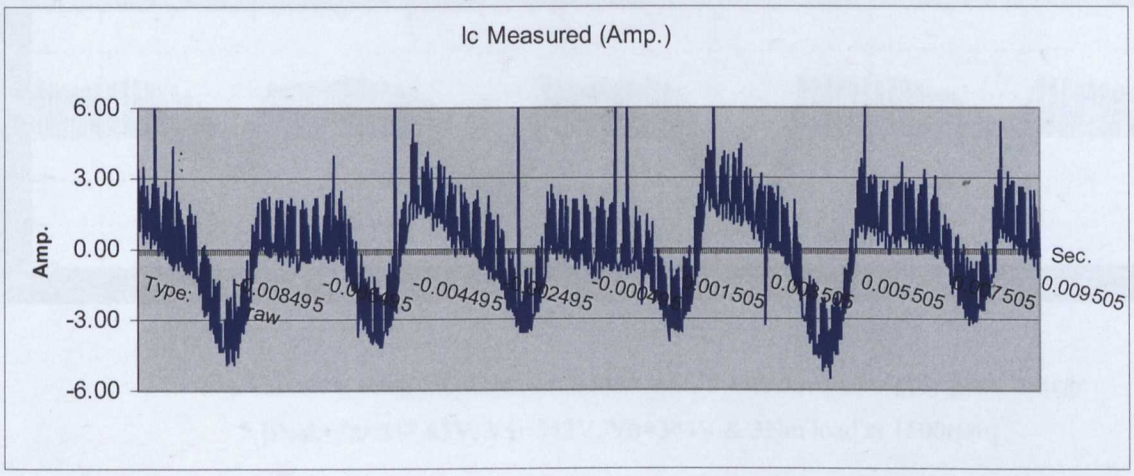


Fig.4.9. Unidrive dc-link capacitor current measurement. [For 3Nm load at 1500rpm]

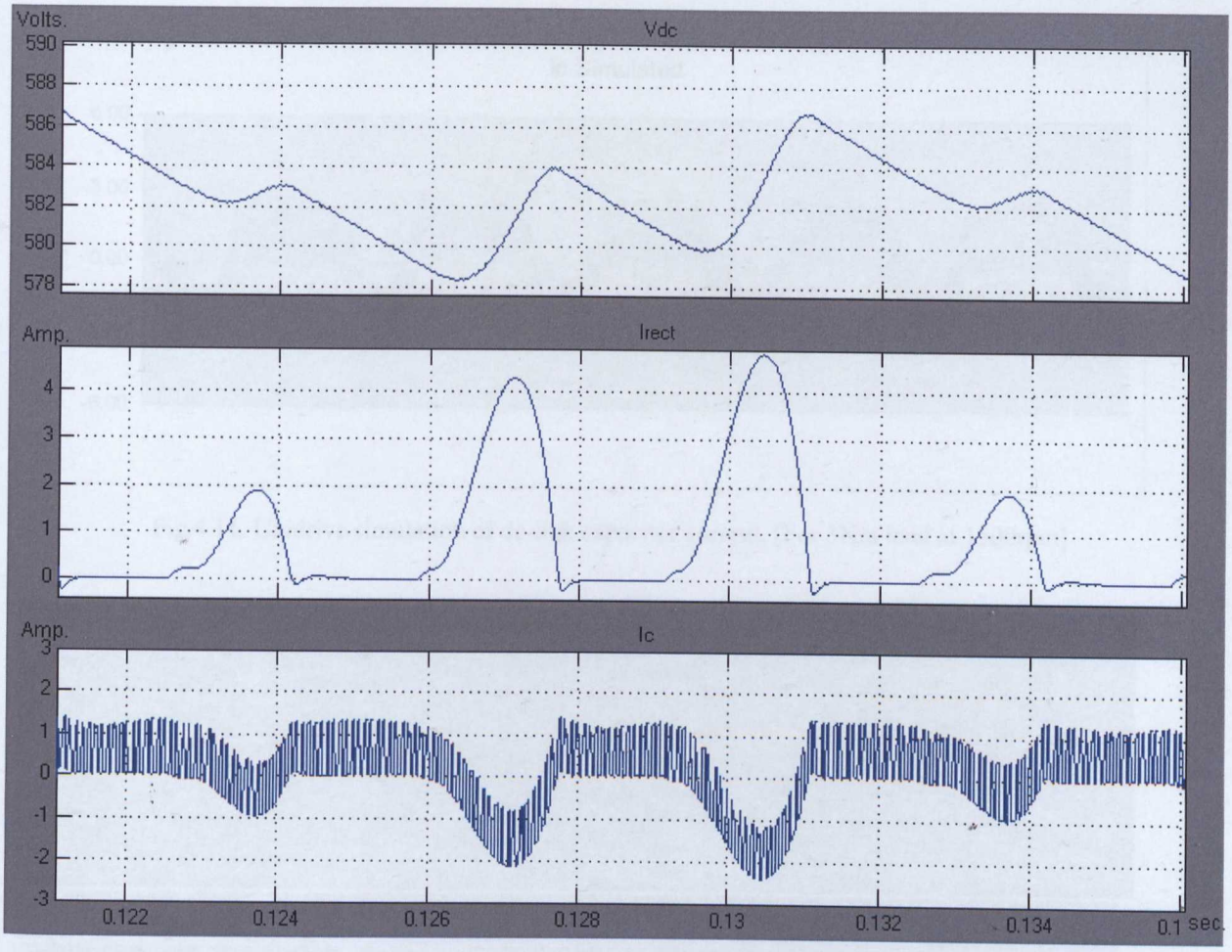


Fig.4.10. Test setup DC-Link simulation results with unequal supply peak voltage [Peak V_R=338.85V, V_Y=342V, V_B=344V & 3Nm load at 1500rpm]

Simulation results of the dc-link capacitor current with perfectly balanced supply voltage and equal line impedances in each phase is shown in Fig.4.11 which clearly does not suffer from the problem of unequal peaks. Concentrating on the 300Hz ripple it is clear that the simulation has good fidelity with the measured results with the peak to peak of the 300Hz ripple being around 4A. Taking a section of the waveform in more detail to allow examination of the PWM elements of the capacitor current gives the results shown in Fig. 4.12. In the section shown the capacitor is seen to be supplying current pulses. Again there is good agreement between simulation and measurement.

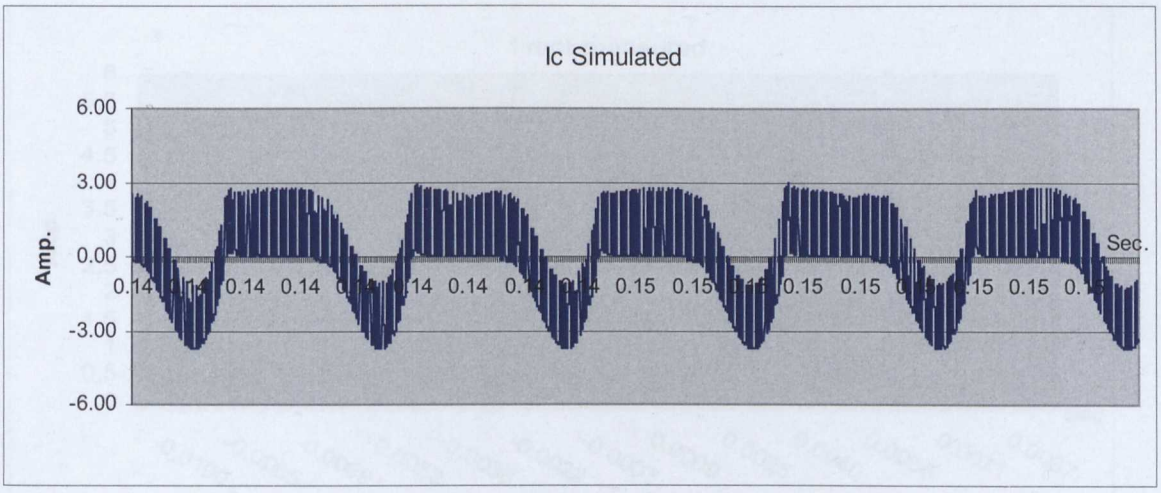


Fig.4.11. Unidrive simulation of dc-link capacitor current. [For 3Nm load at 1500rpm]

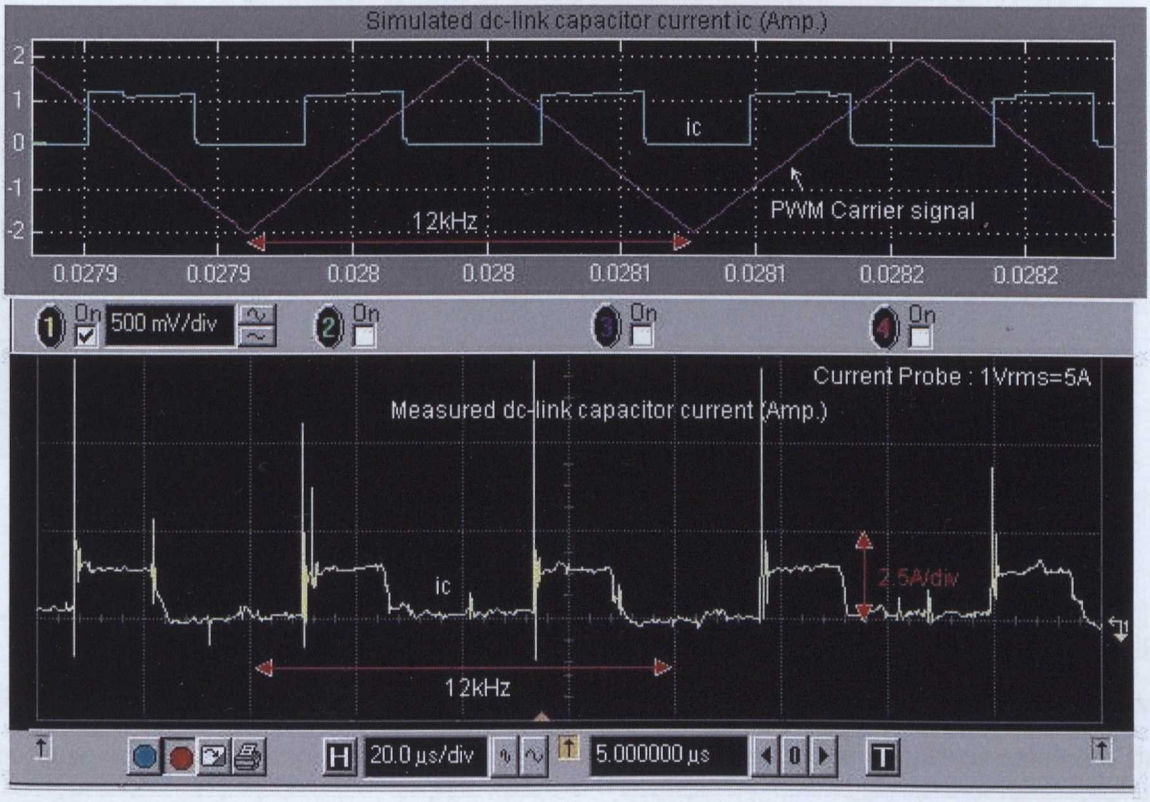


Fig. 4.12 Simulated (top) and measured (bottom) dc-link capacitor current comparison [1500rpm, 3Nm]

The measured signal of Unidrive rectifier output current (i_{rect}) is shown in Fig.4.13(a). This current is reflected in the negative going part of capacitor current (Fig.4.9). The PWM ripple is absorbed by the capacitor and so does not appear on the rectifier side. The uneven peaks of the rectifier current are again caused by supply imbalance.

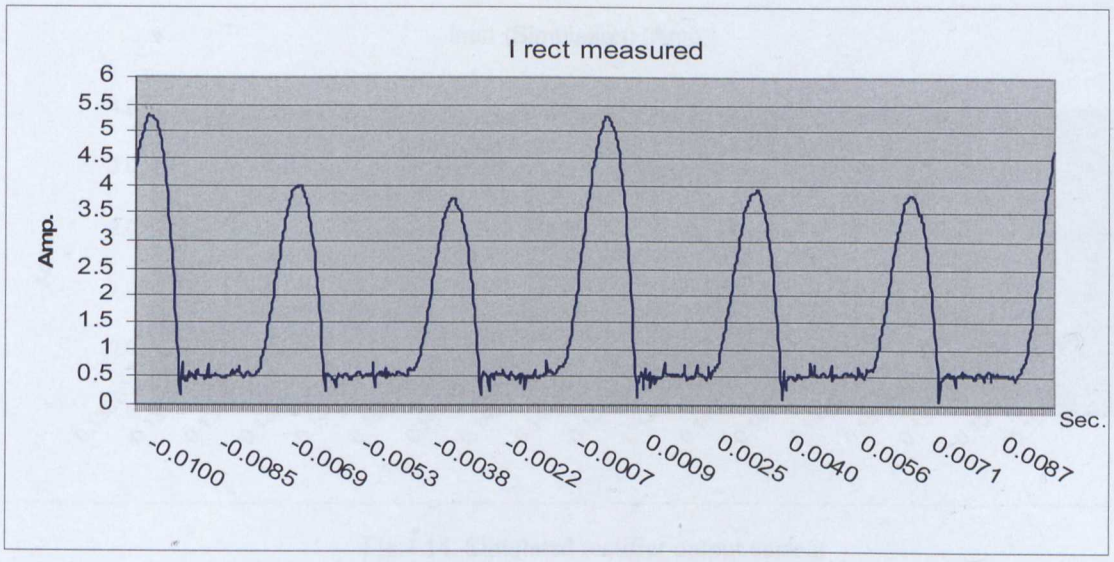


Fig.4.13 (a). Unidrive rectifier output current measurement [For 3Nm load at 1500rpm]

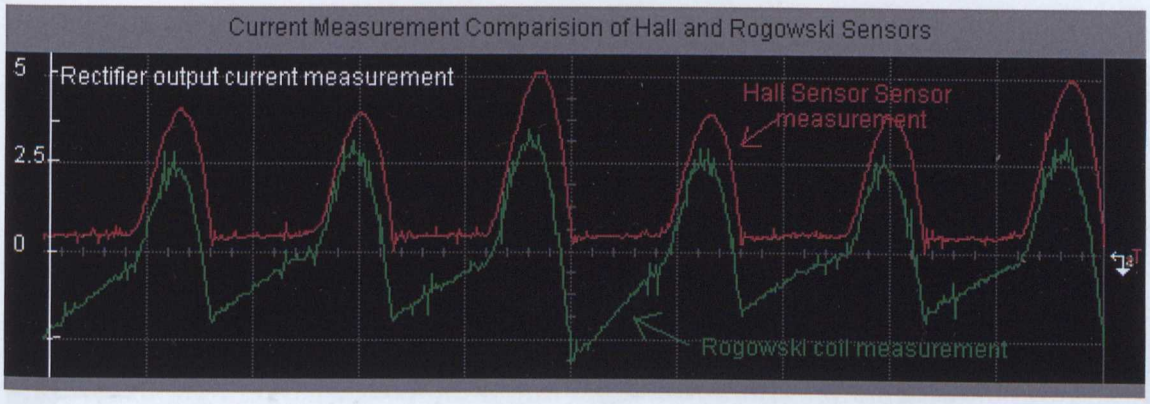


Fig.4.13 (b) Current measurement comparison of Hall sensor and Rogowski coil [For 3Nm load at 1500rpm]

Current measurement from Hall sensor probe as well as Rogowski coil are shown in Fig.4.13 (b) to illustrate how Rogowski measurement produces negative rectifier wave because of flux integrator operational amplifier. Fig.4.14 shows the simulated result for the rectifier current which is calculated for ideal input supply voltages. The magnitude and shape of these simulated rectifier current pulses is very close to the average of the measured rectifier current pulses.

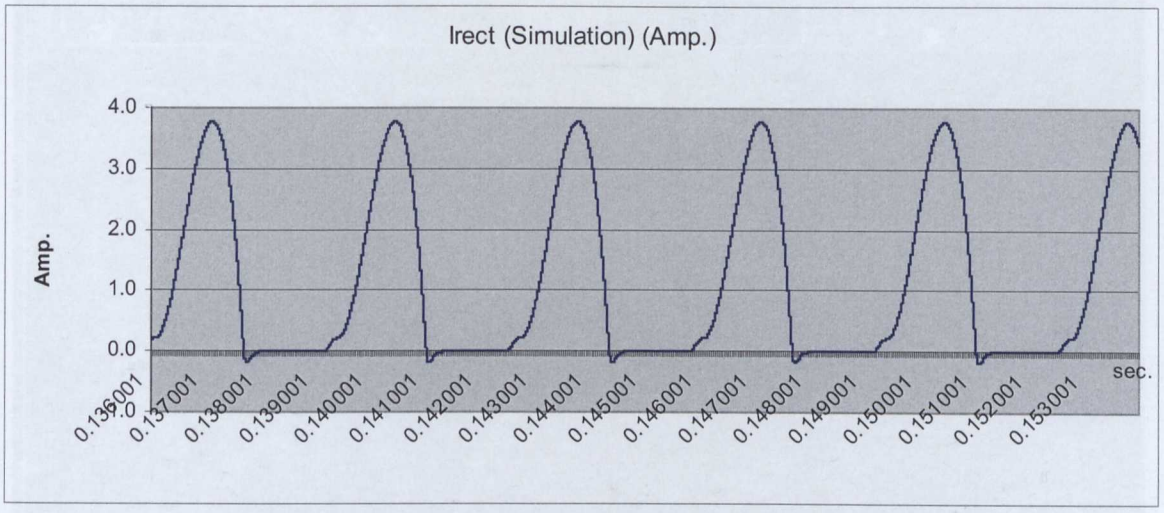


Fig.4.14. Simulated rectifier output current

Once again effect of unequal supply phase inductance is shown on rectifier output current in Fig.4.15 showing the typical pattern for the unbalanced supply.

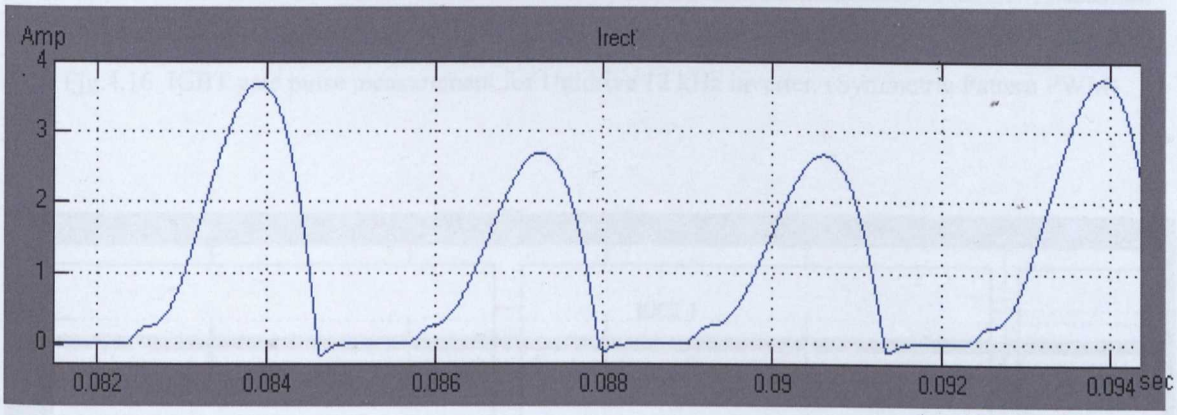


Fig.4.15. Simulation results of rectifier output current with unequal supply phase inductances [L_R=0.5mH, L_Y=0.8mH, L_B=1mH & 3Nm load at 1500rpm]

To verify that the switching methodology used for simulation as described in Chapter 3 is correct, the gate switch pulse from the Unidrive inverter have been measured and compared with the simulation results for the inverter gate pulses. The Unidrive pulse pattern arises from the symmetrical PWM method as discussed in Chapter 3 and the measurements are shown in Fig.4.16. The 12 kHz inverter switching (as used in the Unidrive) has been simulated with the result shown in Fig.4.17. This measurement confirms the sequence generated by the inverter PWM modulation is accurately modelled in the simulation and hence verifies the control and modulation model in the simulation.

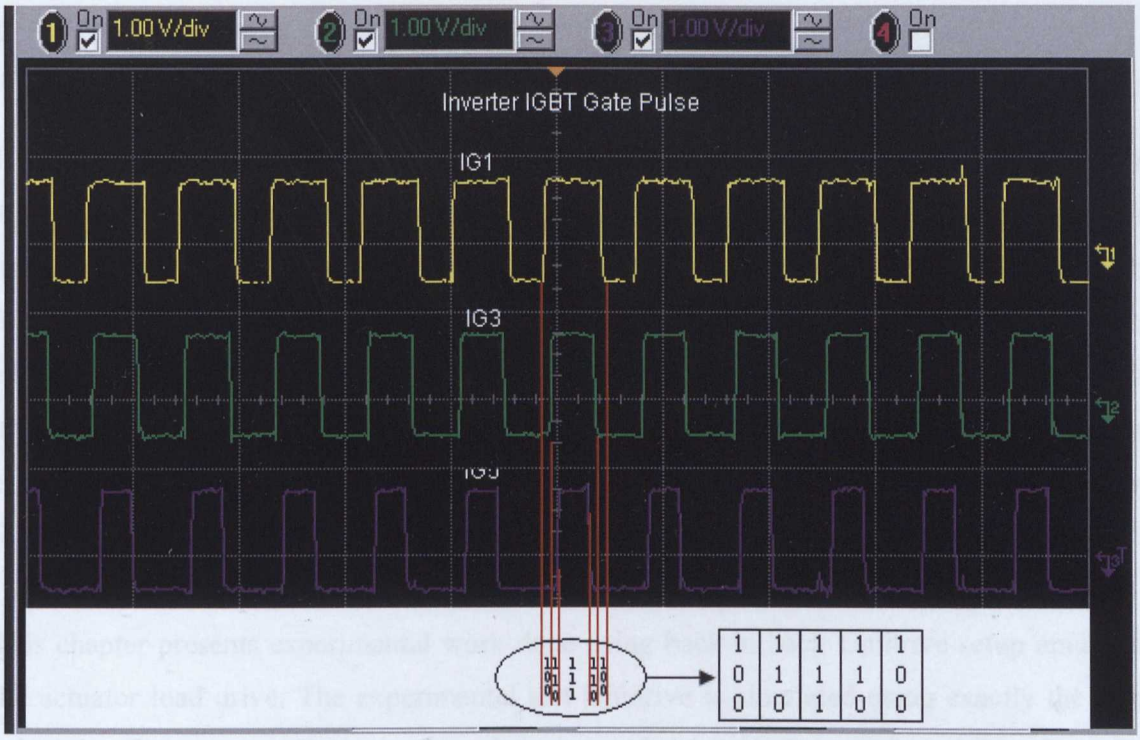


Fig.4.16. IGBT gate pulse measurement for Unidrive 12 kHz inverter. (Symmetric Pattern PWM)

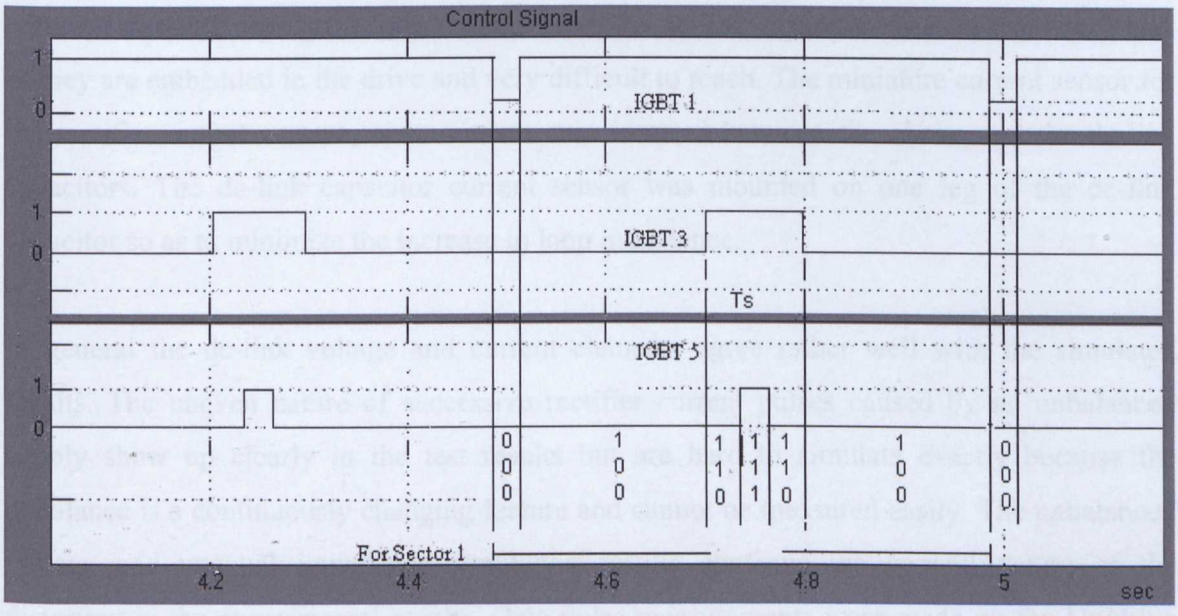


Fig.4.17. IGBT gate pulse from Unidrive inverter simulation (Symmetric Pattern PWM)

4.5 Conclusions

This chapter has been concerned with proving that the simulation system was accurate before it was used to examine a control strategy for reducing the size of the dc-link capacitor. The limitations of practicality meant that the test drive used a diode rectifier as opposed to the fully switching inverter which is the proposed target drive for the capacitor reduction exercise. None the less the drive measured and simulated used the switching strategy of the inverter proposed for the new drive and it has proven possible to measure dc-link current components with good accuracy but still not good enough to recreate supply phase currents for use in rectifier/inverter controller.

This chapter presents experimental work done using back to back Unidrive setup emulating the actuator load drive. The experimental test Unidrive is simulated using exactly the same principles that were used to simulate the proposed drive in Chapter 2 and Chapter 3.The output results of the test drive simulation confirms the simulation method and models. The difficulties with measuring dc-link currents associated with avoiding the introduction of inductance between the capacitors and the inverter have been overcome using miniature current sensors. Keeping the loop inductance to the dc-link capacitors is a far from easy task as they are embedded in the drive and very difficult to reach. The miniature current sensor for the rectifier output current measurements was inserted between the choke and the dc-link capacitors. The dc-link capacitor current sensor was mounted on one leg of the dc-link capacitor so as to minimize the increase in loop inductance.

In general the dc-link voltage and current elements agree rather well with the simulated results. The uneven nature of successive rectifier current pulses caused by an unbalanced supply show up clearly in the test results but are hard to simulate exactly because the unbalance is a continuously changing feature and cannot be measured easily. The unbalanced voltage and unequal impedance simulation results confirms the general nature of the distortion in the experimental results. Gate pulse measurements were made on the Unidrive inverter devices and compared with the simulated pulse pattern. The good agreement with these gate pulse measurements verifies that the simulation of the symmetric pulse pattern control has good fidelity with practice.

It is also clear from the measurements that drive control based on dc-link current sensing is very unreliable. Unequal supply phase impedances and unbalanced supply voltages cause significant changes in the dc-link signals and should not be used to reconstruct or estimate phase currents for control purposes to achieve reduction in dc-link capacitor size. The simulation and experimental results in this chapter encourages the formulation of a control methodology free of dc-link current sensors. The next chapter discusses a dc-link current estimation based method in partnership with a fully switched rectifier whose control is modified so as to achieve a significant reduction in the necessary size of the dc-link capacitor.

CHAPTER 5

DC-LINK ANALYSIS

5.1 Introduction

Previously Chapter 3 demonstrated the simulation of a permanent magnet three phase dc-link drive supplying an actuator with a rated load of 3.4Nm at 10000rpm via a gearbox assembly for various load cases. The measurements on a commercial dc-link converter in Chapter 4 verified the simulation philosophy developed in Chapter 3. This chapter uses the simulation system of Chapter 3 to present a case for the three phase dc-link drive with a fully switching input converter as the drive for a flap actuator (as proposed in Chapter.2 Fig.2.11). As mentioned before the flap actuator drive using multiple single phase inverters (presented in Fig.2.10 *[16]*) requires a $950\,\mu$F dc-link capacitor per phase while the three-phase PM SPWM controlled drive simulation results presented in Chapter 3 were carried out with a dc-link capacitor of $1000\,\mu F$. As discussed in Chapter.2 various research publications suggested ways to reduce the size of dc-link capacitor by changes in control or hardware. This chapter will analyze the effect of various parameters on the necessary size of the dc-link capacitor and a switch prediction methodology is proposed which matches the input and output demands of the dc-link thereby allowing a reduction in the size of dc-link capacitor. This chapter will explore the dependencies of the dc-link capacitor size on drive parameters and the effect of supply unbalance on the drive stability. The chapter will demonstrate the possibility of a very small dc-link capacitor and its limitations in respect of aircraft power quality standards. A small dc-link capacitor makes it feasible to use a highly reliable capacitor technology to achieve flight dispatch reliability specifications without the redundancy that was needed in the previous arrangements. This in turn makes the system simpler, smaller and lighter – all significant advantages.

5.2 The Effect of Reducing DC-Link Capacitor and Supply Inductance on the Drive Performance

When the target three-phase PMSM drive is supplying a constant torque of 3.4Nm at rated speed, the motor output mechanical power P_{mech} is constant as is the three phase resistive loss P_r in the motor. Due to the switching nature of the inverter bridge, the inductive component of the power (P_L) that flows in and out of the motor is pulsed. If the inverter's internal losses can be ignored then the addition of these three motor powers components would be equal to the power supplied by the dc-link (P_{dc}) to the inverter.

So
$$P_{dc} = P_r + P_L + P_{mech} = V_{dc} i_{dc} \tag{5.1}$$

Similarly from the supply end, the power input to the drive can be equated to:-

$$P_{in} = P_{Lr} + P_{rec} \tag{5.2}$$

Where
$$P_{rec} = P_c + P_{dc} \tag{5.3}$$

The power P_{in} is the input from the aircraft power supply P_{Lr} is the pulsed rectifier inductive power and P_c is the power to the dc-link capacitor. It is as expected that the drive operation at rated speed and rated load with a fully pre-charged (460 V) dc-link capacitor of as high a value as 5000μF (Fig.5.1) would be quite smooth because this big capacitor provides significant isolation between the rectifier and the inverter stages. The dc-link variation ($\frac{dV_{dc}}{dt}$) with C=5000μF as predicted by simulation is very low (note the truncated zero in the figure), as expected as is shown in Fig.5.1. The unity power factor (UPF) controller of the rectifier bridge in Fig.3.37 can easily handle this low $\frac{dV_{dc}}{dt}$ and this causes only a small ripple in the reference voltage signal (M<1) and in the supply currents.

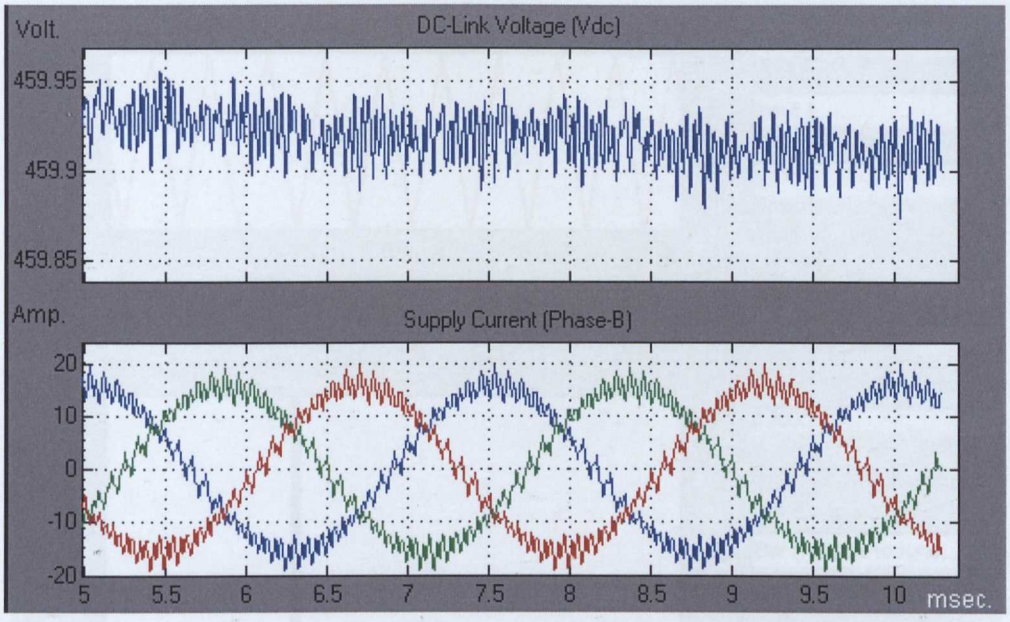


Fig.5.1. DC-Link voltage and supply currents for conventional drive with 5000μF dc-link capacitor

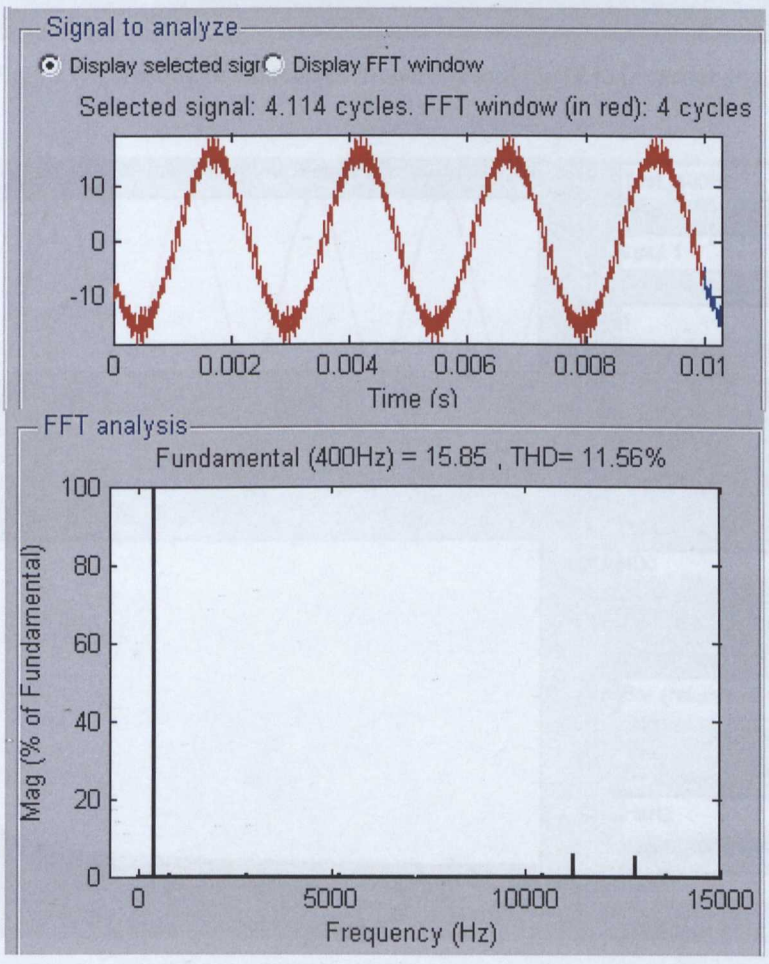


Fig.5.2 (a) FFT analysis of supply phase-B current for conventional drive with 5000μF dc-link capacitor

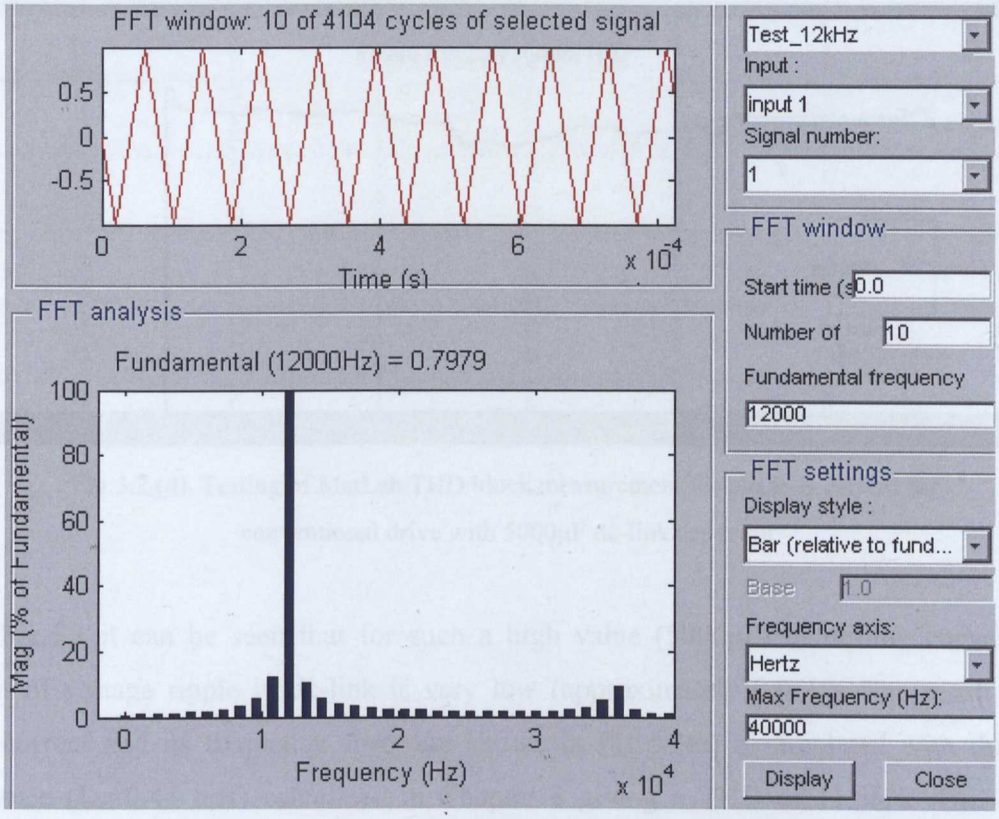


Fig.5.2 (b). Testing of MatLab FFT analysis tool for 12 kHz carrier signal

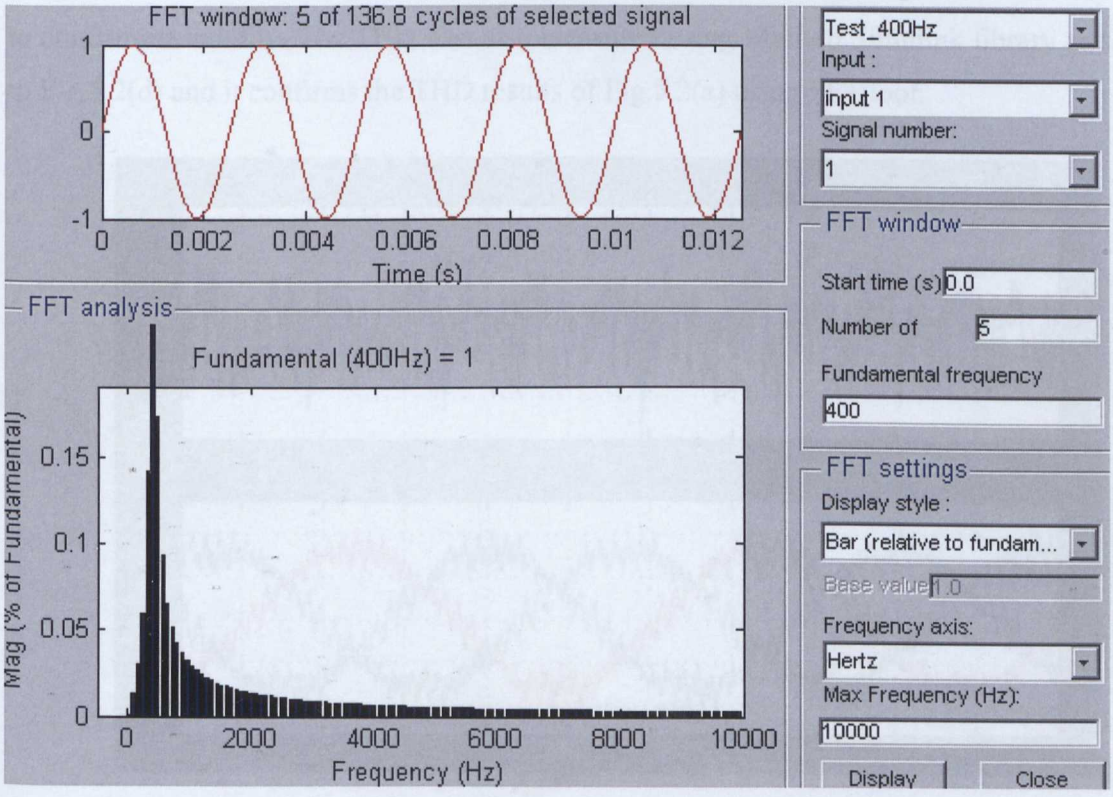


Fig.5.2 (c). Testing of MatLab FFT analysis tool for 400Hz signal

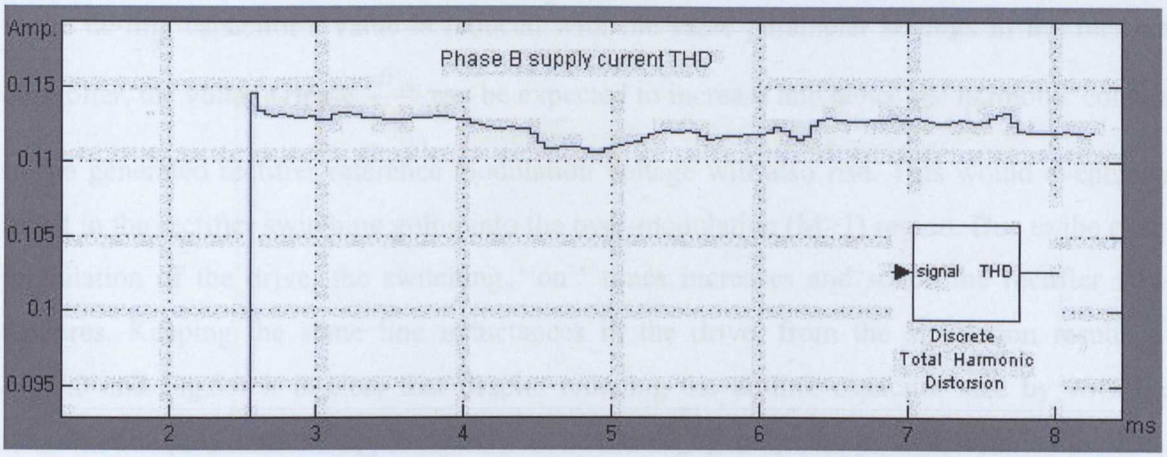


Fig.5.2 (d). Testing of MatLab THD block measurement for phase-B current for conventional drive with 5000μF dc-link capacitor

From Fig.5.1 it can be seen that for such a high value (5000μF) of dc-link capacitor the amount of voltage ripple in dc-link is very low (approximately 0.05V). The result for the phase current and its frequency spectrum shown in Fig.5.2(a) is simulated with the phase inductance (Ls=0.44 mH) calculated in Chapter 3 giving a THD of 11.56%. The 12 kHz switching frequency ripple can be seen in Fig.5.2 (a). A quick test of MatLab FFT analysis tool is done as shown in Fig.5.2 (b) and Fig.5.2(c) for 12 kHz carrier signal and 400Hz signal to confirm its validity. The THD was also measured using MatLab Simulink library as shown in Fig.5.2(d) and it confirms the THD results of Fig.5.2(a) using FFT tool.

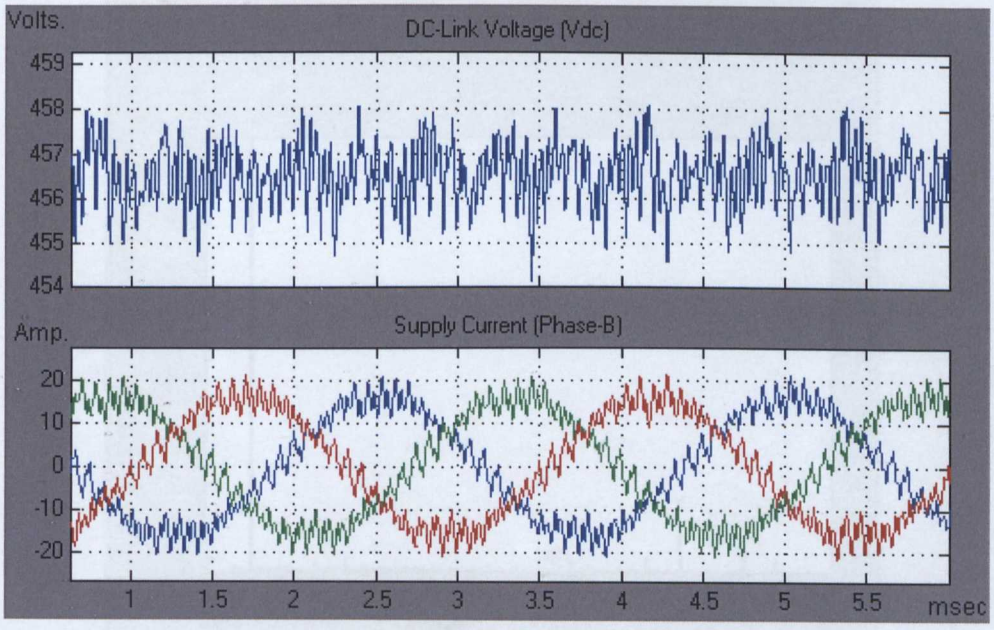


Fig.5.3. DC-Link voltage and supply currents for conventional drive with 100μF dc-link capacitor

If the dc-link capacitor's value is reduced with the same parameter settings in the rectifier controller, the voltage ripple $\frac{dV_{dc}}{dt}$ can be expected to increase and hence the harmonic content of the generated rectifier reference modulation voltage will also rise. This would eventually result in the rectifier switching going into the over-modulation (M>1) region. Due to the over-modulation of the drive, the switching ''on'' times increases and so do the rectifier volt-amperes. Keeping the same line inductances in the drive, from the simulation results of Fig.5.3 and Fig.5.4 it is clear that despite reducing the dc-link capacitor size by 98% the maximum supply current ripple content is increased by only about 50% with stable drive operation. So it can be argued that the reduction of dc-link capacitor has a relatively small effect on the supply current harmonics.

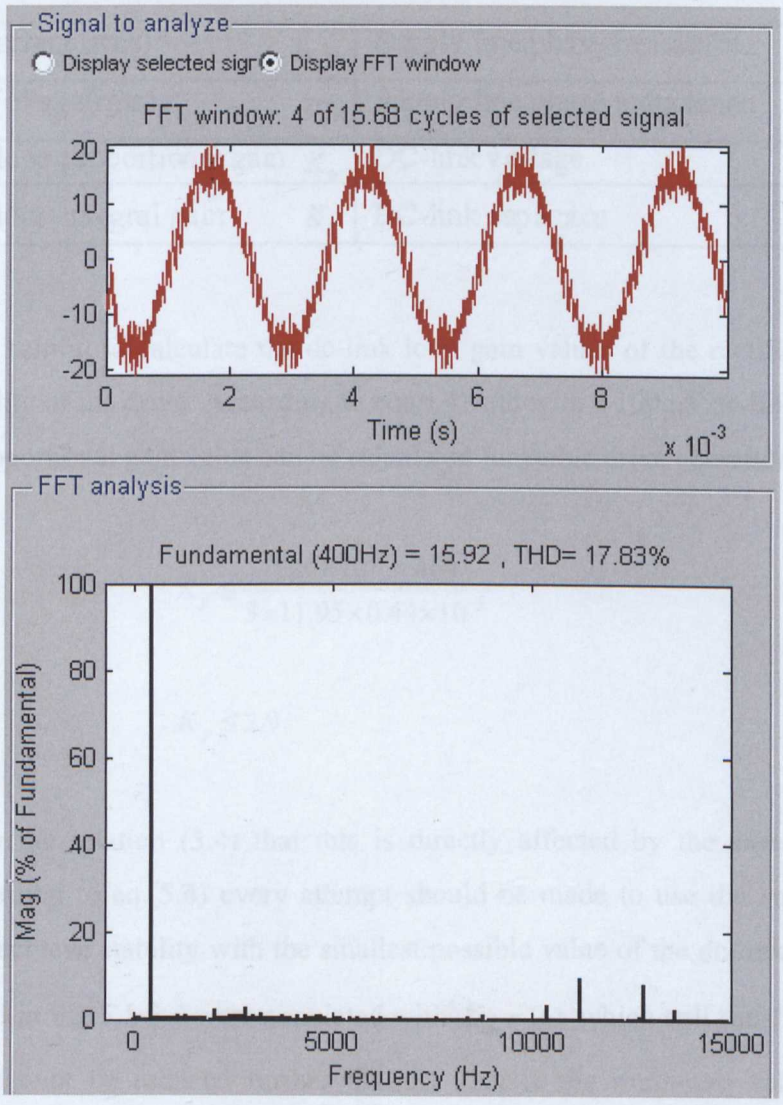


Fig.5.4. FFT analysis of supply phase-B current for conventional drive with 100μF dc-link capacitor

If the dc-link capacitor value is reduced further there comes a point when the drive falls out of stability. The stability criteria for a three-phase fully controlled rectifier can be inferred from *[98]* and *[99]*. According to *[98]* a relation is suggested between the various drive parameters as:

$$i_{s(rms)} \leq \frac{C.V_{dc}}{3.K_p.L_s} \tag{5.4}$$

$$i_{s(rms)} \leq \frac{K_p.V_s}{2RK_p + .L_s.K_i} \tag{5.5}$$

Where

Supply current (rms)	$i_{s(rms)}$	Supply line phase resistance	R
Supply Voltage(rms)	V_s	Supply line phase inductance	L_s
DC-link loop proportional gain	K_p	DC-link voltage	V_{dc}
DC-link loop integral gain	K_i	DC-link capacitor	C

This relation is helpful to calculate the dc-link loop gain values of the rectifier controller to ensure the stability of the drive. According to eq.(5.4) and with a 100 μF dc-link capacitor, the approximate proportional gain value can be calculated for stable drive operation as:

$$K_p \leq \frac{100\times10^{-6}\times460}{3\times11.95\times0.44\times10^{-3}}$$

So

$$K_p \leq 2.9$$

It is clear from the relation (5.4) that this is directly affected by the size of the dc-link capacitor. According to eq.(5.4) every attempt should be made to use the smallest possible value of K_p to achieve stability with the smallest possible value of the dc-link capacitor. The results presented in Fig.5.1-5.4 were simulated with $K_p = 2.1$ which still satisfies the stability criteria but it cannot be reduced further because that is the minimum value required to maintain a near 460V dc-link voltage.

Now again eq.(5.4) can be used for $K_p = 2.1$ (say for $\Delta V_{dc} = 6V$) to calculate the approximate minimum dc-link capacitor as:

$$C \geq \frac{3 \times 11.95 \times 2.1 \times 0.44 \times 10^{-3}}{(460+6)} = 71\mu F$$

$$C \geq 71\mu F$$

So according to the stability calculations above for $K_p = 2.1$ the drive would become unstable for dc-link capacitor values below approximately 71 μF.

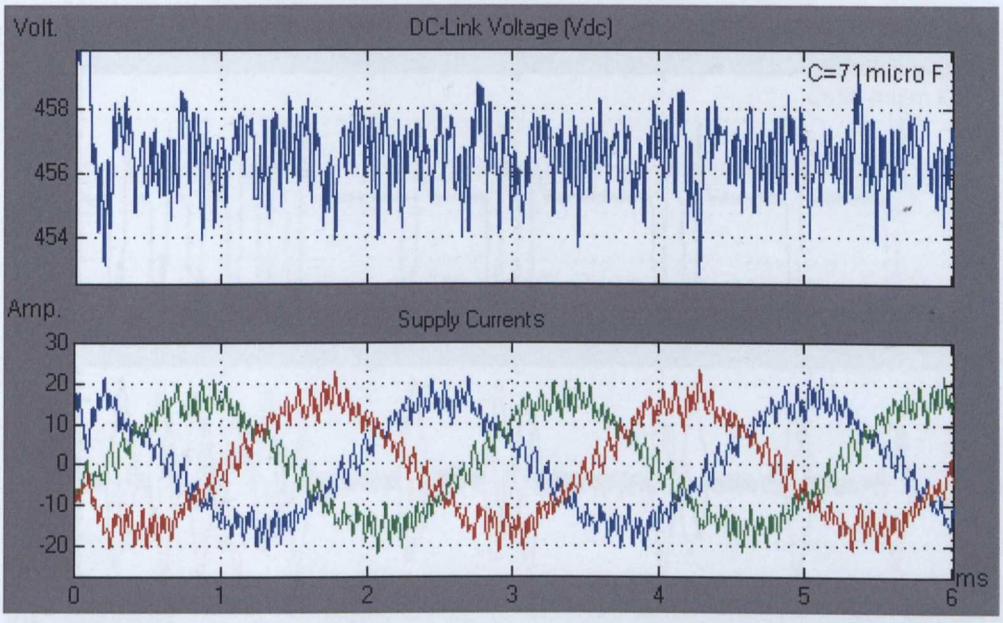


Fig.5.5 DC-Link voltage and supply currents with 71 μF dc-link capacitor, Ls=0.44mH.

With a marginally sufficient value of the dc-link capacitor the drive still manages to remain stable with unity power factor at the rectifier side and vector control at the inverter side. As shown in Fig.5.5, the dc-link voltage and the supply current ripple with 71μF in dc-link are significantly more in comparison to the results obtained with 5000μF. Note that there is little change in the power supplied by the dc-link to the inverter (P_{dc} is unchanged apart from some small disturbances) for the same load at rated speed.

Below C=71μF, the voltage ripple ($\frac{dV_{dc}}{dt}$) gradually increases and no longer satisfies the specified voltage ripple criteria of $\Delta V_{dc} = 6V$. Until the drive has insufficient capacitance between rectifier and inverter units, it maintains an appropriate power flow in and out of the dc-link capacitor. Therefore ideally for a complete switching cycle the average power flow through the dc-link capacitor equates to zero. At very low capacitor values such as 50μF, the reference signal and current harmonics are so high that the rectifier and inverter controller can no longer maintain the stability of the drive. Below 71μF for the same rectifier controller and drive parameters, the dc-link becomes unstable and with it the whole drive as shown in Fig.5.6 for the case of a 50μF capacitor.

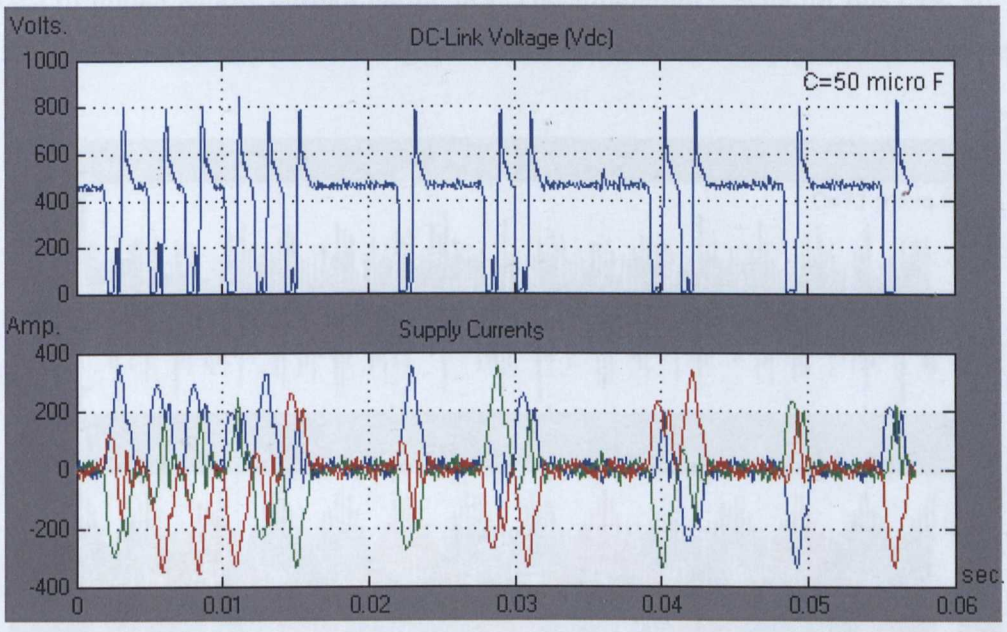


Fig.5.6 DC-Link voltage and supply currents with 50 μF dc-link capacitor

The simulation results above indicate that for a three-phase PMSM drive running at rated speed and supplying rated load torque, the acceptable dc-link capacitor value heavily depends on the rectifier control. It is very important to note here that the analysis presented before to calculate the minimum dc-link capacitor value is by no means sufficient in practice because it does not include the effect of the strict supply quality standards specified for a particular application. In the case presented here the aircraft power supply specification standards are considered in the following sections to determine the minimum dc-link capacitor value.

As discussed in Chapter.3 for fault current limitations the supply filter inductor voltage drop is kept near to 0.1p.u which might not be large enough to satisfy the aircraft supply specifications. From eq.5.4 it is clear that the dc-link capacitor value heavily depends on the supply phase inductance (Ls). To understand the effect of supply inductance on the dc-link capacitor size, consider the case of a lower input inductor in the supply phases. This drive would have a higher supply current harmonic content (THD) and this would force the rectifier controller PWM to go into the over-modulation region (M>1) thus further increasing the switching ''on'' times. Increased switching ''on'' times increases the volt-ampere rating of the rectifier. But on the other hand a reduction in the supply inductance causes the inductive power component P_{Lr} to go down. This means that for a reduced supply inductance, the dc-link voltage ripple is comparatively reduced and this might allow a reduction in capacitor size at the cost of higher supply current harmonics. The simulation results for this case are shown in Fig.5.6 which can be compared to Fig.5.5 for the same value of capacitor in the dc-link.

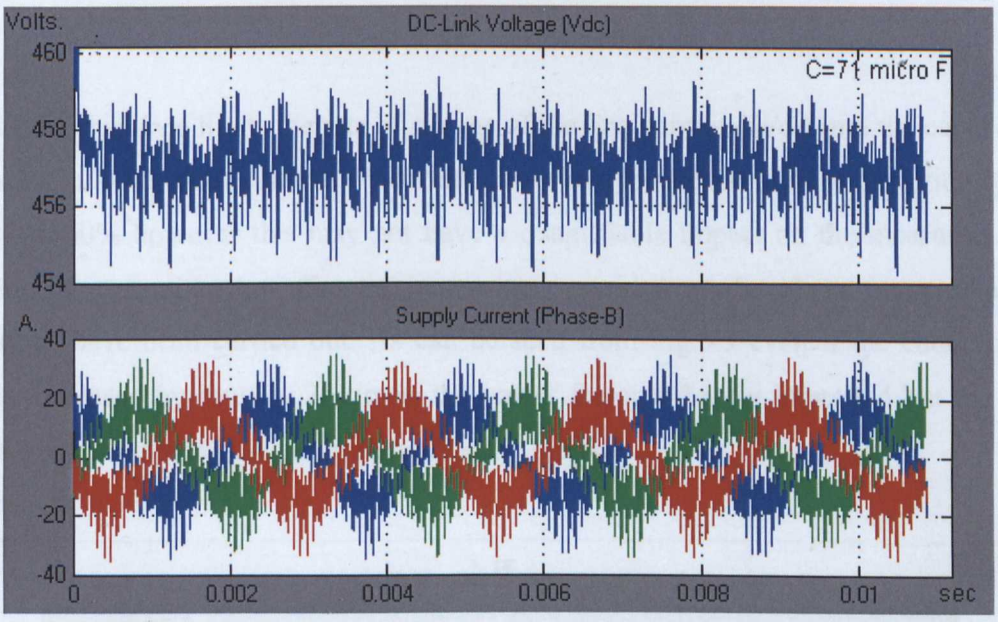


Fig.5.7 DC-Link voltage and supply currents with C=70 μF and Ls= 0.1mH

The impact of reducing the supply side inductance is that far higher currents follow a short circuit in the input converter. The supply inductance is not in the scope of this study and hence it will not be considered as an option for reducing the dc-link capacitance, but a minimum supply inductance value is determined later in this chapter to satisfy aircraft supply standards.

5.3 Effect of a Filter Choke in the DC-Link

In section 5.2 the effect of supply inductance on the stability and control of the three-phase PMSM drive was discussed. A possible alternative to line-side inductors can be the introduction of a dc-link choke to improve the input current waveform and reduce dc-link voltage ripple. The choke is placed after the rectifier and before dc-link capacitor and it performs in a very similar way to the supply-side inductance. It is less expensive and smaller than three phase line side inductors *[83]*.

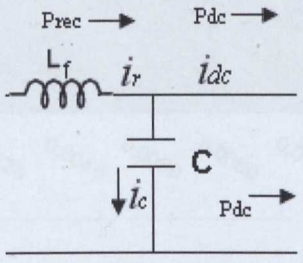


Fig.5.8. DC-Link with choke

The added inductance limits the rate of change of the line current (di/dt) into the capacitor and this results in lower peak currents. A dc-link choke can reduce the current distortion typically by 40% to 60% however this may not have a quantifiable impact on the measured voltage distortion. To examine the effect of increasing the value of the choke inductor a set of simulations have been carried out. As can be seen from Fig.5.9 even if the choke inductor value is increased by roughly 25 times, the power factor is barely improved but the dc-link currents are maintained within increasingly strict limits.

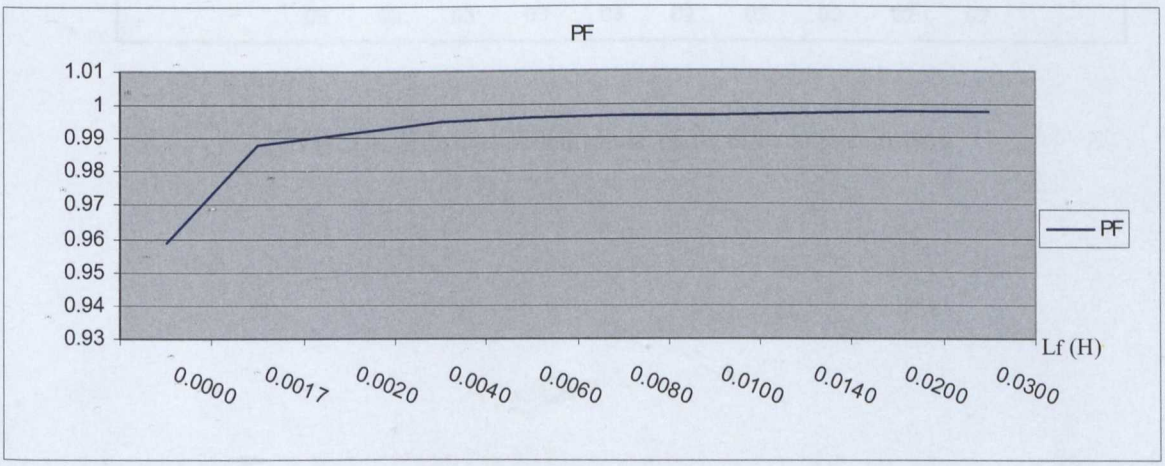


Fig.5.9. Effect of DC-Link choke on power factor

The effect of an increased choke can be seen on the supply currents in Fig.5.10 and on the rectifier output currents in Fig.5.11. There is significant reduction (about 40%) in peak supply and rectifier currents.

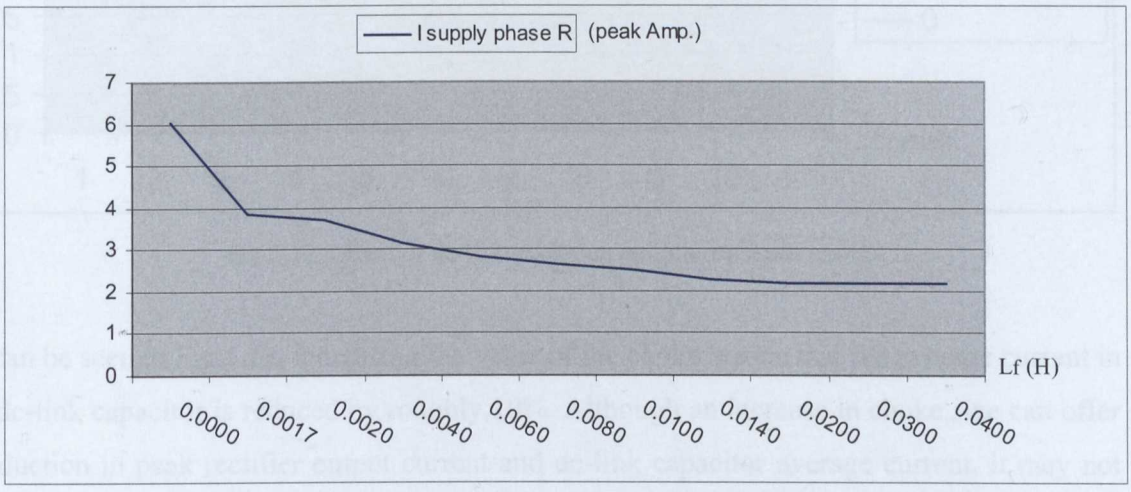


Fig.5.10. Effect of dc-link choke on supply currents

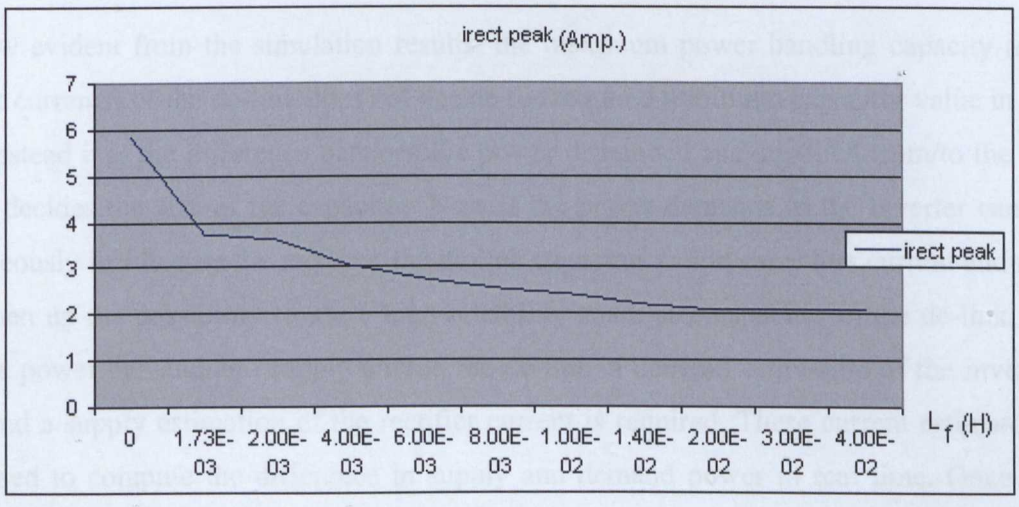


Fig.5.11. Effect of dc-link choke on rectifier output currents

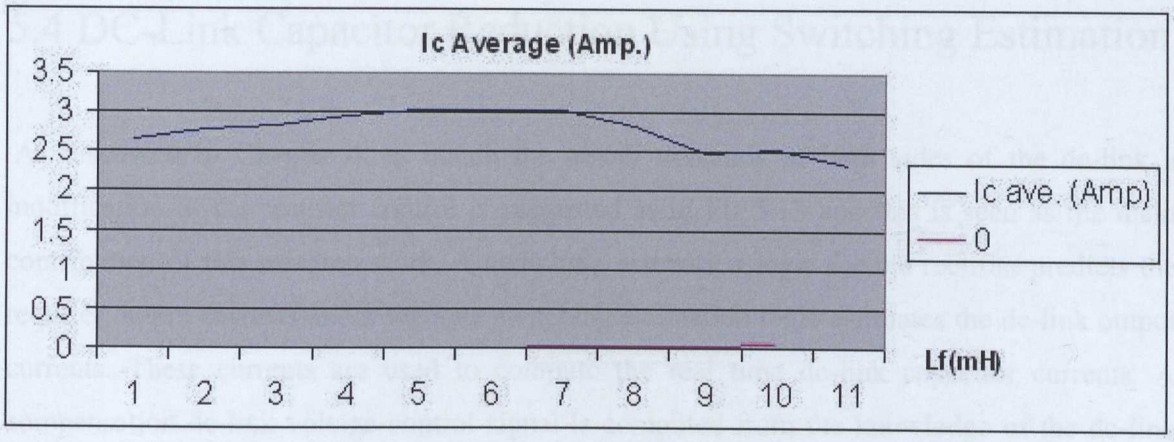


Fig.5.12. Effect of dc-link choke on dc-link capacitor current

As can be seen in Fig.5.12, increasing the value of the choke means that the average current in the dc-link capacitor is reduced by roughly 10%. Although an increase in choke size can offer a reduction in peak rectifier output current and dc-link capacitor average current, it may not have a quantifiable impact on the voltage distortion therefore it cannot be considered as an aid to reduce the dc-link capacitor's size.

As is now evident from the simulation results, the maximum power handling capacity (and thus peak currents) of the dc-link does not decide the required minimum capacitor value in the dc-link instead it is the difference between the power demanded and supplied from/to the dc-link that decides the size of the capacitor. Now if the power demands to the inverter can be instantaneously fulfilled by the rectifier, the dc-link capacitor would carry less current and this would open up the possibility to use a high reliability small size capacitor in the dc-link. To match the power demand and supply around the dc-link, a demand estimation of the inverter current and a supply estimation of the rectifier current is required. These current estimations can be used to compute the difference in supply and demand power in real time. Once the difference between supply and demand power is known it can be used to modify the rectifier dc-link voltage control so as to null the difference between supply and demand. This power estimation requires a detailed understanding of the switching pattern of both the rectifier and inverter bridges.

5.4 DC-Link Capacitor Reduction Using Switching Estimation

As discussed in Chapter 4, to match the power demands of both sides of the dc-link a modification of the rectifier control is suggested as in Fig.5.13 and this is seen as the main contribution of this research work. A switching estimation logic for the rectifier predicts the rectifier output currents and a separate switching estimation logic estimates the dc-link output currents. These currents are used to compute the real time dc-link capacitor currents. A compensation dc-link voltage control signal is computed from the knowledge of the dc-link power and the capacitor current. This control scheme should make it possible to match the input and output power demands of the dc-link and thus reduce the dc-link capacitor's size.

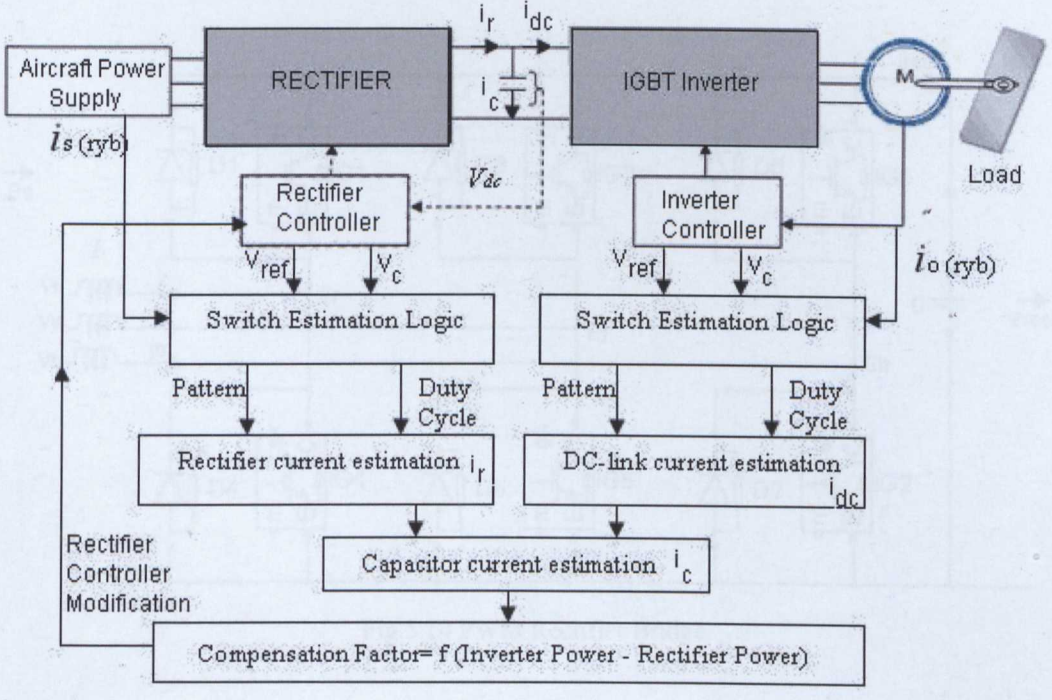


Fig.5.13 Control method to reduce dc-link capacitor

The switching state determination logic for the rectifier needs the input signals from the dc-link controller reference signal, the supply currents and the carrier wave. Similarly the inverter switch estimation logic needs inputs from the reference signal from the vector controller, the motor output currents and the carrier signal information. The method to estimate the switch commutation pattern and durations is explained here for a standard carrier wave PWM method, but the same method can easily be modified for a space vector modulation or other

modulation methods. Although the proposed method here looks similar to other power balancing schemes discussed in Chapter 2.3, unlike them the proposed method uses switch logic estimation for both converters and can responds to both load and supply changes.

Consider a PWM rectifier bridge and an instance of pulse generation by the PWM controller for the bridge as shown in Fig.5.14. Assuming the incoming currents to the rectifier from the supply are considered positive, it is very easy to establish here that for phase R the positive currents can only be circulated by either D1 or by IG4 and negative i_r can only be circulated by either IG1 or D4. Similarly for phase Y, the positive currents would go through IG6 or D3 and negative i_y via IG3 or D6. For phase B, the positive currents can only go through IG2 or D5 and negative i_b would follow either IG5 or D2.

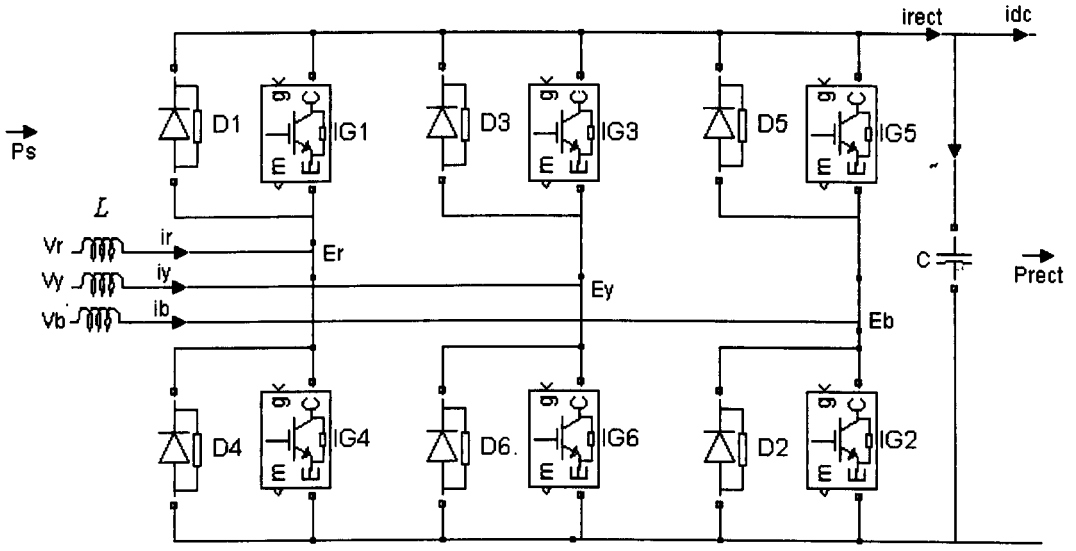


Fig.5.14 PWM Rectifier Bridge

For a known profile of reference voltage and carrier information, the duty cycle for the IGBTs or diodes can easily be calculated using equations (5.6) and (5.7). However the problem that must be solved to predict the switch pattern is to establish which switching devices are carrying the currents at the particular instant considered.

$$D = \frac{V_{ref}(t) - V_{c\min}}{V_{c\max} - V_{c\min}} \tag{5.6}$$

Here

$$D = \frac{T_{off}}{T_{off} + T_{on}} \tag{5.7}$$

The frequency of the three-phase reference signal and the size and frequency of the carrier wave are known, in this case 50Hz signal, $V_c = \pm 10V$, and 12 kHz respectively. It may be helpful in understanding the logic of predicting the pulse pattern for the rectifier bridge using an example: what is the exact status of all the rectifier switching devices at the instant of t=0.265 sec. At t=0.265 sec. the number of cycle completed by phase R's reference signal is:

$$\text{Number of cycle } V_{ref(R)} = \frac{0.265}{1/50} = 13.25$$

At t=0.265 sec. the number of cycles completed by the carrier wave signal is

$$\text{Number of cycle } V_c = \frac{0.265}{1/12000} = 3180$$

The 13.25 cycles of the phase R reference signal corresponds to 13 complete cycles and one fourth of a cycle. This gives information about the exact electrical angle (90° in this case). The reference signal expression from the equation for phase R (eq. 3.43) is:

$$V'_{R.r} = 7.1.Sin(\omega_e t - \frac{5.7 \times \pi}{180})$$

And the rectifier phase R supply current is:

$$i_r = 14.6.Sin(\omega_e t - \frac{5.7 \times \pi}{180})$$

The instantaneous values of the reference signal and the phase R current can be calculated for t=0.265 or $\omega_e t = 90^\circ$ as:-

$$V'_{R,r} = 7.1 \times Sin(\frac{\pi}{2} - \frac{5.7 \times \pi}{180}) = 7.0681 \text{ V}$$

and $$i_r = 14.6.Sin(\frac{\pi}{2} - \frac{5.7 \times \pi}{180}) = 14.5344 \text{ V}$$

This shows that at t=0.256 the current in phase R is positive so either IG4 or D1 could be carrying it. The duty cycle of the switches conducting at t=0.256 can be calculated by using eq. (5.6) and (5.7) as:

$$D = \frac{7.0681 - (-10)}{10 - (-10)} = 0.853$$

so $$D = \frac{T_{off}}{T_{off} + T_{on}} = \frac{T_{off}}{1/12000} = 0.853$$

so $$T_{off} = 7.12 \times 10^{-5} \text{ sec.}$$

and $$T_{on} = T - T_{off} = 1.213 \times 10^{-5} \text{ sec}$$

Thus at t=0.265 either IG4 or D1 is carrying a phase R current of value 14.5A. To ascertain the exact switch status the carrier wave status at t=0.265 needs to be known. At this time the carrier wave has done 3180 cycles and because at this instant $V'_{R,r}$ is higher than V_c that means there will be a gate signal to IG4 and it should be conducting.

The simulation of the pulse pattern estimation for phase R at t=0.256 is shown in Fig.5.15. The pulse pattern of the upper leg of the rectifier is opposite to that of the lower leg so that gives further information about two more switches in the rectifier bridge at that instant of switching. Similar calculations and logical analysis can be done for all three phases of the rectifier bridge for all of the switching instances to estimate the switching pattern.

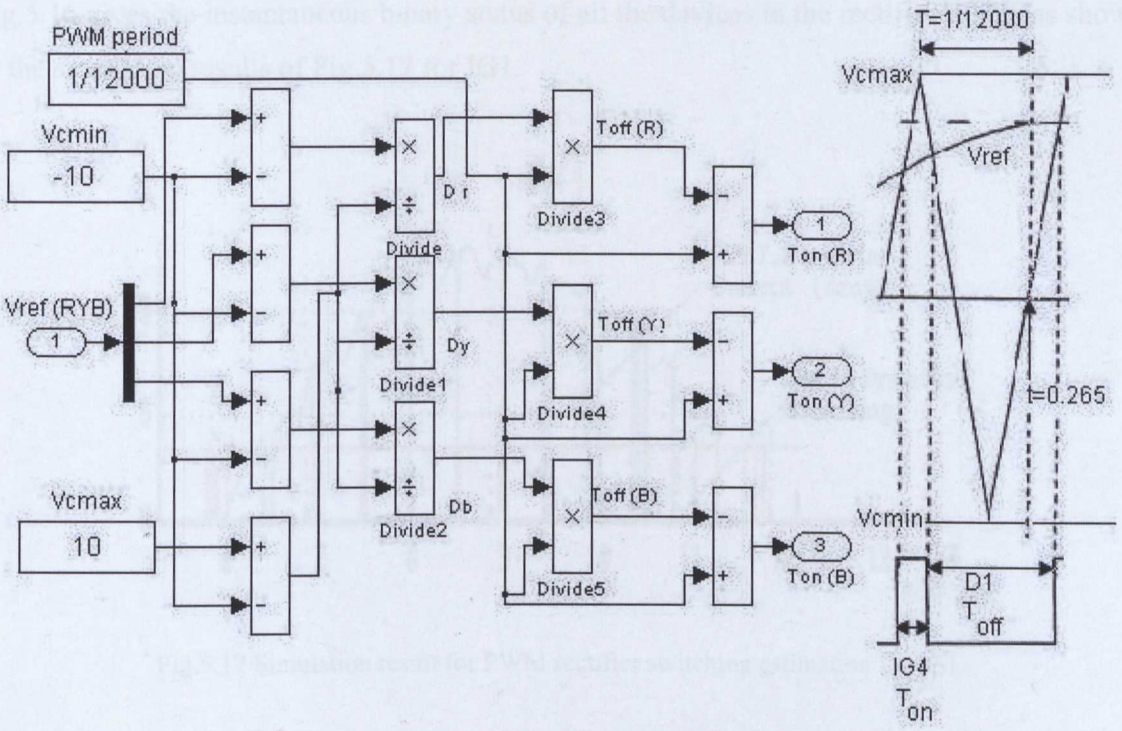


Fig.5.15 PWM rectifier switching time estimation

The analysis above requires logical selection between the devices which depends upon the direction of the current and the instantaneous values of the carrier and reference signals. This logical selection is simulated in Fig.5.16.

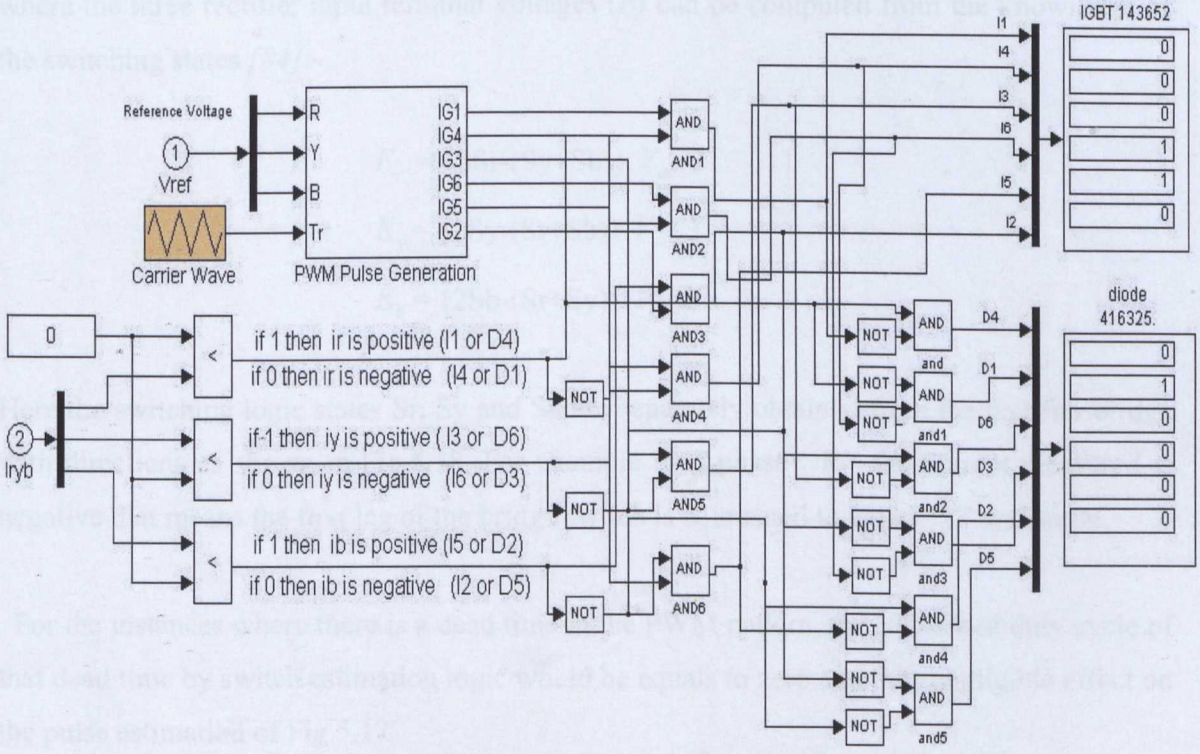


Fig.5.16 Simulation for Logical selection for PWM switch estimation

Fig.5.16 gives the instantaneous binary status of all the devices in the rectifier bridge as shown in the simulation results of Fig.5.17 for IG1.

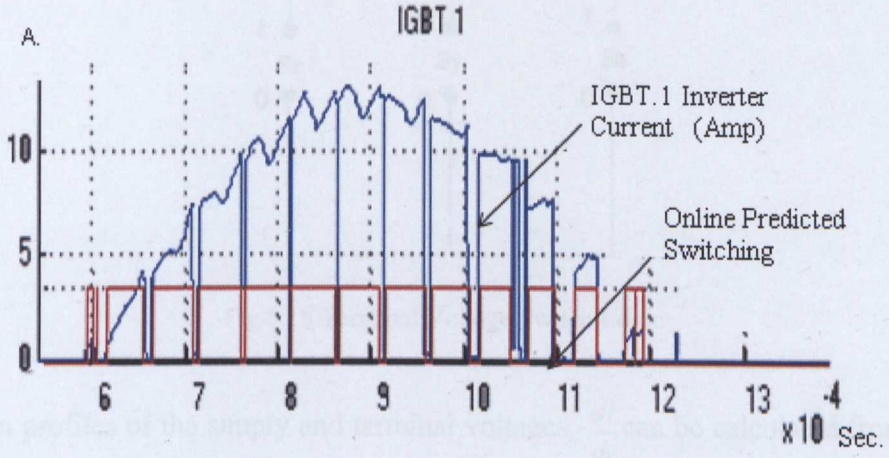


Fig.5.17 Simulation result for PWM rectifier switching estimation for IG1.

The various instantaneous voltages, currents and power can be predicted in real time from the switching information as:-

From Fig.5.14 it can be written that : - $$V = L\frac{di}{dt} + E \tag{5.8}$$

where the three rectifier input terminal voltages (*E*) can be computed from the knowledge of the switching states *[84]*:-

$$E_r = \{2Sr-(Sy+Sb)\}.V_{dc}/3$$

$$E_y = \{2Sy-(Sr+Sb)\}.V_{dc}/3$$

$$E_b = \{2Sb-(Sr+Sy)\}.V_{dc}/3$$

Here the switching logic states Sr, Sy and Sb are separately obtained from the rectifier bridge with directions as shown in Fig.5.18. For example if in phase "R" the current measured is negative that means the first leg of the bridge switch is connected to logic "1" and so on.

For the instances where there is a dead time in the PWM pattern, the calculated duty cycle of that dead time by switch estimation logic would be equals to zero and thus negligible effect on the pulse estimation of Fig.5.17.

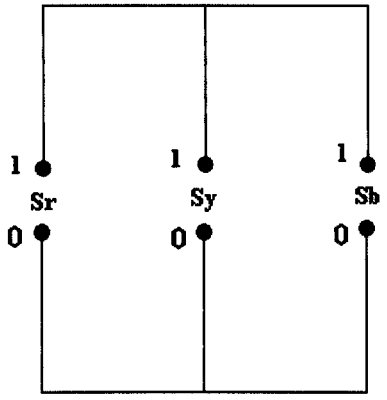


Fig.5.18 Terminal Voltage Switch Logic

With known profiles of the supply and terminal voltages, $\frac{di}{dt}$ can be calculated from eq. (5.8).

The rectifier output current i_{rect} which is a function of three phase supply current can be written as:-

$$i_{rect} = [\text{Sr}.\ i_r + \text{Sy}.\ i_y + \text{Sb}.\ i_b] \tag{5.9}$$

Repeating the above computation for the inverter the dc-link current as a function of motor currents can also be estimated as:-

$$i_{dc} = [\text{Sri}.\ i_{or} + \text{Syi}.\ i_{oy} + \text{Sbi}.\ i_{ob}] \tag{5.10}$$

Here the switching logic states Sri, Syi and Sbi are for the inverter bridge and i_o are the motor output currents.

The dc-link capacitor currents can be calculated as:-

$$i_c = i_{rect} - i_{dc} = C.\frac{dV_{dc}}{dt} \tag{5.11}$$

Fig.5.19 shows the switch estimation simulation closely predicts the rectifier currents (i_{rect}) and the dc-link output current (i_{dc}) in real time.

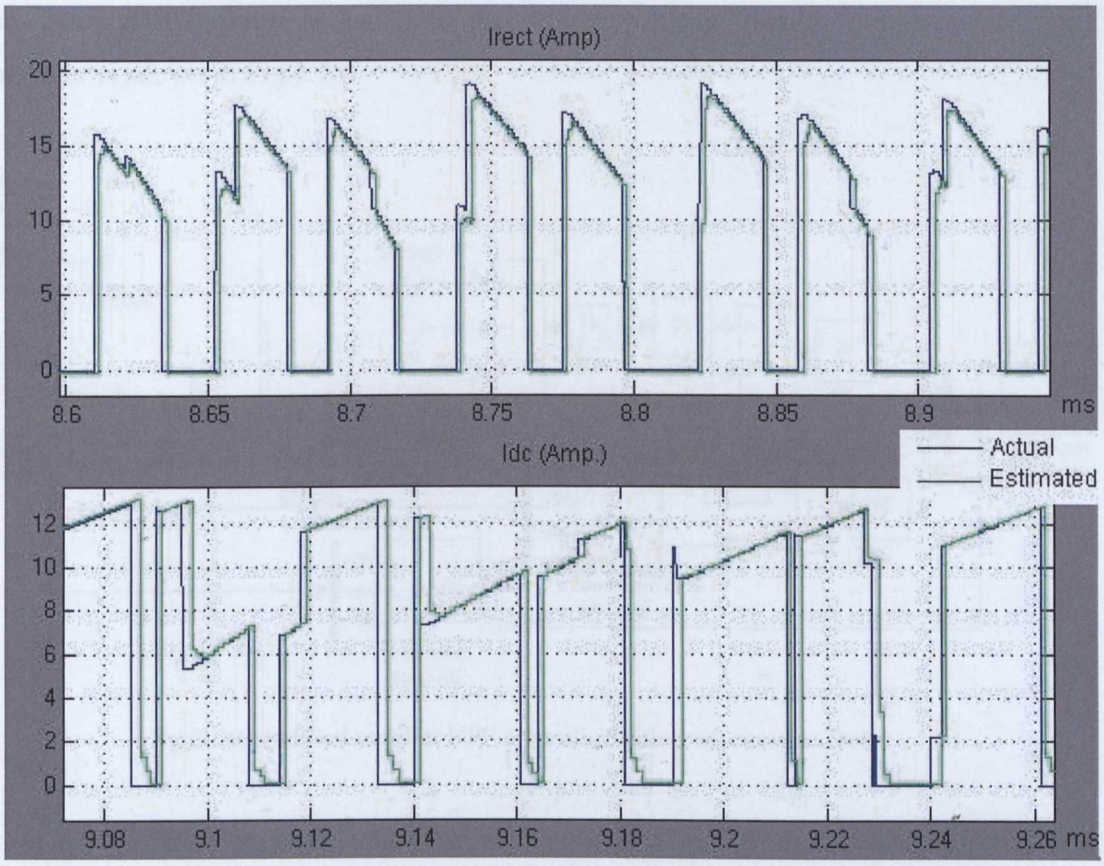


Fig.5.19 Current prediction simulation using switching states

Now that the dc-link currents have been estimated, the rectifier controller can be modified (Fig.5.13) with a compensation term that would be a direct function of the estimated capacitor current and the dc-link input and output power.

The power input to the rectifier is:

$$P_{in} = i_r.V_r + i_y.V_y + i_b.V_{rb} \tag{5.12}$$

So using eq. (5.12) and the estimated current of eq. (5.10) a compensation factor (C.F) can be calculated for the rectifier controller as:

$$\text{C.F}= \frac{P_{in} - P_{dc}}{i_{dc}} \tag{5.13}$$

This compensation term is added to the dc-link voltage control loop and the modified controller is shown in Fig.5.20.

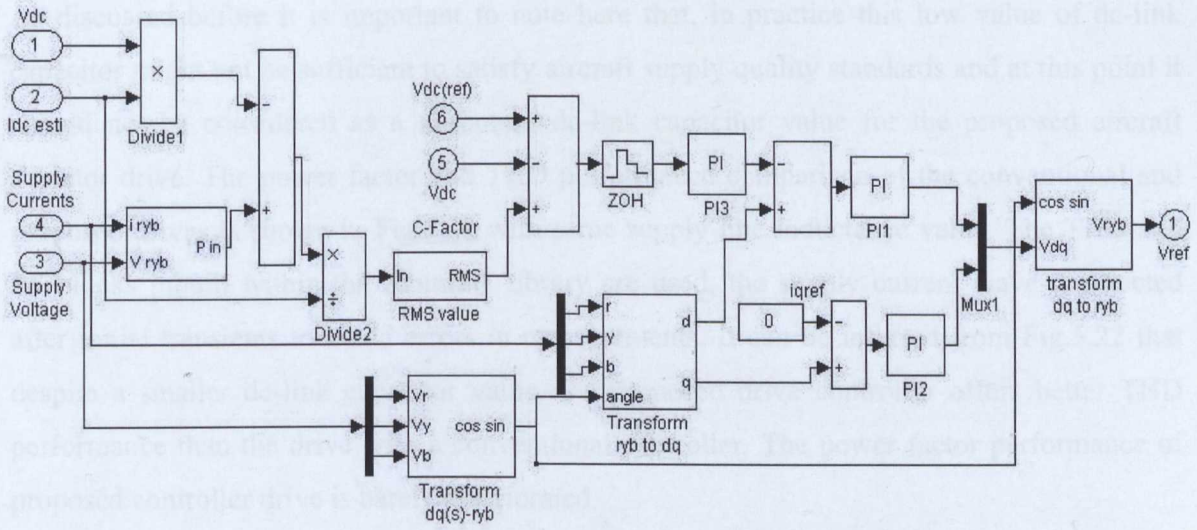


Fig.5.20 Modified rectifier UPF controller with compensation factor

Using the modified rectifier controller with only 20μFin the proposed three-phase PMSM drive, stability was successfully maintained while supplying full load at rated speed. The results shown in Fig.5.5 (for 71μF) can be compared with the results with the proposed modified rectified controller in Fig.5.21 with 20μF.

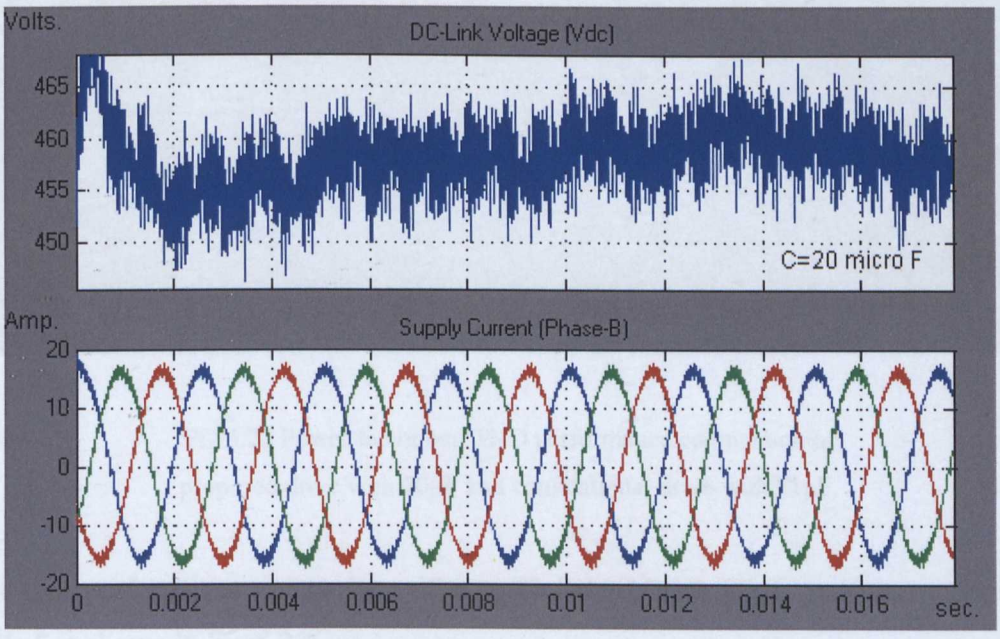


Fig.5.21 Vdc and supply currents simulation for modified rectifier controller with C=20μF

It can be inferred from Fig.5.21 that although the dc-link voltage ripple is much higher (approximately 15Vmax) the compensated rectifier controller helps the drive to retain stability at much lower dc-link capacitor values compared to a conventional rectifier controller drive. As discussed before it is important to note here that, in practice this low value of dc-link capacitor might not be sufficient to satisfy aircraft supply quality standards and at this point it should not be considered as a minimum dc-link capacitor value for the proposed aircraft actuator drive. The power factor and THD performance comparison of the conventional and proposed drives is shown in Fig.5.22 with same supply line inductance value. The THD and PF blocks inbuilt within the Simulink library are used; the supply current wave is selected after initial transients to avoid errors in measurements. It can be inferred from Fig.5.22 that despite a smaller dc-link capacitor value, the proposed drive controller offers better THD performance than the drive with a conventional controller. The power factor performance of proposed controller drive is barely deteriorated.

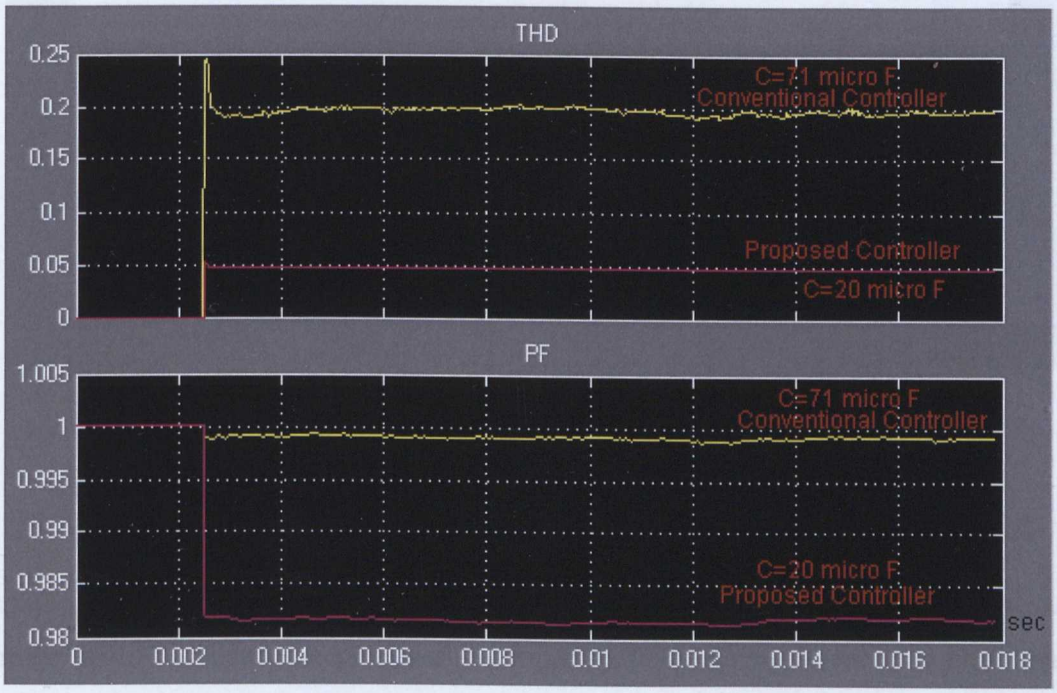


Fig.5.22 Power factor and THD performance comparison of proposed drive with 20μF and conventional drive with 71μF.

The dc-link performance comparison of proposed drive with 20μF and conventional drive with 71μF is shown in Fig.5.23.

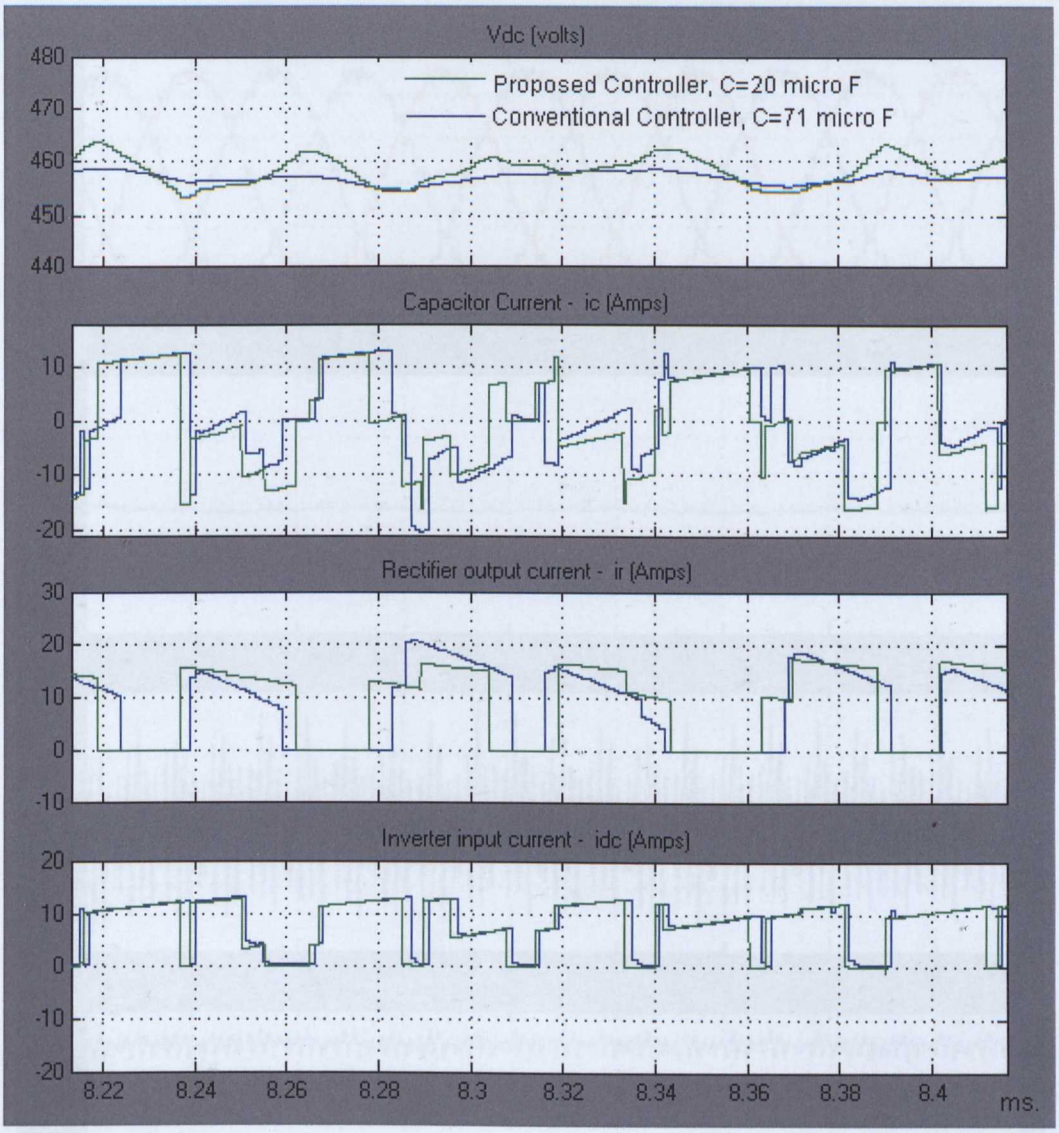


Fig.5.23 DC-Link current result comparison of proposed rectifier controller with C=20μF and conventional drive with 71μF.

Comparing the various current components and the dc-link voltage between a conventional controller with 71μF and the proposed controller with 20μF as shown it is clear that the performance is rather similar despite a very small capacitor in the dc-link for the proposed controller.

The drive output performance of the proposed drive with the 20μF dc-link capacitor is shown in Fig.5.24 and as may be seen the output performance is as required and rather the same as a conventional controller would produce with far more capacitance.

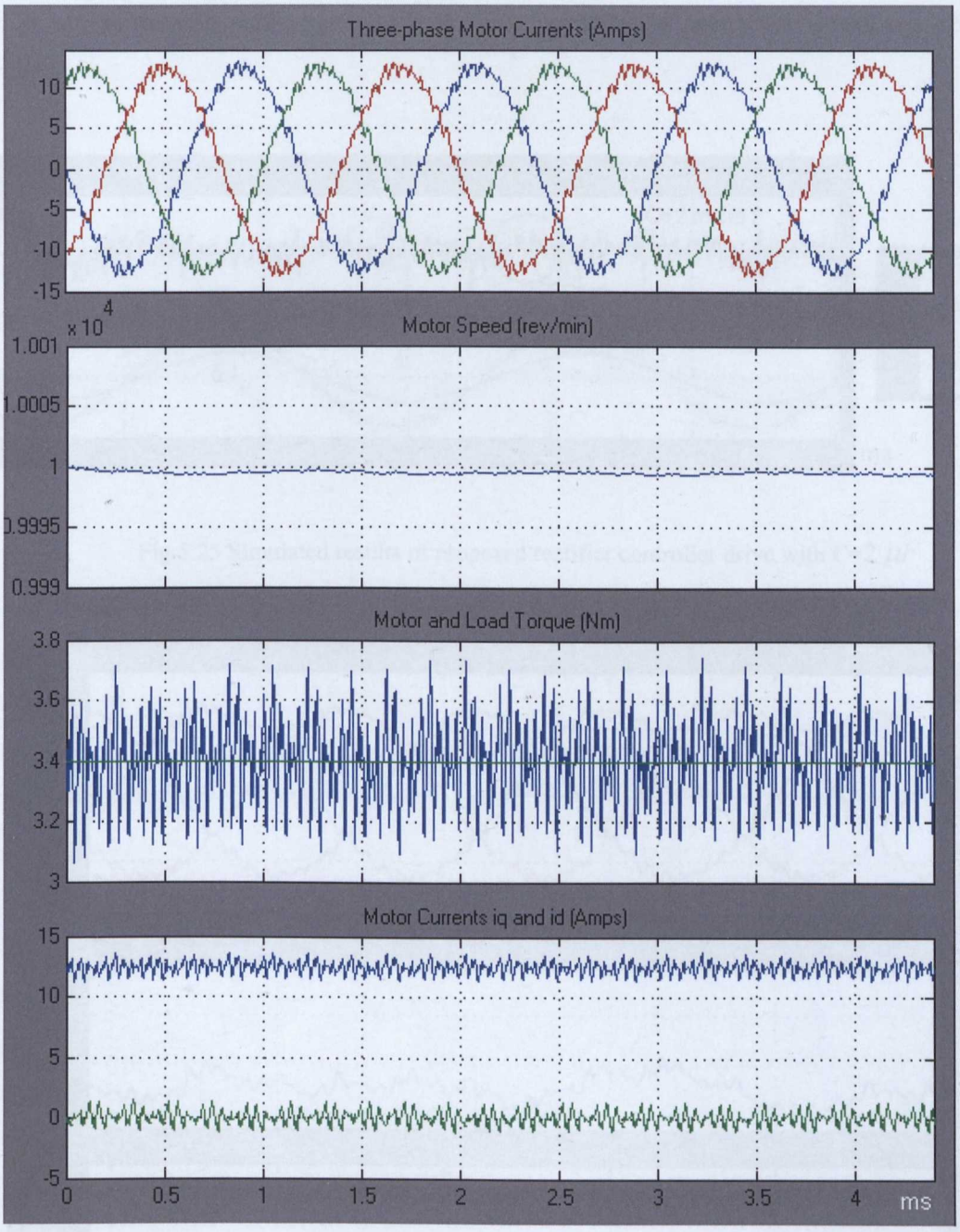


Fig.5.24 Drive output performance simulation results from modified drive with C=20μF

The analysis performed above to establish the minimum dc-link capacitor value before the drive becomes unstable for a conventional drive was done using eq. (5.4). In case of the proposed converter because the dc-link power is estimated in real time and compensated via the modified controller eq. (5.4) no longer applies and theoretically the drive should be able to remain stable even with a miniature dc-link capacitor. The results shown in Fig.5.25 and

Fig.5.26 are simulated with just 2 μF dc-link capacitance using the proposed rectifier controller.

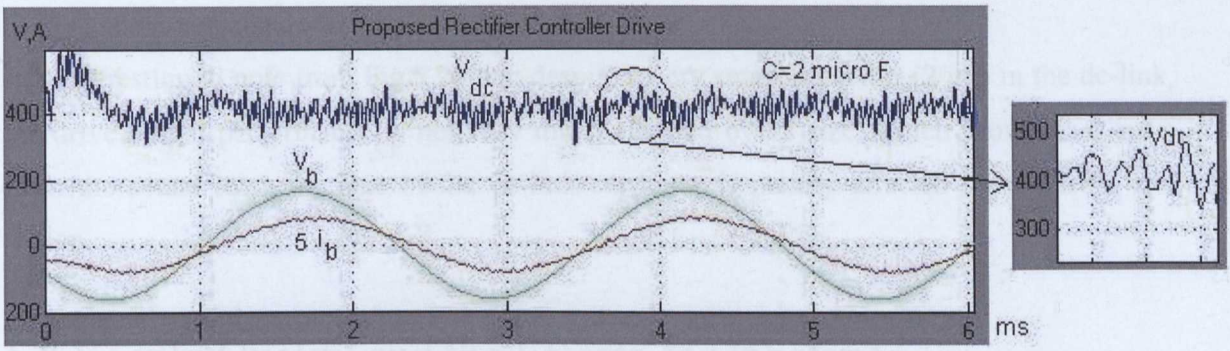


Fig.5.25 Simulated results of proposed rectifier controller drive with C=2 μF

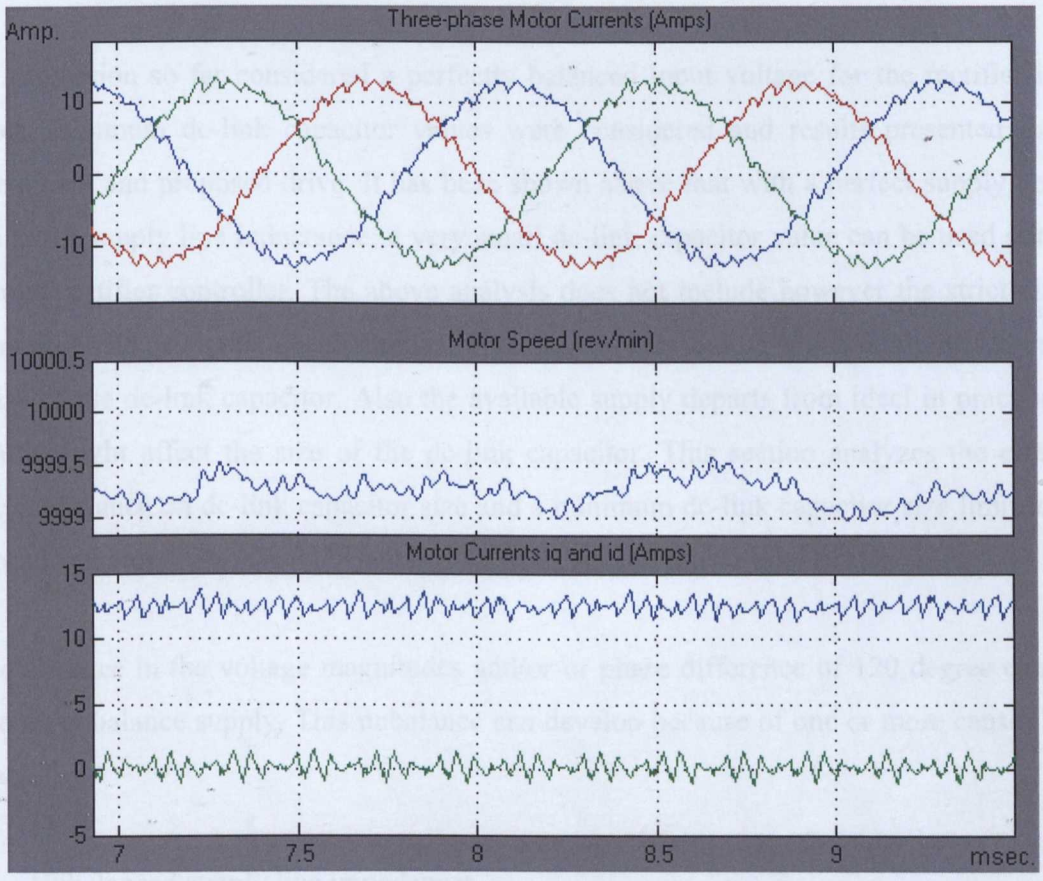


Fig.5.26 Drive output performance simulation results from modified drive with C=2μF

It can be inferred from the Fig.5.25 and 5.26 that the proposed dc-link compensator allows the drive to remain stable despite very low capacitance in the dc-link. It is however clear that whilst stability is achieved the cost of very low capacitance is very high dc-link voltage ripple (100V) and a reduced dc-link voltage.

It is interesting to note from Fig.5.26 that despite a very small capacitor (2 μF) in the dc-link, the drive output performance is not very much affected by its size, which proves that apart from the actual load, the size of the dc-link capacitor is mainly affected by the front end design.

5.5 Supply Quality and the Effects of Unbalance

5.5.1 Supply Quality Requirements

The discussion so far considered a perfectly balanced input voltage for the rectifier input. Various minimum dc-link capacitor values were considered and results presented for the conventional and proposed drive. It has been shown above that with a perfect supply voltage and a small supply line inductance; a very small dc-link capacitor value can be used with the proposed rectifier controller. The above analysis does not include however the strict aircraft current and voltage quality specifications (in respect of harmonics) which might heavily affect the size of the dc-link capacitor. Also the available supply departs from ideal in practice and this also might affect the size of the dc-link capacitor. This section analyzes the effect of supply unbalance on dc-link capacitor size and a minimum dc-link capacitor size limit for the proposed actuator drive is established that satisfies aircraft power quality standards.

Any difference in the voltage magnitudes and/or or phase difference of 120 degree can give rise to an unbalance supply. This unbalance can develop because of one or more causes listed below:-

- Unbalanced supply line impedances.
- Unequal distribution of single-phase loads.
- Unbalanced three-phase loads.

The effect of unbalance is very obvious in the case of three-phase diode rectifier front end drives, where the line current waveform can change its pulse pattern from double pulse to single pulse per half cycle. This leads to various problem associated with triple harmonics in diode rectifiers. In any system an unbalanced supply can result in tripping of the drive system due to excessive AC line currents in some phases and sudden voltage stress on converter devices and the dc-link. A small unbalance in the phase voltages has potential to cause a disproportionately larger unbalance in the phase currents *[91] [95].*

The voltage unbalance is defined by the National Electrical Manufacturers Association (NEMA) as:-

$$\%\text{Unbalance} = \frac{\text{Maximum Deviation from Average}}{\text{Average of Three Phase - to - Phase Voltages}} \times 100.$$

To compensate the effect of unbalance supply in specific applications, a common trend in the power industry is to use fully switched front end rectifiers. As discussed from Chapter 3 onwards, the use of a PWM rectifier front end also offers various other advantages including smaller dc-link components. In the presence of an unbalanced supply the advantages associated with a PWM rectifier cannot be fully exploited. Moreover the use of PWM rectifiers with an unbalanced supply causes increased current distortion, generation of 100 Hz ripple in the dc-link and an increase in the reactive power*[96] [94].* It has also been shown in *[94]-[95]* that the unbalanced input supply results in the appearance of even harmonics in the dc input and odd harmonics in the ac input currents. These effects are very much evident in the experimental results presented in Chapter 4.

According to the aircraft power standard MIL-STD-704F *[97]* and *[96]* the maximum allowable voltage unbalance for the 400Hz AC supply cannot exceed 3% R.M.S. The supply current harmonic current has to be under 5% and the DC voltage ripple cannot exceed 6V (for a 270V system). The simulation results of the FFT analysis of the supply current presented in Fig.5.22 were made assuming Ls=0.44mH and thus a 0.1 p.u. voltage drop in it.

From previous analysis the performance of the conventional and proposed drives can be compared against MIL-STD-704F *[97]* standards as:-

Table-3

Minimum MIL-STD-704F Requirement	Conventional Drive with C=71 μF offers-	Proposed Drive with C=20 μF offers-
5% supply current THD	18% THD	4.58%THD
6V dc-link voltage ripple	5.5Vmax	15Vmax

So it is clear that both (conventional and proposed drive) can operated with given parameters in the Table-3 without considering the limitations of MIL-STD-704F *[97]*. In terms of the supply current THD performance, a conventional drive would require bigger supply line inductance filters. On the other hand with C=20 μF the proposed controller can live with a 0.44mH supply inductance but would require a bigger dc-link capacitance to achieve the 6V dc-link voltage ripple limit.

To satisfy MIL-STD-704F Requirements *[97]*, it can be verified from simulation that the conventional drive would now require a minimum line phase inductance of 1.85mH to achieve less than 5% THD in the supply phase currents. On the other hand increasing Ls would cause an increase in $L_s \frac{di}{dt}$ and as per eq.(5.4) would require adjusting the values of the dc-link capacitor and the dc-link controller gain K_p. The minimum value of K_p to achieve 460V dc-link voltage is now reduced to K_p=1.5 and the drive requires an even higher dc-link capacitance (170 μF) to keep the drive in stable operation. . The FFT analysis of phase-B line current for Ls=1.85mH for the conventional drive controller is shown in Fig.5.27.

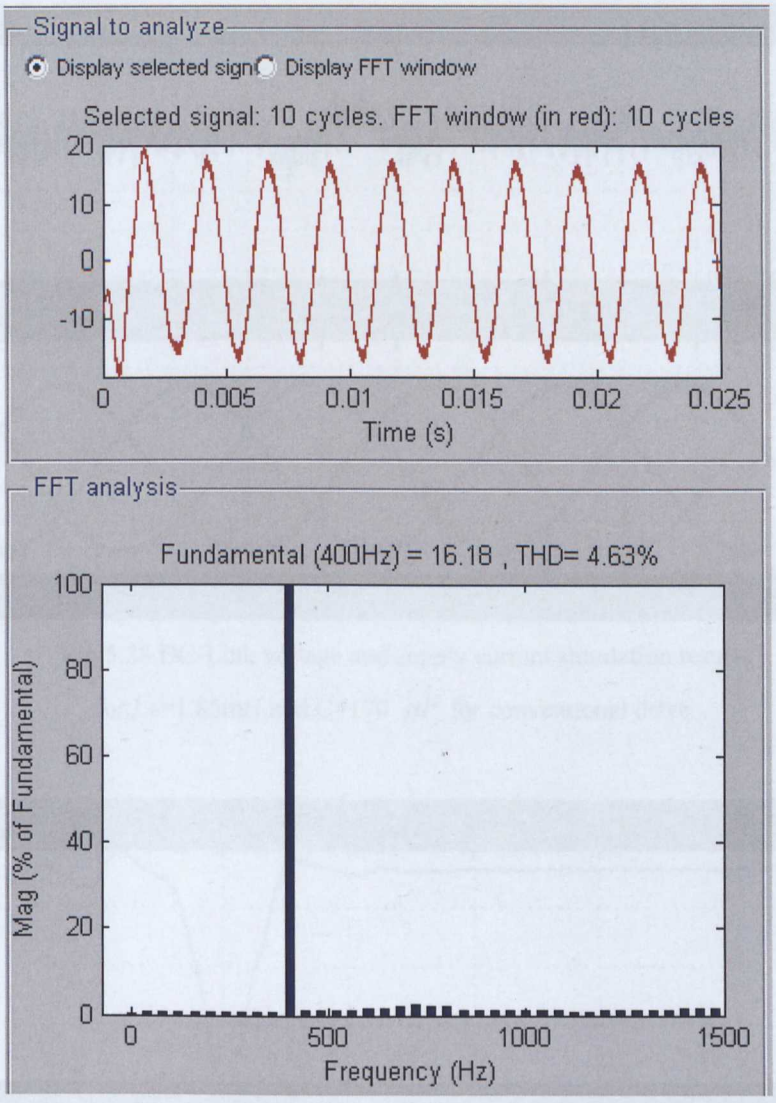


Fig.5.27 FFT analysis of phase-B currents with Ls=1.85mH and C=170 μF for conventional drive

It is clear form Fig.5.28 that with Ls=1.85mH and C=170 μF , the dc-link ripple is below 6V and now satisfies the MIL-STD-704F standards *[97]*. Below C=170 μF the drive would not be able to satisfy MIL-STD-704F standards *[97]* and THD would increase beyond 5%. For C=140 μF the conventional controller drive would become completely unstable as shown in Fig.5.29.

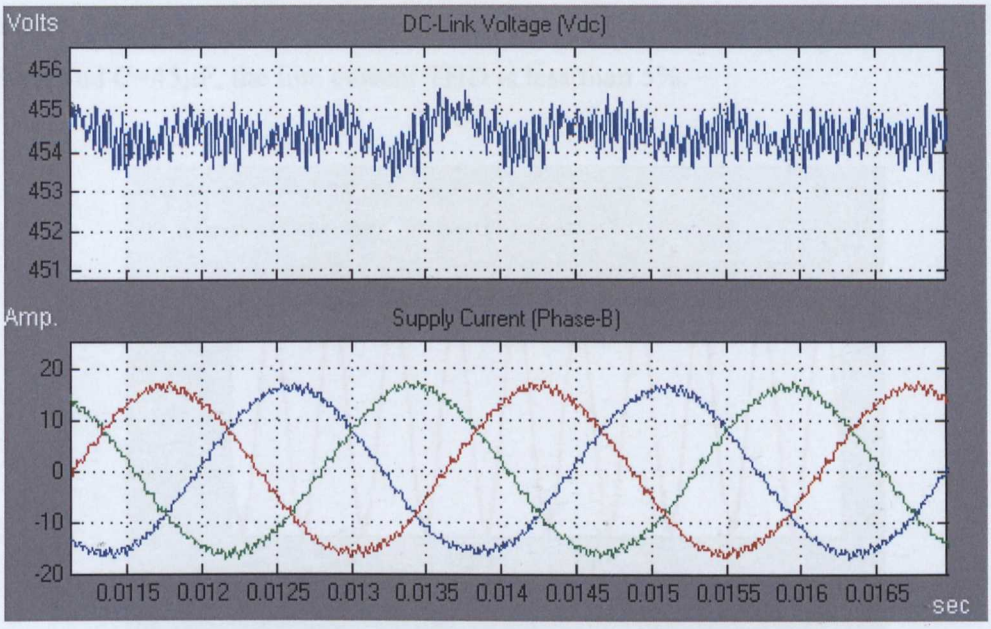


Fig.5.28 DC-Link voltage and supply current simulation results for Ls=1.85mH and C=170 μF for conventional drive

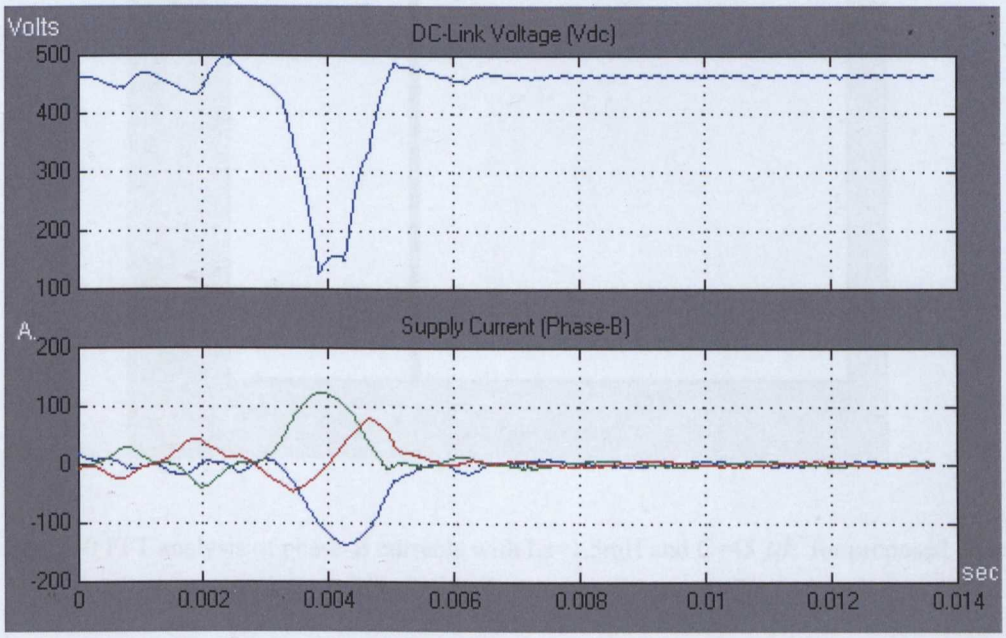


Fig.5.29 Unstable operation of conventional controller drive for Ls=1.85mH and C=140 μF

On the other hand because the proposed controller is no longer exactly controlled by eq.(5.4) to provide dc-link compensation, it requires 1.5mH supply phase inductance and only a slightly bigger dc-link capacitor to satisfy the 6V dc-link ripple specification of MIL-STD-704F standards *[97]*. From simulation it can be established that for the proposed converter the minimum dc-link capacitor required to achieve $\Delta V_{dc} = 6V$ is 45 μF .

The phase-B supply current FFT analysis confirms that for the proposed converter drive with Ls=1.5mH and C=45μF, the line current THD is less than 5%.

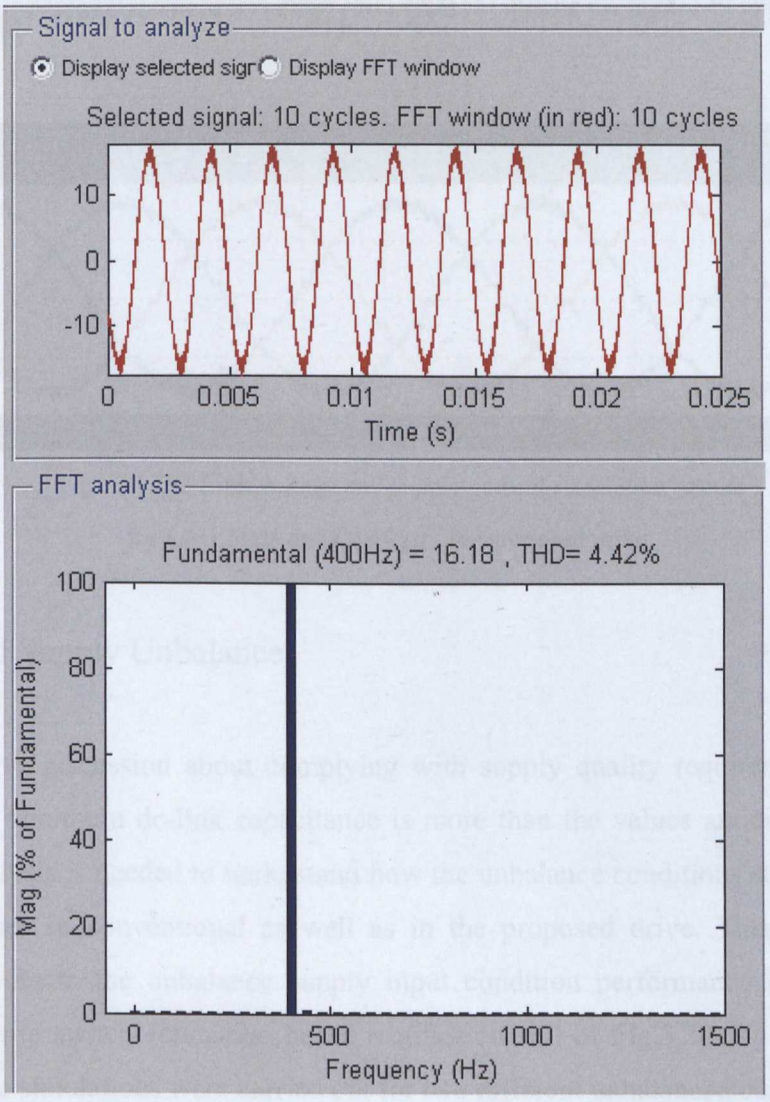


Fig.5.30 FFT analysis of phase-B currents with Ls=1.5mH and C=45 μF for proposed drive

The simulation results of Fig.5.31 for proposed drive controller confirms that for C=45 μF the dc-link voltage ripple is below 6V and now complies with MIL-STD-704F standards *[97]*.

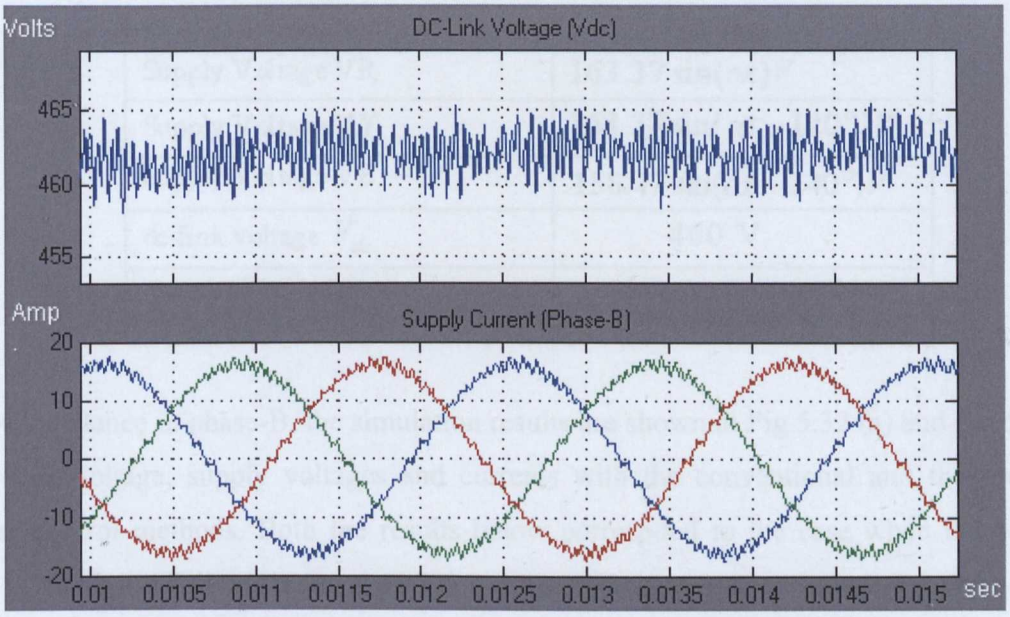


Fig.5.31 DC-Link voltage and supply current simulation results

for Ls=1.5mH and C=45 μF for proposed drive

5.5.2 Effect of Supply Unbalance

From the above discussion about complying with supply quality requirements, it is now known that the minimum dc-link capacitance is more than the values anticipated in section 5.2. Similar analysis is needed to understand how the unbalance conditions stretches the filter component values in conventional as well as in the proposed drive. Therefore it is very important to evaluate the unbalance supply input condition performance of the proposed actuator drive with switch estimation based rectifier control of Fig.5.20. To verify the drive performance, the simulations were carried out for two different unbalanced conditions.

1. Unbalance in one input phase voltage condition.
2. Single line-ground fault condition.

1. Unbalance in one input phase voltage condition: This condition is deliberately chosen as this is the most common type of unbalance found in the supply system. As previously mentioned the aircraft standard MIL-STD-704F *[97]* and *[96]* requires the voltage unbalance to be less than 3% in one of the motor phases. The system parameters selected for this supply unbalance in phase-B is shown below.

Parameter	Value
Supply Voltage VR	$163.37\sin(\omega t)V$
Supply Voltage VY	$163.37\sin(\omega t-120^{\circ})V$
Supply Voltage VB	$158.47\sin(\omega t-240^{\circ})V$
dc-link voltage V_{dc}	460 V
Supply phase inductnace	1.85mH (conventional drive) 0.44mH (proposed drive)

For 3% unbalance in phase-B, the simulation results are shown in Fig.5.32 (a) and Fig.5.32(b) for dc-link voltage, supply voltages and currents with the conventional and the proposed rectifier control methods. Both the results below correspond to the case when the actuator motor is supplying 3.4Nm torque at 10000 rpm (maximum torque and power) to the actuator load while maintaining vector control at the output and UPF control at the input side of the dc-link. It is noted that for such low value of supply unbalance (3%) there is insignificant effect on the drive performance and the supply current's quality. A very slight reduction in dc-link voltage is observed for both methods as expected as a result of the 3% voltage unbalance. Or to put it more plainly 3% imbalance does not form any form of limit for either control method in this case.

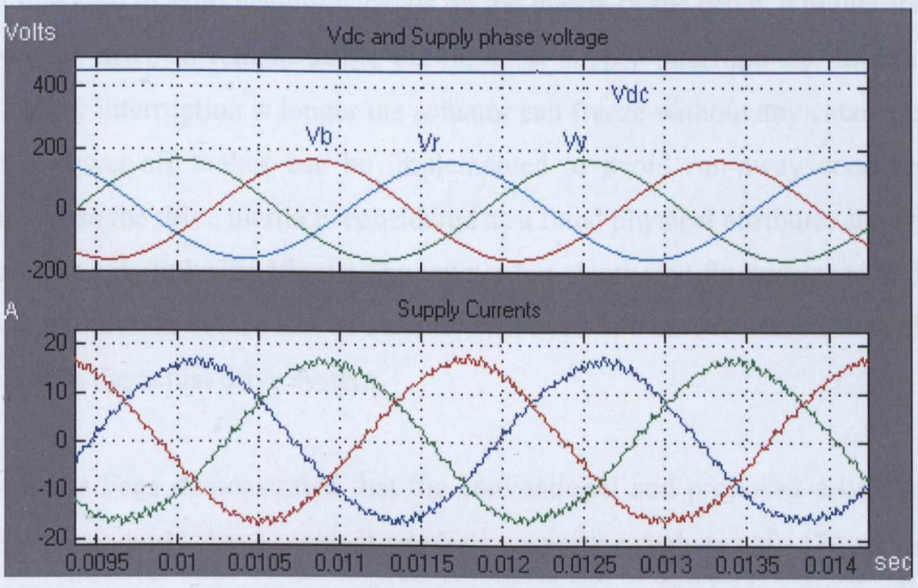


Fig.5.32(a) Simulated results of conventional rectifier controller drive with 3 % of one phase balance for Ls=1.85mH, C=170 μF

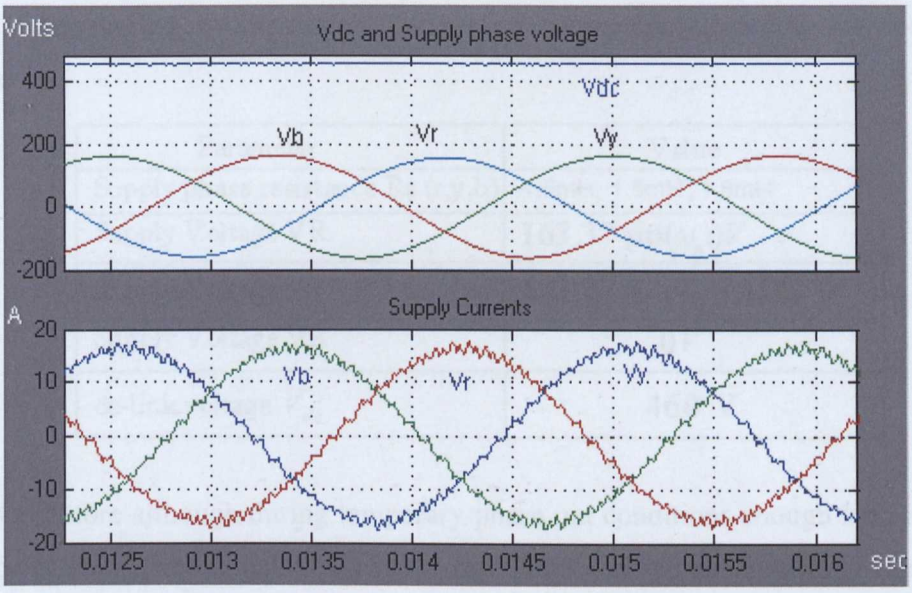


Fig.5.32(b) Simulated results of proposed rectifier controller drive with 3 % of one phase balance for Ls=1.5mH, C=45 μF

2. Single line-to-ground fault condition: This condition is not as frequent as compared to the previous case but simulation of such a condition can give some clear indication of the effects of the size of dc-link capacitor on extremes of voltage unbalance. The survival of drive stability in this kind of fault heavily depends on the inertia of the drive; a higher inertia of the drive allows the drive to remain stable during short supply interruptions. In extreme cases where the supply interruption is longer the actuator can freeze without any catastrophic effects (because the power-off brakes can be implemented to avoid run-away conditions for the flaps). In this case the drive inertia is considered as a fixed physical attribute, and so it will not be considered as a dc-link size affecting parameter but clearly the findings as to such issues as maximum fault duration before loss of stability will need to be reconsidered in the light of the inertia present in the actual drive system.

Previously it has been demonstrated that the conventional and proposed drives that comply with aircraft standards have critical dc-link capacitor values of 170 μF and 45 μF respectively before they become unstable. In this section the proposed drive is subjected to a phase-B line to ground fault outage and unequal phase. The phase-B line inductance is set to 20% higher than the phase-R and phase-Y values. The proposed drive's fault ride through

capability is then "tested" by simulation. The system parameters selected for this condition are shown below.

Parameter	Value
Supply phase resistance Rs (r,y,b)	1.5mH, 1.5mH , 1.8mH
Supply Voltage VR	$163.37\sin(\omega_e t)V$
Supply Voltage VY	$163.37\sin(\omega_e t-120^\circ)V$
Supply Voltage VB	$0V$
dc-link voltage V_{dc}	460 V

As discussed before although during temporary phase out conditions enough load inertia may keep the drive stable, the simulation carried out here is to see for how long the drive can survive with an unlimited single line-ground fault. The simulation for the proposed drive is presented in Fig.5.33 with C= 45 μF where the phase outage is introduced at t=3ms and kept until the drive loses control.

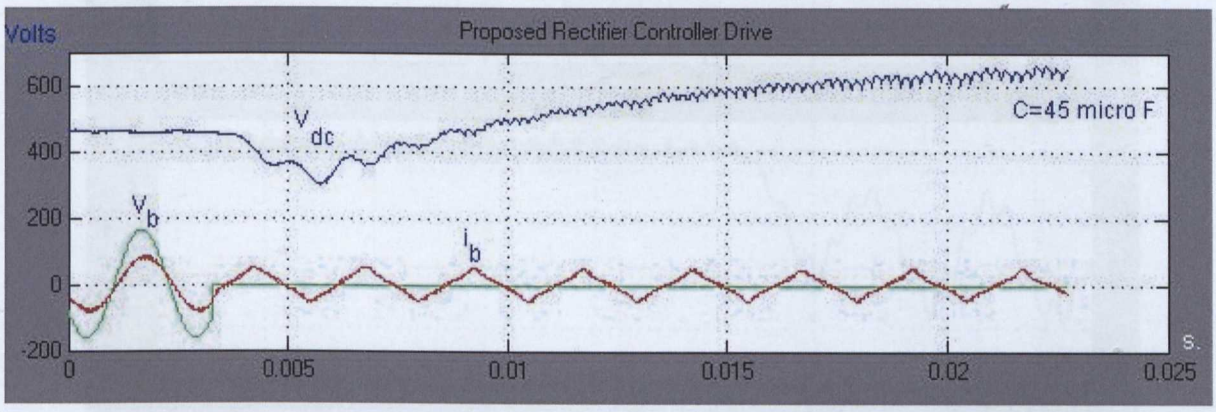


Fig.5.33 Simulated results of proposed drive dc-link voltage and supply voltage, current for unlimited single line-ground fault in phase-B, C=45 μF ,phase-b Ls=1.8mH.

It can be seen from the simulation results of drive output of Fig.5.34 that after the short circuit of phase B at t=3ms, V_b is of course zero, i_b becomes an induced current and the dc-link voltage starts to vary. The drive loses control after 2ms at around t=5ms.

The motor output continues almost normally until after the drives goes unstable at around 5msec as can be seen from Fig. 5.34. The supply input power P_{in} and dc-link power P_{dc} variation for this unlimited single line-ground fault condition are shown in Fig.5.35.

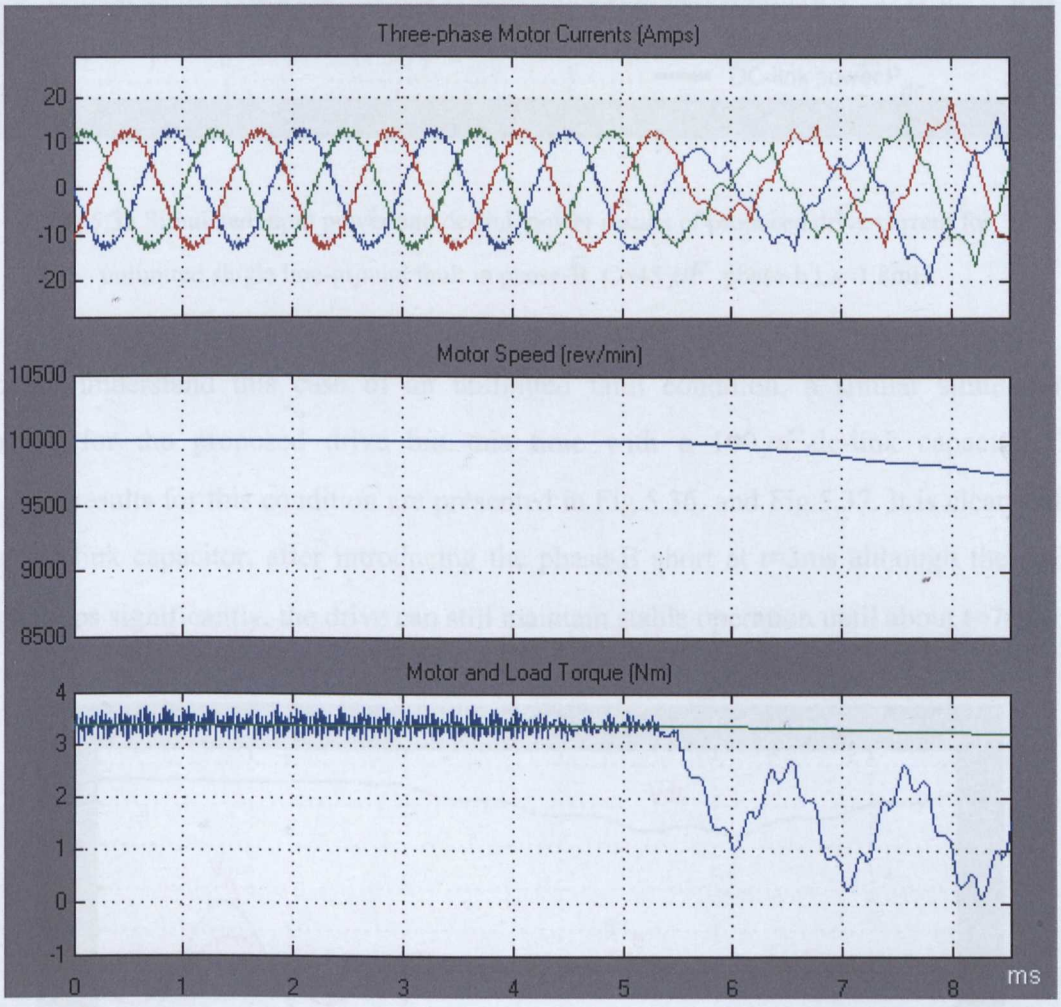


Fig.5.34 Simulated motor output results of proposed drive for unlimited single line-ground fault in phase-B, C=45 μF ,phase-b Ls=1.8mH.

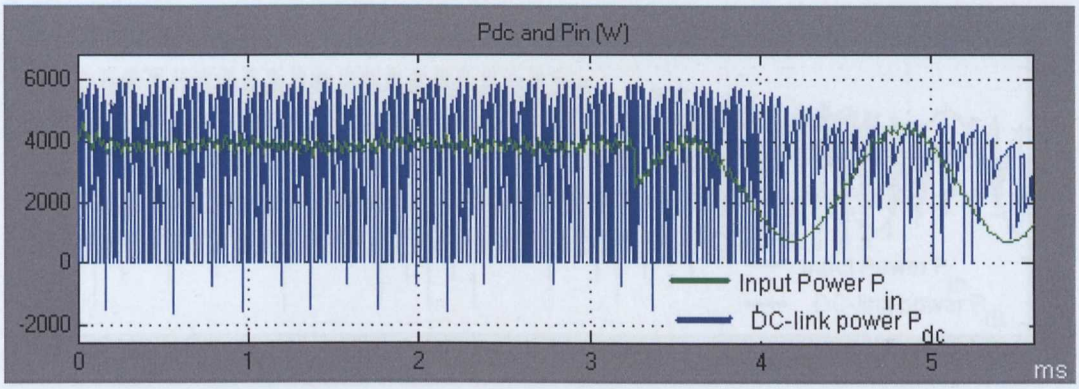


Fig.5.35 Simulated input power and dc-link power results of proposed drive current for unlimited single line-ground fault in phase-B, C=45 μF ,phase-b Ls=1.8mH.

To better understand this case of an unlimited fault condition, a similar simulation is performed for the proposed drive but this time with a 100 μF dc-link capacitor. The simulation results for this condition are presented in Fig.5.36. and Fig.5.37. It is clear that for 100 μF dc-link capacitor, after introducing the phase-B short at t=3ms although the dc-link voltage drops significantly, the drive can still maintain stable operation until about t=7ms.

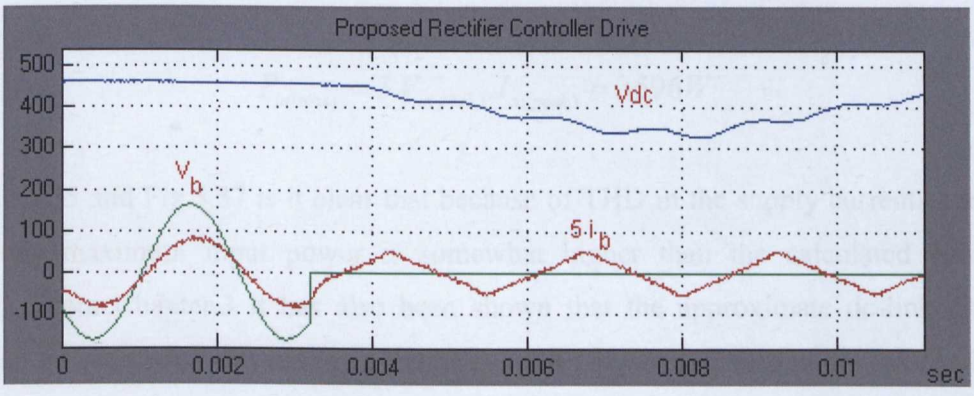


Fig.5.36 Simulated results of proposed drive dc-link voltage, supply voltage and current For unlimited single line-ground fault in phase-B, C=100 μF ,phase-b Ls=1.8mH.

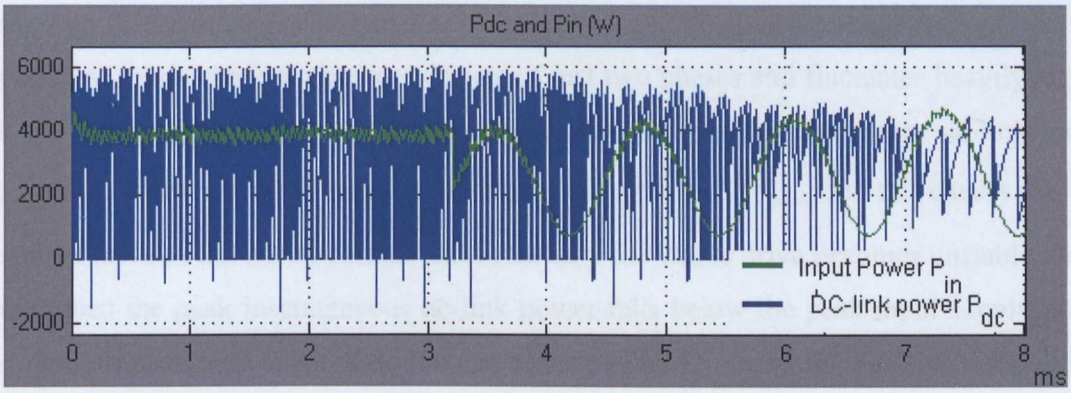


Fig.5.37 Simulated input power and dc-link power results of proposed drive current for unlimited single line-ground fault in phase-B, C=100 μF ,phase-b Ls=1.8mH.

From the above discussion it is now clear that a higher value of dc-link capacitor helps improve the drive's fault ride through capability. Now to further test the proposed drive controller the fault on phase-B is cleared at t=7ms (for the 100 μF case) and the drive should be able to regain full control without significantly affecting the output performance.

It has already been established in Chapter.3 equation (3.39) that the maximum input supply power at any instant to rectifier in the unity power factor condition (ignoring device losses) is given as:-

$$P_{in(\max)} = 3.V_{s(peak)}.I_{s(peak)} = 3596W$$

From Fig.5.35 and Fig.5.37 is it clear that because of THD in the supply currents and device losses, this maximum input power is somewhat higher than the calculated value from eq.(3.39). From Chapter.3 it has also been shown that the approximate dc-link maximum power can be calculated considering MIL-STD-704F *[97]* with specified dc-link ripple of 6V as:-

$$P_{dc(\max)} = .V_{dc(\max)}.I_{dc(\max)} = 463 \times 12.42 = 5750W$$

Again considering the THD in the load currents, the load dc-link maximum power is somewhat higher than the calculated value above.

Now it is worth noting that from Fig.5.35 and Fig.5.37 that, in case of a low load inertia and the absence of power-off brakes, the time duration for which the drive can survive the single line-ground fault depends on the time that the maximum instantaneous dc-link power remains

higher than the input supply power. For example in Fig.5.37 after the single line-ground fault is applied at t=3ms the input power consists of just two phases and fluctuates heavily and the peak dc-link power starts to decrease gradually. At t=7ms the peak dc-link power $P_{dc(peak)}$ falls below the instantaneous maximum input power $P_{in(peak)}$ and this causes the load side of the drive to fall out of control and eventually the whole drive becomes unstable. So the instant when the peak instantaneous dc-link power falls below the peak input supply power, determine the minimum value of dc-link capacitor required to maintain the drive's stability for that fault duration. So the maximum allowed duration of fault plays an important part in deciding the dc-link capacitor size.

Now having established that the drive has a threshold until which it can survive a single line-ground fault a check can be made to see if the drive can regain control if the supply is reinstated before this threshold. The results presented in Fig.5.38-Fig.40 are for 100 μF where phase-B is reinstated just before t=7ms.

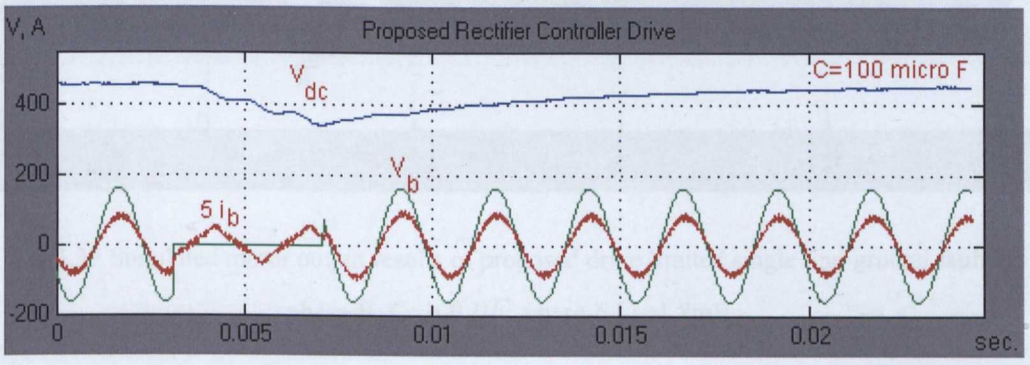


Fig.5.38 Simulated results of proposed drive dc-link voltage, supply voltage and line current with for limited single line-ground fault in phase-B, C=100 μF ,phase-b Ls=1.8mH.

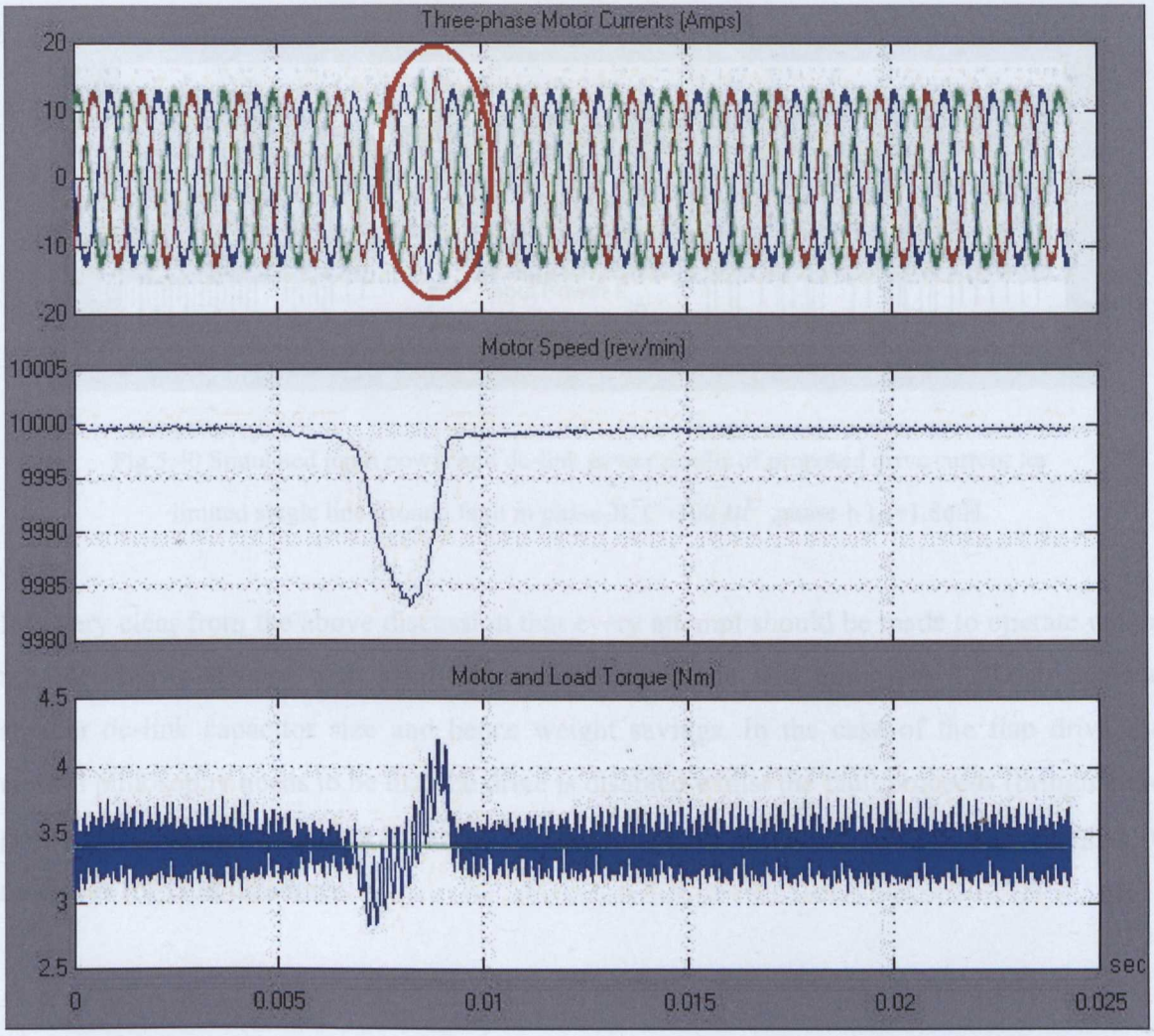


Fig.5.39 Simulated motor output results of proposed drive limited single line-ground fault in phase-B, C=100 μF ,phase-b Ls=1.8mH.

It is clear from Fig.5.38 and Fig.5.39 that after the fault is cleared at t=7ms, the speed drops a little but after t=7ms the drive just manages to regain vector control on the load side and UPF control on the rectifier side.

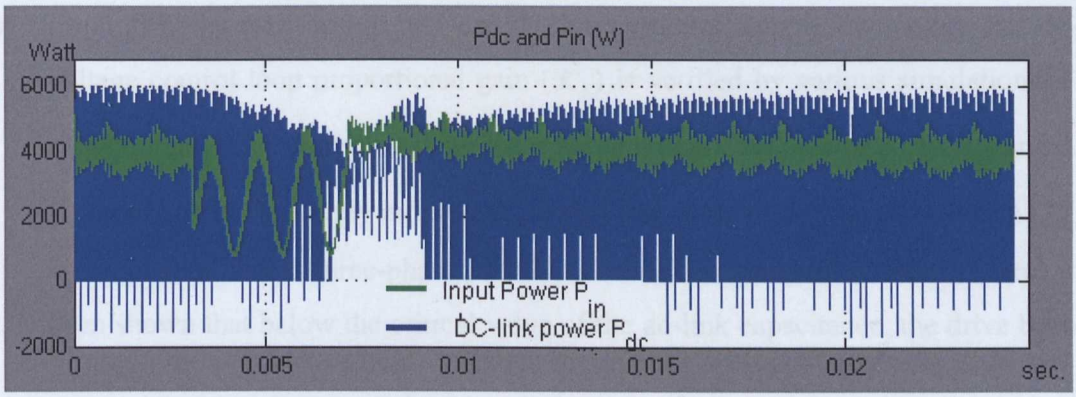


Fig.5.40 Simulated input power and dc-link power results of proposed drive current for limited single line-ground fault in phase-B, C=100 μF ,phase-b Ls=1.8mH.

It is very clear from the above discussion that every attempt should be made to operate with a reliable supply system with smallest possible unbalance and minimum THD to achieve smaller dc-link capacitor size and hence weight savings. In the case of the flap drive the control philosophy needs to be that the drive is disabled whilst the fault proceeds (bringing the power off brakes into action if needed) which will allow the dc-link to stay charged in readiness for fault clearance.

5.6. Conclusions

This chapter provides a detailed understanding of dc-link capacitor size dependencies on the drive parameters. A new switch estimation based rectifier controller is proposed with an aim to reduce the dc-link capacitor value in a dc-link drive to allow a more reliable capacitor technology to be used. The contributions of this chapter are summarized below:-

1) The chapter provides a brief introduction of the need to study various parameters which might affect the size of the dc-link capacitor.
2) To understand the effect of a reduction of the dc-link capacitor, simulation results for a high value of dc-link capacitor drive are presented. It is established that reducing the dc-link capacitor causes higher dc-link voltage ripple and forces the rectifier towards overmodulation and thus increases the VA rating of the converter. It is also establishes that significant reduction in dc-link capacitor causes only a small affect on supply current harmonics.

3) From *[98]* the relationship between dc-link capacitor, supply inductance and dc-link voltage control loop proportional gain (K_p) is verified by various simulations. For a conventional drive controller, with the minimum possible value of K_p(=2.1) and 0.1pu voltage drop in the supply inductance, the critical value of dc-link capacitance (71 μF) is established. For a three-phase PMSM drive with a standard rectifier control it has been shown that below the critical value of the dc-link capacitance, the drive becomes unstable.

4) Reducing the supply line side inductances might allow for a lower dc-link capacitance but is limited by an increase in the size of the fault currents and maximum THD limits. For this reason this is not considered as a suitable method for dc-link capacitor reduction.

5) The effect of a dc-link filter choke has been presented by simulation results but is not considered an option for capacitor reduction because of the insignificant effect on the voltage distortion.

6) A rectifier controller modification has been suggested with an aim to reduce the size of the dc-link capacitor with a minimal effect on the drive performance. This requires a switch estimation mechanism and consequent calculation of a compensation factor to modify the dc-link control loop.

7) A detailed description of the switching estimation method has been given using an example and simulation results have been presented showing how accurately this method estimates the switching pattern and duty cycles of the converters switches.

8) Its has been established in this chapter that with the modified rectifier control the proposed drive can successfully run (at least in simulation with ideal supply voltages) with much lower dc-link capacitor and yet can offer better THD for the supply currents. Because the dc-link power is compensated in real time, the proposed drive has been simulated to give a stable performance with just 2 μF in the dc-link.

9) The aircraft supply quality standards *[97]* imply a limit on minimum dc-link capacitor size as well on supply phase inductance. It has been established that to comply with *[97]* a conventional drive requires a supply inductance of 1.85mH and a dc-link capacitor of 170 μF. On the other hand the proposed controller drive would require supply inductance of 1.5mH and a dc-link capacitor of 45 μF.

10) Performance of the proposed drive under supply unbalanced conditions was simulated and analyzed. It has been established that a phase voltage unbalance of 3% (as per the specification) does not significantly affect the proposed drive's performance. It has also been established that a higher dc-link capacitor helps improve the drive's fault ride through capability. From dc-link and input power waveforms it has been established that when the peak dc-link power falls below the instantaneous maximum input power, the drive becomes unstable. But if the supply phase voltage is reinstated before the dc-link power falls below the input power, the proposed drive regains complete control. This simulation shows that the maximum allowed duration of a fault plays an important role in deciding the dc-link capacitor size.

To improve the system reliability enough to achieve flap actuator drive dispatch specifications, the proposed drive with the small value dc-link capacitor can be realized by a high reliability film capacitor in a conventional three-phase PMSM drive configuration.

CHAPTER 6

FINAL CONCLUSIONS

6.1 Introduction

This thesis is concerned with control a method that allow a reduction in the size of the capacitors in dc-link three-phase rectifier-inverter drives for aircraft control surface actuation. The dc-link capacitor is one of the most unreliable and bulky components in such systems. A reduction in size makes more reliable capacitor technology viable and it was from this standpoint that the objectives of the research were initially set in Chapter 1.

Aircraft control surface actuation using electric drive technology is still actively being developed and there is a requirement to fully implement the ''More Electric Aircraft'' concept in commercial aircraft. Electric actuation of aircraft surfaces has many advantages compared to the conventional hydraulic actuation in commercial passenger aircraft. Flight dispatch figures are related to economics rather than safety *[16]*. As the dc-link capacitors are the least reliable component of the drive, it can be argued that the required reliability to meet the flight dispatch specifications can be achieved using a conventional three-phase dc-link converter if the dc-link capacitor can be replaced by a higher reliability smaller dc-link capacitor and by close control of the operating stress on the power devices. This has the potential to be a smaller, lighter and more efficient solution than the multiphase redundant systems proposed so far *[16]*.

A first simple point is that the higher the switching frequency the lower is the required size of the passive components. This makes the choice of a fully controlled rectifier as opposed to a diode bridge rather obvious. In addition a fully controlled rectifier offers control flexibility which has further advantages in respect of minimizing dc-link capacitance.

It has been demonstrated in this research that the size of the dc-link capacitor is determined by the difference in the power demanded by the inverter and supplied from the rectifier.

A study of previous research work in this area suggests that most of the contemporary methods to reduce dc-link size require significant hardware modifications. This research has shown that power balancing methods seem to offer better solutions towards reducing dc-link filtering components. These methods have so far tended to rely on measuring dc-link quantities, however work on experiments with these methods showed that they are unreliable when based on dc-link measurements and that methods based on a switch estimation method performed far better. Using this switch estimation method the difference between the powers on both sides of the dc-link is calculated and compensated via a modified rectifier control so as to allow lower power injection into the dc-link capacitor.

The simulation results have also demonstrated that such a drive can be controlled using either sine-carrier or space vector switching methods. It was established that the for the purpose of achieving a smaller dc-link capacitor, the symmetric pulse modulation offers comparatively lower THD and this therefore is the preferred method for the proposed drive. Simulation results of the above proposed drive confirm that such a proposed drive can be simulated to satisfy the output requirements set in *[16]*.

6.2 Simulation and Validation

The findings of this thesis rely heavily on simulation. It was clearly necessary to validate the simulation philosophy and its accuracy. A small scale experimental drive was setup using a dc-link inverter supplying a permanent magnet motor. This system is similar to the proposed actuator system differing only in the rectifier stage which in the experimental system is a simple diode rectifier. The motor drives another permanent magnet servo drive which acts as a dynamometer. Another difference to the real actuator is that the system inertia is much lower in the experimental system. This tends to make the simulation a little harder as the faster dynamic response pushes mechanical time constants closer to those of the electrical system. The experimental drive was simulated using exactly the same principles as the proposed drive. Special modifications were made to the experimental drive to measure rectifier output and dc-link capacitor currents using miniature current sensors. It is not a simple matter to measure dc-link current because in this area it is vital to avoid extra inductance which requires very tight packaging of the DC bus. Methods were developed in the research (as described in Chapter 4) that were successful in producing accurate current

measurements without seriously affecting the physical layout of the DC bus. On the whole the measured results compared well with the simulated results. The biggest area of difficulty was in the variation in dc-link current ripple on the supply side caused by unbalance in the input ac supply. Whilst it is easy to measure the operating phase voltages, it is far from easy to determine accurately the effective supply impedance particularly because the laboratory supply's imbalance tends to vary significantly. The drive's inverter gate pulses were also measured and compared with the simulation's modulation signals. The two modulation results match closely and along with the current results engender confidence in the drive simulation philosophy.

6.3 Development and Simulated Testing of the Proposed Drive

As a first step the effect of reducing the dc-link capacitor on a conventional drive was examined. It was established that reducing the dc-link capacitance tended to force the rectifier into overmodulation which causes increasing switching times with increased VA rating with minimum change in dc-link power output. It was also established that reduction of the dc-link capacitance has a relatively small effect on supply current harmonics which are instead mostly controlled by the supply line filters. The effect of supply line inductance, dc-link controller loop gain and dc-link capacitor size on drive stability for the conventional drive were analyzed and it was verified that the stability limits are as suggested using the relations given in *[85]*. This analysis helps establish the minimum value of dc-link capacitor for a given dc-link control loop gain and supply inductance.

Detail simulation work was carried out to establish dc-link dependency on various drive parameters. From this study (Chapter 5) it became clear that minimizing the power injection into dc-link capacitor allowed the capacitor to be smaller and that this in turn leads to the requirement to have a detailed, real time, knowledge of switching device status. Based on switching information, a rectifier controller modification was suggested with an aim to reduce the size of the dc-link capacitor with minimal changes. This uses a switch estimation mechanism and a calculated compensation factor that is applied to the rectifier control loop for the dc-link voltage. Simulation results for both the conventional and the proposed drive were presented in Chapter 5. The simulation showed that the proposed drive was able to operate successfully with only 20 μF in the dc-link and was able to offer lower THD as

compared to the conventional drive with 71 μF for the same supply filter inductance values. There is a penalty for such a small capacitance in the form of increased dc-link ripple and reduced dc-link voltage but neither of these effects are enough to prevent the proposed control arrangement being viable.

In the case of the proposed converter because the dc-link power is estimated in real time and compensated via the modified controller, the relation given in *[85]* no longer applies and theoretically the drive should be able to remain stable even with a miniature dc-link capacitor. Simulation results were presented in Chapter 5 for a case with just 2 μF dc-link capacitance using the proposed rectifier controller with a satisfactory performance.

According to the aircraft power standard MIL-STD-704F *[99]*, the maximum allowable voltage unbalance for the 400Hz AC supply cannot exceed 3% R.M.S. The supply current harmonic current has to be under 5% and the DC voltage ripple cannot exceed 6V (for 270V system). The supply line inductance and dc-link capacitor values were selected for the proposed drive to satisfy the harmonic and ripple requirements and then the performance of the proposed drive under supply unbalanced conditions was simulated and analyzed. It was shown that a phase voltage unbalance of 3% (as per the specification) does not significantly affect the proposed drive's performance.

Fault ride through is clearly an important feature for an aerospace actuator. In the particular case of actuators for high-lift surfaces, which is the major target of this research, operation through a system fault is not absolutely paramount because the safety of the system is guaranteed by power-off brakes which lock the surface in its current position and aircraft are designed to be able to fly and land with the high lift surface in any position. On takeoff the high lift surfaces are often essential but they would be moved into position before takeoff so again locking them in take-off position will not threaten safety. None the less some element of fault ride through is desirable and simulations described in Chapter 5 showed the natural relation between the dc-link capacitor size and fault ride through capability. Examining the dc-link and input power waveforms established that when the peak dc-link power falls below the instantaneous maximum input power, the drive becomes unstable. However if the supply phase voltage is reinstated before the dc-link power falls below the input power, the proposed drive regains complete control. This simulation shows that the maximum allowed duration of a fault plays an important role in deciding the dc-link capacitor size.

6.4 Final Conclusions and Future Work

The overall objective of the research was to improve the reliability of conventional dc-link converters in order to reach failure rates low enough to eliminate the need for fault tolerant drives. The critical issue in the system is the lack of reliability of the dc-link capacitor. Reducing its size will allow a change to a much more reliable technology. This research has shown that much lower dc-link capacitors are possible. If a fully switched rectifier stage with conventional control is pushed to the edge of stability a capacitance of only 71μF film capacitor is viable. This may be compared to a figure of 950 μF *[16]* which would be commonly used per phase in current practice for the same application.

It has been found that using knowledge of the switching states in the converter allows a tighter control of the power flow to the dc-link capacitor via a compensation term in the rectifier's controller for the dc-link voltage. Simulations suggest that a figure of only 20μF is viable with the control method proposed in this work. This seems to promise major improvements to system reliability because such a small value dc-link capacitor can be realized by high reliability film capacitors as discussed in Chapter 2.2.5. With careful control of the stresses on the rest of the components in the system it may be enough to meet flight dispatch figures for actuators driven by a more or less conventional three-phase PMSM drive. This would give major weight, space and cost savings over the proposed fault drive tolerant system of *[16]*.

A simulation has been developed which has been validated using measured data. It has been shown that successful measurements can be made of dc-link currents using miniature current sensors. It has only been possible within this research to examine the feasibility of the proposed system in simulation. The obvious requirement is that the system be proved experimentally.

If the overall objectives of the research are to be fully achieved it is necessary to reexamine the reliability of the full converter in the presence of a much higher reliability capacitor. It is likely that careful control of device stresses will be needed to reach the required reliability demanded by the commercial pressures of flight dispatch requirements.

REFERENCES

[1] Botten S.L., Whitley C.R., King A., ''Flight Control Actuation Technology for Next Generation All-Electric Aircraft'', TRW Aeronautical Systems, Technology Review Journal, Millennium Issue, Fall/Winter 2000.

[2] Churn P.M., Maxwell C.J., Schofield N., Howe, D., Powell D.J., ''Electro-hydraulic actuation of primary flight control surfaces'', IEE Colloquium on All Electric Aircraft, IEE, June1998. pp.3/1-3/5.

[3] NASA Dryden News Releases. December 1998.Release:98-84.

[4] Weimer J.A., ''The role of electric machines and drives in the more electric aircraft''., Electric Machines and Drives Conference, 2003. IEMDC'03, Air Force Res. Lab., Wright-Patterson AFB, OH, USA; 1-4 June 2003, Vol.1, pp.11-15.

[5] Dixon R., Gifford N., Sewell C., Spalton M.C., ''REACTS: reliable electrical actuation systems '', ABB ALSTOM POWER Technol. Centre, Leicester; Electrical Machines and Systems for the More Electric Aircraft (Ref. No. 1999/180), IEE Colloquium , London, 1999, UK , pp.5/1-516.

[6] Richter E., Radun A.V.E, Ferreira C., Ruckstader E., "An integrated electrical starter/generator system for gas turbine application, design and test results", Proc.ICEM, Paris, 1994.

[7] Richter E., "Switched reluctance machines for high performance operations in a harsh environment-A review paper", Proc. ICEM, Boston, 1990.

[8] Richter E., "High temperature switched reluctance motors and generators for future aircraft engine applications", Proc. American Control Con.,Atlanta , June 1988, pp.1846-1851.

[9] Stèphens C.M., "Fault detection and management system for fault tolerant switched reluctance motor drives", IEEE Trans. Ind. Application., Vol. 27, Nov. 1991, pp.1098-1102.

[10] Ferreira A.A., Jones S.R., Drager B.T., Heglund W.S., "Design and implementation of a five-hp switched reluctance, fuel-lube, pump motor drive for a gas turbine engine", IEEE Trans. Power Electron., vol. 10, pp. 55-61, Jan. 1995.

[11] Jack A.G., Mecrow B.C., "Safety critical drives for aerospace applications", Proc. ICEM Conf, Paris, 1994.

[12] Jack A.G., Mecrow B.C., Haylock J.A., "A comparative study of permanent magnet and switched reluctance motors for high-performance fault-tolerant applications'', Newcastle upon Tyne University, Industry Applications, IEEE Transactions , Jul/Aug 1996,Volume: 32, Issue: 4, pp.889-895.

[13] Bennett J.W., Mecrow B.C., Jack A.G., Atkinson D.J., Sewell C., Mason G., Sheldon S., Cooper, B., ''Choice of drive topologies for electrical actuation of aircraft flaps and slats'', Newcastle upon Tyne Univ., UK; Power Electronics , Machines and Drives, 2004. (PEMD 2004), Second International Conference on (Conf. Publ. No. 498), March-April 2004,volume-1, pp.332-337 .

[14] Bennett J.W., Jack A.G., Mecrow B.C., Atkinson D.J, Sewell C, G. Mason. Fault-tolerant control architecture for an electrical actuator. 2004 IEEE 35th Annual Power Electronics Specialists Conference, IEEE. Part Vol.6, 2004 2004, pp.4371-7.

[15] Jahns T.M., "Improved Reliability in Solid State A.C. Drives by means of Multiple Independent Phase-Drive Units", IEEE Trans. IAS, Vol. 16, no. 3, May 1980, pp321-331.

[16] Bennett J.W., Mecrow B.C., Atkinson D.J., Sheldon S., Cooper B., Mason G., Sewell C., Cudley D., ''A Prototype Electrical Actuator for Aircraft Flaps and Slats'', IEEE IEMDC Conference 2005, San Antonio, Texas, pp.41-47.

[17] IEEE Recommended Practice for Reliable Industrial and Commercial Power Systems, IEEE Gold Book, ISBN 1-55937-969-3.

[18] Tavner P.J., Hasson J.P., "Predicting the Design Life of High Integrity Rotating Electrical machines", IEE Ninth International Conference on Electrical Machines and Drives, EMD 99, Canterbury, UK, Sept. 1st -3rd 1999, pp.286-290.

[19] Mecrow B.C., Jack A.G., Haylock J.A., Coles J., "Fault Tolerant Permanent Magnet Machines Drives", IEE Proceedings Electrical Power Applications, November 1996.V-143, pp.437-442.

[20] Venturini M., "A new sine wave in sine wave out, conversion technique which eliminates reactive elements", Proc. POWERCON 7, 1980, pp.E3_1–E3_15.

[21] Venturini M., Alesina A., "The generalized transformer: A new bidirectional sinusoidal waveform frequency converter with continuously adjustable input power factor," in Proc. IEEE PESC'80, 1980,pp. 242–252.

[22] Whitley C.R., Towers G.K., Wheeler P., Clare J., Bradley K., Apap M., Empringham L., ''A Matrix Converter based Electro-Hydrostatic Actuator'', IEE

Matrix Converter Conference ,April 2003.Smiths Aerospace Actuation Systems-Wolverhampton ,UK, pp.6/1- 6/5.

[23] Aten M., Whitley C., Towers G., Wheeler P., Clare J., Bradley K., ''Dynamic performance of a matrix converter driven electro-mechanical actuator for an aircraft rudder, Smiths Aerospace Actuation Systems'', Wolverhampton ,UK, Power Electronics, Machines and Drives, 2004. (PEMD 2004), Second International Conference on (Conf. Publ. No. 498), March-April 2004, Volume: 1, pp.326-331.

[24] Takahashi I., Itoh Y., ''Electrolytic capacitor-less PWM inverter'', Proceeding IPEC-Tokyo,1990, pp131-138.

[25] US Patent 5481451 - Kuwahara, Naruto, AC-to-AC power inverter apparatus functioning without smoothing capacitor, and control method thereof, January-1996.

[26] US Patent 6313602 - Arefeen, Mohammed, Shireen, Wajiha, Modified space vector pulse width modulation technique to reduce DC bus ripple effect in voltage source inverters, November-2001.

[27] Shireen W., ''An AC-DC-AC Converter with Smaller DC-Link Capacitor for Space Power Distribution Systems'', ISSO-UH/UHCL/NASA, pp.96-99.

[28] US Patent 6839249 - Kalman, Gabor, Huggett, Colin, Honeywell International Inc.,AC-to-ac power converter without a dc-link capacitor, January-2005.

[29] Habetler T.G., Divan D.M., ''Rectifier/inverter reactive component minimization'', Industry Applications, IEEE Transactions on Volume 25, Issue 2, Mar/Apr 1989, pp.307-316.

[30] Bose B.K., Kastha D., ''Electrolytic capacitor elimination in power electronic system by high frequency active filter'', Industry Applications Society Annual Meeting, 1991, IEEE, 28 Sep-4 Oct 1991,Vol.1, pp.869-878.

[31] Ziogas P.D., Kang Y.G., Stefenovic V.R., ''Rectifier-inverter frequency-changers with suppressed dc-link components'', IEEE Trans. Ind. Appl., vol. IA-22, Nov./Dec 1986, pp.1027-1036.

[32] Takahashi I., Itoh Y., ''Electrolytic capacitor less PWM inverter'', Int'l Pow. Elec.Conf. Rec., Tokyo, 1990, pp.131-138.

[33] Kim J.S., Sul S.K., ''New control scheme for AC-DC-AC converter without DC link electrolytic capacitor'', Power Electronics Specialists Conference, 1993. PESC apos;93 Record., 24th Annual IEEE, Volume/Issue , 20-24 Jun 1993.pp.300 – 306.

[34] Minari Y.; Shinohara K., Ueda R., ''PWM-rectifier/voltage-source inverter without DC link components for induction motor drive'', Electric Power Applications, IEE Proceedings B, Volume 140, Issue 6, 1993, pp.363 – 368.

[35] Alakula M., ''Vector controlled AC/AC converters with a minimum of energy storage.'', Industry Applications Society Annual Meeting, 1994., Oct 1994, vol.2, pp.1130-1134.

[36] Wheeler N.J., Zhang H., Grant D.A., ''Minimisation of reactive component values in back-to-back converters'', Power Electronics and Variable-Speed Drives Conference, 1994, Issue 26-28 Oct 1994 pp.240-245.

[37] Malesani L., Rossetto L., Tenti P., Tomasin P., ''AC/DC/AC PWM converter with reduced energy storage in the DC link'', Industry Applications, IEEE Transactions on industry applications, Mar/Apr 1995, Volume:31, Issue: 2, pp.287-292.

[38] Dahono P.A., Sato Y., Kataoka T., ''Analysis and minimization of ripple components of input current and voltage of PWM inverters'', IEEE Industry Applications Conference, 8-12 Oct 1995, Orlando, FL, USA ,Volume: 3, pp.2444-2450.

[39] Wen-Song Chien, Ying-Yu Tzou, ''Analysis and design on the reduction of DC-link electrolytic capacitor for AC/DC/AC converter applied to AC motor drives'', Power Electronics Specialists Conference, 1998. PESC 98, IEEE, Volume-1, Issue-17-22, May 1998, pp.275-279.

[40] Kretschmar K., Nee H., ''An AC converter with a small DC link capacitor for a 15 kW permanent magnet synchronous integral motor'', Inst. of Technol., Stockholm, Power Electronics and Variable Speed Drives, 1998. Seventh International, Sep 1998, pp.622-625.

[41] Piepenbreier B., Sack L., ''Regenerative drive converter with line-frequency switched rectifier and without DC link components'', Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual 20-25 June 2004, Volume 5, pp.3917- 3923.

[42] Joohn-Sheok Kim, Seung-Ki Sul, ''Resonant link bidirectional power converter. II. Application to bidirectional AC motor drive without electrolytic capacitor'', IEEE Transactions on Power Electronics, Volume 10, Issue 4, Jul 1995, pp.485 – 493.

[43] Namho Hur, Jinhwan Jung, Kwanghee Nam, ''A fast dynamic DC-link power-balancing scheme for a PWMconverter-inverter system'', IEEE Transactions on Industrial Electronics, Volume 48, Issue 4, Aug 2001, pp.794 – 803.

[44] Marchesoni M., ''DC-link filter capacitors reduction in multilevel modular H-bridge converter structures'', Dipt. di Ingegneria Elettrica, Universita degli Studi di Genova, Italy, Proceedings of the 2002 IEEE International Symposium on Industrial Electronics, 2002. ISIE 2002. 2002, Volume: 3, pp.902-907.

[45] Kieferndorf F.D., Forster M., Lipo T.A., ''Reduction of DC-bus capacitor ripple current with PAM/PWM converter'', Univ. of Wisconsin, Madison, WI, USA, IEEE Transactions on Industry Applications, March-April 2004 Volume: 40, Issue: 2, pp.607-614.

[46] Hobraiche J., Vilain J.P., Plasse C., ''Offline optimized pulse pattern with a view to reducing DC-link capacitor application to a starter generator'', IEEE Power Electronics Specialists Conf., June 2004, Vol-5, pp.3336- 3341.

[47] Liutanakul P., Pierfederici S., Meibody-Tabar F., ''DC-link capacitor reduction of a controlled rectifier supplying N inverter-motor drive systems by compensating the load variations'', IEEE 35th Annual Power Electronics Specialists Conference, Volume 2, Issue-20-25, June 2004, pp.1298 – 1303.

[48] Gu B.G., Nam K.A., ''Theoretical minimum DC-link capacitance in PWM converter-inverter systems'', IEE Proceedings Electric Power Applications, Volume 152, Issue-1, Jan. 2005, pp.81-88.

[49] Gu B.G., Nam K.A., ''A DC-link capacitor minimization method through direct capacitor current control''. IEEE Transactions on Industry Applications, Volume 42, Issue 2, March-April 2006, pp.573-581.

[50] Saren H., Pyrhonen O., Rauma K., Laakkonen O., ''Overmodulation in Voltage Source Inverter with Small DC-link Capacitor'', IEEE Power Electronics Specialists Conf., Issue 11-14, Sept. 2005, pp.892-898.

[51] Lamsahel H., Mutschler P., Reddy M., ''Controlling voltage source converters with minimal energy storage'', European Conference on Power Electronics and Applications, Sept. 2005, pp.9.

[52] Saren H., Pyrhonen O., Luukko J., Laakkonen O., Rauma K., ''Verification of frequency converter with small DC-link capacitor'', European Conference on Power Electronics and Applications, Issue11-14, Sept-05, pp.10.

[53] Gosdu J. F., Elles A.C., Bailey R.R, ''Design and Application of Polycarbonate Capacitors in Aerospace AC Power Systems'', NASA Open study report, Washington DC, Aug-71.

[54] Terzulli G., Peace B.W., ''Film Technology to Replace Electrolytic Technology'', AVX Corporation, www.avx.com.

[55] Esteban F., Vázquez I.,''Film Capacitors for DC-Link Application in Industrial Converters'' EPCOS S, www.epcos.com.

[56] Landrock, Clinton K., Kaminska, Bozena, ''High Temperature Polymer Capacitors for Aerospace Applications'', Design Automation & Test in Europe Conference & Exhibition, 2010, pp.1349-1352.

[57] EPCOS, ''Film Capacitors – Power Electronic Capacitors'', (http://www.epcos.com/inf/20/50/ds/B25655J8567K.pdf)

[58] Gillingham et al., United States Patent US5743490, ''Flap/Slat Actuation System for an Aircraft'', Apr-1998.

[59] Wheeler P.W et al., ''Matrix Converters: A Technology Review'', IEE Transaction on Industrial Electronics, Vol.49, April 2002.

[60] Morel, F.; Retif, J.-M.et al.; ''A predictive control for a matrix converter fed permanent magnet synchronous machine'', Power Electronics Specialists Conference, 2008. PESC 2008. IEEE , 2008 , pp 15 – 21.

[61] L. Empringham, L. de Lillo, P. W. Wheeler, and J. C. Clare, "Matrix Converter Protection for More Electric Aircraft Applications," in IEEE Industrial Electronics, IECON Conference , Paris, France, Nov. 2006, pp. 2564–2568.

[62] J. Mahlein and M. Braun, "A matrix converter without diode clamped over-voltage protection," in Power Electronics and Motion Control Conference, Proceedings. IPEMC 2000. Vol. 2, Beijing, Aug. 15–18, 2000, pp. 817–822.

[63] J. Mahlein, M. Bruckmann, and M. Braun, "Passive protection strategy for a drive system with a matrix converter and an induction machine,"IEEE Trans. Ind. Electron., vol. 49, no. 2, pp. 297–303, Apr. 2002.

[64] A. Schuster, "A matrix converter without reactive clamp elements for an induction motor drive system," in Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE, vol. 1, Fukuoka, May 17–22, 1998, pp. 714–720.

[65] Nowakowski R., King B.;'' Choosing the optimum switching frequency of your DC/DC converter'',Texas Instrument Report.May-2010.

[66] Huo B., Flint T., Moynihan F.; ''Improved single current sensing method and its realization based on ADMCF341 DSP Controller'', Analog Devices, Intelligent Motion Proceedings,2001.pp.281.

[67] Bodkhe S.B., Aware M.V.; ''Speed-sensorless, adjustable-speed induction motor drive based on dc link measurement'', International Journal of Physical Sciences, Vol. 4 (4), pp. 221–232, April 2009.

[68] Pillay P., Krishnan R., ''Modeling of permanent magnet motor drives'', IEEE Transactions on Industrial Electronics, Volume 35, Issue 4, Nov 1988, pp.537–541.

[69] Markku Niemela, ''Position Sensorless Electrically Excited Synchronous Motor Drive for Industrial use based on Direct Flux Linkage and Torque Control'', PhD Thesis, Lappeenranta University of Technology.1999, pp 10-26,126-127.

[70] Prasad H.P., '' Analysis and Comparison of Space Vector Modulation Scheme for Three-Leg and Four-Leg Voltage Source Inverters'', Master of Science Thesis, Electrical Engineering, May 15, 1997, Blacksburg, Virginia Polytechnic Institute and State University.

[71] Mariusz Malinowski, ''Sensorless Control Strategies for Three - Phase PWM Rectifiers'', Ph.D Thesis, Warsaw University of Technology,Electrical Engineering, Institute of Control and Industrial Electronics,Poland.2001.

[72] Control Techniques, User Guide, Unidrive, Model sizes 1 to 5, Universal Variable Speed AC Drive for induction and servo motors, Issue Number:9.

[73] Stefan Soter, Ralf Wegener, Jens Dopheide, Bj¨orn Kiffer, ''Low Cost Vector Control for Permanent-Magnet-Synchronous motor with only one DC-Link current Sensor for Pumping Application'', IEMDC 2005, 15-18.05.2005, San Antonio, TX, USA,

[74] LEM Current Transducer, FHS 40-P/SP600 manual, www.lem.com.

[75] Boys J. T., "Novel Current Sensor for PWM AC Drives", IEE Proc.1988, Vol. 135, Pt. B, No. 1, pp.27–32.

[76] Green T. C., Williams B.W., "Derivation of Motor Line-Current Waveforms from the DC-Link Current of an Inverter", IEE Proc.1989, Vol. 136, Pt. B, No.4, pp.196–204.

[77] Green T.C., Williams B.W., "Control of Induction Motors Using Phase Current Feedback Derived from the DC Link", EPE Aachen 1989, pp.1391–1396.

[78] Habetler T. G., Divan D.M., "Control Strategies for Direct Torque Control Using Discrete Pulse Modulation'', IAS-1989, pp.514–522.

[79] Petruzziello F., Zoos G., Ziogas P.D., "Some Implementation Aspects of Line Current Reconstruction in Three Phase PWM Inverters", IECON '1990, pp.1149–1154.

[80] Joo Hyeong-Gil, Youn Myung-Joong, Shin Hwi-Beom, ''Estimation of Phase Currents from a DC-Link Current Sensor Using Space Vector PWM Method'', Electric Power Components and Systems,V-28:11, 1053 – 1069.

[81] Reese R.W., Wei L., Lukaszewski R.A., ''An indirect method of measuring DC bus capacitor current'', Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, Austin, TX, APEC 2005, 6-10 March 2005, Volume: 2, pp.971-978.

[82] Rogowski Coil, http://www.powertekuk.com/cwtmini.htm

[83] Timothy L. Skvarenina, Electronics Handbook, Industrial Electronic Series, CRC Press, ISBN 0-8493-7336-0.

[84] Carlsson A, ''The back to back converter control and design'' PhD thesis, Dept.of Industrial EE & Automation., Lund Inst. of Tech., Sweden, 1998.

[85] Klumpner C., Thiwanka Wijekoon, Wheeler P., ''Active Compensation of Unbalanced Supply Voltages for Two-Stage Direct Power Converters Using the Clamp Capacitor'', 36th IEEE Power Electronics Specialists Conference, 2005. PESC '05, June 2005,pp 2376-2382.

[86] Annette von Jouanne, Banerjee B., ''Assessment of Voltage Unbalance'',IEEE Transaction of Power Delivery Vol.16, No. 4, Oct-2001.

[87] Murali M. Baggu, Badrul H. Chowdhury, ''Implementation of a Converter in Sequence Domain to Counter Voltage Imbalances'', IEEE Power Engineering Society General Meeting, 2007. pp.1-5.

[88] Yongsug Suh, Thomas A. Lipo, ''A Control Scheme in Hybrid Synchronous-Stationary Frame for PWM AC/DC Converter under Generalized Unbalanced Operating Conditions'' IEEE Transaction on Industry Applications, Vol-42, Issue-3 pp-825-835.

[89] Muljadi E., Schiferl R., Lipo T. A., "Induction machine phase balancing by unsymmetrical thyristor voltage control," IEEE Trans. Industry Applications, vol. IA-21, no. 4, pp. 669–678, May/June 1985.

[90] Lee C. Y., "Effects of unbalanced voltage on the operation performance of a three-phase induction motor," IEEE Trans. Energy Conversion, vol.14, no. 2, pp. 202–208, June 1999.

[91] Enjeti P.N., Choudhury S.A., "A new control strategy to improve the performance of a PWM AC to DC converter under unbalanced operating conditions," IEEE Trans. Power Electron., vol. 8, pp. 493–500, Oct. 1993.

[92] Song S.A, Nam K., "Dual current control scheme for PWM converter under unbalanced input voltage conditions," IEEE Trans. Industrial Electronics, vol. 46, no.5, pp. 953–959, Oct. 1999.

[93] Kang J.K., Sul S.K., Kwanak-Ku S.D., "Control of unbalanced voltage PWM converter using instantaneous ripple power feedback," in IEEE Conference, 1997, pp.503–508.

[94] Morán L., Ziogas P.D., Joos G., "Design aspects of synchronous PWM rectifier-inverter systems under unbalanced input voltage conditions," IEEE Trans. Industry Applications, vol. 28, no. 6, pp. 1286–1293, Nov./Dec. 1986.

[95] Stankovic A.V., T. A. Lipo, "A novel control method for input output harmonic elimination of the pwm boost type rectifier under unbalanced operating conditions," IEEE Trans. on Power Electronics, vol. 16, no. 5,Sept. 2001, pp. 603-611.

[96] Homeyer W.G., Bowles, E.E., Lupan S.P., Rodriguez C., Walia P.S., Shah N.M., Maldonado M.A., Gen. Atomics, San Diego, CA, ''Advanced power converters for More Electric Aircraft applications'', Proceedings of the 31st Intersociety Energy Conversion Engineering Conference, 1996. IECEC 96.,Vol-1,pp.137-142.

[97] MIL-STD-704F , ''Aircraft Electric Power Characteristics'', Department of Defense Interface Standard,March-2004.

[98] Rodr'ıguez J., Dixon J., Espinoza J., Lezana P., ''PWM Regenerative Rectifiers: State of the Art'', IEEE Transactions on Industrial Electronics, Feb.2005. Vol-52, pp-5-22.

[99] Ooi B.T., Dixon J.W., Kulkarni A.B., Nishimoto M., "An integrated AC Drive System Using a Controlled-Current PWM Rectifier/Inverter Link," IEEE Transactions on Power Electronics, Jan. 1988, Vol. 3, N1, pp. 64-71.

[100] Illinois Capacitor Inc., ''Supercapacitors'', www.illcap.com

[101] Zhang Y.C., Wei Li., et al., ''Study of supercapacitors in the application of power electronics'', WSEAS Transaction on circuits and systems, June-09.pp. 508-517.

[102] Linzen, D. Buller, S. Karden, E. De Doncker, R.W., ''Analysis and evaluation of charge balancing circuits on performance, reliability and lifetime of supercapacitor systems '', Industry Applications Conference, Oct-03, Vol.3,pp.1589-1595.

[103] Esteban F., Vazquez I., ''Film capacitors for dc-link applications in industrial converters'', EPCOS S.A. Spain, www.epcos.com.