NANOSCALE CHARACTERISATION OF DIELECTRICS FOR ADVANCED MATERIALS AND ELECTRONIC DEVICES

A THESIS SUBMITTED TO THE FACULTY OF ENGINEERING FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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Abstract

Strained silicon (Si) and silicon-germanium (SiGe) devices have long been recognised for their enhanced mobility and higher on-state current compared with bulk-Si transistors. However, the performance and reliability of dielectrics on strained Si/strained SiGe is usually not same as for bulk-Si. Epitaxial growth of strained Si/SiGe can induce surface roughness. The typical scale of surface roughness is generally higher than bulk-Si and can exceed the device size. Surface roughness has previously been shown to impact the electrical properties of the gate dielectric. Conventional macroscopic characterisation techniques are not capable of studying localised electrical behaviour, and thus prevent an understanding of the influence of large scale surface roughness. However scanning probe microscopy (SPM) techniques are capable of simultaneously imaging material and electrical properties.

This thesis focuses on understanding the relationship between substrate induced surface roughness and the electrical performance of the overlying dielectric in high mobility strained Si/SiGe devices. SPM techniques including conductive atomic force microscopy (C-AFM) and scanning capacitance microscopy (SCM) have been applied to tensile strained Si and compressively strained SiGe materials and devices, suitable for enhancing electron and hole mobility, respectively. Gate leakage current, interface trap density, breakdown behaviour and dielectric thickness uniformity have been studied at the nanoscale. Data obtained by SPM has been compared with macroscopic electrical data from the same devices and found to be in good agreement. For strained Si devices exhibiting the typical crosshatch morphology, the electrical performance and reliability of the dielectric is strongly influenced by the roughness. Troughs and slopes of the crosshatch morphology lead to degraded gate leakage and trapped charge at the interface compared with peaks on the crosshatch undulations. Tensile strained Si material which does not exhibit the crosshatch undulation exhibits improved uniformity in dielectric properties. Quantitative agreement has been found for leakage at a device-level and nanoscale, when accounting for the tip area. The techniques developed can be used to study individual defects or regions on dielectrics whether grown or deposited (including high-κ) and on different substrates including strained Si on insulator (SSOI), strained Ge on insulator (SGOI), strained Ge, silicon carbide (SiC) and graphene. Strained SiGe samples with Ge content varying from 0 to 65% have also been studied. The increase in leakage and trapped charge density with increasing Ge extracted from

SPM data is in good agreement with theory and macroscopic data. The techniques appear to be very sensitive, with SCM analysis detecting other dielectric related defects on a 20% Ge sample and the effects of the 65% Ge later exceeding the critical thickness (increased defects and variability in characteristics).

Further applications and work to advance the use of electrical SPM techniques are also discussed. These include anti-reflective coatings, synthetic chrysotile nanotubes and sensitivity studies.

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Publications

Journal papers

- **R. Kapoor**, E. Escobedo-Cousin, S. H. Olsen, and S. J. Bull, "Nanoscale Characterization of Gate Leakage in Strained High-Mobility Devices," *IEEE Transactions on Electron Devices,* vol. 58, pp. 4016-4023, 2011.
- **R. Kapoor**, E. Escobedo-Cousin, S. H. Olsen, and S. J. Bull, "Characterising Gate Dielectrics in High Mobility Devices Using Novel Nanoscale Techniques," *Microelectronics Reliability,* vol. 50, pp. 1484-1487, 2010.

Conferences

- **R. Kapoor**, S. H. Olsen, D. M. Buca, and J. M. Hartmann, "Nanoscale analysis of electrical properties of thin dielectrics on strained SiGe." **Conference**: European Materials Research Society (E-MRS), Spring meeting, **Location**: Strasbourg, France, **Date**: May 14-18, 2012.
- S. H. Olsen, **R. Kapoor**, and S. J. Bull, "(Invited) Scanning Probe Analysis of Dielectrics on High Mobility Substrates," *ECS Transactions*, vol. 45 (3), pp. 69-78, 2012. **Conference**: 221st ECS meeting, **Location**: Seattle, Washington, **Date**: May 6-10, 2012.
- **R. Kapoor**, E. Escobedo-Cousin, S. H. Olsen, and S. J. Bull, "Characterising Gate Dielectrics in High Mobility Devices Using Novel Nanoscale Techniques." **Conference:** 21st European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis (ESREF), **Location:** Gaeta, Italy, **Date:** October 11-15, 2010.

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a_o	AFM tip-sample contact radius
a_{Si}	Average lattice constant of bulk relaxed Si
a_{SiGe}	Average lattice constant of bulk relaxed SiGe
$a_{SiGe}^{\parallel}$	In-plane lattice constant of the strained layer
$a_{SiGe}^{\perp}$	Perpendicular lattice constant of the strained layer
A_{eff}	Effective AFM tip-sample contact area
A_o	Vibration amplitude of the non-contact AFM tip
C_{dep}	Depletion capacitance
C_{hf}	High frequency MOS capacitance
C_{ox}	Gate dielectric capacitance
C_{tip}	SCM tip-sample capacitance
C_{tot}	Total capacitance of a MOS capacitor
d	Film thickness
D_{it}	Interface trap density
dC/dV	Differential capacitance
E^*	Contact modulus of the contacting surfaces
E_c	Conduction band energy
E_d	Young's modulus of the dielectric material
E_{eff}	Effective electric field
E_F	Fermi level energy
E_g	Band gap energy
E_i	Intrinsic energy level
E_{ox}	Oxide electric field
E_{tip}	Young's modulus of the tip material
E_v	Valence band energy
F'	Force gradient
f_1	Operating frequency of the non-contact AFM tip
f_{ac}	AC signal frequency
f_o	Resonant frequency of the non-contact AFM tip
f_{eff}	Effective resonant frequency of the non-contact AFM tip
h	Planck's constant
h_c	Strained layer critical thickness

I_{ds}	Drain-source current
I_{ds}^{diff}	Diffusion current in the sub-threshold regime
I_{dsat}	Drain-source current in saturation
I_g	Gate leakage current
J_{FN}	Gate leakage in Fowler-Nordheim regime
J_g	Gate leakage current density
k	Boltzmann's constant
k_o	Intrinsic spring constant of the non-contact AFM tip
k_{eff}	Effective spring constant of the non-contact AFM tip
L_g	Gate length
m	Free electron mass
m^*	Effective carrier mass
m_{ox}	Effective electron mass in the dielectric
n	Integer
n_i	Intrinsic carrier concentration
N_{sub}	Substrate doping
N_c	Effective density of states in the conduction band
N_v	Effective density of states in the valence band
P	Normal contact force exerted by the AFM tip
Q_f	Fixed charge in the bulk of the dielectric
Q_{it}	Interface trapped charge
R	Relative radius of curvature of contacting bodies
R_d	Radius of curvature of the dielectric surface
R_{deg}	Degree of relaxation in the semiconductor
R_q	Root Mean Square (rms) surface roughness
R_{tip}	Radius of curvature of the AFM tip
q	Electron charge
T	Temperature
t_{ox}	Dielectric thickness
V_{ac}	Applied AC bias
V_{dc}	Applied DC bias
V_{ds}	Drain-source voltage
V_{dsat}	Drain-source voltage at the onset of saturation
V_{FB}	Flatband voltage
$V_{FB, ideal}$	Ideal flatband voltage

$V_{FB, shift}$	Shift in V_{FB} from $V_{FB, ideal}$
V_g	Gate voltage
V_{off}	Offset voltage
V_{ox}	Oxide voltage drop
V_{poly}	Potential drop in the poly-Si gate
V_{rms}	Root mean square value of the ac bias
V_s	Supply voltage
V_{sub}	Potential drop in the semiconductor substrate
V_t	Threshold voltage
V_{tip}	AFM tip voltage
$V_{tip, peak}$	AFM tip voltage at peak dC/dV
W_g	Gate width
x	Ge concentration in the $Si_{1-x}Ge_x$ alloy
α	Dimensional scaling factor
χ	Electron affinity
ΔA	Change in vibration amplitude of non-contact AFM tip
ΔC	Slope of capacitance
$\Delta \omega$	Angular separation in XRD
Δ_{p-v}	Peak-valley amplitude of surface undulations
ε_{Si}	Strain in Si
ε_{SiGe}	Strain in SiGe
κ	Dielectric constant
λ	Incident wavelength
λ_p	Distance between consecutive surface peaks
μ	Mobility
μ_{eff}	Effective mobility
ω	Incident angle in radians
ω_{Si-Si}	Si-Si lattice vibrations
$\omega_{Si-GeSi}$	Si-Ge lattice vibrations
ω_{Ge-Ge}	Ge-Ge lattice vibrations
φ_B	Potential barrier height
φ_m	Metal workfunction
φ_s	Semiconductor workfunction
ψ_s	Semiconductor potential difference between E_i and E_F
τ	Mean relaxation time between scattering events

θ	Incident angle in degrees
θ_c	Critical angle of incidence
υ	Poisson's ratio

Abbreviations

AFM	Atomic Force Microscopy
BOX	Buried Oxide
C-AFM	Conductive Atomic Force Microscopy
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapour Deposition
DT	Direct Tunnelling
EDX	Energy-Dispersive X-ray spectroscopy
EOT	Equivalent Oxide Thickness
F-N	Fowler-Nordheim
FET	Field Effect Transistor
FGA	Forming Gas Annealing
FWHM	Full Width at Half Maximum
Ge	Germanium
HF	Hydrofluoric acid
HH	Heavy Hole
IC	Integrated Circuit
IPA	Isopropyl Alcohol
ITRS	International Technology Roadmap for Semiconductors
KOH	Potassium Hydroxide
LH	Light Hole
LTO	Low Temperature Oxide
MBE	Molecular Beam Epitaxy
MIM	Metal Insulator Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NiSi	Nickel Silicide
NMP	N-Methyl-2-pyrrolidone
Poly-Si	Polycrystalline-Silicon
PSPD	Position Sensitive Photo Detector
RMS	Root Mean Square
RP-CVD	Reduced-Pressure Chemical Vapour Deposition
SCM	Scanning Capacitance Microscopy
SEM	Scanning Electron Microscope

SGOI	Strained Germanium on Insulator
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon-Germanium
SILC	Stress Induced Leakage Current
SIMS	Secondary Ion Mass Spectroscopy
SMT	Stress Memorisation Technique
SNR	Signal to Noise Ratio
SOI	Silicon on Insulator
SPM	Scanning Probe Microscopy
SRB	Strain Relaxed Buffer
SSOI	Strained Silicon on Insulator
STM	Scanning Tunnelling Microscope
TAT	Trap Assisted Tunnelling
TDD	Threading Dislocation Density
TEM	Transmission Electron Microscopy
VCO	Voltage Controlled Oscillator
XRD	X-ray Diffraction
XPS	X-ray Photoelectron Spectroscopy
XRR	X-ray reflectivity

Chapter 1. Introduction and Literature Survey

The underlying concept of the metal-oxide-semiconductor field-effect transistor (MOSFET) first appeared in the 1930 patent by Julius Edgar Lilienfield [1]. In 1935, Oskar Heil filed a British patent application which contains the first description of an insulated-gate FET [2]. More than a decade later, John Bardeen, Walter Brattain and William Shockley invented the first transistor using Ge crystal at the Bell labs in 1947 [3]. Mid 1950s saw a shift towards Si from Ge which was the initial choice for discrete devices [4]. This was due to the low cost of Si and its ability to form a high quality native oxide. In 1958, Jack Kilby at Texas Instruments was the first person to process different components on a single chip by putting together two bipolar transistors on a single Ge chip using gold contacts [5]. Improvements in planar technology in the 1950s led Robert Noyce at Fairchild Camera and Instrument Corp. in 1959 to present diffused transistors and resistors on a single Si chip interconnected by aluminium (Al) lines [6]. This is now widely known as the monolithic integrated circuit (IC) technology. The first successful Si MOSFET was reported by Kahng and Atalla at the Solid State Device Research Conference in 1960 [7]. The complementary MOS (CMOS) concept which proved to be extremely important in reducing power use by MOS transistors was first reported by Wanlass and Sah in 1963 [8].

In the year 1965, one of the founders of Fairchild Semiconductors who later on co-founded Intel as well, Gordon E. Moore observed a trend in the increase of number of transistors per chip. Moore predicted that the number of transistors on a chip will double about every two years [9]. This trend is widely known in the semiconductor industry as the 'Moore's Law'. Moore's law has significantly driven the technological and commercial success of the semiconductor industry for more than four decades.

While most ICs fabricated during the 1960s and 1970s were based on bipolar transistors, MOSFET based devices gained importance and took over the leading role in the early 1980s [10]. The emergence of the computer industry and the opportunities created by ICs made the MOSFET the basic element of every chip. Initial Si MOSFETs found applications in computer memories and microprocessors. Presently, the MOSFET is the elementary component of integrated circuits which power every analogue and digital electronic system. Nearly 80% of different semiconductor technologies utilise

MOS based devices [10]. The success of the semiconductor industry is largely attributed to Si based MOSFETs.

The basic MOSFET has seen aggressive scaling and multiple technological innovations since Moore's prediction triggered the microelectronics revolution. Polycrystalline Si (poly-Si) became the preferred gate electrode material in the 1970s while silicides of tungsten and titanium were incorporated into the gate stack in the 1980s [11]. These were replaced by cobalt and nickel silicide (NiSi) in the 1990s. At the turn of the century, Copper began to replace Al as contact metal due to its lower resistivity. Silicon dioxide (SiO_2) which has been the traditional choice for the oxide layer between the metal and the semiconductor has been scaled aggressively to a thickness < 1 nm. This has lead to the introduction of gate dielectrics with high permittivity commonly known as the high-κ dielectrics.

1.1 MOSFET fundamentals

Fig. 1.1 shows a schematic representation of a MOSFET with its four terminals: substrate, source, drain and gate. The substrate can be doped either p-type or n-type with the source and the drain having the opposite doping profile compared with the substrate. The gate terminal is separated by a thin insulating layer also known as the gate oxide or the gate dielectric. In an n-type MOSFET (similar to the one shown in Fig. 1.1), the substrate is doped p-type while the source and the drain have relatively higher levels of n-type doping. The doping profiles are reversed for p-type MOSFETs. MOSFETs are voltage controlled devices such that the voltage applied at the gate electrode modulates the flow of current.

The voltage applied at the gate terminal (V_g) controls the MOSFET operation. For an n-type MOSFET (Fig. 1.1), negative values of V_g accumulate the holes (majority carriers) from the underlying substrate. This results in an $n^+p^+n^+$ junction between the source, substrate and the drain. This is similar to two back to back diodes. The first diode goes from the source to the substrate and the other from the substrate to the drain. The two diodes have opposite orientation so that if one allows current flow the other can't. This situation is highly resistive and not much current can flow (the MOSFET is off). At V_g = 0 V an n^+pn^+ junction exists between the source, substrate and the drain which keeps the MOSFET in off state. At a positive V_g, the holes in the p-substrate near the oxide experience an electrostatic repulsive force which drives them away from the

oxide interface. This results in a depletion region (also known as the space charge region) near the semiconductor surface since the region is depleted of its native carriers, the holes. The depletion region is composed of the immobile acceptor ions of the substrate. As V_g increases further, all holes are driven away from the channel and some electrons (from source and drain) enter into the region just below the oxide interface. This region is now n-type (inverted) and results in an n-type inversion layer connecting the source and drain. This is a highly conductive state with no diode behaviour. In the presence of a potential difference between the source and the drain, current flow occurs between source and drain via the inversion channel.

Further increase in V_g requires an increase in electron concentration in the inversion layer. These electrons are supplied by the trap centres (such as dislocations and impurities) in the depletion layer. According to Sah *et al.*, generation and recombination of electron-hole pairs in the space charge region dominates the electrons in the inversion layer [12]. Generation and recombination of carriers is typically explained by the Shockley-Read-Hall, radiation and Auger recombination theories.
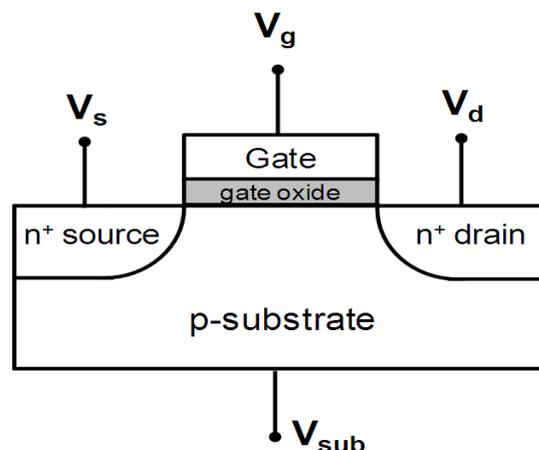
Figure 1.1 Schematic representation of an n-type MOSFET.

The value of V_g at which the electron density at the semiconductor surface equals the hole concentration in the bulk is known as the threshold voltage (V_t). The polarity of charge carriers and V_g which causes inversion are reversed for a p-type MOSFET.

The electrons flow from the source to the drain resulting in a flow of current from the drain to the source. At a given value of V_{ds}, the MOSFET operates in one of the following three regimes (Fig 1.2):

a. *Linear region*. At low values of V_{ds}, the channel exhibits resistive behaviour (current increases linearly with voltage) as shown in Fig. 1.2a. The drain-source current (I_{ds}) is proportional to V_{ds} in this region of operation.

b. *Onset of saturation*. At increased V_{ds}, the lateral electric field exceeds the vertically applied field (through the gate). This reduces the width of the channel at the drain end to zero. At the onset of saturation the channel is said to pinch-off at the drain end (Fig. 1.2b). The value of V_{ds} at pinch-off is called saturation voltage (V_{dsat}) at which I_{ds} begins to saturate.

c. *Saturation region*. Further increase in V_{ds} increases the region in which the drain voltage is higher than the gate voltage. This results in shifting of the pinch-off point towards the source. The channel becomes highly resistive across the pinched-off region. The voltage in the effective channel region is still V_{dsat} and consequently I_{ds} remains saturated at a constant value (I_{dsat}) as shown in Fig. 1.2c.

(a)

(b)

(c)
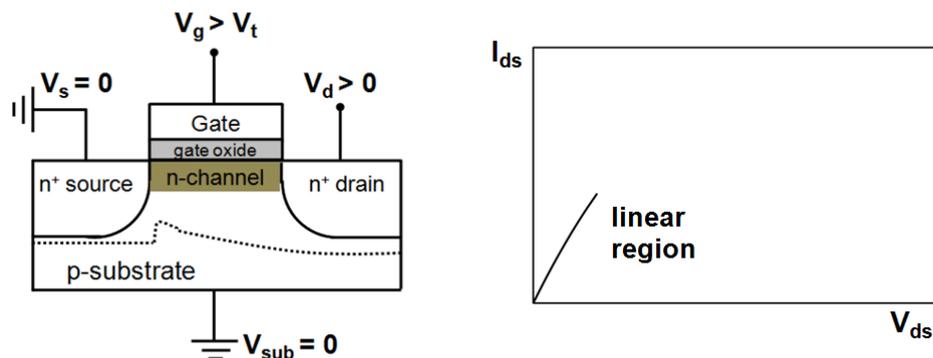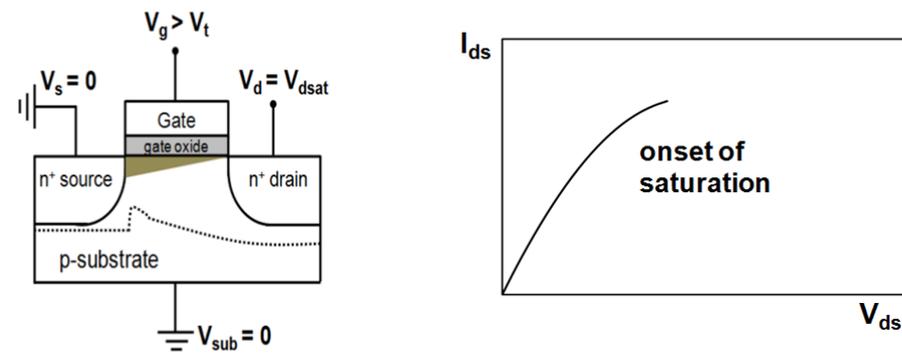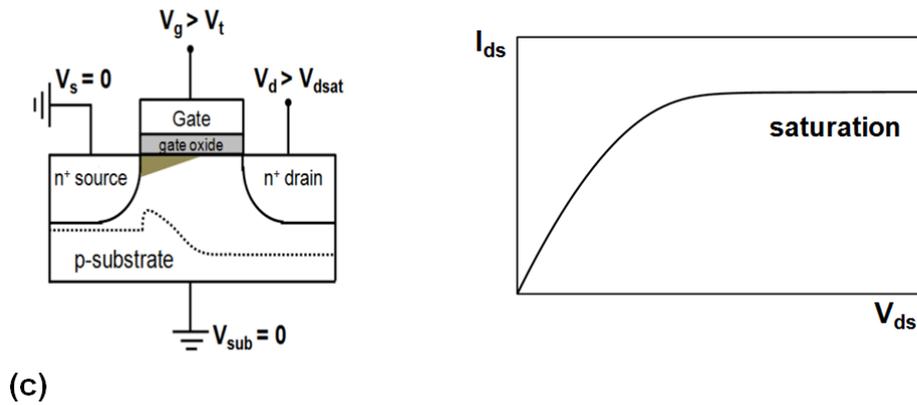
Figure 1.2 Schematic representation of an n-MOSFET in the three regimes of operation: (a) linear region, (b) onset of saturation, and (c) saturation. The dotted line in the cross-sectional view of the MOSFET (left) represents the variation in the depletion region between source, drain and substrate.

Although the region of operation is determined by V_{ds}, the amount of charge in the channel and hence the output current level is determined by V_g. Fig. 1.3 explains the influence of V_g on typical I_{ds}-V_{ds} characteristics of an n-MOSFET. This is the reason that the MOSFET is also referred to as a voltage controlled current source.
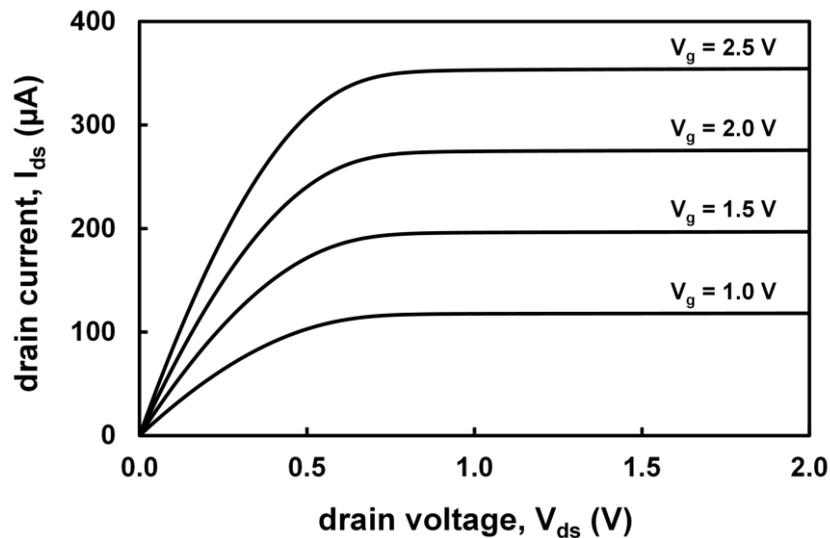
Figure 1.3 Dependence of I_{ds}-V_{ds} characteristics on V_g. Data measured in-house from a bulk-Si channel n-MOSFET with $L_g = W_g = 10$ μm.

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I_{ds} consist of two components: drift current and diffusion current. At $V_g < V_t$, a small value of V_{ds} is capable of resulting in a concentration gradient causing diffusion current which is dominant in the sub-threshold regime. The diffusion current (I_{ds}^{diff}) is a function of the gate overdrive ($V_{gs} - V_t$) and can be described by the following equation [13]:

$$I_{ds}^{diff} \sim exp\left(q\frac{V_g - V_t}{kT}\right),$$

1.1

where, q is the electronic charge, k is the Boltzmann constant and T is temperature.

Under strong inversion, charge concentration in the channel is constant and drift current is caused by the applied electric field. The drift current under strong inversion (I_{dsat}) is written as [13]:

$$I_{dsat} = \frac{W_g}{2L_g}\mu C_{ox}\left(V_g - V_t\right)^2,$$

1.2

where, W_g and L_g are the gate width and length respectively, μ is the carrier mobility and C_{ox} is the capacitance of the gate dielectric. Above V_t and prior to saturation, I_{ds} can be expressed as a function of both V_g and V_{ds} [13]:

$$I_{ds} = \frac{W_g}{L_g}\mu C_{ox}\left[\left(V_g - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right].$$

1.3

In addition to I_{ds}, another important MOSFET parameter is the mobility of charge carriers (μ). It is defined as the drift velocity of charge carriers per unit electric field. It is a measure of the ease with which charge carriers drift through a metal or a semiconductor. It is a vital parameter and is commonly studied to describe device performance. It can be expressed as:

$$\mu = \frac{q\tau}{m^*},$$

1.4

where, τ is the mean relaxation time between scattering events and m^* is the carrier effective mass. The motion of electrons (holes) in a crystal under the influence of externally applied fields and the forces within the crystal lattice can be described as the motion of a free electron but with an effective mass m^* that differs from its mass in the free space (m). It can be expressed as:

$$m^* = \frac{(h/2\pi)^2}{\left(d^2E/dk^2\right)},$$

1.5

where, h is the Planck's constant, E is the kinetic energy of the charge carrier and k is the wave-vector. The quantity $\left(d^2E/dk^2\right)$ represents the energy band curvature. Hence, m^* is inversely proportional to the band curvature.

Different scattering mechanisms in a crystal affect the value of τ and hence of μ in accordance with equation 1.4. In MOSFETs, various scattering mechanisms exist which dominate at different regions of the vertical electric field [14]. These are phonon scattering (lattice vibrations), Coulomb scattering (due to electrically charged interface states) and surface roughness scattering. Fig. 1.4 shows the regions of vertical electric field where each scattering mechanism is dominant [14]. At low fields, Coulomb scattering through interface traps is dominant while at mid fields phonon scattering dominates. Under strong inversion, charge carriers experience maximum interaction with the surface and hence surface roughness scattering is the dominant mobility limiting mechanism at high fields.
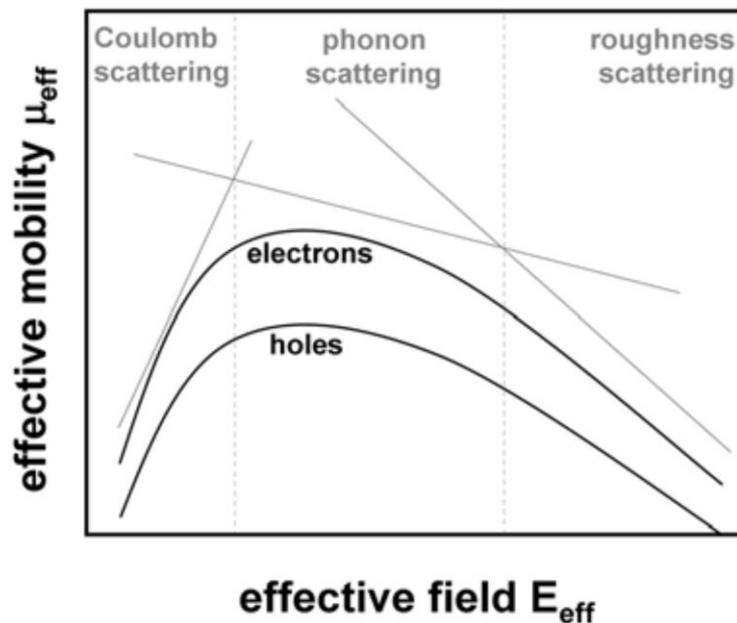
Figure 1.4 Dominant mobility scattering mechanisms with effective vertical electric field [14].

In addition to τ, m^* (usually expressed in terms of its free mass, m) also affects mobility in accordance with equation 1.4. Charge carriers with lower effective mass boost the mobility of the device.

1.1.1 The MOS capacitor

A capacitor is formed when two conducting layers are separated by a dielectric. In a MOSFET, the metal gate electrode, the gate dielectric and the semiconductor substrate form a MOS capacitor as shown in Fig. 1.5.
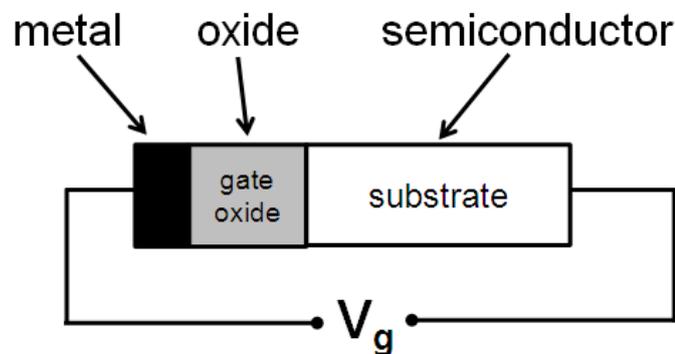
Figure 1.5 Metal-Oxide-Semiconductor (MOS) capacitor formed by the metal gate electrode, gate dielectric and semiconductor substrate in a MOSFET.

The total capacitance of a MOS capacitor (C_{tot}) consists of a series combination of C_{ox} and the capacitance of the depletion layer (C_{dep}) as shown in Fig. 1.6. Under strong accumulation, there is no depletion layer and C_{tot} is only due to the dielectric and hence is equal to C_{ox}. Consequently, C_{ox} is commonly used to estimate the thickness of the dielectric. During depletion and inversion, the total capacitance is due to the dielectric as well as the depletion layer.

The value of V_g which separates accumulation from depletion regime is called the flatband voltage (V_{FB}). The energy band diagrams at accumulation, flatband, depletion and inversion are shown in Fig. 1.7. In order to maintain charge neutrality in the MOS capacitor, the energy band structure is altered under the influence of externally applied V_g. During accumulation, increased hole density at the semiconductor surface causes the bands to bend upwards. When V_{FB} is applied across the gate, the bands are flat which

implies that no charge is present in the semiconductor. Positive V_g increases the density of electrons at the semiconductor surface. This causes the energy bands to bend downwards. This bending of the bands increases further when V_g exceeds V_t, i.e. during inversion (Fig. 1.7).

$$C_{tot} = \frac{C_{ox}C_{dep}}{C_{ox}+C_{dep}}$$
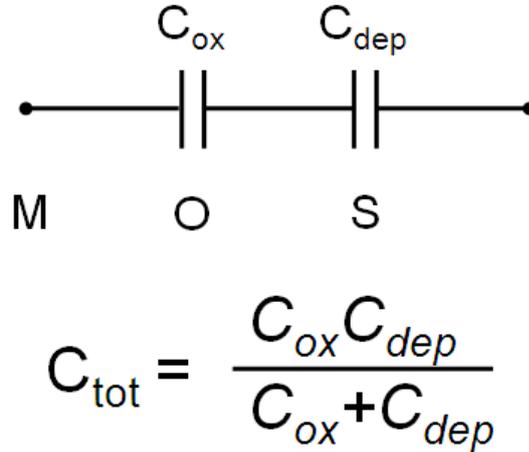
Figure 1.6 Total MOS capacitance (C_{tot}) as a series combination of C_{ox} and C_{dep}.

An ideal MOS capacitor does not have any dielectric charges and workfunction differences between the metal and the semiconductor. Hence the ideal value of V_{FB} is generally assumed as 0 V. If the workfunction difference is not ignored, flatband condition can be realised by applying a voltage at the gate which equals the workfunction difference between the metal and the semiconductor. In this thesis, ideal V_{FB} has been calculated by accounting for the workfunction differences between the metal and the semiconductor. In the presence of charges in the bulk and at the dielectric/semiconductor interface, V_{FB} is altered. In order to account for the potential drop due to the dielectric charges, the value of V_g required to achieve flatband condition is altered. Consequently, variations in V_{FB} are often used to study the polarity and magnitude of charges in the dielectric.

In addition to dielectric charges, the capacitance response of a MOS capacitor can also be used to study useful parameters such as dielectric thickness and substrate doping.
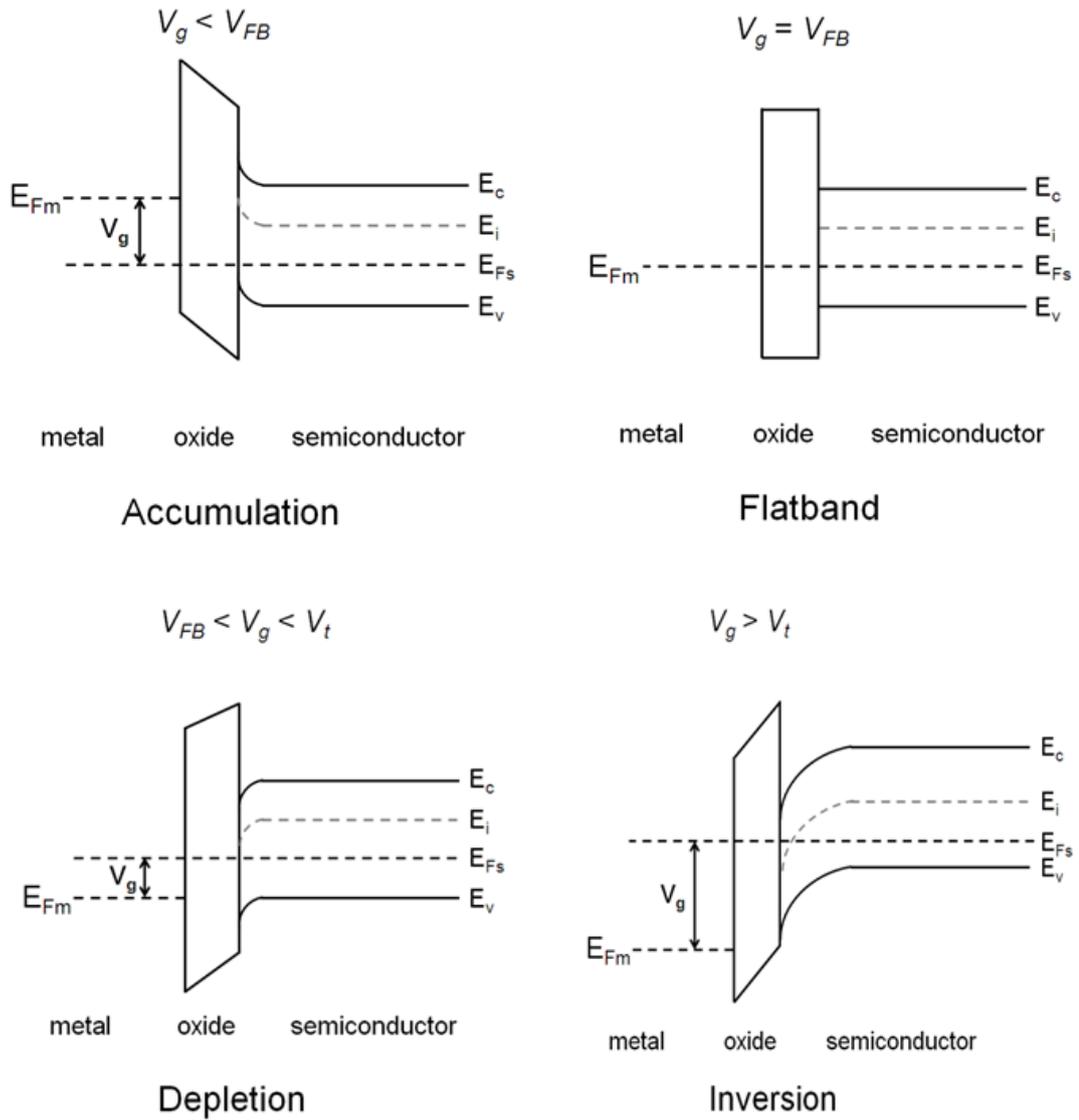
Figure 1.7 Energy band diagrams for an ideal n-MOS capacitor (with no dielectric charges and workfunction differences) during different regimes of operation. E_c and E_v are the conduction and valence bands in the semiconductor, respectively. E_i is the intrinsic Fermi level of the semiconductor, E_{Fs} is the Fermi energy level in the doped semiconductor and E_{Fm} represents the Fermi energy level of the metal.

1.2 CMOS scaling and the need for alternate materials

Over time MOSFETs have been scaled down to smaller devices which has provided more devices and hence more applications per unit area at a smaller cost per device. This deflationary trend has over the years significantly increased the size of the microelectronics industry.

Moore's law has significantly motivated the semiconductor industry towards increased density and improved performance of devices per unit area. A new technology node characterised by a minimum feature size is introduced approximately every two years as shown in Fig. 1.8 [15].
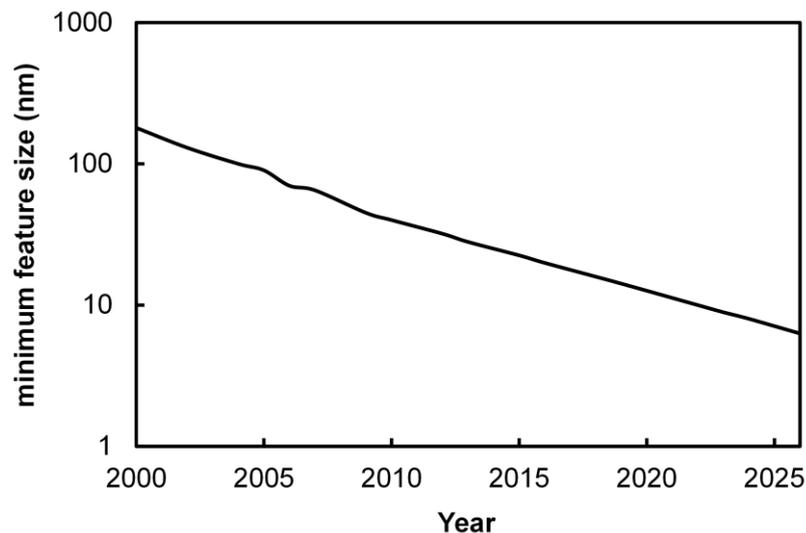
Figure 1.8 The minimum feature size of the technology node along the chronicle time line [15].

1.2.1 Dimensional Scaling of the MOSFET

In order to accommodate twice the number of transistors every two years, MOSFETs have undergone aggressive dimensional scaling. Conventional scaling of MOSFETs over the years has been achieved through reduction of lateral as well as vertical dimensions. The level of reduction in dimensions can be represented by the scaling factor, α. The two common types of scaling are: constant voltage and constant field scaling. Constant voltage scaling requires reduction of lateral dimensions only and does not require supply voltage (V_s) scaling. It is simpler to implement and provides higher

clock speeds (rate at which a processor completes a processing cycle) in integrated circuits. However, continuous reduction of lateral features increases the electric field which can lead to increased gate leakage (J_g), reduced mobility and lower breakdown voltages. Constant field scaling on the other hand maintains the original field distribution and requires scaling of lateral as well as vertical dimensions. It is not a purely geometric process as it also requires scaling of the voltages (V_{ds}, V_g, V_t and V_s). Table 1.1 shows the scaling of various parameters using constant voltage and constant field methods in terms of α [16].

Fig. 1.9 shows the effect of conventional scaling of physical dimensions on the MOSFET device parameters [17, 18].

Table 1.1 Comparison of the effect of constant voltage and constant field scaling on MOSFET device parameters [16]. α is the dimensional scaling factor.

Parameter	Constant voltage scaling	Constant field scaling
Gate length	$1/\alpha$	$1/\alpha$
Gate width	$1/\alpha$	$1/\alpha$
Dielectric thickness	$1/\alpha$	$1/\alpha$
Depletion layer width	$1/\alpha$	$1/\alpha$
Substrate doping	α^2	α^2
Gate capacitance	$1/\alpha$	$1/\alpha$
Dielectric capacitance	α	α
Electric field	α	1
Voltage	1	$1/\alpha$
Current	α	$1/\alpha$
Power dissipation	α	$1/\alpha^2$
Power-delay	$1/\alpha$	$1/\alpha^3$
Circuit delay time	$1/\alpha^2$	$1/\alpha$
Power density	α^3	1
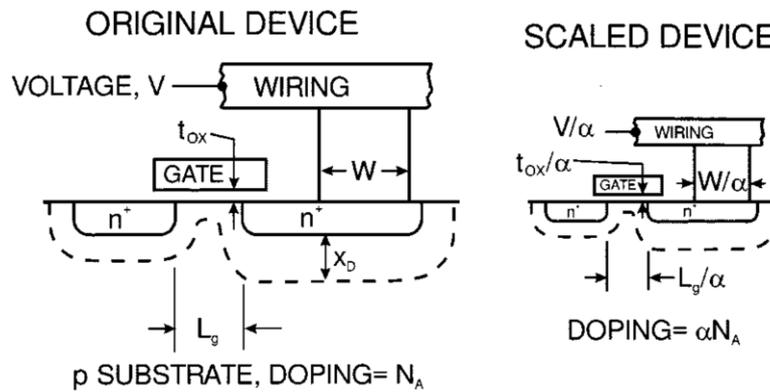
Figure 1.9 Effect of scaling on MOSFET device parameters [17, 18].

1.2.2 Equivalent Scaling

The semiconductor industry has grown immensely by essentially following the Moore's scaling law. As transistor scaling further continues in the 21st century, device dimensions are reaching their physical limits. Several fundamental problems associated with scaled devices are needed to be resolved including variation in J_g (reduced dielectric thickness), V_t control (drain induced barrier lowering and hot electron injection) and mobility degradation (impurity scattering due to high dopant concentration and surface scattering). It is necessary to depart from the classical scaling and introduce novel materials and architectures to maintain performance improvements. Improvement in performance through the introduction of new materials and device architectures in addition to the conventional geometrical scaling is known as 'equivalent scaling'.

Introduction of strain increases mobility without the aggressive scaling of device dimensions. Use of high-κ dielectrics improves performance and also reduces J_g by increasing the equivalent oxide thickness (EOT). Hence, strain and high-κ dielectrics are two of the best examples of equivalent scaling. Equivalent scaling can also be achieved by using other semiconductors such as Ge, SiGe, SiC, Carbon, GaAs and InGaAs. Alternatively, device architectures such as dual channel and multi-gate structures are also effective in improving device performance through equivalent scaling.

1.3 Strained Si/SiGe heterostructures

Strain in semiconductors can be introduced by phonon-induced lattice vibrations, lattice mismatched film growth, externally applied stress and locally introduced stressors [19]. Strain engineering has played a key role in the sub-100 nm technology nodes by improving device performance [20]. Strained Si has been identified by the International Technology Roadmap for Semiconductors (ITRS) in its 2010 update as one of the technological solutions to achieve equivalent scaling in addition to the continued geometrical scaling [21].

Si and Ge have similar diamond like atomic structure with the latter having higher atomic spacing. The lattice mismatch of ~ 4.2% between Si and Ge has been widely exploited to induce strain in the MOSFET channel. Several strain inducing techniques are available which can be divided into global (wafer-level) and local (device-level) techniques. Epitaxial growth of thin films on lattice mismatched relaxed substrates results in biaxial global strain. Uniaxial strain in the direction of the channel can be generated by local stressors embedded in the recessed area of the source and the drain. The biaxial strain arises because the lattice constant of the thin film in the growth plane aligns with that of the substrate which also produces strain in the direction perpendicular to the growth plane. Uniaxial strain exists along one direction (usually along the channel) which is dictated by the local stressors. Fig. 1.10 illustrates the difference between uniaxial and biaxial strain.

Global strain generates much higher levels of strain, while, local strain provides better scalability and is more effective for realising short channel transistors [22]. Fig. 1.11 illustrates the tensile and compressive global strain generated by the heteroepitaxial growth of thin Si and SiGe films on relaxed substrates. The film while trying to match the lattice structure of the underlying substrate undergoes tensile or compressive strain (Fig. 1.11).
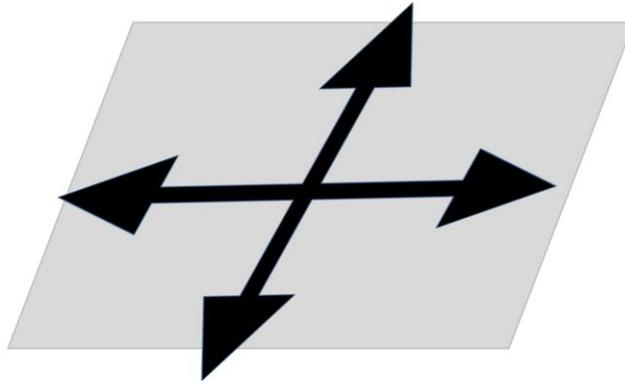
Figure 1.10 Uniaxial and biaxial strain.
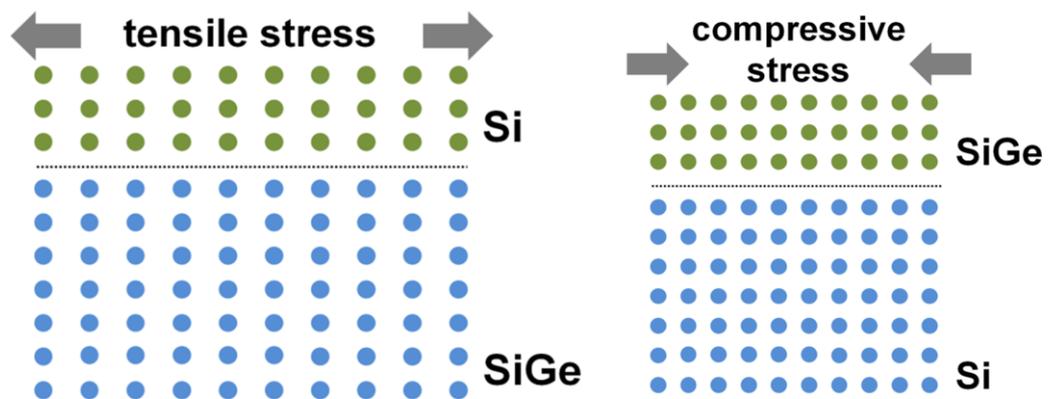
Figure 1.11 Epitaxial growth of Si and SiGe films on relaxed substrates. The Si film is tensile while the SiGe layer undergoes compressive stress.

The most common approaches for inducing local and global strain have been summarised in Fig. 1.12 [22]. Global tensile strained Si or compressively strained Ge channels can be realised by growing them on relaxed Si, $Si_{1-x}Ge_x$ or buried oxide (BOX) as shown in Fig. 1.12a. Local tensile or compressive strain can be introduced in the

channel by using embedded $Si_{1-x}Ge_x$ (compressive) or $Si_{1-y}C_y$ (tensile) stressors in the source/drain (Fig. 1.12b). Alternatively, local strain can also be produced by depositing a contact etch stop layer (CESL) after source, drain and gate silicidation [22, 23]. A CESL acts as a capping layer to prevent contact etching between the metal and the transistor's source, drain and gate regions [24]. Depending on the CESL, local tensile or compressive caps (Fig. 1.12c) can be obtained [22]. Another approach for inducing local strain is the stress memorisation technique [25, 26]. For SMT, the stress is transferred and from the capping layer (such as SiN) to the channel during annealing and subsequent cooling. The capping layer is removed prior to silicidation. The stress induced in the channel by the capping layer remains even after its removal.

In 1992, a research group at Stanford University presented strained Si long channel MOSFETs on compositionally graded $Si_{1-x}Ge_x$ strain relaxed buffers (SRB) which exhibited a nearly 70% improvement in effective mobility (μ_{eff}) over bulk-Si MOSFETs [27]. Prior to this, Manasevit *et al.* in 1982 had reported slightly enhanced electron mobility from $Si/Si_{0.85}Ge_{0.15}$ superlattices grown on Si [28]. In 1984, People *et al.* reported hole mobility from strained $Si_{0.80}Ge_{0.20}$ which was comparable to bulk-Si [29]. In 1985, Abstreiter *et al.* reported that tensile strained Si is able to confine electrons when grown on partially or fully relaxed $Si_{1-x}Ge_x$ alloys [30]. Following these, improvements in electron mobility were reported by few other groups [31, 32]. In spite of such promising observations, defect densities in $Si_{1-x}Ge_x$ were still too high for practical applications. In 1991, realisation of relaxed $Si_{1-x}Ge_x$ SRBs with greatly reduced threading dislocation density [33, 34] led to renewed interest in strained Si. Further improvements in epitaxial growth techniques, especially molecular beam epitaxy (MBE) allowed high quality SiGe SRBs to be realised. Within a year, various groups drastically increased their targets for strain induced carrier mobility. In 1993, enhanced μ_{eff} in strained-Si p-MOSFETs was reported by Nayak *et al.* [35]. In the same year, Xei *et al.* at Bell Labs reported improved μ_{eff} from compressively strained Ge grown on Ge-rich $Si_{1-x}Ge_x$ SRBs [36]. Soon after, improved levels of hole mobility were reported from strained $Si_{1-x}Ge_x$ layers grown on relaxed $Si_{1-y}Ge_y$ (x>y) by Ismail *et. al* [37].
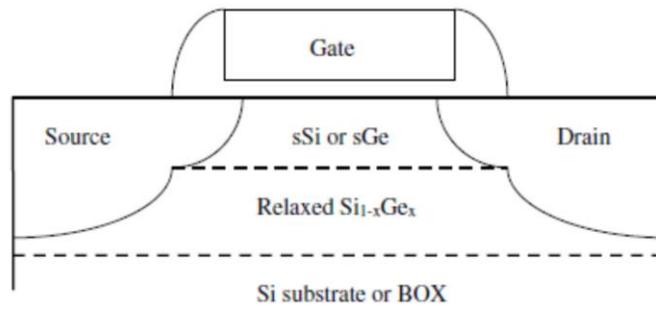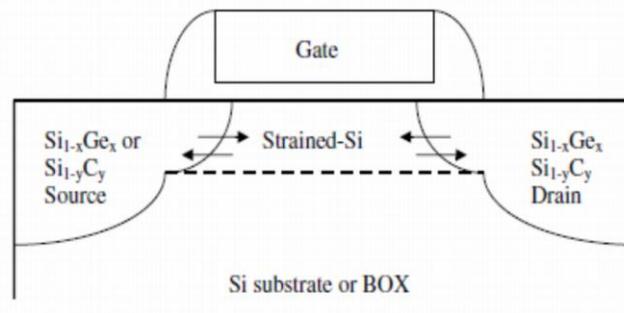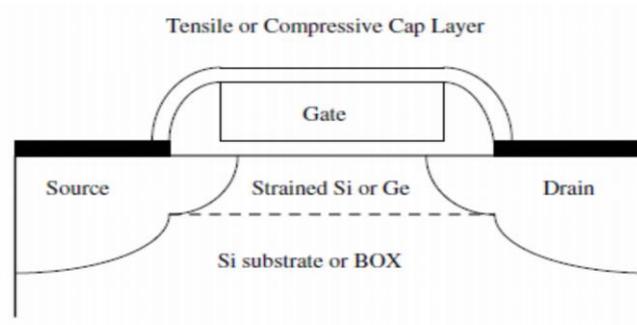
Figure 1.12 Most common strain engineering approaches: (a) global strain, tensile strained Si or compressively strained Ge grown on relaxed Si$_{1-x}$Ge$_x$, (b) local tensile or compressive strain induced by stressors in the source and drain, and (c) local tensile and compressive strain induced in the Si, Ge or Si$_{1-x}$Ge$_x$ channel by a SiN cap layer [22].

1.3.1 High mobility strained Si/SiGe channels

The energy band structures of bulk silicon and germanium are shown in Fig. 1.13 [38, 39]. The conduction band minima for Si lies along the {100} direction (also called the Δ or X direction) while for Ge it lies along the {111} direction (also called the Λ or L direction). The valence band maxima for both Si and Ge occur at a point where two degenerate bands of different curvatures meet, giving rise to "light hole (LH)" and "heavy hole (HH)" bands. In terms of the free electron mass m, the effective hole mass in HH and LH bands for Si are *0.49m* and *0.16m*, respectively [39]. These values for Ge are *0.28m* and *0.044m*, respectively [39]. The conduction band minima of bulk Si and bulk Ge may be represented as constant energy surfaces. These constant energy surfaces are commonly shown as six ellipsoids for Si or eight half-ellipsoids for Ge as shown in Fig. 1.14 [39], representing six and four degenerate valleys for Si and Ge, respectively. The ellipsoids shown in Fig. 1.14 have their long axis directed towards {100} for Si and {111} for Ge. For electrons in Si, the longitudinal effective mass (along the axis) is *1.0m* while the transverse effective mass (perpendicular to the axis) is *0.20m* [39]. The longitudinal and transverse effective electron masses for Ge are *1.6m* and *0.08m* respectively [39].

The energy band structure is altered when Si and $Si_{1-x}Ge_x$ films are strained. Strain shifts and splits the energy bands resulting in lifting of degeneracy of the bands which causes reduced inter-valley scattering. The lifting of degeneracy means that bands with different levels of energy exist.

For Si under the influence of biaxial tensile strain (Fig. 1.12a), the six-fold degeneracy of the conduction band splits into two-fold and four-fold degenerate valleys (Fig. 1.15) [40]. The energy level of the two valleys perpendicular to the growth plane (Δ_2) is lowered with respect to the energy level of the four in-plane valleys (Δ_4) by ~ 67 meV per 10% Ge in the SRB [41]. This causes reduced inter-valley scattering and preferential occupation of electrons in the Δ_2 valleys where they experience lower m^*. This enhances the electron mobility in strained Si n-MOSFETs (equation 1.4). The lowering of the conduction band and the magnitude of strain are a function of Ge content in the underlying SRB. The effect of increasing Ge on the energy band alignment between strained-Si and relaxed $Si_{1-x}Ge_x$ is shown in Fig. 1.16 [20].
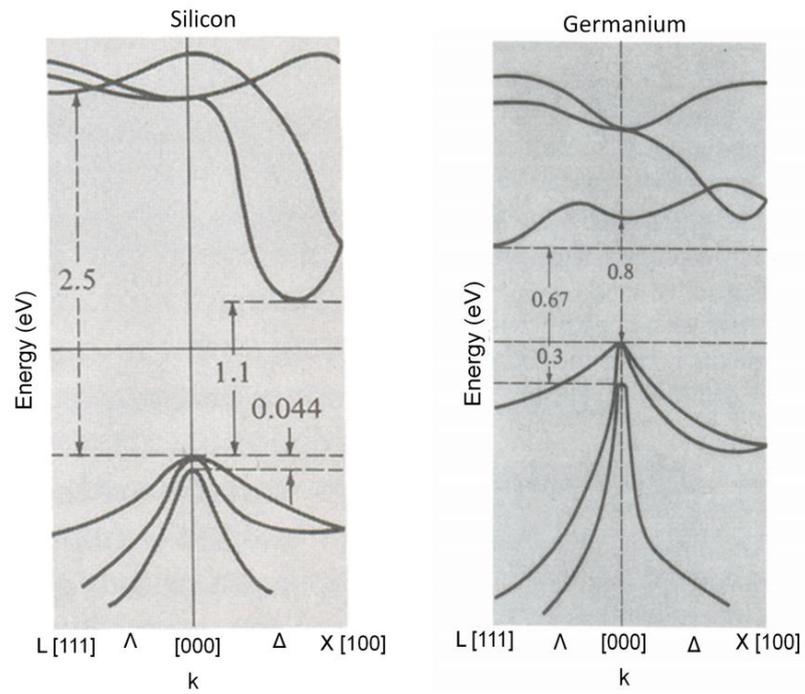
Figure 1.13 Energy bands in Si and Ge showing their respective direct and indirect energy gaps [38, 39].
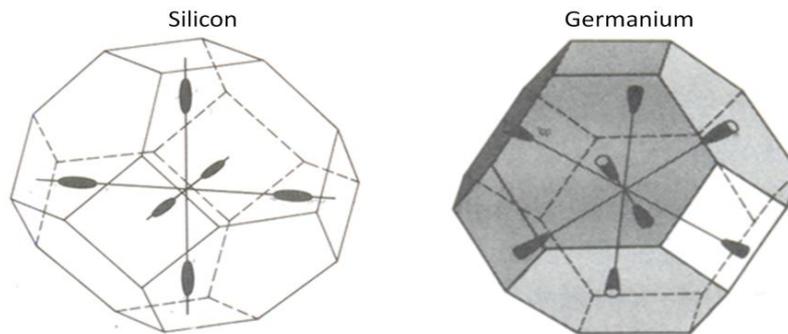
Figure 1.14 Constant-energy surfaces representing the conduction band minima through six ellipsoids for Si and eight half-ellipsoids for Ge [39].
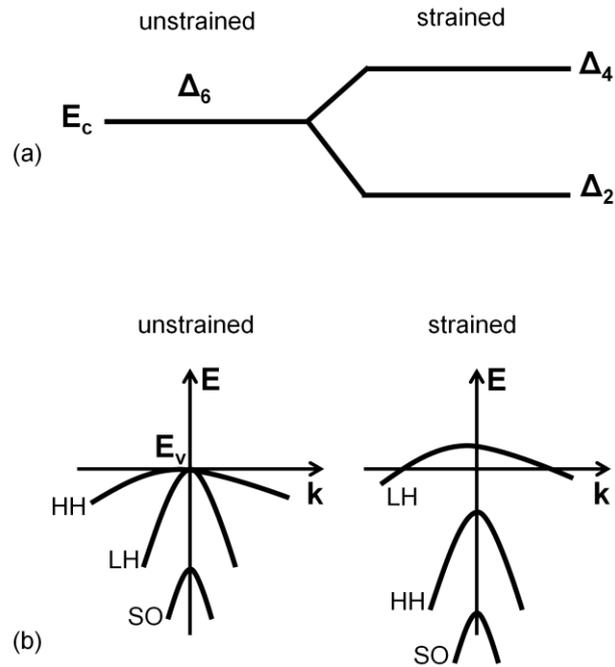
Figure 1.15 Effect of biaxial tensile strain on (a) conduction and (b) valence bands in strained Si [40]. SO signifies the split-off band which measures the spin orbit splitting energy from the valence band maxima.
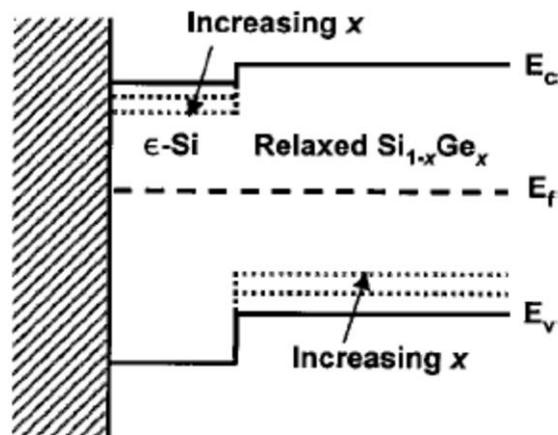
Figure 1.16 Energy band alignments between strained Si and $Si_{1-x}Ge_x$ [20].

Electrical characteristics of strained Si n-MOSFETs have been extensively studied before. Electron mobility as high as 2200-3000 $cm^2V^{-1}s^{-1}$ have been reported in tensile strained-Si channels [42, 43]. Strain induced conduction band lowering also leads to

lower V_t in strained Si devices compared with Si control devices [44, 45]. Additionally, improvements in the on-state drive current [46, 47], J_g [48-50] and short channel effects comparable with bulk-Si channels [51, 52] have also been reported by different groups.

The rate of strain induced valence band splitting in tensile strained Si is lower than in the conduction band [53] and is roughly equal to 40 meV per 10% Ge [54, 55]. This means that for any Ge concentration in the SRB, hole mobility in strained Si MOSFETs is lower than the electron mobility. Hole mobility enhancement is a strong function of Ge content and is drastically lower in p-MOSFETs with Ge content $\leq$ 20% in the underlying $Si_{1-x}Ge_x$ SRB. This is consistent with the observation of μ_{eff} similar to bulk Si, as reported by Mizuno *et. al.* for p-type strained-Si grown on $Si_{0.90}Ge_{0.10}$ [56]. In tensile strained Si p-MOSFETs hole mobility has been found to be a strong function of the gate overdrive [20]. The gate overdrive is the value of V_g in excess of V_t and is mathematically represented as V_g-V_t. High Ge content p-MOSFETs exhibit comparatively higher values of effective electric field (E_{eff}) at which μ_{eff} peaks. Beyond E_{eff} = 0.35-0.5 MV/cm, hole mobility enhancements begin to reduce [57-59]. At $E_{eff} \approx 1$ MVcm^{-1} nearly all improvements in hole mobility are lost [60]. This reduction in hole mobility at high fields in p-MOSFETs is attributed to reduced splitting between the LH and HH bands at high fields due to increased carrier confinement at the strained-Si/SiO$_2$ interface [56]. Increased surface confinement prefers occupation in the HH band [61] while strain prefers occupation in the LH band. This competing effect of strain and surface confinement reduces the hole mobility at high fields in strained Si p-MOSFETs.

Electron mobility in strained-Si n-MOSFETs has been found to saturate at a tensile strain of ~ 0.8%, corresponding to 20% of Ge in the underlying SRB [62]. However, enhancement in hole mobility in p-type strained-Si MOSFETs can be observed for Ge concentration as high as 70%. This difference in hole and electron mobility enhancement is attributed to the lower rate of strain-induced valence band splitting and to the fact that biaxial tension alters the shape of the valence bands, whereas the conduction band shape remains unchanged [53]. These differences in the mobility of electrons and holes in strained-Si pose a problem for CMOS circuits which require complementary devices with identical performance.

In order to compensate for the lower levels of hole mobility in biaxial tensile strained Si, compressively strained SiGe and Ge channels are employed. According to Braunstein, it is known that the energy band structure of $Si_{1-x}Ge_x$ is similar to that of Si as long as the Ge concentration in the alloy is under 85% (i.e. x $\leq$ 0.85) [63]. Strain

induced splitting of the LH-HH bands shifts the LH bands lower on the energy scale. This results in preferential occupation by holes in the low effective mass LH bands, thereby boosting hole mobility (equation 1.4). Fig. 1.17 shows the energy band structure for compressively strained SiGe [64]. For thin SiGe films grown on bulk-Si (which has a lower lattice constant than SiGe) the band offset falls almost entirely in the valence band. Therefore, the SiGe/Si heterojunction can be used to confine holes in a quantum well channel [65]. This hole confinement (defined as the concentration of holes for a given range of energies) increases with Ge content in the SiGe channel [66]. Electrical performance enhancements including high hole mobility and low V_t in devices which employ compressively strained SiGe channels are well documented [67-71]. Hole mobility of the order of 760-1500 $cm^2V^{-1}s^{-1}$ at room temperature has been reported from compressively strained SiGe channel devices [37, 72].
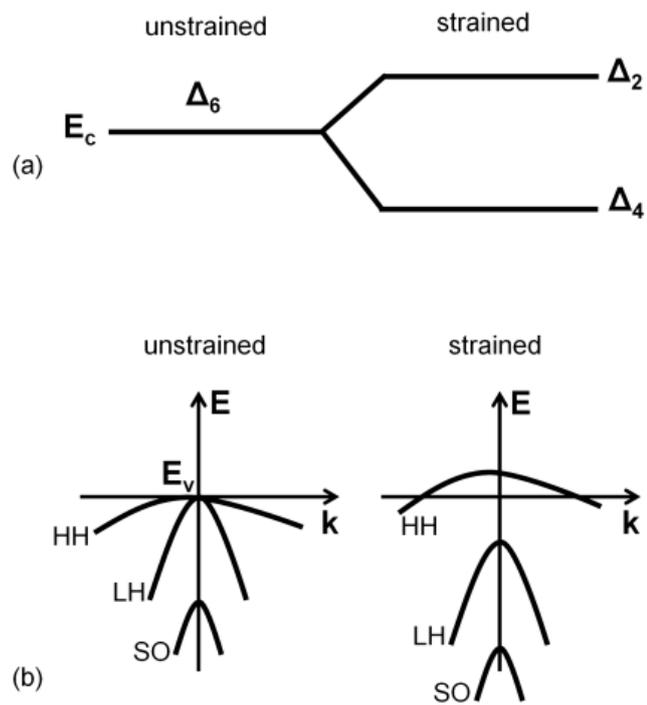
Figure 1.17 Effect of biaxial compressive strain on (a) conduction and (b) valence bands in strained SiGe [64].

Incorporation of strain engineering is primarily aimed at mobility and drive current enhancement. However, it also affects other parameters such as V_t, low frequency noise and gate dielectric quality and reliability. In particular, strain has shown great potential to improve J_g compared with bulk-Si [22, 73]. In experimental studies maximum

improvement in J_g is not achieved. A general understanding that surface roughness and morphology affects strain induced improvements in J_g has only been achieved so far [74, 75]. Hence effect of strain on different parameters is regularly studied in order to maximise potential enhancements.

This thesis presents nanoscale analysis of the quality and reliability of thin gate dielectrics (< 3 nm) in high carrier mobility strained Si/SiGe devices.

1.3.2 Morphology of strained Si/SiGe and other semiconductors

Incorporation of Ge to produce strain requires alterations in device processing. Ge has different material properties than Si and this plays an important role in devices which require SiGe templates. Most of the challenges associated with the use of SiGe/Ge are related to its material quality. SiGe SRBs on Si are of great significance when strained Si devices and integration of III-V materials with Si processes are required. Growth of compositionally graded SiGe SRBs (few microns thick) on Si at high temperature with low levels of threading dislocations has been demonstrated before [76, 77]. Such SRBs are generally grown by MBE or chemical vapour deposition (CVD) and consist of ~ 1 μm thick uniform $Si_{1-x}Ge_x$ cap layer on top of a nearly micron thick compositionally graded layer on Si substrates. These SRBs can be considered as a continuum of low mismatched interfaces. Compositionally graded SRBs relax through a gliding network of misfit dislocations. These misfit dislocations glide towards the surface through threading dislocation arms [78]. Due to the low mismatch between subsequent interfaces, the number of misfit dislocations required for relaxation is low. In-homogenous strain fields associated with misfit dislocations lead to non-uniform growth rates which causes large scale crosshatch surface undulations [76], as shown in Fig. 1.18 [79]. Subsequent growth of epitaxial layers on top of SiGe results in surface propagation of this crosshatch morphology. For SiGe SRBs with crosshatch morphology, surface roughness generally increases with grading rate and final Ge concentration [76]. Due to their final thickness (~ few microns) and high surface roughness (Fig. 1.18), compositionally graded SRBs in this thesis are also referred to as thick or rough SRBs.

Another method of growing SiGe SRBs employs relaxation through dislocation nucleation assisted by point defects [80]. An initial low temperature MBE growth stage causes a high supersaturation of point defects. Relaxation occurs through these point

defects during the second stage of growth which is carried out at a relatively high temperature. The degree of relaxation varies inversely with the temperature of the initial growth stage [80]. Such SRBs are only a few 100's of nm thick and do not exhibit any crosshatch pattern and have surface roughness lower than the rough SRBs as shown in Fig. 1.19 [79]. Hence in this thesis such SRBs are also referred to as thin or smooth SRBs. However, even with reduced roughness, smooth SRBs are rougher than atomically flat bulk-Si substrates.

The surface morphology shown in Fig. 1.18 shows the typical root mean square (rms) roughness values ~ 5 nm in a rough SRB wafer. The amplitude of the crosshatch undulations i.e., the distance between the maximum and minimum surface height ($\Delta_{p\text{-}v}$) can reach 25 nm and the typical distance between consecutive surface peaks (λ_p) is several microns. In contrast, smooth SRBs (Fig. 1.19) exhibit a smoother surface and consistently exhibit rms roughness < 2 nm, with $\Delta_{p\text{-}v}$ < 10 nm and λ_p ~ 400 nm.

Point defects which relax strain in smooth SRBs do not glide like misfit dislocations and are located at their point of origin during subsequent growth and can accumulate to form plane defects. In rough SRBs, misfit dislocations can glide (due to graded growth) to the edge of the wafer where threading dislocation arms may not exist. Consequently, the density of threading dislocations in smooth SRBs can be higher compared with the rough SRBs (see section 2.2.3).
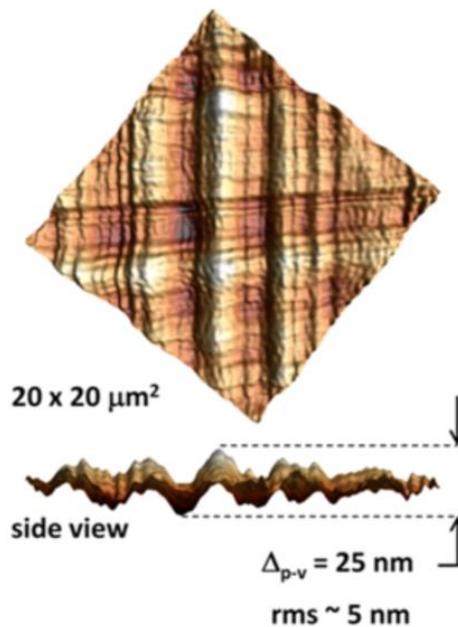
Figure 1.18 Crosshatch surface morphology of a thick (rough) SRB grown by the typical graded composition method [79].

20 x 20 μm²

side view

$\Delta_{p\text{-}v}$ = 9 nm

rms ~ 1 nm
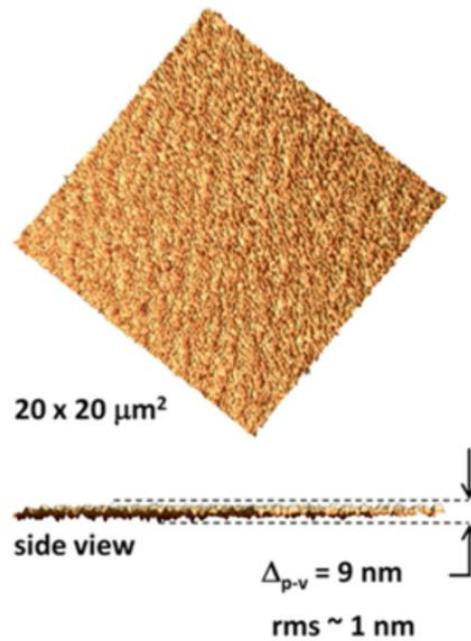
Figure 1.19 Surface morphology of a thin (smooth) SRB grown by the low-temperature method. The roughness is reduced compared with the conventional SRB growth [79].

Similar to relaxed SiGe layers, epitaxially grown strained SiGe thin films can also exhibit varying morphologies and surface roughness depending on strain, layer thickness and processing conditions. Compressively strained SiGe films grown on Si {001} substrates have often exhibited periodic ripples aligned in orthogonal {100} directions parallel to the interface [81] or island-like patterns [82]. Ware *et al.* have demonstrated strain induced surface corrugations and ripples from 10 nm thick fully strained $Si_{0.7}Ge_{0.3}$ layers grown on Si substrates [83]. Increased surface roughness and reduced mobility due to the compressively strained buried SiGe layers in dual and tri channel strained Si/SiGe devices have also been demonstrated [84]. Increase in J_g is also believed to be affected by surface roughness induced by compressively strained SiGe [85].

The morphological quality of strained Si/SiGe films is also affected by the layer thickness. Above a certain critical thickness (h_c), dislocation nucleation is energetically favoured. Strained layers which exceed their h_c experience strain relaxation through a network of misfit dislocations. Due to the 4.2% lattice mismatch between Si and Ge, h_c reduces with increasing Ge content. This inverse dependence of h_c on Ge content has been extensively studied before [86-91] and is shown in Fig. 1.20. Consequently the

level of strain (and hence mobility) is dependent on the thickness of the strained SiGe channel. If the critical thickness of epitaxial SiGe layers is exceeded, small to large scale undulations appear on the surface depending on the final layer thickness [92].
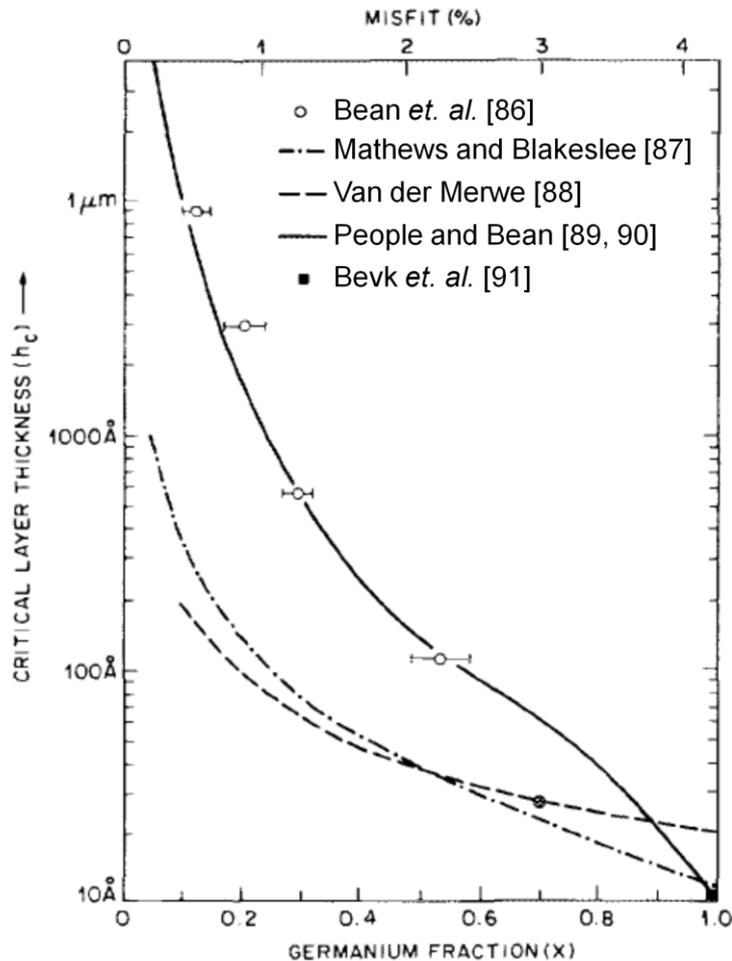
Figure 1.20 Critical thicknesses (h_c) for strained Si$_{1-x}$Ge$_x$ layers grown on Si, as a function of Ge content, as reported by Bean *et al.* [86] (open circles with error bars), Mathews and Blakeslee [87] (dot-dashed line), Van der Merwe [88] (dashed line), People and Bean [89, 90] (solid line) and Bevk *et al.* [91] (solid square).

There are different levels of surface roughness associated with SiGe epitaxy. These can be identified as:

    a. *Macro-roughness or large scale undulations*, which results from misfit dislocation driven strain relaxation. Crosshatch morphology is a result of

large scale surface roughening. λ_p is of the order of few microns (e.g., Fig. 1.18).

b. *Micro-roughness or mid-scale undulations*, which results due to strain relaxation mechanisms in strained films. Partial relaxation of strain energy through re-arrangement of surface mass results in surface perturbations such as ripples and islands. λ_p is of the order of few 100's of nm.

c. *Nanoroughness or atomic scale undulations*, related to the topography of the top-most atomic layer. Nanoroughness may also be a secondary effect of large scale crosshatch roughness with steep slopes being prone to developing higher levels of nanoroughness. λ_p is of the order of few 10's of nm.

In addition to strained Si/SiGe, heteroepitaxial strained III-V semiconductors such as GaAs, GaAsP and InGaAs also exhibit crosshatched surface morphology [93-96]. The impact of surface morphology on electrical performance in strained Si/SiGe devices is also likely to be extended to these other heterostructures.

1.4 Gate dielectrics on strained Si/SiGe

Introduction of dielectrics on new materials can be a challenging task as electrical performance and reliability can vary. Gate dielectric performance in strained Si/SiGe devices is generally different compared with bulk-Si devices.

1.4.1 Scaled dielectrics

The gate dielectric is a critical layer in a MOSFET as it confines charge carriers in the channel. Thermally grown SiO_2 has excellent thickness uniformity and thermal stability. However, in order to avoid short channel effects, SiO_2 has been scaled down to a thickness < 1 nm. This thickness is lower than the 3 nm limit for direct tunnelling to occur [97]. For such ultra-thin gate dielectrics, J_g increases manifold and this affects power consumption and heat dissipation. One of the major constraints to scaling is the level of tunnelling currents through the gate dielectric. Gate leakage constitutes 40-50% of all power consumed in the 65 nm generation, and this figure grows to 60-70% for devices processed under the 45 nm node [98]. Large levels of J_g can also affect the

accuracy of some characterisation techniques. For example, low frequency capacitance-voltage (*C-V*) measurements are severely affected by leakage currents [97].

Strain engineering can assist aggressive CMOS scaling by increasing carrier mobility and drive current.

1.4.2 Incorporation of high-κ dielectrics in strained devices

High quality gate dielectrics are paramount if MOSFETs with high performance and reliability are to be realised. There is a growing need for alternate dielectric materials. However, replacement of SiO_2 with another dielectric increases process complexity. SiO_2 is the native oxide of Si which can be grown by thermal oxidation of Si and has been the traditional material choice for the gate dielectric. In spite of the improvements in J_g and increased scope for scalability, the interface and bulk charge densities are usually higher in high-κ dielectrics than in SiO_2. High-κ dielectrics such as HfO_2 can result in the formation of interfacial silicates and oxides which degrade the gate stack quality by increasing trapped charges [99, 100]. Furthermore, beyond a certain post deposition annealing temperature serious crystallisation of high-κ dielectrics can lead to an increase in J_g [101].

Strained SiGe devices generally use high-κ dielectrics and incorporate a thin Si cap between the dielectric and the substrate to improve the interface quality. However, this Si cap which is usually very thin can get partially or completely consumed during oxidation. The thickness of the Si cap can be increased to compensate for consumption during oxidation. However, a thick Si cap is capable of behaving as a parasitic channel especially at high fields [102]. A thin Si cap may not be able to mitigate the effect of interface roughness. Consequently, the thickness of the Si cap has been optimised for strained SiGe devices and is generally < 5 nm. For poly-Si/high-κ gate stacks another significant problem is that of Fermi-level pinning [103] which results in high values of V_t. This is unsuitable for high performance and low power applications which require high gate overdrive. In order to have more control over V_t, metal/high-κ gate stacks have been implemented. However, metal electrodes can affect the gate dielectric reliability through diffusion and intermixing with the dielectric [103].

1.4.3 Dielectric quality and reliability in strained Si/SiGe devices

Theoretically, strain induced alterations in the band structure and carrier effective mass in the dielectric are expected to reduce J_g [22, 73]. In practice however, different trends in J_g with strain have been reported. According to [22], both improvement and degradation in J_g with strain can be expected depending on the nature of strain and charge carriers considered. Gate current increases for p-channel and reduces for n-channel Si transistors under uniaxial tensile stress [104]. For strained Si n-MOSFETs, J_g increases at lower fields and reduces at higher fields compared with unstrained devices [74]. Hole tunnelling current in p-MOSFETs was found to reduce for uniaxial and biaxial compressive stress while it increased for biaxial tensile strain [105]. According to Hsieh *et al.*, variation in J_g with strain can be used to estimate the level of strain [106].

Bulk and interface trapped charges are often higher in strained devices compared with their unstrained counterparts [75, 107, 108]. This can lead to increased trap assisted tunnelling at low fields [74]. Different factors including, increased out-diffused Ge [109], threading dislocations reaching the channel [110] and surface roughness [111, 112] are believed to contribute to increased dielectric charges in strained Si/SiGe devices. Significant analysis of strained materials and devices in the past has focussed on device-level performance, effect of Ge, chemical interactions, bonding and interface quality. However, the impact of morphological fluctuations on gate dielectric performance is not well understood.

1.4.4 Surface morphology and dielectric performance on strained Si/SiGe and other semiconductors

Bulk-Si is atomically flat, however strained Si/SiGe layers can exhibit a wide variety of morphological features such as ripples, islands, and small to large scale undulations (section 1.3.2).

Deterioration of surface morphology is known to impact electrical performance and reliability characteristics in bulk-Si devices. J_g, time to breakdown and charge to breakdown are significantly degraded with an increase in surface roughness of bulk-Si channels [113-116]. Surface roughness scattering is also the dominant mobility limiting mechanism at high electric fields (Fig. 1.4).

For strained Si MOSFETs, nanoroughness associated with the top-most atomic layer and micro corrugations on the surface can affect the flow of charge carriers, thereby reducing mobility [117]. Sugii *et al.* have demonstrated improved performance from strained Si MOSFETs fabricated on chemical-mechanical polished SiGe SRBs [118]. Degraded device and dielectric performance from strained Si channels grown on rough SRBs with crosshatch morphology has been reported before [75, 111, 119, 120]. The dominating lengths of the various types of roughness are significantly greater than those in bulk Si, ranging from several tens of nm to μm (section 1.3.2). Consequently, there is little understanding why such large scale roughness appears to play such an important role in dielectric properties.

Recently it has been shown that thermally grown SiO_2 on 3C-SiC and 4H-SiC exhibits preferential breakdown in the vicinity of step-bunching edges due to local concentration of electric field in these regions [121, 122]. According to Jung *et al.*, addition of Zr to HfO_2 dielectric can improve reliability characteristics due to morphological improvements in fully crystallised ZrO_2 compared with HfO_2 [123]. Grain boundaries associated with the surface of rare earth oxides such as Gd_2O_3 and Y_2O_3 enhance J_g in poly-Si gate devices employing such dielectrics [124]. Incorporation of an interstitial SiO_2 layer between HfO_2 and Si-substrate improves electrical performance by improving surface morphology [125].

In summary, it is evident that surface roughness and morphology of semiconductor channels affects dielectric performance and reliability. To ensure that the performance of gate dielectrics on various emerging substrate and channel materials is not compromised, design and process parameters require optimisation. This requires a good understanding of the influence of localised morphological features on dielectric performance and reliability.

In this thesis, the morphological influence of the underlying strained Si/SiGe layers on nanoscale dielectric performance and reliability has been studied. During processing, the substrate surface morphology can be modified. Therefore, techniques have been developed to characterise devices on a nanoscale. To validate the techniques, nanoscale results have been compared with macroscopic data and trends from the same devices. The methods developed are suitable for a wide range of semiconductor material systems, as well as other advanced technologies.

1.5 Metrology challenges for emerging materials and devices

Conventionally devices have been studied using macroscopic techniques where conductive probes characterise the devices through large metal contact pads. Such techniques have been extensively developed over time and have provided reliable results. However, the trends provided by such device level techniques are indicative of the entire area under study. Such techniques cannot determine the localised electrical signatures and thus performance from different regions. In order to obtain localised behaviour, it is necessary that analysis be performed directly at the region of interest. This requires characterisation techniques which can probe directly at the nanoscale. Optimisation of design and growth parameters is not possible until it is known how specific material properties affect electrical performance.

The rapid introduction of new materials, reduced feature size and new device structures continues to challenge reliable and successful characterisation of materials and devices. Metrology methods must routinely measure near and at atomic scale dimensions which requires a thorough understanding of nanoscale materials and of the physics involved in making the measurement [15]. New materials add to the complexity of measurements. Efficient metrology techniques can reduce the cost of manufacturing and time-to-market for new devices. Consequently, it may not be possible to characterise novel materials and device structures by existing conventional measurement techniques. There is a growing emphasis that active areas on fully processed devices be measured instead of test structures.

1.5.1 Strained Si/SiGe and need for novel metrology techniques

Gate dielectric metrology becomes even more complex when strained Si and Ge channel structures are used as the starting material instead of bulk Si or silicon on insulator (SOI) wafers. According to the ITRS 2011 report [15], irrespective of how strained Si is grown, its metrology is crucial with a large numbers of parameters to be controlled: 1) thickness and Ge profile of the SiGe SRB, 2) thickness of the strained Si channel, 3) roughness of the Si/SiGe interface and the Si surface, 4) magnitude and local variation of stress in the Si channel, 5) threading dislocation density in the Si channel, 6) density of other defects, such as twins, dislocation pile-ups, or misfit dislocations, particularly at the SiGe/Si channel interface, and 7) distribution of dopants in channel and SRB (particularly after thermal annealing).

Usually microscopy imaging is the first step in the "being able to see it, measure it, and control it" chain [15]. There is a need for characterising the structure and local properties of current CMOS devices as they scale down in size, as well as for anticipating the metrology requirements of post CMOS device technologies. High resolution microscopy techniques which are capable of measuring at the nanoscale are expected to play a vital role in meeting future metrology challenges associated with emerging materials and devices.

1.5.2 Scanning probe microscopy

Scanning probe microscopy (SPM) is the name given to the family of techniques where a sharp tip scans across the surface of interest to obtain two or three dimensional images of the surface. Such techniques are generally non-destructive and have a high lateral and vertical resolution. The scanning tunnelling microscope (STM) invented in 1982 [126] was the original application of SPM. In STM, a very sharp conductive tip scans across the surface of the sample. Although it can image at atomic resolution its use is only limited to conductive samples.

In 1986, the atomic force microscope (AFM) which is capable of imaging the surfaces of insulating layers was introduced by Binnig *et al.* [127]. Over the years, the AFM has developed into a highly useful instrument capable of providing important insights in the fields of surface science, electrochemistry, biology and semiconductors. The AFM operates by measuring the force between the probe and the sample. This force depends on the material properties, distance between the probe and the sample, probe geometry, and surface contamination.

The schematic representation of the AFM setup is shown in Fig. 1.21. A sharp probe tip is mounted at the end of a cantilever. As the distance between the atoms at the tip and the atoms on the surface of the sample becomes shorter, these atoms interact with each other. When the distance between the tip and the surface atoms is very short, the interactive force is repulsive in nature due to electrostatic repulsion. When the distance gets relatively longer, the interactive force becomes attractive due to the long range van der Waals forces. Conventional AFMs use a piezo tube scanner below the sample which is responsible for movement in all the three directions. This results in a non-orthogonal relationship between the three axes which causes cross talk and non-linearity. The XE-150 AFM from Park systems used for analysis in this thesis has two separate scanners,

x-y scanner which scans the surface in two-dimensional space and z-scanner which moves the tip in the z direction. The information detected by the two independent scanners is processed by the AFM controllers to obtain the 3-D topography image.
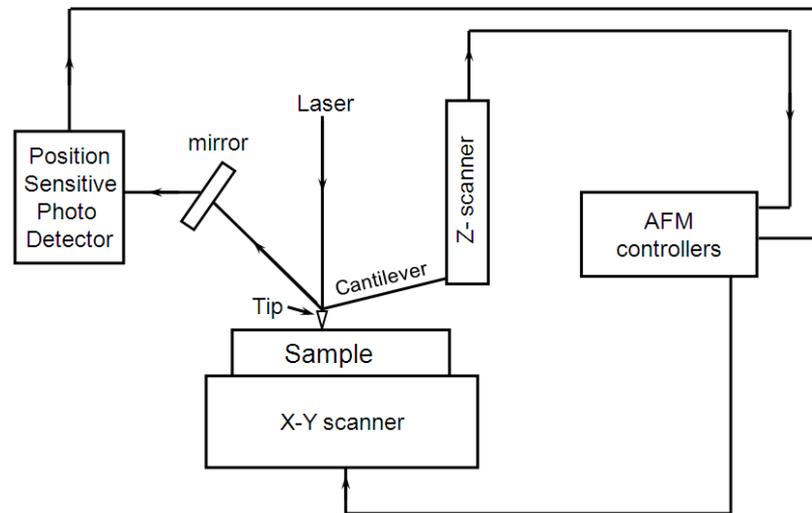
Figure 1.21 Schematic representation of the AFM measurement setup.

The AFM can be operated in different modes which are:

a. *Contact mode*. The probe tip is in soft contact with the surface during the entire duration of the scan. The repulsive force between the sample and the probe tip is utilised to study the topography. The spring constant of the cantilever is sufficiently small to allow it to react to minute force changes of the order of few nN. The interaction between the inter-atomic forces can bend or deflect the cantilever depending on the curvature of the region under study. This deflection of the cantilever deflects the laser from the back of the cantilever which is then steered through a set of mirrors on to a position sensitive photo detector (PSPD), as shown in Fig. 1.21. The cantilever deflection (which varies with surface topography) is quantified by the position of the deflected laser on the PSPD. This enables the control system to generate a map of the surface topography. The PSPD forms a feedback loop which controls the vertical movement of the scanner as the cantilever moves across the surface. The contact mode of measurement is commonly used for hard surfaces which do not get deformed by the AFM probe tip.

b. *Non-contact mode.* The attractive van der Waals forces are utilised while recording the topography in non-contact mode. Due to the weak attractive forces the deflection or bending of the cantilever cannot be measured directly. The tip is given a small oscillation and ac detection methods are used to detect the weak forces between the tip and the sample surface. The changes in the phase or vibration amplitude of the cantilever due to weak attractive forces are detected. A non-contact cantilever has a resonant frequency (f_0) between 100 kHz and 400 kHz and vibration amplitude of a few nanometres. Due to the tip-sample attractive force, a cantilever vibration at its resonant frequency near the sample surface causes its spring constant to change. The resulting effective spring constant (k_{eff}) is related to the intrinsic spring constant (k_o) by the following expression:

$$k_{eff} = k_o - F',$$ **1.6**

where, $F' = \left(\frac{\partial F}{\partial}\right)$ is the force gradient and is positive. The value of k_{eff} becomes smaller with increasing interaction (i.e., reducing distance) between the tip and the sample. The resonant frequency of the cantilever also shifts (from f_0 to f_{eff}, as shown in Fig. 1.22) during atomic interactions in accordance with:

$$f_0 = \sqrt{\frac{k_o}{m_{cantilever}}},$$ **1.7**

where, $m_{cantilever}$ is the mass of the cantilever.

The cantilever is vibrated at a frequency, f_1 (slightly higher than f_0) where a steep slope is observed in the graph of frequency vs. amplitude (Fig. 1.22). This results in a large change in amplitude (ΔA) even if the change in the resonant frequency (due to atomic attractions) is very small. This change in amplitude reflects the change in the distance between the tip and the sample (due to surface topography) during imaging. The change in resonant frequency or ΔA is measured and a non-contact feedback loop is established which compensates the changes in the tip-sample distance during scanning. By maintaining constant amplitude (A_0) and tip-sample distance, non-contact mode can record the surface topography of the sample without requiring physical contact with the sample

surface. Non-contact mode is highly suitable for soft biological samples which can get easily modified or damaged by the probe tip.

c. *Tapping mode*. The probe tip makes intermittent contact with the sample thereby providing high resolution without dragging the tip across the surface. As the oscillating tip touches the surface the amplitude of oscillation changes and this change is monitored to measure the surface features. Tapping mode works well for soft, adhesive, or fragile samples which can get easily damaged. The XE-150 AFM from Park systems refers to the tapping mode by dynamic force microscopy.
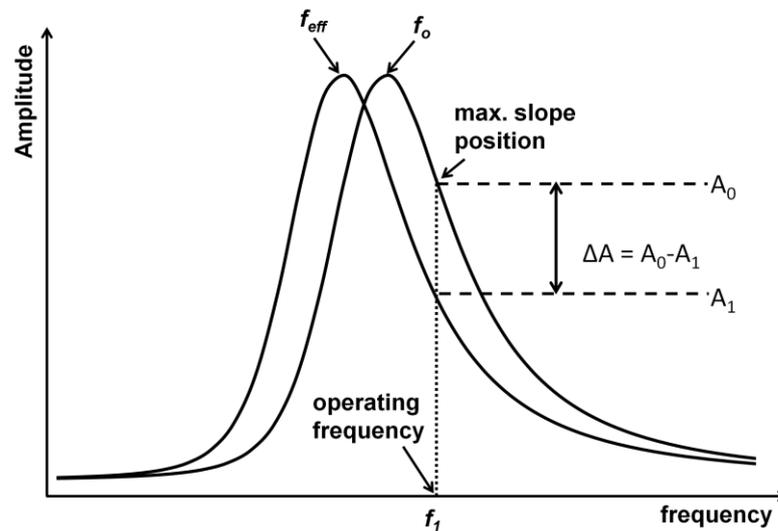
Figure 1.22 Shift in the non-contact AFM tip resonance curve due to variations in surface morphology.

The AFM has now become a standard technique when morphological assessments are required. Vertical resolution of 1 Å and lateral resolution of ~ 5 nm can be routinely obtained [128]. Possibility of non-destructive high resolution imaging has made the AFM an attractive option for 'in-line' surface roughness and defect density monitoring [129]. The AFM has found applications at various stages of semiconductor device fabrication, from the Czochralski-grown bulk silicon [130] to the investigation of surface roughness on polished [131], etched [132], oxidised [116] and metallised [133] surfaces. The AFM can also be used to monitor the development of new etch resists [134] and to monitor the growth of epitaxial layers [135]. It can also be used to

investigate sub-surface structures by cleaving a semiconductor wafer and analysing the cleaved surface [136].

1.5.3 Electrical SPM techniques

SPM techniques are an important tool for characterizing at the nanoscale and find their primary application in recording topography. However, when combined with additional electrical setup these techniques can provide vital insight into the localized electrical phenomenon in semiconductor devices which are getting scaled continuously. In addition to scaled devices, electrical SPM techniques find application in characterizing new dielectrics other than SiO_2 as such dielectrics are usually associated with distinct morphologies which may affect electrical performance. Understanding of localized topographical features is paramount if acceptable leakage, lifetime and reliability are to be realized. Owing to its high spatial resolution, AFM coupled with additional electrical setup has been used for analyzing different dielectric related parameters including nanoscale J_g [137, 138], post breakdown behaviour [139, 140], dielectric thickness [141], and dielectric/semiconductor interface quality [142, 143].

In this work, two electrical variants of AFM based SPM techniques: C-AFM and SCM have been used. An in-depth analysis of the gate dielectric and its interface with the underlying semiconductor has been carried out. The detailed working of C-AFM and SCM measurement setups is explained in sections 2.5.1 and 3.3.1 respectively.

1.6 Other characterisation techniques

In addition to AFM based characterisation, other techniques have also been used in this work to study material and electrical properties of dielectrics and strained layers. These are now discussed.

1.6.1 Raman spectroscopy

Raman spectroscopy is based on the Raman effect first reported in 1928 [144]. According to this effect, when light particles or photons are scattered from the surface of a sample, a very small portion (few parts per million) of these photons exhibit a change from the incident wavelength and holds the information about different material

properties. This weak inelastic scattering is also known as Raman scattering. The shift in energy level (due to inelastic Raman scattering) is usually referred to as Raman shift or wavenumber shift. This shift is sensitive to material properties like chemical composition, crystal orientation, crystallinity and strain.

Strain in Si/SiGe heterostructures has been extensively studied using Raman spectroscopy [145-148]. Fig. 1.23 compares the Si-Si lattice vibrations from bulk Si, poly-Si, tensile strained Si on a $Si_{0.8}Ge_{0.2}$ SRB and compressively strained $Si_{0.5}Ge_{0.5}$ on bulk Si. It can be seen that the Raman spectra of poly-Si and strained Si are different from that of single crystal bulk-Si in terms of wavenumber shift and width.
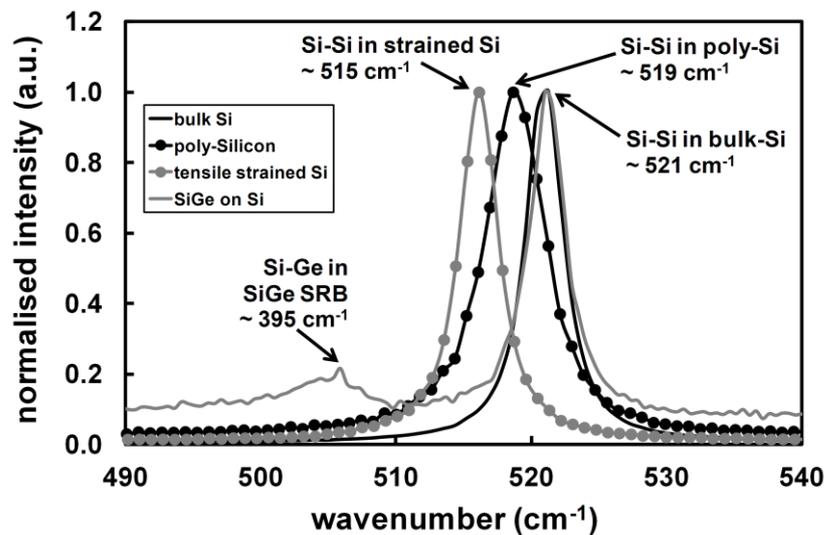
Figure 1.23 Raman spectra showing the Si-Si vibrations in bulk Si, poly-Si, tensile strained Si and compressively strained SiGe.

1.6.2 Scanning electron microscopy (SEM) and energy-dispersive x-ray spectroscopy (EDX)

SEM is a high resolution imaging technique in which a focussed electron beam incident on the sample reveals information about topography, chemical composition and crystalline structure. Scattering of incident electrons may be inelastic (resulting in secondary electrons) or elastic (resulting in back-scattered electrons). Secondary electrons form the conventional SEM image revealing information about topography. Back-scattered electrons are useful for obtaining contrasting images of multi-layered structures. Additionally, SEM analysis also produces X-rays (which may be used for

elemental analysis), cathodoluminescence and heat. SEM is generally non-destructive, however, cross-sectional analysis of multi-layered structures may render the sample unusable after cleaving. Insulating samples may charge during SEM imaging causing image artefacts. To avoid this, insulating samples are generally coated with electrically conductive materials such as gold. Although SEM imaging can be repeatedly carried out, conductive coating may not allow further surface characterisation using other techniques.

EDX is usually attached to the SEM equipment to allow for elemental composition analysis. The incident electron beam scatters a lower shell electron which is filled by a higher shell electron by losing energy. This energy is released in the form of x-rays and is characteristic of the atom which produced it. Consequently, these x-rays are analysed to extract information about the elemental composition.

Physical and chemical characterisation of strained Si/SiGe layers using electron based spectroscopy techniques such as SEM and EDX has been carried out previously [149-151].

1.6.3 X-ray diffraction (XRD)

XRD is a non-destructive and non-contact characterisation technique commonly used to study the atomic structure of crystalline solids. A monochromatic x-ray beam is irradiated on the sample at an angle ω (or θ) and diffracted x-rays are recorded by a detector which is placed at an angle 2θ with respect to the incident beam. Hence XRD spectra are also referred to as ω-2θ curves. Conditions for constructive interference of scattered x-rays (diffraction) to occur are given by Bragg's law and can be expressed by the following equation [97]:

$$n\lambda = 2d \sin\theta \qquad\qquad \textbf{1.8}$$

where, n is an integer, λ is the incident wavelength and d is the lattice constant of the crystalline solid. Usually, first order diffraction ($n = 1$) is studied. As θ is increased to a value at which $\lambda = 2d\sin\theta$, a diffraction peak appears. The angular position of this diffraction peak is sensitive to the lattice constant, d (i.e. crystal structure).

Different XRD curves are commonly reported depending on the intended requirement. These are rocking curves (X-ray intensity *vs. ω*), detector scans (X-ray intensity *vs. 2θ*, at a constant ω) and coupled scans (X-ray intensity *vs. 2θ*, but ω also

changes such that ω=θ). A coupled scan is obtained to determine the Bragg angle, θ when lattice mismatch, strain and relaxation are required to be evaluated. XRD has been widely used to study strained Si/SiGe layers in order to determine alloy concentration, strain and degree of relaxation [92, 152-154].

1.6.4 X-ray reflectivity (XRR)

XRR is another non-destructive and non-contact characterisation technique which uses X–rays. It is commonly used for assessing density, thickness and roughness of thin films. Unlike XRD, XRR can be applied to crystalline as well as amorphous solids. XRR involves monitoring of reflected X-rays from the sample at grazing angles. Below a certain incident angle, called critical angle (θ_c) total reflection occurs as x-rays are not able to penetrate the surface. For most materials, the value of θ_c is less than 0.3°. In accordance with Fresnel's laws of reflectivity, the reflected intensity reduces rapidly with increasing incidence angle. Above θ_c, X-rays penetrate through the surface and reflected x-rays from different interfaces interfere resulting in interference fringes in the reflective pattern. Film density is sensitive to θ_c while the angular spacing between the consecutive interference fringes is a measure of film thickness. Consequently, interference fringes are commonly referred to as thickness fringes in the XRR spectra. Thicker films are usually difficult to measure with XRR as thickness fringes are not well defined for such films. There is usually an upper limit of 0.4-0.5 μm on the thickness which can be measured by XRR.

Another important parameter measured by XRR is the surface roughness. A rougher surface increases diffuse reflection and reduces specular (mirror like) reflection. This causes increased interference from reflected rays and consequently, thickness fringes are not well modulated. The slope of the XRR spectra after θ_c is exceeded is a measure of surface and interface roughness. It is usual not to observe any thickness fringes from films with a surface roughness of more than 2 nm and hence a nearly constant slope is observed for higher values of roughness. Additionally, rougher films make thickness characterisation difficult due to the lack of well-defined thickness fringes.

Thin epitaxial films such as strained Si/SiGe have been regularly characterised using XRR analysis [154-157].

1.6.5 Macroscopic electrical analysis

In order to compare nanoscale observations with device-level data, macroscopic electrical analysis has also been carried out. Device-level variation in current (*I*) and capacitance (*C*) with applied voltage (*V*) i.e., *I-V* and *C-V* analysis has been carried out using the parameter and impedance analysers. Details of macroscopic measurements have been included in relevant sections.

1.7 Thesis outline

The aim of this thesis is to analyse the impact of substrate induced surface morphology on the electrical behaviour of overlying gate dielectrics at the nanoscale. Localised spatial variations in J_g, breakdown behaviour, thickness and interface trapped charge for thin dielectrics on strained Si/SiGe layers are presented.

In chapter 2, the impact of surface morphology on J_g in fully processed strained Si devices is presented. The buried gate dielectric was uncovered by developing reverse processing procedures which stopped at the gate dielectric surface. Localised morphological features have been related to the simultaneously obtained current images from C-AFM. Localised differences in dielectric thickness and breakdown have also been studied through individual leakage curves obtained using the spectroscopy mode of C-AFM. The techniques were validated by comparison of the macroscopic (device-level) and nanoscale measurements on the same devices. Good agreement in breakdown, leakage, dielectric thickness and reliability was obtained for three sets of devices.

In chapter 3, defects and trap sites at the dielectric/semiconductor interface in strained Si devices has been studied using SCM. Variations in trapped charge density and V_{FB} have been studied using the scanning and spectroscopic mode of SCM. Localised variations have been related to the surface morphology. A good agreement in trends for all devices was observed. Interface trap density was evaluated at specific regions of the semiconductor substrate.

In chapter 4, nanoscale J_g (using C-AFM) and interface trap density (using SCM) have been studied for thin dielectrics on compressively strained SiGe layers. The impact of surface morphology and compressive strain on dielectric performance and reliability was studied by varying the Ge content in the SiGe layer (from 0 to 65%). Small scale

variations in surface roughness were also characterised using high resolution AFM imaging.

Nanoscale trends in dielectric performance have been shown to be in agreement with theory and previously reported macroscopic data. The SCM analysis developed has been validated by detecting degradation in dielectric performance with increasing Ge content. Other dielectric related defects have also been detected for one of the samples which indicate the sensitivity of SCM to study other defects.

The analysis in chapter 4 shows that while Ge affects performance, improvements in epitaxial growth minimises the degradation in performance due to surface roughness.

Chapter 5 discusses the future work and applications which may benefit from the electrical SPM techniques and analysis presented in this thesis. The chapter includes interfacial analysis of thin anti-reflective coatings on glass windows. This is followed by a brief description of the SCM analysis of standard SiO_2/Si samples to allow better understanding of its sensitivity. Finally, applications to nanoscale tubular structures are discussed.

Finally, conclusions are summarised in chapter 6.

Chapter 2. Nanoscale Analysis of Leakage in Dielectrics in Strained Silicon Devices

The work in this chapter investigates the effect of substrate induced surface roughness on leakage through gate dielectrics on epitaxially grown high mobility strained Si channels on relaxed SiGe substrates. Macroscopically, large scale roughness appears to affect gate leakage and other dielectric parameters (section 1.4.4). To understand precisely the effect of this roughness on the gate dielectric properties, high spatial resolution characterisation techniques are used. C-AFM is applied to study gate leakage at the nanoscale in fully processed high mobility strained Si n-MOSFETs. This is achieved by the selective removal of the gate from the dielectric followed by nanoscale C-AFM analysis of the dielectric surface. The removal of the layers in the gate stack was verified using Raman spectroscopy, SEM, EDX and C-AFM. A Hertzian contact model has been used to account for the AFM tip-sample contact area in order to extract leakage current density at the nanoscale. The techniques are applied to strained Si and Si control devices with different surface morphologies and macroscopic electrical data.

2.1 Background

High mobility channels are recognised technology boosters to compensate the loss in performance encountered through high-κ dielectrics, heavy doping profiles and increased parasitic effects in highly scaled devices. Improvements in μ_{eff}, I_{ds}, V_t and J_g from strained Si MOSFETs compared with bulk-Si devices have been extensively reported before [43, 52, 75, 120, 158-162]. However, device processing and material quality affect whether the strain induced theoretical enhancements are realised in practice. Dielectric quality and reliability in strained Si devices is not same as bulk-Si devices (sections 1.4.3 and 1.4.4). Surface roughness induced by the SiGe SRBs appears to have a major impact on J_g and dielectric reliability (section 1.4.4). For devices having the same strained Si channel thickness and processed simultaneously, devices fabricated on rough SRBs exhibiting the typical crosshatch surface morphology exhibit degraded dielectric properties compared with devices fabricated on smoother substrates [75, 120]. Although small scale surface roughness is known to affect J_g in bulk Si devices (section 1.4.4), in strained Si/SiGe devices the dominating lengths of the various types of

roughness are significantly greater than those in bulk Si, ranging from several tens of nm to μm (section 1.3.2). Rough SRBs with crosshatch undulations can exhibit surface roughness of the order of few microns (section 1.3.2). The role of the large scale roughness and its effect on dielectric behaviour is required to be understood.

In order to enable the appropriate modifications to epitaxial growth of Si on SiGe buffers for optimal device reliability (which is affected by gate leakage) as well as speed, leakage must therefore be analysed at nanoscale and compared directly with the underlying surface morphology. Such nanoscale characterisation is in contrast with the conventional device level measurements which average out any localised behaviour (section 1.5). Nanoscale leakage and reliability studies on dielectrics are commonly carried out on blanket materials. However since thermal device processing can modify the surface morphology of strained Si/SiGe substrates [163], nanoscale analysis on fully processed devices is more helpful to understand the device level behaviour. This requires well-controlled layer-by-layer reverse processing of transistors which also enables to establish any correlation between macroscopic electrical device measurements and nanoscale material properties.

In this chapter, C-AFM is applied to study gate leakage in fully processed strained Si MOSFETs. This was achieved by selective removal of the gate above the dielectric using a wet-etch recipe. These nanoscale measurements are then related to the underlying substrate morphology. It is shown here that large scale surface undulations result in variation in leakage across the crosshatch period. C-AFM in spectroscopy mode has also been used to obtain localised leakage curves from different regions of interest. Macroscopic device level gate leakage measurements and breakdown characteristics are compared with nanoscale measurements from the same devices.

2.2 Material growth and device processing

2.2.1 Material Growth

The thick (rough) SRBs were grown using the graded composition method at Warwick University (UK). Thin (smooth) SRBs were fabricated using the low temperature growth method at Stuttgart University (Germany). The differences between the two growth methods and the typical surface roughness and morphology have been discussed in section 1.3.2. The complete structure of the two SRBs is shown in Fig. 2.1.
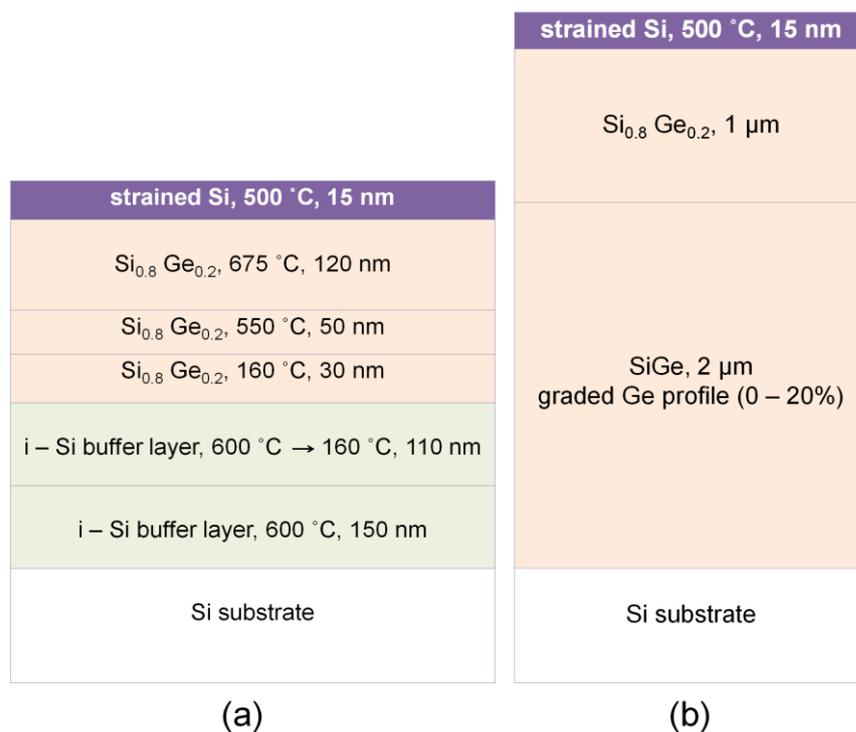
Figure 2.1 Epitaxial structure of (a) smooth and (b) rough SiGe SRBs.

Rough SRBs were deposited on Si wafers using a linear grading of Ge up to a final value of 20%. The graded structure was capped with ~ 1 μm thick $Si_{0.80}Ge_{0.20}$ layer. The final thickness of rough SRBs was nearly 3 μm. For smooth SRBs, the growth temperature was reduced from 600 °C to 160 °C during the deposition of an intrinsic Si buffer. A 30 nm thick $Si_{0.80}Ge_{0.20}$ layer was grown at 160 °C to cause supersaturation of point defects (section 1.3.2). After this, the growth temperature was increased to 550 °C and then to 675 °C to result in smooth SiGe SRBs of final thickness ~ 200 nm. Following this, a 15 nm thick strained Si layer was grown on top of the two SRBs at the

KTH Royal Institute of Technology (Sweden). The channel was subjected to a Boron implantation dose of 6×10^{12} cm^{-2} at 40 keV followed by another dose of 6×10^{12} cm^{-2} at 140 keV for an intended doping density of $\sim 6 \times 10^{17}$ cm^{-3}.

2.2.2 Strain and relaxation using Raman spectroscopy

Relaxation in the two SRBs and strain in the epitaxial strained Si layer were determined using Raman spectroscopy. Figs. 2.2 and 2.3 show the Raman spectra obtained from the strained Si layers grown on the two SRBs using two different laser wavelengths. In total, 10 Raman spectra from strained Si layers on each SRB were obtained. The reason for using two different wavelengths was to control the penetration depth of the laser. A lower wavelength results in smaller penetration depth [145]. This allows accurate characterisation of thin surface films. A laser of high wavelength penetrates deeper and allows characterisation of multi-layered stacks.
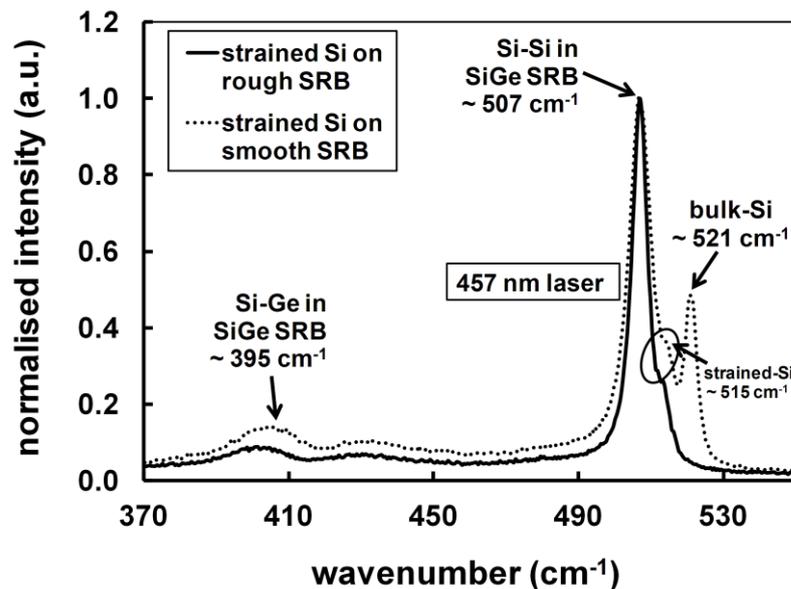
Figure 2.2 Raman spectra obtained from 15 nm thick strained Si layers grown on rough and smooth SiGe SRBs. Laser wavelength: 457 nm (visible). Due to the higher penetration depth of the laser on Si (> 200 nm), lattice vibrations from the SiGe SRBs are also observed.
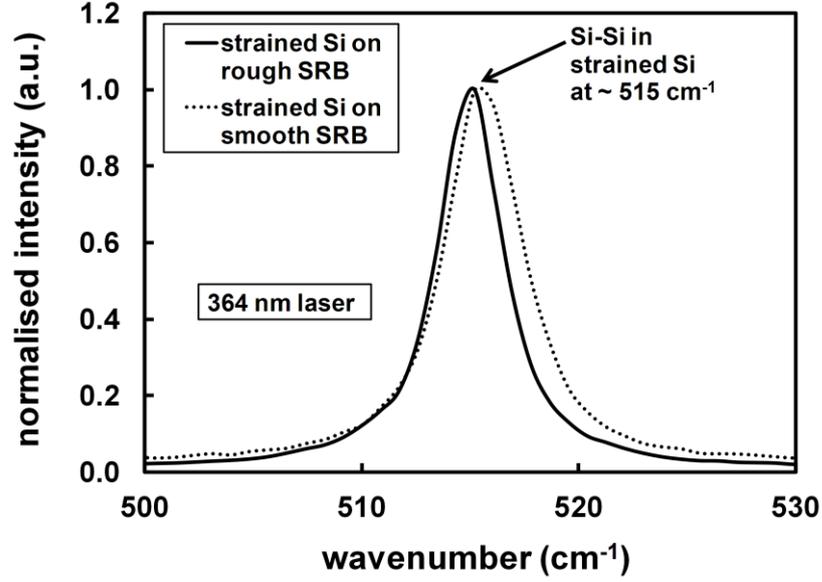
Figure 2.3 Raman spectra obtained from 15 nm thick strained Si layers grown on rough and smooth SiGe SRBs. Laser wavelength: 364 nm (ultra-violet, UV). Due to the lower penetration depth of the laser on Si (< 15 nm), lattice vibrations from the SiGe SRBs are not observed.

Raman spectra obtained using the 457 nm laser (Fig. 2.2) shows lattice vibrations from the strained Si layer as well the SiGe SRBs. This is because a 457 nm visible laser on Si penetrates by more than 200 nm [145, 164]. The 364 nm UV laser has a penetration depth less than 15 nm when incident on Si. Hence, lattice vibrations from the strained Si layer are only observed as shown in Fig. 2.3. The amount of strain (ε) in strained Si/SiGe layers can be estimated from the following equations [148, 165].

$$\varepsilon_{Si} = \left(\frac{520.7 - \omega_{Si-Si}^{s-Si}}{715} \right), \qquad\qquad \textbf{2.1}$$

$$\varepsilon_{SiGe} = \left(\frac{520.7 - \omega_{Si-Si}^{s-SiGe} - 66.9x}{730} \right), \qquad\qquad \textbf{2.2}$$

where, ε_{Si} and ε_{SiGe} are the values of strain in Si and SiGe layers respectively, ω_{Si-Si}^{s-Si} and ω_{Si-Si}^{s-SiGe} are the Raman peak positions of Si-Si lattice vibrations in strained Si and SiGe layers respectively, and x is the amount of Ge in the SiGe SRB.

Calculation of the degree of relaxation in the underlying SRBs requires that the in-plane lattice constant of the SiGe layers ($a_{SiGe}^{\parallel}$) is known. Once ε_{SiGe} has been obtained using equation 2.2, $a_{SiGe}^{\parallel}$ can be calculated from the following equation [166]:

$$\varepsilon_{SiGe} = \left(\frac{a_{SiGe}^{\parallel} - a_{SiGe}}{a_{SiGe}}\right),$$ **2.3**

where, a_{SiGe} is the average lattice constant of a fully relaxed SiGe layer which varies with the amount of Ge (x) and can be written as [92]:

$$a_{SiGe} = 5.4311 + 0.1988x + 0.028x^2.$$ **2.4**

 Following this, the degree of relaxation in the SiGe SRBs (R_{deg}^{SiGe}) can be evaluated from the following equation [92]:

$$R_{deg}^{SiGe} = \left(\frac{a_{SiGe}^{\parallel} - a_{Si}}{a_{SiGe} - a_{Si}}\right),$$ **2.5**

where, a_{Si} (5.4309 Å) is the average lattice constant of the bulk-Si substrate.

Similar equations for strain and degree of relaxation in strained Si layers grown on SiGe SRBs can be written:

$$\varepsilon_{Si} = \left(\frac{a_{Si}^{\parallel} - a_{Si}}{a_{Si}}\right),$$ **2.6**

$$R_{Si}^{deg} = \left(\frac{a_{Si}^{\parallel} - a_{SiGe}}{a_{Si} - a_{SiGe}}\right),$$ **2.7**

where, $a_{Si}^{\parallel}$ is the in-plane lattice constant of strained Si.

Using the Raman spectra in Figs. 2.2 and 2.3 and equations 2.1-2.7, strain in the strained Si channel and relaxation in the underlying SiGe SRBs have been calculated. A relaxation of ~ 98% has been observed in both the SRBs while the epitaxial strained Si layer has a strain of ~ 0.75%. This value of strain agrees well for a fully strained Si layer grown on a $Si_{0.80}Ge_{0.20}$ SRB (~ 0.76%, as calculated using equations 2.4 and 2.6).

2.2.3 Dislocation density in the rough and smooth SRBs

Misfit dislocations which relieve strain in the rough SRBs propagate from the interface to the surface through threading dislocations (section 1.3.2). Threading dislocation density (TDD) in bulk-Si substrate and the two SRBs was estimated through Schimmel defect etching over 100×100 μm^2 areas. A modified Schimmel etching solution (55% vol. CrO$_3$ (0.4 M) and 45% vol. HF (49%)) was used to enable defect etching [78]. Preferential etching by the Schimmel solution reveals dislocations which appear as pits as shown by the defect micrographs in Fig. 2.4a-c. Smooth and rough SRBs require defects for relieving strain and hence exhibit higher TDD compared with bulk-Si substrates (Fig. 2.4d).
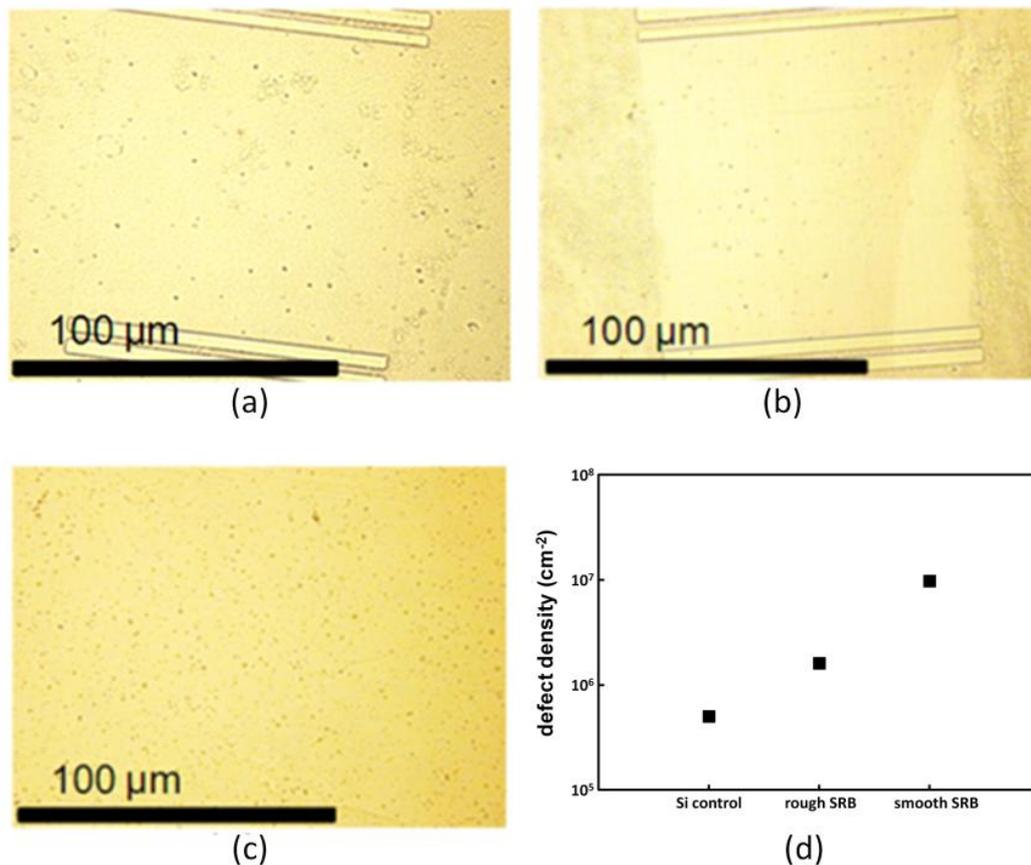
Figure 2.4 Micrographs of (a) bulk-Si, (b) rough SRB, (c) smooth SRB following Schimmel etching, and (d) variation in defect density. Defect measurements by Dr. Enrique Escobedo-Cousin, Newcastle University.

Fig. 2.4d also shows that the smooth SRBs exhibit higher TDD compared with the rough SRBs. This is possibly because strain relaxes in smooth SRBs through point defects which accumulate at their point of growth and do not glide like misfit dislocations in rough SRBs (section 1.3.2). For rough SRBs it is possible that misfit dislocations glide towards and terminate at the edge of the wafer, thereby reducing defect density.

2.2.4 Device processing

The gate stack consisted of a 2.7 nm SiO_2 grown by thermal oxidation at 700 °C and annealed in forming gas (N_2 + H_2) for passivation. This was followed by 150 nm of standard in-situ highly doped poly-Si. The doping concentration in the poly-Si was 3×10^{20} cm^{-3}. The source and drain implants used Arsenic and rapid thermal annealing was carried out at 950 °C for 30 s for dopant activation. The gate, source and drain areas were silicided for reducing the sheet, parasitic, contact, and interconnect resistances in these regions. Silicidation used Ni, and resulted in a 20 nm NiSi layer. The devices were covered by a 150 nm layer of low temperature oxide (LTO) for device isolation. Si control devices were also fabricated and processed alongside the strained Si devices for comparison. The cross-sectional MOSFET architecture of the Si control and strained Si devices is shown in Fig. 2.5.
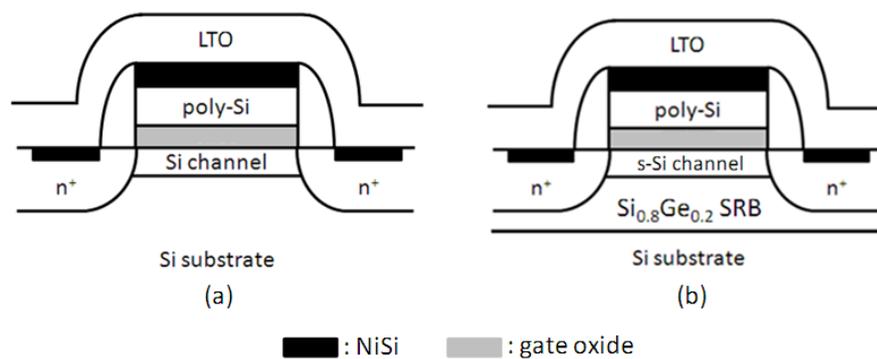
Figure 2.5 Cross-sectional architecture of (a) Si control and (b) strained Si.

2.3 Macroscopic gate leakage and dielectric breakdown

2.3.1 Experimental details

Macroscopic (device-level) J_g measurements were carried out using the Agilent 4155C parameter analyzer. The typical gate leakage measurement setup for an n-MOSFET is shown in Fig. 2.6. The source, drain and substrate are grounded while the gate is positively biased. Such measurement setup maximises the accurate component of gate leakage current which flows from the gate to the substrate. In total, 5 devices of each type (Si control, rough and smooth SRB strained Si) were measured. The area of the devices studied was 100 μm^2 ($L_g = W_g = 10$ μm). This area was chosen because the scale of crosshatch surface roughness associated with rough SRBs is typically a few microns (section 1.3.2).
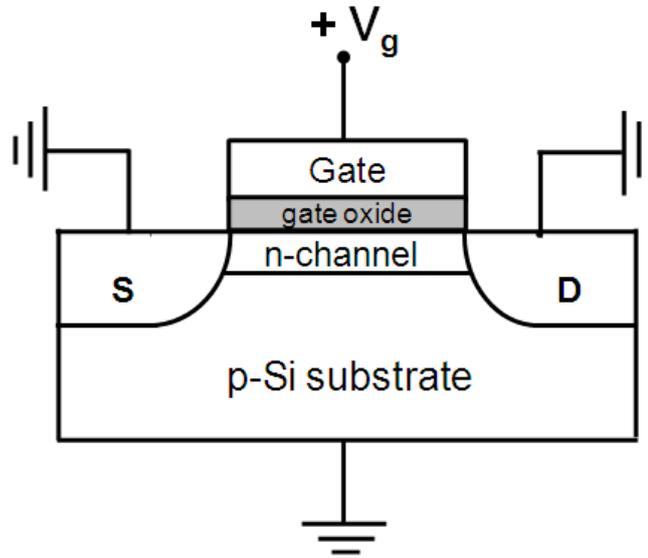
Figure 2.6 Gate leakage current (I_g) – gate voltage (V_g) measurement setup for an n-MOSFET.

The macroscopic oxide electric field (E_{ox}) and the voltage drop across the oxide (V_{ox}), can be calculated by using the following equations [97]:

$$E_{ox} = \frac{V_{ox}}{t_{ox}}, \qquad\qquad \textbf{2.8}$$

$$V_{ox} = V_g - (V_{FB} + V_{poly} + V_{sub}),$$ **2.9**

where, t_{ox} is the dielectric thickness, V_{poly} is the potential drop in the poly-Si gate and V_{sub} is the potential drop in the semiconductor (Si/strained Si).

Macroscopic *C-V* characteristics were obtained using the Agilent 4294A impedance analyzer in two-probe configuration (see section 3.2). These were then analysed by the CVC software developed at the North Carolina State University [167] to extract t_{ox}, V_{FB}, V_{poly} and V_{sub}. Once E_{ox} is obtained, J_g can be evaluated with varying E_{ox}.

Constant high field stressing (at $E_{ox} = 18$ MVcm^{-1}) was performed to induce Fowler-Nordheim (F-N) leakage until hard breakdown was achieved. Source, drain and substrate were grounded during electrical stressing.

2.3.2 Macroscopic gate leakage

Typical J_g-E_{ox} curves from unstressed Si control and strained Si devices are shown in Fig. 2.7. Si control devices show higher J_g compared with both strained Si devices, which is in agreement with previous studies [75]. The maximum reduction observed in J_g was 31% for smooth SRB strained Si devices over Si control. This improvement was reduced to 17% for rough SRB strained Si devices. Such improved leakage behaviour from strained Si devices is due to the higher transverse effective mass in the Δ_2 valleys (preferentially occupied by electrons) and increased electron affinity compared with unstrained bulk-Si [22, 73]. Fig. 2.7 also shows that strained Si devices grown on smooth SRBs have improved (lower) leakage compared with those on rough SRBs, despite having the same levels of strain (section 2.2.2). Differences in t_{ox} can also affect leakage. However, analysis of *C-V* data by the CVC software indicated a uniform dielectric with $t_{ox} = 2.7 \pm 0.11$ nm. It has also been shown before that reduction in TDD reduces J_g in high mobility semiconductor devices [168, 169]. However, smooth SRBs have exhibited higher TDD compared with rough SRBs (Fig. 2.4).

Hence, ε_{Si}, t_{ox} and TDD cannot explain the differences in macroscopic J_g between the rough and smooth SRB strained Si devices which exhibit significantly different surface morphology and roughness (Figs. 1.18 and 1.19).
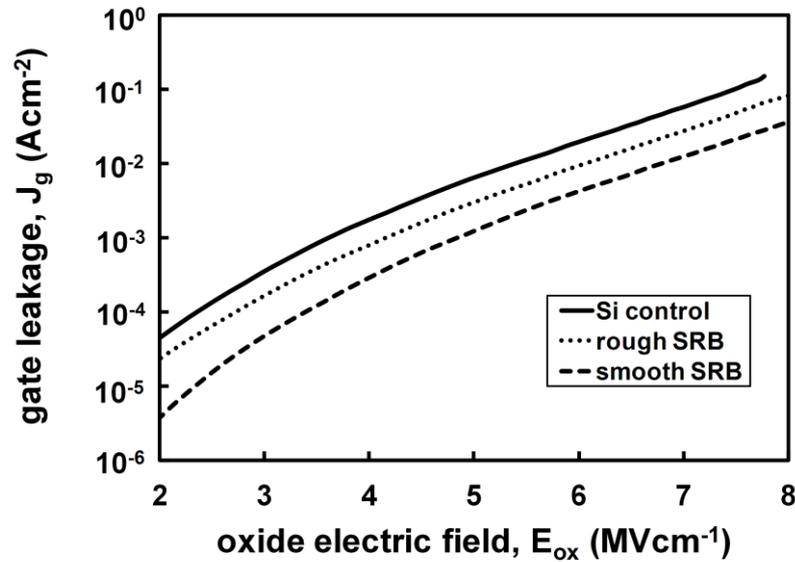
Figure 2.7 Gate leakage for the Si control, rough and smooth SRB strained-Si devices before breakdown.

2.3.3 Stress induced leakage and dielectric breakdown

Fig. 2.8 shows the time to hard breakdown for Si control and strained Si devices. Strained Si devices with lower surface roughness (smooth SRB) were found to be the most resilient to electrical stressing followed by rougher strained devices and Si control devices (Fig. 2.8).

Fig. 2.9 shows J_g-E_{ox} curves from Si control and strained Si devices after hard breakdown was achieved. Higher J_g for smooth SRB devices was observed compared with the unstressed condition (Fig. 2.9). For Si control and rough SRB devices, hard breakdown appears to result in drop in stress current because the compliance limit of the equipment was exceeded. This drop in stress current for similar devices has been observed before [75].

The improved electrical breakdown behaviour for strained Si devices with lower surface roughness (smooth SRB) is in agreement with previous reports [75, 170, 171]. However, there is a lack of understanding about the role of surface roughness on the breakdown of strained Si devices in literature.
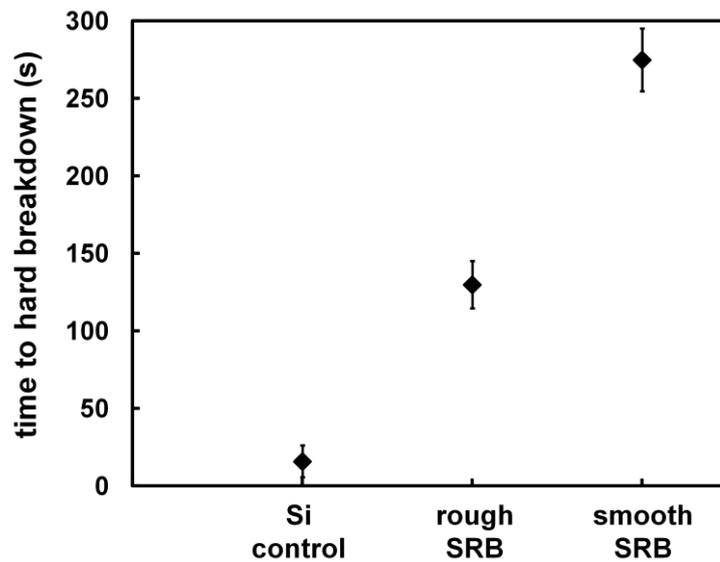
Figure 2.8 Typical time to hard breakdown for Si control, rough, and smooth SRB strained Si devices subjected to a constant field stressing of 18 MVcm^{-1}.
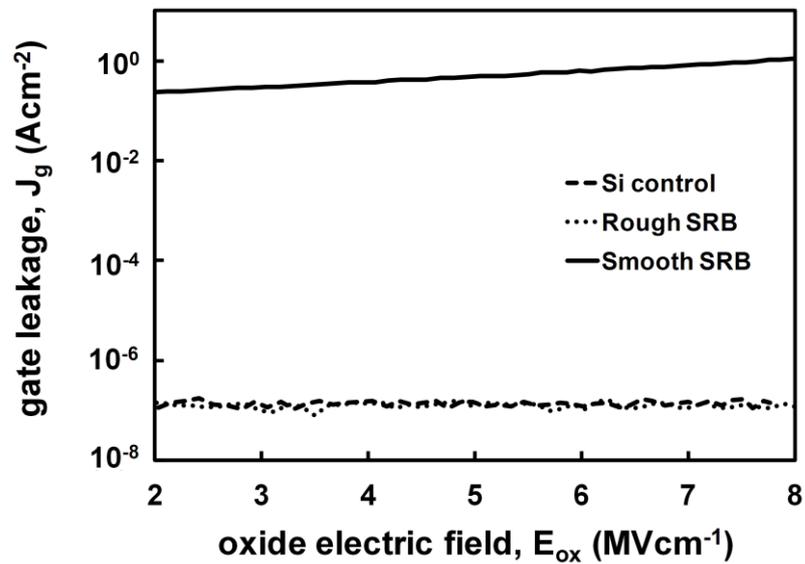
Figure 2.9 Gate leakage for the Si control, rough and smooth SRB strained-Si devices after breakdown. The drop in J_g post breakdown for Si control and rough SRB strained Si devices has been reported before in [75].

2.4 Reverse processing the gate stack

In order to relate the device-level response to the surface morphology, gate de-processing was carried out to allow a comparison of surface roughness and gate dielectric leakage on a nanoscale. Layers above the thin SiO_2 gate dielectric (LTO, NiSi and poly-Si) were etched without damaging the dielectric surface to enable C-AFM measurements to be performed on macroscopically measured devices.

Gate reverse processing was carried out using hydrofluoric acid (HF) (10:1) for 75 s which removed isolation above the gate (LTO) and NiSi. Poly-Si was removed using poly-etch ($HNO_3:H_2O:HF$, 50:20:1) for 5 s followed by 10% potassium hydroxide (KOH) solution for 5 minutes. The intermediate etch step of poly-etch was required as KOH was not able to etch poly-Si after HF etching. This was possibly due to the formation of a KOH resistant layer due to the reaction between HF and NiSi. The poly-etch itself can be used to remove poly-Si [172], however, it is highly acidic and its etch selectivity against SiO_2 is poor compared with KOH [173]. All etching was carried out at room temperature.

Fig. 2.10 shows a cross-sectional SEM image of a smooth SRB strained Si device before the de-processing. Raman spectroscopy (using a 364 nm UV laser) was primarily used to systematically monitor the removal of layers (LTO, NiSi and poly-Si) during the gate stack etching along with SEM, EDX and C-AFM.
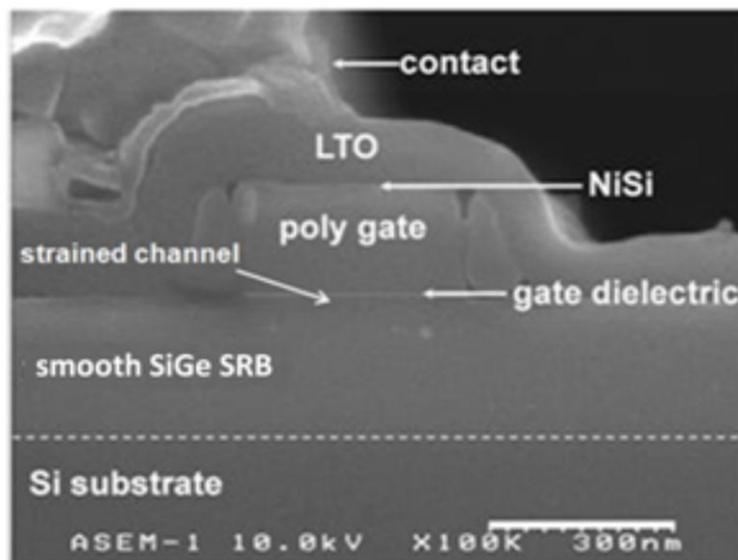
Figure 2.10 Cross-sectional SEM image of a 10 x 10 μm^2 strained Si MOSFET device on a smooth SRB.

2.4.1 Removal of LTO and NiSi

Fig. 2.11 shows the Raman spectra taken on the gate region before and after HF etching. The spectrum corresponding to the unetched device features characteristic peaks of NiSi around the 200 and 300 cm^{-1} wavenumber region, indicating the presence of NiSi [174, 175]. These peaks disappear after 75 s of HF etch, indicating removal of NiSi. Reduction in background intensity associated with the presence of NiSi after HF etching is another indicator of NiSi removal. Removal of LTO and NiSi is further confirmed by the SEM image taken after 90 seconds of HF (10:1) etching, as shown in Fig. 2.12. A ~ 200 nm thick grainy layer resembling poly-Si is observed after HF etching. The thickness of ~ 200 nm for poly-Si (Fig. 2.12) is higher than the initial thickness of 150 nm (Fig. 2.10). This difference may be due to the gold coating on the sample which was required for SEM imaging.

The SEM measurement setup had an attached X-ray spectrometer which allowed EDX measurements. Elemental compositions of different layers in the gate stack and the substrate were studied before and after HF etching. The spatial resolution of EDX is dictated by the penetration depth and the spread of the incident electron beam which vary with the density of the sample under study. A penetration depth and a spot size of 1-2 μm can be typically observed.

The relative atomic concentration of various elements in a smooth SRB strained Si device measured by EDX is shown in Fig. 2.13. It can be observed that after HF etching, Ni is not observed at all confirming removal of NiSi. The concentration of oxygen also reduces which is due to the etching of the thick layer of LTO, however, some native oxide and the gate oxide are still present. Owing to the large penetration depth (1-2 μm), presence of Si and Ge is also recorded. Since Si and Ge are not etched by HF, their relative concentrations show an increase after HF etching (Fig. 2.13). The presence of Al on gate (although very small amounts) is possibly due to surface contamination. HF etching and subsequent rinse with DI water removes surface contaminants and hence no Al is observed after HF use.
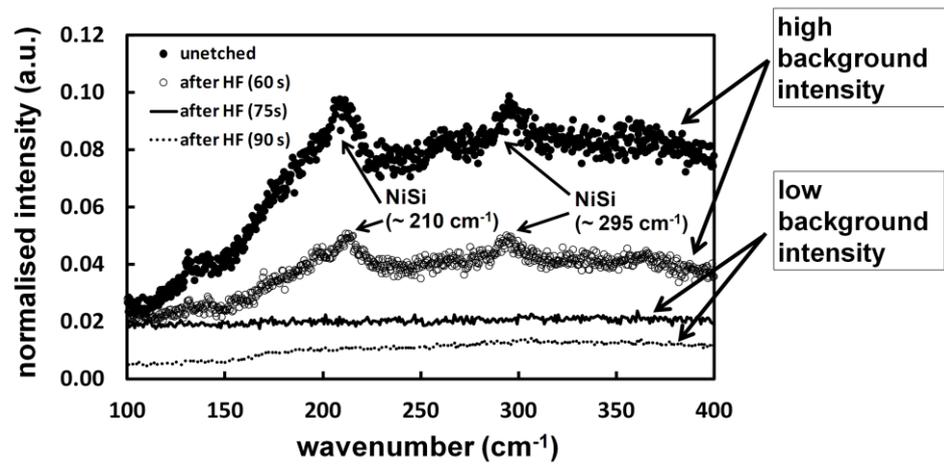
Figure 2.11 NiSi removal from the gate stack.
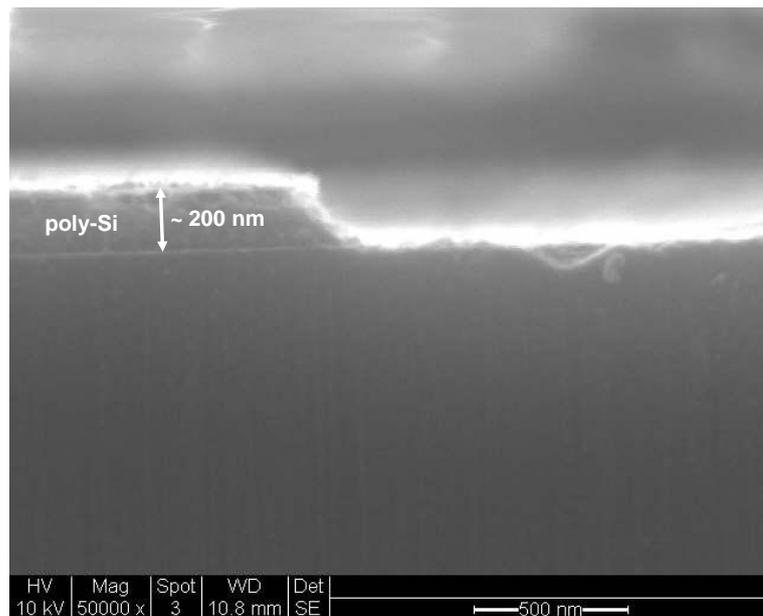
Figure 2.12 Cross-sectional SEM image of a 10 x 10 μm^2 smooth SRB strained Si device obtained after 90 s of HF (10:1) etching. Poly-Si is observed indicating that the gate stack is still intact with LTO and NiSi removed.
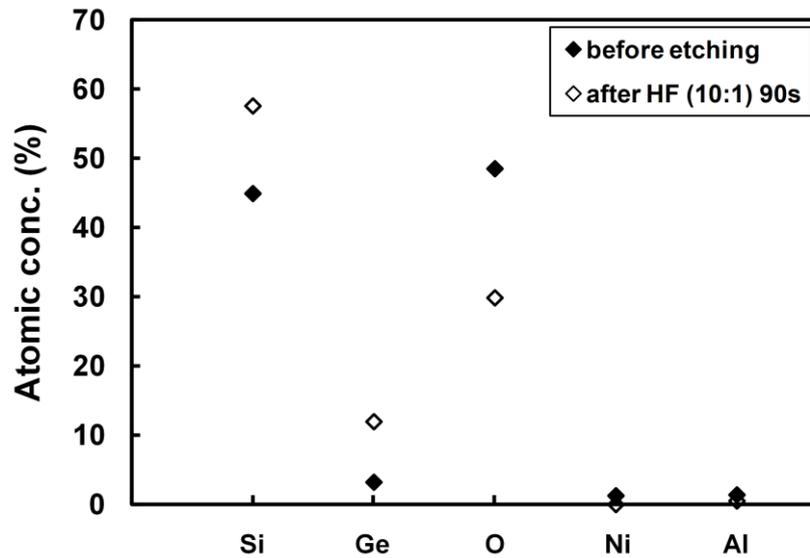
Figure 2.13 EDX analysis showing relative elemental concentration in a smooth SRB strained Si device before and after HF (10:1) etching.

2.4.2 Assessment of poly-Si removal using Raman spectroscopy

Fig. 2.14 presents a comparison of Raman spectra measured on the gate region before, during and after full gate de-processing i.e. after LTO, NiSi and poly-Si removal on a Si control (Fig. 2.14a) and a smooth SRB strained Si device (Fig. 2.14b). For the Si control sample (Fig. 2.14a), un-etched and HF-etched samples exhibit a high intensity peak at ~ 518 cm^{-1}. This peak is asymmetrically broadened towards the lower side with increased half width compared with the bulk Si reference position of 521 cm^{-1} and hence represents Si-Si vibrations in poly-Si [176]. The penetration depth of the 364 nm UV laser on NiSi is ~ 21 nm which is more than its thickness of 20 nm. Consequently, the Si-Si vibrations from poly-Si are also observed in the Raman spectra before and after HF etching (Fig. 2.14).

Following poly-etch and KOH etch, the broad poly-Si peak disappears and a comparatively narrower peak at ~ 521 cm^{-1} is observed as shown in Fig. 2.14a. This is the expected peak position for Si-Si vibrations in bulk-Si. Similarly, Fig. 2.14b shows disappearance of the broad poly-Si peak and appearance of a comparatively narrower peak at ~ 515 cm^{-1}. This is the expected peak position for Si-Si vibrations in strained Si grown on Si$_{0.80}$Ge$_{0.20}$ SRB (Fig. 2.3). From these results it can therefore be concluded

that poly-Si has been removed entirely, since in all samples the Raman peak of the gate region matches that of the channel material beneath the gate.
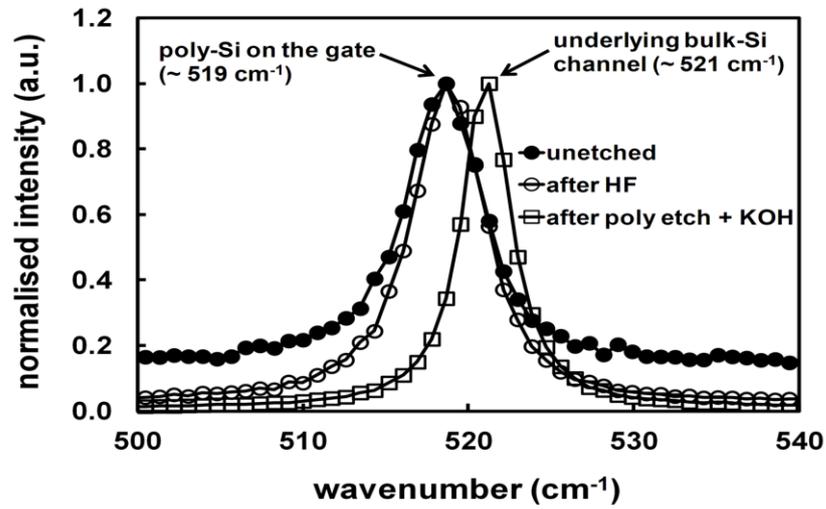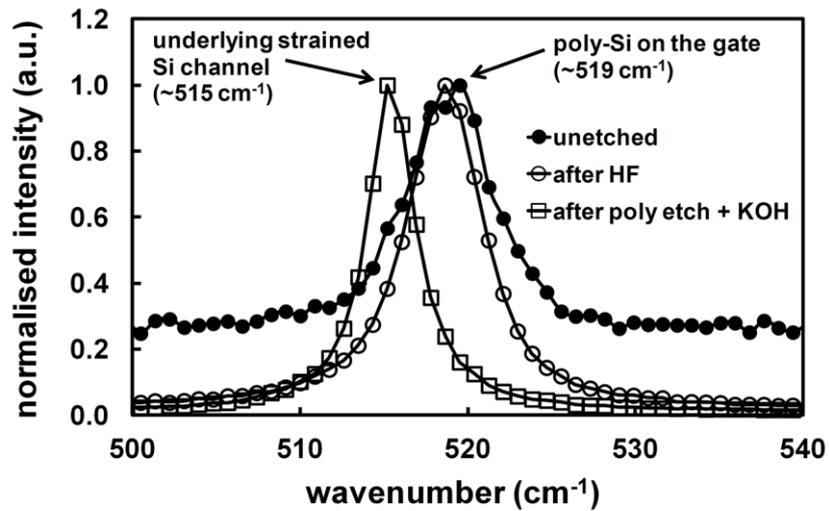
Figure 2.14 Raman spectra showing the removal of poly-Si in the (a) Si control and (b) strained Si gate regions.

The change in the Raman peak position for Si-Si vibrations for a strained Si device is presented in Fig. 2.15 as a function of the etch process. There is a change of the 518 cm^{-1} poly-Si peak to the expected position for strained Si (515 cm^{-1}) as the poly-Si is removed after KOH etching. The strained Si peak position on regions outside the gate (field) has also been measured at each etch stage for comparison. The field region is not covered by poly-Si and consistently exhibits a peak position at 515 cm^{-1} at every stage

of etching indicating the presence of the strained Si layer. After complete de-processing using HF (10:1) for 75 s followed by 5 s of poly etch and 5 minutes of 10% KOH, the peak positions for the gate and field regions converge at 515 cm^{-1}. This further confirms that the poly-Si has been removed. Five measurements on each gate region for three different devices were obtained and included in Fig. 2.15. However due to the same peak position at different regions of the gate on the same device these points overlap. In contrast, strained Si measured in the field region is very consistent between the devices. The data points corresponding to poly-Si show a significant dispersion at every stage of the de-processing but when poly-Si was removed all data points show same peak position with no dispersion. This is due to the single crystal uniformity of Si/strained Si, whereas poly-Si exhibits a wider range of wavenumbers depending on the size of its crystallites [177]. The dispersion itself can therefore prove useful in confirming poly-Si layer removal.

Variation in Raman peak position similar to Fig. 2.15 was also observed for rough SRB devices.
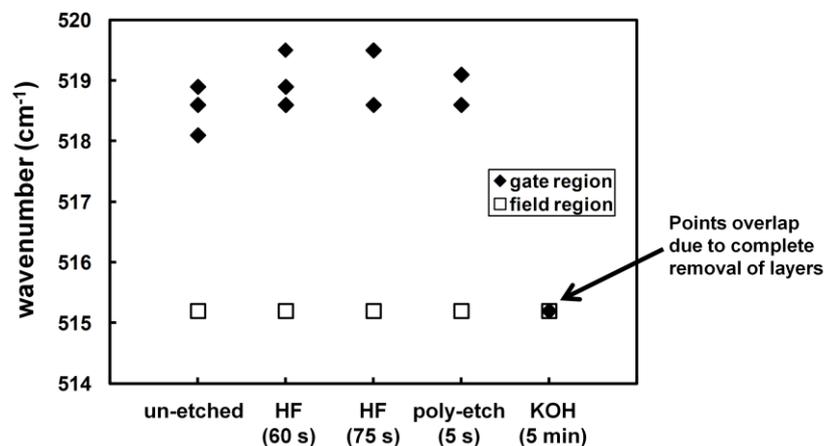
Figure 2.15 Variation in Raman peak position with increasing etch time measured on a smooth SRB device.

2.4.3 Assessment of poly-Si removal using C-AFM

C-AFM was also used to detect thin poly-Si residues which may have gone undetected by Raman spectroscopy. Fig. 2.16 shows the topography (left) and current (right) maps during poly-Si removal in a strained Si device on a rough SRB. The crosshatch pattern which was transferred on the surface of the dielectric is evident in regions where poly-Si is completely removed. In other areas poly-Si residues appear as bright regions in the current map, in contrast with uncovered gate dielectric regions which exhibit no current. A low AFM tip-sample bias of 0.2 V was chosen to highlight the significant difference in the conductivity of the highly doped poly-Si and the SiO_2 gate dielectric. Further etching was needed after this stage which removed the poly-Si residues. Fig. 2.17 shows the topography and current maps after complete removal of poly-Si. The crosshatch pattern is clearly visible on the surface of the dielectric. Significantly low level of current at a higher voltage (1.5 V) compared with the C-AFM image in Fig. 2.16 indicates complete removal of poly-Si and presence of the dielectric. Following this, C-AFM *I-V* traces were obtained at different points on the surface of the uncovered gate dielectric and these are shown in Fig. 2.18. It can be seen that the traces are typical to that of a dielectric such as SiO_2 which breaks at higher voltages. This concludes that not only the layers in the gate stack above the gate dielectric have been successfully removed, the dielectric is still present.
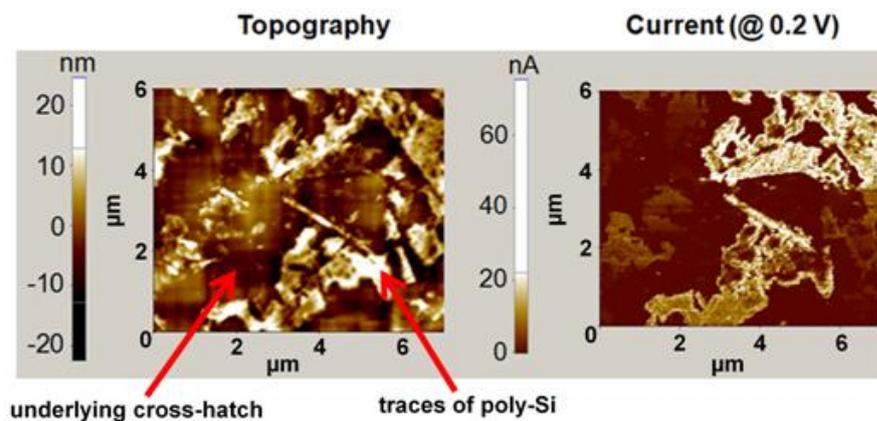
Figure 2.16 Topography and current map from gate region showing incomplete poly-Si removal. Large traces of poly-Si are visible in the topography image with corresponding as (bright regions) high current at a low bias of 0.2 V in the current map.
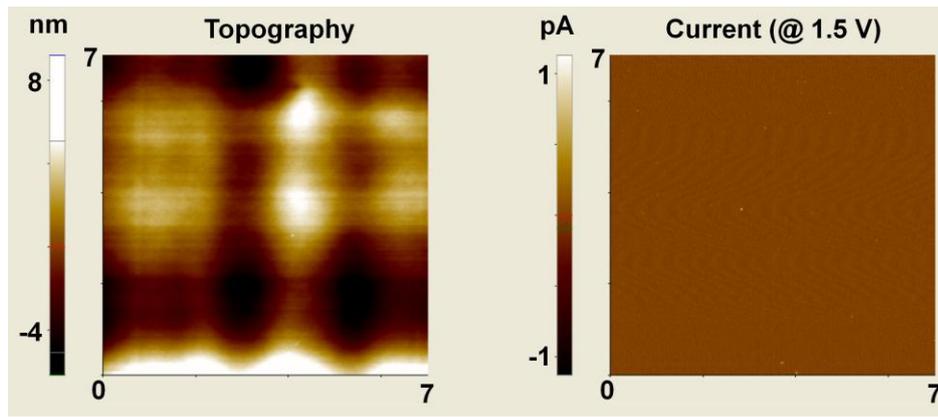
Figure 2.17 Topography and current map from gate region after complete removal of poly-Si. Significantly low level of current at a higher voltage compared with the C-AFM image in Fig. 2.16 indicates complete removal of poly-Si and presence of the dielectric.
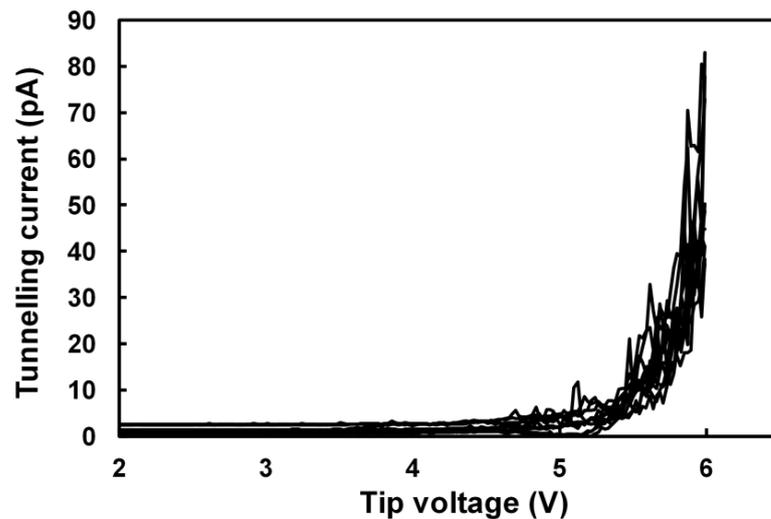
Figure 2.18 *I-V* traces from 12 random locations across the surface of the gate dielectric of a smooth SRB device after successful reverse processing obtained using C-AFM in spectroscopy mode.

Fig. 2.19 compares the topography of the gate region before and after full gate de-processing using AFM. After de-processing the metal contacts are removed completely and the gate region is below the surrounding LTO, indicating poly-Si removal. The surrounding LTO in the field region was ~ 0.5 μm thick and was not completely

removed during de-processing. Hence, the surrounding LTO was observed as shown in Fig. 2.19. The metal contacts were removed during HF etching and the poly-etch stage.
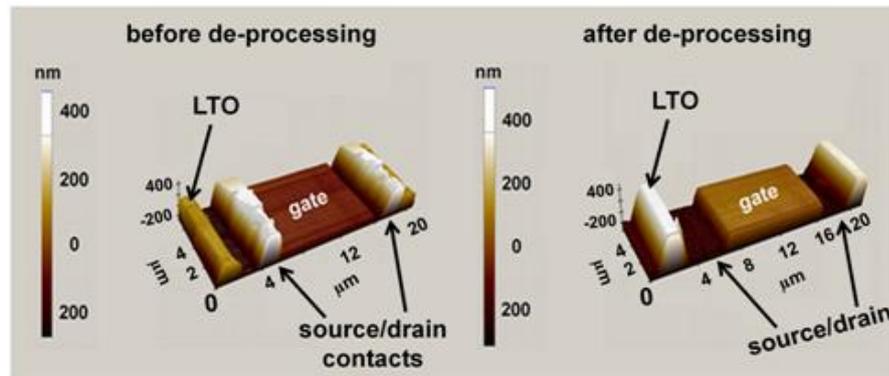
Figure 2.19 AFM images showing the gate region before and after de-processing.

2.5 Nanoscale electrical analysis using C-AFM

2.5.1 C-AFM measurement setup

The XE-150 AFM from Park Systems was used to obtain the topography and nanoscale current maps operating in the C-AFM mode. Fig. 2.20 shows the C-AFM measurement setup. In addition to the usual components used for recording topography (Fig. 1.21), the conductive probe tip is also connected to the AFM controllers through a low noise current amplifier to obtain simultaneous current maps. The force between the atoms at the sample's surface and those at the cantilever's tip deflects the cantilever which is monitored to obtain the surface topography (section 1.5.2). Since the tip is conductive and connected to a current amplifier, the C-AFM setup is able to respond to differences in conductivity across the scanned area. The AFM controller is also used for providing the dc bias during measurements which is typically applied through the substrate. A slightly doped diamond coated tip has been used for C-AFM measurements. The diamond tips have a high mechanical Q-factor for high sensitivity. The detector side of the cantilever has a nearly 30 nm thick Al coating which enhances the reflectivity of the laser beam by a factor of about 2.5. The typical radius of the diamond coated conductive tips is nearly 100 nm.

The C-AFM tip has a thin wire attached to it which connects to the low noise current amplifier via a head extension module as shown in Fig. 2.21. The head extension module provides a near short circuit between the C-AFM tip and the current amplifier to avoid any resistive loss. The connected components are shown in Fig. 2.22. The amplified current signals are transferred to the AFM controllers via a frame module. Fig. 2.23 shows the C-AFM set-up mounted on the AFM which is inside the isolation box to avoid the influence of the ambient environment. The Z-scanner is located behind the AFM head. The X-Y stage which is physically separated from the Z-scanner is also shown in Fig. 2.23.
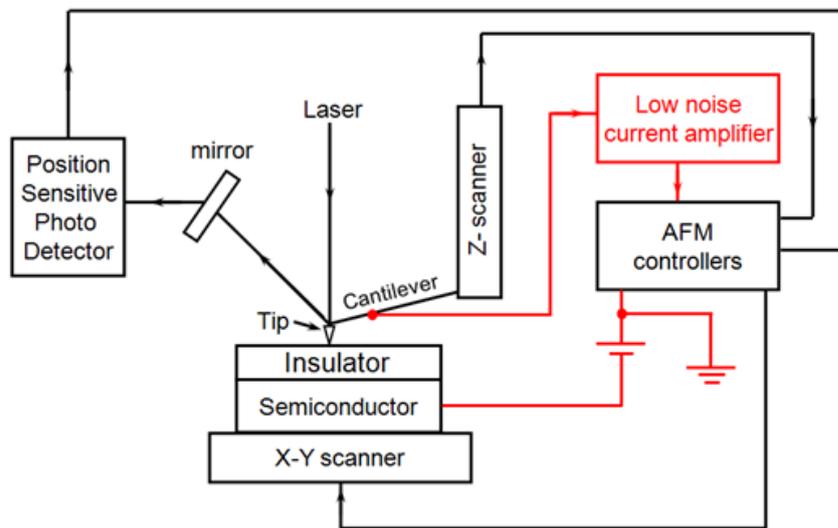
Figure 2.20 Schematic diagram of the C-AFM measurement setup.
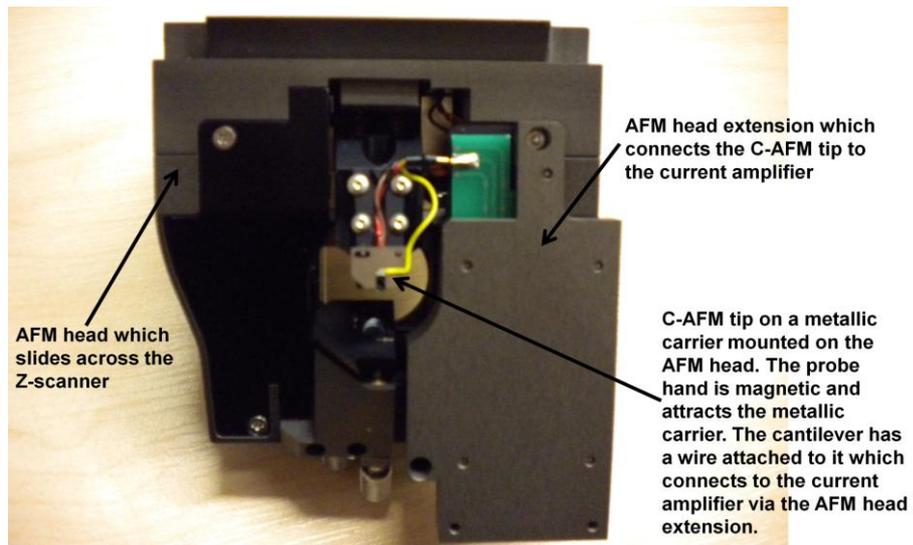
Figure 2.21 Diamond coated C-AFM tip mounted on the AFM head. The tip is connected to the current amplifier via a head extension module.
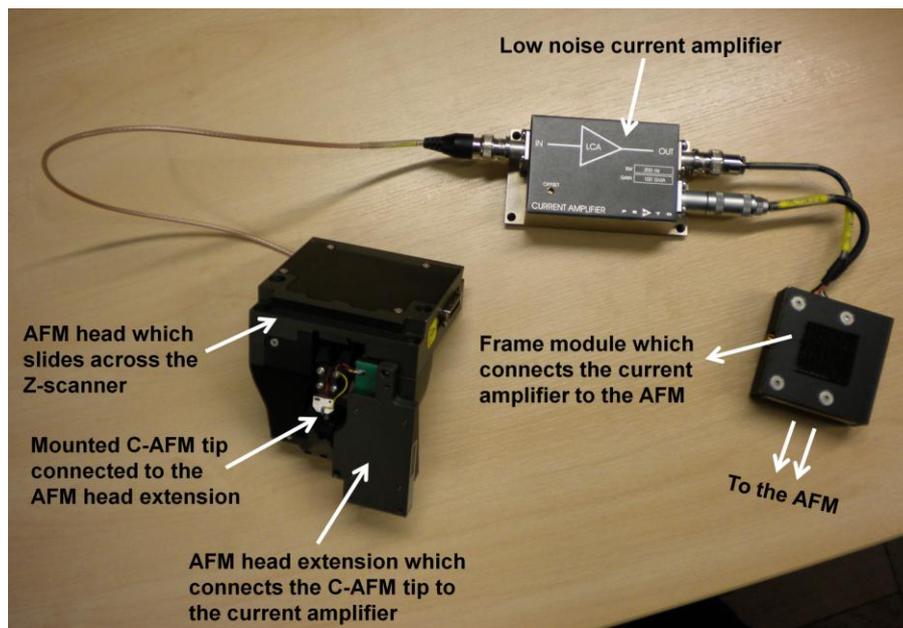
Figure 2.22 AFM head with the mounted tip connected to the current amplifier which is connected to the AFM through a frame module.
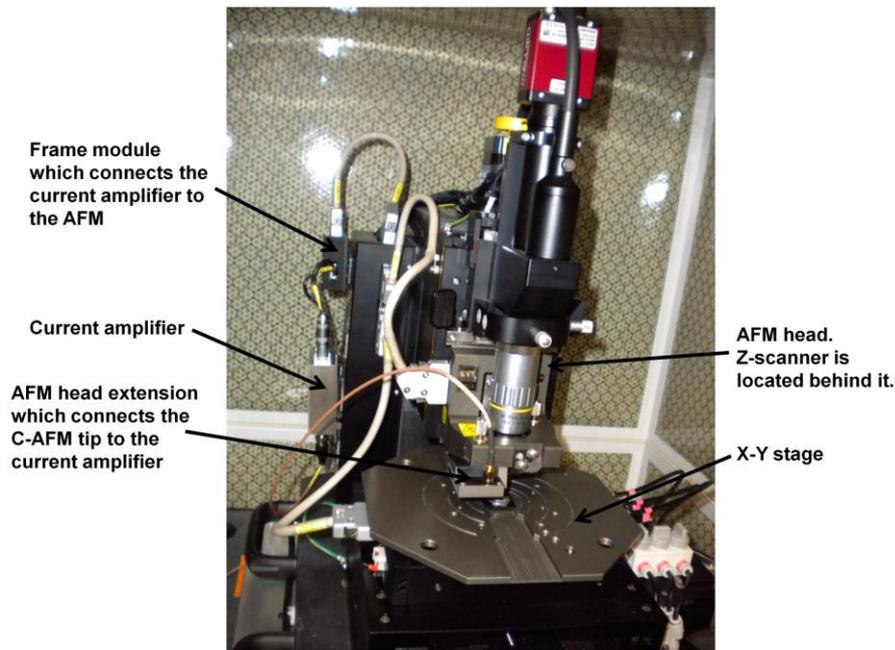
Figure 2.23 The C-AFM components mounted on the AFM inside the isolation box to avoid the effects of the ambient environment.

To scan a soft material such as SiO_2 with a relatively hard material such as a diamond coated C-AFM tip requires optimisation of the normal force of contact (P) between the tip and the dielectric surface. Such optimisation is needed to avoid any physical and electrical damage to the sample. In order to achieve this, C-AFM scans were obtained from SiO_2 on bulk-Si substrate at different levels of P. The C-AFM set-up used in this thesis has a default value of 750 nN for P. C-AFM scans were obtained by varying P from 750 nN to 200 nN. These are shown in Fig. 2.24 with topography shown on the left and current images on the right. The tip-sample bias was kept constant at 4V for different values of P.

Fig. 2.25 compares the variation in R_q, $\Delta_{p\text{-}v}$ and average leakage current through the dielectric with varying P. The values of R_q and $\Delta_{p\text{-}v}$ do not show any difference with varying P. However, the average leakage current shows a decrease with decreasing values of P. Since the applied bias is same (4 V), Fig. 2.25 shows that the dielectric is prone to an early breakdown at high values of P compared with smaller values of P. Fig. 2.25 also shows that there is no change in the level of leakage current for $P = 300$ nN and 200 nN. Consequently, a value between 200 and 300 nN for P is optimum for C-AFM imaging of the samples under study.
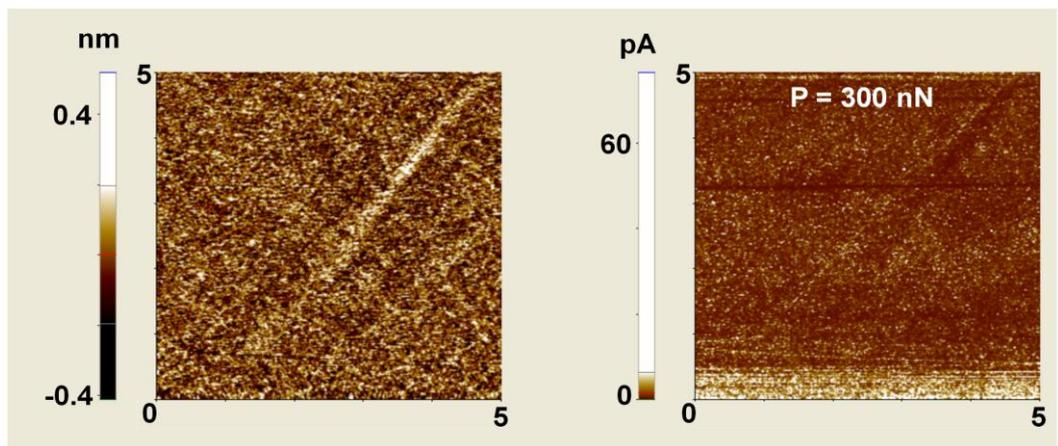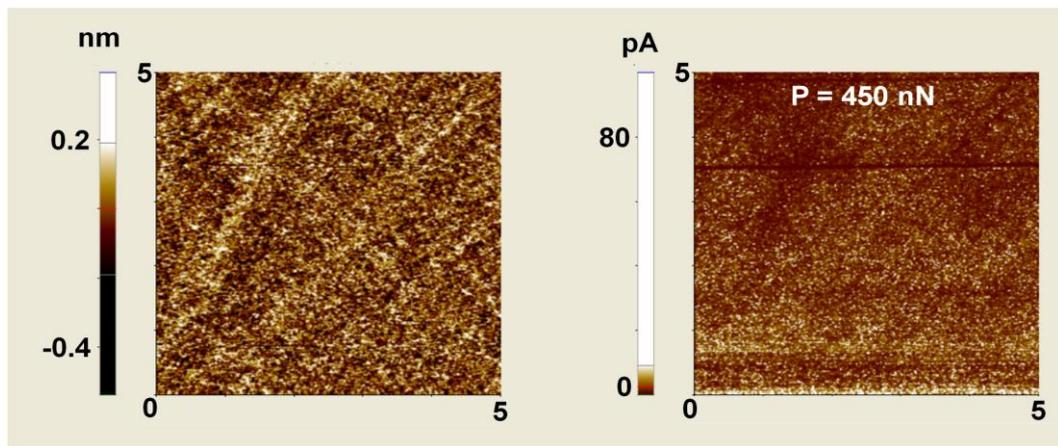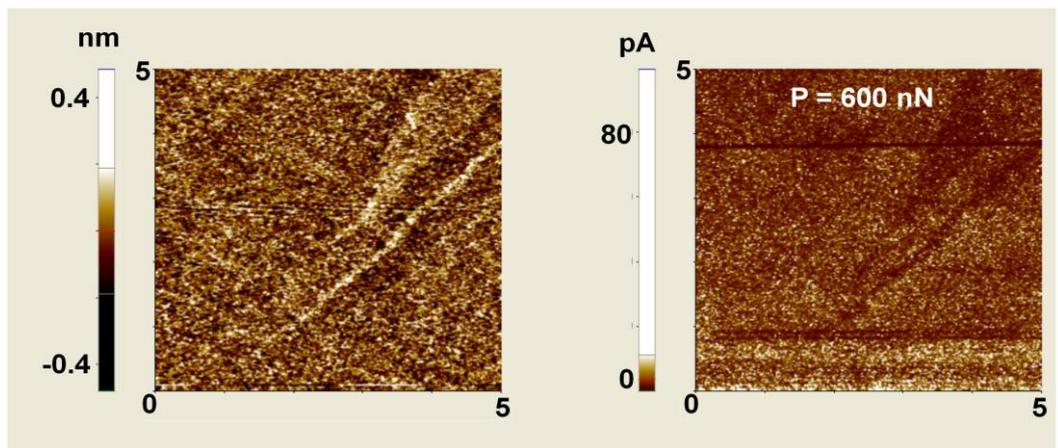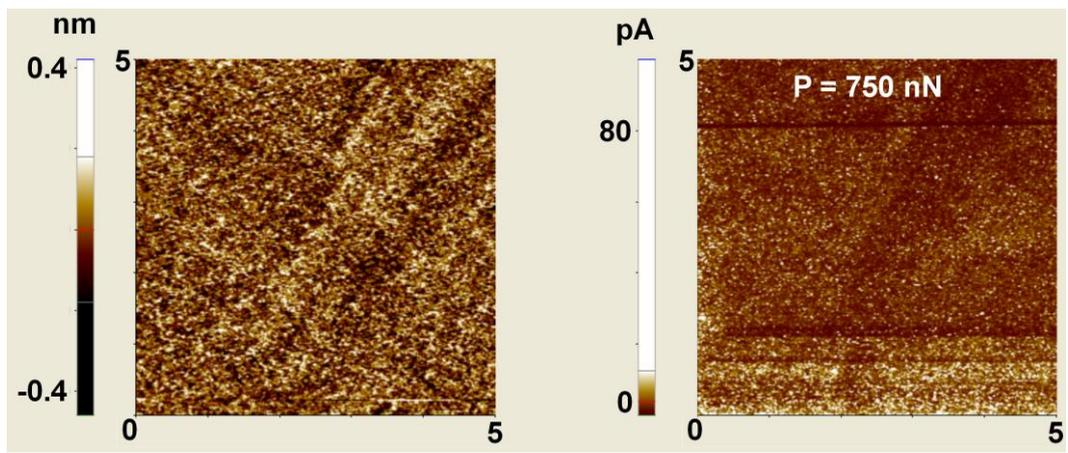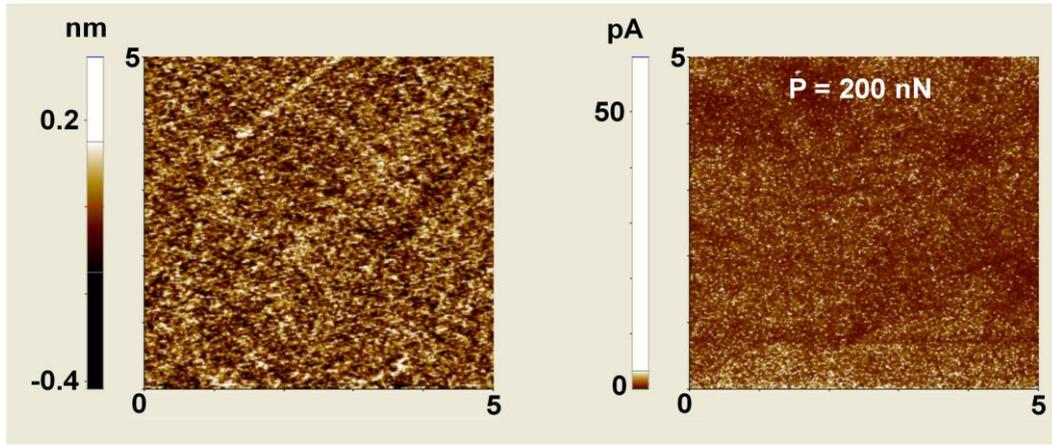
Figure 2.24 Topography (left) and current (right) maps obtained at different values of the normal contact force (*P*). The tip-sample bias was kept at 4 V.
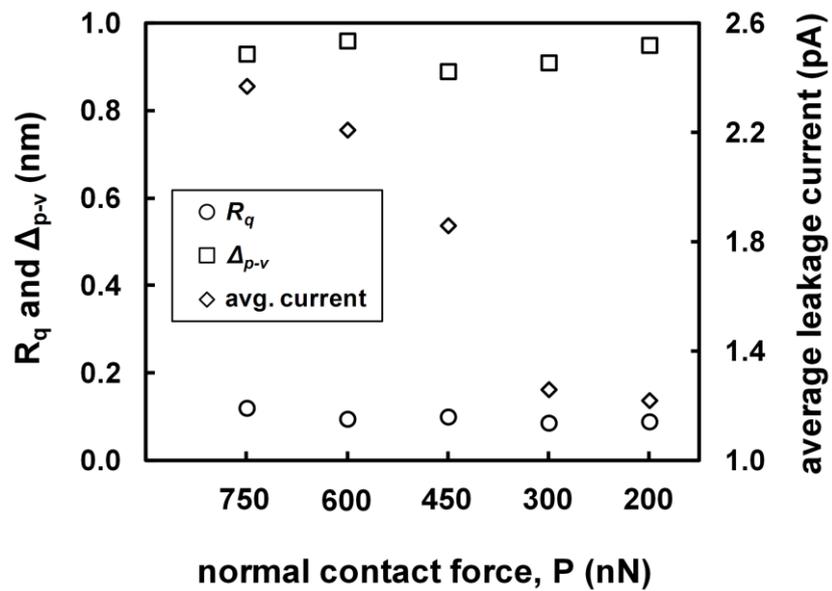
Figure 2.25 Variation in R_q, $\varDelta_{p\text{-}v}$ and average leakage current with different levels of *P*.

2.5.2 Effect of surface morphology on gate leakage

Figs. 2.26-2.28 show the topography (left) and corresponding current (right) images obtained from the de-processed gates of unstressed Si control and strained Si devices. Three measurements for each device type were obtained. The applied dc bias was varied (3V, 4V and 5V) to study whether the impact of surface morphology (if any) changes with different electrical stress.

The dielectrics on Si control exhibit the smoothest topography with $R_q = 0.14 \pm 0.00$ nm while the dielectrics on smooth SRB devices exhibit $R_q = 0.65 \pm 0.05$ nm. The typical crosshatch morphology of rough SRBs propagate on the surface of the thin dielectrics resulting in an R_q of 1.78 ± 0.81 nm. The values of R_q and $\Delta_{p\text{-}v}$ for Si control and strained Si devices obtained using C-AFM have been included in Fig. 2.29.

The bright regions in the C-AFM current maps represent the areas with high leakage through the dielectric. The current maps for the Si control devices (Fig. 2.26) and smooth SRB strained Si devices (Fig. 2.27) exhibit a random distribution of leakage regions. In contrast, the bright regions in the rough SRB strained Si device (Fig. 2.28) align with the crosshatch pattern shown in the corresponding topography image. This shows that gate leakage is directly impacted by the crosshatch roughness of the underlying semiconductor, which was significantly greater for the rough SRB device than the smooth SRB and Si control devices.
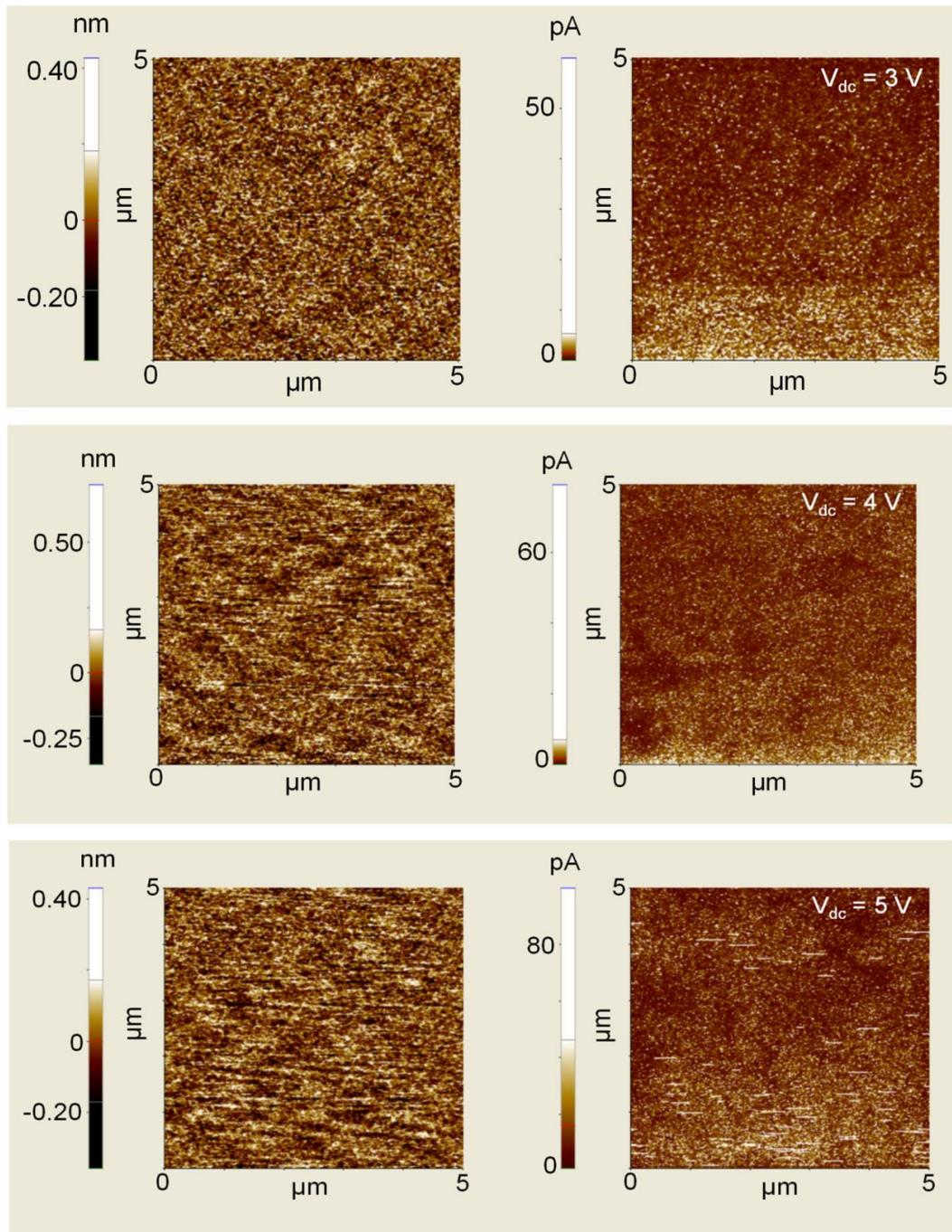
Figure 2.26 (Before electrical stressing) C-AFM maps of SiO$_2$ on Si control devices. The applied dc substrate bias is 3 V, 4 V and 5 V.
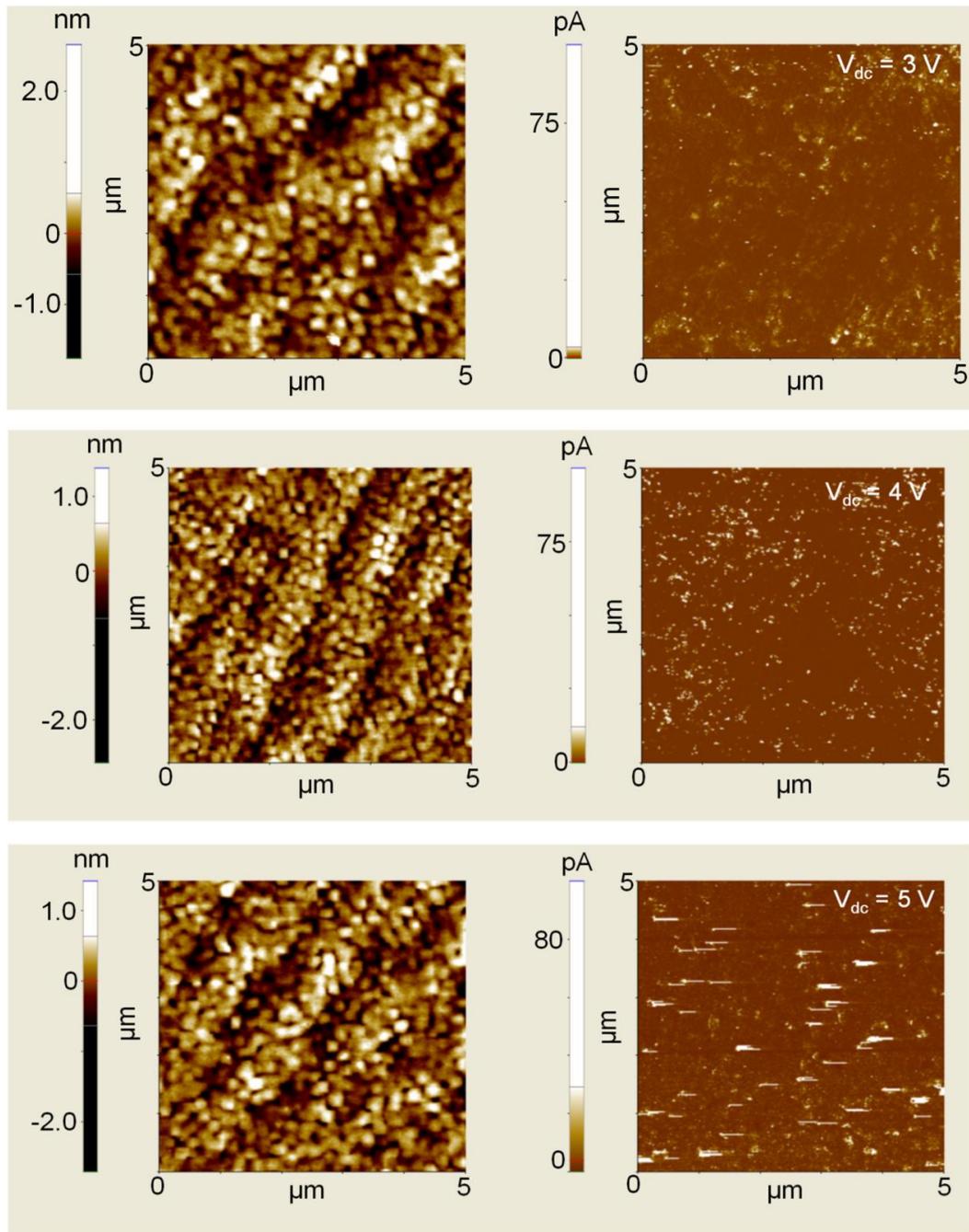
Figure 2.27 (Before electrical stressing) C-AFM maps of SiO₂ on smooth SRB strained Si devices. The applied dc substrate bias is 3 V, 4 V and 5 V.
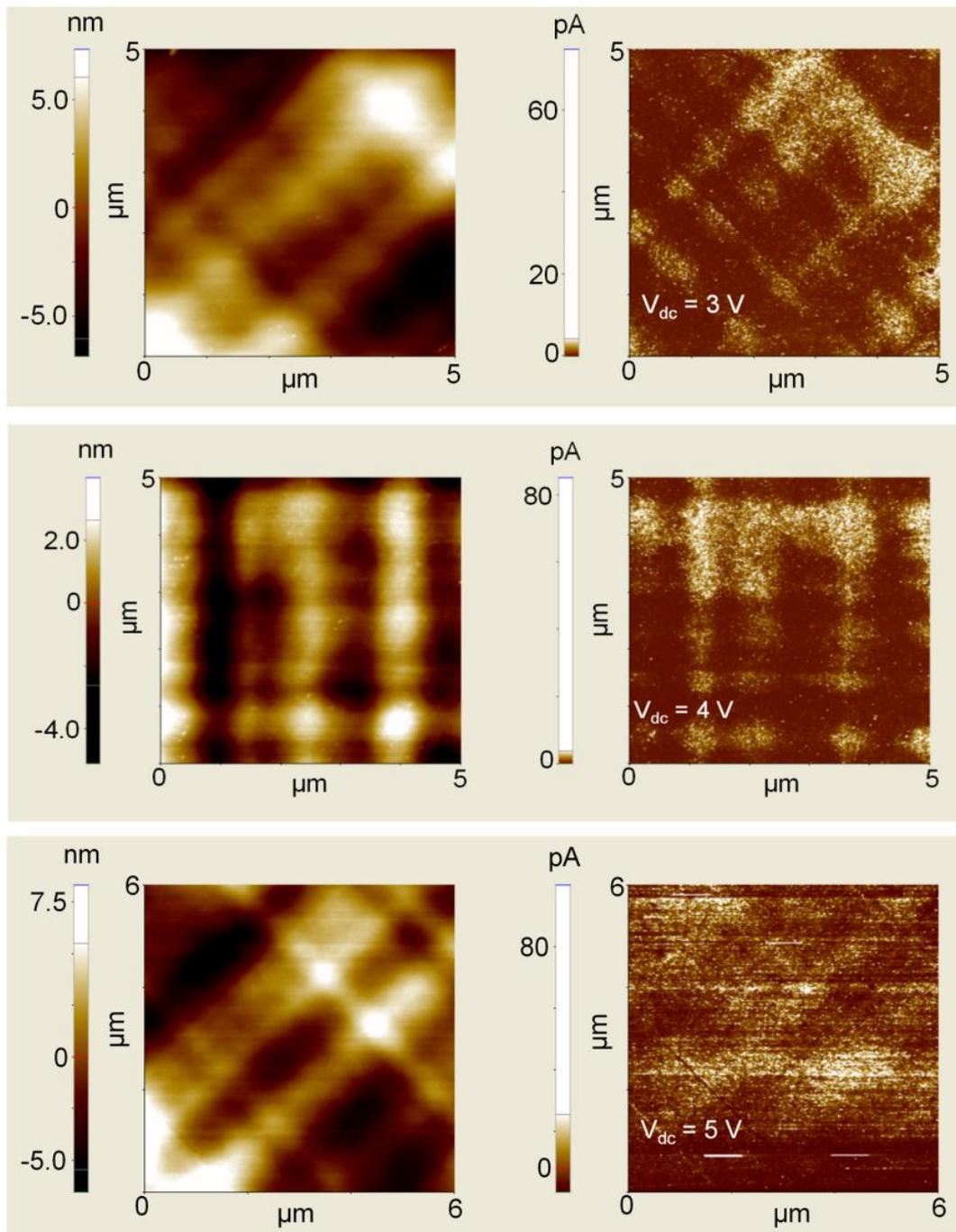
Figure 2.28 (Before electrical stressing) C-AFM maps of SiO$_2$ on rough SRB strained Si devices. The applied dc substrate bias is 3 V, 4 V and 5 V.
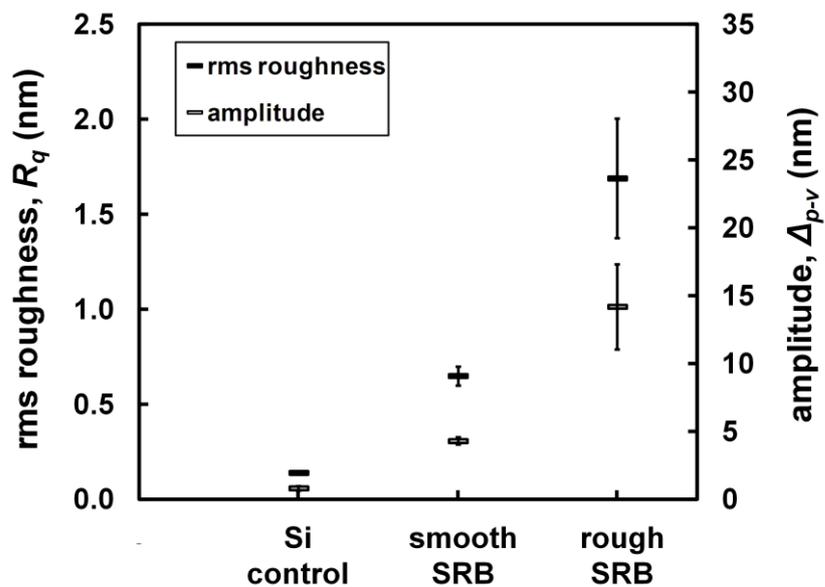
Figure 2.29 Comparison of rms roughness (R_q) and the amplitude of surface undulations ($\Delta_{p\text{-}v}$) for Si control and strained Si devices obtained using C-AFM.

Fig. 2.30 shows a comparison of surface heights and corresponding leakage across individual crosshatch undulations in a rough SRB device. A one to one correlation between surface features with corresponding leakage is shown. The linescans have been alphabetically labelled on the C-AFM image and on the graphs which show the variations in leakage with height. It can be observed that J_g is enhanced around troughs and along the steep slopes of the crosshatch (Fig. 2.30). A graph of height vs. leakage would not have differentiated between troughs and steep slopes, hence individual linescans have been shown in Fig. 2.30. Fig. 2.30 further shows that leakage degradation is higher across certain regions of large scale crosshatch undulations.
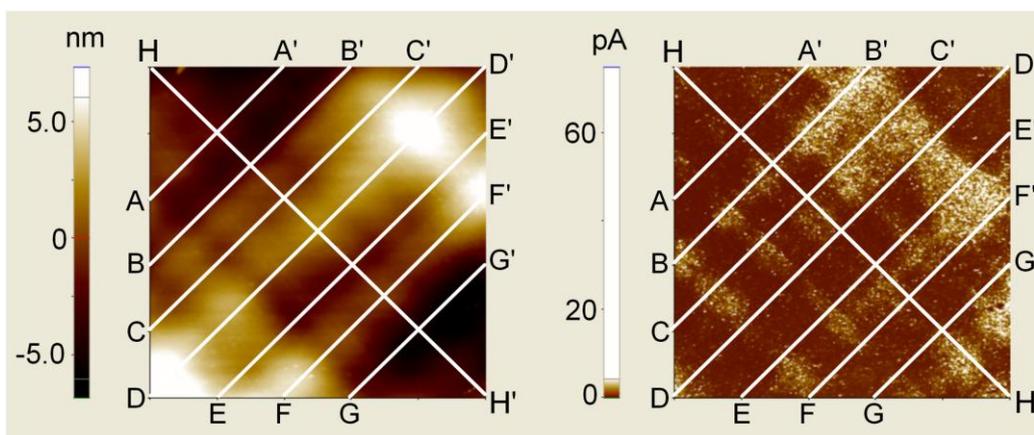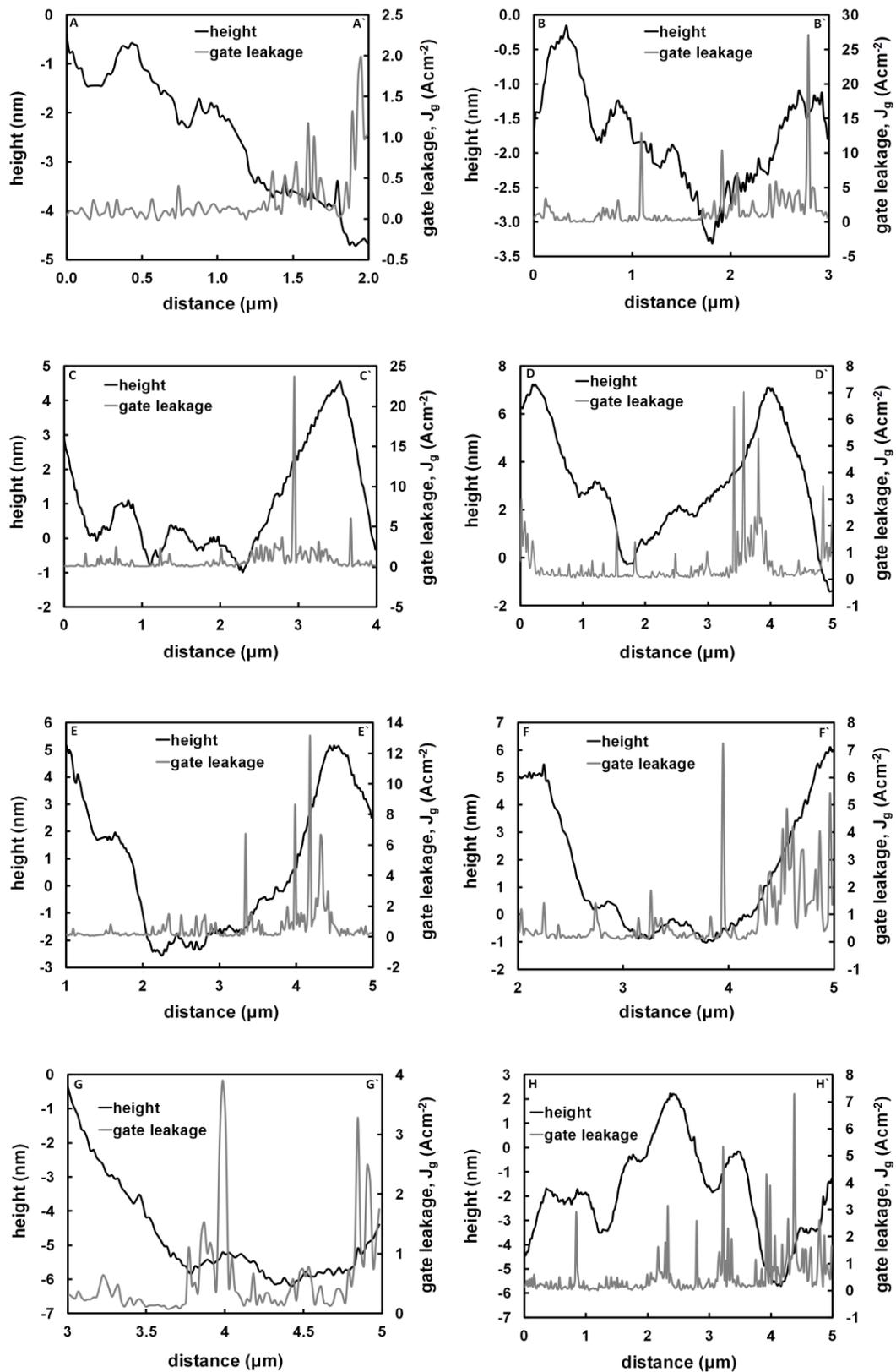
Figure 2.30 Individual line scans comparing crosshatch surface undulations with corresponding leakage behaviour in a rough SRB device. Troughs and steep slopes exhibit higher leakage compared with crests.

The improved leakage behaviour from strained Si devices is due to the higher transverse effective mass in the Δ_2 valleys and increased electron affinity compared with unstrained bulk-Si (section 2.3.2). The difference in the leakage behaviour of the two simultaneously processed and similarly strained Si devices is explained by the morphological dependence of leakage current for these devices (Figs. 2.28 and 2.30).

These results clearly have implications for dielectrics on other semiconductor material systems such as SOI, GaAs and InGaAs which also exhibit crosshatch undulations (section 1.3.2). Since the variation in leakage arises from the substrate rather than the dielectric, these results show that the substrate quality as well as the dielectric must be considered in devices which combine high-κ dielectrics with high mobility substrates.

2.5.3 Origins of enhanced leakage across crosshatch morphology

The variations in leakage across crosshatch undulations may be due to variations in the dielectric thickness and enhanced nanoscale roughness across high vicinal angle regions [111]. Alternatively, strain fluctuations due to non-uniform growth rates [76] and alterations in semiconductor composition across the dielectric interface through enhanced Ge diffusion from the underlying SRB [178] may also be responsible for enhanced leakage across crosshatch undulations. It has also been suggested that local concentration of electric fields on top of step-bunching edges may lead to enhanced leakage across SiO_2/SiC interfaces [121, 179]. It is possible that similar mechanisms take place at the dielectric/strained-Si interfaces in rough SRB devices, since both the step-bunching edges and crosshatch undulations exhibit steep profiles.

In order to clearly understand the factors responsible for the morphological dependence of leakage current in rough SRB devices, localised analysis is required.

2.5.4 Comparison of macroscopic and nanoscale leakage measurements

In order to calculate J_g at the nanoscale, calculation of the effective area of contact between the C-AFM tip and the dielectric surface (A_{eff}) is required:

$$J_g = \frac{I_g}{A_{eff}}, \qquad\qquad \textbf{2.10}$$

In order to calculate A_{eff}, Hertz contact model [180] has been used. According to the Hertzian model, two spherical bodies in contact under the effect of normal force result in a circular contact (radius, a_0). The model takes into account the material properties including Young's modulus and Poisson's ratio of the two bodies in contact as well as the normal force acting between them. In this case, the two bodies in contact are the conductive diamond coated tip and the gate dielectric (thermally grown SiO_2). The expressions for a_0 and A_{eff} are given as [180]:

$$a_0 = \left(\frac{3PR}{4E^*}\right)^{1/3}, \qquad \qquad \textbf{2.11}$$

$$A_{eff} = \pi a_o{}^2 = \pi \left(\frac{3PR}{4E^*}\right)^{2/3}, \qquad \qquad \textbf{2.12}$$

where, R is the relative radius of curvature of the contacting bodies and E^* is the contact modulus of the contacting surfaces. The expressions for R and E^* are given as [180]:

$$\frac{1}{R} = \frac{1}{R_{tip}} + \frac{1}{R_d}, \qquad \qquad \textbf{2.13}$$

$$\frac{1}{E^*} = \frac{1 - v_{tip}{}^2}{E_{tip}} + \frac{1 - v_d{}^2}{E_d}, \qquad \qquad \textbf{2.14}$$

where, R_{tip} and R_d are the individual radii of curvature of the tip and the dielectric respectively. In equations 2.13 and 2.14, v_{tip}, v_d and E_{tip}, E_d are the Poisson's ratio and Young's moduli, of the surface of the diamond tip and the dielectric, respectively. The dielectric can be considered as a flat surface with infinite radius, hence $R = R_{tip}$.

Table 2.1 lists the values of the parameters required to obtain A_{eff} [181-183]. Calculations using equations 2.11-2.14 resulted in $a_0 \sim 6.15$ nm and $A_{eff} \sim 120$ nm^2.

Table 2.1 Material parameters required for calculating A_{eff} [181-183].

Parameter	Value
P	200 nN
R_{tip}	100 nm
R_d	Infinite
v_{tip}	0.2
v_d	0.2
E_{tip}	900-1050 GPa
E_d	57-68 GPa

Similar to the oxide voltage at macroscale, V_{ox} at nanoscale is also not equal to the applied tip voltage (V_{tip}). For the MOS capacitor formed by the C-AFM tip, gate dielectric and the Si/strained Si semiconductor, V_{ox} is written as [184]:

$$V_{ox} = V_{tip} - (V_{FB} + V_{sub}). \qquad \textbf{2.15}$$

Equation 2.15 is similar to equation 2.9 except that the voltage drop in the poly-Si is not taken into account after de-processing.

According to [184], V_{FB} for nanoscale C-AFM analysis can be accounted for by the workfunction difference between the C-AFM tip and the underlying semiconductor (Si/strained Si):

$$V_{FB} = \varphi_m - \varphi_s, \qquad \textbf{2.16}$$

where, φ_m and φ_s are the metal and semiconductor workfunctions, respectively.

Equation 2.16 does not take into account the effect of dielectric charges on V_{FB}. This is because nanoscale C-AFM analysis is generally carried out on blanket layers and not on fully processed devices. For the devices studied in this chapter, the macroscopic values of V_{FB} are known through the analysis of macroscopic *C-V* data by the CVC software (section 2.3.1). The workfunction difference between an Al gate and the diamond coated tip (~ 0.70 eV) was taken into account for obtaining V_{FB} at the nanoscale.

For applied voltages that are relevant to C-AFM measurements, an n-MOSFET can be assumed to be in strong inversion. Under strong inversion, V_{sub} for an n-MOSFET is written as [13]:

$$V_{sub} = 2\psi_s, \qquad\qquad\qquad \textbf{2.17}$$

where, ψ_s is the potential difference between the intrinsic Fermi level and the Fermi level of the doped semiconductor (Si/strained-Si) and can be expressed as [13]:

$$\psi_s = \frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right), \qquad\qquad\qquad \textbf{2.18}$$

where, k is the Boltzmann constant, T is temperature, q is electron charge, N_{sub} is the substrate doping density and n_i is the intrinsic carrier concentration. The value of N_{sub} for both Si control and strained Si devices was obtained from the CVC software as 5.6 x 10^{17} cm^{-3} which is in close agreement with the intended doping density of 6 x 10^{17} cm^{-3} (section 2.2.1). The expression for n_i is given as [13]:

$$n_i = \sqrt{N_c N_v} \exp\left(-\frac{E_g}{2kT}\right), \qquad\qquad\qquad \textbf{2.19}$$

where, N_c and N_v are the effective density of states in the conduction and valence bands of the semiconductor (Si/strained Si), respectively and E_g is the energy of the band gap. Since strain alters the band structure, the values of E_g, N_c, N_v and consequently, n_i for strained Si are not same as bulk-Si and vary with the Ge content (and hence strain) in the underlying SRB [185].

Using equations 2.15 and 2.17, V_{ox} at nanoscale for an n-MOSFET can be expressed as,

$$V_{ox} = V_{tip} - (V_{FB} + 2\psi_s). \qquad\qquad\qquad \textbf{2.20}$$

The values of parameters required for calculating V_{ox} at the nanoscale for Si control and strained Si devices have been included in Table 2.2 [184-188]. Once V_{ox} has been calculated using equation 2.20, E_{ox} at the nanoscale is similar to equation 2.8:

$$E_{ox} = \frac{V_{ox}}{t_{ox}}. \qquad\qquad\qquad \textbf{2.21}$$

Table 2.2 Parameters required to calculate V_{ox} at the nanoscale [184-188]. Nanoscale V_{FB} has been obtained by correcting the macroscopic V_{FB} for the workfunction difference between the Al gate and the diamond coated AFM tip.

device	φ_m (eV) (Dia.)	φ_m (eV) (Al)	V_{FB} (V)	N_c (cm^{-3}) (x 10^{19})	N_v (cm^{-3}) (x 10^{19})	E_g (eV)	n_i (cm^{-3}) (x 10^{10})	ψ_s (V)
Si control	4.80	4.10	-0.25	2.80	2.50	1.12	1.03	0.46
rough SRB	4.80	4.10	-0.40	0.90	0.56	1.00	2.82	0.44
smooth SRB	4.80	4.10	-0.32	0.90	0.56	1.00	2.82	0.44

After calculating A_{eff} (equation 2.12) and V_{ox} (equation 2.20) for nanoscale leakage analysis, the average leakage current and the applied dc bias from the C-AFM maps of Figs. 2.26-2.28 were converted to J_g and E_{ox} respectively. These were then compared with previously reported device level data [75] from similar devices. Fig. 2.31 shows that the values of nanoscale J_g obtained by C-AFM is comparable with macroscopic J_g measured on the same devices with varying E_{ox}.
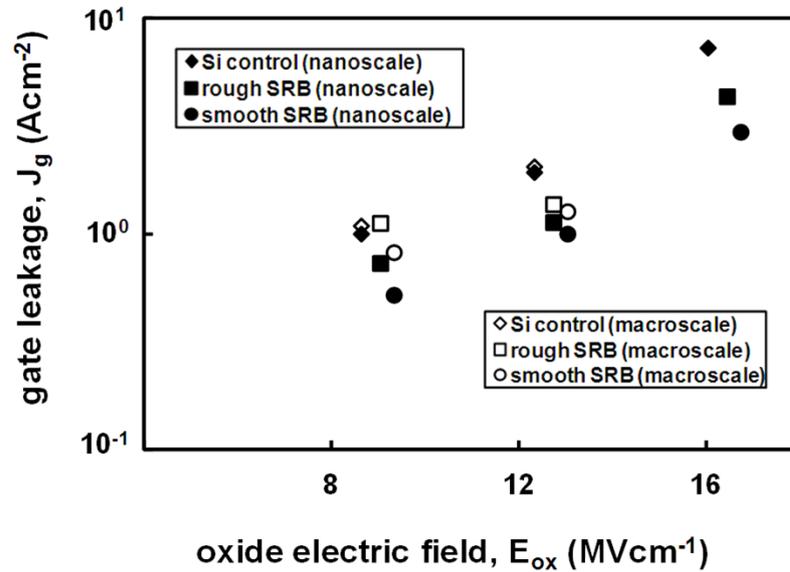
Figure 2.31 Comparison of nanoscale J_g obtained by C-AFM with previously reported macroscopic data [75] from similar devices. Macroscopic J_g at E_{ox} = 16 MVcm^{-1} is not shown because the data was not available.

The good correlation between macro and nanoscale variations in gate leakage in the Si control and strained Si devices (Fig. 2.31) demonstrates the accuracy of the nanoscale measurements, including reverse processing and calculation of A_{eff}.

2.5.5 Localised leakage characteristics

The C-AFM can also be operated in the spectroscopy mode where individual *I-V* traces from the tip-sample contact area at different points can be obtained. This is particularly useful when localised information from different features in the surface topography and current images is desired. *I-V* traces obtained using C-AFM in spectroscopy mode were converted to localised J_g-E_{ox} curves using equations 2.10-2.21. This is required to directly compare the nanoscale and macroscale gate leakage trends.

Fig. 2.32 shows localised J_g-E_{ox} curves measured across 25 random points across the gate dielectric using C-AFM in spectroscopy mode. Fig. 2.33 compares the typical nanoscale J_g-E_{ox} curves for Si control and strained Si devices. Si control devices consistently exhibit higher leakage current density (Figs. 2.32 and 2.33) and reach the current limit of the measurement setup (100 pA) before strained Si devices. Between the two strained Si devices, rough SRB devices exhibit higher leakage than the smooth SRB devices (Figs. 2.32 and 2.33). Some of the J_g-E_{ox} traces in Fig. 2.32 may not follow this trend. This is due to the fact that these curves are point measurements and are indicative of the A_{eff} at that point and do not represent an averaged out leakage behaviour. Some points on the gate dielectric of the Si control devices may be more resilient to electrical stressing compared with strained Si devices. However, on the basis of the histogram shown in Fig. 2.34 it can be concluded that majority of the points on the gate dielectric of the Si control device show higher leakage (at E_{ox} = 16 MVcm^{-1}) compared with the majority of points on the gate dielectric of strained Si devices. This also applies when rough and smooth SRB strained Si devices are compared.

Similar to the macroscopic case (Fig. 2.7), the nanoscale characteristics show improved leakage in strained Si devices compared with Si control devices. Strained Si devices with a smooth dielectric interface exhibit improved leakage characteristics than those on the rough SRB.
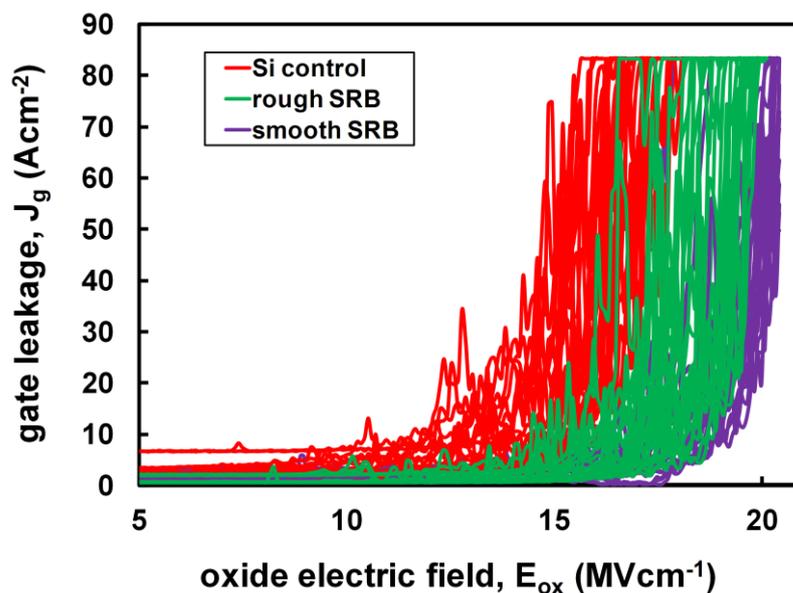
Figure 2.32 Nanoscale J_g**-**E_{ox} **curves from 25 random locations across the deprocessed gates of Si control, rough SRB and smooth SRB strained Si devices obtained using C-AFM in spectroscopy mode.**
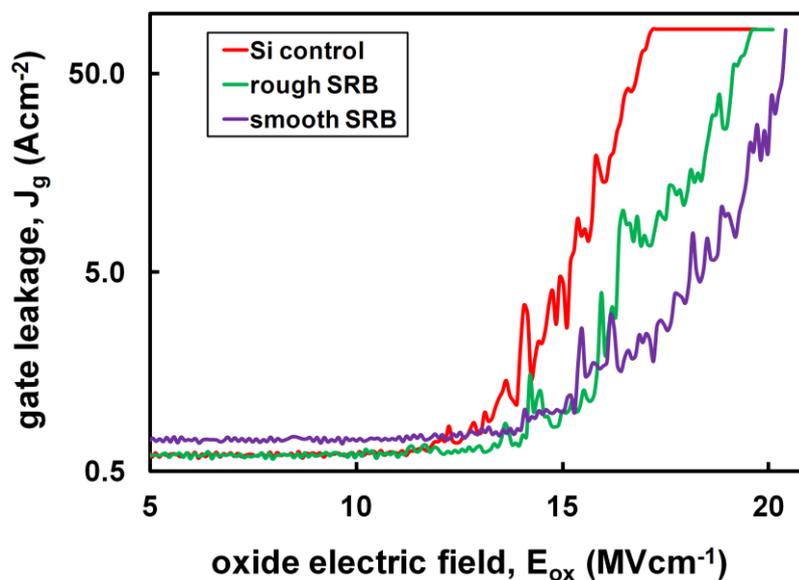
Figure 2.33 Typical J_g**-**E_{ox} **curves for Si control, rough SRB, and smooth SRB strained Si devices obtained by C-AFM.**
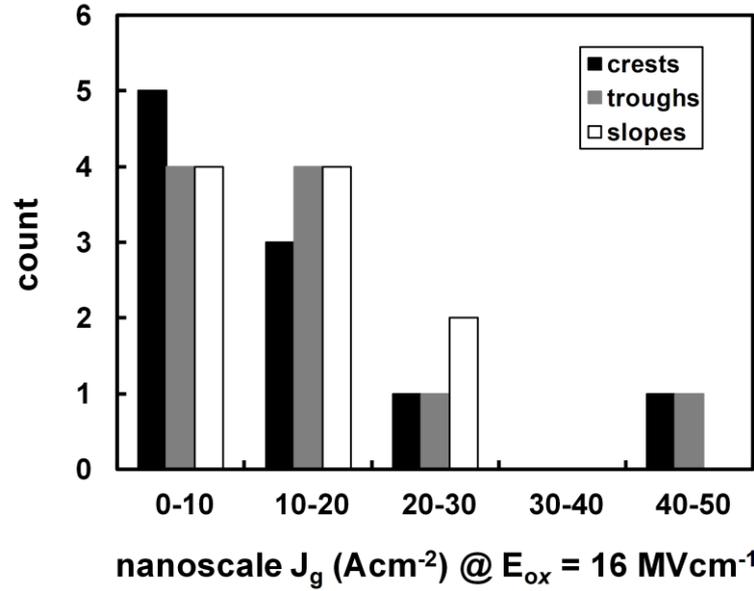
Figure 2.34 Histogram comparing the level of nanoscale J_g at E_{ox} = 16 MVcm^{-1} for Si control and strained Si devices. The high field of 16 MVcm^{-1} was chosen as the J_g-E_{ox} curves in Fig. 2.27 clearly highlight the differences in the level of J_g for the three different devices.

2.5.6 Localised variations in dielectric thickness

The localised J_g-E_{ox} curves shown in Fig. 2.32 can be used for assessing the uniformity in the dielectric thickness. Fig. 2.35 shows the F-N plots of the typical leakage curves shown in Fig. 2.33. Linear behaviour at high fields indicates the dominance of the F-N leakage at such fields.

In order to determine t_{ox} at the nanoscale, J_g-E_{ox} curves of Fig. 2.32 have been superposed by model leakage curves in the F-N regime. F-N leakage is E_{ox} dependent and since E_{ox} varies with t_{ox} (equations 2.8 and 2.21), leakage in the F-N regime can be used to estimate t_{ox}, since all other parameters are known and assumed as constant. The F-N leakage current density model is described by the following equation [97]:

$$J_{FN} = AE_{ox}^2 \exp\left(-\frac{B}{Eox}\right),$$
2.22

where, A and B are expressed as,

$$A = \frac{q^3 \left(\frac{m}{m_{ox}}\right)}{8\pi h \varphi_B} = 1.54 \times 10^6 \left(\frac{m}{m_{ox}}\right) \frac{1}{\varphi_B} \qquad \left[\frac{A}{MV^2}\right] \qquad \textbf{2.23}$$

$$B = \frac{8\pi \sqrt{2 m_{ox} \varphi_B^3}}{3qh} = 68.3 \sqrt{\frac{m_{ox}}{m}} \varphi_B^3 \qquad \left[\frac{MV}{cm}\right] \qquad \textbf{2.24}$$

In equations 2.22-2.24, J_{FN} is the gate leakage current density in the F-N regime, m_{ox} is the effective electron mass in the dielectric, φ_B is the potential barrier height and h is the Planck's constant. The values of m_{ox} and φ_B for Si control and strained Si devices have been included in Table 2.3 [75, 189].

A similar approach of determining thickness of thermally grown SiO_2 on blanket layers of bulk-Si by semi-empirical modelling of C-AFM sweeps in the F-N regime has been reported before [184, 190]. In this chapter, localised variations in t_{ox} on bulk-Si and strained Si channels in fully processed devices are presented.
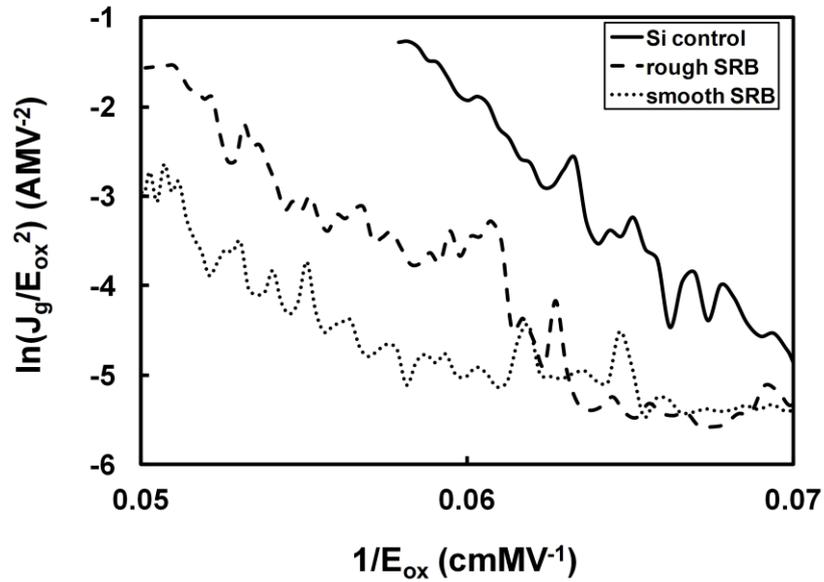
Figure 2.35 F-N plot of the typical leakage curves for Si control and strained Si devices in Fig. 2.33. Linear behaviour at high fields indicates the dominance of F-N leakage.

Table 2.3 Parameters used for calculating model leakage curves in the F-N regime [75, 189]. The free electron mass is represented by *m*.

Device	m_{ox}	φ_B (eV)
Si control	0.4m	3.30
strained Si (20% Ge in the SRB)	0.4m	3.42

Fig. 2.36 shows the experimental J_g-E_{ox} curves for Si control and strained Si devices superposed on calculated F-N model curves. For each of the three devices, the highest and the lowest leakage curves have been shown after fitting with model curves. This provides the maximum range of variation in t_{ox} and is easier to view. Assuming all other parameters as constant, the results of F-N fitting indicate that for the Si control devices, t_{ox} varies from 2.54 to 2.92 nm. This variation is 2.65 to 3.03 nm for rough SRB and 2.74 to 3.06 nm for smooth SRB strained Si devices. These values indicate a highly uniform dielectric.
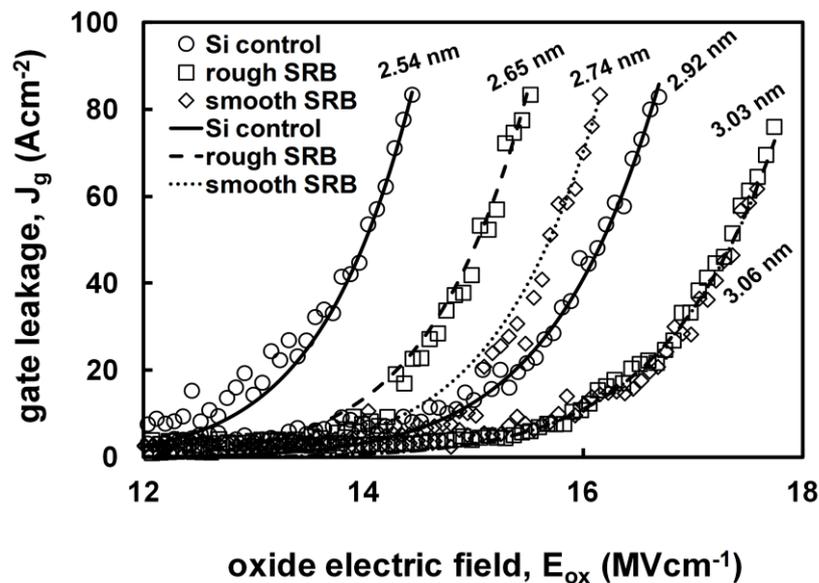
Figure 2.36 Experimental nanoscale gate leakage responses modelled in the F-N regime for different values of t_{ox}. F-N model curves are represented by lines while symbols show the experimental data.

The uniformity of t_{ox} is further demonstrated by the overall variation in t_{ox} as shown in Fig. 2.37. For Si control, rough SRB and smooth SRB strained Si devices, the variation in t_{ox} has been found to be 2.69 ± 0.08 nm, 2.79 ± 0.09 nm and 2.84 ± 0.09 nm, respectively. These values of t_{ox} are in close agreement with the macroscopic value of 2.7 nm. Fig. 2.37 shows that even in the presence of large scale crosshatch undulations in rough SRB devices, dielectrics with a uniform thickness can be obtained.
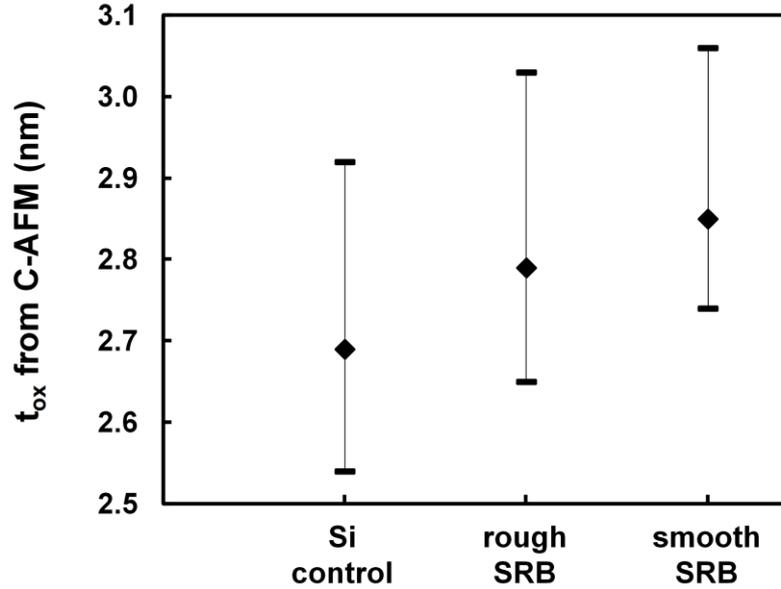
Figure 2.37 Nanoscale variations in t_{ox} (< 4 Å) obtained by the superposition of experimental leakage curves on calculated F-N model curves. Nanoscale value for t_{ox} is in agreement with the macroscopic value of 2.7 nm.

The values of φ_B used for obtaining the model leakage curves in Fig. 2.36 were verified by using the F-N plots in Fig. 2.35. Equation 2.22 can also be written as:

$$\ln\left(\frac{J_{FN}}{E_{ox}^2}\right) = \ln A - \frac{B}{E_{ox}}, \qquad \textbf{2.25}$$

Equation 2.25 represents the linear F-N plot as an equation of a straight line with slope equal to −B and an intercept equal to ln(A). Consequently, the slope of the F-N plot will yield B which will provide a value of φ_B in accordance with equation 2.24. Linear fitting of the F-N plots in Fig. 2.35 is shown in Fig. 2.38. The values of slope, intercept and φ_B are also indicated in Fig. 2.38. The values of φ_B obtained by linear

fitting have been found to be 3.38 eV, 3.30 eV and 3.36 eV for Si control, rough SRB and smooth SRB strained Si devices, respectively (Fig. 2.38). These values are in close agreement with the values of φ_B included in Table 2.3.
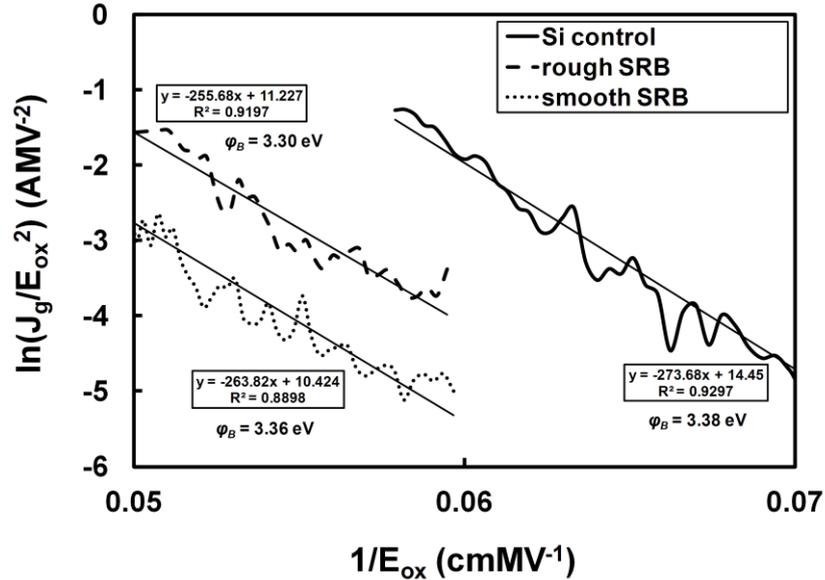
Figure 2.38 Linear fitting of the F-N plots in Fig. 2.35 along with the extracted values of φ_B.

2.5.7 Variation in leakage and dielectric thickness along the crosshatch

Fig. 2.39 compares the J_g-E_{ox} curves from crests, troughs and highly sloped regions of crosshatch undulations in rough SRB devices. In total, 10 sweeps from each region of the crosshatch morphology were obtained and are shown in Fig. 2.39. No significant difference between the individual leakage curves from different regions of the crosshatch undulations was observed. This is further confirmed by the histogram in Fig. 2.40 which compares the nanoscale J_g at $E_{ox} = 16$ MVcm^{-1} across the different regions of crosshatch morphology. Figs. 2.39 and 2.40 also indicate that the dielectric thickness is highly uniform across different regions of the crosshatch undulations.

Localised analysis of uniformity in t_{ox} (sections 2.5.6 and 2.5.7) has eliminated it as a factor responsible for the different device-level leakage behaviour of the two strained Si devices (Fig. 2.7). C-AFM imaging has shown that leakage follows the large scale crosshatch undulations. This implies that the enhanced leakage in rough SRB devices

compared with smooth SRB devices is largely due to the increased roughness across the undulating slopes of the crosshatch since t_{ox} is fairly uniform. Additionally strain fluctuations and Ge out-diffusion from the underlying SRB may also be responsible for enhanced leakage in rough SRB devices.
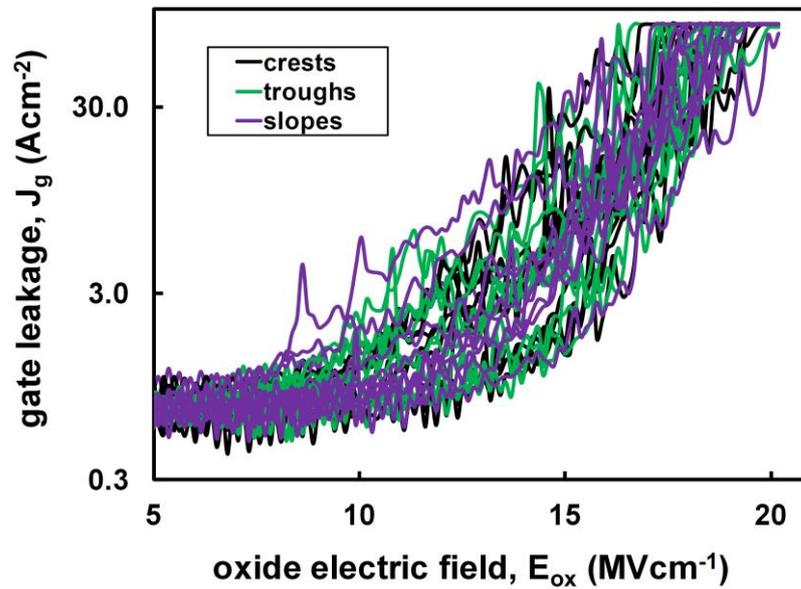
Figure 2.39 Nanoscale J_g-E_{ox} sweeps obtained from crests, troughs and steep slopes of the crosshatch undulations.
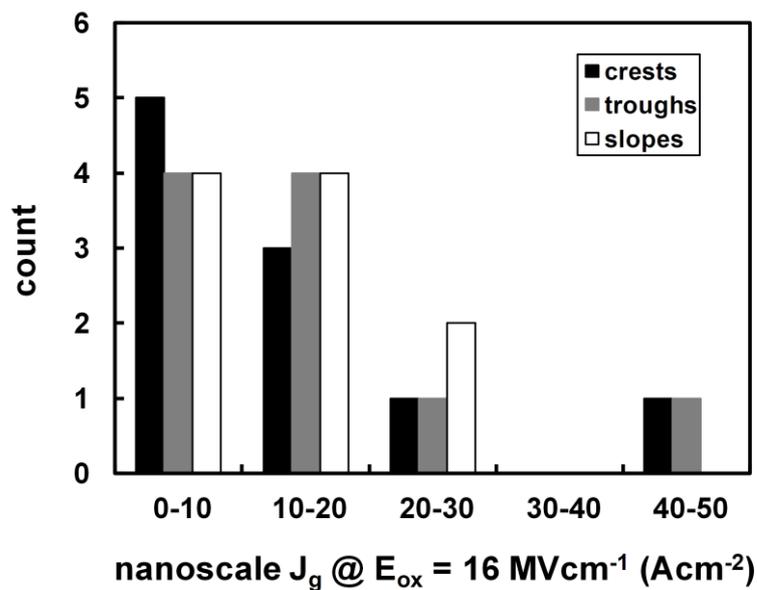
Figure 2.40 Histogram comparing the level of nanoscale J_g at E_{ox} = 16 MVcm^{-1} across the different regions of crosshatch undulations.

2.5.8 C-AFM mapping of broken gate dielectrics

Fig. 2.41 shows the topography and current AFM maps from electrically stressed gates from each set of devices following de-processing. The devices were stressed at E_{ox} = 18 MV cm^{-1} (section 2.3.1). On every type of device, electrical stress resulted in a structural weakening of the gate dielectric in the form of holes which are observed as black spots on the topography images. Such holes act like leakage spots, and generate high current regions in the corresponding current maps (Fig. 2.41). The leakage spots in all the devices (Fig. 2.41) are a consequence of the devices reaching hard breakdown during electrical stressing. Although Fig. 2.41b shows that there are more bright spots on the rough SRB compared with Si control, stressed gates on the Si control samples continued to show higher rms leakage (~ 16 nA) than both strained Si counterparts (11.2 nA for the rough SRB device and 7.5 nA for the smooth SRB device). This shows that the rough SRB device (with large scale crosshatch roughness) has more sites which are prone to breakdown than other devices. Although current values do not directly represent leakage through the gate dielectric since the C-AFM tip is able to probe through the dielectric holes into the semiconductor beneath the gate, the rms current values obtained in stressed dielectrics can be considered a measure of the dielectric structural damage induced by the electrical stressing on the devices. During poly-Si removal, KOH may have filtered through the breakdown spots in the gate dielectric reaching the substrate beneath. The etching of the Si beneath the dielectric resulted in increased depth of the holes. Figs. 2.28 and 2.41b suggest that the topography dependence of the gate leakage in rough SRB devices is lost beyond hard breakdown since the leakage spots in Fig. 2.41b do not align with the crosshatch pattern of the substrate as they appear in Fig. 2.28 prior to stressing. Instead, they have a random distribution similar to the current map of Si control devices and exhibit no dependence on topography.

Only a few leakage spots are observed for the electrically stressed smooth SRB strained Si device in Fig. 2.41c. This result is also in good agreement with the hard breakdown leakage characteristic measured macroscopically for the same device where the leakage current does not exceed the equipment compliance limit shown in Fig. 2.9. Fig. 2.41c therefore also demonstrates the improved integrity of gate dielectrics of devices fabricated on the smooth SRB compared with those on the rough SRB material.

Fig. 2.42 is an example of a breakdown spot on the smooth SRB device. The holes can have breakdown area of thousands of nm^2 which is comparable to breakdown areas reported before on stressed bulk-Si [139, 191, 192].
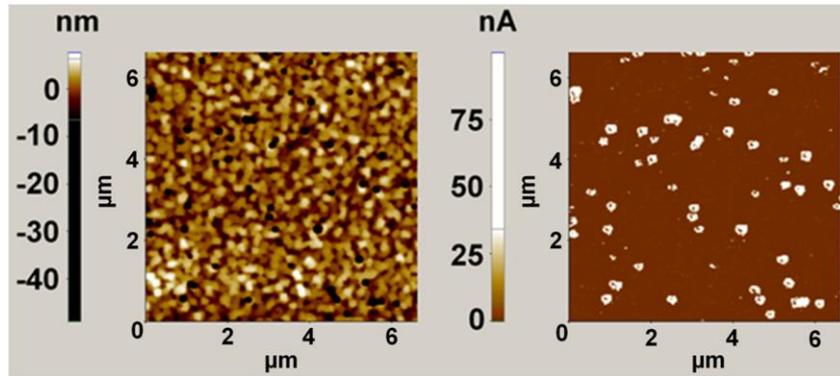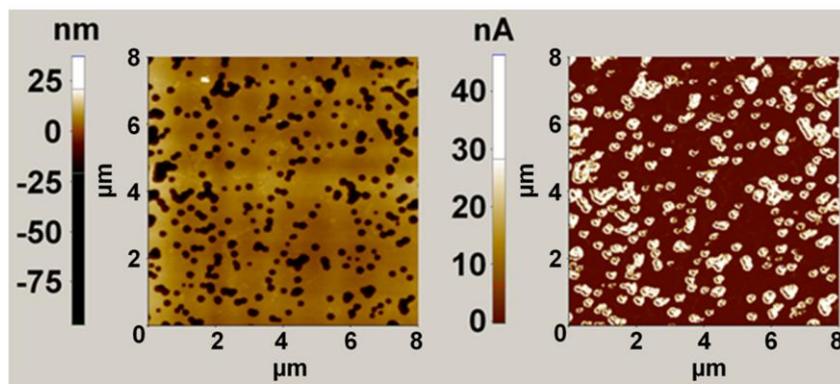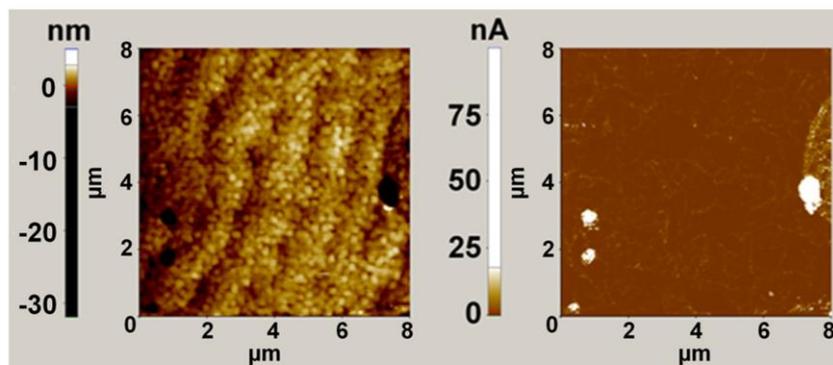
Figure 2.41 C-AFM maps of the (a) Si control, (b) rough SRB, and (c) smooth SRB strained Si devices at a dc bias of 2 V after hard breakdown.
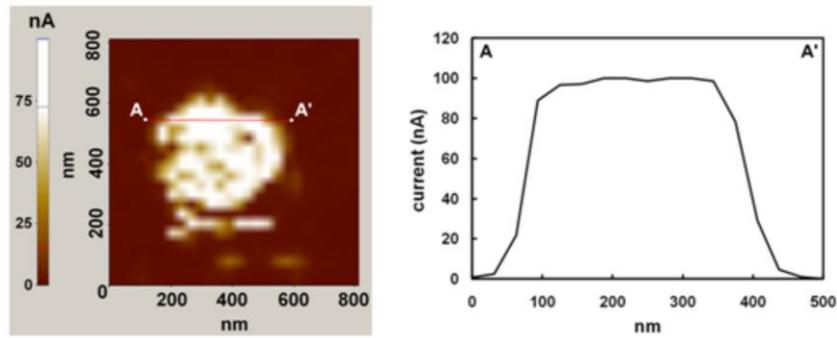
Figure 2.42 C-AFM map of a localised breakdown spot on the smooth SRB strained Si devices exhibiting significant increase in current.

2.6. Summary

A study investigating the impact of substrate morphology on gate dielectric leakage of high mobility MOSFETs has been carried out. It is demonstrated that semiconductor topography in the form of crosshatching can influence the distributions of leakage in the gate dielectric of MOS devices. Through carefully developed reverse processing procedures, correlation has been established between morphology measured by AFM measurements, nanoscale gate leakage data obtained by C-AFM and macroscopic electrical measurements of strained Si/SiGe transistors exhibiting various levels of gate leakage. C-AFM measurements on de-processed MOSFETs demonstrate that the compromised leakage and dielectric breakdown characteristics of strained Si devices fabricated on rough SiGe SRBs arises from large scale crosshatching, and that leakage correlates with the regular crosshatch morphology. Gate leakage in Si control devices and devices fabricated on smooth SiGe SRBs (which avoids the crosshatch pattern) does not appear to relate to any features on the underlying substrate. Both sets of strained Si devices have the same level of channel strain (0.75%) for the same Ge content in the SRB (20%). Since the crosshatch pattern is evident in many SRBs, including SiGe and GaAs, the results have implications for several material systems. Furthermore since the variations in leakage arise from the substrate, the findings are relevant for many dielectrics, whether deposited or grown.

The gate leakage has been quantified at the device-level (macroscopically) and compared with nanoscale measurements on the same devices using C-AFM after reverse-processing down to the SiO_2 gate dielectric. Using the Hertzian model to

account for the AFM tip size there is a good agreement between macroscopic and nanoscale measurements, confirming the validity of the method. At both macro and nanoscale, the larger electron affinity and smaller transverse effective mass lead to lower leakage in strained Si n-MOSFETs compared with bulk Si control devices. However a smooth SRB is required to obtain the full benefits of strained Si and avoid the enhanced leakage identified on the sloping edges of the crosshatched surface. The maximum reduction in tunnelling current observed due to strain was 31 % which was reduced to 17 % for non-optimised SRB growth. Nanoscale analysis has also shown that the dielectric thickness is nearly similar in all the devices studied. It has been shown that even in the presence of large scale crosshatch morphology in rough SRB devices, dielectrics with a uniform thickness can be obtained.

Dielectrics fabricated on both types of SRB exhibit improved time to breakdown compared with the Si controls, with the smooth SRB devices displaying the greatest resilience to breakdown compared with the rough SRB and Si control device. Post hard breakdown, leakage was no longer found to correspond to the crosshatch pattern in the rough SRB. The improved leakage and dielectric breakdown characteristics measured on a nanoscale are also in agreement with previous macroscopic studies of dielectrics on strained Si.

From the results presented it is evident that improvements in epitaxy techniques used in the fabrication of new generations of devices will result in extended device lifetime governed by dielectrics. It is possible that other dielectric materials may undergo similar degradation on rough substrates. Since the leakage properties are related to the substrate material the results are relevant to other dielectrics formed on epitaxial material prone to strain induced roughening. Furthermore the results explain how epitaxial surface roughness severely impacts gate dielectric quality even where the length scale of the roughness is much greater than the size of devices.

Chapter 3. Nanoscale Analysis of Interface Trap Density in Strained Si Devices

The quality of the interface between dielectric and semiconductor in MOS devices is of great importance since it directly affects electrical performance and reliability. In this chapter, the effect of strain induced surface roughness on D_{it} is assessed. Localised variations in D_{it} for strained Si devices are studied at a nanoscale using SCM. These measurements, similar to J_g results in the preceding chapter have been related to the underlying substrate morphology using capacitance maps and localised individual differential capacitance (dC/dV) sweeps. The good correlation between macroscale and nanoscale trends in D_{it} validates the measurement setup and analysis. Regions where D_{it} may be enhanced have been identified on the basis of individual dC/dV sweeps from localised regions of interest. Localised behaviour in D_{it} from crosshatch undulations is similar to variations in J_g shown in chapter 2. The morphological dependence of D_{it} in strained Si devices shown here is relevant for many dielectric and semiconductor material systems.

3.1 Background

Atoms on the surface of a semiconductor behave differently than the ones in the bulk as they are not chemically satisfied by similar atoms [193]. These unsatisfied states at the surface can act as sites for trapping charge carriers. Electron spin resonance (ESR) measurements have identified these traps at the interface as unsatisfied dangling bonds [194]. Fig. 3.1 shows the dangling bonds designated as P_{b0}, and P_{b1} centres on (100) Si oriented surface [195]. Fig. 3.2 shows the bulk and interface traps for a SiO_2/Si interface in an n-MOS device. Interface traps have energy levels inside the silicon forbidden bandgap and are in direct electrical contact with the underlying silicon. Various factors including oxidation and annealing conditions [196-198], dielectric thickness [199], channel thickness in strained Si devices [107] and interface roughness [199, 200] dictate the level of interface states. External electrical bias or irradiation can also increase the level of trap centres at the interface [201-203]. Charge carriers under external electrical stress can tunnel through these traps at the interface [204]. Gate dielectrics subjected to high field electrical stressing exhibit high leakage current compared with the pre-stress

condition. This enhancement in gate current is referred to as stress induced leakage current or SILC [97]. For thin dielectrics, at low fields SILC is commonly modelled as trap-assisted tunnelling [205-207] as it is usually the dominating mechanism. In relatively thick dielectrics, presence of several traps can enhance SILC and eventually cause breakdown [208]. In addition to tunnelling current, interface traps are also responsible for mobility degradation at low fields. Coulomb scattering due to interface traps is the dominant mobility degradation mechanism at low fields (Fig. 1.4). These factors highlight the importance of a good quality interface between the dielectric and the channel.
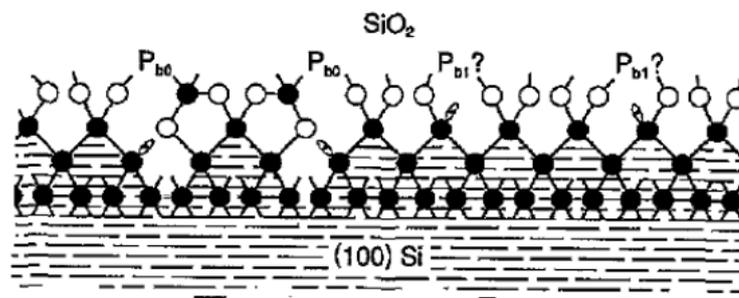
Figure 3.1 Dangling bonds at the surface of (100) Si, designated as P_{b0} and P_{b1} centres [195].
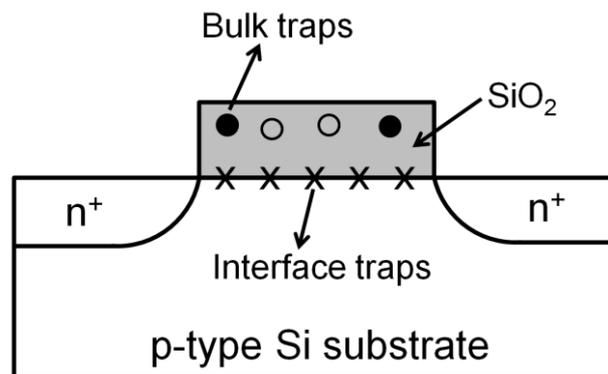
Figure 3.2 Bulk and interface traps in SiO_2 of an n-MOS structure.

Dielectric interface quality in strained Si/SiGe devices is not always as good as bulk-Si devices (section 1.4.3). Strained Si devices generally exhibit higher levels of D_{it} compared with bulk-Si devices [75, 107, 109, 209]. Strained materials can exhibit high levels of surface roughness compared with bulk-Si (section 1.3.2). It has been widely

reported before that the increase in surface roughness leads to increased levels of D_{it} for bulk-Si as well as strained Si devices [75, 85, 199, 200, 210, 211]. Simultaneously processed strained Si devices have shown different levels of D_{it} in spite of identical strain and channel thickness [75]. This difference has been attributed to different levels of SRB induced surface roughening. Improvement in D_{it} also results in reduced mobility degradation (reduced Coulomb scattering) at low fields for smooth SRB devices compared with those processed on rougher substrates [75]. Hence any possibility to reduce D_{it} is an advantage.

In addition to surface roughness, strained Si devices often suffer from out-diffusion of Ge from the underlying SRB during high thermal budget processing. The gate dielectric interface quality is severely affected by the out-diffused Ge atoms at the interface [85, 107, 212].

It has been shown that increasing Ge content in the underlying SRB (which increases Ge diffusion and surface roughness) degrades D_{it} in strained Si devices [85, 107, 211, 213, 214].

High-κ dielectrics are a common choice for strained Si/SiGe devices, especially because Ge based devices do not have a natural native oxide like Si. High-κ dielectrics should alleviate some of the aforementioned issues. However, in spite of all the advantages offered by high-κ dielectrics, obtaining a good quality interface with the underlying strained Si channel remains challenging (section 1.4.2). Irrespective of the dielectric used, alternate channel materials such as strained Si/SiGe appear to still influence D_{it} [75, 107, 109, 209].

Nanoscale C-AFM measurements have already shown that strained Si devices exhibiting conventional large scale crosshatch undulations have degraded gate leakage across steep slopes (section 2.5). Smooth SRB devices exhibit improved levels of D_{it} compared with rough SRB devices [75]. However, it is not clear if localised morphological features are responsible for different macroscopic D_{it} signatures. This is because roughness correlation lengths are very different. However, the results presented in chapter 2 have shown that large scale roughness does influence gate leakage properties. In this chapter, nanoscale D_{it} analysis in strained Si devices with varying surface roughness is assessed. SCM, like C-AFM is an electrical variant of AFM based SPM techniques. It is sensitive to localised capacitive variations. SCM has been extensively developed as a successful technique for nanoscale dopant profiling [215-218]. It also finds application in the localised characterisation of insulating layers on

semiconductors [141, 142, 219-221]. However, it has never been used to study specific regions of surface roughness.

In this chapter, SCM analysis on localised regions of surface roughness in fully processed strained Si devices is presented. Material growth, device fabrication and reverse processing of the devices analysed in this chapter have been explained in sections 2.2.1, 2.2.4 and 2.4 respectively.

3.2 Macroscopic high frequency capacitance analysis

Device-level *C-V* characteristics were obtained using the Agilent 4294A Impedance Analyzer (in two-probe configuration) on large area capacitors (10^{-4} cm^{-2}). In total, 3 large area capacitors ($100 \times 100 \ \mu m^2$) of each type were analysed. V_g was swept from accumulation (-3V) to inversion (+3V) with substrate, source and drain all shorted together to ground. A certain value of V_g balances the workfunction difference, dielectric charges and potential drop in the semiconductor. This value of V_g is known as the flatband voltage (V_{FB}) as semiconductor energy bands are flat at this voltage (section 1.1.1). Hence at V_{FB} charge neutrality is maintained. Consequently, V_{FB} is a measure of charges in the dielectric. Variations in V_{FB} usually result in a parallel shift in the *C-V* curve. In addition to parallel shift, dependence of interface trapped charges on V_g also manifests in the form of a stretch-out of the *C-V* curve. Typical parallel shift and stretch-out of a *C-V* curve in the presence of dielectric charges is shown by the simulated curves (Fig. 3.3) obtained using the MOSCap software [222].

Fig. 3.4 shows the device-level (macroscopic) *C-V* curves for Si control and strained Si devices. It can be observed that the *C-V* curves of the three sets of devices with similar t_{ox} and N_{sub} exhibit different parallel shift and stretch-out with respect to each other. This indicates differences in the level of dielectric charges and hence V_{FB} and D_{it}. It can also be observed in Fig. 3.4 that *C-V* curves of the two strained Si devices with different surface roughness exhibit different parallel shift and stretch-out in spite of having same level of strain and channel thickness. It has been shown before on the basis of macroscopic conductance measurements that Si control devices exhibit lower levels of D_{it} (~ 3 x 10^{11} eV^{-1}cm^{-2}) compared with the two strained Si devices [75]. Between the two strained Si devices rough SRB devices exhibit higher D_{it} (~ 5 x 10^{11} eV^{-1}cm^{-2}) compared with smooth SRB devices (~ 4 x 10^{11} eV^{-1}cm^{-2}) [75]. Fig. 3.5 shows this trend in D_{it} for Si control and strained Si. Diffusion of Ge to the strained Si surface and

increase in surface roughness has been identified as the reason for increased levels of D_{it} in strained Si devices. The difference in D_{it} for the two sets of strained Si devices is expected to be due to increased surface roughness in the rough SRB devices which is a direct consequence of the substrate quality [75, 85]. However, the reason behind the increase in D_{it} due to large scale surface roughness in strained Si/SiGe devices has never been fully understood.

Macroscopic C-V and D_{it} measurements (similar to Figs. 3.3-3.5) average out any localised trends and are indicative of the entire area under study. This results in the need of a high spatial resolution technique such as SCM which can relate localized D_{it} trends with substrate surface morphology.
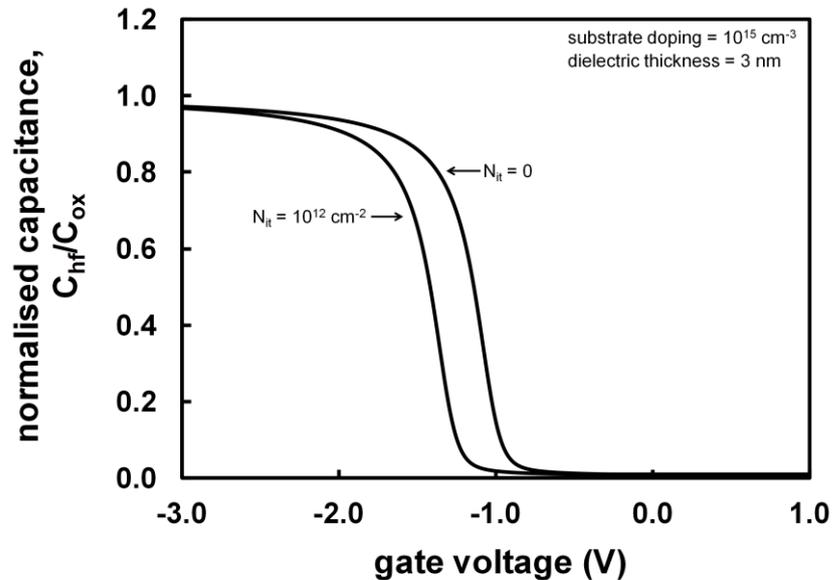
Figure 3.3 Parallel shift and stretch-out of a _C-V_ curve in the presence of dielectric charges. _C-V_ curves simulated using the MOSCap software [222] for an Al gate (4.10 eV) n-MOS capacitor. Symbols: _C_{hf}_: High-frequency capacitance, _C_{ox}_: dielectric capacitance, _N_{it}_: trapped charge density. Simulation parameters: _N_{sub}_ = 10^{15} cm^{-3}, _t_{ox}_ = 3 nm, _N_{it}_ = 10^{12} cm^{-2}.
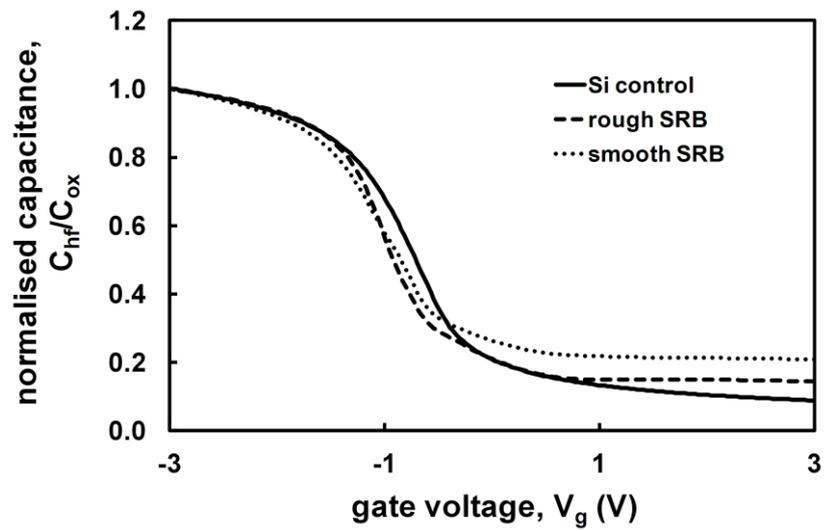
Figure 3.4 Macroscopic *C-V* characteristics for Si control and strained Si devices.
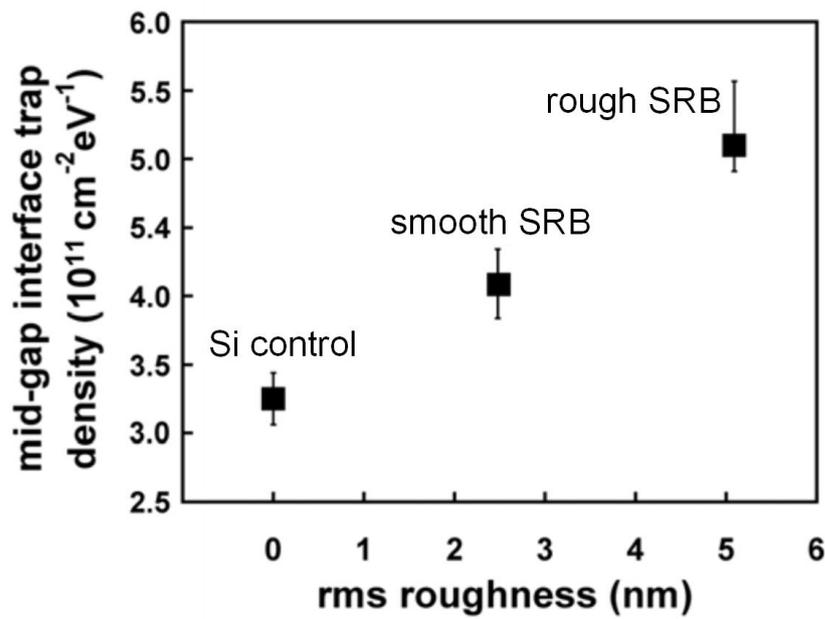
Figure 3.5 Mid-gap D_{it} (measured using the conductance method) as a function of rms surface roughness for Si control and strained Si devices [75].

3.3 Nanoscale analysis of interface quality using SCM

Detailed operation of the SCM measurement setup is explained in section 3.3.1 followed by the nanoscale analysis of dielectric/semiconductor interface quality in strained Si and Si control devices.

3.3.1 SCM measurement setup

The ITRS 2010 update has listed SCM among other SPM techniques as one of the next generation potential defect inspection technique [21]. SCM measures the change in capacitance between the probe tip and the underlying semiconductor (ΔC) in response to an applied ac bias (V_{ac}) at a given dc bias (V_{dc}). In addition to differential capacitance images, SCM in spectroscopy mode is capable of generating dC/dV curves as a function of V_{dc}. Such dC/dV curves are similar to the differentiated form of *C-V* curves commonly measured by the conventional device-level techniques. Fig. 3.6 shows the typical dc bias dependence of capacitance and dC/dV curves for p-MOS and n-MOS capacitors.

The operation of SCM is based on the working of a MOS capacitor (section 1.1.1). V_{dc} applied at the gate electrode controls the operation of the capacitor. In an n-MOS capacitor, negative V_g accumulates holes in the underlying semiconductor. Under strong accumulation, capacitance is only due to the dielectric. On the other hand, positive V_g depletes holes and attracts the electrons. During depletion, total capacitance is due to the dielectric as well as the channel. In SCM, the conductive probe tip, gate dielectric and the underlying semiconductor model a MOS capacitor, which is shown in Fig. 3.7 along with the equivalent circuit. The total capacitance consists of the fixed dielectric capacitance (C_{ox}) and a variable tip-sample capacitance (C_{tip}). A substrate applied V_{dc} accumulates or depletes the charge carriers while V_{ac} modulates the depletion region and results in a variation in C_{tip} at a given V_{dc}. This change in C_{tip} is monitored during SCM measurements. At a given V_{dc}, the measured SCM signal is proportional to the slope of the *C-V* curve as shown in Fig. 3.8. Hence the SCM signal is commonly known as the ΔC or the dC signal. The SCM image is a representation of the ΔC signal across the scanned area for a given dc bias. The response of this ΔC signal to a wide range of V_{dc} at a localised point can also be obtained by operating SCM in the spectroscopy mode. The ΔC or the dC signal obtained in spectroscopy mode is divided by the rms value of V_{ac}

and is commonly represented as the *dC/dV* signal. This *dC/dV* curve is similar to the differentiated high frequency *C-V* curve.
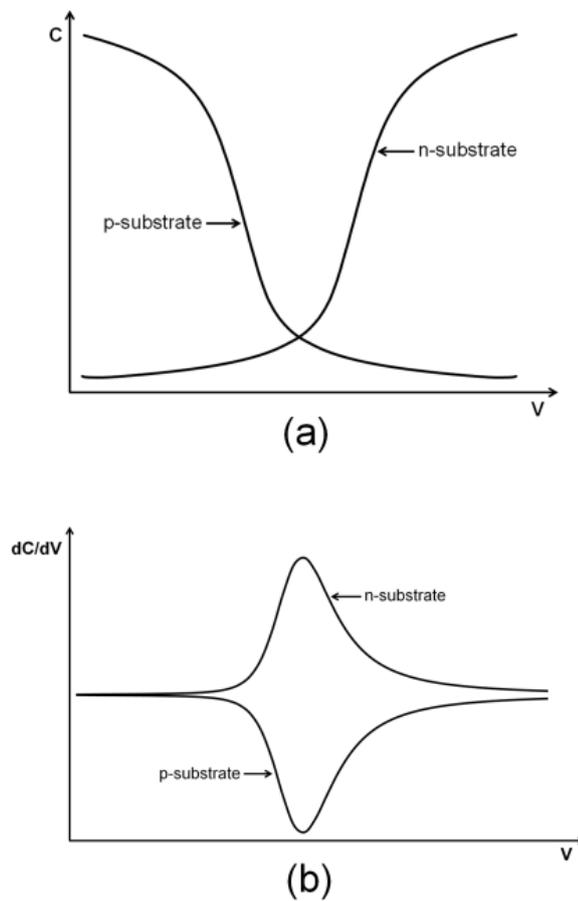
Figure 3.6 Typical (a) *C-V* and (b) *dC/dV* curves for p-substrate and n-substrate MOS capacitors.
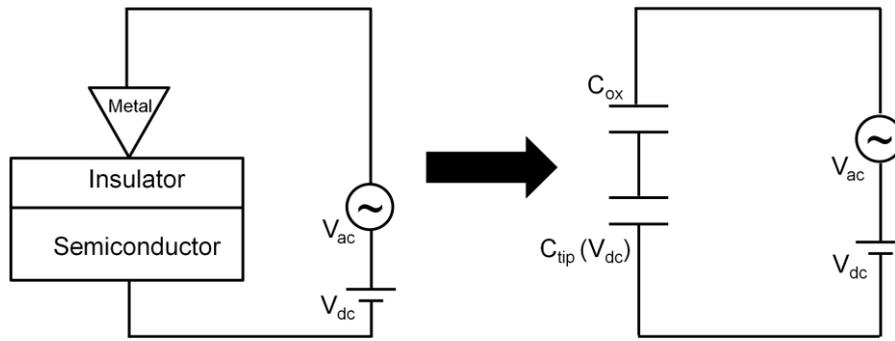
Figure 3.7 MOS capacitor formed during SCM analysis and the equivalent circuit.
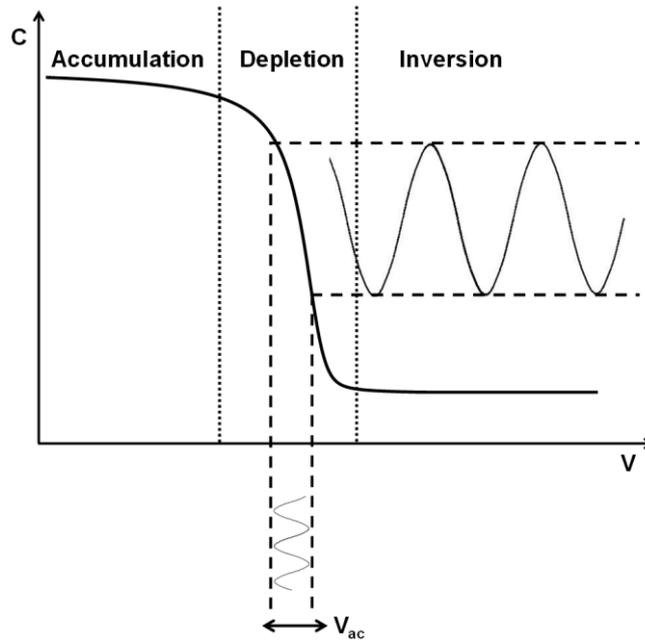
Figure 3.8 Detection scheme of *dC/dV* measurements for an n-MOS capacitor.

The full width at half maximum (*FWHM*) of *dC/dV* sweeps obtained from SCM in spectroscopy mode is a qualitative measure of D_{it} [142, 219, 223] whereas the peak intensity of such sweeps is influenced by N_{sub} and t_{ox} [141, 219, 221]. The value of V_{tip} at which the *dC/dV* response peaks ($V_{tip,\,peak}$) is not necessarily equal to but is close to V_{FB} [223, 224] and hence is an indicator of the polarity and the magnitude of dielectric charges. Fig. 3.9 shows the effect of charges in the dielectric on the *dC/dV* response from SCM. A shift in $V_{tip,\,peak}$ and an increase in *FWHM* can be observed in the presence

of charges in the dielectric. These features of the *dC/dV* curves have been exploited in the past for studying dielectric parameters such as t_{ox}, V_{FB} and D_{it} in semiconductor devices. However, so far only qualitative analysis and relative comparison between different samples has been reported. Stray effects and *dC/dV* data being unitless have made quantitative interpretation difficult. In this chapter, the variation in *FWHM* and $V_{tip,\ peak}$ of *dC/dV* sweeps between and within samples has been used to characterise the interface quality and locate areas where D_{it} may be enhanced in strained Si devices.
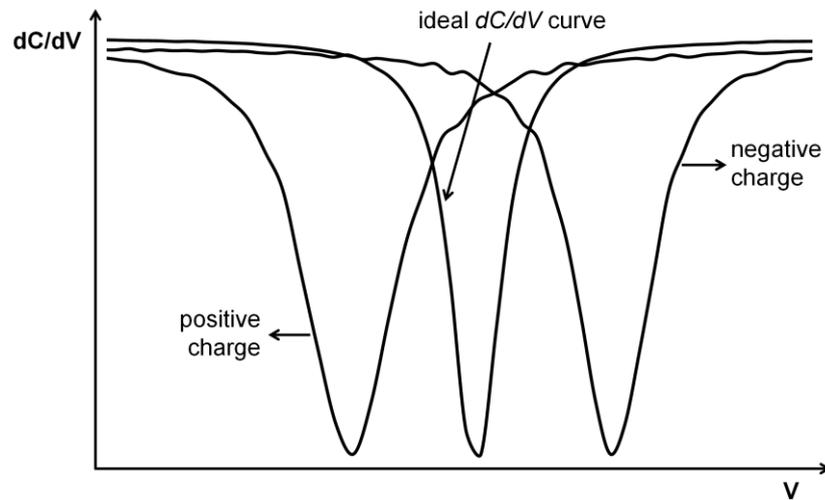
Figure 3.9 Impact of charges in the dielectric on *dC/dV* curves. Parallel shift and increase in width can be observed due to charges of different polarities in the dielectric.

Fig. 3.10 shows the schematic of the setup used for the SCM measurements. The changes in C_{tip} are detected by the capacitance detector which is a part of an electrically shielded resonator. Variations in C_{tip} are processed by an external lock-in amplifier to obtain ΔC images and *dC/dV* sweeps. The resonator also houses a variable capacitor and other RF detection circuitry and operates at high frequencies (~ 1 GHz) supplied by a voltage controlled oscillator (VCO). The resonator comprises a resonance circuitry along with the probe and the sample. During initial calibration, the VCO is swept from -10 V to +10 V to obtain the resonance curve for a given tip-sample system. An operating frequency in the maximum slope region of this resonance curve is selected as this ensures high sensitivity and spatial resolution for the probe. Resonance frequency usually varies for different channel and dielectric materials. Changes in C_{tip} shift the

resonance curve which changes the maximum slope position corresponding to the operating frequency of the resonator as shown in Fig. 3.11. Changes in resonance characteristics change the output from the detector and it is this change in the detector signal which is monitored during scanning to obtain the SCM image.
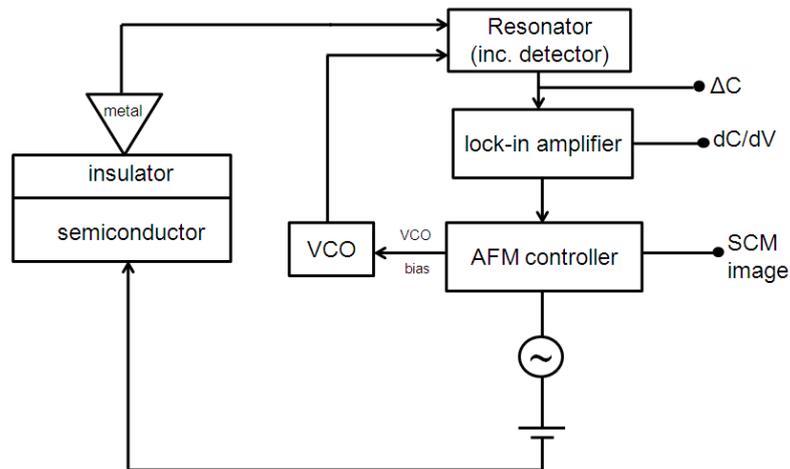
Figure 3.10 Schematic of the SCM measurement setup.
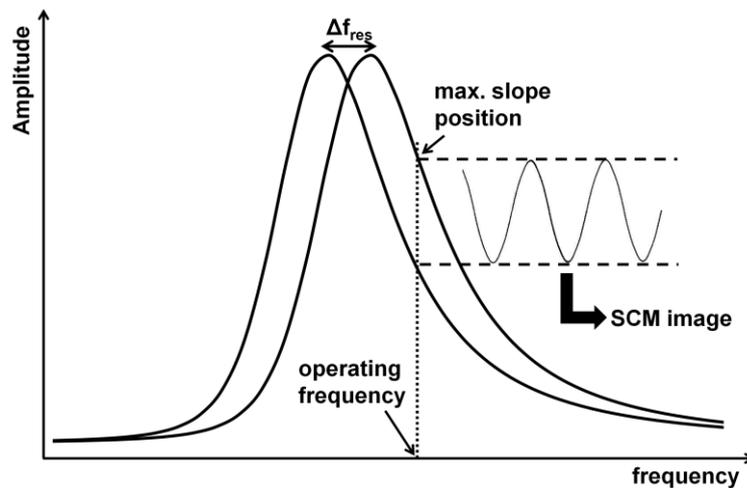
Figure 3.11 Shift in resonance curve of the resonator due to changes in C_{tip}.

Fig. 3.12 shows the SCM tip mounted on the AFM head and connected to the resonator. Fig. 3.13 shows the connected components required for SCM measurements.

The SCM tip is connected to the resonator which is connected to the frame module which houses the VCO and other circuitry. The signal from the VCO is transferred to the resonator for its operation while the detected capacitance signals are transferred from the resonator to the lock-in amplifier for processing via the frame module. Fig. 3.14 shows the SCM components mounted on the AFM for SCM analysis.
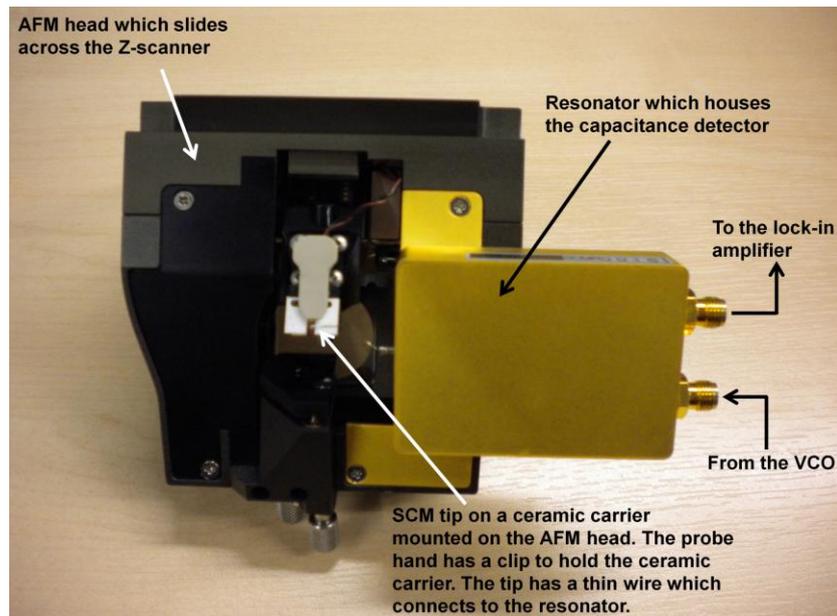
Figure 3.12 The SCM tip on a ceramic carrier mounted on the AFM head and connected to the resonator.
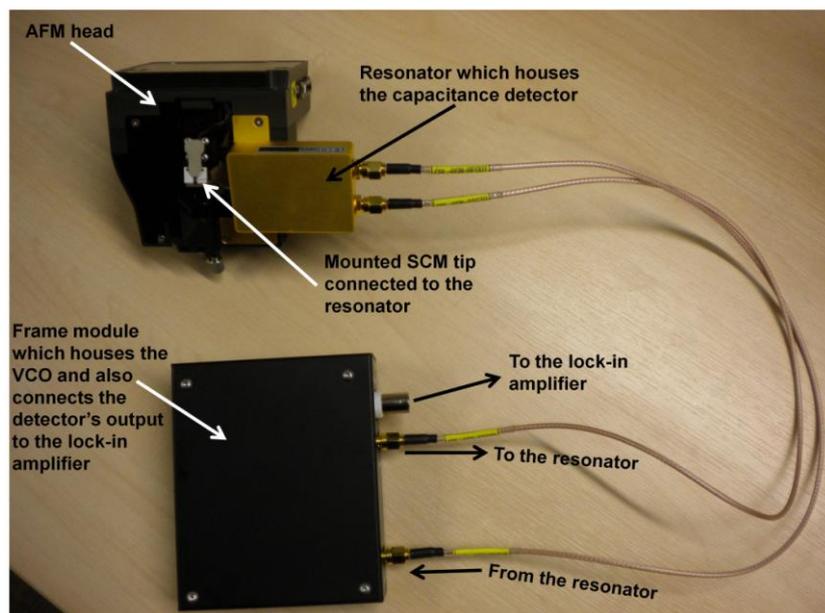
Figure 3.13 Connected components required for SCM imaging.
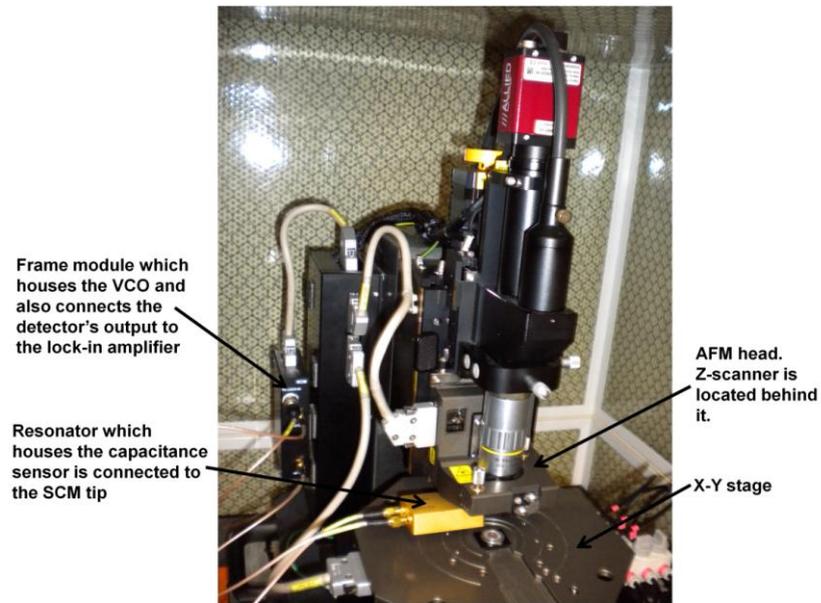
Figure 3.14 SCM components mounted on the AFM inside the isolation box.

The detected signals have been processed by an external SR830 lock-in amplifier by Stanford Research Systems (Fig. 3.15). Lock-in amplifiers are typically used for detecting and measuring very small ac signals which usually have more noise than useful information. Lock-in amplifiers can detect ac signals of the order of nV. These typically use phase sensitive detection to single out components of a signal at a specific reference frequency. Components which have frequency different from the reference signal are rejected and do not affect the working of the lock-in amplifier. In this work, the SR830 provides the external V_{ac} and uses it as the reference signal. Hence the lock-in amplifier selects and amplifies the detected signals which have the same frequency as the input ac signal.

Figure 3.15 The SR830 lock-in amplifier.

As the SCM detector operates at RF frequencies, electro-magnetic radiation from the resonator to the metallic structures in the vicinity causes stray capacitance. The XE-150 SCM used in this work incorporates various features to reduce stray capacitances. These include electrically shielding the resonator, mounting of the probe on a ceramic carrier, minimisation of the length of the wire between the probe and the resonator and optimisation of the size of the opening at the front of the resonator. Other parasitic effects can also produce stray components in the detected signal. These include, distance between successive measurement locations and illumination by the AFM laser etc. Such parasitic effects result in the detected signals having a low signal to noise ratio (SNR) and hence additional processing of the raw SCM data is required.

The SCM maps in this work were obtained at a dc substrate bias of 0 V under ac lock-in conditions of 2 V_{rms} and 20 kHz. The high ac bias of 2 V_{rms} and 20 kHz frequency (f_{ac}) increases the SNR, thereby resulting in better contrast in the SCM image [141, 216]. A high contrast SCM image is critical when analysing localised interface quality at specific regions of the gate. High V_{ac} is not suitable for the traditional SCM application of dopant profiling as a high ac bias degrades the spatial resolution of the measured carrier profile [216]. While obtaining the dC/dV sweeps the dc bias which was applied from the substrate was varied from -1 V to +5 V at 2 V/s. The sweep rate is much higher than the one used during conventional macroscopic C-V measurements to establish equilibrium. The high sweep rate has been used to reduce the response of surface charges to the applied bias thus minimizing their effect on the measured ΔC values [225]. This sweep rate is similar to some of the previously reported SCM analysis of interface traps [142, 219] and carrier profile [225]. The ac bias during these sweeps was reduced to 0.2 V_{rms} to reduce electrical stress during measurement. The phase of the ac signal was set at -90 degrees to obtain the typical U-shaped dC/dV response of p-type substrate MOS devices. This change in phase also required f_{ac} to be increased to 75 kHz to reduce distortion in the dC/dV sweeps. The dC/dV sweeps in the following sections are presented with varying V_{tip}, which has the opposite polarity from V_{dc} which is applied through the substrate.

3.3.2 Effect of surface morphology on capacitance

Figs. 3.16-3.18 show SCM maps from the de-processed gates of three different rough SRB, smooth SRB and Si control devices respectively. In all the SCM maps topography is shown on the left while SCM maps are shown on the right. The dielectrics on Si control exhibit the smoothest topography with $R_q = 0.12 \pm 0.00$ nm while the dielectrics on smooth SRB devices exhibit $R_q = 0.46 \pm 0.05$ nm. The typical crosshatch morphology of rough SRBs propagate on the surface of the thin dielectrics resulting in an rms roughness of 1.69 ± 0.81 nm. The values of R_q and $\Delta_{p\text{-}v}$ for Si control and strained Si devices obtained using SCM have been included in Fig. 3.19. The values of R_q and $\Delta_{p\text{-}v}$ in Fig. 3.19 are in strong agreement with the values obtained during C-AFM scanning (Fig. 2.29).
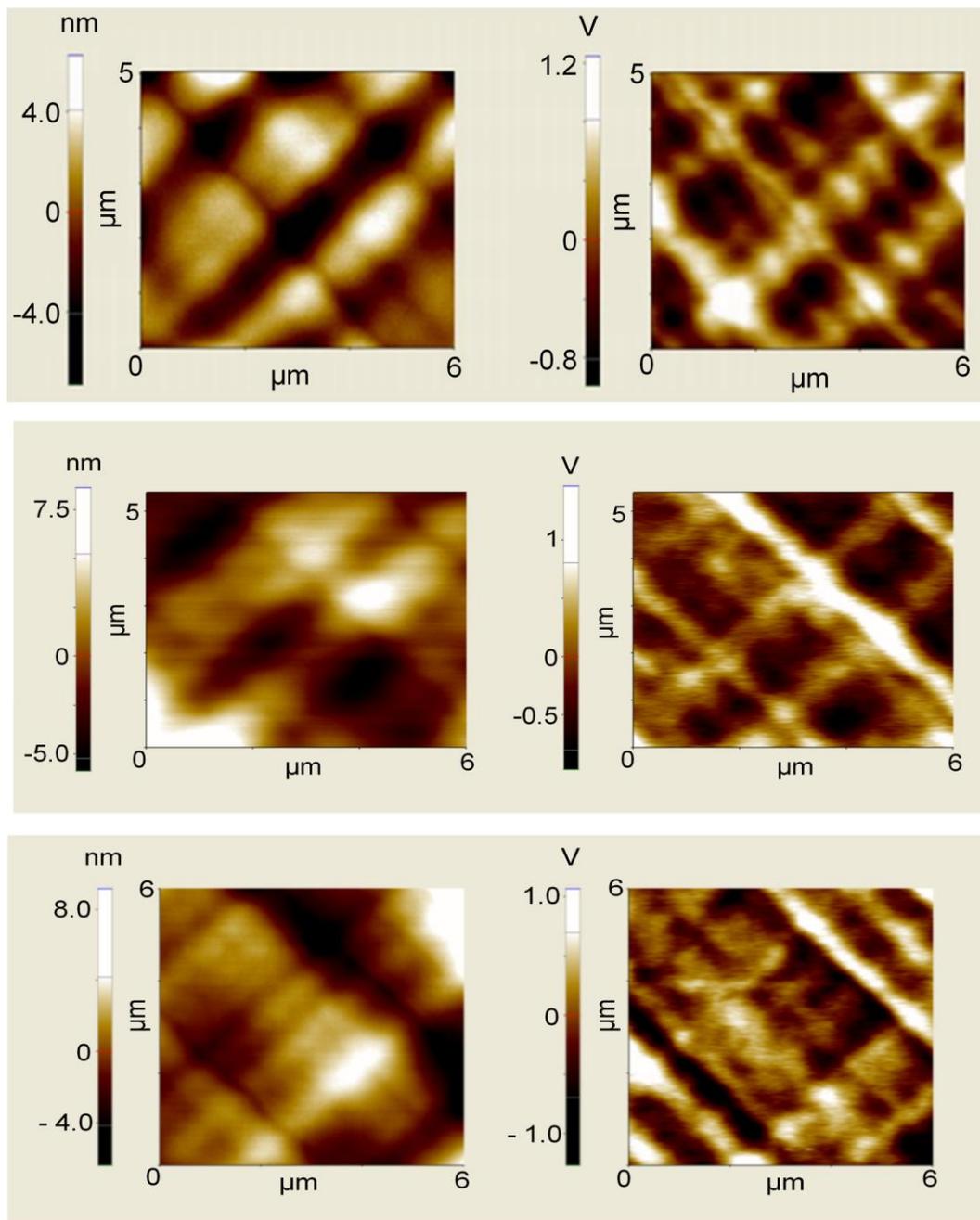
Figure 3.16 Topography (left) and SCM images (right) from the de-processed gates of rough SRB strained Si devices. Parameters: $V_{ac} = 2\ V_{rms}$, $f_{ac} = 20$ kHz, $V_{dc} = 0$V.
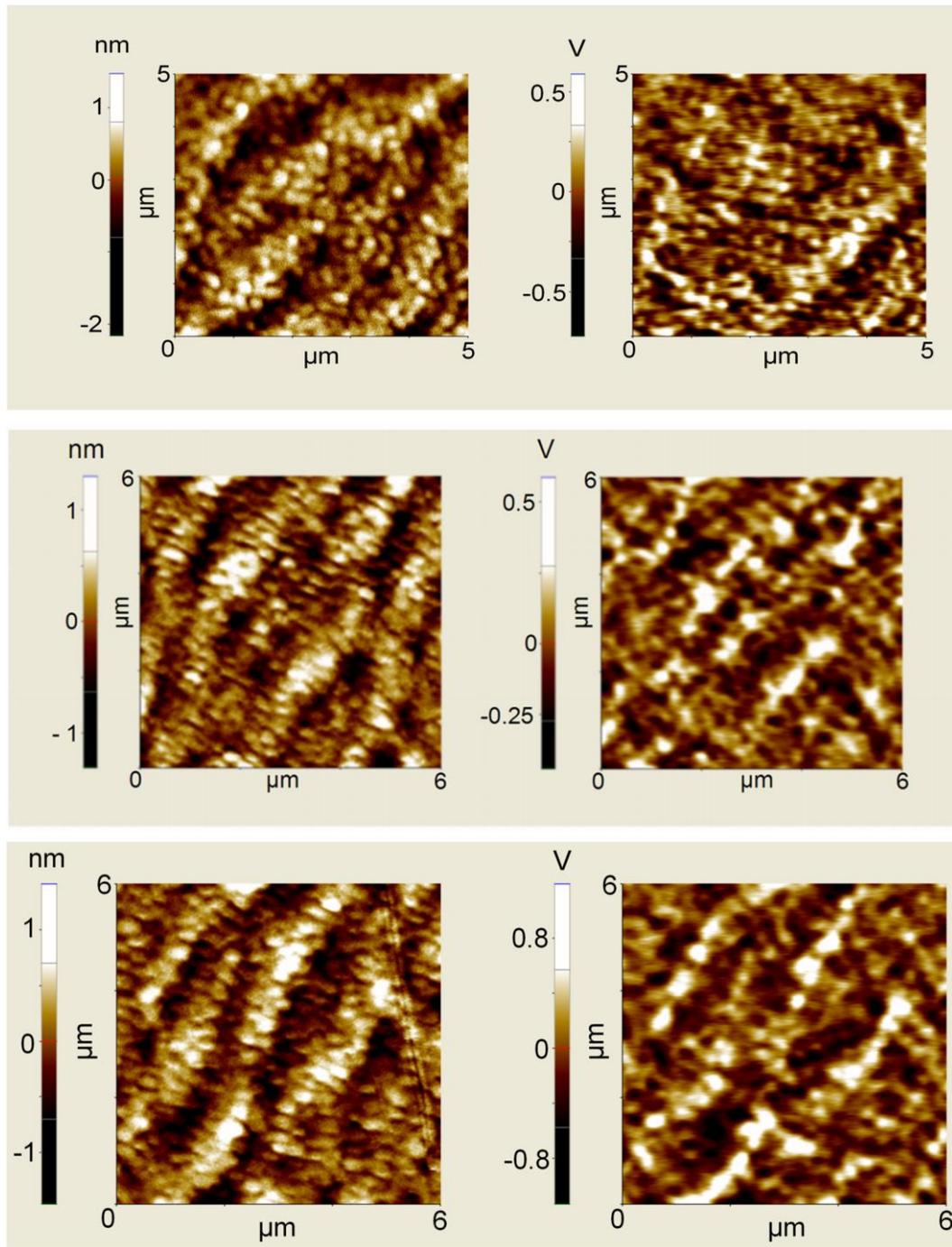
Figure 3.17 Topography (left) and SCM images (right) from the de-processed gate of smooth SRB strained Si devices. Parameters: $V_{ac} = 2\ V_{rms}$, $f_{ac} = 20$ **kHz,** $V_{dc} = 0$**V.**
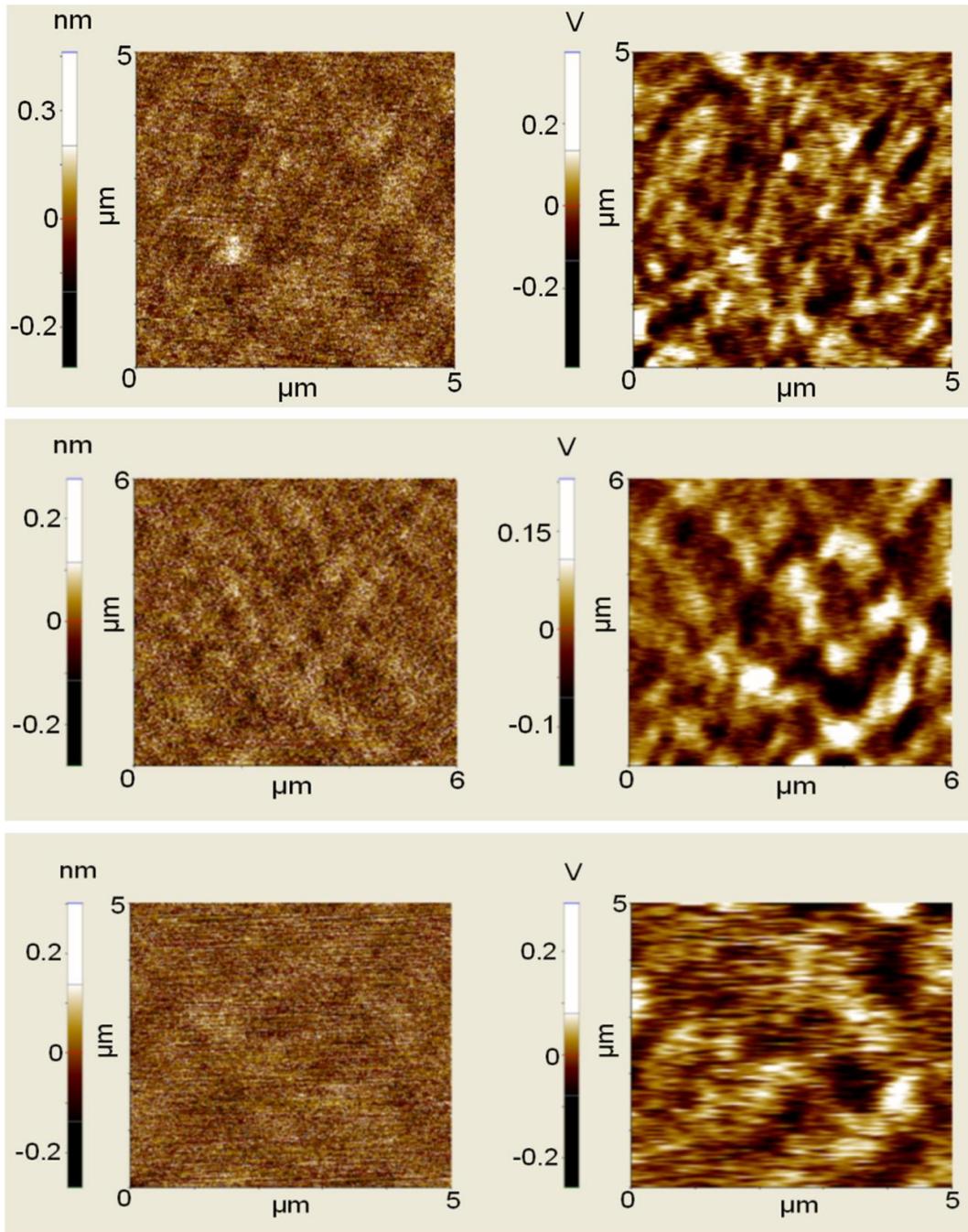
Figure 3.18 Topography (left) and SCM images (right) from the de-processed gate of Si control devices. Parameters: $V_{ac} = 2 \; V_{rms}, f_{ac} = 20 \; \text{kHz}, V_{dc} = 0V$
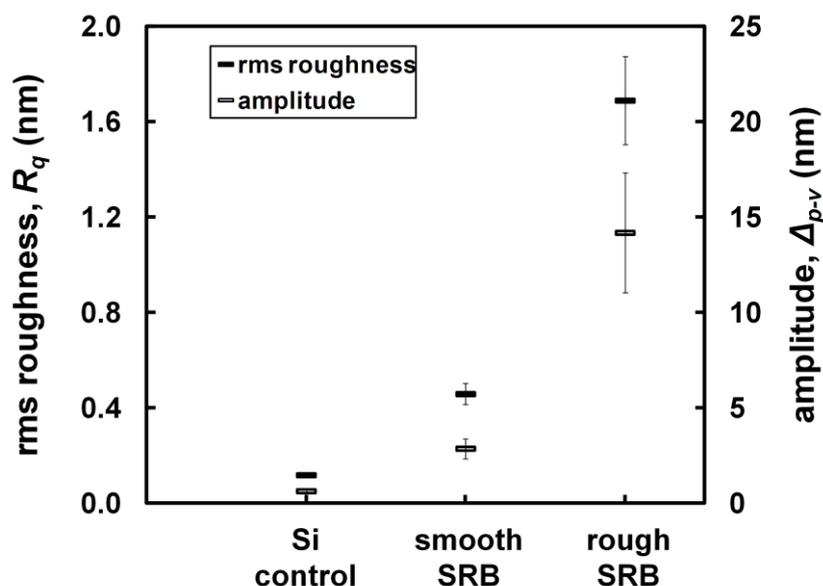
Figure 3.19 Comparison of rms roughness (R_q) and the amplitude of surface undulations ($\Delta_{p\text{-}v}$) for Si control and strained Si devices obtained using C-AFM.

In accordance with previous reports [121, 141, 226-228], SCM maps are expected to exhibit an inverse relationship with local variations in dielectric thickness caused by morphological fluctuations. This causes SCM scans to be an inverse image of the topography. Hence the pattern exhibited in the SCM maps of strained Si devices (Figs. 3.16 and 3.17) is considered to be largely due to the substrate induced surface morphology which propagates to the surface of the dielectric. For rough SRB devices, SCM maps clearly follow the crosshatch morphology (Fig. 3.16). Also, the differences in the ΔC signal in the SCM images of Figs. 3.16-3.18 can also be attributed to the level of substrate induced spatial variations, since all the scans were recorded under identical lock-in conditions. Consequently, rough SRB strained Si devices exhibit highest ΔC signal followed by smooth SRB and Si control devices. The SCM maps from Si control devices (Fig. 3.16) which do not exhibit any topographic pattern, show bright and dark contrasting regions.

Si control and strained Si devices have a fairly uniform dielectric with nearly identical variations in thickness (section 2.5.6). Also, a closer look at the SCM maps of rough SRB strained Si devices (Fig. 3.16) show that the inverse relationship between the features in topography and SCM images is not followed everywhere. For instance, in rough SRB devices (Fig. 3.16) troughs and highly sloped regions which have distinguishable contrast in the topography image may appear as bright regions in the SCM map with very little or no contrast. Fig. 3.20 shows the relationship between

surface height (depth) and SCM signal for rough SRB strained Si devices obtained from 5000 random individual points in the topography and SCM maps. SCM signal decreases (becomes more negative) with increasing surface height and vice versa (Fig. 3.20). However, it can also be seen that for a given height (or depth) on the surface, the level of the SCM signal can be different. The SCM measurement setup may not be able to respond to surface features such as small steps and steep undulations or SCM maps may also be receiving capacitive contributions from random defects and trapped charges. Alternatively, it is likely that the SCM signal at a given location is collectively influenced by morphology and random trapped charges depending on the position along the crosshatch period. Since high V_{ac} (2 V_{rms}) and low f_{ac} (20 kHz) were used for high SNR and hence better contrast, the measurement setup is unlikely to explain the lack of contrast across steep slopes.

Similar variation in the SCM signal with height has also been observed for smooth SRB devices (Fig. 3.21). Since there are no specific topographical features on the surface of Si control devices (Fig. 3.18), it is possible that any contrasting features in the SCM maps may be due to defects and trapped charges.
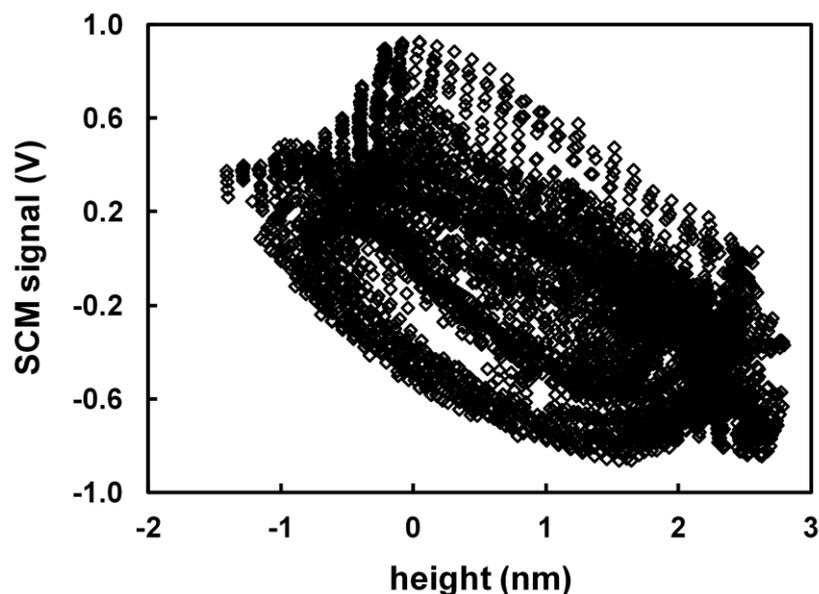
Figure 3.20 Plot of SCM signal vs. surface height (depth) for rough SRB strained Si devices.
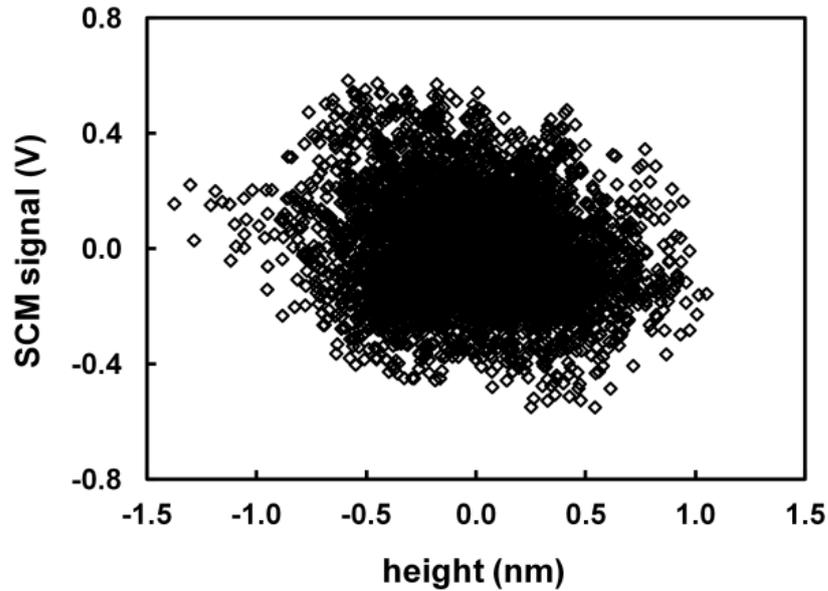
Figure 3.21 Plot of SCM signal vs. surface height (depth) for smooth SRB strained Si devices.

SCM imaging indicates that it may be possible to identify regions in the SCM map where interface quality is degraded due to charge trapping. This differs from some previous reports [121, 141, 226-228] where the SCM image has only been affected by the variations in dielectric thickness caused by surface morphology and the impact of defects and trapped charges is negligible. This contradiction may be answered by the quality of the dielectric. The dielectrics on strained Si and Si control devices studied in this work exhibit low surface roughness (Figs. 2.29 and 3.19) and minimal variations in t_{ox} (section 2.5.6). The dielectrics studied in [227, 228] have a surface roughness of 3 nm which is nearly twice the typical surface roughness of dielectrics on rough SRB devices. Such high levels of roughness may mask the influence of defects and trapped charges on the SCM signal, since both t_{ox} and D_{it} can be simultaneously influenced by surface roughness [141]. According to [121], the inverse relationship between morphology and SCM signal is not observed when the surface roughness is reduced from 6.9 nm to 0.2 nm. According to [226], a decrease of 4.3 nm in t_{ox} increases the SCM signal by 1.5 V. For strained Si and Si control devices studied in this chapter, the variation in t_{ox} is under 0.4 nm (section 2.5.6) while the SCM signal varies by at least 2 V for rough SRB, 1 V for smooth SRB and 0.4 V for Si control devices (Figs. 3.16-3.18). Hence it is likely that the SCM images shown in Figs. 3.16-3.18 are being influenced by random defects and trapped charges. In summary, it is easier to study

defects and trapped charges using SCM if dielectrics with low levels of surface roughness and uniform thickness can be obtained.

These observations further support the need for improved material growth, device processing and sample preparation techniques to obtain maximum information from the SCM measurement setup. In order to clearly understand the influence of trapped charges on SCM images localised analysis at individual points on the substrate is required.

3.3.3 Localised C-V analysis

In order to identify regions on the substrate with enhanced D_{it}, individual dC/dV curves were obtained from different locations. Fig. 3.22 shows the variation in dC/dV sweeps with V_{tip} obtained from 20 random locations across the gate dielectrics of Si control and strained Si devices. Differences in $FWHM$ and position of $V_{tip, peak}$ can be observed for the three types of devices in Fig. 3.22. This difference is better visible in Fig. 3.23 which shows the typical dC/dV curves for the three sets of devices. The variation in $V_{tip, peak}$ and $FWHM$ of the dC/dV sweeps in Fig. 3.22 is shown in Fig. 3.24. It can be seen that the dC/dV sweeps of Si control devices exhibit lowest $FWHM$ followed by smooth SRB devices. Amongst all the devices measured, dC/dV sweeps of rough SRB devices have consistently shown the highest $FWHM$. $FWHM$ of dC/dV sweeps is a direct qualitative measure of D_{it} (section 3.3.1). Hence, Fig. 3.24 indicates that Si control devices exhibit lower D_{it} compared with strained Si devices. Rough SRB devices also exhibit higher D_{it} than smooth SRB devices on the basis of the variation in $FWHM$ of their dC/dV sweeps (Fig. 3.24). These trends in $FWHM$ (and hence D_{it}) obtained from nanoscale measurements are in good agreement with the previously reported [75] macroscopic results for gate dielectrics on these type of substrates.
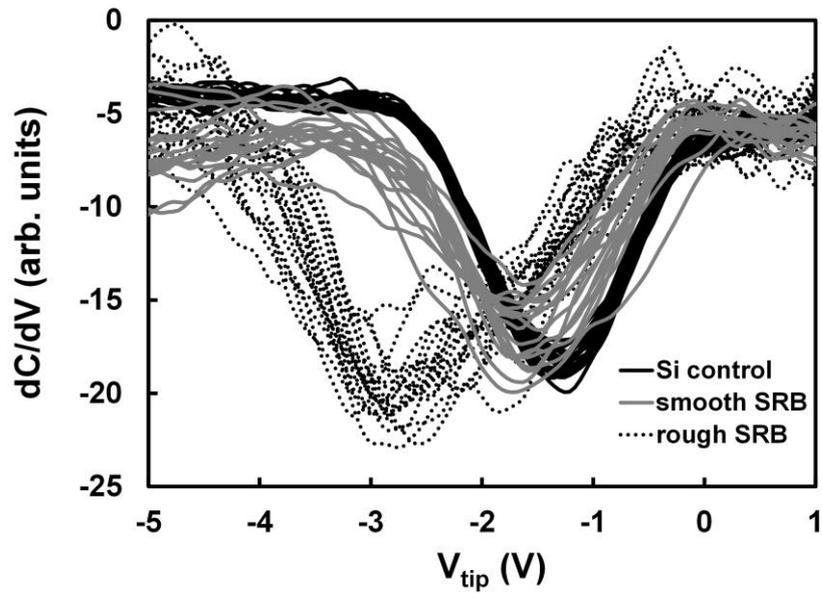
Figure 3.22 *dC/dV* response from 20 random locations across the de-processed gates of Si control, rough SRB, and smooth SRB strained Si devices obtained using SCM in the spectroscopy mode.
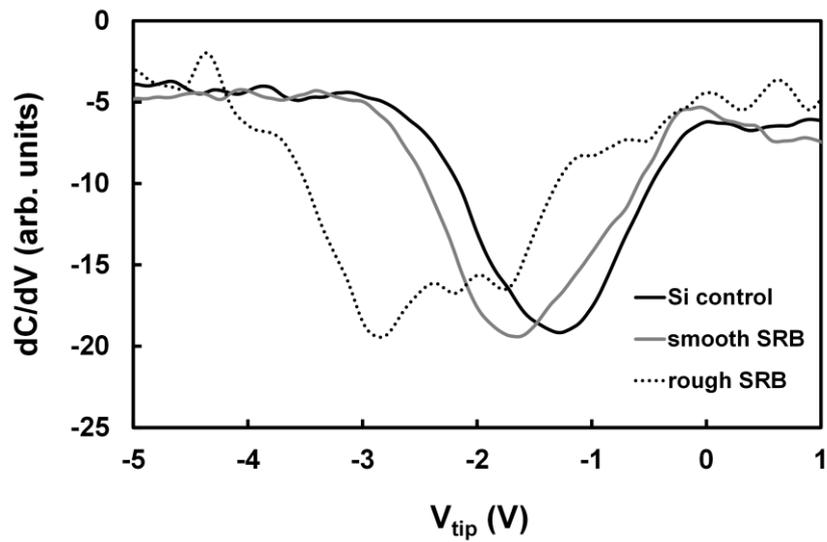
Figure 3.23 Typical *dC/dV* curves for Si control and strained Si devices.
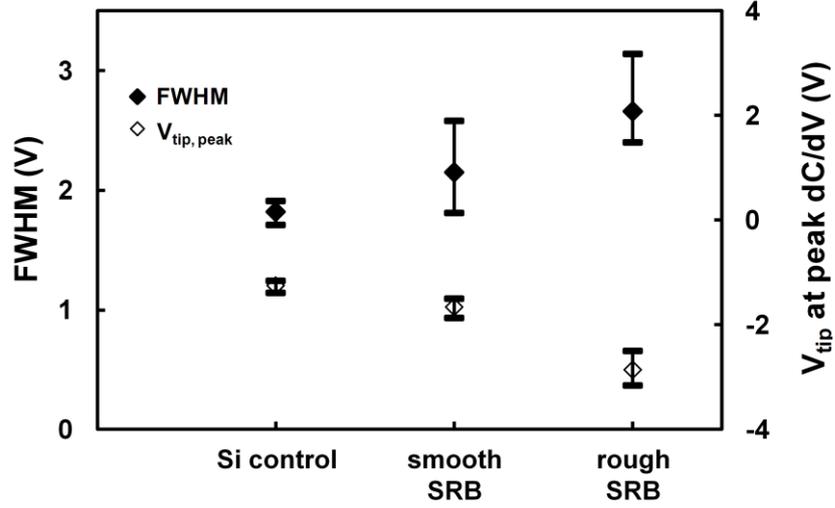
Figure 3.24 Variation in *FWHM* and *V*$_{tip, peak}$ of *dC/dV* sweeps of Si control, rough SRB, and smooth SRB strained Si devices.

3.3.4 Parameter extraction at the nanoscale and comparison with macroscopic trends

Fig. 3.25 compares the nanoscale trends in D_{it} (Fig. 3.24) with previously reported macroscopic values of D_{it} [75] for devices processed on similar substrates. A good correlation between the device-level and nanoscale trends can be observed in Fig. 3.25. Such correlation validates the SCM measurement setup for measuring D_{it}.

Similarly, $V_{tip, peak}$ which is an indicator of V_{FB} (section 3.3.1) and hence its shift from the ideal value ($V_{FB, shift}$) has also been found to be different for Si control and strained Si devices. The ideal value of V_{FB} ($V_{FB, ideal}$), is equal to the workfunction difference between the metal coated tip and the underlying semiconductor (Si/strained Si) [13]:

$$V_{FB, \ ideal} = \ \varphi_m - \varphi_s.$$ **3.1**

For a p-type semiconductor, φ_s is expressed as [13],

$$\varphi_s = \ \chi + \frac{E_g}{2q} + \psi_s \ ,$$ **3.2**

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where, χ is the electron affinity of the semiconductor (Si/strained Si). The values of φ_m, χ, E_g and ψ_s along with the calculated values of φ_s and $V_{FB,\,ideal}$ for Si control and strained Si devices have been included in Table 3.1 [184, 186, 187].
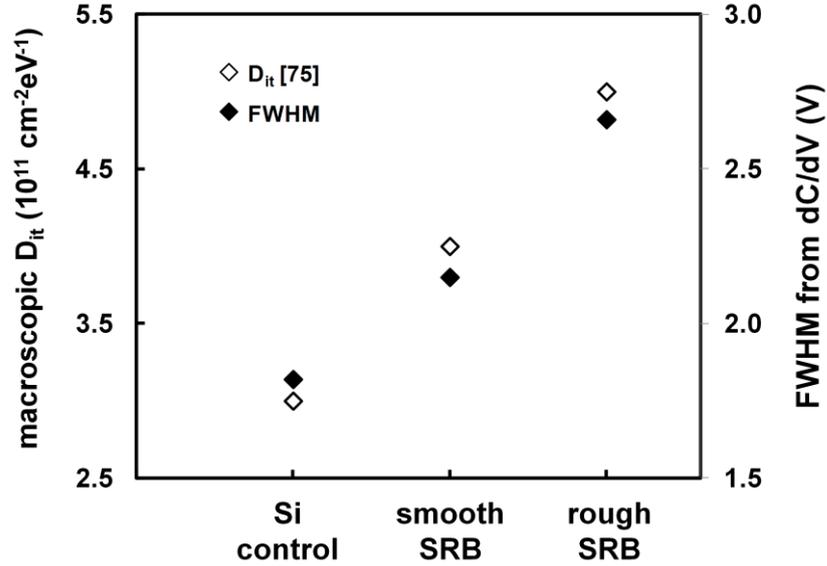
Figure 3.25 Median *FWHM* of SCM *dC/dV* sweeps compared with macroscopically measured D_{it} [75] for Si control, rough SRB, and smooth SRB strained Si devices.

Table 3.1 Parameters required to calculate $V_{FB,\,ideal}$ for Si control and strained Si devices [184, 186, 187].

device	φ_m (eV) (Pt)	χ (eV)	E_g (eV)	ψ_s (V)	φ_s (eV)	$V_{FB,\,ideal}$ (V)
Si control	5.60	4.05	1.12	0.46	5.07	0.53
strained Si (20% Ge in the SRB)	5.60	4.16	1.00	0.44	5.10	0.50

Fig. 3.26 shows the variation in the magnitude of $V_{FB, shift}$ for Si control and strained Si devices obtained by subtracting $V_{FB, ideal}$ from $V_{tip, peak}$. It can be seen that $V_{FB, shift}$ increases for strained Si devices with rough SRB devices exhibiting the highest values of $V_{FB, shift}$. This further confirms the increased levels of dielectric charges in the strained Si devices compared with Si control devices as indicated by Fig. 3.24.
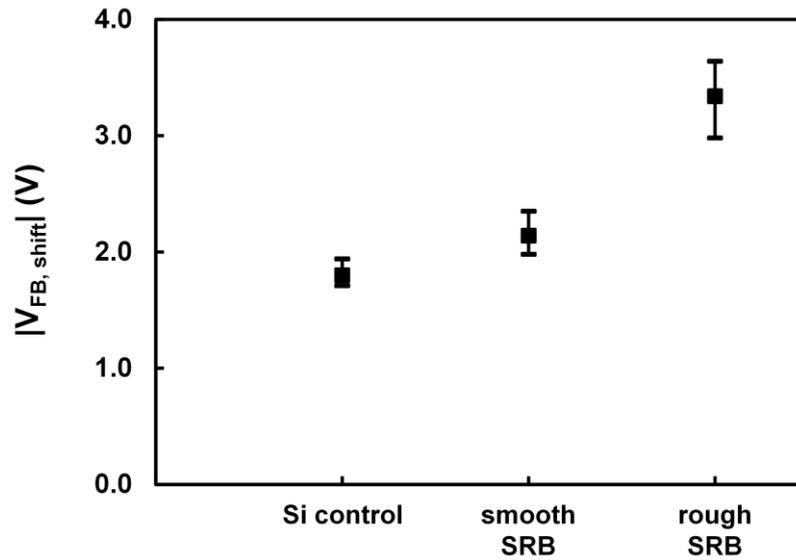
Figure 3.26 |$V_{FB, shift}$| for Si control, rough SRB, and smooth SRB strained Si devices obtained by subtracting $V_{FB, ideal}$ from the $V_{tip, peak}$ of *dC/dV* sweeps.

3.3.5 Relationship between FWHM and $V_{tip, peak}$

Fig. 3.27 shows the variation in FWHM (indicator of D_{it}) with $V_{tip, peak}$ (indicator of V_{FB}) of the *dC/dV* sweeps in Fig. 3.22. A very weak relationship has been observed between the *FWHM* and $V_{tip, peak}$ of *dC/dV* sweeps.

It can be seen in Fig. 3.27 that rough SRB strained Si devices show an 8-fold increase in linearity between *FWHM* and $V_{tip, peak}$ compared with Si control devices. However, even with such increase, *FWHM* has been found to be a very weak function of $V_{tip, peak}$. For a given value of $V_{tip, peak}$, different values of *FWHM* have been observed. This may be due to the fact that V_{FB} is influenced not only by interface trapped charges but also by bulk charges and workfunction differences, while D_{it} is only a measure of charge density at the interface. Additionally, presence of charges of both polarities in

the dielectric may also explain the weak relationship between the *FWHM* and $V_{tip, peak}$ of *dC/dV* sweeps (Fig. 3.27).
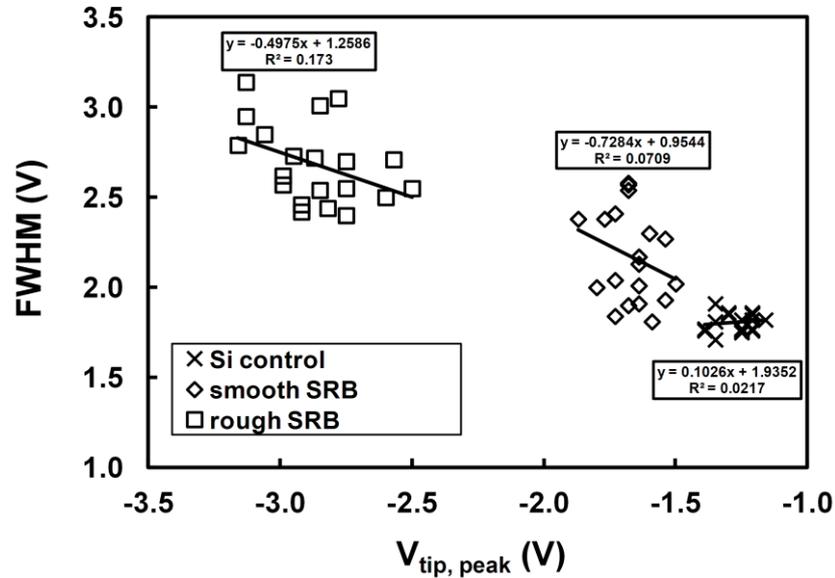
Figure 3.27 Plot of *FWHM* vs. $V_{tip, peak}$ showing the weak relationship between the two parameters after linear fitting.

3.3.6 Interface quality at contrasting regions in SCM images

To understand precisely which regions develop increased D_{it} in rough SRB devices, individual *dC/dV* sweeps were obtained from contrasting regions in the SCM maps of Fig. 3.16. Fig. 3.28 presents the *dC/dV* sweeps and variations in $V_{tip, peak}$ and *FWHM* from bright and dark regions in the SCM maps of the rough SRB devices. In total, 12 sweeps each from bright and dark regions are presented. In general, Fig. 3.28 suggests that *dC/dV* sweeps from bright regions in the SCM image show higher *FWHM* compared with dark regions. Since bright regions in the SCM maps correspond to troughs and steep slopes in topography (Fig. 3.16), Fig. 3.28 implies that D_{it} is enhanced in these regions. This morphological dependence of D_{it} in rough SRB devices is similar to the variation in J_g for similar devices as shown in the preceding chapter. With a fairly uniform dielectric and similar channel thickness, increased interface roughness due to large scale crosshatch undulations [119], threading dislocations penetrating in the channel [110] and variable Ge diffusion [178] are likely to be responsible for the regional variations in D_{it} in rough SRB devices. Increased D_{it} at troughs and along the

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steep slopes of crosshatch morphology in the rough SRB devices can also contribute to enhanced J_g at these regions [209].
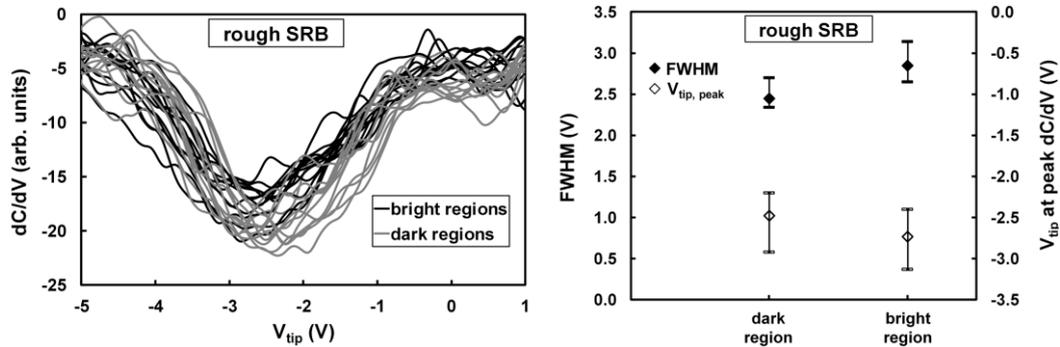
Figure 3.28 *dC/dV* **sweeps and variation in** *FWHM* **and** $V_{tip, peak}$ **from contrasting regions in the SCM maps of rough SRB devices.**

The difference in *FWHM* (and hence D_{it}) between bright and dark regions of the SCM maps is reduced when strained Si devices on a smooth SRB are analysed. Fig. 3.29 shows that although the highest *FWHM* is obtained from a bright region, the *FWHM* obtained from dark regions is not very less either. It may be concluded that reduction in crosshatch not only reduces overall D_{it}, but also makes the interface quality more uniform across the substrate. Hence the quality of the underlying SRB has implications on device reliability and variability.

Analysis of the Si control device (Fig. 3.30) also shows that the highest *FWHM* values are obtained from bright regions. Some of the *dC/dV* sweeps from bright and dark regions show similar *FWHM* indicating similar levels of D_{it}, however it can be seen that the highest value of *FWHM* (and hence D_{it}) has been obtained from a bright region in the SCM map.
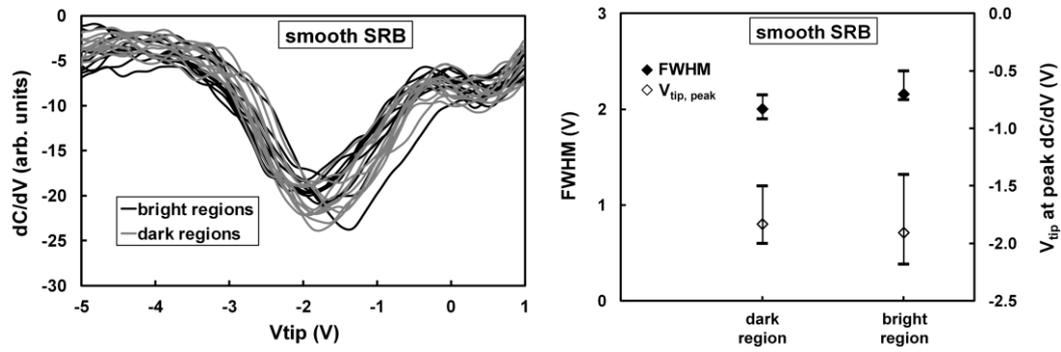
Figure 3.29 *dC/dV* sweeps and variation in *FWHM* and $V_{tip, peak}$ from contrasting regions in the SCM maps of smooth SRB devices.
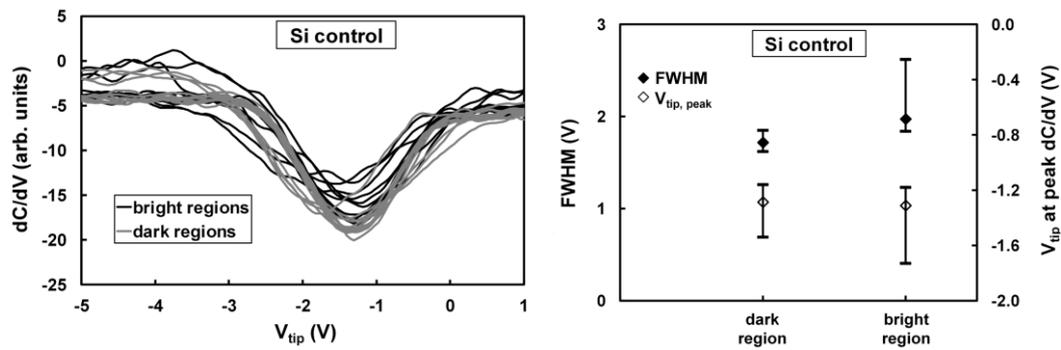
Figure 3.30 *dC/dV* sweeps and variation in *FWHM* and $V_{tip, peak}$ from contrasting regions in the SCM maps of Si control devices.

3.4 Summary

The quality of the interface between thin dielectrics and high mobility strained Si channels has been assessed. Nanoscale analysis of D_{it} in fully processed bulk-Si and strained Si n-MOSFETs has been carried out using SCM in both scanning and spectroscopy mode. A correlation between macroscale and nanoscale trends in D_{it} in Si control and strained Si n-MOSFETs has been established which validates the analysis and measurement setup.

For strained Si devices, SCM maps follow the surface topography induced by the underlying SRB. In rough SRB devices with large scale crosshatch pattern, slopes and troughs show some contrast in the topography. However, these regions appear as bright regions in the SCM image with little or no contrast. This lack of contrast in the SCM

images is unlikely to be explained by the measurement setup since large ac voltage and low frequency was used while scanning which increases SNR. Contrasting regions were observed in the SCM maps of atomically flat dielectrics on Si control devices. Since surface roughness is low and t_{ox} is highly uniform, SCM maps appear to be receiving contributions from random defects and trapped charges. This further supports the need for improved material growth, device processing and sample preparation to obtain maximum information from SCM.

To further study the information contained in the SCM maps of different devices, individual dC/dV sweeps from 20 random locations were recorded. From these sweeps, variations in $FWHM$ (which is a qualitative measure of D_{it}) and $V_{tip, peak}$ (which is closer to V_{FB} and is an indicator of dielectric charges) have been analysed. Nanoscale trends in D_{it} are similar to macroscopic trends reported previously for devices fabricated on similar substrates.

Individual dC/dV sweeps from SCM, relating to D_{it}, have been related to localized regions on the substrate. It has been shown that dC/dV sweeps from troughs and steep slopes of crosshatch undulations which appear as bright regions in the SCM maps exhibit higher FWHM and hence higher D_{it} compared with peaks or crests. This morphological dependence of D_{it} on crosshatch undulations is similar to the variations in J_g for similar devices studied in the preceding chapter. With a fairly uniform dielectric and similar channel thickness, non-uniform behaviour in D_{it} for rough SRB devices is expected to be due to increased interface roughness, threading dislocations and fluctuations in substrate composition along the interface. Increased charge trapping at troughs and along the steep slopes of the conventional crosshatch morphology can enhance J_g at these regions.

The difference in $FWHM$ (and hence D_{it}) between the bright and dark regions is reduced for smooth SRB devices compared with the devices processed on rougher substrates. Strained devices which do not exhibit large scale crosshatch undulations but are rougher than Si control devices show reduced and more uniform levels of D_{it} compared with rough SRB devices. Si control devices did not exhibit any morphological pattern, however, dC/dV sweeps from bright regions in the SCM maps of these devices exhibited higher $FWHM$ compared with dark regions.

The conclusions drawn from the results presented in this chapter have implications for different material systems where the substrate can induce morphological changes. This includes technologies using relaxed SiGe templates, such as strained Si on

insulator (SSOI), strained Ge on insulator (SGOI) and strained Ge. Additionally, the impact of modifications introduced at the interface by using high-κ dielectrics such as ZrO_2 and HfO_2 etc. may also be studied using the setup and analysis presented in this chapter.

Chapter 4. Scanning Probe Analysis of Thin Dielectrics on Compressively Strained Si$_{1-x}$Ge$_x$

Compressively strained SiGe is an attractive channel material due to its high hole mobility and compatibility with existing CMOS processes. In this chapter, electrical properties of thin dielectrics on epitaxially grown thin Si$_{1-x}$Ge$_x$ layers are presented. Dielectric leakage, breakdown behaviour, thickness and interface traps are analysed on a nanoscale for thin dielectrics grown on strained SiGe with varying Ge. Through analysis of C-AFM, SCM and semi-empirical modelling, contributions to the electrical properties originating from localised regions on the substrate and dielectric are identified. The impact of Ge content (and hence strain) is assessed using different Ge contents (0, 20, 35, 50 and 65%). Surface morphology of thin dielectrics on strained Si$_{1-x}$Ge$_x$ layers has been studied using a sharp AFM tip in non-contact mode. Nanoscale electrical analysis shows that J_g and D_{it} increase with Ge in the strained layer. These observations are in agreement with theory and previously reported macroscopic trends. The results show that if morphological fluctuations often associated with strained SiGe layers can be avoided, a uniform electrical behaviour can be obtained.

4.1 Background

The benefits provided by conventional CMOS scaling are fast approaching saturation because of limitations on physical dimensions (section 1.2.1). Individual SiGe stressors in the source and drain have been widely employed to realise high mobility strained Si p-MOSFETs [229, 230]. However, enhancements from uniaxial strain (produced by individual SiGe stressors) is also expected to reach its limits [231, 232]. Consequently, alternate channel materials especially those which can be processed on a Si platform are continuously being explored. Si$_{1-x}$Ge$_x$ when grown epitaxially on Si (which has a lower lattice constant) undergoes compressive strain and the amount of strain can be controlled by Ge concentration and layer thickness. Strain induced splitting of energy bands alters the band structure of SiGe and leads to preferential occupation by holes in LH bands, thereby enhancing hole mobility (section 1.3.1). SiGe channels have exhibited improved performance through enhanced hole mobility which is not possible with tensile strained Si channels (section 1.3.1). Hence, compressively strained SiGe

layers have emerged as an attractive alternate channel material. Electrical performance enhancements including high hole mobility, increased on-state current and low V_t in SiGe channel devices are well documented [67-71, 231, 233]. For a 1.6% compressive strain in the SiGe channel, hole mobility enhancement factor of 2.5-4.5 can be expected [234, 235].

However, Ge-induced changes in the material and dielectric interface quality strongly affect the final device performance. Devices which employ relaxed or strained SiGe layers often suffer from Ge segregation. Lower oxidation rates in SiGe cause selective consumption of Si during oxidation which results in a pile-up of Ge atoms at the dielectric/semiconductor interface [236-238]. Such dangling Ge atoms at the interface are in direct electrical contact with the channel and can increase trapped charges at the interface [239-241]. Increase in Ge content leads to a higher density of un-bonded Ge atoms at the interface. Consequently, dielectric performance in strained SiGe devices is usually not as good as bulk-Si and is further degraded for Ge rich devices. Previous reports show that devices employing strained SiGe channels exhibit increased levels of J_g and D_{it} compared with bulk-Si devices and this degradation enhances with Ge [69, 101, 242-245]. To counter Ge segregation, SiGe channel devices generally employ a thin Si cap above the channel (section 1.4.2).

4.1.1 Surface morphology of compressively strained SiGe layers

Surface roughness either due to dislocations or excessive strain energy is a common feature of strained Si/SiGe epitaxy (section 1.3.2). Surface roughness of fully relaxed SiGe layers increases with Ge content (section 1.3.2). For thin epitaxial strained SiGe layers, increase in strain often influences surface morphology and results in increased levels of surface roughness [84, 246]. Surface morphology of strained SiGe layers is generally different compared with relaxed layers. Surface roughness typically associated with strained SiGe is lower compared with fully relaxed SiGe substrates [83, 92]. Strained SiGe layers can be expected to exhibit micro-roughness in the form of surface ripples, island like patterns and surface corrugations [81-83]. The scale of micro-roughness generally increases for Ge rich strained alloys due to excessive strain energy. This is because excessive strain favours partial relaxation to reduce surface energy.

SiGe layer thickness also influences surface morphology and roughness (section 1.3.2). Strain relaxation through dislocations strongly influences surface roughness and

morphology. Above h_c, strain relaxation increases rapidly with increasing layer thickness for a given Ge content [92]. Mid to large scale undulations due to strain relaxation appear on the surface of thin SiGe layers when layer thickness exceeds h_c for a given Ge content. The scale of surface undulations and consequently, the roughness length scales increase with layer thickness.

The effect of compressive strain on the surface morphology of strained SiGe layers is shown in Fig. 4.1. AFM images obtained from epitaxially grown strained SiGe layers with varying Ge (and hence strain) show different surface morphology and roughness. Fig. 4.1 shows an increase in R_q and Δ_{p-v} with compressive strain in SiGe.

Ge content (%)	Strain (%)	R_q (nm)	Δ_{p-v} (nm)
20	-0.63	0.27	2.77
50	-0.73	0.57	4.08
100	-0.77	1.56	5.13
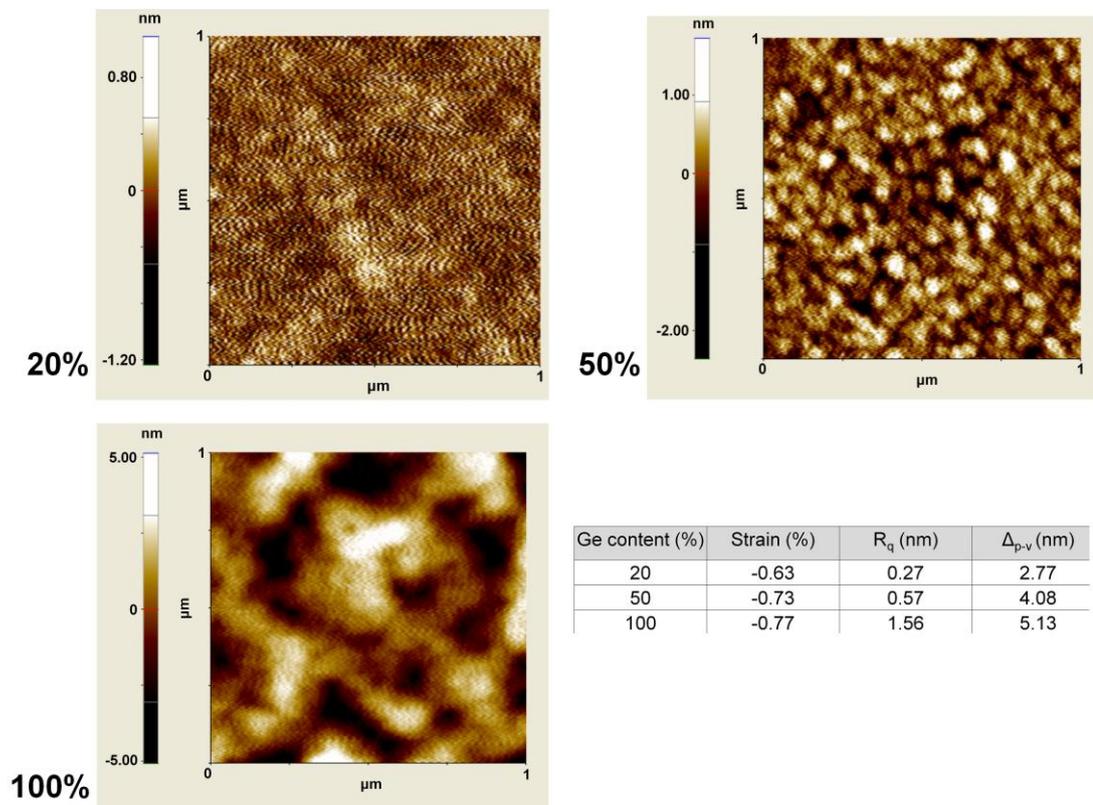
Figure 4.1 Variations in the surface morphology and roughness with increasing compressive strain in epitaxial SiGe layers grown on bulk-Si.

4.1.2 Dielectrics on compressively strained SiGe

It has been shown in the preceding chapters that surface roughness induced by the fully relaxed SiGe substrates in tensile strained Si devices adversely affects dielectric performance and reliability. Enhanced J_g (section 2.5) and D_{it} (section 3.3) have been

observed around the troughs and steep slopes of conventional crosshatch undulations induced by the underlying SiGe SRB. Strained SiGe exhibits different morphology compared with relaxed SiGe layers (section 4.1.1). Consequently, surface topography and typical roughness length scales of strained SiGe layers are expected to be different than strained Si layers grown on relaxed SiGe SRBs. This implies that dielectrics grown or deposited on strained SiGe channels can exhibit different surface morphology than on strained Si channels. Consequently, any morphological dependence of dielectric reliability on compressively strained SiGe channels is likely to be different.

According to [84], compressive strain induced surface corrugations are expected to degrade dielectric performance in strained SiGe channel devices. Additionally, high field mobility in strained SiGe devices is also expected to be influenced by strain induced surface roughness (surface roughness scattering). Increased interface roughness from a buried compressively strained $Si_{0.70}Ge_{0.30}$ channel has been shown to degrade gate dielectric quality in dual channel devices [85]. However, there are no reports which relate strained SiGe surface morphology with dielectric performance in strained SiGe devices. This chapter presents a nanoscale electrical analysis of thin dielectrics on strained SiGe layers using electrical SPM techniques. Nanoscale J_g, t_{ox} and localised breakdown behaviour is studied using C-AFM maps and spectroscopic I-V curves. SCM maps and spectroscopic dC/dV sweeps have been obtained to study the localised variations in D_{it}, V_{FB} and $V_{FB, shift}$.

The effects associated with new dielectrics have been avoided by analysing thermally grown SiO_2 on strained SiGe layers. Since the effect of the underlying SiGe layer has been studied, the findings also hold significance for high-κ dielectrics on strained SiGe.

4.2 Material growth and characterisation

4.2.1 Growth of strained SiGe layers

Strained SiGe layers studied in this work were grown at CEA-LETI (Grenoble, France) using the Epi Centura reduced pressure-chemical vapour deposition (RP-CVD) industrial cluster tool manufactured by Applied Materials.

Lightly boron doped bulk-Si wafers with resistivity of 8-20 Ω-cm (N_{sub} ~ 10^{15} cm^{-3}) were baked in-situ for 2 minutes in H$_2$ environment at 1100 °C at a pressure of 20 Torr. This thermal processing removed any native oxide and allowed epitaxial growth to be initiated on atomically smooth Si surfaces. Following this a few tens of nm thick Si buffer was grown for all the samples.

Blanket Si$_{1-x}$Ge$_x$ layers of different Ge content (20%, 35%, 50% and 65%) were then grown using the RP-CVD method. The growth pressure was 20 Torr. Pure dichlorosilane (SiH$_2$Cl$_2$) was used as the source of Si while germane (GeH$_4$) diluted at 2% in H$_2$ was the source of Ge. Higher levels of Ge were obtained by gradually increasing the mass flow ratio of GeH$_4$ and H$_2$. The growth temperature was reduced from 650 °C to 550 °C as the targeted Ge concentration was increased from 20% to 65%, in order to minimize surface roughening. This reduction in temperature was also based on the growth kinetics of SiGe. For a fixed growth temperature, growth rate of SiGe layers increases linearly with Ge content [92]. Hence, in order to have reasonable growth rates in line with the intended layer thickness, growth temperature was reduced for Ge rich layers.

Si$_{1-x}$Ge$_x$ layers did not receive any intended doping and can be expected to have a doping profile similar to the underlying Si substrate. Epitaxial SiGe layers were passivated by a thin Si cap (~ 4 nm) which was grown in two stages.

Details of growth of different layers are included in Table 4.1. A cross-sectional schematic of the materials studied in this chapter is shown in Fig. 4.2.

Table 4.1 Material growth conditions for the sample studied.

Layer	Growth temp. (°C)	mass-flow ratios	Growth time (s)	Growth rate (nm/min)
Si buffer	900	$F(SiH_2Cl_2)/F(H_2) = 1.25 \times 10^{-3}$	30	-
$Si_{0.80}Ge_{0.20}$	650	$F(SiH_2Cl_2)/F(H_2) = 2.5 \times 10^{-3}$ $F(GeH_4)/F(H_2) = 8.33 \times 10^{-5}$	78	8.3
$Si_{0.65}Ge_{0.35}$	600	$F(SiH_2Cl_2)/F(H_2) = 2.5 \times 10^{-3}$ $F(GeH_4)/F(H_2) = 1.67 \times 10^{-4}$	130	5.5
$Si_{0.50}Ge_{0.50}$	550	$F(SiH_2Cl_2)/F(H_2) = 2.5 \times 10^{-3}$ $F(GeH_4)/F(H_2) = 4.58 \times 10^{-4}$	112	6.5
$Si_{0.35}Ge_{0.65}$	550	$F(SiH_2Cl_2)/F(H_2) = 1.83 \times 10^{-3}$ $F(GeH_4)/F(H_2) = 8.25 \times 10^{-4}$	79	17.2
Si cap	Stage 1: 550 Stage 2: 600	$F(SiH_4)/F(H_2) = 0.01$	Stage 1: 60 Stage 2: 100	-
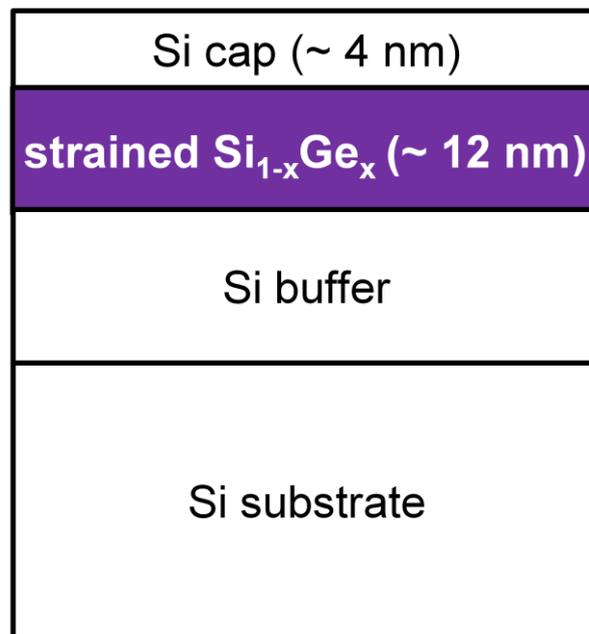
Figure 4.2 Cross-sectional schematic of the samples studied in this chapter.

4.2.2 XRR and XRD analysis of layer thickness and alloy content

XRR curves were obtained to confirm the thickness of SiGe and Si cap layers. In addition, XRD measurements were also carried out to verify the thickness of SiGe layers and estimate the amount of Ge in the strained alloys.

XRR curves obtained from $Si_{1-x}Ge_x$ layers (capped with Si) with different Ge contents are shown in Fig. 4.3. A definite modulation of intensity can be observed over a large angular range (Fig. 4.3), indicating low levels of surface and interface roughness [247]. The angular spacing between the fringes is inversely proportional to the combined thickness of SiGe and Si cap, while the thickness of Si cap is to a first approximation inversely proportional to the angular spacing of maxima and minima of the envelope curve of the main fringes. The increase in the amplitude of oscillations with Ge content (Fig. 4.3) is due to the increase in density for SiGe compared with Si (density (Si) = 2.328 gcm^{-3}, density (Ge) = 5.327 gcm^{-3}). Thickness of SiGe and Si cap layers has been extracted from a fast Fourier transform of XRR curves, with a precision of ± 6 Å. This error is introduced by the CCD detector in the XRR measurement setup.
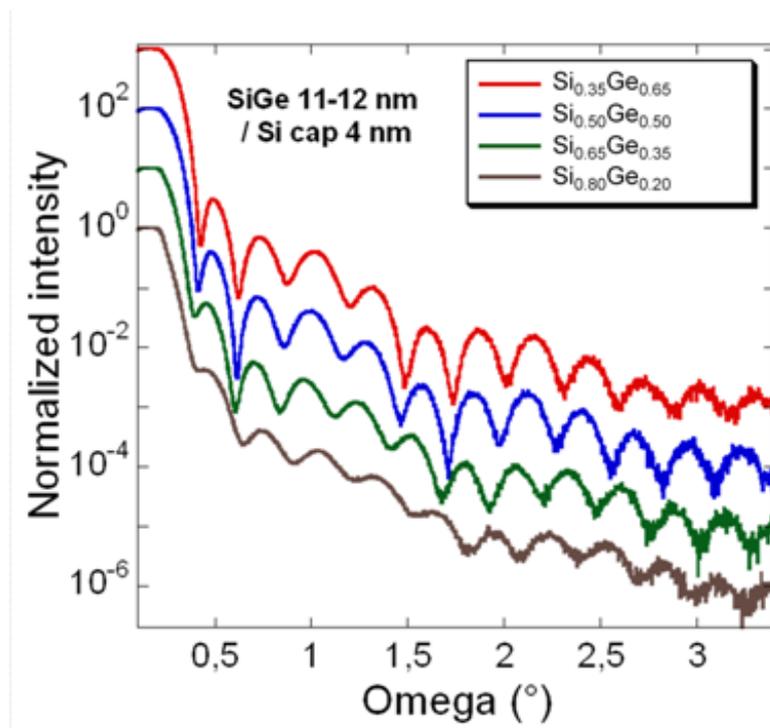
Figure 4.3 XRR curves from Si capped $Si_{1-x}Ge_x$ layers with varying Ge levels. (XRR measurements and analysis by J.M. Hartmann at CEA-LETI, Grenoble, France).

XRD curves obtained from Si capped SiGe layers with varying Ge content are shown in Fig. 4.4. Shift towards the lower side with increasing Ge indicates increasing compressive strain [153]. Well-defined thickness fringes on either side of the layer peak were observed except for the strained alloy with 65% Ge. Similar to the XRR curves, layer thickness is inversely proportional to the angular spacing between the thickness fringes in XRD curves.
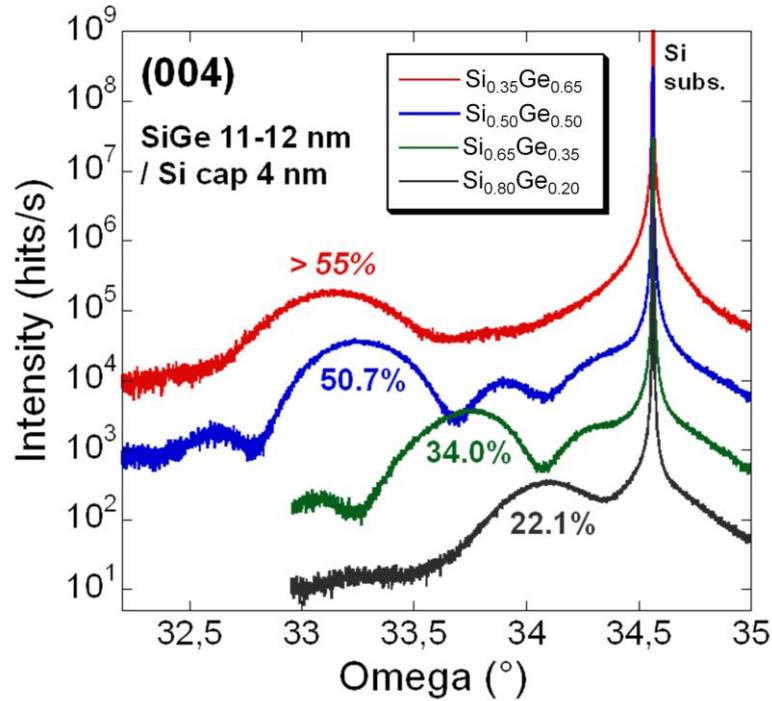
Figure 4.4 XRD curves from Si capped $Si_{1-x}Ge_x$ layers with varying Ge levels. (XRD measurements and analysis by J.M. Hartmann at CEA-LETI, Grenoble, France).

Thin epitaxial SiGe films when grown on Si are compressively strained along the plane of growth while the nature of strain in the perpendicular direction is tensile. Consequently, the lattice constants in parallel and perpendicular directions are different. The perpendicular lattice constant for strained SiGe ($a_{SiGe}^{\perp}$) is calculated from the XRD spectra in accordance with Bragg's law [153, 166]:

$$a_{SiGe}^{\perp} = \frac{3.081}{\sin(\theta_{Si} + \Delta\omega)}, \qquad \textbf{4.1}$$

where, θ_{Si} is the angular peak position of the Si substrate and $\Delta\omega$ is the angular separation between the Si substrate peak and the strained SiGe layer peak.

The average lattice constant of un-strained bulk SiGe (a_{SiGe}) is related to $a_{SiGe}^{\perp}$ by the following equation [92]:

$$a_{SiGe}^{\perp} = a_{SiGe} + \left(\frac{2v}{1-v}\right)(a_{SiGe} - a_{Si}), \qquad \textbf{4.2}$$

where, v is the Poisson ratio of the SiGe layer whose value for different Ge contents can be extrapolated from the values of Si (0.278) and Ge (0.271).

Once a_{SiGe} has been calculated, Ge concentration (x) in the strained alloy can be calculated by solving the following quadratic equation [92, 153]:

$$a_{SiGe} = 0.028x^2 + 0.1988x + 5.4311. \qquad \textbf{4.3}$$

Owing to the broad peak of SiGe layers in Fig. 4.4, the Ge content extracted from XRD spectra has an error of $\pm 0.5\%$.

The thicknesses and alloy content for different samples as extracted from the XRR and XRD measurements have been included in Table 4.2. A good agreement between the values of SiGe layer thickness from XRR and XRD measurements can be seen except for the $Si_{0.35}Ge_{0.65}$ sample. The difference in thickness arises due to the lack of clearly defined thickness fringes on either side of the layer peak in the XRD spectra from the $Si_{0.35}Ge_{0.65}$ layer. This lack of thickness fringes is an indicator of slight relaxation in the $Si_{0.35}Ge_{0.65}$ layer [92]. This slight relaxation in the $Si_{0.35}Ge_{0.65}$ layer is due to its higher Ge content and thickness similar to other samples. For an epitaxial $Si_{0.35}Ge_{0.65}$ layer grown on bulk-Si, h_c is expected to be between 4-8 nm [86-90], which is lower than the thickness of the layers studied in this chapter. Hence, a slight relaxation in the $Si_{0.35}Ge_{0.65}$ layer is not unexpected.

Table 4.2 also shows that the Ge content obtained from XRD is in agreement with the targeted concentration except for the $Si_{0.35}Ge_{0.65}$ sample. This discrepancy arises because the angular position of the XRD peaks of $Si_{0.50}Ge_{0.50}$ and $Si_{0.35}Ge_{0.65}$ layers is nearly similar (Fig. 4.4). This means that the XRD peak from the $Si_{0.35}Ge_{0.65}$ layer has experienced a shift towards the Si substrate peak. Additionally, $Si_{0.35}Ge_{0.65}$ layer peak appears to be broader compared with those from layers of lower Ge content. This shift and broadening of the XRD peak is another indicator of slight strain relaxation in the $Si_{0.35}Ge_{0.65}$ layer [92].

Table 4.2 SiGe and Si cap thickness and Ge content in the SiGe films as determined by the XRR and XRD measurements.

Sample	SiGe layer thickness (nm) (XRR)	SiGe layer thickness (nm) (XRD)	Ge concentration (%) (XRD)	Si cap thickness (nm) (XRR)
$Si_{0.80}Ge_{0.20}$	10.8	11.0	22.1	4.0
$Si_{0.65}Ge_{0.35}$	12.0	12.2	34.0	4.0
$Si_{0.50}Ge_{0.50}$	12.2	11.7	50.7	3.7
$Si_{0.35}Ge_{0.65}$	11.2	9.0	55.1	4.2

To summarise the XRR and XRD analysis, lack of thickness fringes on either side of the XRD layer peak (Fig. 4.4), XRD thickness lower than XRR (Table 4.2) and lower than targeted Ge content (Table 4.2) indicates that the $Si_{0.35}Ge_{0.65}$/Si stack is slightly relaxed with Ge content higher than indicated by XRD. Also, $Si_{1-x}Ge_x$/Si stacks for Ge content up to 50% are fully pseudomorphic (lattice matched).

4.2.3 Surface morphology of Si capped SiGe layers prior to oxidation

Surface morphology of Si capped $Si_{0.50}Ge_{0.50}$ and $Si_{0.35}Ge_{0.65}$ layers were studied by AFM measurements in tapping mode. Fig. 4.5 shows the surface morphology of Si-cap/$Si_{0.50}Ge_{0.50}$ and Si-cap/$Si_{0.35}Ge_{0.65}$ stacks, prior to oxidation. The surface of the $Si_{0.50}Ge_{0.50}$ layer (with ~ 4 nm of Si cap) is smooth and featureless, which can be expected for a fully pseudomorphic stack without any relaxation. By contrast, the surface of $Si_{0.35}Ge_{0.65}$ sample (capped with ~ 4 nm of Si) is characterised by small height undulations indicating slight elastic strain relaxation [92]. In addition to these small scale undulations, numerous "short lines" along the {110} directions can also be seen. These are likely due to partial plastic relaxation, as the {110} directions correspond to the intersection of the {111} dislocation gliding planes with the {001} surface [92].

Quantitatively, R_q and the maximum surface height (R_{max}) associated with the Si$_{0.35}$Ge$_{0.65}$ sample were found to be 0.17 nm and 1.7 nm respectively. These values for the Si$_{0.50}$Ge$_{0.50}$ sample were found to be 0.07 nm and 0.77 nm respectively.
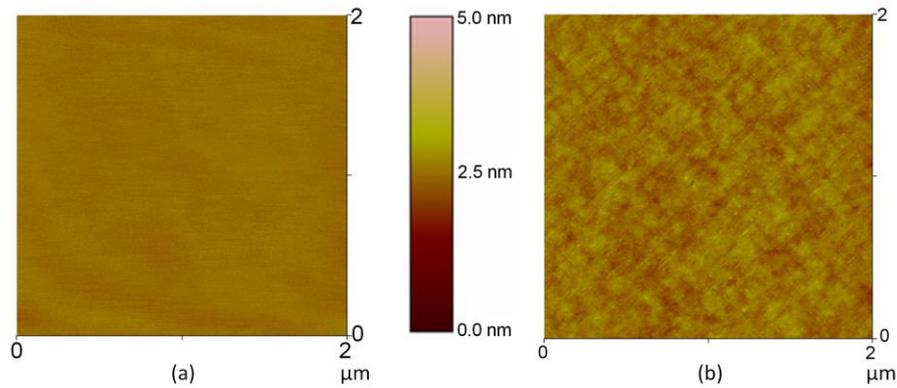
Figure 4.5 Tapping mode AFM images of the (a) Si$_{0.50}$Ge$_{0.50}$ and (b) Si$_{0.35}$Ge$_{0.65}$ samples prior to oxidation. Image sides are more or less along the {100} directions. (Tapping mode AFM measurements by J.M. Hartmann at CEA-LETI, Grenoble, France).

4.2.4 Oxidation of Si capped SiGe layers

The Si cap on the SiGe layers with varying Ge was subsequently oxidised at the Peter Grünberg Institute (PGI9-IT, Jülich, Germany). Wet oxidation at 600 °C for 60 minutes was carried out. The thickness of the oxide was measured at various points using ellipsometry and was found to be ~ 2.85 nm for all the samples. It is likely that ~ 1 nm of the Si cap was left after oxidation. However, this was not verified.

Control samples were also processed under identical conditions. After processing, the samples containing Ge were coated with an unbaked 2-3 μm thick AZ5214 photoresist for surface protection. This photoresist was removed using N-Methyl-2-pyrrolidone (NMP) and isopropyl alcohol (IPA) before further characterisation.

4.2.5 Surface morphology of strained SiGe layers post oxidation

High resolution AFM images (1×1 μm^2 at 1024 points/line) in non-contact mode were obtained to study the surface morphology after the oxidation of the Si cap. These are shown in Figs. 4.6-4.10. The surface of SiO_2 on SiGe layers with varying Ge has been found to be smooth as indicated by the low levels of R_q and $\varDelta_{p\text{-}v}$. Similar to the AFM images prior to oxidation (Fig. 4.5), no large scale roughness features were observed after oxidation. For the oxidised $Si_{0.50}Ge_{0.50}$ sample, R_q and R_{max} have been found to be 0.07 ± 0.01 nm and 1.03 ± 0.11 nm respectively. These values are similar to the values observed prior to oxidation (section 4.2.3). For the oxidised $Si_{0.35}Ge_{0.65}$ layer, R_q and R_{max} have been found to be 0.10 ± 0.01 nm and 1.06 ± 0.12 nm respectively. On comparing with the AFM analysis prior to oxidation, it is observed that the surface roughness and the maximum height observed on the surface of the Si capped $Si_{0.35}Ge_{0.65}$ layer has reduced post oxidation. The small scale undulations observed prior to oxidation (Fig. 4.5) are also visible after oxidation (Fig. 4.10).

The high resolution AFM images (Figs. 4.6-4.10) were filtered using MATLAB to reject any large to medium scale roughness components. This was needed as the AFM image analysis software is not able to separate the nanoscale roughness from large scale components. Additionally, the roughness correlation length cannot be measured by the AFM image analysis software. Figs. 4.11 and 4.12 respectively show the surface roughness and correlation length before and after filtering the AFM scans of Figs. 4.6-4.10. It can be observed that the surface roughness before filtering is comparable until the concentration of Ge exceeds 50%. For dielectrics on strained $Si_{0.35}Ge_{0.65}$ layer, surface roughness before filtering shows a slight increase due to the partial relaxation of the $Si_{0.35}Ge_{0.65}$ layer (as indicated by Figs. 4.5 and 4.10). After filtering ($\lambda_p = 20$ nm), it can be observed that the nanoscale surface roughness shows a slight increase with increasing Ge. The increase in the nanoscale surface roughness when Ge concentration is increased from 50% to 65% (~ 8 pm) is significantly higher than the increase when Ge concentration is increased from 0% to 50% (~ 3 pm). Although, the increase in roughness with Ge is small (Fig. 4.11), it can be expected to influence mobility [248] and gate dielectric properties [249].

The correlation length shows a reduction with increase in Ge content (Fig. 4.12). This is due to the increased compression in the strained SiGe layer with increasing Ge which reduces the roughness correlation length [84]. According to [84, 117], roughness correlation lengths between 250-350 nm due to surface micro-corrugations can be

expected to adversely influence mobility. Consequently, the correlation lengths observed for the samples studied in this chapter (Fig. 4.12) are unlikely to influence mobility.

$$0\% \text{ Ge}$$
$$R_q = 0.07 \pm 0.01 \text{ nm}$$
$$\Delta_{p\text{-}v} = 2.00 \pm 1.04 \text{ nm}$$
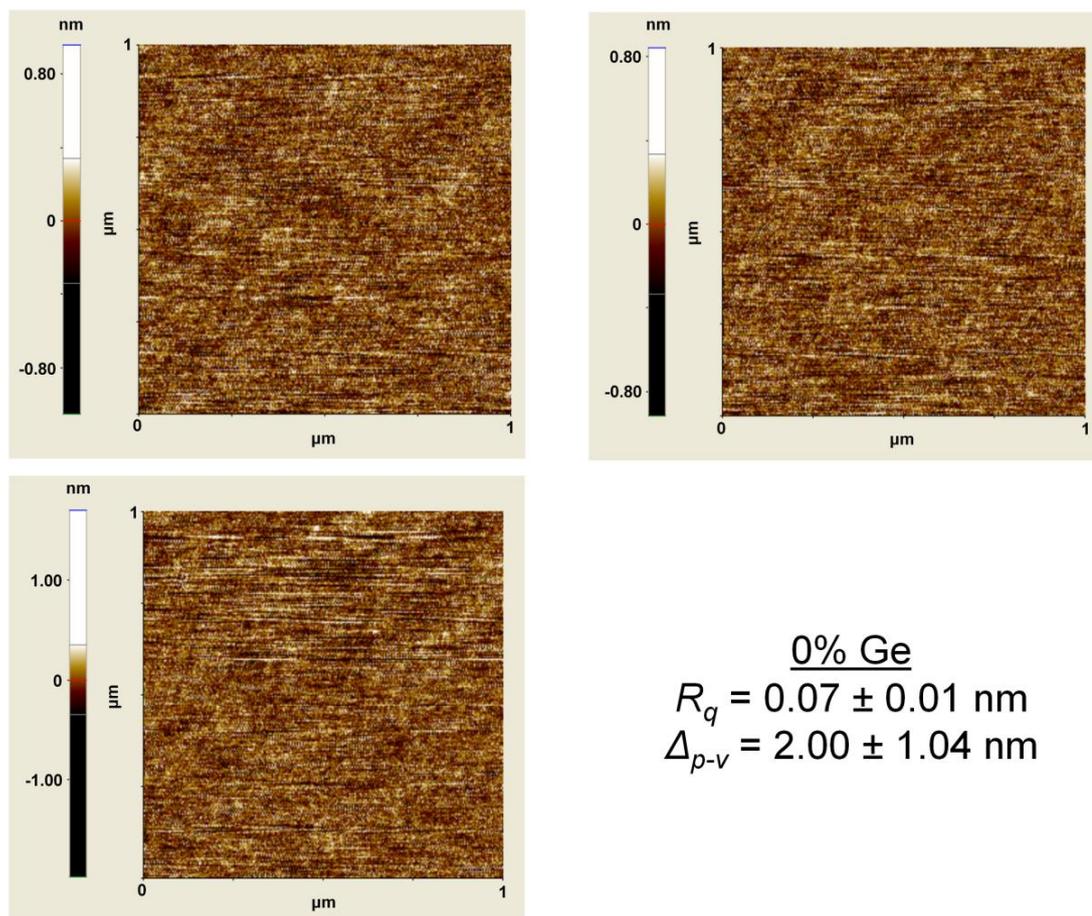
Figure 4.6 High resolution (1024 points/line) topographic maps of SiO$_2$ on bulk-Si obtained in non-contact mode using a sharp tip of radius < 5 nm.
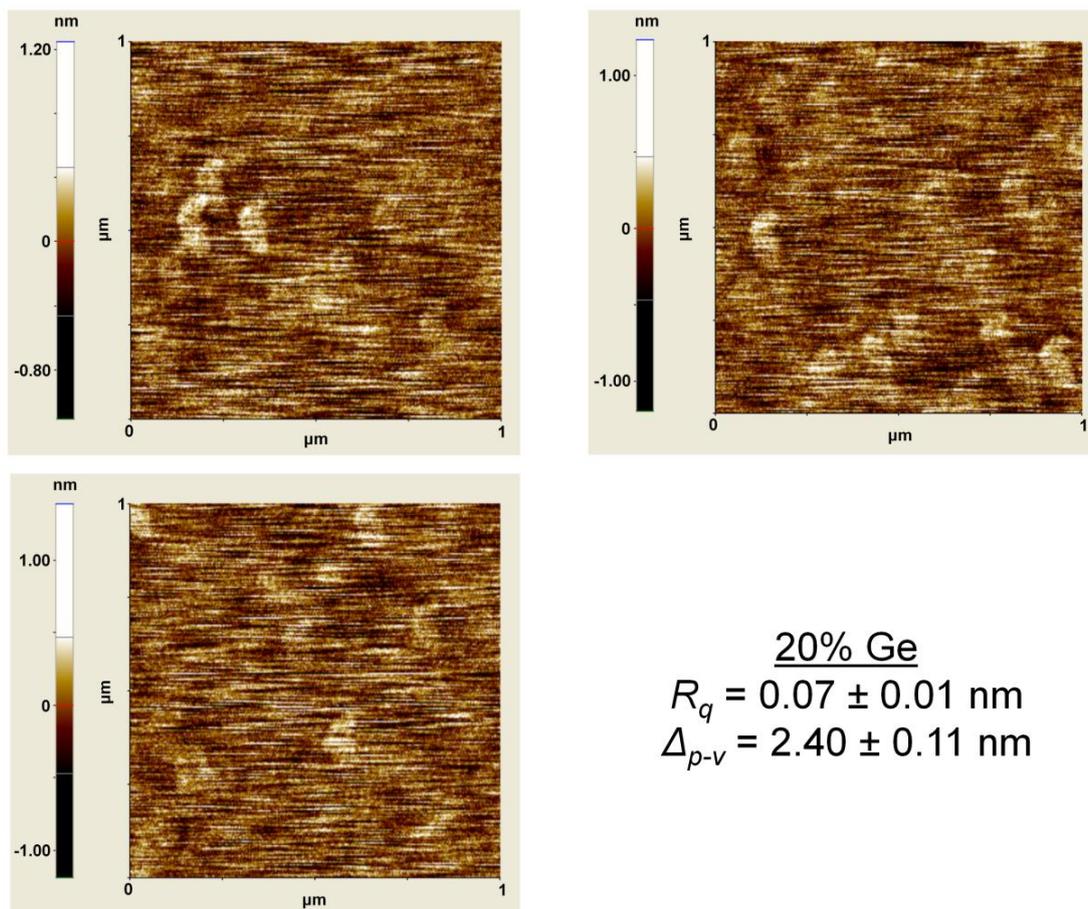
Figure 4.7 High resolution (1024 points/line) topographic maps of SiO$_2$ on Si$_{0.80}$Ge$_{0.20}$ obtained in non-contact mode using a sharp tip of radius < 5 nm.

$$\underline{35\% \text{ Ge}}$$
$$R_q = 0.06 \pm 0.01 \text{ nm}$$
$$\Delta_{p\text{-}v} = 2.70 \pm 0.11 \text{ nm}$$
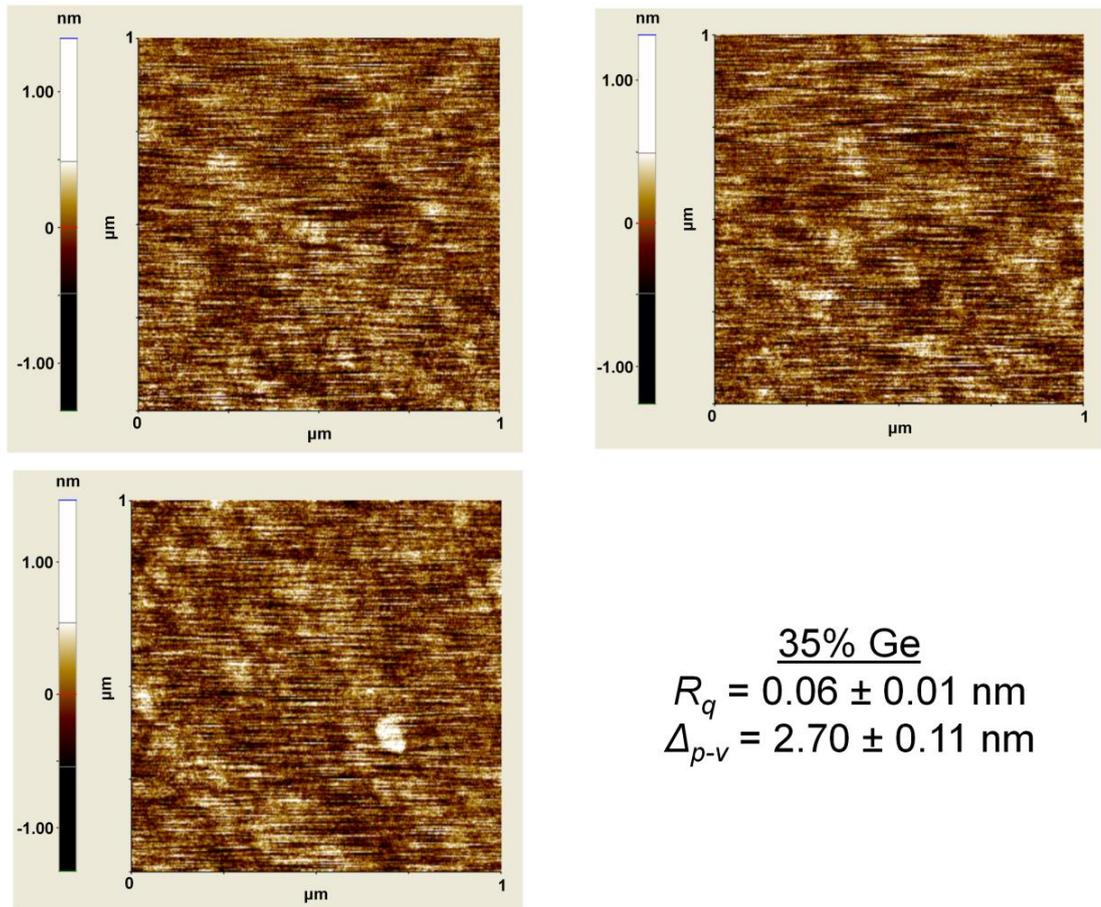
Figure 4.8 High resolution (1024 points/line) topographic maps of SiO$_2$ on Si$_{0.65}$Ge$_{0.35}$ obtained in non-contact mode using a sharp tip of radius < 5 nm.

50% Ge
R_q = 0.07 ± 0.01 nm
$\Delta_{p\text{-}v}$ = 2.10 ± 0.40 nm
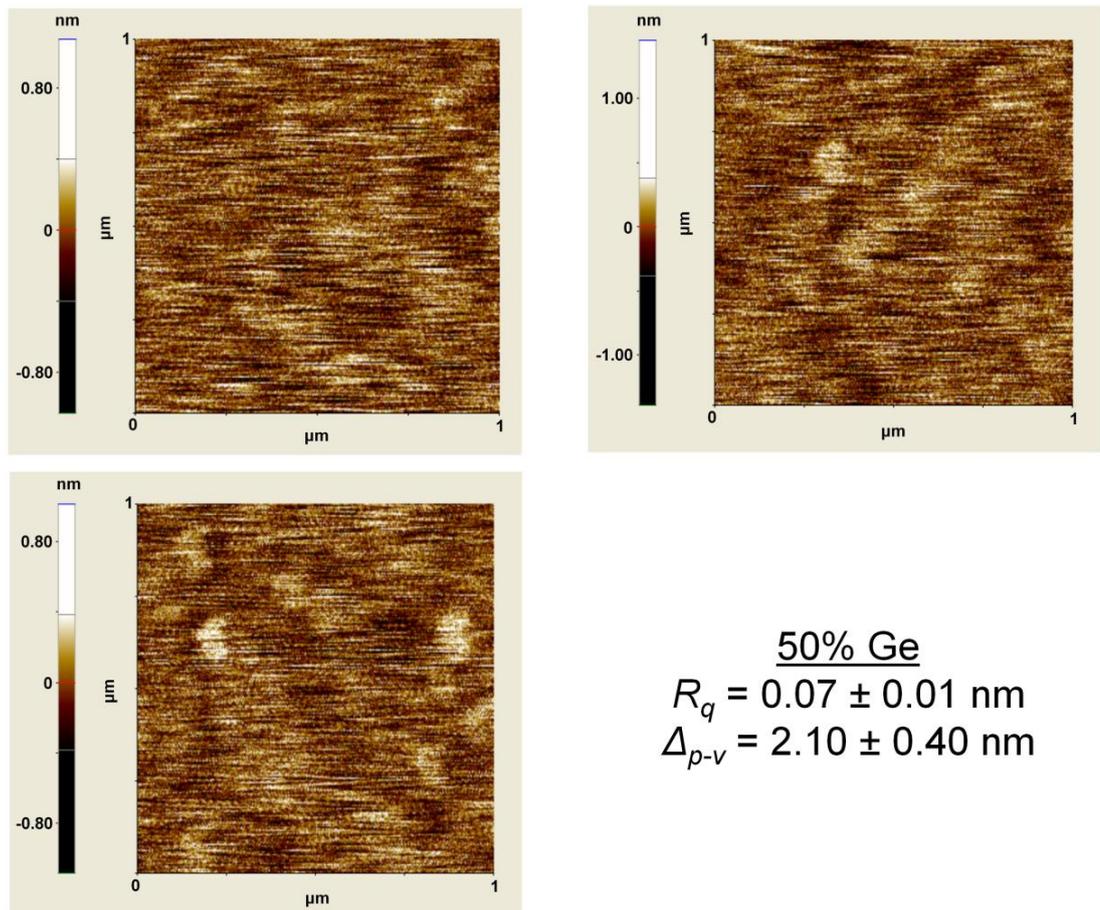
Figure 4.9 High resolution (1024 points/line) topographic maps of SiO₂ on Si$_{0.50}$Ge$_{0.50}$ obtained in non-contact mode using a sharp tip of radius < 5 nm.

65% Ge
R_q = 0.09 ± 0.01 nm
$\Delta_{p\text{-}v}$ = 2.20 ± 0.25 nm
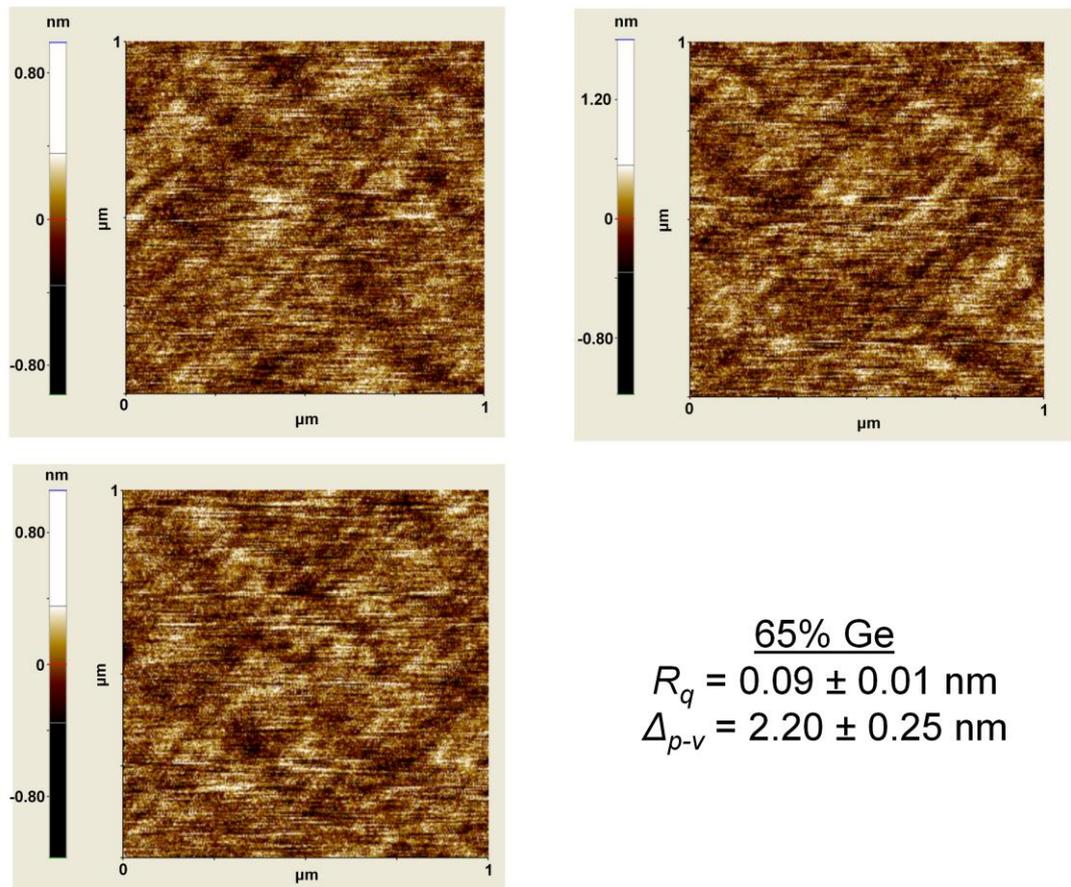
Figure 4.10 High resolution (1024 points/line) topographic maps of SiO₂ on Si$_{0.35}$Ge$_{0.65}$ obtained in non-contact mode using a sharp tip of radius < 5 nm.
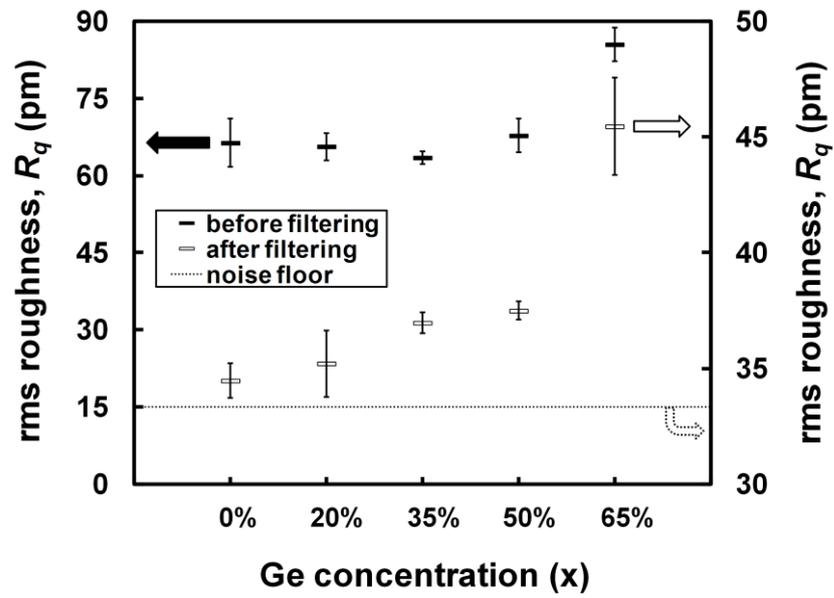
Figure 4.11 Variation in surface roughness before and after filtering with varying Ge.
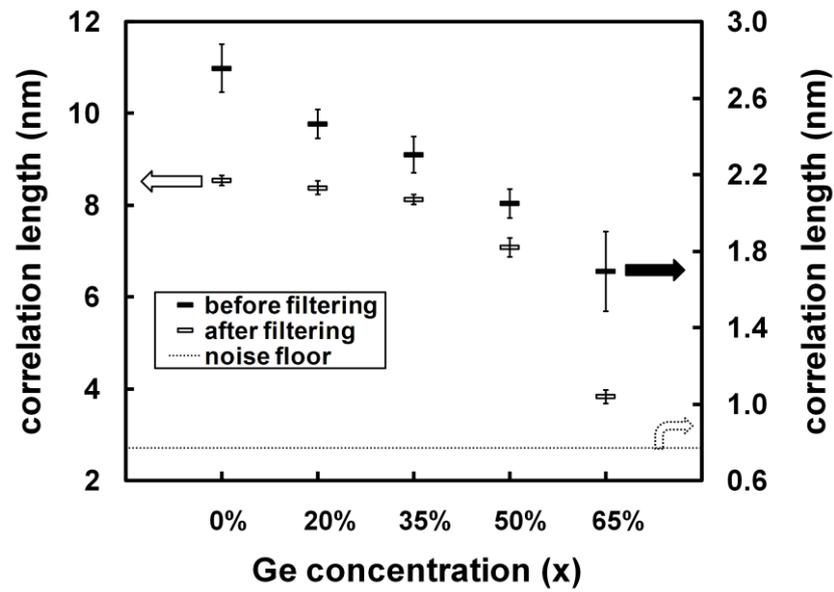
Figure 4.12 Variation in roughness correlation length before and after filtering with varying Ge.

It has been observed that the surface morphology and roughness of SiGe layers studied in this chapter (Figs. 4.6-4.10) is significantly different than most of the previous reports [81-84]. For e.g., a comparison of Figs. 4.6-4.10 with Fig. 4.1 shows that the surface features associated with the samples studied in this work do not exhibit significant change with increasing Ge in the strained alloy. The AFM scans of Figs. 4.6-4.10 exhibit significantly lower values of R_q and Δ_{p-v} compared with the AFM scans in Fig. 4.1. Such improvements in the strained SiGe material quality (Figs. 4.6-4.10) are expected to improve the dielectric reliability and variability in devices which employ such layers as channels.

4.2.6 Strain and degree of relaxation

It is now clear that the $Si_{1-x}Ge_x$ layers are fully strained until the Ge concentration does not exceed 50%. Above this concentration, slight relaxation is to be expected. Following this, XRD curves in Fig. 4.4 have been used to quantify strain (ϵ_{SiGe}) and the degree of relaxation (R_{deg}^{SiGe}) in epitaxially grown compressively strained $Si_{1-x}Ge_x$ layers studied in this chapter. The expressions for ϵ_{SiGe} and R_{deg}^{SiGe} are given by equations 4.4 and 4.5, respectively [92, 166]:

$$\epsilon_{SiGe} = \left(\frac{a_{SiGe}^{\parallel} - a_{SiGe}}{a_{SiGe}} \right), \qquad\qquad \textbf{4.4}$$

$$R_{deg}^{SiGe} = \left(\frac{a_{SiGe}^{\parallel} - a_{Si}}{a_{SiGe} - a_{Si}} \right), \qquad\qquad \textbf{4.5}$$

where, $a_{SiGe}^{\parallel}$ is the in-plane lattice constant of strained SiGe layer and can be calculated from the following equation [92, 153]:

$$a_{SiGe} = \left(\frac{1-\nu}{1+\nu} \right) a_{SiGe}^{\perp} + \left(\frac{2\nu}{1+\nu} \right) a_{SiGe}^{\parallel}, \qquad\qquad \textbf{4.6}$$

The values of $a_{SiGe}^{\perp}$ and a_{SiGe} are calculated from equations 4.1 and 4.2, respectively.

Strain and relaxation for SiGe layers with varying Ge have also been calculated using Raman spectroscopy. Fig. 4.13 shows the Raman spectra obtained from the oxidised SiGe layers with varying Ge using a 457 nm (visible) laser. In total, Raman spectra from 12 different locations were obtained for each sample. For every sample, Raman spectra were found to be identical. For the 457 nm laser incident on compressively strained SiGe layers grown on Si, penetration depth is ~ 40 nm. Consequently, the Si-Si

vibrations from the bulk-Si substrate are also observed (Fig. 4.13). The position of the Si-Si lattice vibrations in the SiGe layers shifts towards the lower side compared with the Si-Si lattice vibrations in bulk-Si (~ 521 cm^{-1}) with increasing Ge indicating increasing levels of compressive strain [148]. The intensity of Si-Si vibrations in the SiGe layers reduce for higher Ge levels. Si-Ge and Ge-Ge lattice vibrations are clearly visible for higher Ge contents (50% and 65%).
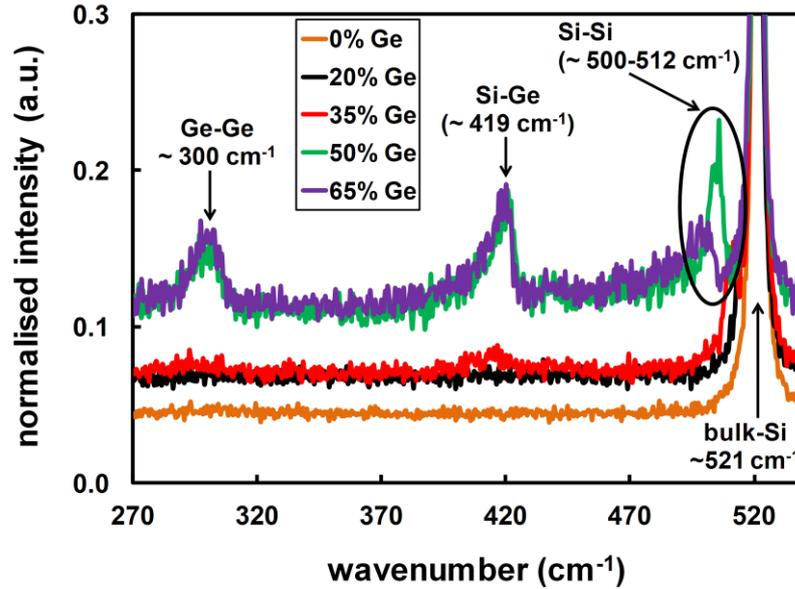
Figure 4.13 Raman spectra from the oxidised SiGe layers with varying Ge. Laser Wavelength: 457 nm (visible). Differences in Si-Si, Si-Ge and Ge-Ge lattice vibrations can be observed indicating different levels of strain.

For compressively strained SiGe layers on bulk-Si, the vibrational properties in the Raman spectra of Fig. 4.13 can be used to estimate the level of ε_{SiGe} [148]:

$$\varepsilon_{SiGe} = \left(\frac{520.7 - \omega_{Si-Si}^{s-SiGe} - 66.9x}{730}\right), \qquad \textbf{4.7}$$

$$\varepsilon_{SiGe} = \left(\frac{400.1 - \omega_{Si-Ge}^{s-SiGe} + 24.5x - 4.5x^2 - 33.5x^3}{570}\right), \qquad \textbf{4.8}$$

$$\varepsilon_{SiGe} = \left(\frac{280.3 - \omega_{Ge-Ge}^{s-SiGe} + 19.4x}{450}\right), \qquad \textbf{4.9}$$

where, ω_{Si-Si}^{s-SiGe}, ω_{Si-Ge}^{s-SiGe} and ω_{Ge-Ge}^{s-SiGe} are the Si-Si, Si-Ge and Ge-Ge lattice vibrations in the SiGe alloy, respectively.

The values of ϵ_{SiGe} and R_{deg}^{SiGe} obtained using XRD and Raman spectroscopy have been shown in Fig. 4.14. Due to its compressive nature, the value of strain is negative. It can be observed that the magnitude of strain increases with Ge content. This is expected since the lattice mismatch (which dictates the level of strain) between epitaxial $Si_{1-x}Ge_x$ layer and the underlying Si substrate increases with increasing Ge. Fig. 4.14 confirms that $Si_{1-x}Ge_x$ layers are fully strained for Ge concentrations up to 50% while slight relaxation (~ 4% with XRD and ~ 2% with Raman spectroscopy) is observed for the $Si_{0.35}Ge_{0.65}$ layers.
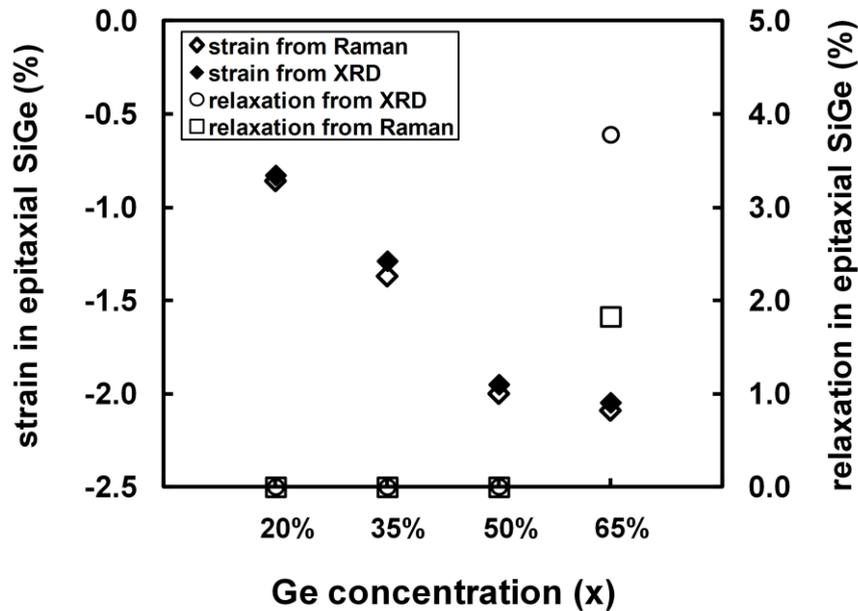
Figure 4.14 Level of strain and degree of relaxation in epitaxial Si₁₋ₓGeₓ layers grown on bulk-Si.

Table 4.3 compares the values of ϵ_{SiGe} obtained from XRD and Raman spectroscopy with the theoretical values (equation 4.4) for fully strained SiGe layers. Overall, a strong agreement between the values of ϵ_{SiGe} from XRD and Raman spectroscopy has been observed. Strain calculated from Raman spectroscopy has been found to be higher than the theoretical values (Table 4.3). This error may have occurred during peak fitting and the calculation of strain using equations 4.7-4.9 since various groups have reported different equations for calculating strain from Raman spectroscopy. Once ϵ_{SiGe} was calculated using Raman spectroscopy, the values of $a_{SiGe}^{\parallel}$ were obtained by using

equation 2.3. This was followed by the calculation of R_{deg}^{SiGe} using equation 2.5. Consequently, the difference in the values of ϵ_{SiGe} obtained from XRD and Raman spectroscopy is reflected in the values of R_{deg}^{SiGe} as shown in Fig. 4.14.

Table 4.3 Comparison of the values of strain calculated from XRD and Raman spectroscopy with theoretical values for fully strained SiGe layers with varying Ge. The difference in the values of strain from XRD and Raman spectroscopy for the Si$_{0.35}$Ge$_{0.65}$ layer explains the difference in the values of relaxation obtained from the two techniques in Fig. 4.14.

Sample	Theoretical Strain (%)	Strain from XRD (%)	Strain from Raman spectroscopy (%)
Si$_{0.80}$Ge$_{0.20}$	-0.83	-0.82	-0.86
Si$_{0.65}$Ge$_{0.35}$	-1.29	-1.28	-1.37
Si$_{0.50}$Ge$_{0.50}$	-1.95	-1.96	-2.00
Si$_{0.35}$Ge$_{0.65}$	-2.13	-2.05	-2.09

4.3 Gate leakage and reliability analysis of $SiO_2/Si_{1-x}Ge_x/Si$ stacks

Nanoscale gate leakage, localised breakdown and spatial variations in thickness of dielectrics on strained SiGe layers have been studied using C-AFM. These are now discussed.

4.3.1 Topography and leakage current maps

Figs. 4.15-4.19 show 5×5 μm^2 topography (left) and current (right) maps obtained by scanning the surface of SiO_2 on SiGe layers with varying Ge content (from 0 to 65%). In total, 3 scans from each sample were measured at different substrate applied dc bias. The scans have been obtained using conductive diamond coated tips of radius ~ 100 nm. It can be seen that the surface topography of the dielectric (SiO_2) grown on fully strained SiGe layers with different Ge contents is very smooth with no definite features. Fig. 4.20 compares the values of R_q with varying Ge obtained using the conductive diamond coated C-AFM tips. No significant difference in surface roughness with Ge has been observed during C-AFM measurements. Dielectric surface roughness on $Si_{0.35}Ge_{0.65}$ layer shows a slight increase compared with other concentrations of Ge. The small scale morphological features due to slight relaxation in the $Si_{0.35}Ge_{0.65}$ layer (Figs. 4.5 and 4.10) were not observed during C-AFM scanning. This may be because C-AFM scans have been carried out in contact mode using tips with a relatively large radius (~ 100 nm in this case) due to the conductive coating. This may result in certain small scale roughness features (such as small height undulations and "short lines") not being recorded during C-AFM scanning.

Electrical SPM techniques generally suffer from lower resolution compared with topographic modes of AFM. This is because of the conductive coating on the tips used for electrical SPM measurements which increases the effective contact area. This issue can be mitigated by employing conductive tips with lower radius. Alternatively, surface roughness and electrical analysis can be carried out separately. This is useful when smooth surfaces (similar to those studied in this chapter) are required to be analysed.
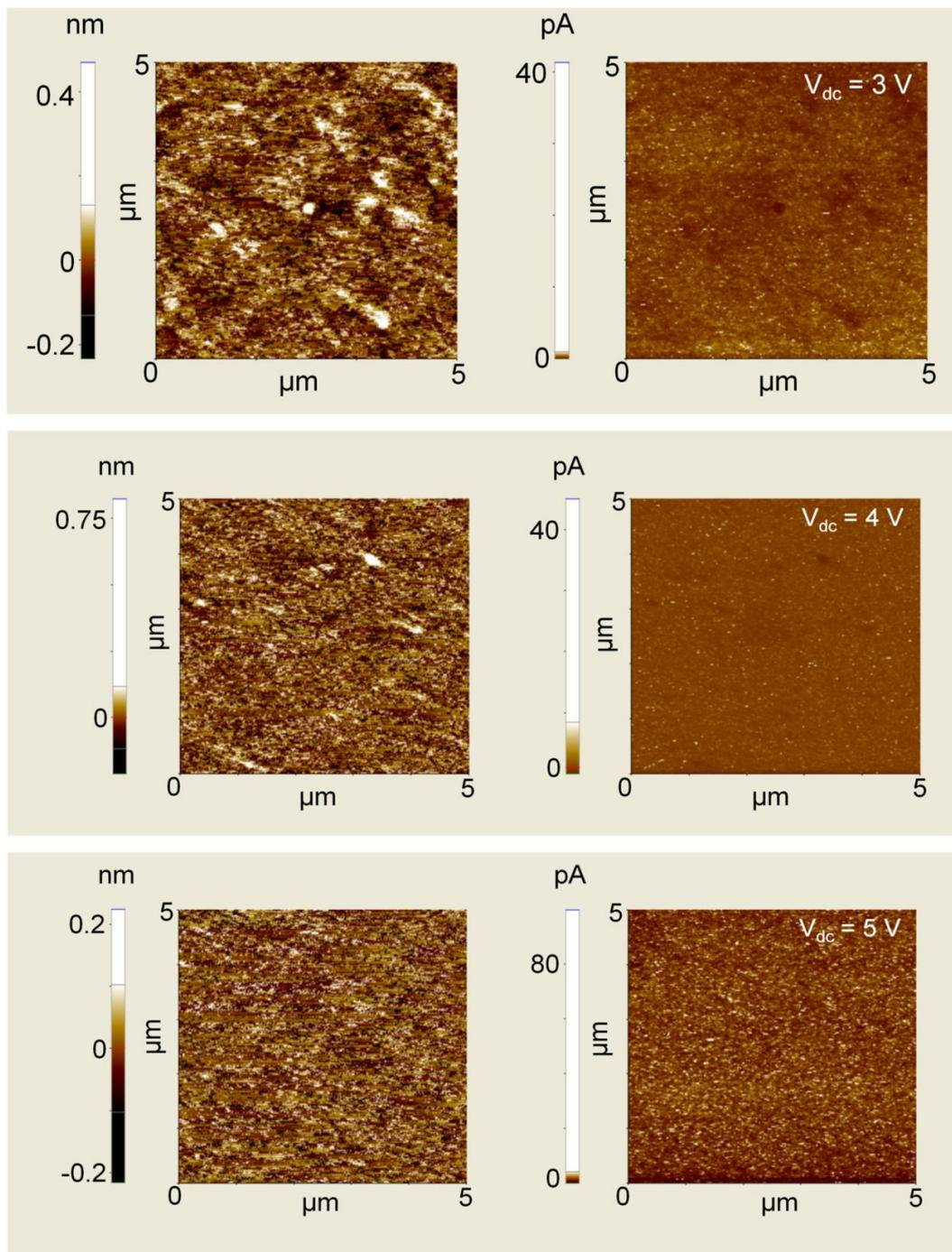
Figure 4.15 Simultaneously obtained topography and current maps from SiO₂ on bulk-Si. The applied dc substrate bias is 3 V, 4 V and 5 V.
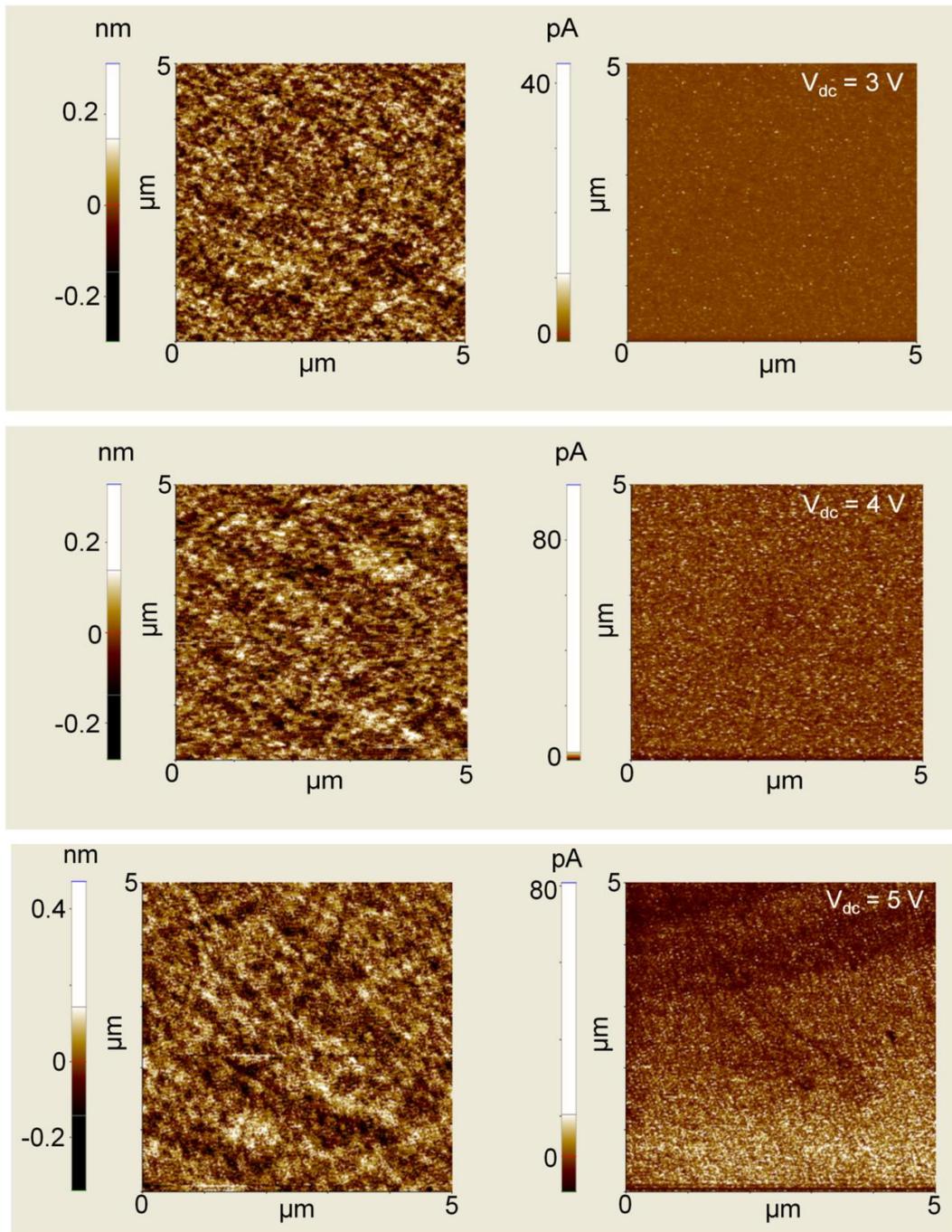
Figure 4.16 Simultaneously obtained topography and current maps from SiO$_2$ on Si$_{0.80}$Ge$_{0.20}$. The applied dc substrate bias is 3 V, 4 V and 5 V.
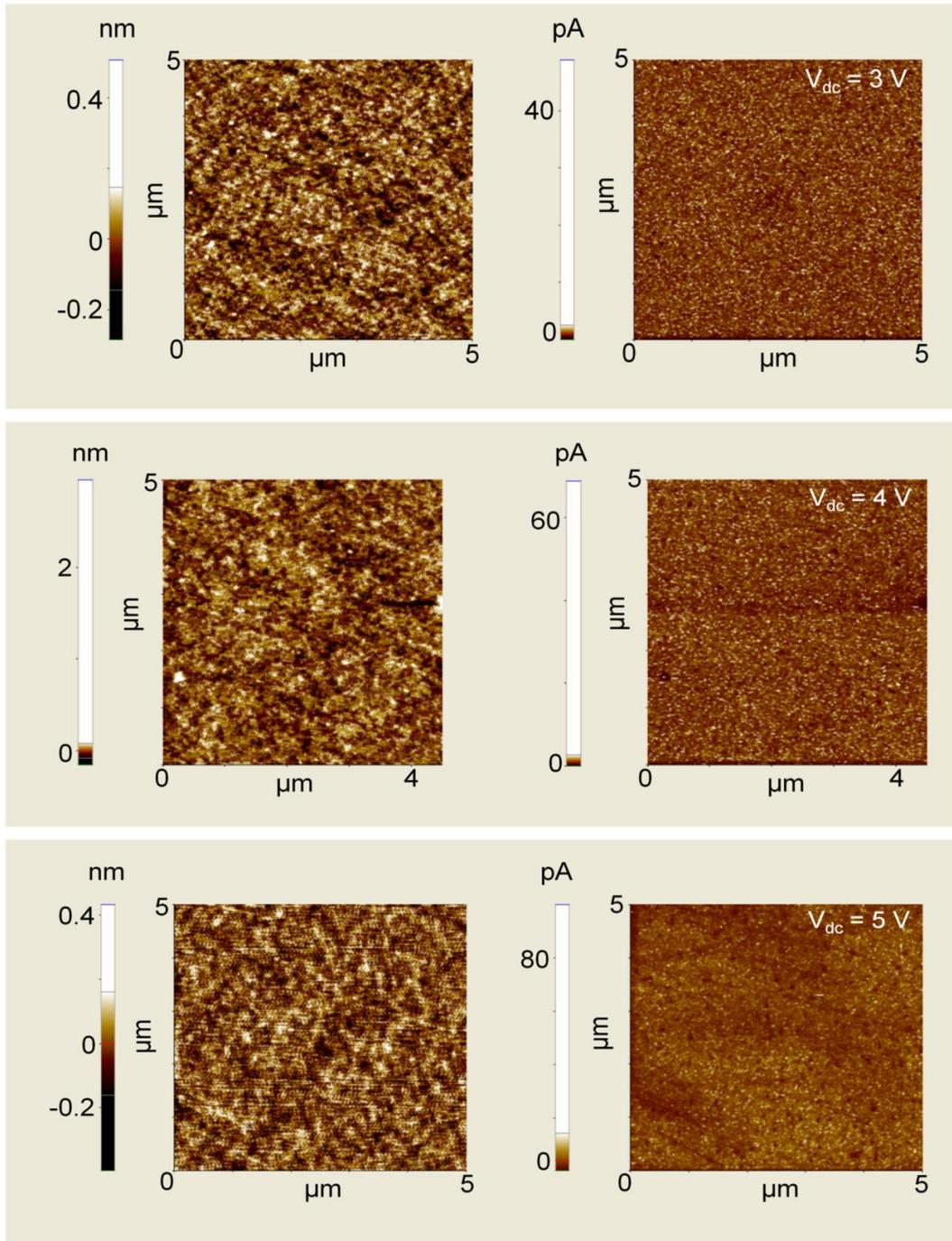
Figure 4.17 Simultaneously obtained topography and current maps from SiO$_2$ on Si$_{0.65}$Ge$_{0.35}$. The applied dc substrate bias is 3 V, 4 V and 5 V.
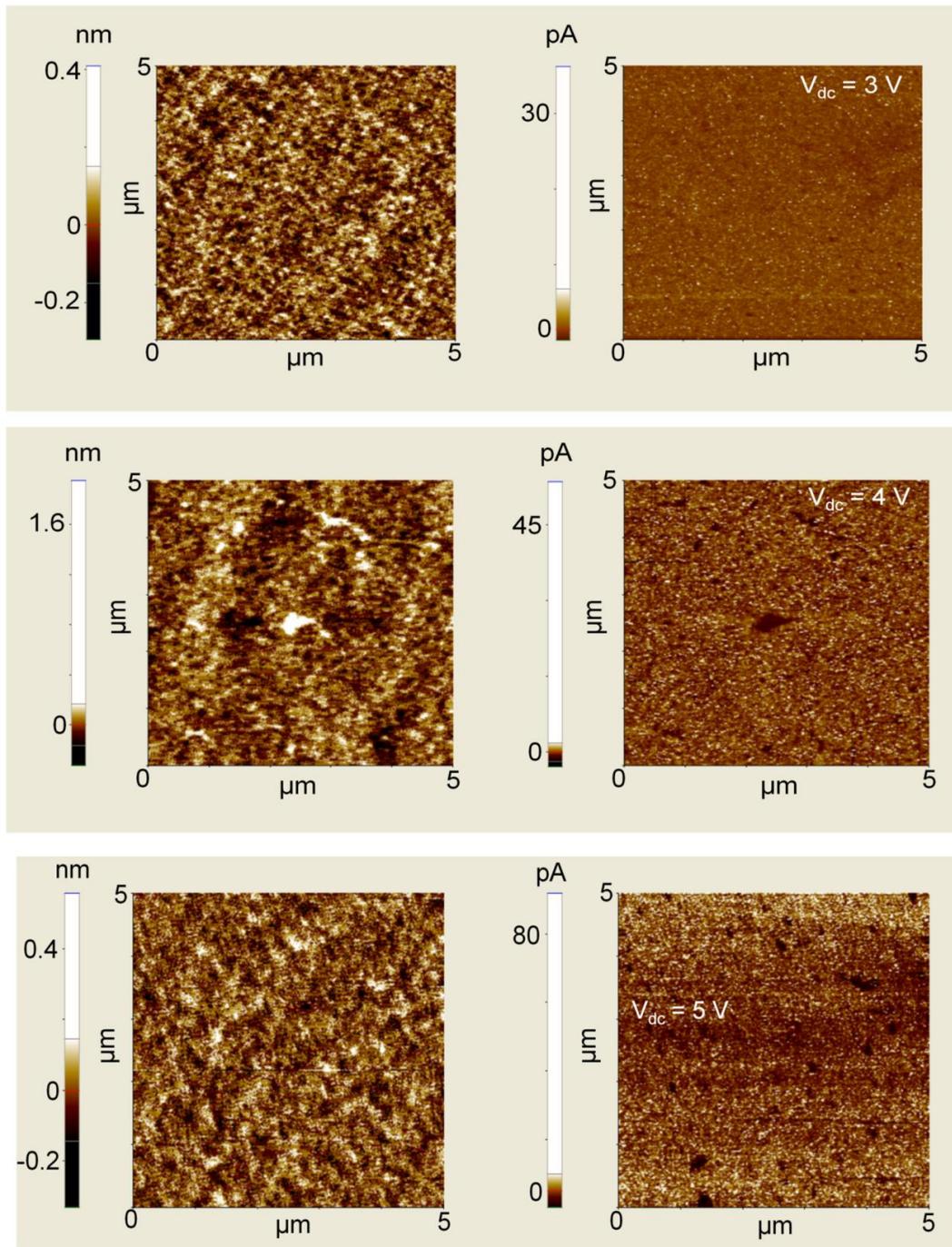
Figure 4.18 Simultaneously obtained topography and current maps from SiO$_2$ on Si$_{0.50}$Ge$_{0.50}$. The applied dc substrate bias is 3 V, 4 V and 5 V.
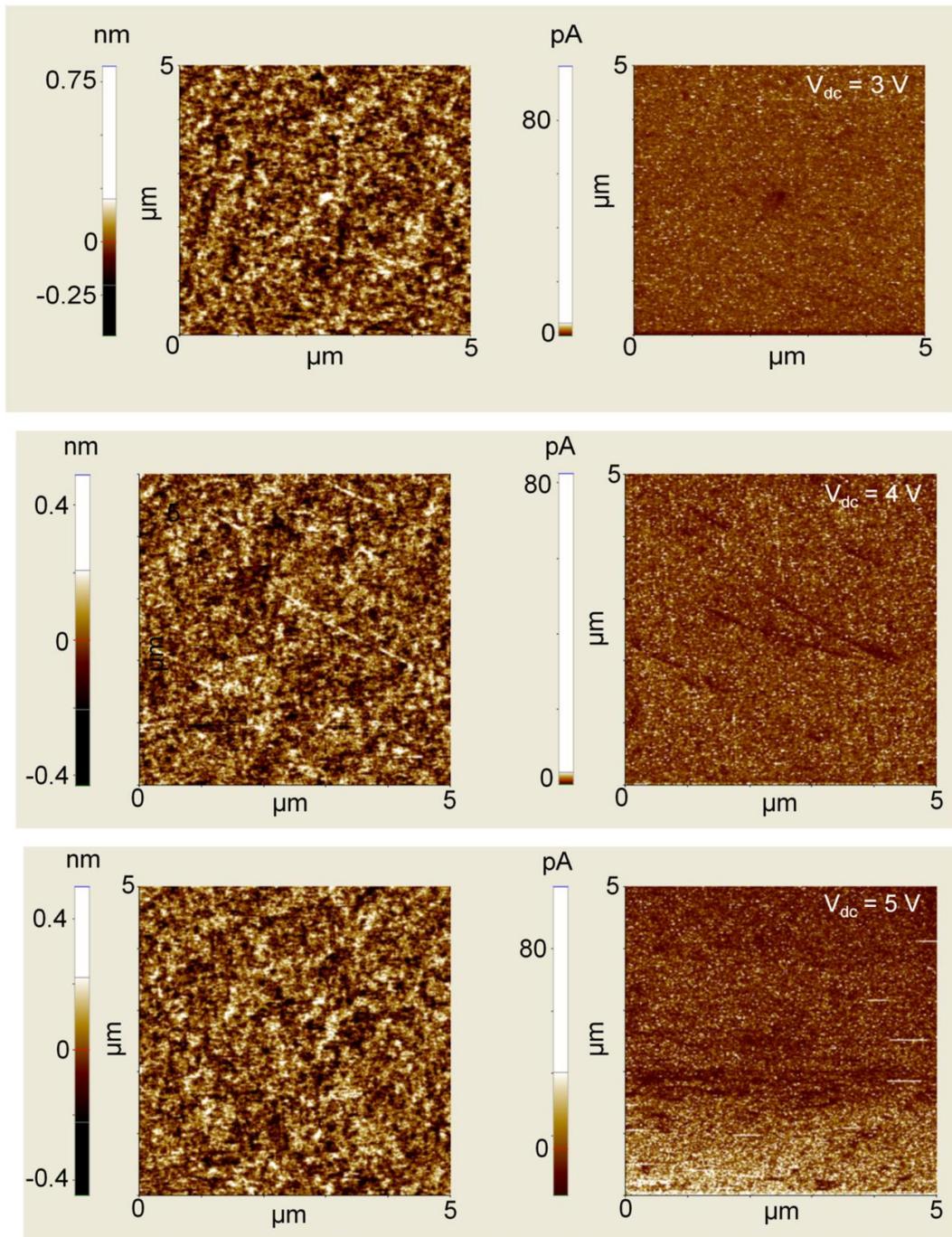
Figure 4.19 Simultaneously obtained topography and current maps from SiO$_2$ on Si$_{0.35}$Ge$_{0.65}$. The applied dc substrate bias is 3 V, 4 V and 5 V.
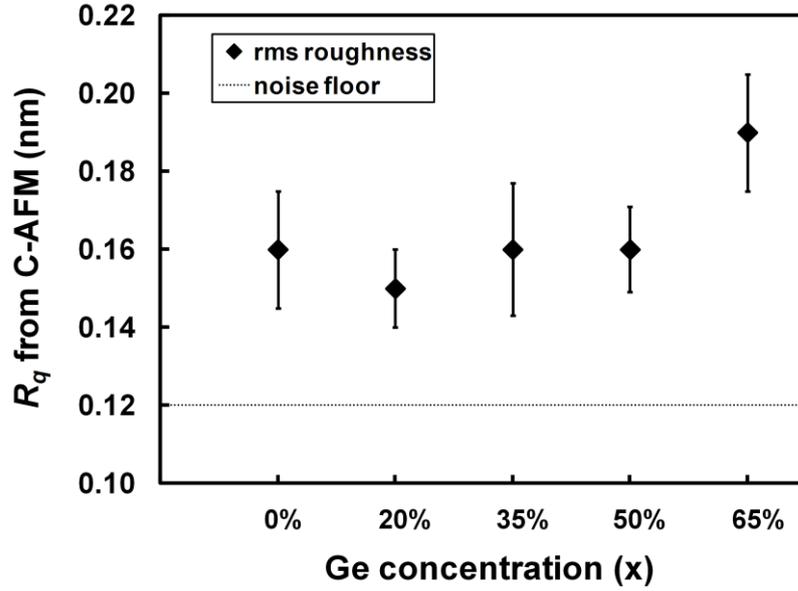
Figure 4.20 Variation in rms surface roughness (R_q) with varying Ge obtained by the conductive diamond coated C-AFM tips.

Clearly, in the absence of any definite morphological pattern (Figs. 4.15-4.19), leakage hotspots have been found to be randomly distributed for all the samples. This shows that if morphological instabilities (such as ripples and surface undulations, often associated with epitaxially grown strained Si/SiGe layers) can be avoided, a highly uniform distribution of gate leakage can be obtained.

Although no morphological dependence of gate leakage has been found, C-AFM maps in Figs. 4.15-4.19 appear to be showing differences in the density of leakage hotspots (bright regions) with varying Ge. This is supported by Fig. 4.21 which shows the variation in average nanoscale J_g with Ge at different E_{ox}. The values of J_g in Fig. 4.21 were calculated by calculating A_{eff} using equations 2.11-2.14 as described in section 2.5.4. The values of E_{ox} in Fig. 4.21 were obtained using equations 2.20 and 2.21. Since blanket layers have been studied in this chapter, nanoscale V_{FB} was accounted for by the workfunction difference (equation 2.16). The values of φ_s (required to calculate V_{FB}) were calculated using the following equation [13]:

$$\varphi_s = \chi + \frac{E_g}{2q} + \psi_s,$$
4.10

where, χ is the electron affinity and E_g is the energy bandgap of the strained SiGe layer while ψ_s is the potential difference between the intrinsic Fermi level and the Fermi level

of the doped semiconductor (strained SiGe). The values of χ, E_g and ψ_s vary with the level of Ge (and hence strain) in the strained $Si_{1-x}Ge_x$ alloy.
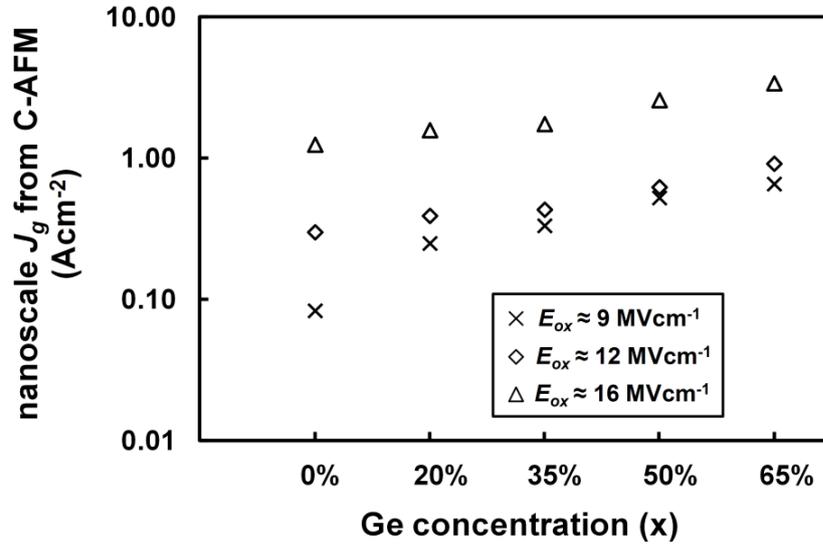
Figure 4.21 Average nanoscale J_g through SiO_2 on epitaxial $Si_{1-x}Ge_x$ layers with varying Ge content at different levels of nanoscale E_{ox}. The values of J_g and E_{ox} were obtained by using equations 2.11-2.14, 2.20 and 2.21. The values of different parameters required to calculate J_g and E_{ox} for strained SiGe layers with varying Ge have been included in Table 4.4.

Clearly, an increase in J_g is observed with increasing Ge content (Fig. 4.21). This trend is not surprising as SiGe channel devices have previously exhibited increased levels of macroscopic J_g compared with bulk-Si channel devices [69, 101, 242]. For strained SiGe, χ is comparable with bulk-Si [64]. Consequently, any influence of χ on J_g in strained SiGe devices (in comparison with bulk-Si) is negligible. Another parameter which influences J_g is the transverse effective mass experienced by the charge carriers. Compressive strain in SiGe causes preferential occupation of charge carriers in the LH bands where transverse effective mass is lower than the unstrained condition [250]. It is known that decrease in transverse effective mass increases leakage currents [22, 73, 104]. According to [250], the transverse effective mass reduces with increasing Ge (and strain) in strained SiGe alloys. This implies increase in J_g with increasing Ge for dielectrics on strained SiGe layers. The SiO_2/Si valence band offsets may also play a secondary role in increasing J_g with Ge [105]. Increased out-diffused Ge to the channel surface has also been identified as a reason for enhanced J_g in SiGe channel devices

[242]. Since oxidation has been carried out at a relatively low temperature (600 °C), diffusion of Ge is likely to be low [62, 119, 251]. Additionally, the possibility of a thin Si cap (section 4.2.4) means that the influence of Ge segregation is likely to be low.

At lower fields, leakage is generally modelled by trap assisted tunnelling or TAT due to out-diffused Ge as it is the dominating mechanism (section 3.1). At higher fields (V_{ox} > φ_B), F-N leakage (t_{ox} dependent) is expected to dominate [97]. Direct tunnelling (DT) through the dielectric generally dominates for dielectrics with t_{ox} < 3 nm and at $V_{ox} < \varphi_B$ [97]. For the samples studied here, t_{ox} is close to 3 nm (2.85 nm) which indicates that DT can also occur. Diffusion of Ge is likely to be low (relatively low oxidation temperature). Consequently, the level of TAT and DT (if present) may be low. For a 2.85 nm thick dielectric grown on strained SiGe layers, $V_{ox} = \varphi_B$ corresponds to an E_{ox} ~ 12 MVcm^{-1}. This means that F-N leakage is expected to dominate at E_{ox} > 12 MVcm^{-1}. Fig. 4.21 shows a ~ 4-fold increase in J_g with Ge for E_{ox} > 12 MVcm^{-1}. At relatively lower fields (E_{ox} = 9 MVcm^{-1} and 12 MVcm^{-1}), J_g is comparable for all Ge concentrations (except for bulk-Si). This suggests low levels of TAT and DT at low fields and dominance of F-N leakage at high fields.

4.3.2 Localised gate leakage behaviour

Spectroscopic C-AFM *I-V* curves were also obtained from 15-20 random locations to study the localised resilience of the dielectric to electrical stress. These were then converted to J_g-E_{ox} curves using the equations described in section 2.5.4 and equation 4.10. Like strained Si, electrical and material parameters change for strained SiGe layers with varying Ge. The values for various parameters required for obtaining J_g-E_{ox} curves have been included in Table 4.4 [64, 184, 185, 252].

J_g-E_{ox} curves for each sample are shown in Fig. 4.22. Differences in leakage response have been observed with varying Ge concentration. This difference is better observed when one typical J_g-E_{ox} curve for each Ge concentration is compared, as shown in Fig. 4.23. An increase in J_g with Ge has been observed. Leakage curves from Ge-rich samples (50% and 65% Ge) reach the current limit of the measurement setup (100 pA) before Si-rich samples. This implies that dielectrics on Ge-rich layers are expected to break earlier than Si-rich samples. The increase in J_g with Ge is further highlighted by the histogram in Fig. 4.24 which shows the variation in nanoscale J_g at E_{ox} = 18 MVcm^{-1} for different concentrations of Ge.

Table 4.4 Material and electrical parameters required for calculating J_g, E_{ox} and $V_{FB, ideal}$ for SiO$_2$/Si$_{1-x}$Ge$_x$ stacks with different Ge contents [64, 184, 185, 252].

Parameter	Si	Si$_{0.80}$Ge$_{0.20}$	Si$_{0.65}$Ge$_{0.35}$	Si$_{0.50}$Ge$_{0.50}$	Si$_{0.35}$Ge$_{0.65}$
χ (eV)	4.05	4.03	4.03	4.05	4.04
E_g (eV)	1.12	1.00	0.90	0.81	0.73
N_c (cm^{-3})	2.80 x 10^{19}	1.95 x 10^{19}	1.95 x 10^{19}	1.95 x 10^{19}	1.95 x 10^{19}
N_v (cm^{-3})	2.50 x 10^{19}	8.70 x 10^{18}	5.50 x 10^{18}	3.70 x 10^{18}	2.50 x 10^{18}
n_i (cm^{-3})	1.03 x 10^{10}	5.18 x 10^{10}	2.85 x 10^{11}	1.33 x 10^{12}	5.15 x 10^{12}
ψ_s (V)	0.30	0.26	0.21	0.17	0.14
φ_S (eV)	4.91	4.79	4.69	4.63	4.55
φ_m (Dia.) (eV)	4.80	4.80	4.80	4.80	4.80
φ_m (Pt) (eV)	5.60	5.60	5.60	5.60	5.60
$V_{FB, ideal}$ (V)	0.69	0.81	0.91	0.97	1.05
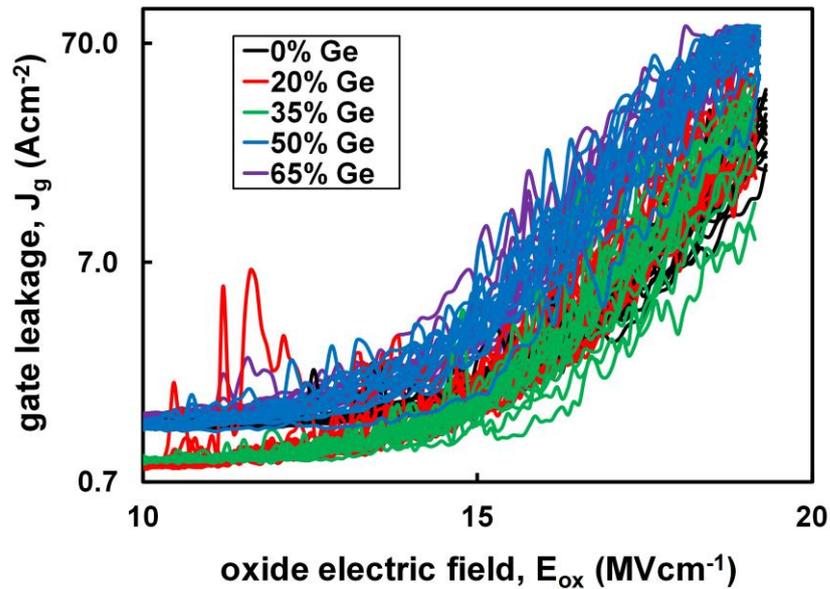
Figure 4.22 Localised J_g-E_{ox} curves obtained from the surface of SiO$_2$ on epitaxial Si$_{1-x}$Ge$_x$ layers with varying Ge content.
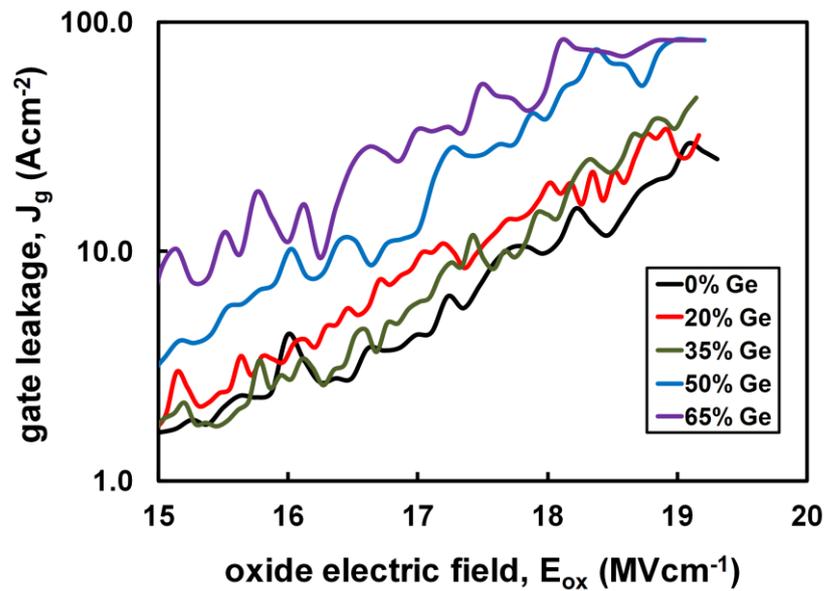
Figure 4.23 Typical J_g-E_{ox} curves from the surface of SiO_2 on epitaxial $Si_{1-x}Ge_x$ layers with varying Ge content.
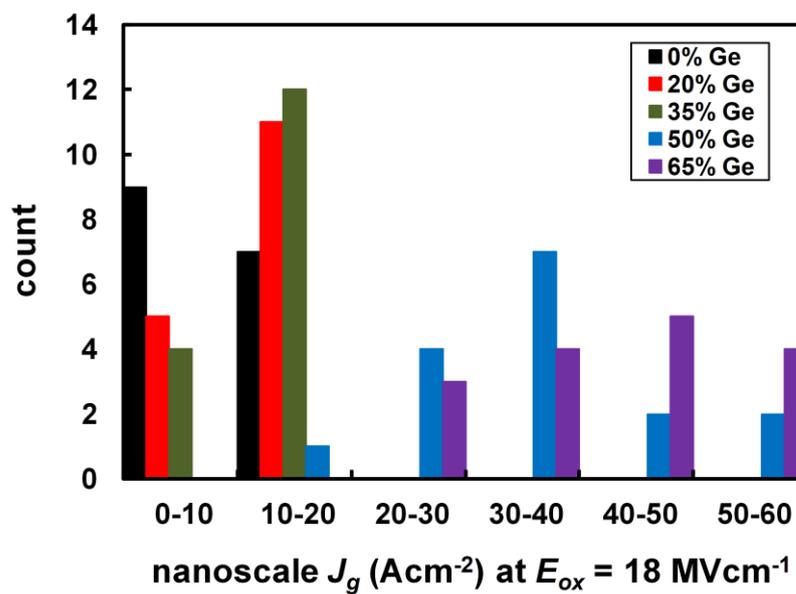
Figure 4.24 Histogram showing the variation in nanoscale J_g at E_{ox} = 18 $MVcm^{-1}$ with varying Ge.

4.3.3 Comparison of leakage at the nanoscale and macroscale

Fig. 4.25 compares the nanoscale J_g at $E_{ox} = 18$ MVcm[-1] (this work) with previously reported macroscopic leakage data [68, 69, 166, 233, 242, 253-259] from SiGe channel devices with varying Ge. It can be observed that nanoscale J_g (at $E_{ox} = 18$ MVcm[-1]) with varying Ge is comparable with previously reported macroscopic values at similar E_{ox}. For the highest Ge concentration (65%) studied in this work, nanoscale J_g is comparable with macroscopic J_g for lower concentrations at similar E_{ox}.
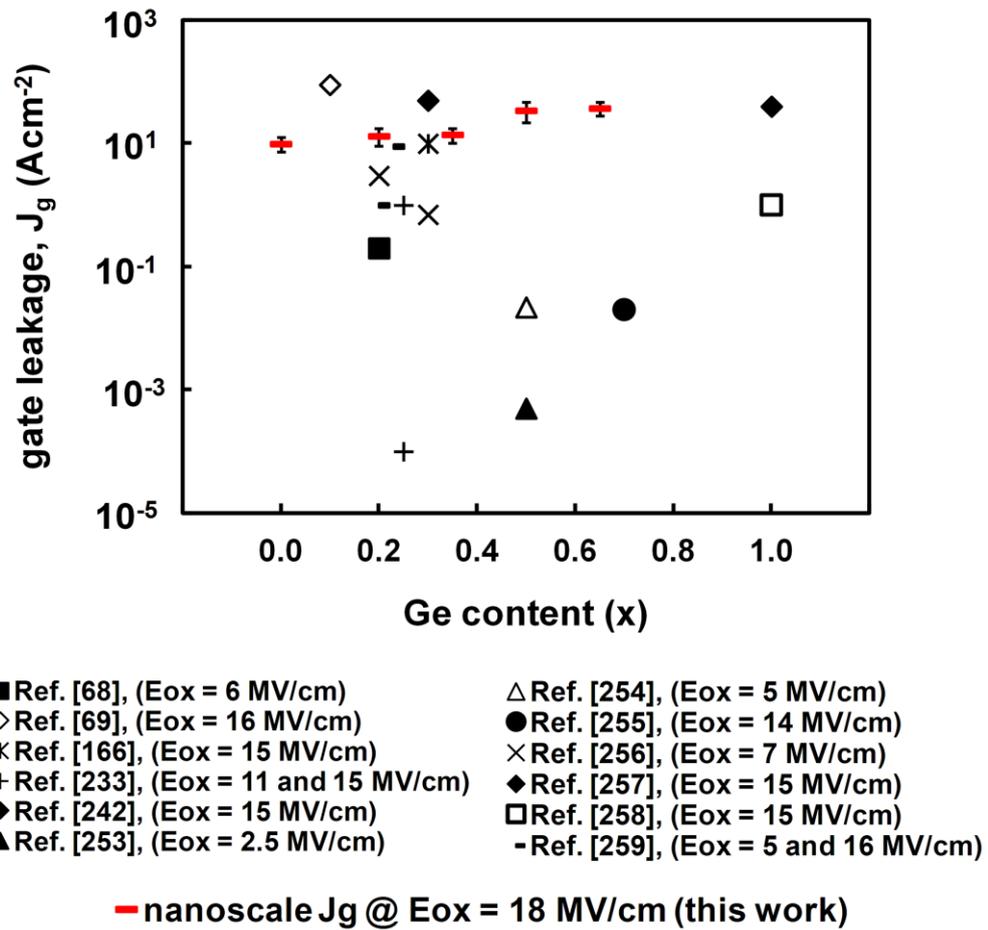
Figure 4.25 Comparison of nanoscale J_g at $E_{ox} = 18$ MVcm[-1] (this work) with previously reported device level data [68, 69, 166, 233, 242, 253-259].

Increased J_g with Ge (Figs. 4.21-4.24) means that devices which employ compressively strained SiGe channels are subject to a potential trade-off between carrier mobility and power consumption (J_g). The comparison of nanoscale J_g with previously

reported macroscopic data (Fig. 4.25) indicates that 65% Ge in the strained SiGe alloy can be implemented as an optimum concentration for improving carrier mobility whilst maintaining acceptable levels of gate leakage. This is a step towards realizing high performance strained Ge channels with acceptable levels of gate dielectric leakage.

4.3.4 Localised variations in dielectric thickness

Fig. 4.26 shows the F-N plots of the typical leakage curves shown in Fig. 4.23. Linear behaviour at high electric fields indicates dominance of F-N tunnelling at these fields. Following this, leakage curves were modelled in the F-N regime using equations 2.22-2.24.
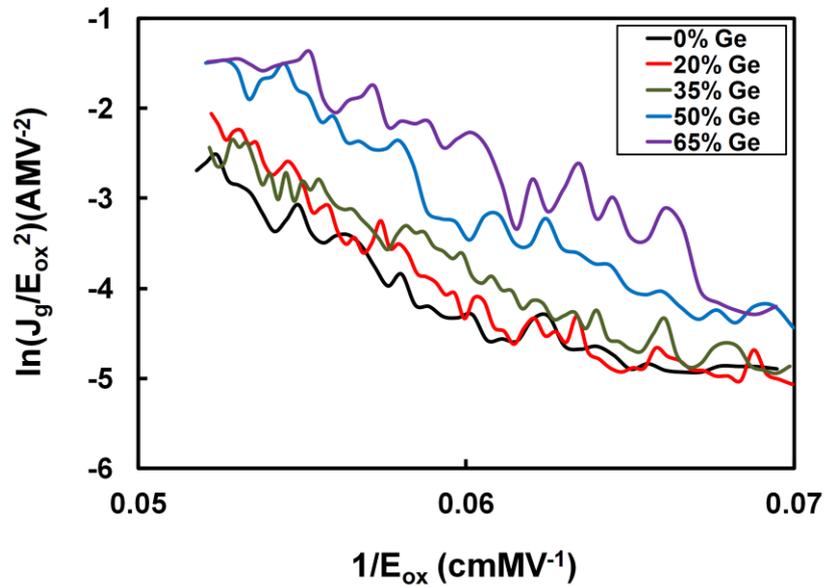
Figure 4.26 F-N plot of typical leakage curves shown in Fig. 4.23. Linear behaviour indicates dominance of F-N leakage at high fields.

The values for m_{ox} (as a factor of m) and φ_B for $SiO_2/Si_{1-x}Ge_x$ stacks with different Ge contents have been included in Table 4.5 [64, 189]. Model F-N curves were superposed on experimental leakage curves in Fig. 4.22 while t_{ox} was varied to achieve the best fit.

The values of t_{ox} obtained by superposing experimental leakage curves on F-N model curves are shown in Fig. 4.27. The values of t_{ox} obtained at the nanoscale (Fig. 4.27) are in close agreement with the macroscopic value of 2.85 nm and also indicate a uniform dielectric.

Table 4.5 Values for m_{ox} and φ_B required to model nanoscale leakage curves in the F-N regime [64, 189].

Sample	m_{ox}	φ_B
Si	$0.40m$	3.30
$Si_{0.80}Ge_{0.20}$	$0.40m$	3.28
$Si_{0.65}Ge_{0.35}$	$0.40m$	3.28
$Si_{0.50}Ge_{0.50}$	$0.40m$	3.30
$Si_{0.35}Ge_{0.65}$	$0.40m$	3.29
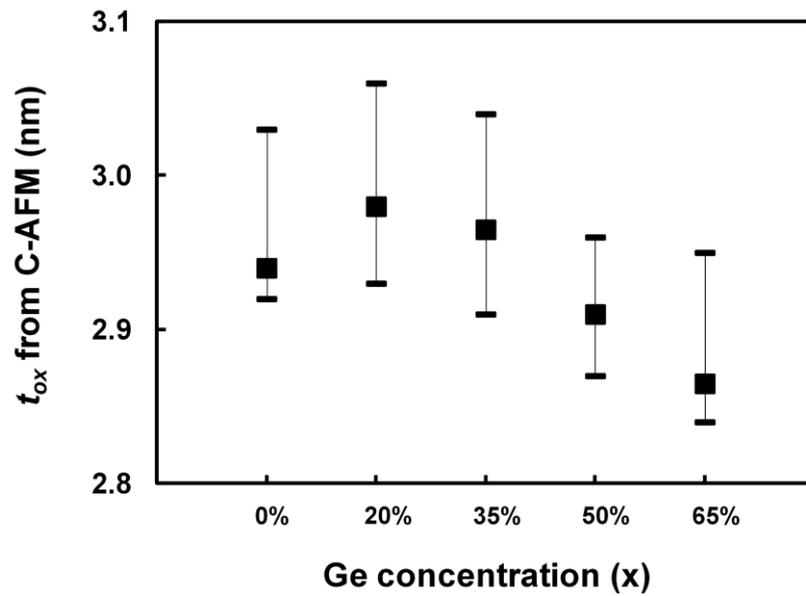
Figure 4.27 Localised variations (< 2 Å) in t_{ox} obtained by modelling C-AFM leakage curves in the F-N regime.

4.4 Interface quality of SiO$_2$/Si$_{1-x}$Ge$_x$ stacks studied using SCM

4.4.1 Topography and capacitance maps

Figs. 4.28-4.32 show 5×5 µm^2 topography (left) and capacitance (right) maps obtained by scanning the surface of SiO$_2$ on SiGe layers with varying Ge content (from 0 to 65%). In total, 3 scans from each sample have been obtained from different locations at a dc bias of 0 V under ac lock-in conditions of 2 V_{rms} and 20 kHz. The scans have been obtained using conductive PtIr5 coated tips of radius ~ 25 nm.

The smooth morphology and absence of any definite features further confirms the pseudomorphic nature of the strained SiGe layers. Slight relaxation induced small scale features (Figs. 4.5 and 4.10) in the Si$_{0.35}$Ge$_{0.65}$ layer were not observed during SCM scanning which used tips with a radius lower than the diamond coated C-AFM tips. Fig. 4.33 compares R_q with varying Ge obtained during SCM scanning. The values of R_q in Fig. 4.33 are similar to the values observed during C-AFM scanning (Fig. 4.20).

Localised variations in surface morphology caused by variations in dielectric thickness cause SCM maps to be an inverse image of topography (section 3.3.2). A closer look at the topography and SCM images of Figs. 4.28-4.32 shows that SCM images inversely follow the small scale features in the topography for Ge concentration $\geq$ 20%.

With a smooth morphology (Figs. 4.28-4.32) and uniform t_{ox} (Fig. 4.27), it may be possible to spatially map the interface quality through a thorough spectroscopic analysis of the SCM images in Figs. 4.28-4.32.
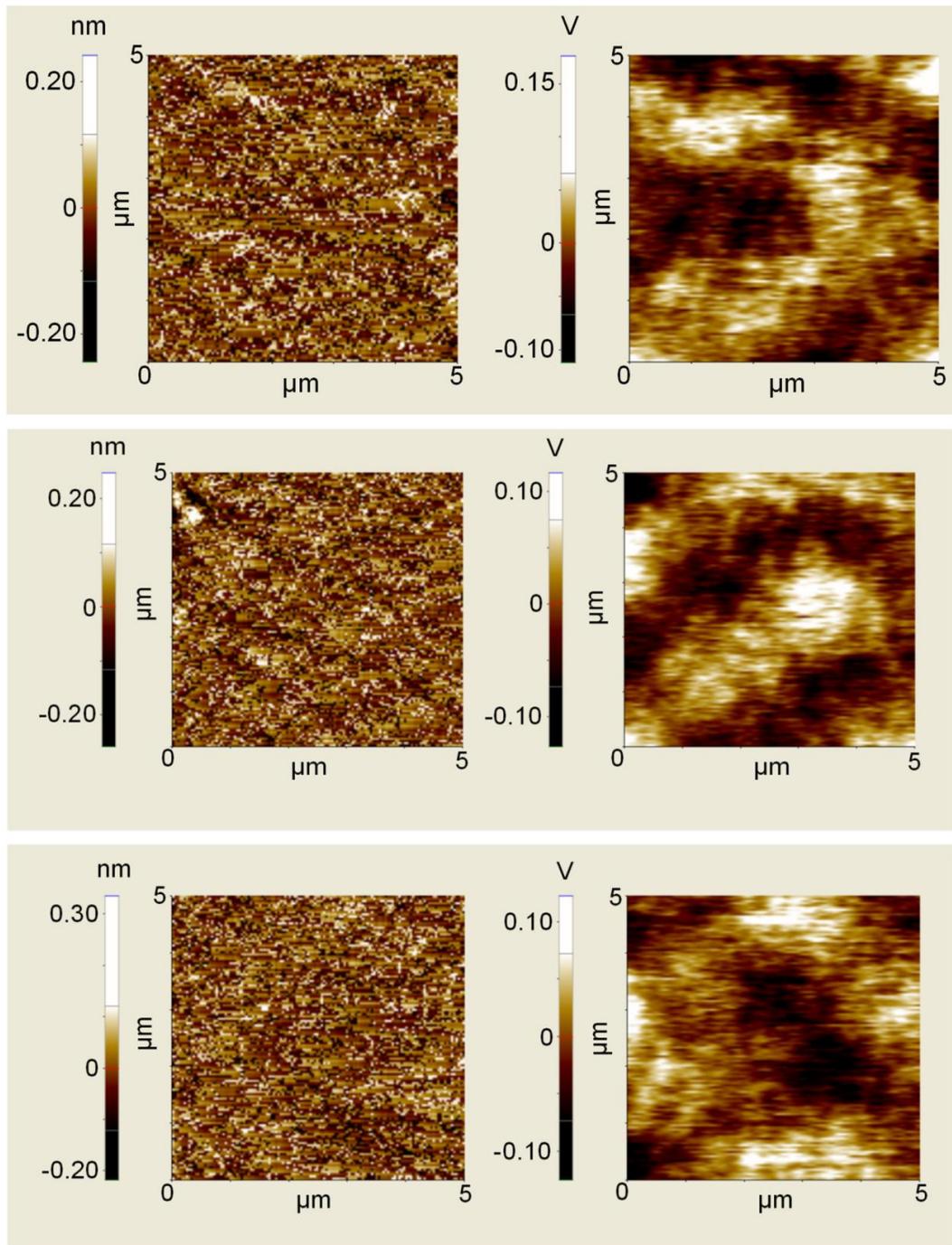
Figure 4.28 Simultaneously obtained topography (left) and capacitance (right) maps from SiO$_2$ on bulk-Si. Parameters: V_{dc} = 0 V, V_{ac} = 2 V_{rms} and f_{ac} = 20 kHz.
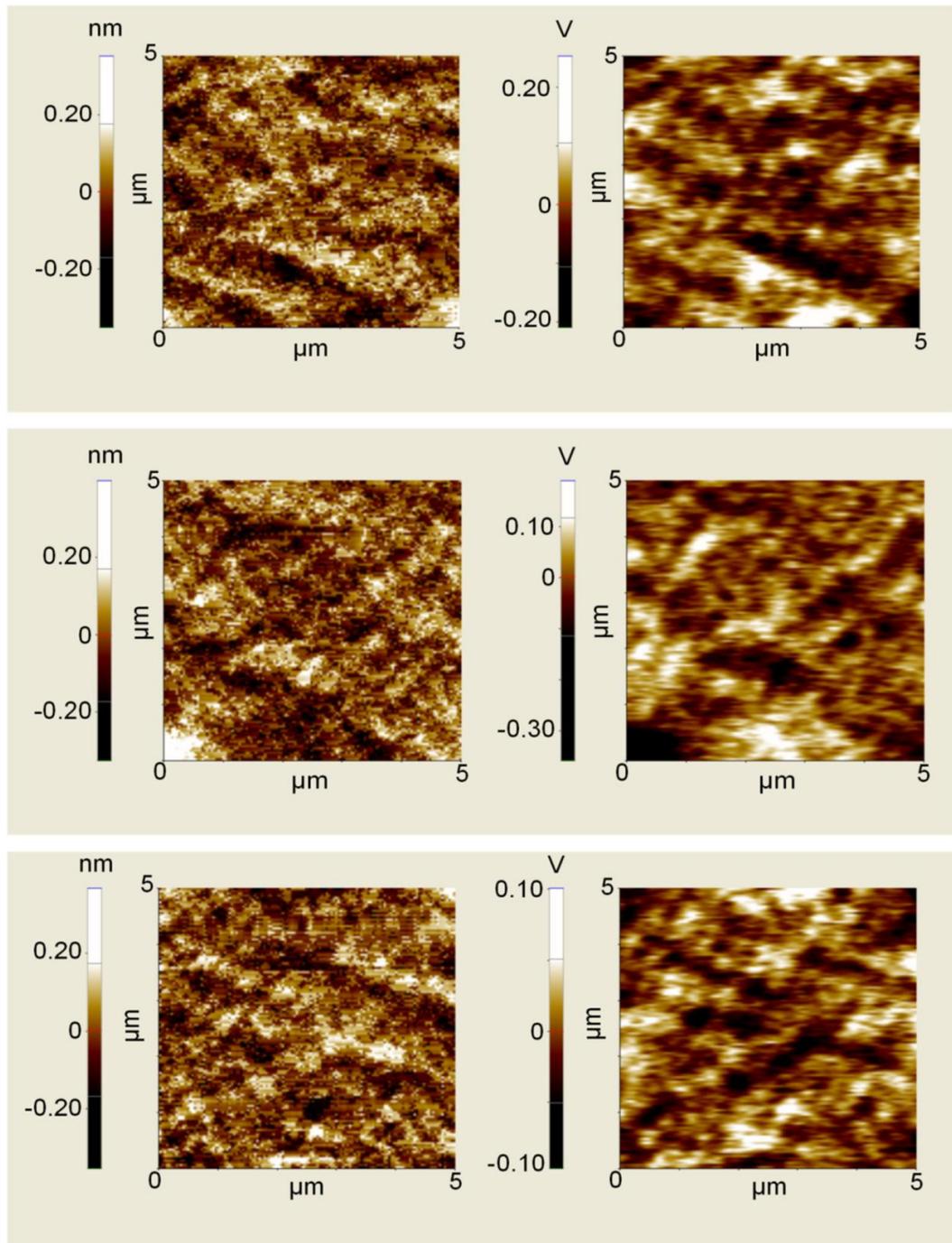
Figure 4.29 Simultaneously obtained topography (left) and capacitance (right) maps from SiO$_2$ on strained Si$_{0.80}$Ge$_{0.20}$. Parameters: $V_{dc} = 0$ V, $V_{ac} = 2$ V_{rms} and $f_{ac} = 20$ kHz.
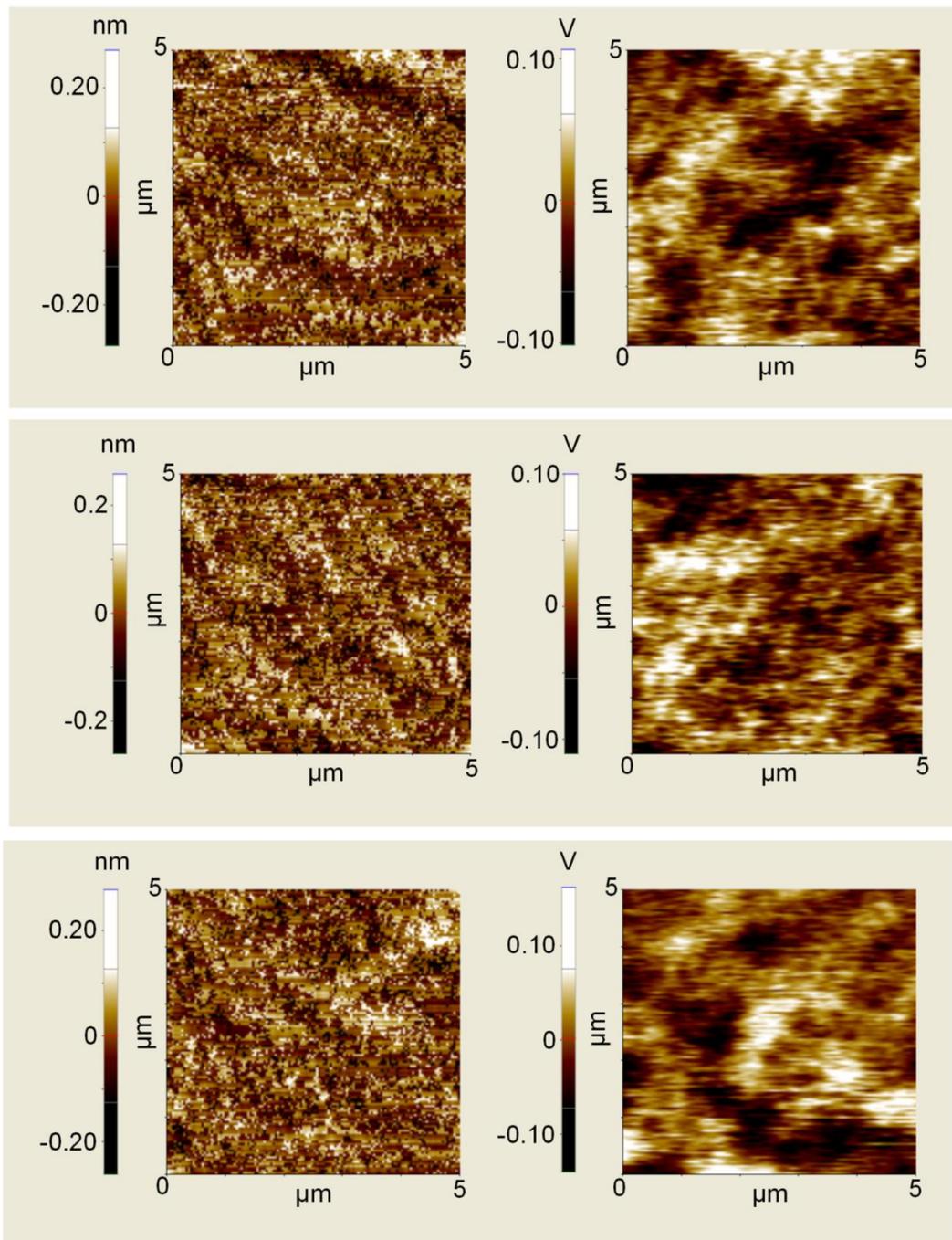
Figure 4.30 Simultaneously obtained topography (left) and capacitance (right) maps from SiO$_2$ on strained Si$_{0.65}$Ge$_{0.35}$. Parameters: $V_{dc} = 0$ V, $V_{ac} = 2$ V_{rms} and $f_{ac} = 20$ kHz.
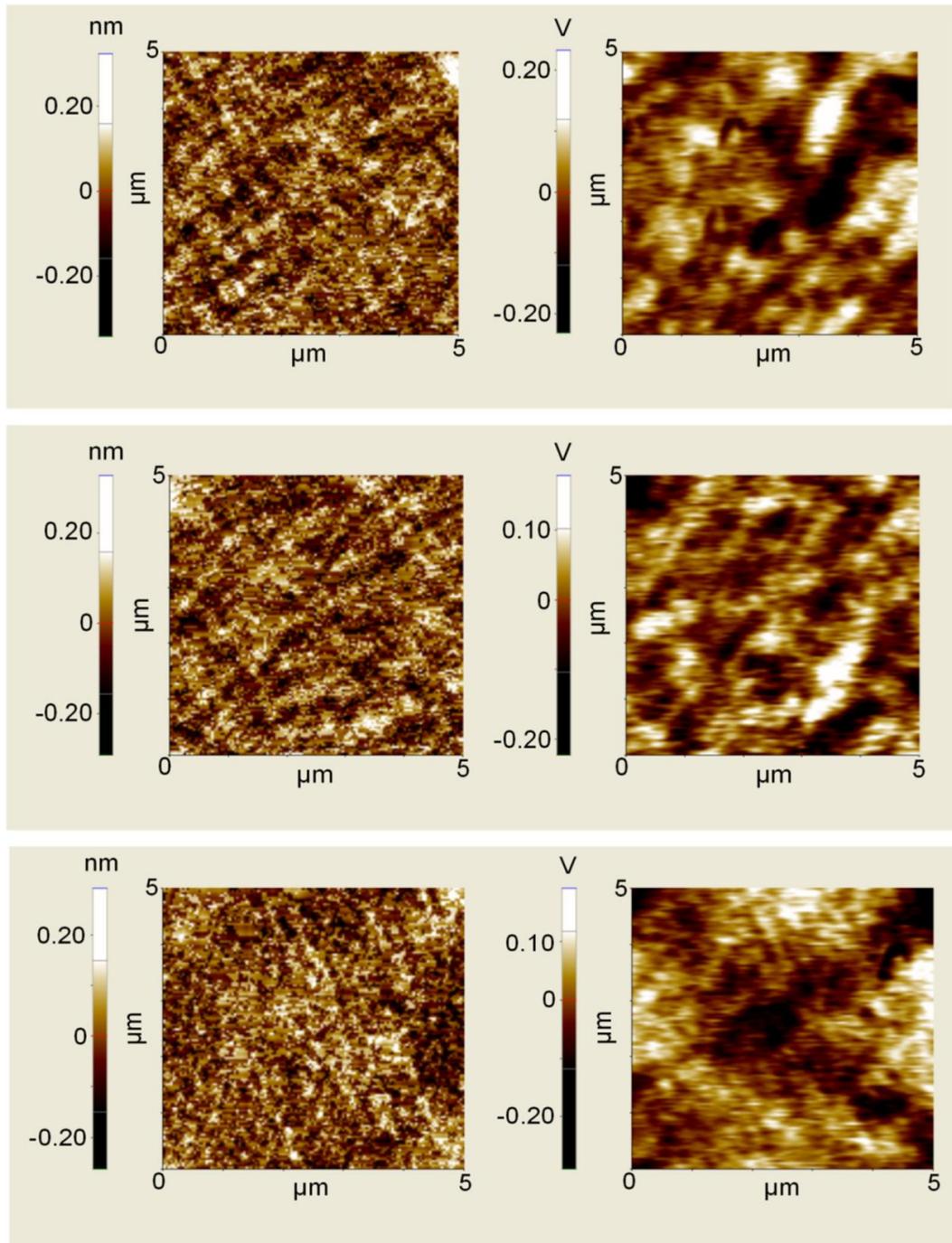
Figure 4.31 Simultaneously obtained topography (left) and capacitance (right) maps from SiO$_2$ on strained Si$_{0.50}$Ge$_{0.50}$. Parameters: V_{dc} = 0 V, V_{ac} = 2 V_{rms} and f_{ac} = 20 kHz.
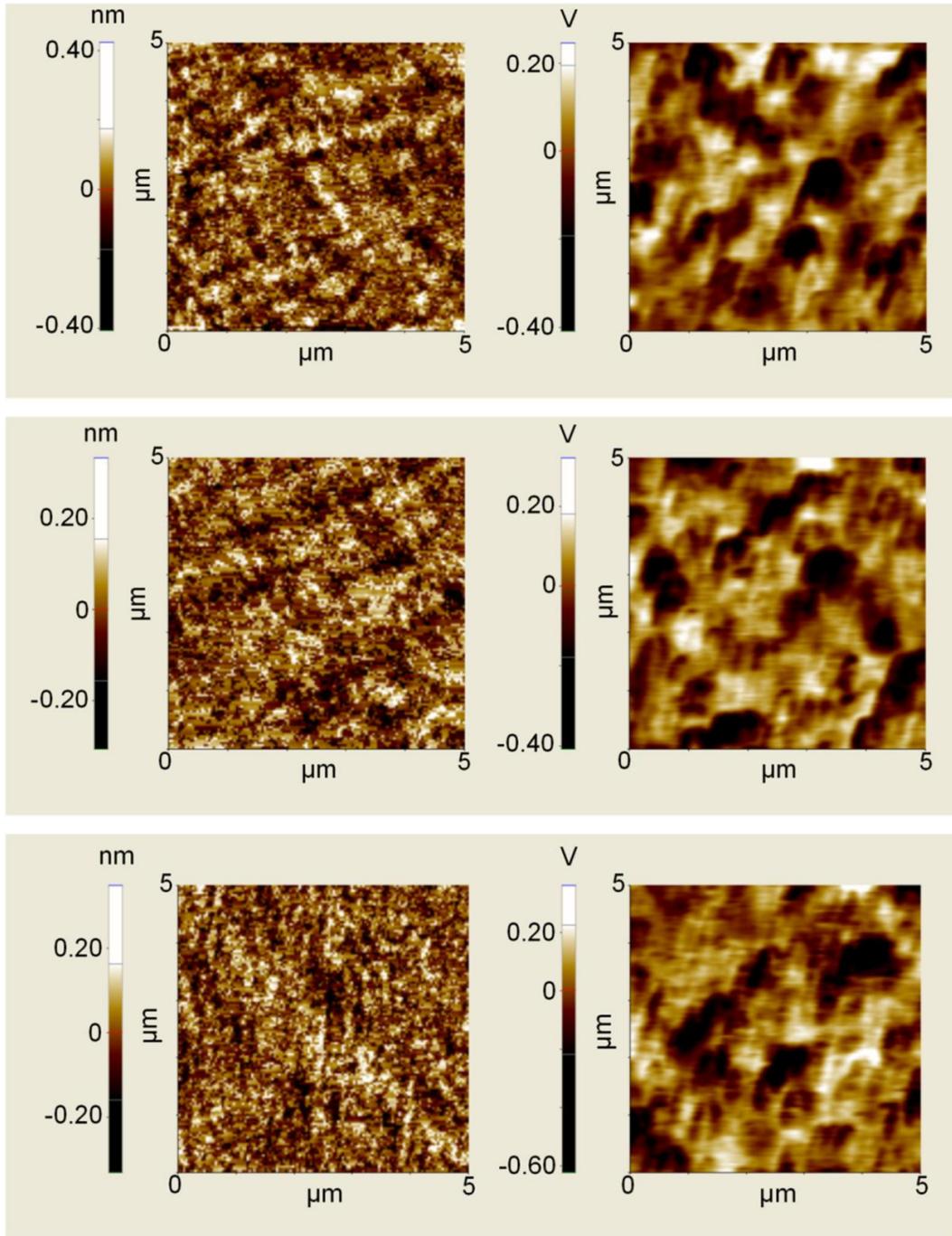
Figure 4.32 Simultaneously obtained topography (left) and capacitance (right) maps from SiO$_2$ on strained Si$_{0.35}$Ge$_{0.65}$. Parameters: V_{dc} = 0 V, V_{ac} = 2 V_{rms} and f_{ac} = 20 kHz.
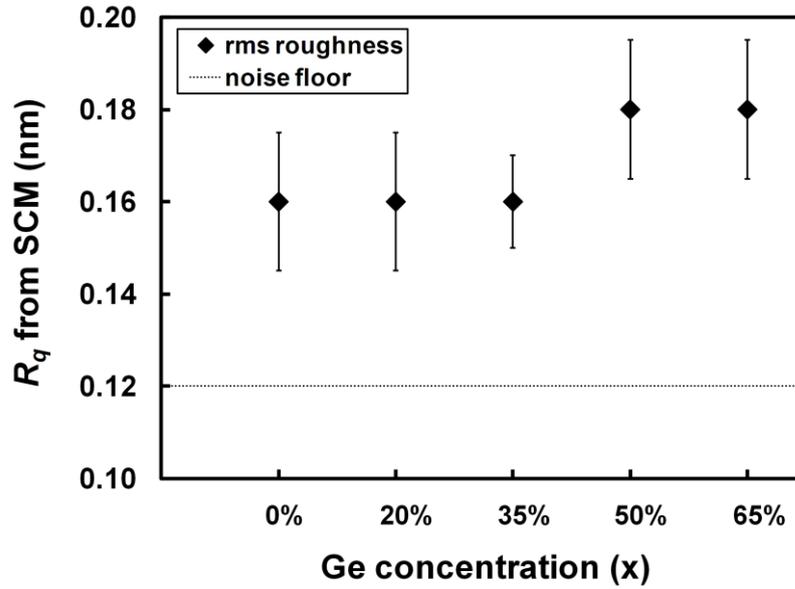
Figure 4.33 Variation in R_q with varying Ge obtained by the conductive PtIr5 coated SCM tips.

4.4.2 Extraction of D_{it} and V_{FB} at the nanoscale

Fig. 4.34 shows individual dC/dV sweeps with V_{tip}, obtained from 20 random locations across the surface of $SiO_2/Si_{1-x}Ge_x$ stacks with varying Ge concentrations. In order to clearly observe the differences in the dC/dV sweeps in Fig. 4.34, Fig. 4.35 shows one typical curve for each Ge concentration. The magnitude of dC/dV sweeps which is strongly affected by N_{sub} and t_{ox} (section 3.3.1) has been found to be comparable for all the samples (Fig. 4.34), thus ruling out any major variations in N_{sub} and t_{ox}. This is in agreement with the localised variations in t_{ox} studied by C-AFM (Fig. 4.27). The *FWHM* of dC/dV sweeps which is a direct qualitative measure of D_{it} (section 3.3.1) has been found to be different for samples with different Ge contents (Figs. 4.34 and 4.35).

The $V_{tip, peak}$ of dC/dV sweeps which is an indicator of V_{FB} (section 3.3.1) has also been found to vary with Ge (Figs. 4.34 and 4.35) indicating different levels of dielectric charges. It may also be seen in Fig. 4.34 that dC/dV sweeps indicate a uniform behaviour until the Ge concentration in the underlying strained alloy exceeds 50%. Beyond 50%, dC/dV sweeps exhibit a wide range of $V_{tip, peak}$. The sign of $V_{tip, peak}$ can be complicated while obtaining the dC/dV sweeps, especially for dielectrics with high levels of charge density [219]. Therefore, Fig. 4.34 suggests that the charge density in

the dielectric may be increased when Ge concentration in the SiGe alloy is increased from 50% to 65%. Alternatively, interfacial defects due to slight relaxation in the $Si_{0.35}Ge_{0.65}$ layer may also be responsible for the wide range of $V_{tip,\ peak}$ of dC/dV sweeps from the oxidised $Si_{0.35}Ge_{0.65}$ layer.
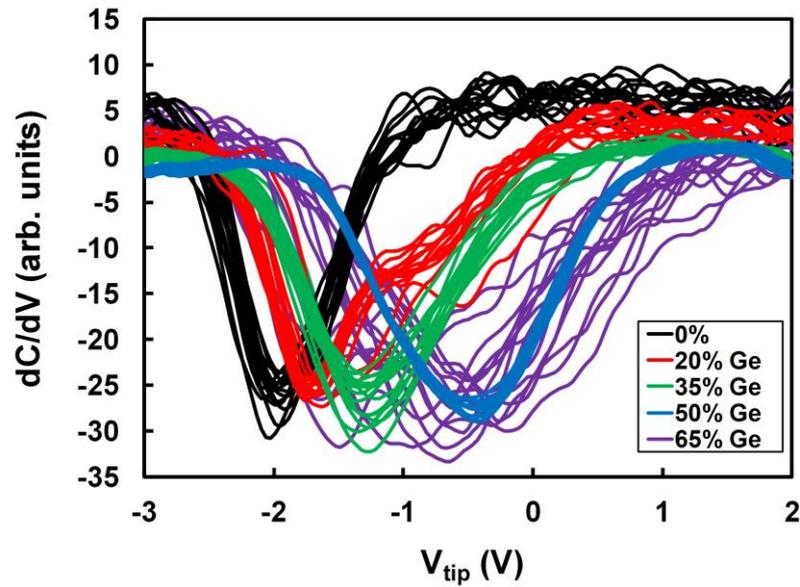
Figure 4.34 Individual *dC/dV* sweeps obtained from 20 random locations across the surface of SiO$_2$ dielectric on strained epitaxial Si$_{1-x}$Ge$_x$ layers with varying Ge concentration.
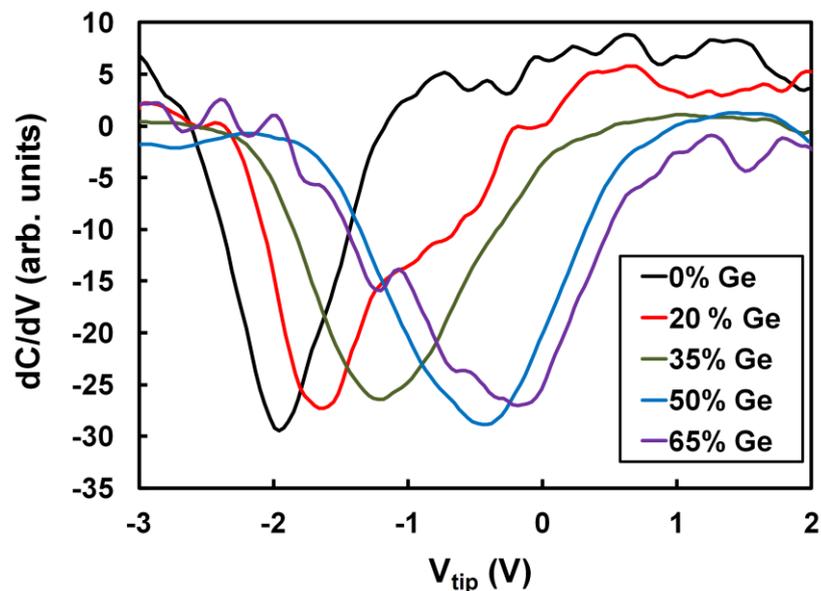
Figure 4.35 Typical *dC/dV* sweeps showing the impact of varying Ge concentration on the interface quality.

The variation in *FWHM* and $V_{tip, peak}$ of the *dC/dV* sweeps as observed for different samples in Fig. 4.34 is shown in Fig. 4.36. It can be seen that the *FWHM* of *dC/dV* sweeps (and hence D_{it}) increases as the amount of Ge in the strained $Si_{1-x}Ge_x$ alloy is increased. Ge-enhanced Si oxidation results in increased segregation of Ge at the interface which results in increased charge densities at the interface (section 4.1) thereby, explaining the trends shown in Fig. 4.36.
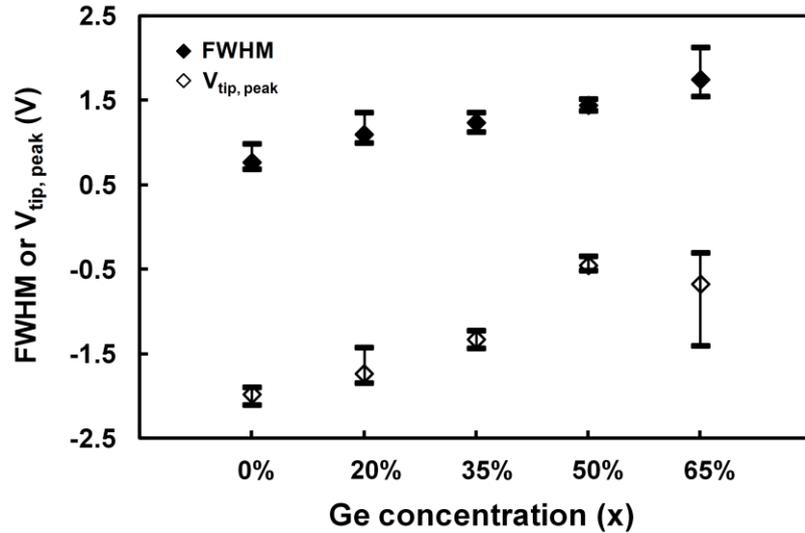
Figure 4.36 Variation in *FWHM* and $V_{tip, peak}$ of *dC/dV* sweeps shown in Fig. 4.34. Increase in *FWHM* (D_{it}) with Ge content can be observed.

The SCM analysis of strained Si devices (chapter 3) showed that the *FWHM* of SCM sweeps is increased by 0.84 V from 1.82 V (Si control) to 2.66 V (rough SRB strained Si) corresponding to an increase in D_{it} from 3 x 10^{11} (Si control) to 5 x 10^{11} cm^{-2}eV^{-1} (rough SRB strained Si). According to Wong *et al.*, an increase in D_{it} from 3.5 x 10^{14} to 6.5 x 10^{14} cm^{-2}eV^{-1} can increase the *FWHM* of SCM sweeps from 4 V to 6 V (an increase of 2 V) [260]. For the strained SiGe samples studied in this work, the increase in *FWHM* (Fig. 4.36) when the level of Ge is increased from 0% to 65% is ~ 1 V (from 0.77 V to 1.75 V). Comparison of *FWHM* in Fig. 4.36 with the values of *FWHM* and D_{it} in the preceding chapter and in [260] suggests that D_{it} for the samples studied in this work can be expected to be < 5 x 10^{11} cm^{-2}eV^{-1}. Moreover, the increase in D_{it} with Ge is not significant and is likely to be under an order of magnitude.

According to [107], a 10% increase in Ge content leads to a ~ 2% increase in the accumulated Ge at the interface which is sufficient to increase D_{it} by an order of magnitude. Hence, the small increase in *FWHM* (Fig. 4.36) with Ge supports the likelihood that the amount of Ge diffusion (due to low thermal budget) may not be significant. Chemical analysis (using techniques such as photoelectron spectroscopy or XPS) is required to confirm this.

The quality of the dielectric and its interface with the underlying strained SiGe layer has also been studied by analyzing $V_{tip,\ peak}$. $V_{FB,\ ideal}$ is equal to the metal and the semiconductor workfunction difference, φ_m-φ_s (equation 3.1). Increase in Ge content in strained $Si_{1-x}Ge_x$ layers reduces E_g which in turn reduces φ_s (equation 4.10). This in accordance with equation 3.1 results in increased $V_{FB,\ ideal}$ with increasing Ge content for strained $Si_{1-x}Ge_x$ layers (Table 4.4).

In the non-ideal case (i.e. in the presence of dielectric charges), V_{FB} can be written as [97],

$$V_{FB} = V_{FBi} - \left(\frac{Q_f}{C_{ox}} + \frac{Q_{it}}{C_{ox}}\right), \qquad \textbf{4.11}$$

where Q_f and Q_{it} are the fixed (bulk) and interface trapped charge densities in the dielectric, respectively.

Equation 4.11 indicates that in the presence of net positive charges in the dielectric, V_{FB} should be less than $V_{FB,\ ideal}$ and vice versa. Fig. 4.36 has shown that V_{FB} is negative for all the samples. This indicates presence of net positive charges in the dielectric since $V_{FB,\ ideal}$ has been calculated to be positive for all the samples (Table 4.4). It can also be seen in Fig. 4.36 that $V_{tip,\ peak}$ increases (becomes more positive) until the concentration of Ge in the SiGe layer reaches 50%. For the highest Ge concentration of 65% studied, $V_{tip,\ peak}$ reduces and becomes more negative. This may be due to the presence of dielectric charges of both polarities and an increase in the net charge density when Ge is increased from 50% to 65%. This is also supported by the widely scattered *dC/dV* sweeps in Fig. 4.34 when Ge level is increased from 50% to 65%.

Using the values of $V_{FB,\ ideal}$ as given in Table 4.4 and using $V_{tip,\ peak}$ as a measure of V_{FB}, the magnitude of $V_{FB,\ shift}$ has been calculated and is shown in Fig. 4.37 with Ge concentration. It has been found that the magnitude of $V_{FB,\ shift}$ reduces up to a Ge concentration of 50% and increases when the amount of Ge is increased to 65%. This is

because experimental $|V_{FB}|$ reduces with Ge while the theoretical $|V_{FB, ideal}|$ increases with Ge. When the Ge concentration is increased from 50% to 65% $|V_{FB}|$ increases which increases $|V_{FB, shift}|$. Fig. 4.36 shows that D_{it} increases with Ge while Fig. 4.37 shows that $|V_{FB, shift}|$ due to dielectric charges reduces until the level of Ge exceeds 50%. Since V_{FB} depends not only on interface charges (like D_{it}) but also on bulk charges and workfunction differences, Fig. 4.37 suggests that dielectric charges of both polarities may be present in the samples studied.
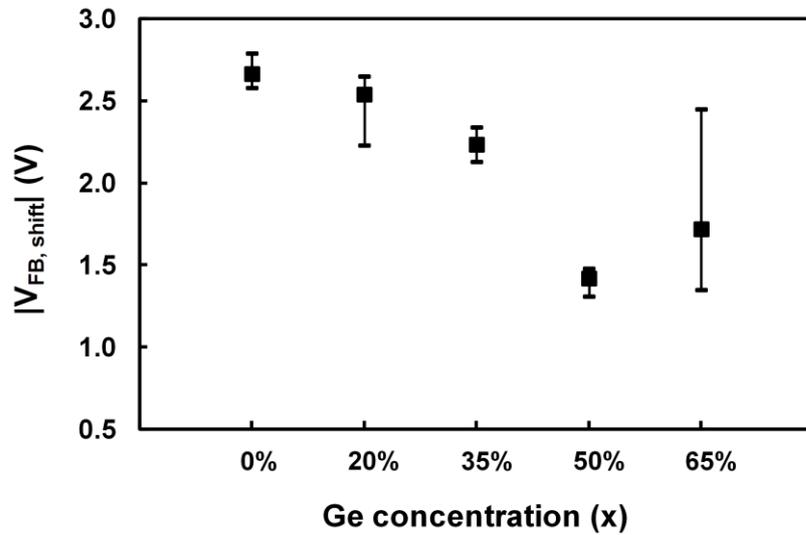
Figure 4.37 $|V_{FB, shift}|$ **for PtIr5/SiO$_2$/Si$_{1-x}$Ge$_x$ MOS capacitors with varying Ge content obtained by subtracting $V_{FB, ideal}$ in Table 4.4 from $V_{tip, peak}$ of dC/dV sweeps in Fig. 4.36.**

4.4.3 Sensitivity of SCM for identifying other dielectric related defects

Fig. 4.38 shows the dC/dV sweeps from the oxidised Si$_{0.80}$Ge$_{0.20}$ layer. A feature which has been regularly observed is that the dC/dV sweeps from the oxidised Si$_{0.80}$Ge$_{0.20}$ layer do not exhibit the expected U-shape throughout. A distortion in the dC/dV sweeps at $V_{tip} \sim -1$ V has been consistently observed (Fig. 4.38). Interface traps associated with metallic contamination induced defects are expected to cause such distortion in the dC/dV sweeps [261, 262]. The reliability of semiconductor devices is strongly affected by metal contamination [263, 264]. Metallic contaminants can induce interfacial defects, such as metal precipitates and oxidation induced stacking faults during processing [265, 266]. Material characterisation prior to oxidation did not

identify any difference in terms of defects. It is likely that there was an oxidation anomaly. Iron (Fe) which is a commonly observed donor-type impurity in Si wafers can diffuse into Si during thermal oxidation, resulting in Fe-related defects such as Fe_i and Fe-B pairs [261, 267]. Both Fe_i and Fe-B are strong recombination centres and can cause minority carriers in the region to respond to the ac modulation during SCM analysis [261, 268].
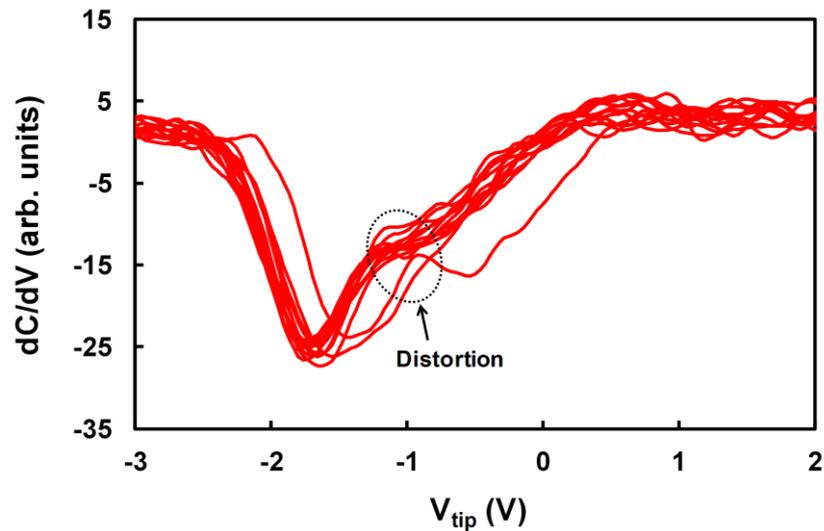
Figure 4.38 *dC/dV* sweeps from the oxidised Si$_{0.80}$Ge$_{0.20}$ layers showing distortion at V_{tip} ~ -1 V.

Presence of defects induced distortion (Fig. 4.38) is an indicator of high sensitivity of the SCM measurement setup to other dielectric related defects. However, such distortion has only been observed for a low Ge concentration (20%). Further chemical characterisation using techniques such as XRD, EDX and XPS is required to identify any differences in the interface quality and composition for the sample under consideration.

4.4.4 Comparison of nanoscale D_{it} and V_{FB} with macroscopic data

Nanoscale SCM analysis has shown that D_{it} increases with Ge content in the strained SiGe layer (section 4.4.2). Effect of Ge content on D_{it} has been extensively studied before [243-245, 253, 269-277]. Fig. 4.39 compares the nanoscale D_{it} trends shown in this chapter with some of the previously reported macroscopic D_{it} data. It can be

observed that the trends in D_{it} (increase with Ge) obtained at nanoscale are similar to previously reported device level behaviour. Such good correlation validates the SCM measurement setup and analysis for analysing dielectric performance on strained SiGe layers.
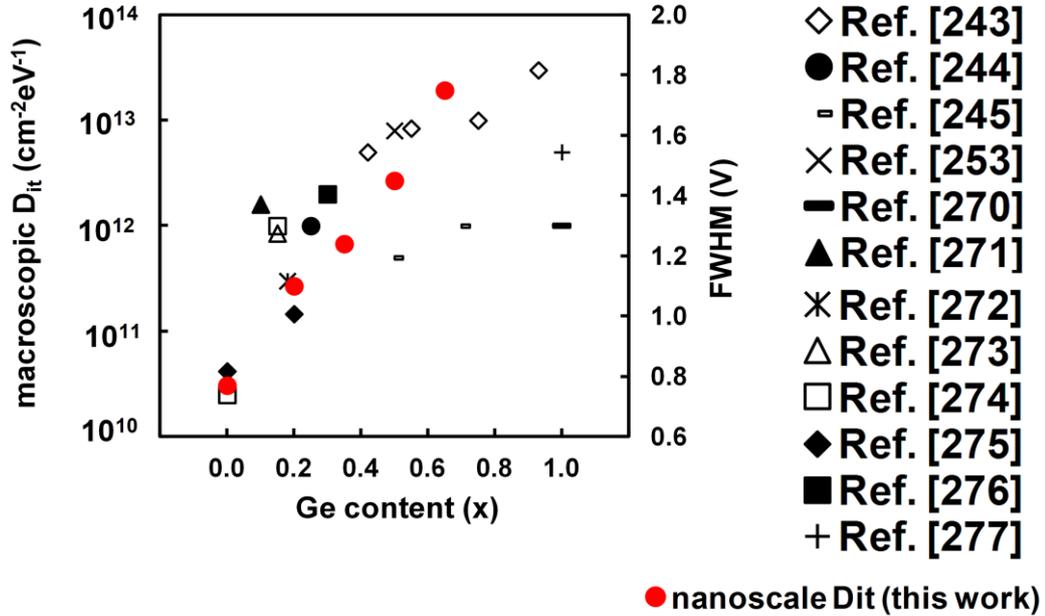
Figure 4.39 Comparison of nanoscale D_{it} trends (from SCM) with previously reported device level behaviour [243-245, 253, 270-277].

The level of D_{it} for the samples studied in this work is expected to be less than 5 x 10^{11} cm^{-2}eV^{-1} (section 4.4.2). This is either lower than or comparable with previously reported macroscopic data (Fig. 4.39). This further confirms 65% of Ge as an optimum concentration for strained SiGe devices.

Fig. 4.40 compares previously reported macroscopic values of V_{FB} [278-280] with the values of nanoscale V_{FB} ($V_{tip, peak}$) (Fig. 4.36). The values for macroscale V_{FB} shown in Fig. 4.40 have been corrected for the respective workfunction differences with a PtIr5 coated tip. Although the trend of increase in V_{FB} with Ge agrees at macro and nanoscale, the exact values of V_{FB} exhibit opposite polarity. This shows that negative charges in the dielectrics on strained SiGe layers have been generally reported. For the samples studied in this work, net positive dielectric charges have been observed. This may not be an issue as charges of both polarities can be present in the dielectric. Similar differences in polarity of macroscale V_{FB} with $V_{tip, peak}$ from SCM have been reported

before [219]. Further SCM analysis on other materials and interface systems may be able to answer this contradiction.
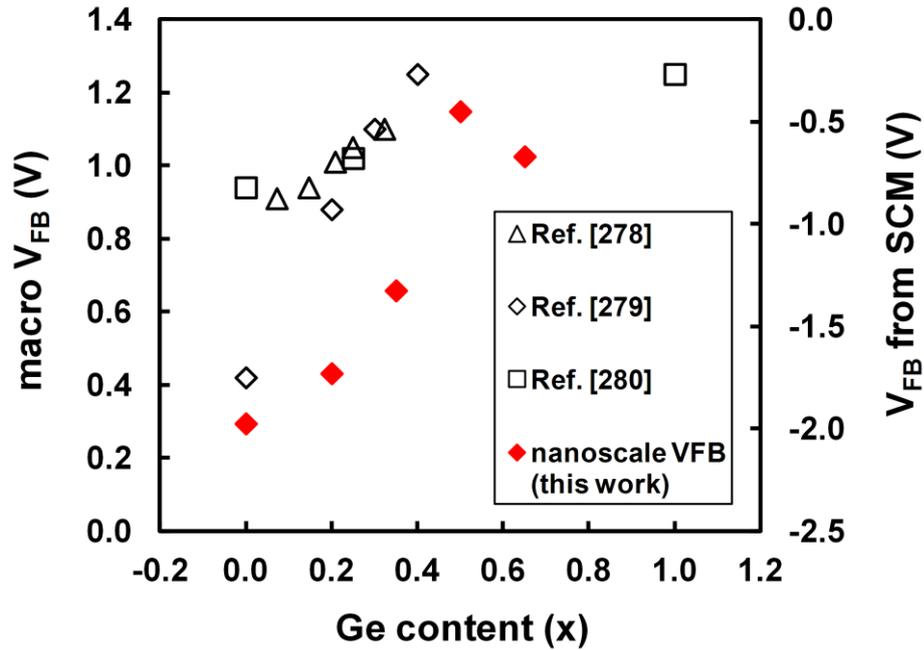
Figure 4.40 Comparison of nanoscale V_{FB} ($V_{tip, peak}$) with previously reported macroscopic values [278-280].

4.4.5 Interface quality at contrasting regions in SCM images

It has been shown in section 3.3.6 that bright regions in the SCM maps of SiO_2 on rough SRB strained Si channels exhibit high *FWHM* indicating enhanced D_{it} at troughs and along the steep slopes of crosshatch undulations. In order to identify similar trends for D_{it} in compressively strained SiGe devices, *dC/dV* sweeps from contrasting regions of the SCM maps were obtained. In total, 20 *dC/dV* sweeps including 10 each from bright and dark areas in the SCM maps of each sample were recorded. These sweeps and the variation in *FWHM* and $V_{tip, peak}$ exhibited by them are shown in Fig. 4.41. The *FWHM* and $V_{tip, peak}$ from bright and dark regions have been found to be nearly similar and have failed to indicate any definite trend. This may be due to the fact that the levels of D_{it} in these samples may be low and uniformly distributed (since surface roughness in these samples has been found to be considerably lower than the tensile strained Si samples studied in the preceding chapters).
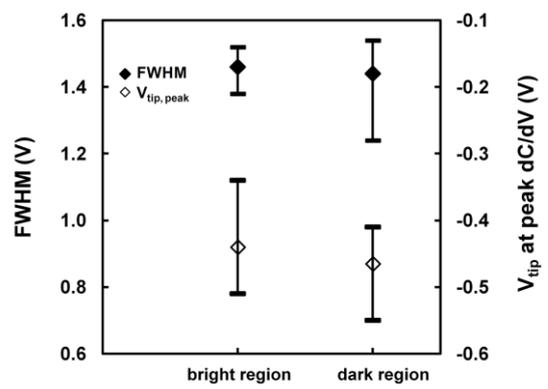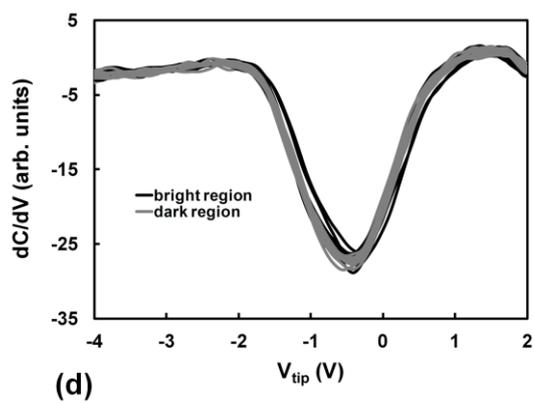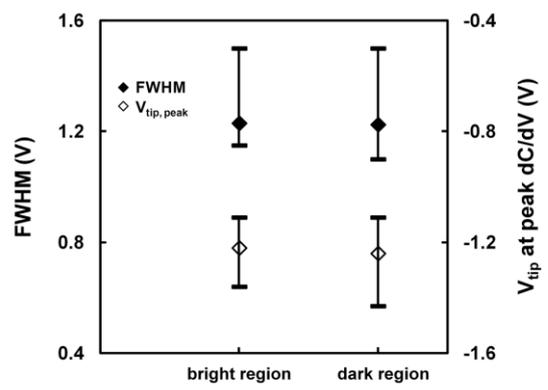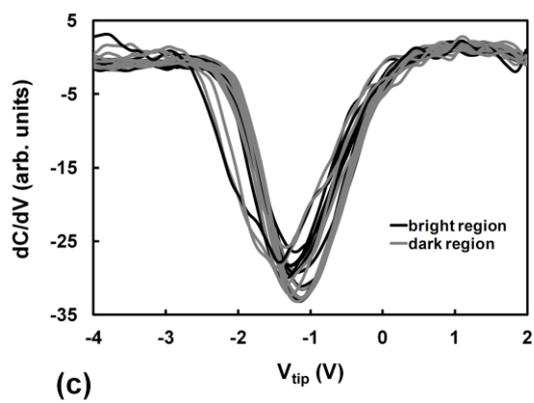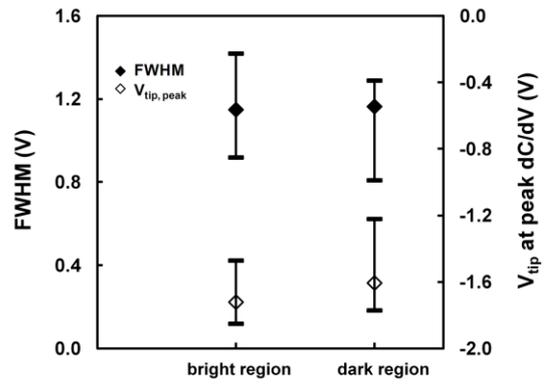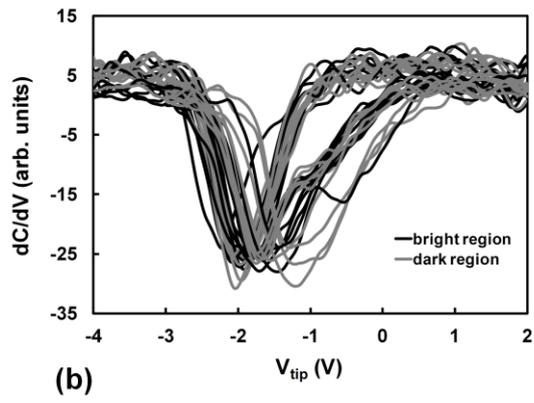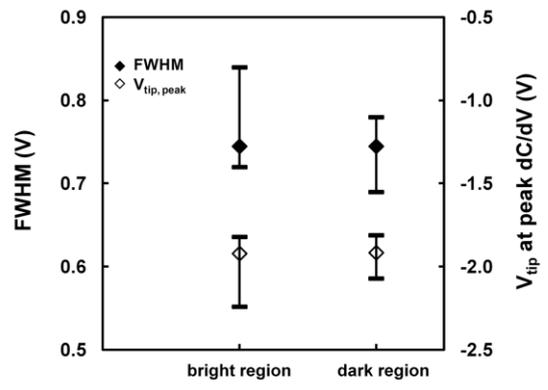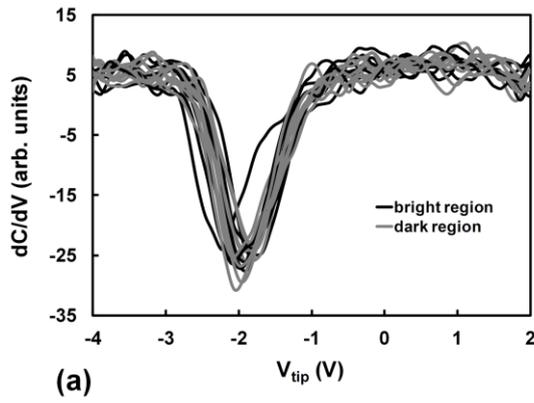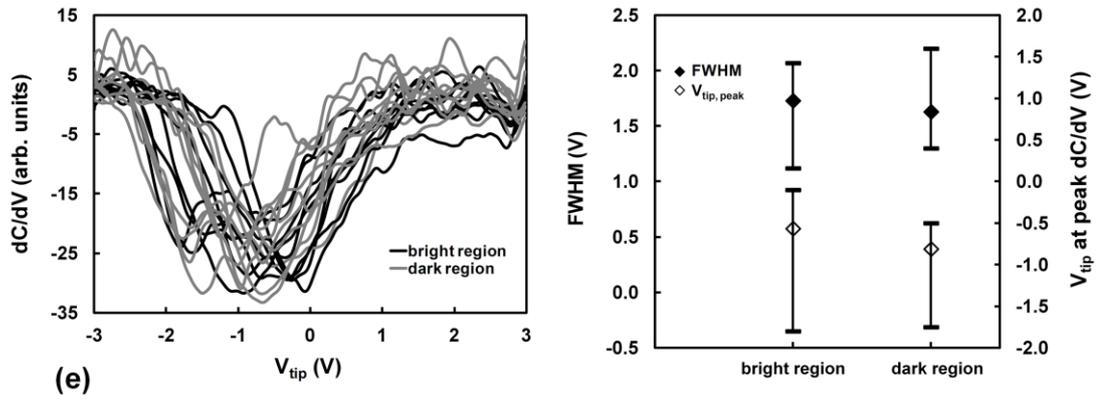
Figure 4.41 Individual *dC/dV* sweeps (left) and variation in *FWHM* and $V_{tip, peak}$ (right) obtained from the bright and dark regions of the SCM maps for $SiO_2/Si_{1-x}Ge_x$ stacks with (a) x = 0, (b) x = 0.20, (c) x = 0.35, (d) x = 0.50, and (e) x = 0.65.

No difference in *dC/dV* sweeps from contrasting regions in the SCM maps was observed (Fig. 4.41). This poses a question on the impact of the finite tip geometry. Consequently, the sensitivity of the current SCM setup requires further understanding.

In the absence of any differences in D_{it} from bright and dark regions (Fig. 4.41), the contrasting regions in the SCM maps (Figs. 4.28-4.32) can be largely attributed to small scale features in the surface morphology. In addition, collective influence of minor variations in N_{sub}, t_{ox}, Q_f, and Q_{it} may also have contributed under ac modulation during SCM scanning.

4.5 Summary

Nanoscale analysis of leakage, localised breakdown, dielectric thickness and dielectric/semiconductor interface quality of thin oxides on compressively strained $Si_{1-x}Ge_x$ layers with varying Ge levels has been carried out.

Surface morphology and roughness has not been found to vary significantly with Ge for the samples studied. This is in contrast with most of the previous reports which show that roughness increases with the amount of Ge in the strained SiGe alloy. Small scale undulations on the surface of Si capped and oxidised $Si_{0.35}Ge_{0.65}$ layers were observed. Slight increase in small scale roughness was observed when high resolution AFM images were filtered using MATLAB. According to some previous reports, minor

variations in roughness can also influence gate dielectric performance. No undulations or differences in surface roughness were observed when electrical AFM tips with conductive coatings were used. This is expected to be due to the large contact areas and contact mode imaging.

It is shown that uniform distribution of leakage spots is observed if morphological instabilities such as ripples and undulations often associated with epitaxially grown strained SiGe layers can be avoided. Gate leakage at nanoscale has been quantified and has been found to increase with Ge concentration. It has been shown that samples with higher Ge content (50% and 65%) reach the current limit of the measurement setup before lower concentrations. This implies that dielectrics on Ge-rich strained SiGe layers are expected to break earlier than Si-rich layers. Electron affinity comparable with bulk-Si and higher transverse effective mass are expected to be the primary reasons for enhanced leakage with Ge. Additionally, Ge out-diffusion and valence band offsets are also expected to play a secondary role in enhancing leakage at higher Ge concentrations. Nanoscale variations in J_g are in agreement with theory and previously reported device level data. The level of nanoscale J_g is comparable with previously reported macroscopic values of J_g for strained SiGe channel devices. This implies that 65% of Ge in the strained SiGe channel is an optimum concentration for enhancing mobility and maintaining acceptable levels of gate leakage. Localised variations (< 2 Å) in t_{ox} show that variation in Ge content does not influence t_{ox}.

Nanoscale SCM measurements show that D_{it} increases with increase in Ge content in the strained SiGe layer. Such nanoscale D_{it} behaviour is similar to previously reported macroscopic trends. Comparison of *FWHM* in this work with *FWHM* and D_{it} in a previous report and the preceding chapter suggest that D_{it} in the samples studied is less than 5×10^{11} cm^{-2}eV^{-1}. Also, the increase in D_{it} with Ge is likely to be under an order of magnitude. Such levels of D_{it} are either comparable with or lower than previously reported macroscopic D_{it} in strained SiGe channel devices. The small increase in *FWHM* (and hence D_{it}) with varying Ge also supports the likelihood that Ge diffusion due to low thermal budget may not be significant. SCM analysis of nanoscale D_{it} has further shown that 65% Ge is an optimum concentration for realising high carrier mobility strained SiGe devices.

Variation in V_{FB} and its shift from its ideal value with varying Ge has also been studied. It has been observed that $|V_{FB, shift}|$ reduces until the Ge concentration exceeds 50%. This reduction may be explained by the fact that V_{FB} depends on both bulk and

interface charges and metal-semiconductor workfunction difference. Presence of charges of both polarities may have resulted in $|V_{FB, shift}|$ reducing till Ge content exceeds 50%. An increase in $|V_{FB, shift}|$ is observed when Ge content is increased from 50% to 65%. This may be due to the increased net charge density. Which is also supported by the widely scattered *dC/dV* sweeps when Ge level is increased from 50% to 65%.

SCM setup does appear to detect defects and trap-sites. However, no difference in *dC/dV* sweeps from contrasting regions in the SCM maps was observed. This poses a question on the impact of the finite tip geometry. While a sharper tip will enhance the topographic resolution it may not be able to easily locate trap sites as the contact area is considerably reduced. This issue gains further importance when devices which exhibit low levels of D_{it} are analysed by sharp tips. Large number of measurements preferably using more than one probe tip may be obtained in such a scenario. Hence, sensitivity of the current SCM measurement setup is required to be studied in greater detail. SCM analysis of standard SiO_2/Si stacks with a wide spread in D_{it} can help in understanding the lower limit of D_{it} which can be studied by SCM.

Although performance of SiO_2 has been studied in this work, the measurement techniques and the results discussed here have implications for high-κ dielectrics. This is because high-κ dielectrics generally undergo low thermal budget (similar to the samples studied in this chapter) which reduces Ge out-diffusion and hence the issue of segregation is controlled.

The attractive electrical performance of dielectrics on epitaxial SiGe layers shown in this chapter is a step towards realizing high performance strained Ge channel devices (which exhibit high levels of hole mobility) with acceptable leakage and interfacial quality.

Chapter 5. Further work and applications

The applicability of electrical SPM techniques has been demonstrated for strained Si/SiGe in the preceding chapters. This chapter discusses the current work and further applications which can use electrical SPM analysis developed in this thesis. The first section discusses the interfacial analysis in thin anti-reflective coatings on glass windows. The second section describes the applicability of electrical SPM techniques to nanoscale tubular structures. This is followed by a brief description of the SCM analysis of standard SiO_2/Si samples to allow a better understanding of its sensitivity.

5.1 Thin anti-reflective coatings on glass windows

5.1.1 Background

A technologically important requirement from architectural windows is to achieve improved thermal and optical properties whilst maintaining aesthetic appearance. Proper design and choice of glass windows affect the energy usage of a building. In view of the need to manage energy, there is a widespread interest for materials which improve the performance of glazed windows [281, 282]. An energy efficient window is capable of harnessing natural visible light and avoiding heat transfer between the interiors and the outside environment, thereby reducing the energy load. Thin anti-reflective coatings (which are transparent in the visible region and opaque for infra-red wavelengths) transmit light and block heat transfer. This results in energy efficient glass windows which are beneficial for buildings which involve large amounts of glass, e.g. skyscrapers.

Multi-layer coated systems such as solar control coatings consisting of a metal layer (e.g. silver, Ag) sandwiched between dielectrics (e.g. tin oxide, SnO_2 and zinc oxide, ZnO) or wide bandgap semiconductors (e.g. zinc sulphide, ZnS) act as anti-reflection layers used for realising energy efficient windows [282-286]. The choice of materials is governed by geography and climate. The thickness of materials in the stack also affects the performance and is varied according to the intended application [286].

5.1.1.1 Failure of anti-reflective coatings

The quality of the interfaces between coatings or a coating and its substrate play an important role as failure at these interfaces can cause the anti-reflective coatings to fail [287]. The requirement is to have a strong adhesion between the coating and its substrate under normal operating conditions [288]. Delamination of coatings while in contact has been identified as an adhesive failure of multi-stack solar control coatings [287]. Adhesive failure of coatings on glass is effectively a fracture process occurring at or near the coating/substrate interface. This includes local optical failure such as a visible scratch. Many interfacial failures are caused by contact induced stresses, for e.g., transit scratches which occur during delivery [287]. Such transit scratches cause adhesion failure in multi-layer coatings during normal operation. For thin hard coatings, failure may be due to interfacial fractures during handling or cleaning [285]. The interfacial defects are effectively small voids (which may be aggregates of vacancies) or low density of chemical bonding across the interface. There are defects called disclinations which are effectively planes of low atomic density. The failure mode is like a crack, bonds are broken to extend the crack and then they reform in a different place so there is relative motion between the two halves of the crystal. Interfacial defects are about 1 micron apart. Failure can also mean loss of anti-reflection behaviour in a large area, however, this generally occurs at the end of life rather than during delivery.

Irrespective of the reasons for failure (handling, delivery or normal operation), nanoscale interfacial characterisation is desirable.

5.1.1.2 Characterisation of failure in anti-reflective coatings

The interfacial toughness in solar control coatings has been extensively studied before using different methods [287, 289-292]. Most of these methods deliberately induce cracks at the interface. The propagation of such cracks is then studied as a measure of interfacial quality. However, these methods are not very reliable when coating layers are very thin [288]. Alternative methods such as nanoindentation, strained over-layer and scratch tests have been developed to study thin coatings on glass substrates [287, 289, 292]. However, these techniques suffer from issues like successfully inducing failure and quantifying stress state in the vicinity of failed regions [288]. Through the analysis in this chapter, a non-destructive electrical analysis of

interfacial defects and cracks is presented. SCM is capable of studying interfaces between thin films or a thin film and its substrate as demonstrated in the preceding chapters. Consequently, SCM measurement setup and analysis developed in the preceding chapters is used to analyse interfacial failure in multi-layer solar control coatings on glass substrates.

5.1.2 Coatings investigated and sample preparation

5.1.2.1 Multi-layer coatings on glass substrate

The coatings studied here are the main components of solar control coatings including SnO_2, Ag, ZnO, TiO_xN_y (titanium oxynitride) and glass. The coated systems are multilayer stacks consisting of very thin layers deposited with the same architecture and deposition conditions as in a commercial solar control coating. The multi-layer stack is shown in Fig. 5.1. The most important layer in such coatings is a 10 nm thick active layer of Ag surrounded by anti-reflection coatings (40 or 200 nm of SnO_2, 10 nm of ZnO) and 5 nm of TiO_xN_y barrier layers. The thin layer of zirconium, Zr (5 nm) allows deposition of SnO_2 on Ag. The coatings were produced on a full scale experimental glass coating line at the Pilkington Technology Centre (Lathom, UK) using an identical recipe as in the commercial solar control coatings.
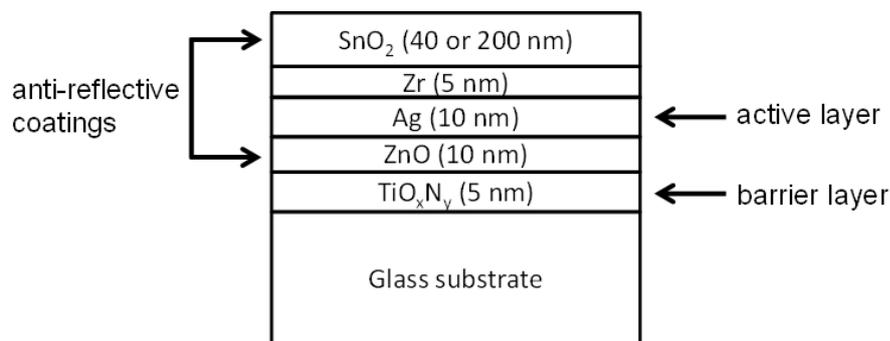
Figure 5.1 Schematic of the multi-layer stack studied in this work.

5.1.2.2 Sample preparation

The interface between the active layer of Ag and SnO_2 has been studied. Analysis of the other interface between Ag and ZnO (another anti-reflective material) was not possible due to impractical sample preparation for SCM measurements. This interface has recently been studied through finite element modelling [287].

Since Ag was buried below SnO_2 and a thin layer of Zr (which was required to deposit SnO_2 on Ag). The coatings of SnO_2 and Zr were damaged using flat metal and then conductive silver paint was used to make a contact between the active layer and the AFM metal disc. This preparation was required to allow application of dc and ac bias to the active layer through the substrate. Fig. 5.2 shows the sample prepared for measurement under the AFM. The PtIr5 coated SCM tip, SnO_2 and Ag layer formed a metal-insulator-metal (MIM) capacitor.
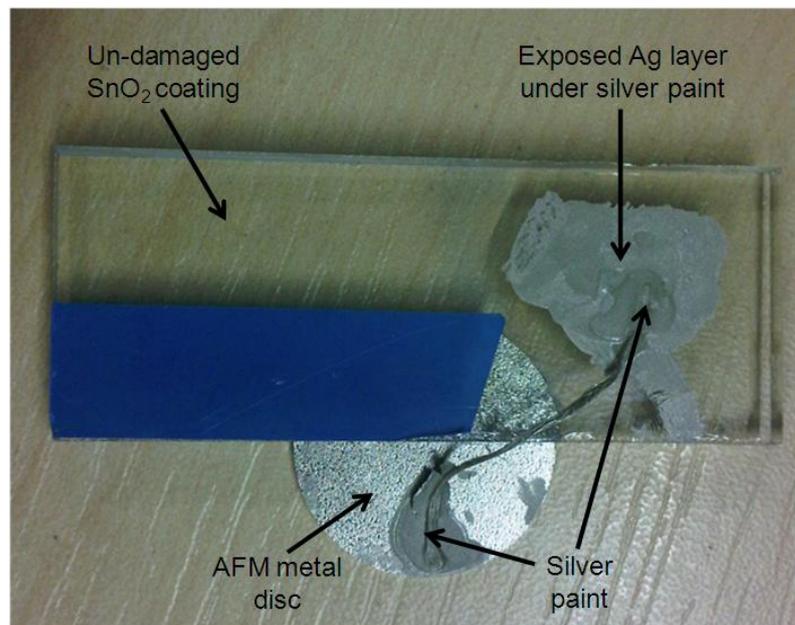
Figure 5.2 Prepared sample for SCM measurement.

5.1.3 Nanoscale electrical analysis

5.1.3.1 Measurement conditions

Two samples with different SnO_2 thickness (40 nm and 200 nm) were studied. SCM images were obtained at $V_{dc} = 0$ V, $V_{ac} = 3$ V_{rms} and $f_{ac} = 20$ kHz. Identical measurement settings on the lock-in amplifier were used for both the samples. The value for V_{ac} is higher than the ones used for analysing strained Si and SiGe materials in chapters 3 and 4 respectively. This is because a MIM capacitor is expected to have a capacitance response which does not vary significantly with applied voltage. This means that the slope of capacitance, ΔC (parameter measured in SCM) is expected to be very small. Hence in order to enhance the contrast in the SCM image due to minor capacitive variations (which otherwise may go undetected), V_{ac} was increased to a high value of 3 V_{rms} [216].

5.1.3.2 SCM imaging of the SnO$_2$/Ag interface

Figs. 5.3 and 5.4 show 5 x 5 μm^2 topography (left) and SCM (right) images obtained from the surfaces of 40 nm and 200 thick SnO_2 coatings, respectively. No particular features in the SCM images were observed for either of the samples. Figs. 5.3 and 5.4 also show that the magnitude of the SCM signal is higher for a thinner dielectric and vice versa. This is in agreement with the inverse linear relationship between capacitance and dielectric thickness. The reduction in the SCM signal magnitude is ~ 4 times (from $\pm$ 0.8 V to $\pm$ 0.2 V) for a 5 fold increase (from 40 nm to 200 nm) in thickness. This indicates that the SCM setup is responding to differences in the thickness of SnO_2 layer which suggests that the SCM setup is not only capable of studying MOS systems but can also be applied to other materials and interfaces such as MIM capacitors. Uniform level of SCM signal (with no particularly contrasting features) in Figs. 5.3 and 5.4 indicates a capacitor with low level of non-linearity in its capacitive behaviour and a uniform thickness of the dielectric.

Lack of definite features in the SCM images in Figs. 5.3 and 5.4 suggest that the interface between SnO_2 and Ag may not be the reason for the failure in solar control coatings. Recently on the basis of finite element modelling analysis it has been suggested that cracks may develop during handling and transit due to the failure at the

Ag/ZnO interface in a ZnO-Ag-ZnO solar coatings stack [287]. Hence the SCM analysis (Figs. 5.3 and 5.4) supports the results presented in [287].
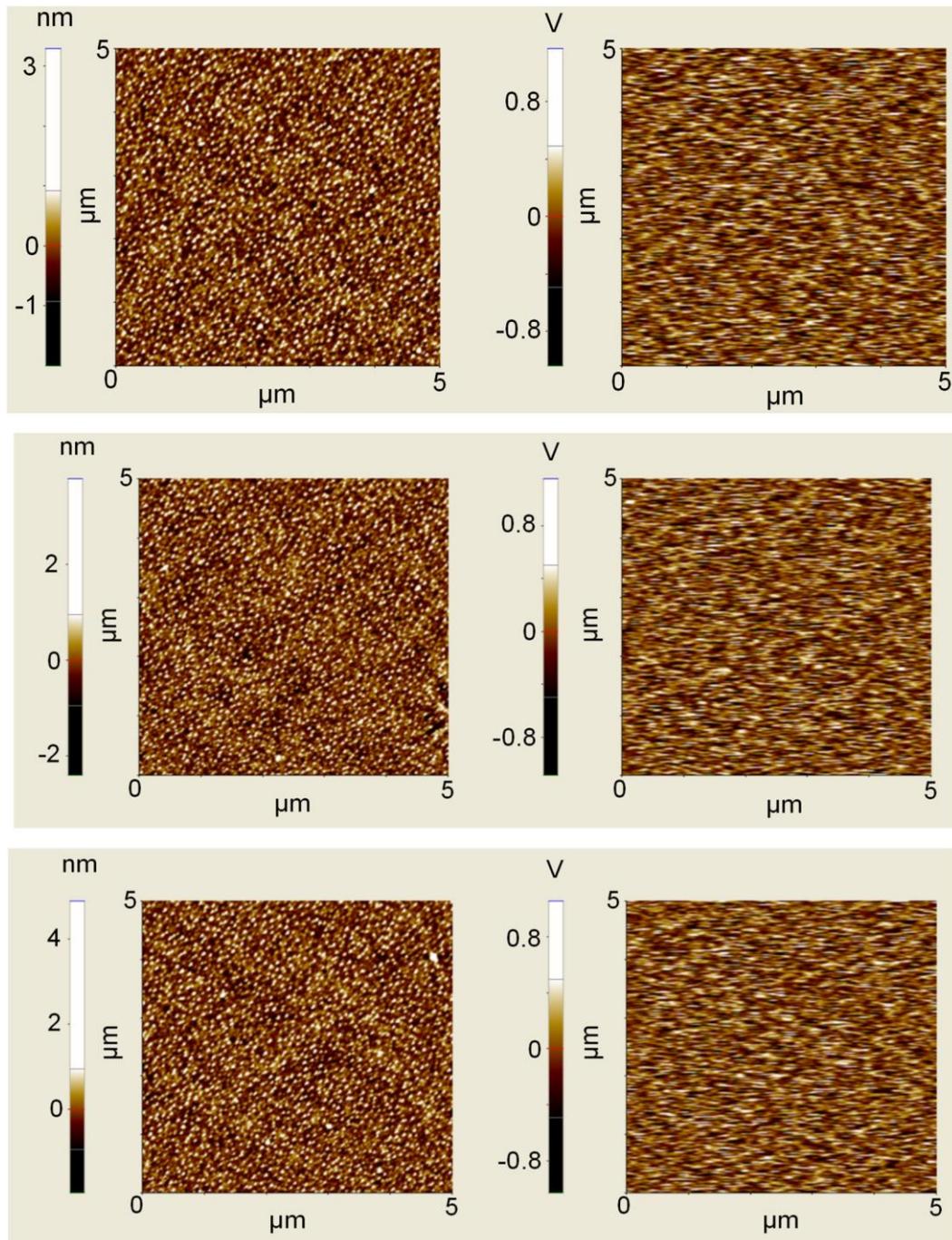
Figure 5.3 Topography (left) and SCM (right) images from the surface of 40 nm SnO$_2$ coated on a thin active layer of Ag.
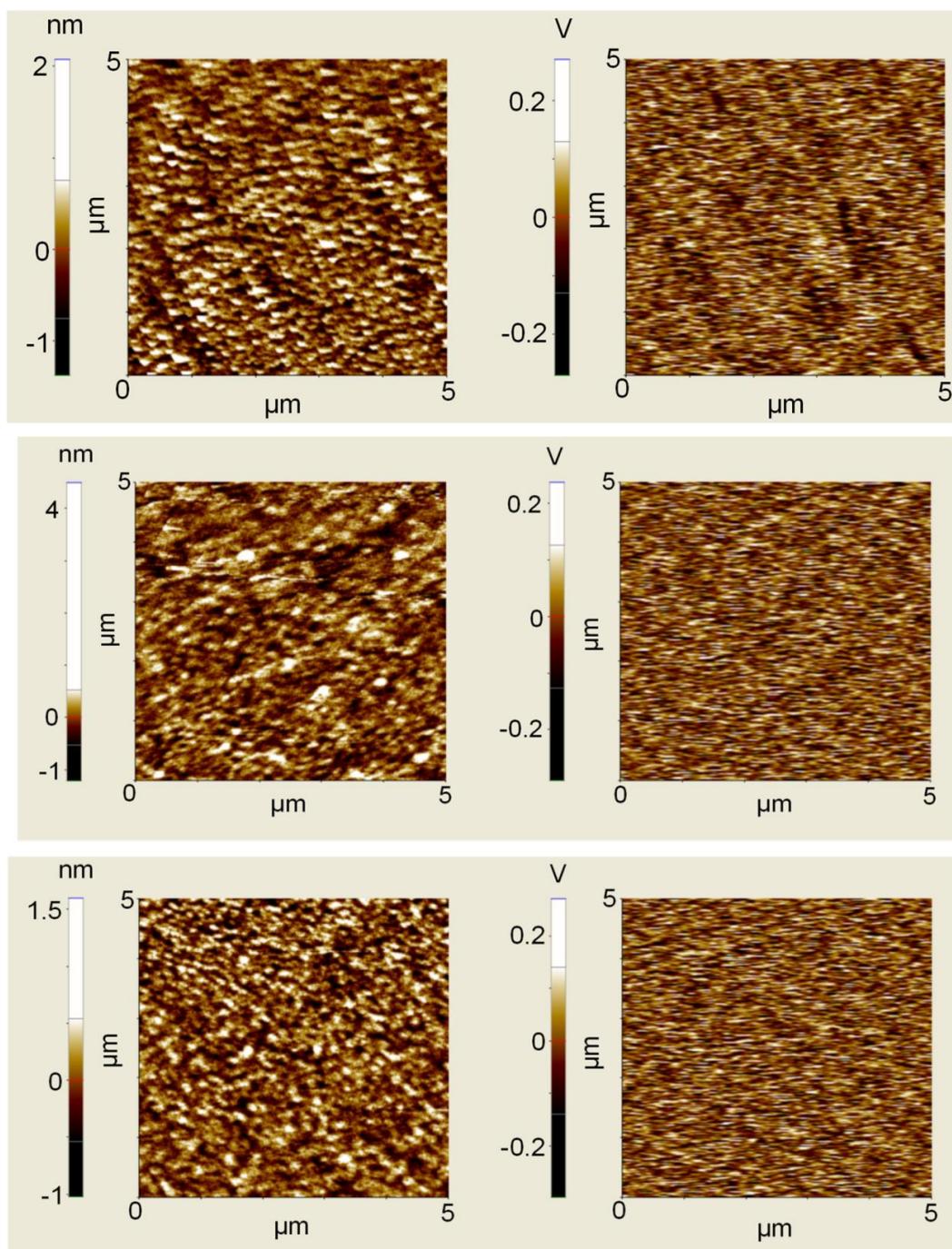
Figure 5.4 Topography (left) and SCM (right) images from the surface of 200 nm SnO₂ coated on a thin active layer of Ag.

It is possible that defects and trap sites at the SnO_2/Ag interface are located farther apart than 5 μm (scan size of Figs. 5.3 and 5.4) and may have gone undetected while the scans of Figs. 5.3 and 5.4 were recorded. Therefore, larger (10 x 10 μm^2) scans were obtained which are shown in Figs. 5.5 (SnO_2 thickness = 40 nm) and 5.6 (SnO_2 thickness = 200 nm). SCM images of Figs. 5.5 and 5.6 exhibit similar behaviour as smaller areas (Figs. 5.3 and 5.4). This suggests that the dielectric thickness is uniform over a large area and the interface between the anti-reflective SnO_2 and active layer of Ag may not be responsible for the failure of SnO_2/Ag/ZnO solar control coatings.
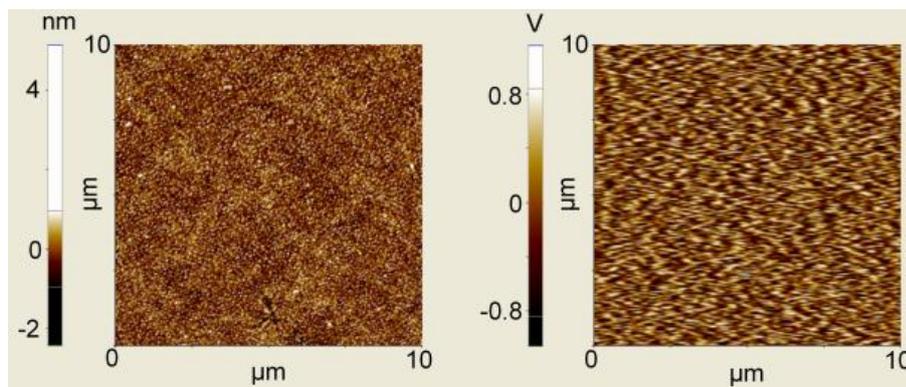
Figure 5.5 Topography (left) and SCM (right) scan from the surface of 40 nm SnO_2 coated on a thin active layer of Ag. Scan size: 10 x 10 μm^2.
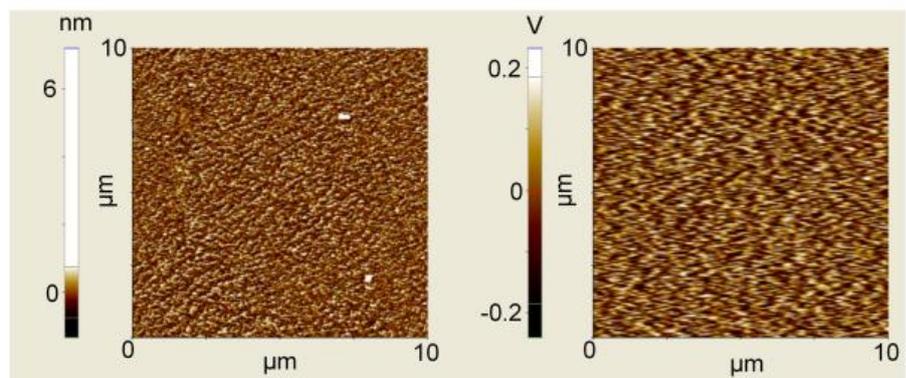
Figure 5.6 Topography (left) and SCM (right) scan from the surface of 200 nm SnO_2 coated on a thin active layer of Ag. Scan size: 10 x 10 μm^2.

5.1.3.3 Localised analysis using spectroscopic dC/dV sweeps

In the absence of any capacitive variations due to large scale interfacial defects (Figs. 5.3-5.6), *dC/dV* sweeps were obtained from 20 random locations using the SCM in spectroscopic mode. Figs. 5.7 and 5.8 show individual *dC/dV* sweeps obtained from SnO_2/Ag stacks with different SnO_2 thickness (40 nm and 200 nm). The sweeps in Figs. 5.7 and 5.8 exhibit near constant levels of *dC/dV* magnitude with V_{tip}. This indicates that the capacitance response of MIM capacitors is largely constant as no influence of defects or trapped charges is observed. Fig. 5.9 shows a comparison of a typical *dC/dV* sweep for both the samples. The *dC/dV* magnitude is reduced for thicker dielectrics compared with those with lower thickness. The reduction in the level of *dC/dV* signal is nearly 5 times for a similar increase in thickness. This confirms the sensitivity of the SCM measurement setup to MIM capacitors in accordance with the inverse relationship between capacitance and dielectric thickness.

MIM capacitors with thin high-κ dielectrics exhibit nearly constant capacitance response with applied voltage and this linearity increases with dielectric thickness [293-295]. SnO_2 has a lower dielectric constant (κ ~ 10) compared with commonly used high-κ dielectrics, such as HfO_2 (κ ~ 25), ZrO_2 (κ ~ 25), TiO_2 (κ ~ 80) and $SrTiO_3$ (κ ~ 2000). Also, the typical oxide thickness in solar control coatings (few tens of nm) is considerably higher compared with commonly observed dielectric thickness (< 10 nm) in high-κ MIM capacitors such as HfO_2 and ZrO_2. Therefore, a MIM capacitor with a relatively thick SnO_2 is expected to exhibit nearly constant capacitance (since capacitance is directly proportional to κ and inversely proportional to t_{ox}) over the whole range of measurement. Consequently, the slope (*dC/dV*) of such a capacitance curve will be close to zero and nearly constant as observed in Figs. 5.7-5.9.
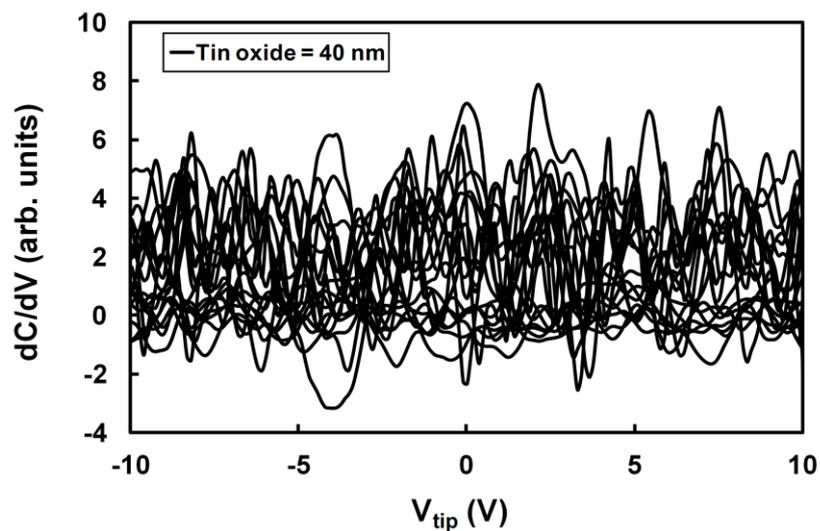
Figure 5.7 Individual *dC/dV* sweeps obtained from the surface of a 40 nm thick SnO₂ coating on a thin active layer of Ag.
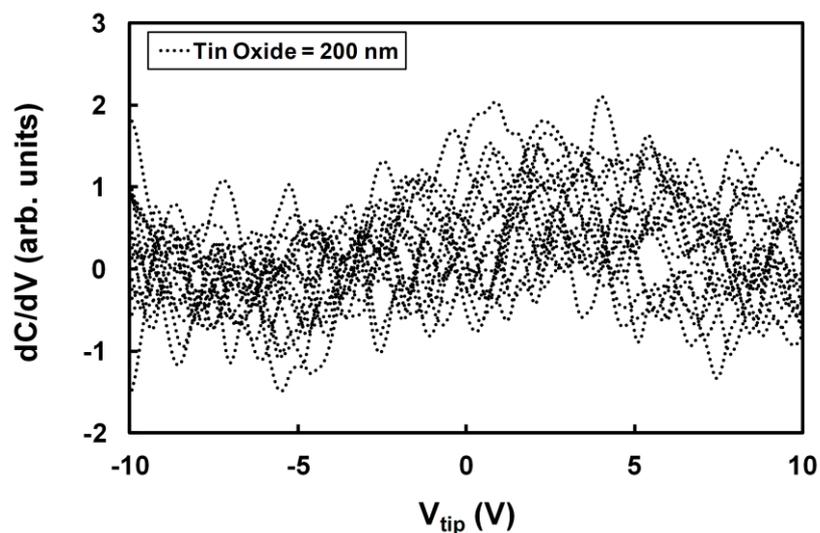
Figure 5.8 Individual *dC/dV* sweeps obtained from the surface of a 200 nm thick SnO₂ coating on a thin active layer of Ag.
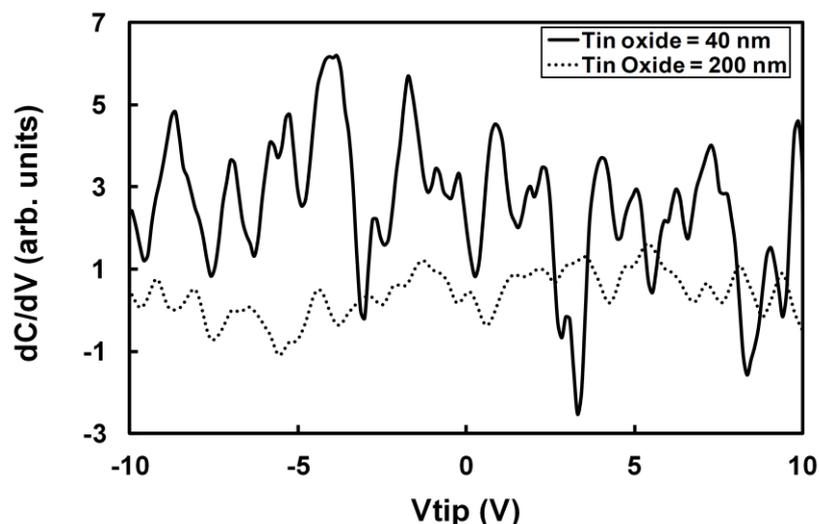
Figure 5.9 Typical *dC/dV* sweeps obtained from the surface of SnO₂ coatings of different thickness on a thin active layer of Ag.

5.1.4 Summary

The SCM measurement setup described in the preceding chapters has been applied to industrial standard solar control coating system. The SCM metal tip, oxide coating and the active (Ag) layer formed a MIM capacitor which responded accurately to variations in oxide (SnO_2) thickness. The data suggests that the interface between the anti-reflective coating of SnO_2 and the active Ag layer may not be responsible for the failure of solar control coatings. These observations based on SCM analysis support the recently reported finite element modelling study which states that the Ag/ZnO interface is more likely to fail during contact. The SnO_2/Ag interface may fail over time during normal operation. However, this requires further analysis of solar control coatings which have been in active use for varying lengths of time. The work demonstrates that the SCM can be applied to thin anti-reflective coatings which may require nm scale analysis.

5.2 Synthetic chrysotile nanotubes

Novel materials with nanoscale dimensions have simulated new scientific and technological breakthroughs in the field of solid-state electronics. Hollow cylindrical nanotubes have gained significant ground due to their attractive electrical and optical properties. Such nanotubes can be exploited to suit various semiconducting and superconducting applications.

Synthetic chrysotile (white asbestos) is non-toxic and possesses asbestos fibre properties, such as heat resistance, non-combustibility, high tensile strength and resistance to selective chemical attack [296, 297]. Asbestos tubes are highly insulating and can confine different materials in its hollow core. These attractive properties make synthetic chrysotile nanotubes excellent candidates to prepare innovative inorganic nanowires. Such nanowires can be realised by filling the inner hollow core with metal, non-metal, semiconductor and organic materials depending on the intended application. Fig. 5.10 shows a TEM image of a single tubular chrysotile nanocrystal [296, 297].

Although, compositional analysis and potential applications of chrysotile nanotubes is well documented, electrical performance of these is rarely reported. Ivanova *et al.* reported resistance-temperature variation in chrysotile nanotubes filled with molten Hg, Bi, and InSb in 1995 [298]. Since then there is a lack of electrical analysis of chrysotile nanotubes.

200 nm

Figure 5.10 TEM image of a single tubular chrysotile nanocrystal [296, 297].

Owing to the typical dimensions of individual nanotubes, nanoscale imaging techniques are expected to play a pivotal role in their characterisation. Spacing between individual nanocrystals enclosed in the nanotubes has till now been studied using

transmission electron microscopy (TEM) which is a complex, expensive and destructive technique. It is highly desirable to provide a comparatively easier and a non-destructive characterisation method.

Electrical SPM techniques such as C-AFM and SCM may be used to spatially locate the enclosed crystals on the basis of their localised electrical signatures.

A frequent challenge associated with imaging nanostructures with AFM is sample preparation. In order to measure such nanoparticles with AFM there are 3 major requirements:

1. Strong adhesive contact between the particles and the substrate.

2. Substrate should be flatter than the typical height of the particles.

3. Particles should be well dispersed on the substrate.

For electrical AFM imaging another requirement of a conductive contact arises. This is because electrical bias is typically applied through the substrate. AFM imaging of chrysotile nanotubes has been carried out by drying them on mica which is an insulator. This is not suitable for electrical analysis. Therefore, a small piece of clean Si wafer may be used on which nanotubes can be studied. Si substrate will be smooth as well as conductive and hence may be able to satisfy the above requirements.

For best results, it is necessary to locate individual nanotubes for electrical characterisation. Fig. 5.11 shows an AFM image of synthetic chrysotile nanotubes which were dropped from a liquid suspension and dried on mica surface [296, 297, 299]. Only few individual nanotubes in the middle of large lumps of nanotubes can be observed. Consequently, locating a single nanotube is a major challenge before electrical SPM techniques can be applied to such nanotubular structures.
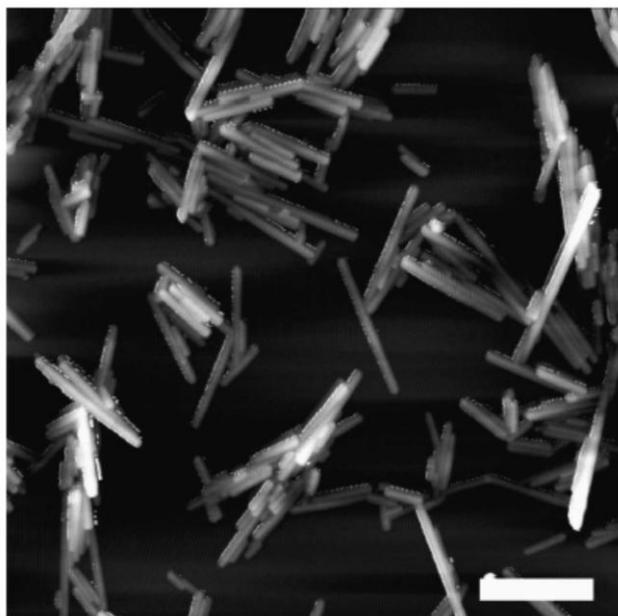
Figure 5.11 AFM image of synthetic chrysotile nanotubes [296, 297, 299]; scale bar = 500 nm.

5.3 Sensitivity of SCM for thin dielectrics

5.3.1 Identification of other dielectric related defects

Fig. 4.38 in section 4.4.3 showed that the *dC/dV* sweeps from the $SiO_2/Si_{0.80}Ge_{0.20}$ stacks exhibited distortion at $V_{tip} \sim$ -1 V. This is expected to be due to interface defects caused by metal contaminants which diffuse during oxidation. Material characterisation prior to oxidation did not identify any difference in terms of defects. Further chemical characterisation of oxidised samples is required to fully understand the SCM sweeps of Fig. 4.38.

Material characterisation techniques such as XRD, EDX and XPS can be applied to study the interface quality and chemical composition for the oxidised sample under consideration.

Differences in chemical composition for 20% Ge compared with other Ge concentrations (if verified) would validate the sensitivity of the SCM setup for other dielectric related defects.

5.3.2 Analysis of standard SiO$_2$/Si stacks

SCM analysis has suggested that the SCM setup is responding to defects and trap sites. This is because correlation between macroscopic and nanoscale trends has been established for two sets of materials namely, strained Si (chapter 3) and strained SiGe (chapter 4). However, sensitivity of the SCM setup requires further thought and experimentation. Sharp AFM tips enhance the topographic resolution but also reduce the effective contact area which reduces the probability of locating degraded areas along the interface. This issue gains further importance when uniformly distributed defects and trap sites with sharp tips are analysed.

In order to identify the lower limit of SCM with different tip geometries and charge distributions, standard samples with varying D_{it} can be studied. SiO$_2$/Si is regarded as the most stable interface in the semiconductor industry. Si is atomically smooth and its interface with its natural oxide generally exhibits low levels of roughness and hence D_{it} (under 10^{10} cm^{-2}ev^{-1}). The material and electrical effects of new semiconductors and dielectrics will be avoided if SiO$_2$/Si interface is analysed. Consequently, SiO$_2$/Si stacks with varying levels of D_{it} (preferably spread over 4-5 orders of magnitude) may be studied with SCM to understand its limits. The *FWHM* values obtained during the SCM analysis of such standard samples can then be compared with macroscopically measured D_{it} on the same wafers after metallisation. This should provide more significance and reliability to the values of *FWHM* generally obtained with SCM.

In order to obtain samples with a wide range of D_{it}, deliberate alterations in processing have been implemented to obtain samples with varying surface roughness (since R_q directly affects D_{it}). The alterations in processing were based on an initial set of experiments. Bare Si wafers were subjected to different etchants to study the influence on surface roughness. One set of wafer was subjected to Caro etch (H$_2$SO$_4$:H$_2$O$_2$, 6:1 at 140 °C for 15 minutes) and mild HF (5%) clean while another set of wafer was subjected to Caro etch, RCA clean (NH$_4$OH:H$_2$O$_2$:H$_2$O, 1:1:5 at 75 °C for 10 minutes) and mild HF. Fig. 5.12 shows the effect of different cleaning procedures on the Si surface.

On the basis of the results in Fig. 5.12, different processing conditions have been implemented. These are shown in Table 5.1 along with the resulting surface roughness. In total, 18 bulk-Si wafers have been processed. All the wafers were subjected to a pre-clean using TMH (tri-methyl-oxy-ethyl-ammonium-hydroxide) in a megasonic bath.

Thirteen wafers were subjected to two different concentrations of RCA clean while five wafers were not subjected to any RCA clean (Table 5.1). Three wafers were not oxidised to understand the influence of RCA cleaning and oxidation on surface roughness. One wafer (no. 11) was treated with HF (10%) for 6 minutes while another wafer (no. 12) was treated with 40% NH$_4$F for 6 minutes (Table 5.1).
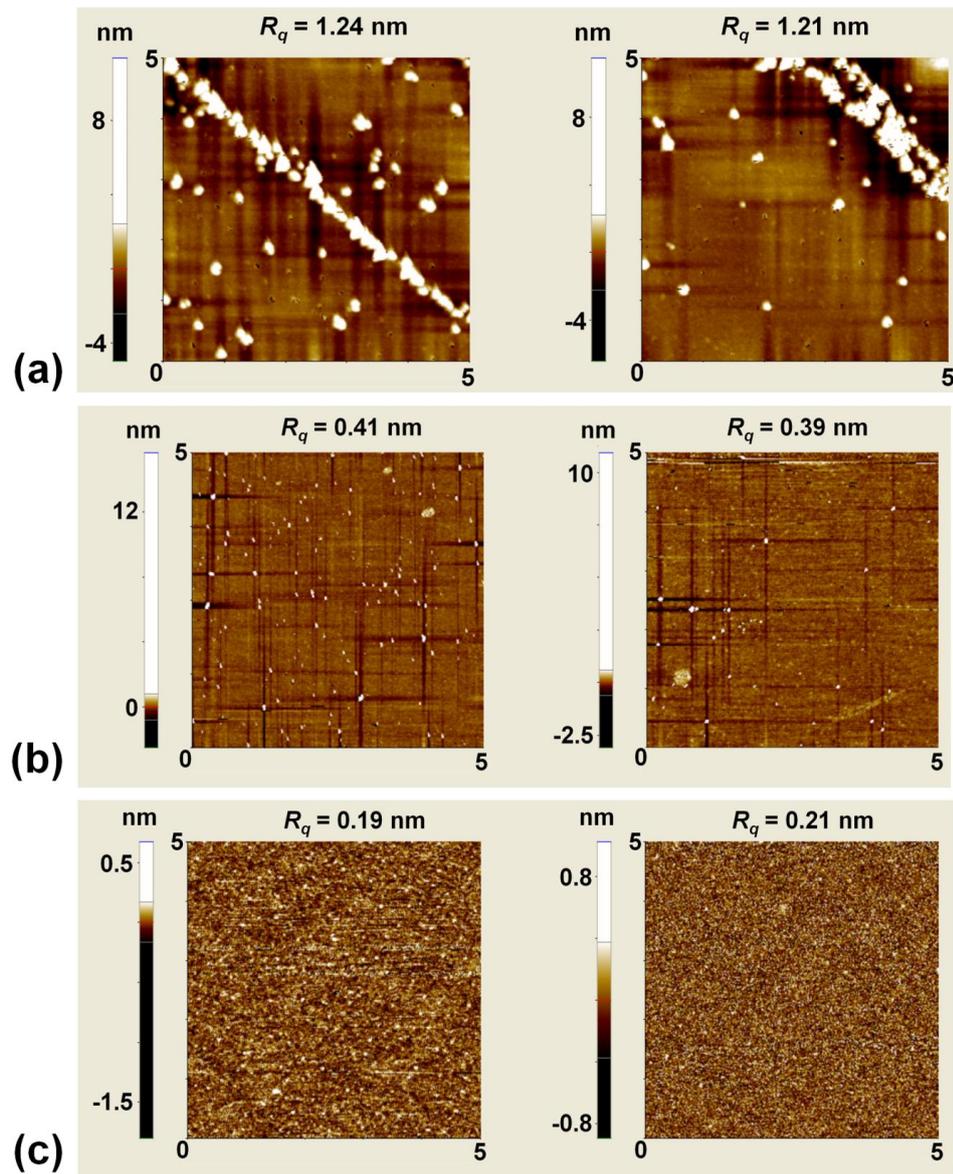
Figure 5.12 Variation in surface roughness, (a) before cleaning, (b) after Caro etch and HF, and (c) after Caro etch, RCA and HF.

Table 5.1 Different processing steps for obtaining bulk-Si wafers with varying surface roughness and hence D_{it}. Processing and metallisation was carried out at Fraunhofer Institute for Integrated Systems and Device Technology (IISB), Erlangen, Germany.

Wafer number	RCA clean ($NH_4OH:H_2O_2:H_2O$)	HF (10%, 6 min.)	NH_4F (40%, 6 min.)	Post oxidation FGA temperature (°C)	rms surface roughness R_q (nm)
1	1:1:5				0.14
2	1:1:5			430	0.20
3	1:1:5			200	0.18
4	1:1:5			700	0.18
5	1:1:5			not oxidised	0.24
6	3:1:5				0.20
7	3:1:5			430	0.19
8	3:1:5			200	0.18
9	3:1:5			700	0.12
10	3:1:5				<u>0.08</u>
11	3:1:5	✓			<u>0.07</u>
12	3:1:5		✓		<u>0.40</u>
13	3:1:5			not oxidised	0.21
14					0.21
15				430	0.18
16				200	0.18
17				700	<u>0.45</u>
18				not oxidised	0.18

Following this, 15 wafers were subjected to dry oxidation with an intended oxide thickness of 3 nm. Oxide thickness was estimated using ellipsometry and was found to be 2.96 ± 0.14 nm. For every RCA clean and no RCA clean, three different post oxidation FGA temperatures were implemented while six samples did not undergo FGA after oxidation.

Following this, wafers were bisected and one set of each wafer was metallised by physical vapour deposition resulting in a metal contact of 20 nm of titanium followed by 300 nm of aluminium. Another set of each wafer has been set aside for AFM/SCM analysis.

Fig. 5.13 shows 500 x 500 nm^2 AFM scans from wafers which exhibited lowest and highest surface roughness. Lowest surface roughness was observed from wafer number 10 (0.08 nm) and 11 (0.07 nm) which were subjected to the strongest RCA concentration ($NH_4OH:H_2O_2:H_2O$ = 3:1:5). Wafer number 11 was also subjected to HF treatment (Table 5.1). High surface roughness was observed from wafer number 12 (0.40 nm) which was subjected to the strongest RCA clean and NH_4F treatment. Wafer number 17 which did not undergo any RCA clean and was subjected to the highest FGA temperature (700 °C) exhibited highest surface roughness (0.45 nm) as shown in Table 5.1 and Fig. 5.13. Samples which were subjected to a relatively mild RCA clean ($NH_4OH:H_2O_2:H_2O$ = 1:1:5) did not exhibit any significant difference in surface roughness with the post oxidation FGA temperature (Table 5.1).

Fig. 5.14 shows one typical C-V curve from each oxidised wafer obtained after metallisation. Differences in the C-V response suggest differences in V_{FB} and D_{it}. Macroscopic D_{it} measurements of metallised wafers and SCM analysis of the wafers which did not undergo metallisation are required to be obtained. Subsequent comparison of the macroscopic D_{it} and *FWHM* of nanoscale dC/dV sweeps from the same set of wafers is expected to provide better understanding about the sensitivity of the current SCM measurement setup.

Fig. 5.15 compares the C-V curves from metallised wafers with minimum and maximum surface roughness. Relative differences in parallel shift and stretch-out of the C-V curves (Figs. 5.14 and 5.15) indicate differences in D_{it} and V_{FB}.
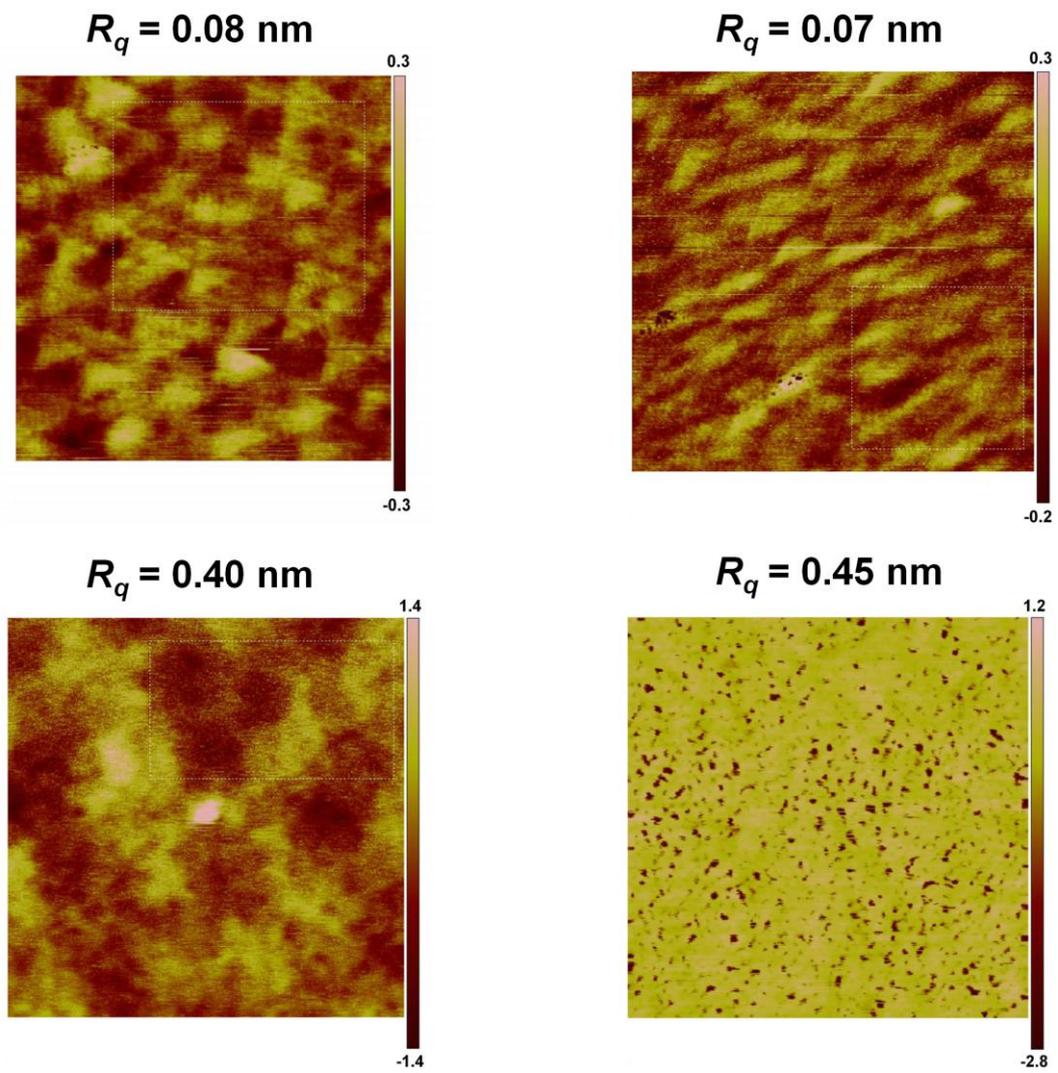
Figure 5.13 500 × 500 nm^2 AFM images for wafers with lowest and highest surface roughness. AFM imaging carried out at Fraunhofer IISB, Erlangen, Germany.
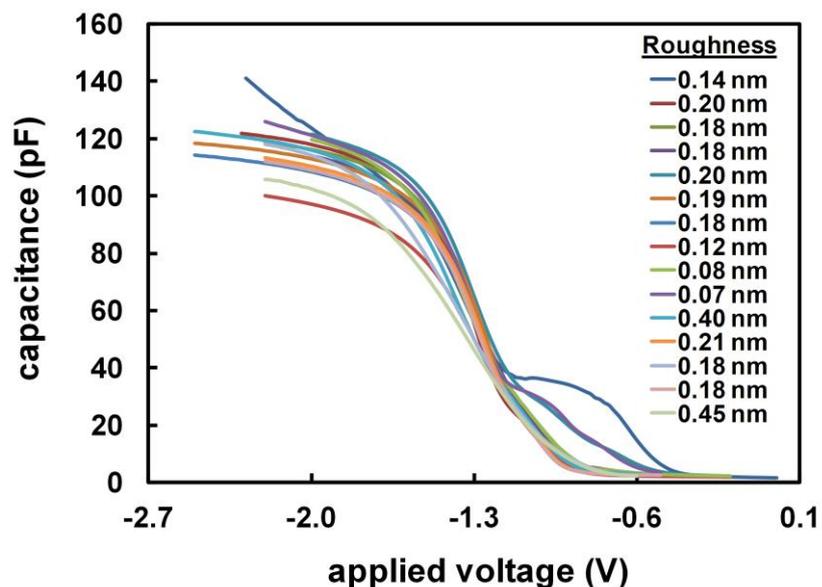
Figure 5.14 *C-V* curves obtained from differently processed oxidised Si wafers post metallisation. Differences in *C-V* response with varying surface roughness can be observed. *C-V* measurements obtained at Fraunhofer IISB, Erlangen, Germany.
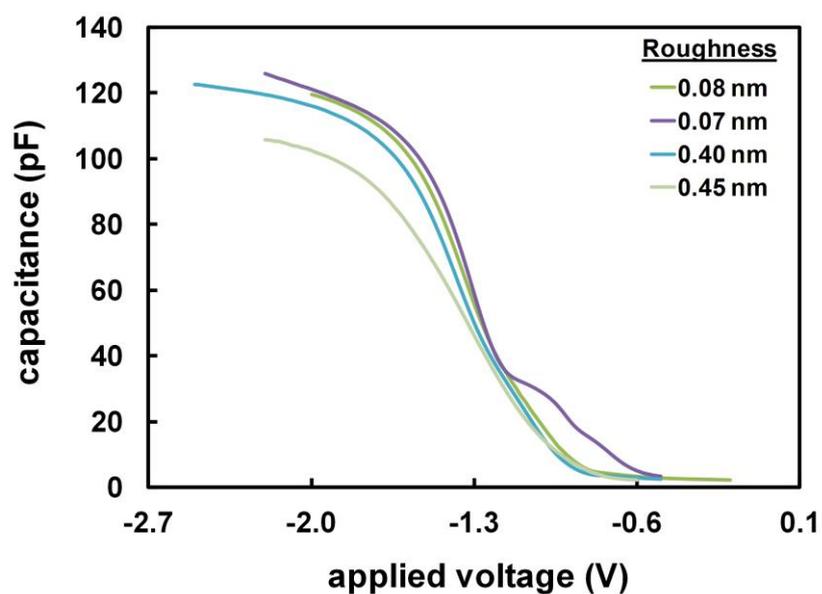
Figure 5.15 Comparison of *C-V* curves for wafers with minimum and maximum surface roughness. Differences in parallel shift and stretch-out suggest differences in D_{it} and V_{FB}. *C-V* measurements obtained at Fraunhofer IISB, Erlangen, Germany.

Such SCM analysis of standard SiO_2/Si samples may also pave the way for the quantification of the SCM data which is still a major challenge. Wong *et al.* have attempted to quantify the *FWHM* from SCM sweeps to D_{it} [300]. However, the model provided in [300] suffers from inconsistencies and consequently has not received major following. The analysis of standard samples as described above can be helpful in accurately quantifying the SCM data to D_{it}. This is because the SCM data and macroscopic D_{it} values from the same set of wafers will be available.

Chapter 6. Summary and conclusions

The quality and reliability of dielectrics grown on high carrier mobility strained Si and strained SiGe layers used in MOS devices were investigated at the nanoscale using electrical SPM techniques. Nanoscale analysis based on C-AFM and SCM was developed to study the localised variations in leakage current and trapped charge densities in thin dielectrics (< 3 nm) due to the underlying strained Si/SiGe surface morphology. Such nanoscale variations are masked during conventional macroscopic measurements. Agreement between device-level (macroscale) and nanoscale data validates the accuracy of the device de-processing, procedures, nanoscale measurements and the subsequent analysis for all devices evaluated.

The influence of substrate induced surface morphology on J_g in strained Si devices was assessed using C-AFM and the findings were presented in chapter 2. Fully processed MOS devices were analysed after layer by layer removal of the gate stack above the dielectric using wet etching at room temperature. LTO (150 nm) and NiSi (20 nm) were removed by using HF (10:1) for 75s while a 10% KOH solution at room temperature was required to remove 150 nm of poly-Si. An intermediate stage of poly-etch (HNO_3:H_2O:HF, 50:20:1) was also used between HF and KOH. This was needed as NiSi etching possibly resulted in a KOH resistant layer. Although poly-etch itself can be used for etching poly-Si, it is highly acidic and its etch selectivity against SiO_2 is poor compared with KOH. Hot phosphoric acid (H_3PO_4) was also attempted to remove NiSi. However, the etchant was not very effective as the etch rate could not be controlled. Raman spectroscopy, SEM, EDX and C-AFM were used at different stages to verify successful de-processing.

Following reverse processing, simultaneously obtained topography and leakage current maps were used to study the morphological dependence of J_g in strained Si MOSFETs. It was shown that degraded leakage and earlier dielectric breakdown characteristics of strained Si devices fabricated on rough SRBs observed macroscopically arise from large scale crosshatch morphology. The leakage correlates with the large regular surface undulations. Higher J_g was observed around troughs and steep slopes of the crosshatch compared with crosshatch peaks or crests. Increased nanoscale interface roughness, fluctuations in substrate composition and strain

fluctuations due to non-uniform growth rates may be responsible for the degraded leakage in these regions.

Gate leakage at the nanoscale was quantified using the Hertzian contact model to account for the AFM tip size. There is a good agreement between the magnitude of J_g at macroscale (device-level) and nanoscale for the same devices, confirming the accuracy of the method, including reverse processing and calculation of A_{eff}. Strong agreement between the breakdown behaviour at macroscale and nanoscale has also been observed with the smooth SRB devices having less leakage and taking longer time to break than the rough SRB devices. Bulk-Si devices showed the highest leakage due to lower barrier height.

Gate leakage in Si control devices and devices fabricated on smooth SiGe SRBs (which avoids the crosshatch pattern) does not appear to relate to any features on the underlying substrate. The morphological dependence of J_g on crosshatch undulations was lost after electrical stressing resulted in hard breakdown of the dielectric. This shows the need for smooth SRBs to obtain strain induced reduction in J_g expected with strained Si compared with bulk-Si. The maximum reduction in tunnelling current observed due to strain was 31% which was reduced to 17% for non-optimised SRB growth.

In chapter 3, nanoscale analysis of D_{it} in strained Si devices has been assessed using the SCM analysis. D_{it} has been obtained from individual locations on the substrate and has been related to the underlying defects and morphology.

Individual dC/dV sweeps showed that nanoscale D_{it} trends for bulk-Si and strained Si are in agreement with the macroscopic behaviour from devices grown on similar substrates, i.e., strained Si devices exhibit higher D_{it} compared with bulk-Si devices with rough SRB devices exhibiting the highest D_{it} amongst the three sets of devices. It has also been shown that dC/dV sweeps from troughs and steep slopes of crosshatch undulations (which appear as bright regions in the SCM maps) exhibit higher *FWHM* and hence higher D_{it} compared with peaks or crests. This morphological dependence of D_{it} on crosshatch undulations in rough SRB devices is similar to the variations in J_g studied in chapter 2, i.e. both J_g and D_{it} are enhanced near troughs and across steep slopes. With a fairly uniform dielectric, similar channel thickness and identical processing conditions, increased interface roughness across the conventional crosshatch undulations may explain the non-uniform behaviour in D_{it} for rough SRB devices. Fluctuations in Ge composition (out-diffusion during thermal processing) may also

contribute to non-uniform D_{it} and J_g along the crosshatch period. The difference in *FWHM* (and hence D_{it}) between the contrasting regions in the SCM maps of smooth SRB devices is reduced compared with the devices processed on rough SRB (with crosshatch). Strained devices which do not exhibit large crosshatch undulations but are rougher than Si control devices show reduced and more uniform levels of D_{it} compared with rough SRB devices. This is in agreement with previously reported macroscopic trends. Si control devices did not exhibit any morphological pattern, however, *dC/dV* sweeps from bright regions in the SCM maps of these devices exhibited higher *FWHM* (D_{it}) compared with dark regions.

The spectroscopic SCM analysis has also shown that large scale surface roughness has an impact on device variability. Smooth SRB and Si control devices exhibited smaller differences in D_{it} at different locations compared with rough SRB devices with large scale crosshatching.

Electrical characteristics of SiO_2 on compressively strained SiGe layers were studied using C-AFM and SCM in chapter 4. The variations in surface morphology and dielectric reliability with varying strain were studied by analysing different Ge concentrations (0%, 20%, 35%, 50% and 65%). The analysis in chapter 4 also allowed a comparison with the performance of SiO_2 on tensile strained Si channels (chapter 2). Layers with 50% or less Ge were found to be fully pseudomorphic. Slight relaxation was observed for the SiGe layers with 65% Ge as indicated by the XRD, Raman spectroscopy and AFM analysis. This is because the thickness of the $Si_{0.35}Ge_{0.65}$ layer exceeded its critical thickness. The Si cap on the strained SiGe layers was oxidised which resulted in a thermal oxide (SiO_2) with a thickness ~ 2.85 nm.

Leakage hotspots were found to be randomly distributed with no relationship observed between morphology and J_g using C-AFM. J_g was quantified and found to be increasing with the level of Ge in the strained SiGe layer. It has been shown that higher Ge contents (50% and 65%) reach the current limit of the measurement setup before lower concentrations. This implies that dielectrics on Ge rich strained SiGe layers break earlier than Si rich layers. Such leakage and breakdown behaviour is in accordance with previously reported device level data. Electron affinity comparable with bulk-Si and higher transverse effective mass are expected to be the reasons for degraded leakage with increasing Ge. Ge out-diffusion and the SiO_2/Si valence band offsets are also expected to play a role in enhancing leakage at higher Ge concentrations. Defects due to slight strain relaxation in the $Si_{0.35}Ge_{0.65}$ layers may also contribute to J_g. Nanoscale J_g

shown in chapter 4 is comparable with previously reported device-level data from compressively strained SiGe channel devices. Localised variations (< 2 Å) in t_{ox} show that variation in Ge content does not influence t_{ox}.

D_{it} is also found to increase with Ge content in the strained SiGe layer. Such nanoscale D_{it} behaviour is similar to previously reported macroscopic trends. Although D_{it} could not be quantified, comparison of *FWHM* and D_{it} from tensile strained Si (chapter 2) and a previous report suggested that D_{it} is less than 5×10^{11} cm^{-2}eV^{-1} for strained SiGe layers studied in chapter 4. Such levels of D_{it} are either comparable with or lower than previously reported macroscopic D_{it} in strained SiGe channel devices and hence are acceptable, especially for Ge rich SiGe channel devices. Moreover, the increase in D_{it} with Ge as indicated by the SCM analysis is expected to be less than an order of magnitude. The small increase in D_{it} with increasing Ge also supports the likelihood that Ge diffusion due to low thermal budget may not be significant.

The effect of increasing Ge on V_{FB} has also been studied by SCM. Variation in V_{FB} and $|V_{FB, shift}|$ suggests the presence of dielectric charges of both polarities. A reduction in V_{FB} and increase in $|V_{FB, shift}|$ has been observed when Ge content is increased from 50% to 65% in the strained SiGe alloy. This suggests increased net charge density which is also supported by the widely scattered *dC/dV* sweeps from the oxidised Si$_{0.35}$Ge$_{0.65}$ layer.

Sensitivity of the SCM setup to study other interfacial defects has also been indicated. For a low Ge content (20%) in the strained SiGe alloy, distortions in the *dC/dV* sweeps possibly due to metal contamination induced defects have been observed. This suggests that SCM has the potential to be a very sensitive technique for parameter extraction at the nanoscale.

The increased charge density and variability of the 65% Ge sample (which exceeded its critical thickness) further demonstrate the sensitivity of the SCM setup to study other defects and dislocations.

The SCM measurement setup has responded to differences in material quality and the nanoscale trends have found strong agreement with device-level data. However, low variability in nanoscale D_{it} and V_{FB} for some samples has posed a question on the effect of finite tip geometry. Devices which exhibit low density of uniformly distributed trap centres should be analysed through large number of measurements preferably using

more than one probe tip. The lower limit of D_{it} which may be studied with the current-up SCM setup requires further understanding.

In chapter 5, further work and applications which may utilise electrical SPM techniques are discussed. SCM analysis developed in the preceding chapters was applied to glass substrates coated with thin anti-reflective coatings. Such coatings are extensively used for realising energy efficient glass windows. The SCM metal tip, oxide coating (SnO_2) and the active layer (Ag) formed a MIM capacitor which responded accurately to variations in oxide thickness. The data suggests that the interface between the anti-reflective coating of SnO_2 and the active Ag layer is not responsible for the failure of solar control coatings. This agrees with finite element modelling which suggested that the Ag/ZnO interface is more likely to fail due to contact induced stresses. The SnO_2/Ag interface may fail over time during normal operation. However, this requires further analysis of solar control coatings which have been in active use for varying lengths of time. The work demonstrates that the SCM can be applied to thin anti-reflective coatings which may require nm scale analysis.

In order to fully understand the sensitivity of the SCM setup and to quantify the *FWHM* values from SCM to D_{it}, SCM analysis of standard SiO_2/Si samples is recommended.

To conclude, independent contributions to the electrical properties originating from localised regions on the substrate and dielectric have been identified on the basis of CAFM and SCM analysis. Nanoscale analysis has shown that a smooth SRB is required to obtain the full benefits of strained Si and avoid the enhanced leakage and charge density identified on the sloping edges of the crosshatched surface. The correlation between surface morphology, gate leakage and SCM signal suggests that for all dielectrics on high mobility substrates prone to surface roughening, the morphology as well as the dielectric itself can play a major role in the final dielectric quality. Optimized epitaxial growth will enable improved device performance, reliability and variability, as well as carrier mobility, for technologies incorporating CMOS on high mobility substrates.

The techniques developed to study strained Si/SiGe layers can also be used to study individual defects or regions on dielectrics whether grown or deposited (including high-κ) and on different substrates including SSOI, SGOI, strained Ge, SiC and graphene.

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