Investigation of High Bandwidth Biodevices for Transcutaneous Wireless Telemetry

By

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Thesis submitted for the degree of Doctor of Philosophy in Engineering

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July 2010

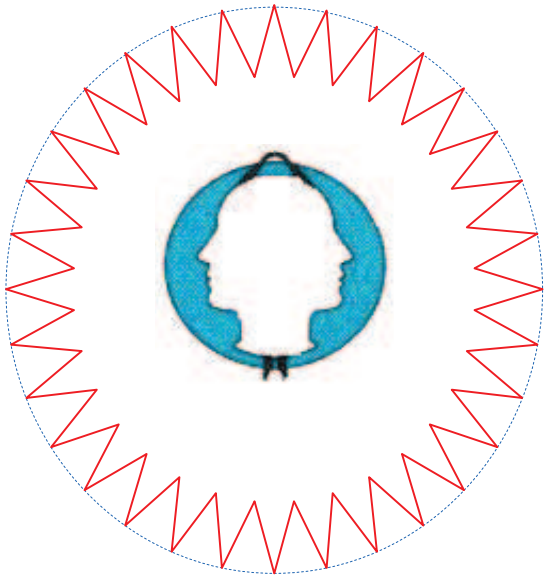
Abstract of the Dissertation

BIODEVICE implants for telemetry are increasingly applied today in various areas applications. There are many examples such as; telemedicine, biotelemetry, health care, treatments for chronic diseases, epilepsy and blindness, all of which are using a wireless infrastructure environment. They use microelectronics technology for diagnostics or monitoring signals such as Electroencephalography or Electromyography. Conceptually the biodevices are defined as one of these technologies combined with transcutaneous wireless implant telemetry (TWIT). A wireless inductive coupling link is a common way for transferring the RF power and data, to communicate between a reader and a battery-less implant. Demand for higher data rate for the acquisition data returned from the body is increasing, and requires an efficient modulator to achieve high transfer rate and low power consumption. In such applications, Quadrature Phase Shift Keying (QPSK) modulation has advantages over other schemes, and double the symbol rate with respect to Binary Phase Shift Keying (BPSK) over the same spectrum band. In contrast to analogue modulators for generating QPSK signals, where the circuit complexity and power dissipation are unsuitable for medical purposes, a digital approach has advantages. Eventually a simple design can be achieved by mixing the hardware and software to minimize size and power consumption for implantable telemetry applications. This work proposes a new approach to digital modulator techniques, applied to transcutaneous implantable telemetry applications; inherently increasing the data rate and simplifying the hardware design. A novel design for a QPSK VHDL modulator to convey a high data rate is demonstrated. Essentially, CPLD/FPGA technology is used to generate hardware from VHDL code, and implement the device which performs the modulation. This improves the data transmission rate between the reader and biodevice. This type of modulator provides digital synthesis and the flexibility to reconfigure and upgrade with the two most often languages used being VHDL and Verilog (IEEE Standard) being used as hardware structure description languages. The second objective of this thesis is to improve the wireless coupling power (WCP). An efficient power amplifier was developed and a new algorithm developed for auto-power control design at the reader unit, which monitors the implant device and keeps the device working within the safety regulation power limits (SAR).

The proposed system design has also been modeled and simulated with MATLAB/Simulink to validate the modulator and examine the performance of the proposed modulator in relation to its specifications.

Acknowledgement

First and foremost, I would like to express my appreciation to my supervisor , ***Dr. Graeme Chester*****,** for help and guidance during my studies. He has always been willing to help, explain and discuss any matters with me over the past three years. I would also thank my second supervisor, ***Mr. Jeffrey Neasham***, for his helpful explanations, and guidance in the experimental setup , and practical discussion. I am intensely indebted to many people who made my time in the EECE School, at the electronics Lab use the design Tools and taught me how to use the Measurement equipments. Namely, Mr. Brian Smith, Mr Stephen Robson, Mr. Darren Mackie, Mr. Jack Noble, Mr. Jeffrey Warren, and Mr. Graham Ewart, the Staff of ITC for their support during my study. Ultimately, the staff of Mechanical workshop for their support and helpful during my PhD.



Second, I acknowledge with thanks the support provided by the scholarship from the Higher Education Ministry in Libya to study and complete my degree .I must thank friends in H.E.M in Libya, the UK regional section, and also all the staff in Libyan Cultural Affairs in the Libyan Bureau in UK, I am specially indebted to thanks of all my colleagues in the general post telecommunication company, and the higher professional electronics institute. I would like to thanks Newcastle University for its support and good facilities to study. Finally, I would like to dedicate this work to my wife, my parent and family for the extraordinary sacrifices and their constant encouragement through of my study and emotional support whenever needed during my time at Newcastle University. Finally, I thank my friends for the support they have given me in so many ways.

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Introduction

Introduction

Chapter I

Semiconductor chips are used today not only in communication or control systems, but also in our bodies, for diagnostic or monitoring signals, such as electroencephalograph (EEG), and electrooculography (EOG). They are used to understand electrical brain activity, with the nervous system behavior, and process it within implant circuitry [44] [46] [47] and [68] [75]. Generally, the investigation of the brain function has been targeted by many researchers and universities in the past and this century [114]. The human brain maintains over 14- billion nerve cells; 9-billion of these are distributed over 64 sections in the brain [210]. These bulk networks are being investigated by researchers and neuroscientists who have began to use bundles of tiny wire cables and multi electrode arrays, for monitoring and analysis of the many neurons in the brain, which are essential to understand the neural substrates of many physiological and pathological brain diseases, such as epilepsy and paralysis. The transcutaneous wireless telemetry implant is one of these technology solutions applied in biomedical applications, used to avoid a susceptible path to infection in the body and reliability problems. This eliminates the needs for tethering wires or implantable batteries [45] [50]. The research is continuing to develop many different types of electronic biomedical devices which may give prosthetics for treatments of a range of other wide ailments, such as blindness, quadriplegia, epilepsy and Parkinson's diseases [161]. On the other hand, these electronic devices are used especially in biomedical applications. These characteristics are imperative because the devices are difficult to access and the consequences are serious if the devices malfunction or fail, which requires knowledge of material behaviour and media. This chapter gives an overview of biomedical device topologies that are used in medical treatment in hospitals, clinical, telemedicine, and healthcare. Finally, there is a summary of the applications of transcutaneous biodevices, which are based on wireless infrastructure and a study of most of the applications for the magnetic field applied to the human body.

1.1 Biodevices Technology

Biomedical devices technology has been recently used for medical applications in the human body, by monitoring or recording many signals such as electrocardiogram (EKG), electroretinogram (ERG), and electromyography (EMG) [154] and [164]. Many research groups at institutes and universities are focusing on biomedical circuit devices. Predominantly these are to understand disorders of brain behaviour and processing it within the implant circuitry. These biodevices may solve many biomedical disorders, such as epilepsy and Parkinson's disease, which are caused by many factors. Typically, a wireless biomedical device consists of two parts, a reader that transfers a power RF signal, when the biomedical electronics device is swallowed or surgically implanted in a subject/patient, and can control the device from outside the body through an inductive coupling downlink, using a variety of modulated energy forms like electromagnetic energy [137]. On the other hand, the implantable device can communicate with exterior world by up-link, whether over inductive wireless coupling or UHF links to transmit the acquired data from the body [100] [96]. General examples of applications for the human body are shown in Figure (1.0).

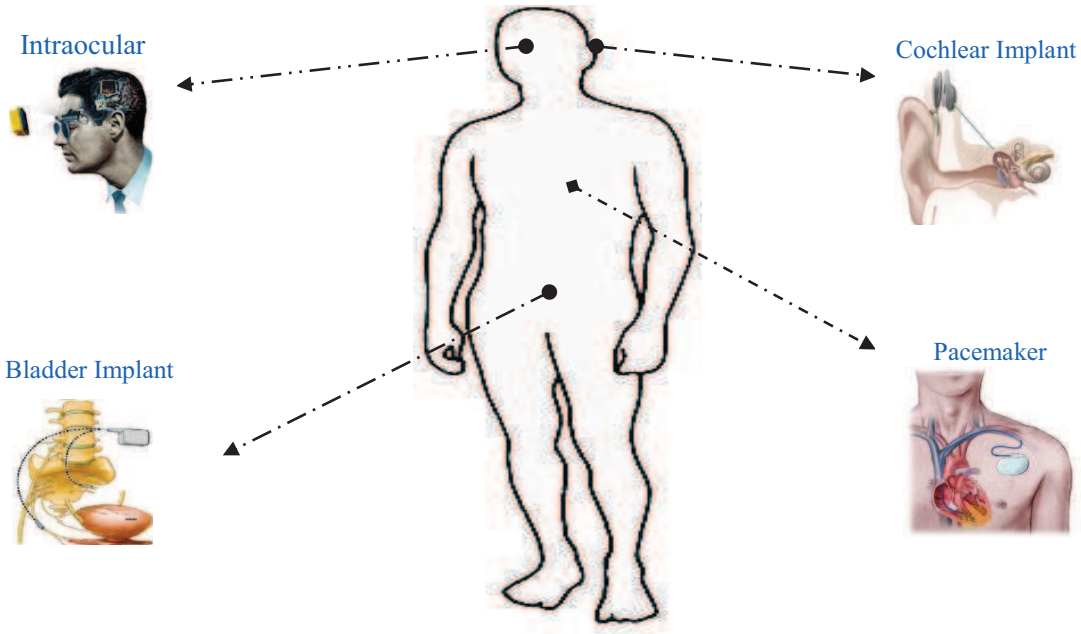


Figure (1.0) Implant technology applications in the human body

Conceptually, most biodevices are bi-directional systems which transmit RF signal carriers when they are swallowed or surgically implanted in a subject/ patient. They can communicate with biological or physiological parameters which are transferred through different medium types between two locations including air space, water and biological tissue (blood, fat, bone, etc) [43],[48]. The classification types of most common Passive/Active wireless telemetry applications and purposes are illustrated in Figure (1.1) [151] [193].

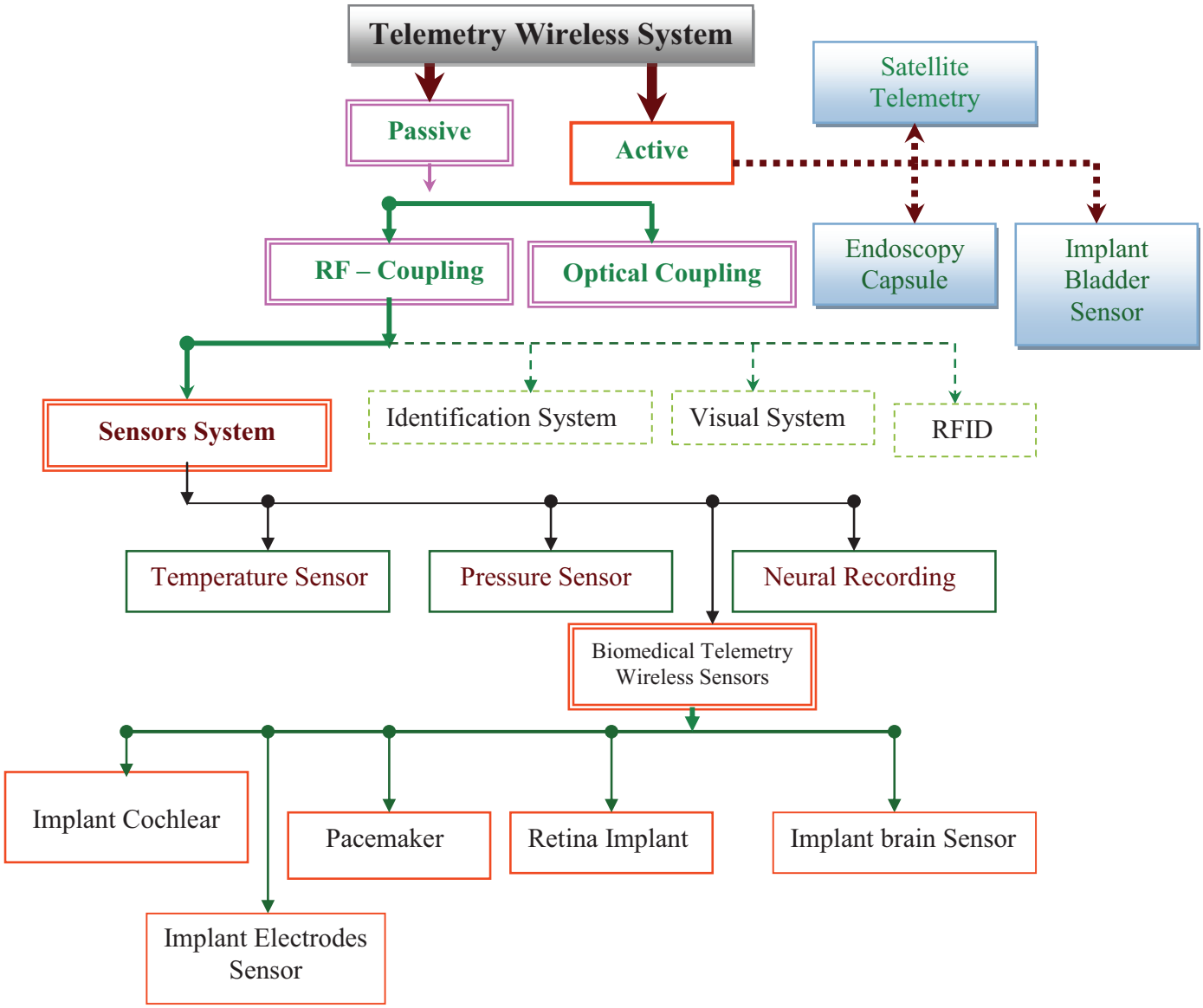


Figure (1.1) the active and passive wireless telemetry types and applications

1.2 Implantable Technologies For Medical Applications

Implant technology has developed via further investigation and studies on human diseases in combination with work on electronic circuits. One of these technologies which is now used wireless implantable sensors; this new technology application is derived from the transcutaneous implant telemetry devices inside the body. It has been recently used for medical applications in the human body; one of these application examples is rehabilitation for replacing the damaged organs by biomechanical electronic devices to do the same function [154] [155] [159] and [160]. Almost all conventional wireless telemetry has limited applications, and this chapter describes most of the applications topology using inductive coupling as based in our work, whilst chapter three covers the background and design of the inductive coupling link and data over a magnetic link. The basic system consists of a bi-directional data transmission channel through the skin tissue of the patient. The data acquired from the matrices of sensors are converted into digital form modulated signal and retransmitted into a reader unit for analysis and processing (Up-link) [82] [105] and [175]. The general bio-communication architecture system for collecting data from the nervous system is described in Figure (1.2) as an example based on the work in the this thesis.

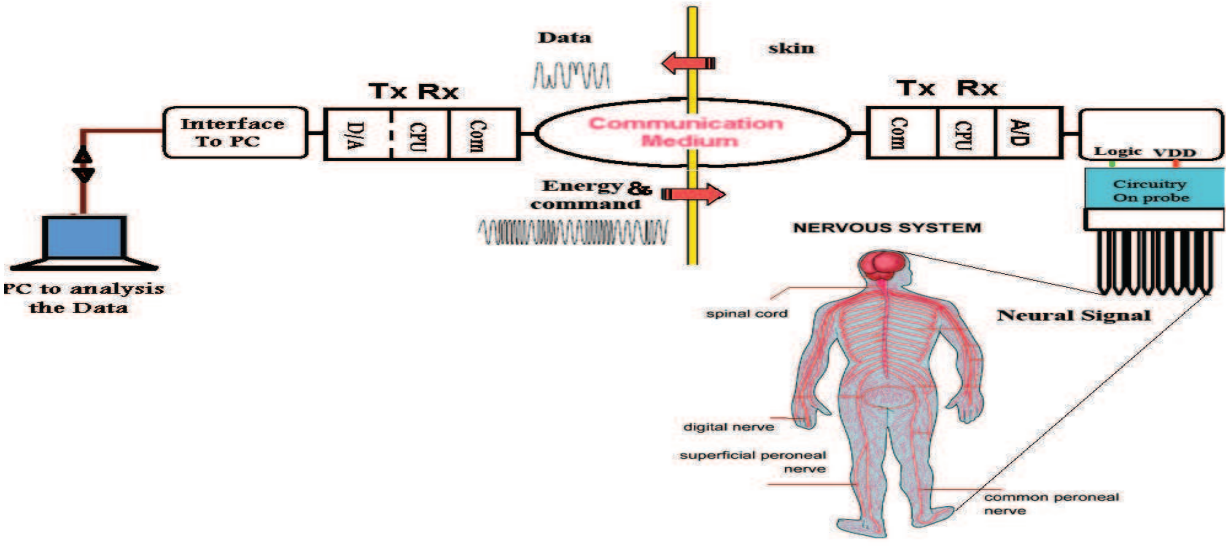


Figure (1.2) the bio-communications system architecture

1.2.1 Implant Cochlear Technology

Cochlear technology uses wireless coupling coils through human tissue, with the interior implant inside the head of a patient, and the exterior part outside the body [67] [148]. The exterior part picks up the sound from around a microphone, amplifies it and manipulates this sound by a speech processor, and then retransmits it through the inductive coupling. However, the interior coil is implanted surgically, and placed to get the optimum coupling with the exterior coil. The modulated RF signal offers the DC-source for the implant electronic circuits, and the electronics used in the implant cochlear device need to be of low power consumption and high reliability [109]. When the demodulated data are converted into electrical signals for the cochlear nerve, the electrical pulses are sent to the brain. The brain analyses these electrical pulses as received information, which enable the patient to understand and respond to sound, and can enable disabled patients to hear. Generally, the principle of cochlear implant technique has been shown in Figure (1.3). Typically the acoustic band frequency for humans is between 300~ 3400 Hz, the transferred data through the coils are low rate, which is a few kbps [70] [144]. This kind of technology overlaps with the work presented here because of the inductive coupling link, for the implant coil design.

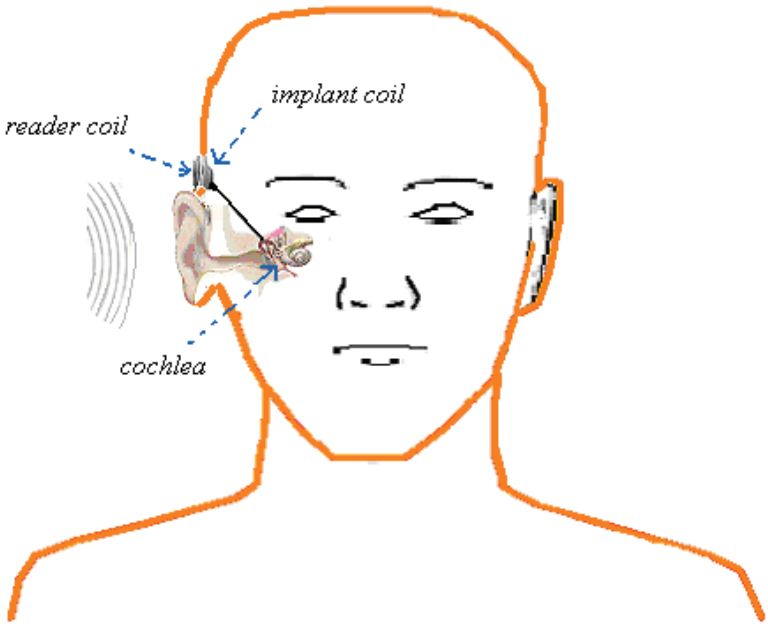


Figure (1.3) the cochlear implantable coil

1.2.2 Intraocular (Retinal) Implant

One of the main growth areas in application research is retinal implant or Bionic eye technology, to help blind patients or retinal disease sufferers with their sight, and help people get a sense of their surroundings. This technique replaces and strengthens the damaged optic nerve (ganglion cells). It provides light and image to the brain's vision system for normal processing [112] [76]. The RF antenna foe inductive coupling is used to communicate with the exterior part reader, which supplies the implant with the required DC power, and transfers the image data from the video camera. Moreover, a tiny implant coil on the surface of the eye receives the wireless signals from an external camera, which the patient wears on a pair of spectacles that contain a camera, transmitter and wearable computer to process the signal from the camera. The camera stimulates the normal eye which converts the view into an electrical image signal modulated to transfer over wireless coupling link into the implant coupling inside the eye. Light and image signals are received through a pair of coils and received by an array of electrodes surgically implanted on the retina. The array delivers electrical signals to the nerve cells in the eye, mimicking the role of light-sensitive cells lost in degenerative retinal disease. The general architecture of a retina implant is shown in Figure (1.4).

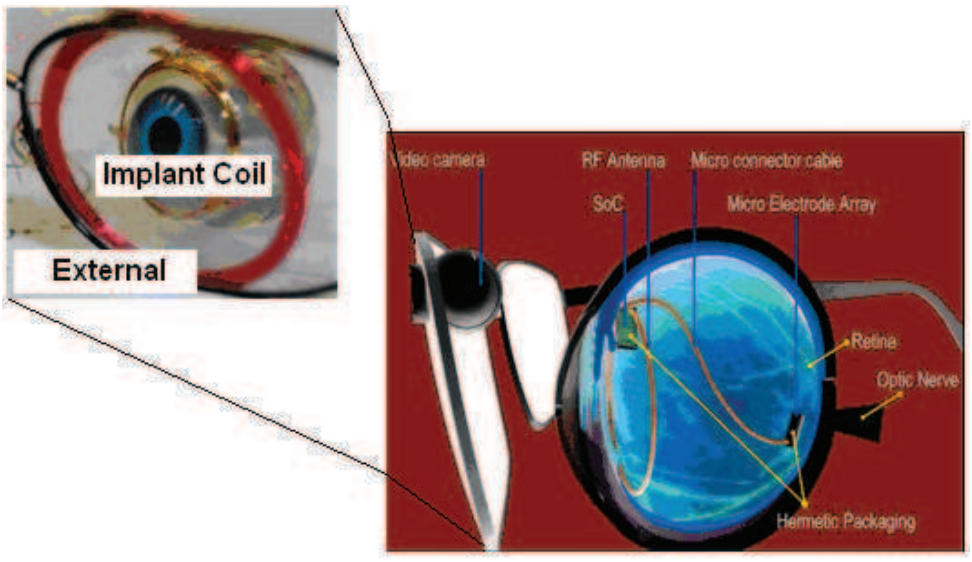


Figure (1.4) Principle architecture of the retinal implant device [198]

1.2.3 Brain Implant Device

Brain-stimulation devices for treating depression have faced unexpected setbacks, to help millions of people who fail to respond to antidepressant drugs. The brain pacemaker device is implanted in the chest of a patient, with leads that send electrical impulses into parts of the brain. They have already been approved to treat movement disorders such as epilepsy, and Parkinson's disease tremors and depressed patients have improved significantly [117] [175]. Figure (1.5) shows the brain stimulator pacemaker construction for the patient, surrounding the vagus nerve [218]. In particular, children suffering from dystonias can benefit from brain pacemaker surgery. However, a brain pacemaker implantation is only advised in cases when the aforementioned drugs and combinations thereof do not lead to satisfactory treatment results and in patients less than 70 years of age. Additionally, the brain device is powered with a long life battery. One of the development solutions introduces a wireless power coupling technology to avoid additional regular surgical operations to replace the old battery, and which may cause the malfunction of the device when the battery is replaced. The wireless technique offers full control for the device and improves the performance, and gives more flexibility for the patient remotely.

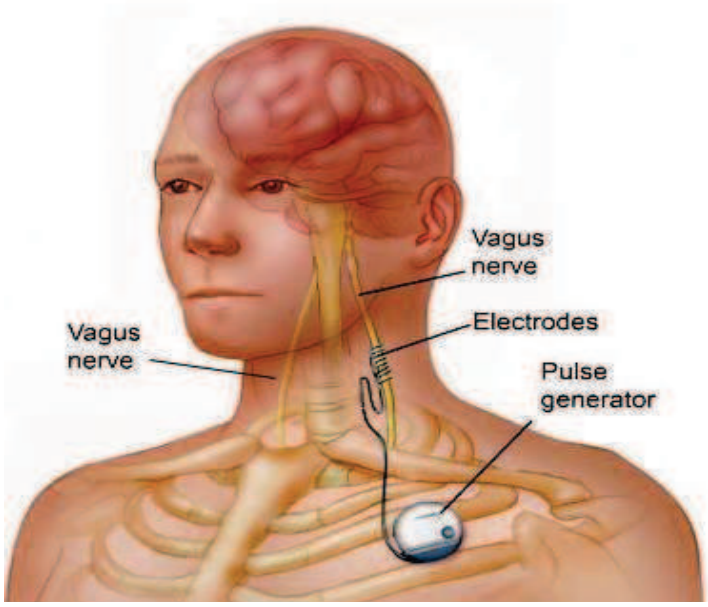


Figure (1.5) the brain pacemaker implant device [218]

1.2.4 Pacemaker Device

In recent years there has been a high rate of surgery for artificial heart implants and cardiac pacemakers for monitoring and controlling irregular heart rhythms, especially for babies and the elderly. A newly developed artificial heart is called the intelligent smart artificial heart, created in order to realize the safe treatment and effective control for patients [154]. However, wireless inductive coupling can be used to communicate between the pacemaker and artificial heart using a wearable reader outside the patient [159] [160]. This avoids the surgical procedure for replacing the battery. Typically it provides the energy and control data, gathering back data from the implant pacemaker device. We demonstrate in Figure (1.6) the wireless application for a pacemaker or artificial heart. The new technology using Bluetooth can provide a simple interface with the patient, where the information can be accessed by mobile phone or interface with a web network to connect them to the Hospital or clinic. Obviously, electrical magnetic interference (EMI) may be one of the main effective causes, and could be a defect of the highly sensitive devices, which work in, near or interface with magnetic environment field such as RFID magnetic area [72].

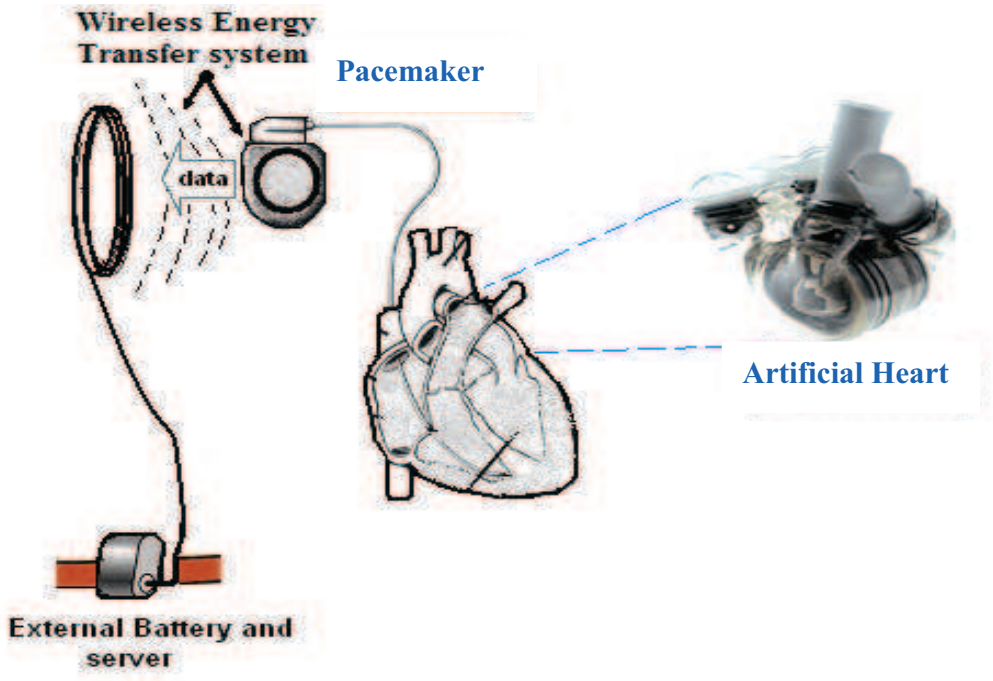


Figure (1.6) the wireless communication for artificial pacemaker device

1.2.5 Wireless Capsule Endoscopy

The wireless capsule endoscopy (WCE) is based in a vitamin size pill which captures the images of the digestive tract, while it is transported passively by peristalsis. The device consists of an image sensor, an illumination module, a radio frequency transmitter and a battery [203] [157]. The architecture diagram of a capsule endoscope is shown in Figure (1.7). The WCE is used to perform a painless diagnosis inside the gastrointestinal tract. The test requires a patient to ingest, after a one night fast, the WCE, which is carried by peristalsis through the digestive area. During the transit the pill takes images from the CCD camera system, which are transmitted to an antenna placed outside the patient's body. The second generation of WCE uses magnetic fields generated for controlling the capsule from outside the body in certain directions [76]. The received electromagnetic energy is converted into a power supply for the capsule that is capable of localizing the device and determining the location of the pill inside the patient's body. Figure (1.8) describes the movement of the capsule inside the patient body, which communicates with wireless transmission to the PC.

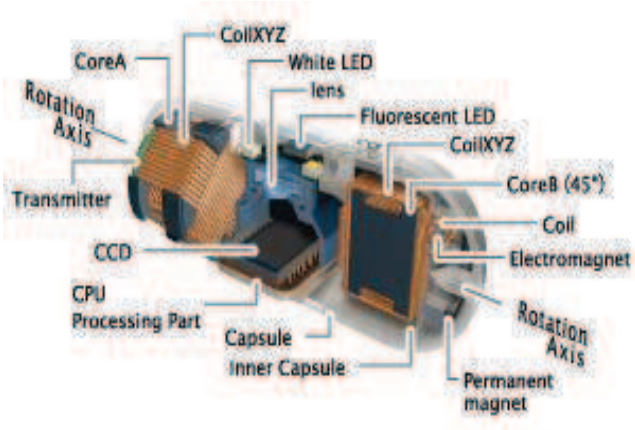


Figure (1.7) the Architecture of Endoscopy Capsule [203]

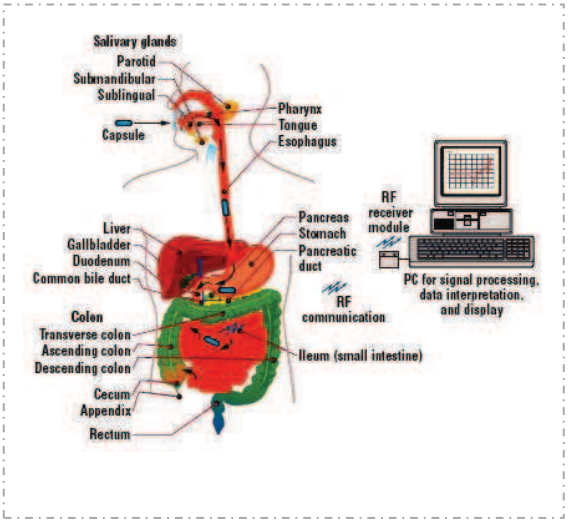


Figure (1.8) the Endoscopy System [76]

1.3 Media Absorption Side Effects and Technology Limitations

Generally, there are an increased number of wireless applications, with most of the biomedical devices being augmented by the wireless environment techniques. The biomedical electronics devices use inductive magnetic communication for controlling or monitoring the acquisition back data from the patient. The magnetic flux that crosses the patient's skin is coupled with the implant coil inside the body. The body attenuates the magnetic field, which is dependent on the frequency used for coupling [143]. Table (1.0) illustrates the electrical properties of the body at ISM frequency [201], and the occupational exposure level of the electrical and magnetic fields varying with time are shown in Table (1.1) [211].

Table (1.0) the Electrical data of biological tissue used at 402MHz [201]

Biological Tissue	**Permittivity (ε_r)**	**Conductivity** $\sigma(s/m)$	**Mass Density** $\rho(g/cm^3)$
Brain	**49.7**	**0.59**	**1.04**
Skin	**46.7**	**0.69**	**1.01**
Fat	**11.6**	**0.08**	**0.92**
Blood	**64.2**	**1.35**	**1.06**
Bone	**13.1**	**0.09**	**1.81**
Muscle	**58.8**	**0.84**	**1.04**

Table (1.1) Permitted level of exposure for electric and magnetic fields over frequency [211]

Frequency range	**E-field strength** $(V\,m^{-1})$	**H- field strength** $(A\,m^{-1})$	**B-field** (μT)	**Equivalent plane wave power density** $S_{eq}(Wm^{-2})$
up to 1 Hz	—	1.63×10^5	2×10^5	—
1–8 Hz	20,000	$1.63 \times 10^5/f^2$	$2 \times 10^5/f^2$	—
8–25 Hz	20,000	$2 \times 10^4/f$	$2.5 \times 10^4/f$	—
0.025–0.82 kHz	$500/f$	$20/f$	$25/f$	—
0.82–65 kHz	610	24.4	30.7	—
0.065–1 MHz	610	$1.6/f$	$2.0/f$	—
1–10 MHz	$610/f$	$1.6/f$	$2.0/f$	—
10–400 MHz	61	0.16	0.2	10
400–2,000 MHz	$3f^{1/2}$	$0.008f^{1/2}$	$0.01f^{1/2}$	$f/40$
2–300 GHz	137	0.36	0.45	50

1.3.1 Skin Tissue Attenuation

One of the objectives of this thesis is to investigate the body skin attenuation for electromagnetic fields. Most of the studies for electromagnetic radiation exposure of the biological tissue cover the mobile phone radiation effects for a human body. The interactions of the radio frequencies are not specific to a certain frequency; the exposure field is characterised by the frequency, intensity and polarization. For microwave radiation it is essential to compute the absorption rate (SAR) for high EMF power [211]. At low frequency working in biomedical device applications, the RF EMF generated by the transmitter coil toward the human body, received by a small loop coil as implant part, is less than a few Watts. In practice, the area where the type of coil is located at the external layer of the skin is the critical place to be considered for reduced attenuation. However, the body tissue layers affect the absorption of electrical and magnetic energy. A generic body model is defined consisting of planar layers of skin, fat and muscle tissue. Fat tissue has very low water content and therefore a significantly lower permittivity and conductivity (ε_r = 5.5, σ= 0.05S/ m), whereas muscle tissue has permittivity and conductivity of (ε_r = 55.0 σ= 0.95S/m) [72]. The skin tissue varies from 0.4mm to 2.6mm thick. These values include the epidermis and dermis and cover an age range from newborn to 60 years. On other the hand the fat layer thickness takes into account all possible effects due to impedance matching in the body layers. The layered body tissue is shown in Figure (1.9). The main factors affecting the attenuation for electromagnetic signal through the patient skin can be expressed in equation (1.1) [210].

$$\alpha = \omega\sqrt{\frac{\mu\varepsilon}{2}}\left[\sqrt{1+\left(\frac{\sigma}{\omega\varepsilon}\right)^2}-1\right] \qquad (1.1)$$

where:

- *(ω) is the angular frequency*
- *(ε) is the permittivity*
- *(σ) is the conductivity*
- *(μ) is the Permeability*

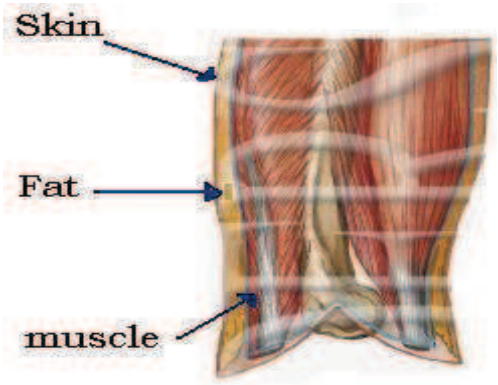


Figure (1.9) Different layers for the skin [209]

It clear that the greatest effect of RF energy as a result of exposure to electromagnetic fields at relatively low levels (below 10 mW/cm ^{2}), is on the eye and the gonads. Those are particularly susceptible to heat, and have been extensively investigated [139]. The radiation at frequencies above 800 MHz can produce injury to the eye and this type of injury depends on the frequency, and millimeter waves can produce keratitis. Cataracts develop after a sufficiently long exposure to power densities above 100mW/cm ^{2} . The biological effects are related to the intensities of the fields within the living body, not to the external intensity of an exposure field. The internal fields are a complex function of exposure conditions and other parameters. The internal fields are frequently described in terms of the Specific Absorption Rate (SAR), which expresses the rate of energy absorption (e.g., at a given location, or averaged over the whole body) and is proportional to the square of the internal electric field intensity. The proportionality constant depends on the electrical properties of the tissue. The average SAR for a whole body, far-field (far away from the radiator) exposure depends on the field frequency, intensity, direction, subject-to-source configuration, subject's size and shape, and presence of other objects. Particularly with metal objects in the immediate vicinity, increased absorption occurs in various places inside the body, resulting in so-called "hotspots". For human beings maximum energy absorption take place between 30 and 100 MHz, depending on the body size and the environment [174]. For an average man isolated from ground the frequency of the maximum absorption is about 80 MHz. However, for the SAR the important parameters are absorbed energy in the area where the type of antenna is located, the outer layer of the skin current distribution and the distance between reader transmit coils and the receiver coils, in near field radiation of transcutaneous wireless coupling. The SAR is usually averaged either over the whole body or over a small sample volume typically (1g or 10g of tissue) and has units of Watts per kilogram. It can be calculated from the electrical field within the tissue as defined in the equation [219]:

$$SAR = \frac{\sigma |E^2|}{2\rho} \quad \left[\frac{W}{kg}\right] \tag{1.2}$$

where:

- *(E) is the Electrical field strength*
- *(σ) is the conductivity of tissue*
- *(ρ) is the sample of mass density of tissue*

1.3.2 Electromagnetic Interference (EMI)

The electromagnetic inductive coupling link has been used in biomedical applications, and the implant device coil can receive any transmit signals around it. That could cause the device to malfunction, if it is resonant at the same received frequency [72] [115]. Hence, it is difficult to shield the inductive coupling, which is an open transformer, to protect the implant microelectronics device from undesirable magnetic fields. It is required to develop a suitable solution to minimize the risk for the patients. Typically, the low frequency field induces currents in the human body that can have an effect on the sensory, nerve and muscle cells. The greater field strength, the more pronounced the effects [217] [196]. On the other hand, the high frequency fields heat the human body, and the degree of the absorption of electromagnetic waves is a function of the frequency and intensity of the field and the type of tissue. The organs with lesser blood flow are the most endangered, e.g. the eyes. In contrast, the heart and brain are better at handling heat due to their better blood flow [187]. However, the strength of field decreases at increasing distance from the source of radiation. In addition, the electrical charges absorbed by the body (static charge) could cause malfunction of electronic devices. Figure (1.10) demonstrates the most common sources around the patient which could cause effects.

Figure (1.10) the most common EMI interfaced into the human body

1.3.3 ISM Band Frequency For Medical Applications

The implant biomedical system is under rapid development for many applications. There are demands for a higher data rate over the wireless environment that requires a high bandwidth and high frequency carrier. A new unlicensed Industrial Scientific and Medical "ISM" frequency band (402~405 MHz) was recently reserved for medical implant communication system by the FCC Federal Communication Commission, and recommended by ITU-R [192] [210]. This band seems attractive providing low body absorption at these frequencies comparing to other frequencies. Figure (1.11) demonstrates the most common frequencies covered in biomedical wireless applications. However, the frequency for transcutaneous telemetry devices rises up into the microwave band, which is shared with other wireless applications. Typically other applications use the microwave frequency band (2.45 GHz-5.8GHz), for example the satellite telemetry for animal tracking and microwave tomography for medical image analysis, and widely used devices such as RFID, Bluetooth, car alarms, microwave ovens and wireless home phones, which are operated at 2.45GHz, may cause interference effects for various implant devices. Disadvantages of using the microwave frequency in the human body, concern certain frequencies which have biological effects such as thermal damage or overheating of the blood or tissue [139]. Conversely, the chosen carrier frequency is most important for designing the electronic implant system, for less interference; our chosen frequency was 135 kHz as RF power carrier frequency in our application, whilst our target frequency is 402MHz for the implant device.

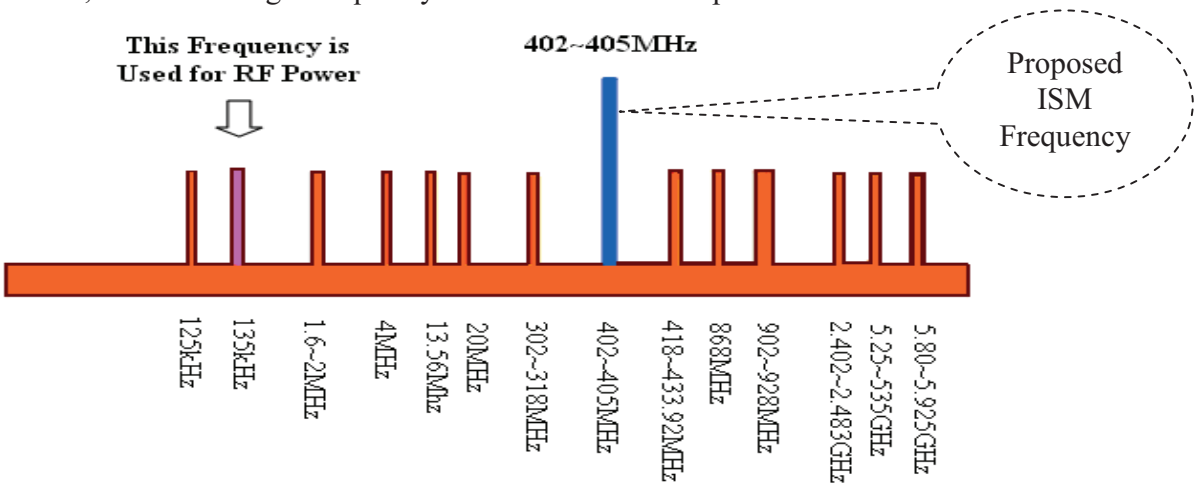


Figure (1.11) ISM frequency bands used for medical applications

1.4 Acquisition of Neural Signals

To acquire and record neural signals, such as Electroencephalography (EEG) or electromyography (EMG), to assist understanding of the brain behaviour signals, requires processing of signals within active integrated electronic implant circuitry [114]. The EMG has an amplitude of only 1mV so to detect it an amplifier is needed and filtering is required for the noise or electromagnetic interference. Generally, the noise is generated by many common applications such as power lines, fluorescent lights, computer and monitors, and that is added and amplified with the EEG signal will often swamps the EEG signal [105] [140]. Figure (1.12) demonstrates the frequencies with respect to amplitude for different acquisition signals from the body. The Utah microelectrode array captures the respond commands signals from neuron cells, processing and coding this information and re-transmitted to the reader unit or interface PC. Eventually Utah electrodes are brought out to a small printed circuit board with multiplexer brought out to a micro tech connector [44] [150] and [151]. The architecture of the Utah microelectrodes arrays (UEA) is demonstrated in Figure (1.13). The UEA total is (10 x 10) array of 100 platinum–tipped silicon extra cellular electrodes, and amplifies the neural signal from each electrode. This data is digitized and transmitted over an RF link mounted on the chip [168] [137] and [161]. It is necessary to increase the conveyed bit rate, and reduce the effects of the interference or increase signal to noise ratio (S/N), where the neural signal is less than 500μV.

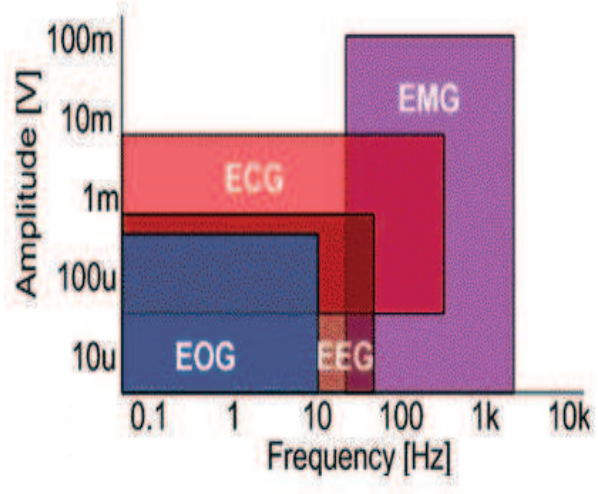


Figure (1.12) the frequencies and amplitudes of body signals

Finally, samples of signals captured by Utah microelectrodes are presented in Figure (1.14).

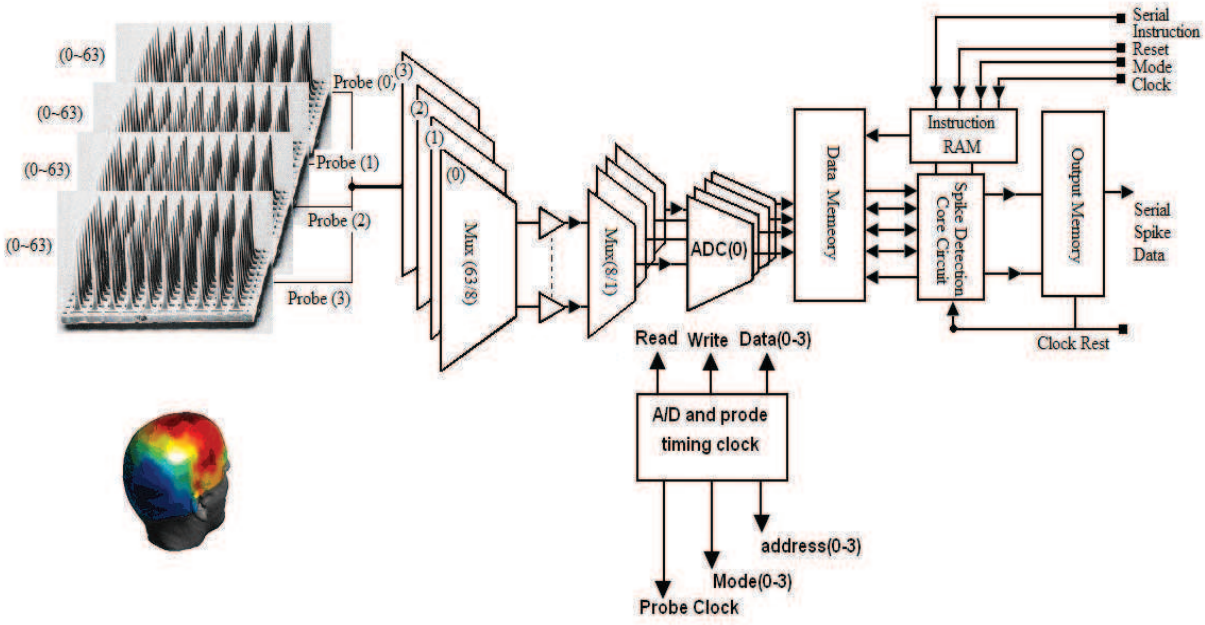


Figure (1.13) the architecture of Utah microelectrodes array [151]

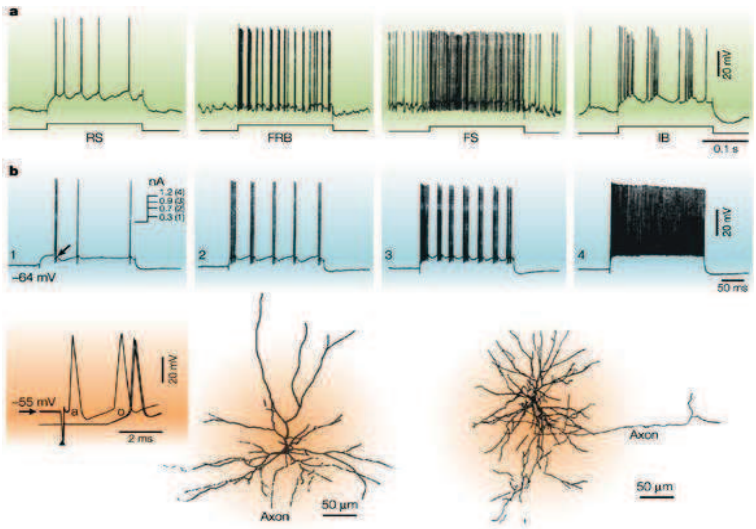


Figure (1.14) Captured signals from Utah microelectrodes [196]

1.5 Biomedical Telemetry Chips and Applications

In recent years, many researchers have developed different packages of miniature implantable devices. To study the complex neurons involved in scientific phenomena such as cochlear disease, epilepsy, and aggressive behaviour, it is necessary to observe the electrophysiological activity in real time. Figure (1.15) shows the prototype samples of fabricated chips for medical purposes, and there are different chips for medical solutions such as blood pressure sensors, bladder sensor, and cochlear implant, retina and sphincter sensor [156]. However, there are many medical instruments that use electronic devices, such as insulin pumps and breathing activity monitor. There are still many biodevices under investigation for improving the power efficiency and coupling link and using different schemes for maximizing the data rate with low noise and minimum size. The second research point is the interface technology with the medical device and networks or appropriate adapters such as PC or mobile phones. This gives to the patient the flexibility to use the devices remotely. Figure (1.16) shows the biomedical device interfaces for communication and flexibility of technology for patient use [48] [49] [177].

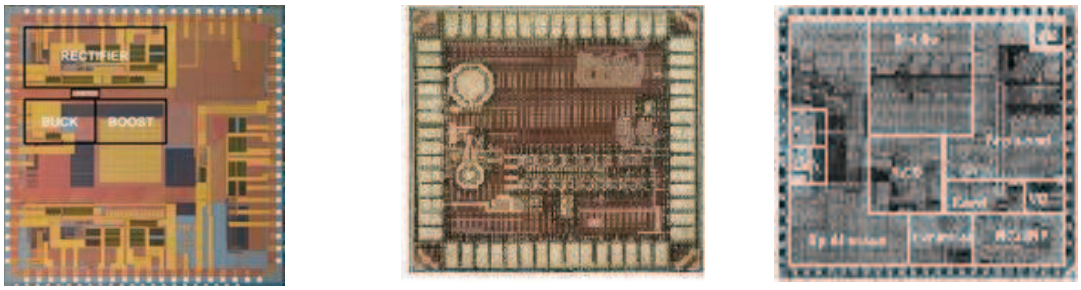


Figure (1.15) the layout of different medical chips [49]

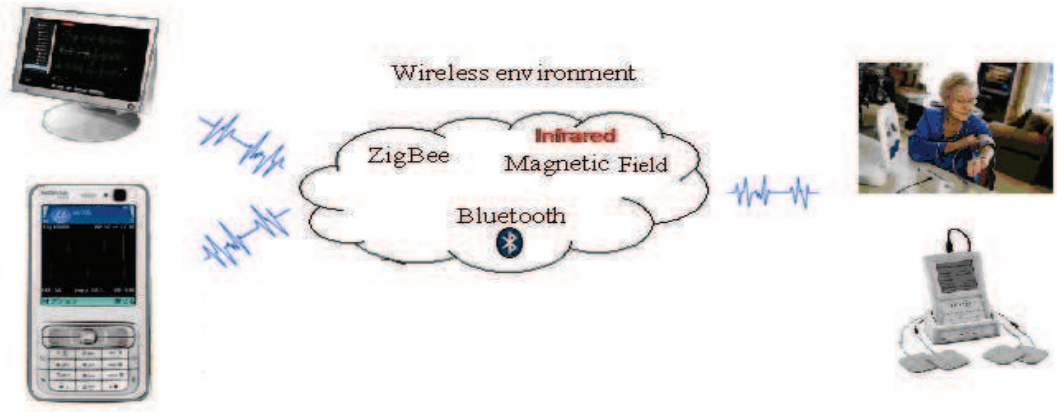


Figure (1.16) the medical care interface communication

1.6 Chapter Summary

This chapter has shown an introductory summary of the recent and previous study cases and researchers working on biomedical implant telemetry devices applications. Briefly, it describes the disorders and ailments of the human body such as epilepsy, paralysis, Parkinson's disease, and nervous system disorders. It has briefly summarized the key design elements of most of the design factors for electronic implant devices that are commonly used in wireless communication. The Table below (1.2) shows the main comparison parameters between data rate and communication distance, for different biomedical applications. They use different modulation schemes over the wireless coupled link and different RF carrier frequencies. The term near field communication is used when signals are inductively coupled between reader and implant for data transmission. However, demand for a higher data rate for the acquisition data returned from the body is increasing, and requires an efficient modulation technique for achieving a high transfer rate and low power consumption. These are the main challenge factors in implant devices, and are therefore our goal in this work. For example, the human voice band is between 300~3400 kHz; obviously it does not require a high RF frequency for manipulation. However, visual implants such as retinal implants or wireless endoscopy capsules, which work with image data and control signals transmitted in real time, deal with high speed data for transfer over a magnetic communication link. These types of technology may need a high rate modulator to encode the huge amount of information.

Table (1.2) summary of the published research for implant devices

TX- Carrier Frequency	Data encoding Modulation	Data - Rate	Comm. Range	Publication Year	Publication References
125 to135 kHz	FSK	4kbps	20cm	2002	[201]
1.6-2MHz	FSK	1.2kbps	3.5cm	2005	[179]
4 MHz	ASK&PWAM	60kbps	2.8cm	2004	[128]
13.56MHz	BPSK	1.12Mbps	1.5cm	2005	[135]
2MHz	ASK	8bps	0.6cm	2005	[150]
27MHz	FM	9bps	1-2cm	1998	[45]
402-405MHz	FSK	20kbps	1-2cm	2005	[145]
868 to 928 MHz	FM	Low rate	91cm	2005	[151]
3.2 GHz	FM	Low rate	2.5 cm	1995	[204]

The previous table (1.2) compares the main research approaches for implant devices design. Most implantable biomedical devices have attributes of small size and high reliability, long retention rate, with very low power dissipation and field conformability. Clearly, most of the published works by researchers are using in analogue modulation and high carrier frequency, where the communication is still very short distance. So we consider in our work these points for introducing a new design for improved performance. Figure (1.17) shows the different biomedical devices applications and compares the power dissipation for each device with respect to data rate over communication range between telemetry device and reader over inductive passive coupling [67] [94] [158] and [164].

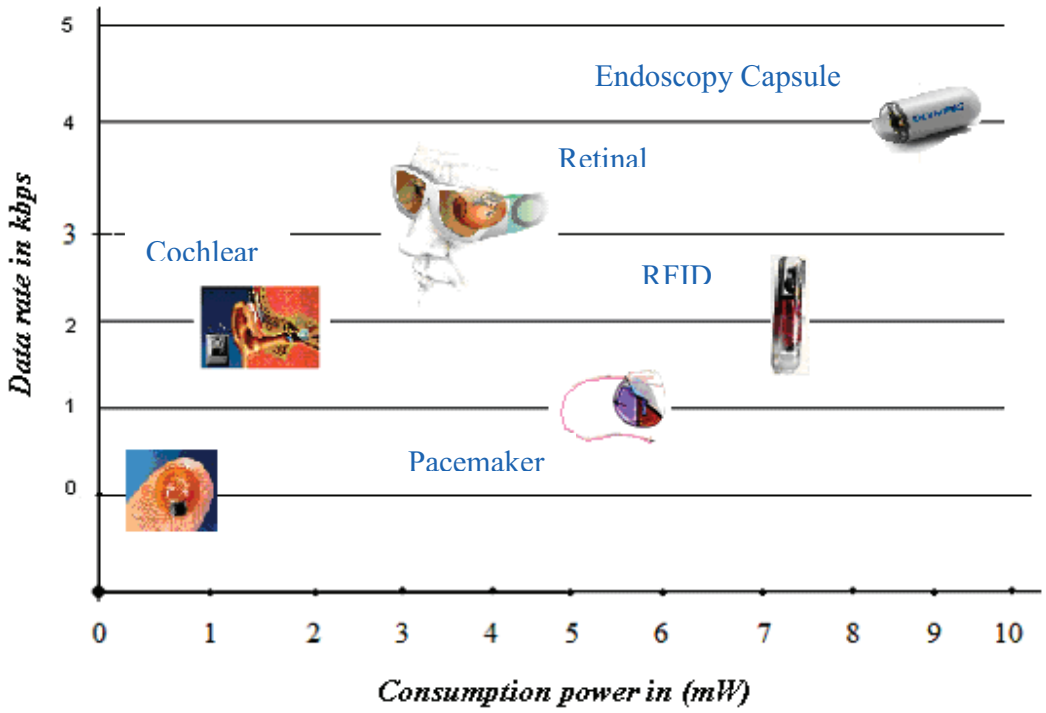


Figure (1.17) comparing the power dissipation for biomedical devices with respect to data rate

Finally, most of the acquisition data signals have been summarised, which can be observed or captured from the human body. Predominantly, this is generated by organs such as the heart under different conditions or is measured from the nervous system to communicate with the brain and perform the motion of the body's reaction with respect to the external world as shown in Figure (1.18). These are signals can be recorded monitored or captured from the human body. However, the new tele-medical health help care technology is able to access a web network that offers to the patient the facility for interface with hospital and their doctors remotely.

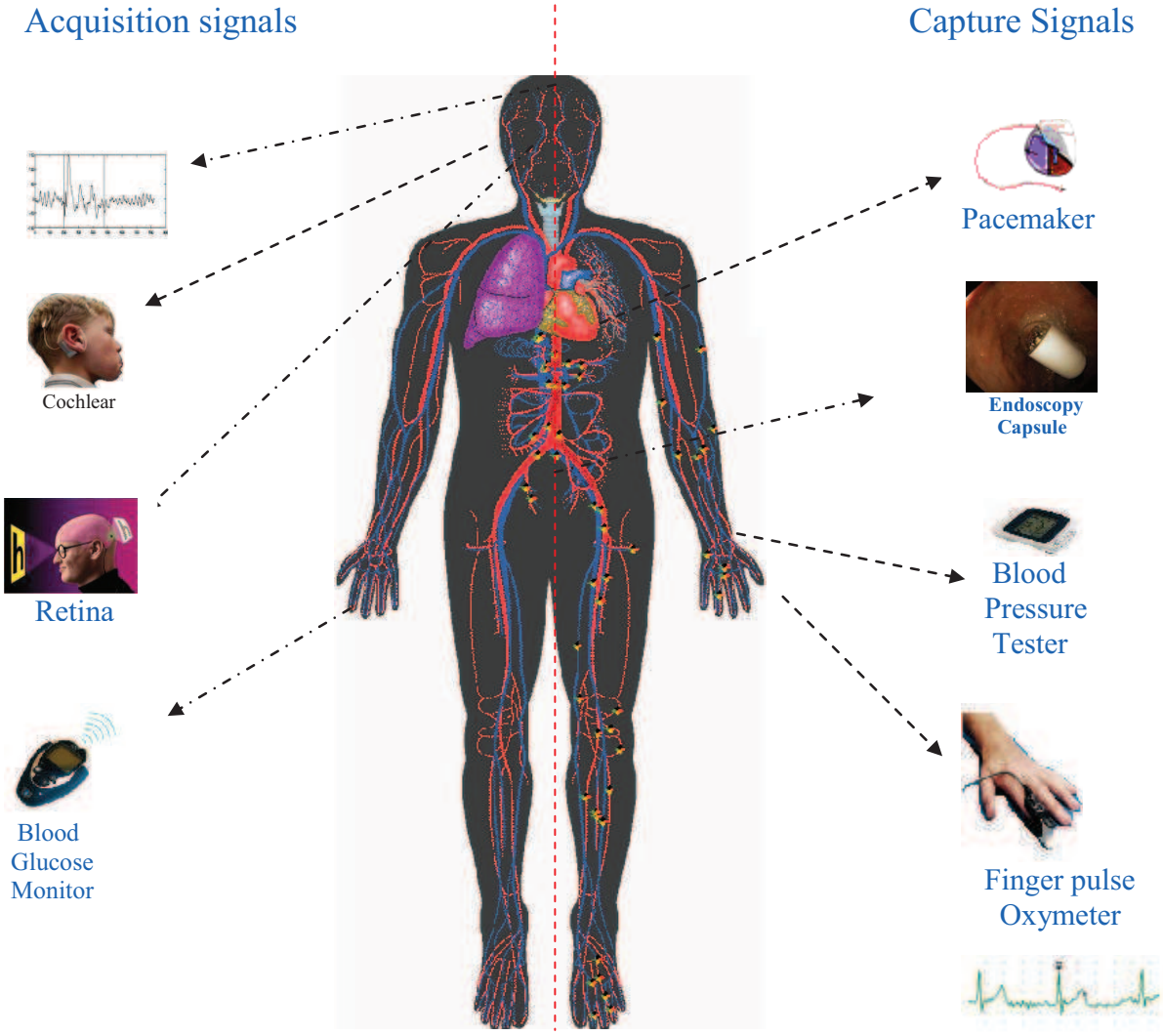


Figure (1.18) the acquisition and capture of signals from the body

1.7 Motivation of Thesis

The main challenges in biomedical devices are strictly for a higher transfer rate, and transmitting over wireless communication. This mainly needs an efficient system to hand over the information with minimum error; enhanced encoding of information is the key factor to protect the original data especially with data acquisition returned from the human body, converted into digital information. Furthermore, the amount of health care data is increasing. It is called "BIOSTEC" which includes Bio-signals, Bio-medical devices, and Bio-health. Mostly the recent and previous reports and research in this area have studied the behaviour of diseases of the human body, such as epilepsy, brain, nervous system disorder; focusing on improving the prosthesis or treatment for it. This work tries to study and investigate the problem of low data rate over a given spectrum bandwidth. The challenge for design of a modulator is to transfer a high data rate from the implantable wireless device into a reader unit, over a digital channel at industrial scientific medical (ISM) frequency band. In addition, we need to work with new technologies to design an efficient and optimum system, to improve the low data rate for conventional biodevice systems.

1.8 Thesis Organization

In this thesis we describe the current state of the research on a low power wireless telemetry system for medical applications. A study of existing biomedical device technologies and their key applications is presented. A brief assessment of future trends for wireless telemetry with a focus on emerging technologies with different digital modulation scheme techniques is given This thesis has been split into six chapters as:

- Chapter 1:

This chapter describes the general knowledge overview of the bio-telemetry and biomedical devices applied for medical applications. For example, implant telemetry, telemedicine, and healthcare, which describe the types of implantable sensors and acquisition signals data from the human body. Most of the researchers working in this area mention the behavioural diseases, specifically focusing on the transfer of data over wireless environment using inductive link

solutions. We summarise in detail the main design parameters for a wireless inductive coupling link for biodevices technology. In addition, these are demonstrated, described and concluded in figures, graphs and tables. Eventually, we try to clarify the applications of most biodevices working with wireless transfer data and the biomedical devices applications.

- Chapter 2:

This chapter focuses on analogue, digital wireless techniques for quadrature modulation, and coding the information signal. These are necessary as background for the digital modulator design in this thesis. We explore the basic principle of analogue and digital modulation categories, studying analysis mathematically and investigating different techniques. Methods which are commonly used for wireless applications may be suitable for biomedical implantable device purposes. The thesis also focuses on the appropriate modulation and demodulation techniques and the effect on power dissipation which includes the shared wireless received power with other parts in implant device, in a battery less system. Most of the common analogue and digital modulation schemes applied in biomedical devices, which are reported in many papers and journals, are reviewed, studied, and partially simulated. Summaries of the main modulation topologies appropriate for biomedical applications are the background of our work.

- Chapter 3:

The third chapter presents the background of our work, the challenges, and tries to classify in four sections that can be specified as: first section: inductive coupling link. Obviously, this describes the background of the inductive coupling link and the principle of the magnetic coupling, covering the mathematical calculation for maximum transfer power, and optimum coupling coefficient between reader and implant, synthesis of power amplifier for transmission over the inductive link. The second part generally reviews the power amplifiers and emphasizes the power requirement to transfer the magnetic flux. That presents the new synthesized design for hybrid power amplifier transmitter link for class E and F power amplifiers. The third part covers the wireless power investigation to provide the essential DC voltage for implant devices inside the human body.

Finally, the last part demonstrates the wireless system that transmission of the high data rate over a wireless inductive coupling link.

- Chapter 4:

The fourth chapter demonstrates our new work approach, which describes the main work for the proposed modulator. The VHDL programming code is used to generate n-PSK digital signals. A new simple design for BPSK, QPSK and 8PSK modulators architecture modulators is applied for implantable telemetry applications. The modelled modulator has been designed and simulated and performance was evaluated by measurements. The design has low power consumption and size for biomedical applications. Furthermore, the advantages of this modulator are that it can be reconfigured and upgraded to enhance the data rate.

- Chapter 5:

The fifth chapter concludes the hardware work in the thesis describing the complete system design. Generally, the work was classified in two main parts: reader units and implant device. The evaluation lab measurements were performed for each part of project, concluding with the hardware and the measurement results discussion.

- Chapter 6:

The last chapter concludes and summarises the completed hardware work in this thesis: simulation, measurements and results discussion. A simulation-based comparison of several basic control algorithms has been carried out for controlling a different magnetic technique. This achieves good performance with auto-control and moderate complexity. Finally, the work described in this thesis can be improved and extended in many ways as mentioned in the suggestions for Future Work.

• Publications

The following publications arising from this thesis work have resulted in posters and submitted publications.

A. Posters

1. Gihad Elamary, Graeme Chester, Jeff Neasham "**High Bandwidth Transcutaneous Wireless Telemetry"** The second event of the poster competition at North Umbria University (Supported by UK GRAND) UK on 03/05/ 2006.
2. Gihad Elamary, Graeme Chester, Jeff Neasham "**Implantable telemetry devices**" Newcastle University medical school poster competition on 05/05/2007
3. Gihad Elamary, Graeme Chester, Jeff Neasham"**Implantable Electronics telemetry Devices**" Graduate Poster Conferences Competition at Leeds University. (Supported by UK GRAND). 09/07/2007

B. Conference papers

1. Gihad Elamary, Graeme Chester, Jeff Neasham "**Experimental Digital BPSK Modulator Design with VHDL Code for Biodevices Applications**". Porto-Portugal,14/17.January.2009. BIOSTEC_Biodevices-2009.IEEE
2. Gihad Elamary, Graeme Chester, Jeff Neasham "**A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGAs for Biomedical Devices Applications**", London-UK 03/12/2009/ WCE_2009. ICEEE.
3. Gihad Elamary, Graeme Chester, Jeff Neasham "**An Analysis of Wireless Inductive for Higher Data Rate Biomedical Telemetry Using a New VHDL n-PSK Modulator**" 16th ICECS-2009-13th-16th/12/2009. IEEE

Chapter

2

Literature Review for Analogue and Digital Modulations Applied in Biomedical Applications

Background and Literature Review

Chapter II

2. Implantable Devices Modulation Schemes

BIODEVICES have increased rapidly in recent years; there has been a relentless push for a higher data rate and lower power consumption, augmented toward the wireless infrastructure environment. Principally, the gathered acquisition returned data from the body is defined as up-link, while the downlink provides the essential RF power signal and control information into the implant device. However, the modulator and demodulator are targeted for synthesis with low power consumption, and simplicity of circuits for implant devices [104] [136]. The magnetic field influence from a reader is modulated; subsequently a simple demodulator is use to detect the data at the implant part. The most common and simple modulator used is amplitude shift keying (ASK) [57] [65]. Typically, different RF schemes are applied for powering the implant downlink and back modulation from the body. Up-link techniques will be described in this chapter. In Figure (2.0), we demonstrate the most common analogue and digital modulation techniques applied for implantable communication that will be compared to our proposed VHDL-QPSK modulator design discussed in chapter four in detail.

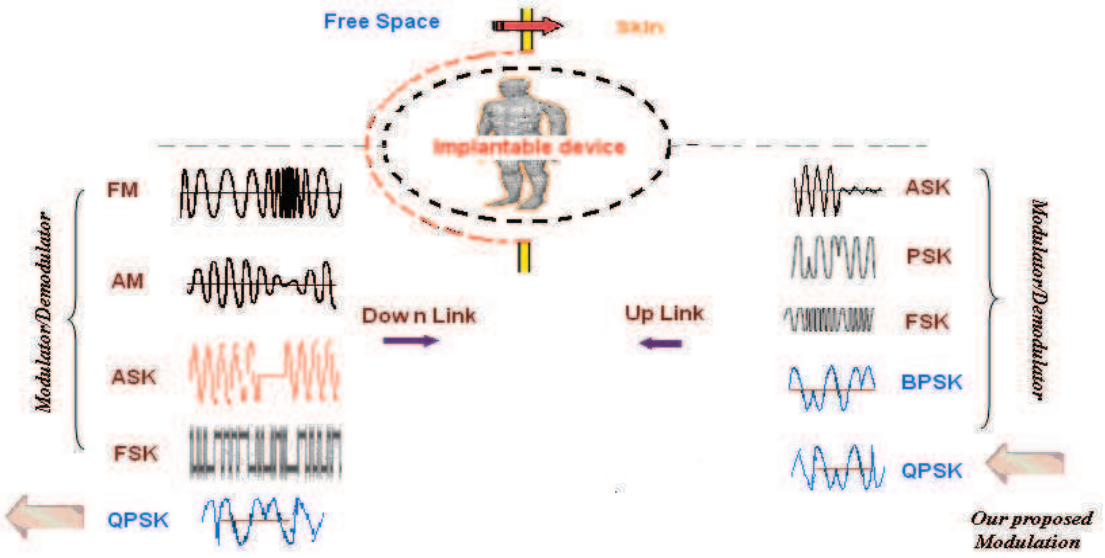


Figure (2.0) Modulation techniques applied to most biomedical devices

2.1 Analogue Modulation Background

2.1.1 Introduction To Analogue Modulation

Analogue modulation schemes are generally limited in biomedical applications. There are few reported papers implementing the analogue modulation such as amplitude modulation (AM), frequency modulation (FM) and pulse width modulation [115], [125]. The analogue schemes can be classified into two categories; the pulse shape modulation (PSM) and the pulse time modulation (PTM). The classification hierarchy of the most common analogue modulation formats applied in telecommunication coding is described in Figure (2.1). One of the simplest applications of this format is pulse amplitude modulation (PAM), in this technique the amplitude of individual, regularly spaced pulses is varied in accordance with the amplitude of modulating signal. Such a format is inefficient with bandwidth, and does not deliver the signal to noise ratio (S/N). On other hand, the demodulation of PWM is complicated at implant device applications [137] [184]. Practically, the ASK modulation is more suitable than FM and AM at implant device [190], which uses a simple demodulator for reproducing the data. The second goal for designing the ASK demodulator is to reduce the effect on the implant device performance since it is sharing the same source as wireless power [136]. Obviously, the conventional analogue modulation is not appropriate for the most of biomedical devices as large circuits are needed and this causes high power dissipation, which is the main disadvantage of this scheme.

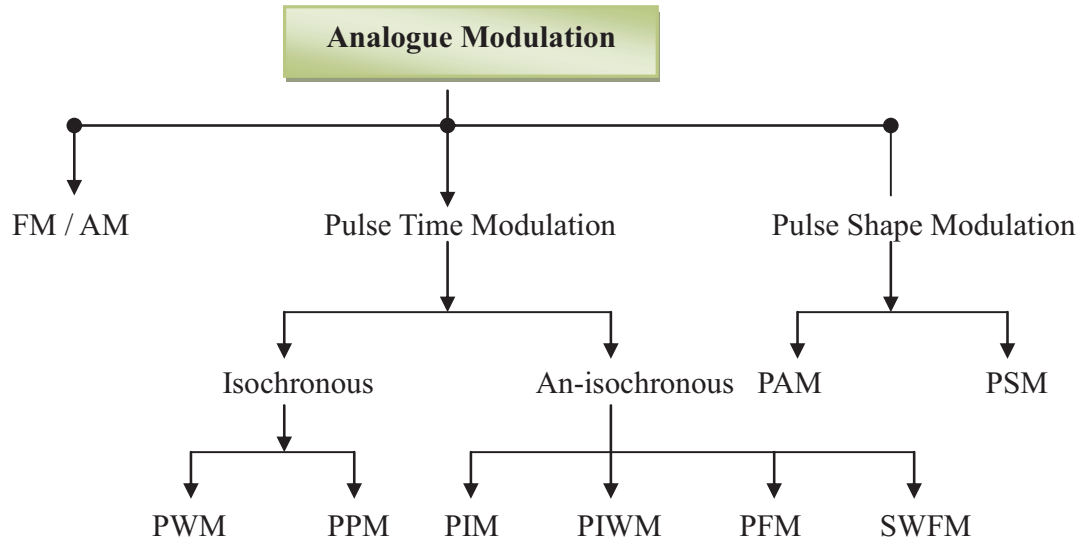


Figure (2.1) demonstration of the hierarchy of analogue modulations

2.2 Background of Principle Digital Modulations

2.2.1 Introduction to digital modulation

This section explains briefly the digital modulation techniques applied for biomedical devices. Generally, the transmissions of digital information are increasing at a rapid rate, which are used in several biomedical applications, to communicate between implant and reader. The most common modulation schemes are ASK, PSK, BPSK and QPSK employed in near field communication or satellite telemetry, RFID and commercial smart cards [1] [184]. Typically, there are other digital modulators, which not discussed in this thesis [9] [27] [216]. However, we describe in Figure (2.2) the classification hierarchy of the most common digital modulation formats [199], and investigate most of the common digital modulations, which are appropriate for medical application in this work. We are considering the simple implementation circuit, in reader unit or at implant devices, and these are analyzed and simulated where used to design a digital modulator that is suitable for medical purposes. However, in this thesis we choose pulse shape modulation techniques and selected the QPSK modulation as more appropriate to implement within digital hardware.

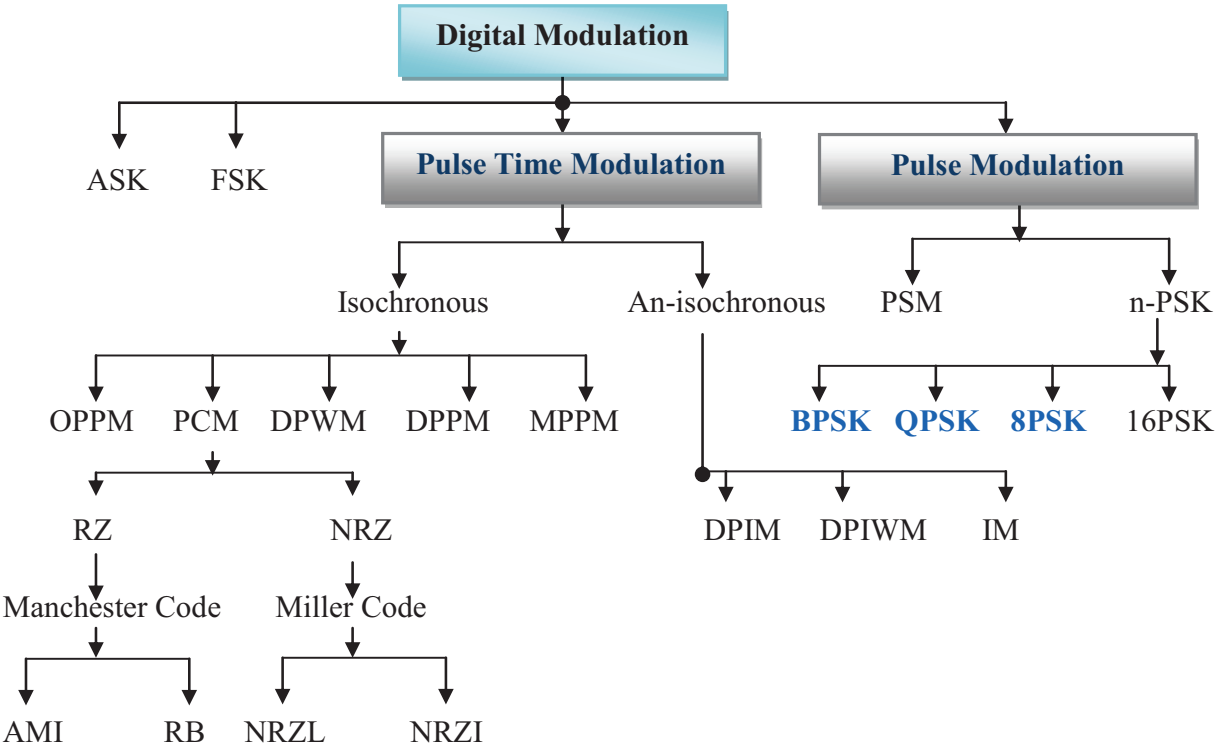


Figure (2.2) demonstration of the hierarchy of the most common digital modulation schemes

2.2.2 ASK Modulation Background

One of the simplest digital modulations is amplitude shift keying (ASK) or OOk (On/Off keying); these are commonly employed in wireless systems such RFID and biomedical device applications. It is a simple modulation and demodulation scheme with simple hardware implementation, known as one-dimensional modulation, where no carrier is presented during the transmission time. This conserves the power consumption of the modulator [65] [104]. The principle of ASK transmission is shown in Figure (2.3) and the constellation diagram is depicted in Figure (2.4) [10]. The mathematical expression for ASK modulation is presented in equations (2.0) and (2.1) respectively, where b(t) is defined the binary message and c(t) defined the carrier signal E_b represents the bit energy and the T_b is defined by the bit duration.

$$S_{ASK}(t) = b(t) \times c(t) \tag{2.0}$$

$$\text{Where } b(t) = \begin{cases} \sqrt{E_b} & binary\ 1 \\ 0 & binary\ 0 \end{cases} \quad \text{and} \quad c(t) = \sqrt{\frac{2E_b}{T_b}} \cos(\omega_c t)$$

$$S_{ASK} = \sqrt{\frac{2E_b}{T}} \cos(\omega_c t) \tag{2.1}$$

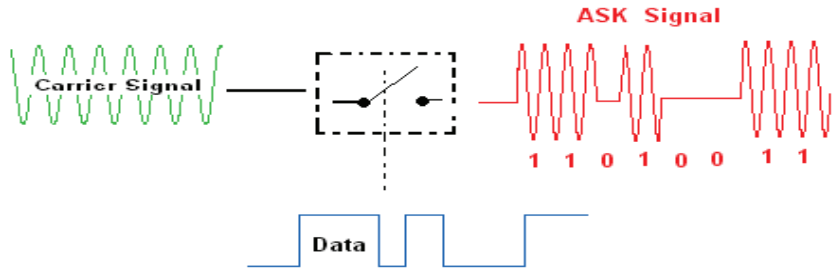


Figure (2.3) Principle of ASK modulation

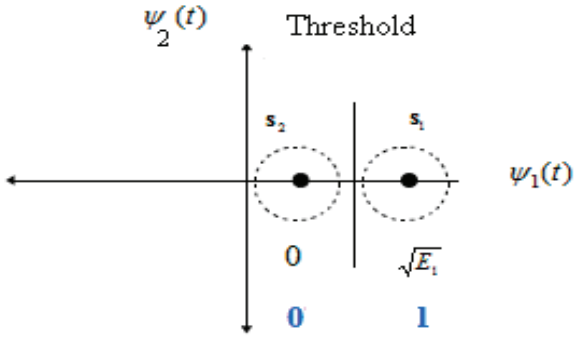


Figure (2.4) Constellation diagram of ASK signal

The spectrum of an ASK signal is shown in Figure (2.5) which demonstrate the upper side band (USB) and lower side band (LSB) of the transmitter signal.

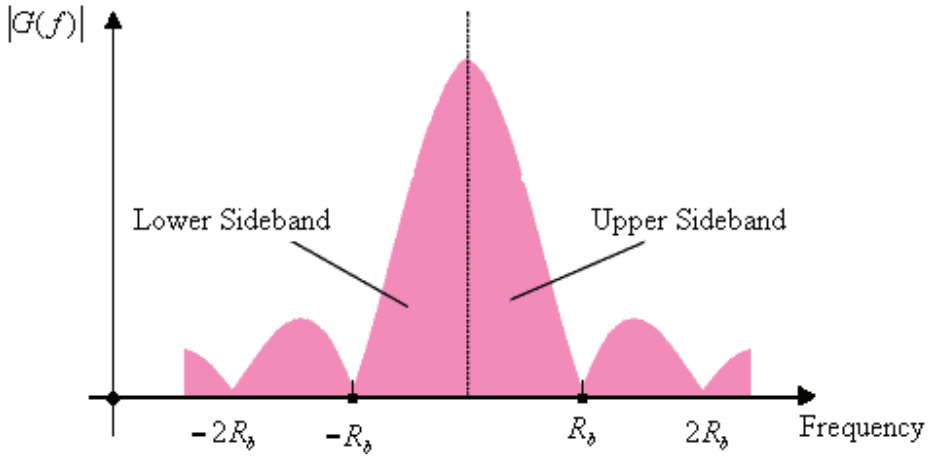


Figure (2.5) Spectrum of the ASK signal

The second method for generating an ASK signal is by changing the modulation depth which is expressed by [(A-B)/ (A+B)*100%] as shown in Figure (2.6), where **A**, **B** represents the maximum and minimum amplitudes of modulated signal waveform. The Fourier series coefficients of pulse signal with amplitude of (**a**) and duty ratio of ***D*** given by the function is even so the (**b**) coefficients are all zero [28] [39] and [40], whereas the Fourier coefficient of the fundamental frequency is a function of duty ratio ***D***. From this ratio we can control the duty and control ASK depth by modifying the pulse duration ***K*** as shown in Figure (2.7) where the duty ratio is (D = K/T). For example, the ASK modulator can be designed at 10% of modulation depth by having fixed carrier signal amplitude that provides stable power transfer and independent data modulation; this is suitable to provide constant RF signal into an implant device. These advantages give high readability for DC voltage at different distances from the reader coil at the implant part. Compared with other demodulators such as AM and FSK or FM, the ASK demodulator is practically a more simple design for implant parts. However, if we are considering this modulation for implant design, the ASK modulation suffers from a low data transmission rate. Consequently, that is not appropriate for this work as an up-link modulator for implant parts. ASK is also most susceptible to the effects of non-linear devices, which may compress and distort the signal amplitude. Typically, to avoid such distortion the system must operate in the linear range away from the point of maximum power.

where most of the non-linear devices behaviour occurs.

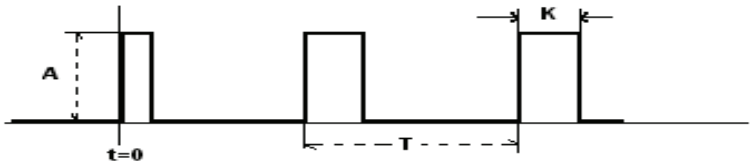


Figure (2. 6) the pulse controlling in the modulation depth

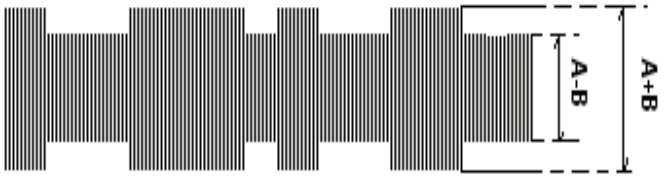


Figure (2.7) the ASK modulation depth

2.2.3 ASK Demodulation Technique

The demodulator technique in biodevices is still a challenge with the implant devices, for ultra low power circuit operation [113] [116] [158]. Principally, the ASK received signal is demodulated by an envelope detector after a tuned circuit at resonant frequency, the demodulated signal then passes through a LPF. Due to high input signal at short range, typically a few centimeters, there is no need for an amplifier as a simple Schmitt-trigger is able to provide and shape the output of the demodulator, and buffered [57]. The block diagram of common ASK demodulator is presented in Figure (2.8). The ASK demodulator will be discussed further in detail in chapter (5).

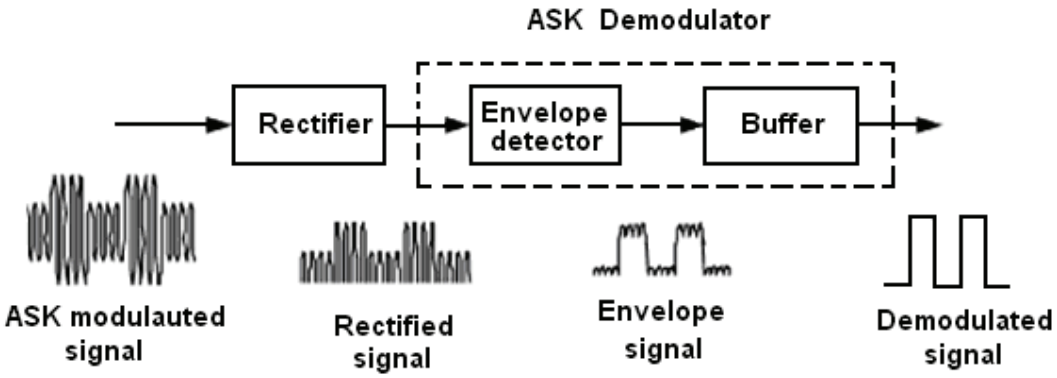


Figure (2.8) the block diagram of ASK demodulator [57]

2.3 Principle of n-PSK Modulation

2.3.1 Binary Phase Shift Keying (BPSK)

This chapter reviewed how different types of digital modulation schemes are in use in wireless communication for the biomedical modulation techniques in our work studied. The most common digital schemes appropriate in biomedical transmission are briefly described such as: PSK, BPSK and QPSK [54], [102]. However, it is an important challenge to transmit and read the data from/to exterior world body with minimum noise. Typically, numerous different types of modulations are applied for transmitting signals using either analogue or digital modulation. The power consumption is a very important factor in a battery-less system. In practice, the modulator is the critical part of the design in most biomedical device that could reduce the implant performance. The first simple digital modulation scheme is the binary phase shift keying (BPSK), which offers a practical circuit implementation. The carrier shifted by influence the input binary data for transmitting 1-bit, which dose not change the phase carrier $\sin(\omega_c t)$, while there is change for the carrier phase by $-\sin(\omega_c t)$ for 0-bit. However, the BPSK is only able to modulate 1-bit/symbol, which may not give high enough data rate, where the bandwidth (BW) is limited [10], [27]. Conceptually, in digital communication, the information signals are usually binary data, which needs to be converted in to a NRZ signal for encoding the data, and the carrier is continuous wave (CW) sinusoidal signal. The principle of the BPSK Tx–modulator is demonstrated in Figure (2.9); it includes a filter for output signal for harmonic suppression.

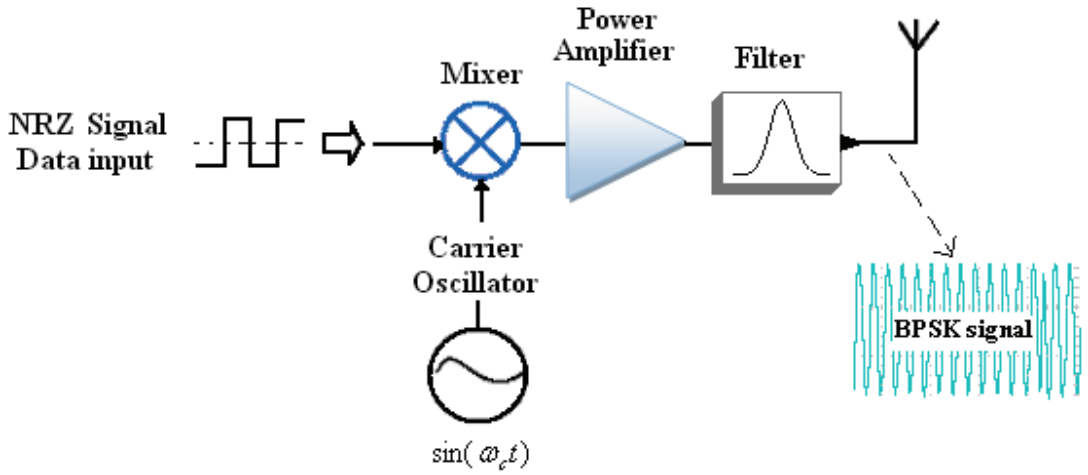


Figure (2.9) the block diagram of the BPSK modulator

The binary data selects one of the two opposite phases of the carrier; the carrier signal is shifted by the input data information. The result of this process is to provide a BPSK signal, which is illustrated in Figure (2.10). Graphically, this can be represented by two dots on the constellation diagram [53] [73].

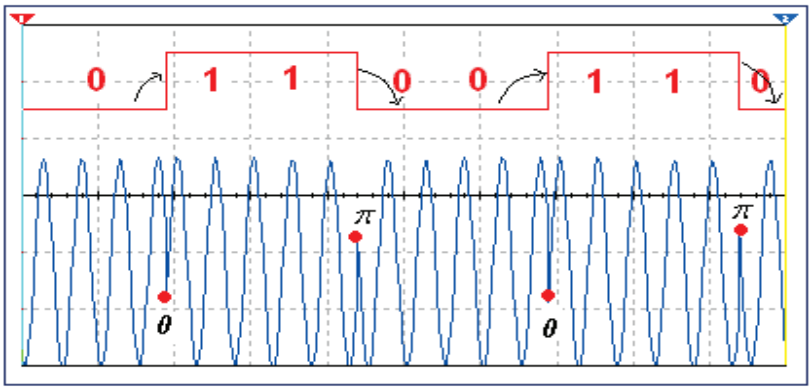


Figure (2.10) the BPSK waveform with respect to binary state

The result of this modulated BPSK signal can be expressed mathematically in equation (2.2); where the phase shift $\theta(t)$ is given by $\theta(t) = i\pi$, with $i = 0$ or 1 represents the input bit. The binary input data *m (t)* represents the input stream of data with a value of $-A_{RF}$ for logic (0) and $+A_{RF}$ for logic (1).

$$S_{BPSK}(t) = m(t)\sqrt{\frac{2E_b}{T_b}}\cos(\omega_c t + \phi) \tag{2.2}$$

There is a wide *sinc* response in the frequency domain around the carrier frequency. The power spectral density for BPSK signal can be mathematically expressed in the equation (2.3) [54]:

$$S_{BPSK}(\omega) = \frac{A_{Rf}^2 T_{bit}}{4}\frac{\sin^2[(\omega+\omega_c)T_{bit}/2]}{[(\omega+\omega_c)T_{bit}/2]^2} + \frac{A_{Rf}^2 T_{bit}}{4}\frac{\sin^2[(\omega-\omega_c)T_{bit}/2]}{[(\omega-\omega_c)T_{bit}/2]^2} \tag{2.3}$$

The spectrums of the transmitted BPSK signal is shown in Figure (2.12), where the T_{bit} is the bit period, and the width of the main lobe, referred to as the null-to-null bandwidth is found to be twice the bit rate R_b:

$$BW_{BPSK} = 2R_b = \frac{2}{T_b} \tag{2.4}$$

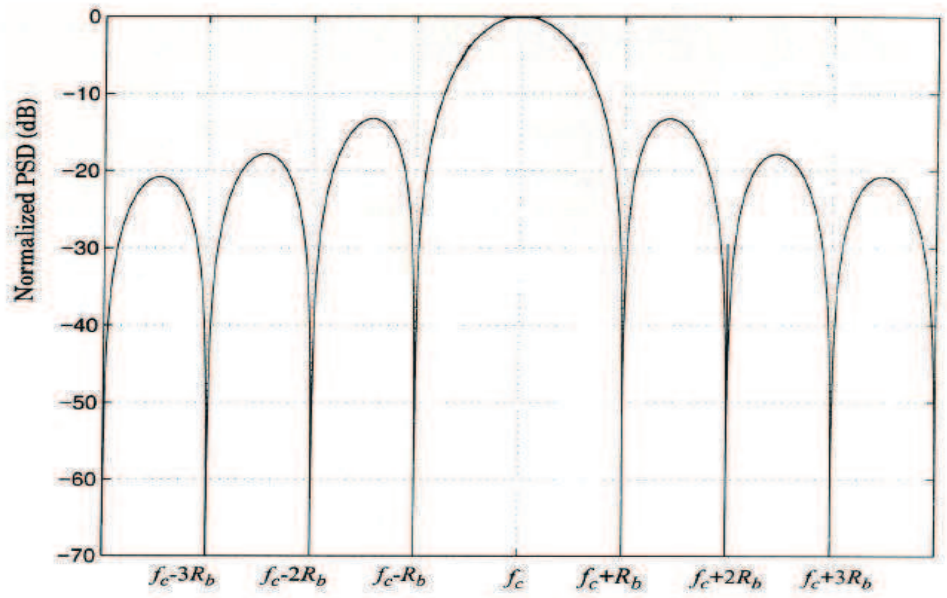


Figure (2.11) Spectrum for the BPSK Signal

2.3.2 Demodulator For BPSK

There are many BPSK demodulation methods and techniques such as the Costas loop, re-modulation or inverse modulation, multiply filter divide method, square loop and pulse detection [63], [99]. We describe the most popular and simple techniques for demodulating the BPSK, the classic type is the Costas loop demodulator, which is widely used in wireless communication and is described in Figure (2.12). The system involves two parallel tracking loops operating simultaneously from the same VCO (Voltage-Controlled Oscillator) The first loop is the in-phase loop I , and the second, called the quadrature loop Q uses a 90 degree shifted VCO. The result of Q and I multiplier outputs are filtered by single pole Butterworth low pass filters. Then, Q and I filter output are multiplied together and the product is scaled and filtered to produce the loop error used to control the VCO. The loop error should settle to a value when the loop is locked. A negative loop error decreases the VCO increment resulting in a lower VCO frequency, and similarly a positive loop error increases the VCO increment resulting in a higher VCO frequency [51]. The second method of BPSK demodulation is the coherent receiver using an anti-parallel

synchronization loop [51] [110]. There are many techniques in this method, which have been described and one of these techniques is for demodulating the BPSK received signal. The block diagram of anti-parallel synchronization loop circuit is shown in Figure (2.13). It contains a dual loop with a 180° phase shifter in the lower loop. The phase detectors used for this anti parallel loop utilize two multiplier type detectors, and a DC offset V_{dc} at each detector. These DC offsets are introduced using two voltage summers, which play an important role for the operation of these anti-parallel loops followed by two switches, an inverter and a comparator, as a control circuit [60],[74].

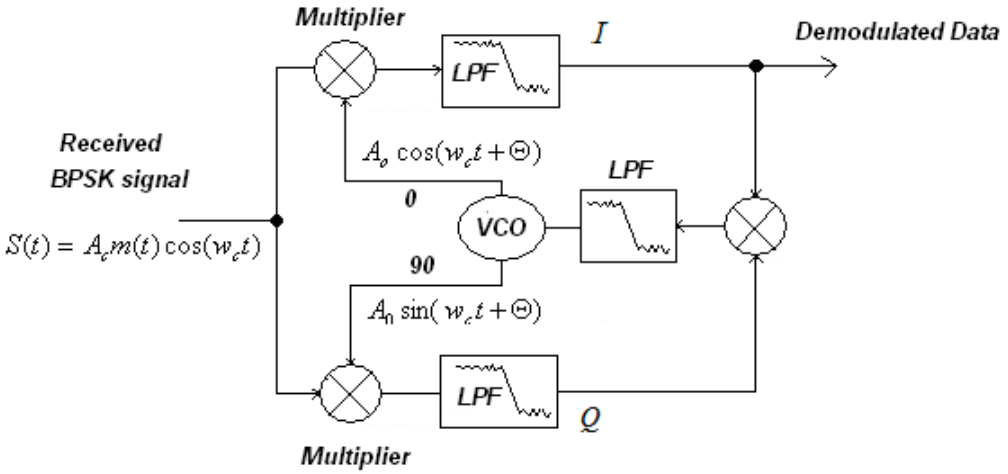


Figure (2.12) the Costas loop demodulator for BPSK

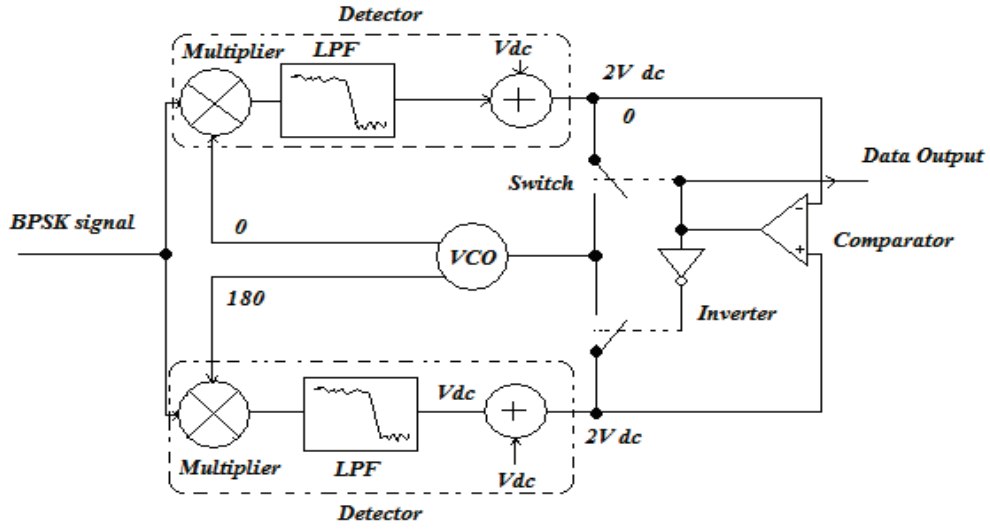


Figure (2.13) the Anti-parallel synchronization loop demodulator for BPSK

Different topologies have been used to improve the bit error rate (BER) at the receiver, which indicates the demodulator performance with respect to signal noise-to-ratio. In BPSK the phase of the constant amplitude signal is switched between two values due to two possible data signals S1 and S2 corresponding to binary 1 and 0 respectively; typically, the transition phase is 180°. Mathematically the average probability of symbol error can calculate the analytical probability of detector error for BPSK demodulation at ($R_e = R_b / 2$) is given in equation (2.5).

$$P_e = \tfrac{1}{2} erfc\left(\sqrt{\frac{E_b}{N_0}}\right) \tag{2.5}$$

E_b is the energy per bit for BPSK symbol rate one bit, N_0 is the noise power spectral density, and the complementary error function (erf) is defined by:

$$erf(x) = \tfrac{2}{\sqrt{\pi}} \int_0^x e^{-x^2} dx \tag{2.6}$$

$$erfc(x) = 1 - erf(x) \tag{2.7}$$

Hence, the BPSK has double the (E_b / N_0) for BFSK signal, this is obvious when comparing the bandwidth of BPSK with respect to BFSK. The BFSK requires twice the bandwidth of BPSK for the same data rate. This means that the probability of false decision in the BFSK is double its BPSK counterpart [89]. The bandwidth increases with the increase in the number of bits per symbol; this affect the efficiency of the demodulator. The channel bandwidth required to pass M-array PSK signals is expressed in equation (2.8).

$$B_{BPSK} = \frac{2}{T_b} \tag{2.8}$$

T_b is the symbol duration that is related to bit duration by $R_b = 1/T_b$, substituting this in equation (2.9) gives:

$$B_{BPSK} = \frac{2R_b}{\log_2 M} \tag{2.9}$$

$$\therefore \quad \eta_B = \frac{R_b}{B} \qquad bits / Hz \tag{2.10}$$

where the η_B *defines the bandwidth efficiency*

we substitute equation (2.9) in the equation (2.10) which yields:

$$\eta_B = \frac{\log_2 M}{2} \tag{2.11}$$

2.3.3 Quadrature Phase Shift Keying (QPSK)

The efficiency and bandwidth in the wireless communication are mainly important and the quadrature carrier multiplexing system has been proven to be effective for this purpose in such systems [66] [56]. The QPSK modulation is a 4-ary PSK signal, the phase carrier acquires four discrete states (45º, 135º, 225º, 315º) or (0º, 90º, 180º, 270º) as shown in Figure (2.14), which correspond to a pair of message bits. The symbol period is twice the bit period $T_s = 2T_b$; it is used for increasing the bandwidth and the spectrum efficiency. The binary data stream is divided into two separate streams in two-dimensional phase (I-phase), and (Q-quadrature). The RF signal can be represented in polar coordinates by magnitude and phase, in digital radio terminology, X is represented by ***I*** and Y replaced by ***Q***. The (±90 º) degree shifter generates the quadrature signals; that yield the transition with respect to the input binary data as shown in Figure (2.15).

$$S(\omega_c t)_{QPSK} = \begin{bmatrix} \frac{A_c}{\sqrt{2}}\cos(\omega_c t) & + \frac{A_c}{\sqrt{2}}\sin(\omega_c t) & 00 & 45^0 \\ -\frac{A_c}{\sqrt{2}}\cos(\omega_c t) & + \frac{A_c}{\sqrt{2}}\sin(\omega_c t) & 01 & 135^0 \\ -\frac{A}{\sqrt{2}}\cos(\omega_c t) & - \frac{A_c}{\sqrt{2}}\sin(\omega_c t) & 10 & 225^0 \\ \frac{A_c}{\sqrt{2}}\cos(\omega_c t) & - \frac{A_c}{\sqrt{2}}\sin(\omega_c t) & 11 & 315^0 \end{bmatrix}$$

Figure (2.14) the transition with respect to binary data states for RF QPSK signal

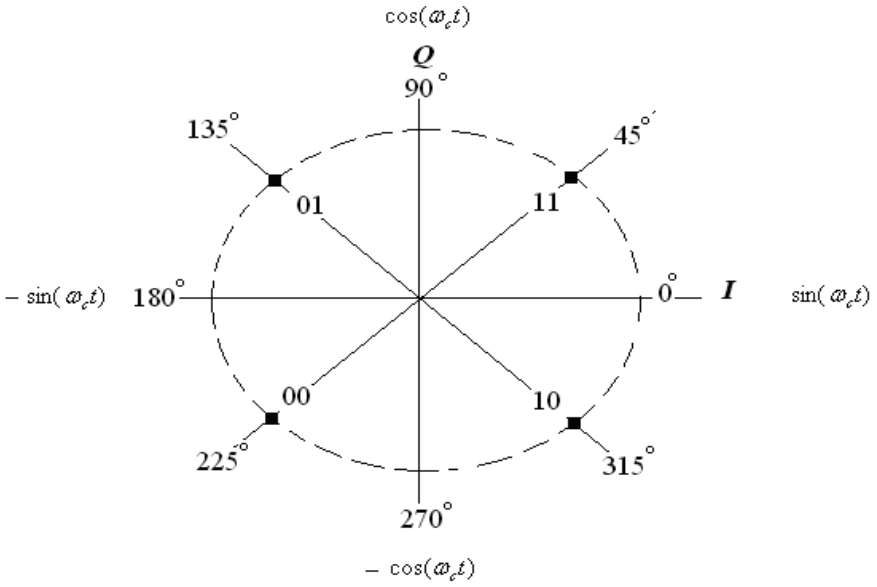


Figure (2.15) Constellation diagram of QPSK signal

All analogue or hybrid analogue/digital QPSK modulators work with the carrier phase shift angle (φ) as a key of modulation. The phase shifter is the most important part in the modulator to acquire two discrete signals $\sin(\omega_c t)$ and $\cos(\omega_c t)$ [172]. However, the NRZ format is essential for mapping (***I***) and ***(Q)***, the analogue QPSK signal can be represented mathematically in the equation (2.12). The transition of the RF carrier signal is influenced by the binary input data is depicted in Figure (2.16). Practically, it uses a Direct Digital Synthesizer DDS [23] [182] or a Numerical Control Oscillator to perform the carrier transitions [55] [166].

$$S_{QPSK}(t) = \sqrt{\frac{2E_s}{T_s}}[\cos(\omega_c t + (i-1)\tfrac{\pi}{2}] \qquad (0 \le t \le T_s \text{ , i =1, 2, 3, 4}) \tag{2.12}$$

by using the trigonometric identity equation (2.12) can be rewritten for the interval $0 \le t \le T_s$ as defined in equation (2.13), where (***I***) and (***Q***)are expressed in equations (2, 14) and (2.15):

$$S_{QPSK}(t) = \sqrt{\frac{2E_s}{T_s}}[\cos(\omega_c t + (i-1)\tfrac{\pi}{2}]\cos(\omega_c t) - \sqrt{\frac{2E_s}{T_s}}\sin[(i-1)\tfrac{\pi}{2}]\sin(\omega_c t) \tag{2.13}$$

$$I(t) = \sqrt{\tfrac{2E_s}{T_s}}\cos[(2i-1)\pi/4] \tag{2.14}$$

$$Q(t) = \sqrt{\tfrac{2E_s}{T_s}}\sin[(2i-1)\pi/4] \tag{2.15}$$

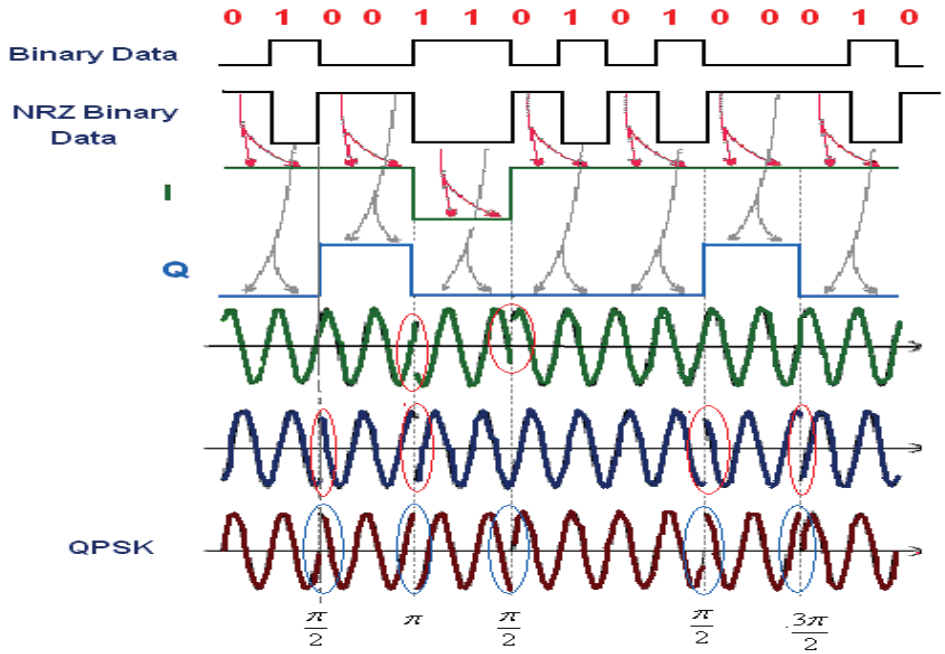


Figure (2.16) illustrates the QPSK waveform with respect to binary and NRZ states

The typical analogue QPSK modulator that generates a QPSK analogue signal is demonstrated in Figure (2.17).

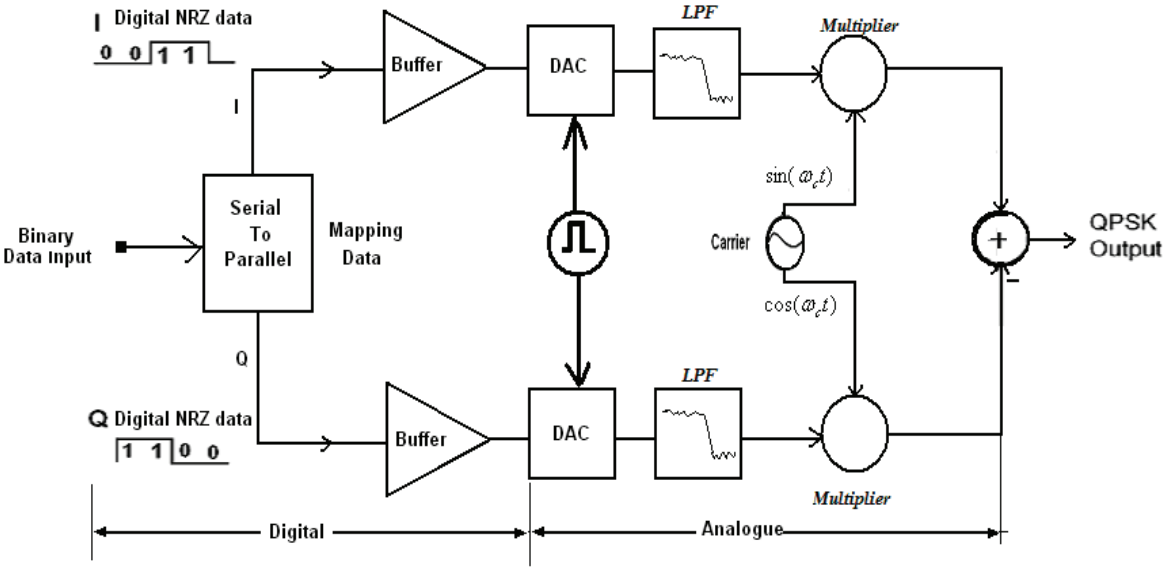


Figure (2.17) the block diagram of conventional QPSK modulator

Obviously, the bandwidth of QPSK signal is shown in Figure (2.18), only half ($R_b/2$) of the BPSK for the same data rate as compared between them. The signal of QPSK has closer points to each other as illustrated in the constellation diagram in Figure (2.15). However, this causes it to increase the probability of error with respect to data and noise, which adversely affects the modulation quality [129] [131]. The advantage of QPSK modulation is that the carrier-suppressed modulation decreases the spectral energy density, because the carrier energy is not in the frequency spectrum that makes it difficult for the receiver to recover it. It can be seen that most of the QPSK signal energy transmitted and the carrier is null (suppressed carrier) thus saving most of the energy of the carrier as shown in Figure (2.19).

$$S_{QPSK}(BW) = \frac{A_b^2 T_b}{2}\frac{\sin^2[(\omega+\omega_c)T_b]}{[(\omega+\omega_c)T_b]^2} + \frac{A_b^2 T_b}{2}\frac{\sin^2[(\omega-\omega_c)T_b]}{[(\omega-\omega_c)T_b]^2} \tag{2.16}$$

The bandwidth of the main lobe for the bit rate R_b and T_b is the bit period, in equation (2.17):

$$BW_{QPSK} = 2\left(\frac{R_b}{2}\right) = R_b = \frac{1}{T_b} \tag{2.17}$$

Therefore, the QPSK requires only half of the bandwidth of the BPSK for the same data rate. In addition, the adjacent points in the signal constellation diagram for QPSK are a smaller distance apart compared to BPSK, which increases the probability of error in the presence of noise, which may affect the modulator quality. However, the symbol energy (E_s) in QPSK is given in equation (2.18):

$$E_S = \frac{A_b^{\,2}}{2}(2T_b) = A_b^{\,2}T_b \tag{2.18}$$

Furthermore, the technique can also be extended to higher modulation level such as 8-PSK. The phase shift for the carrier has eight possible states, (45º) in I/Q plane, and each symbol is composed of 3 bits as shown in Figure (2.19). In 8-quadrature amplitude modulation (QAM), there are 8 phases in the ***I*** and ***Q*** plane. It can extend to more modulation levels for example 16-QAM up to 256QAM both the phase and amplitude of the transmit carrier are varied [95], [111] and [32]. That means the separation between phase states becomes smaller and increases susceptibility to noise.

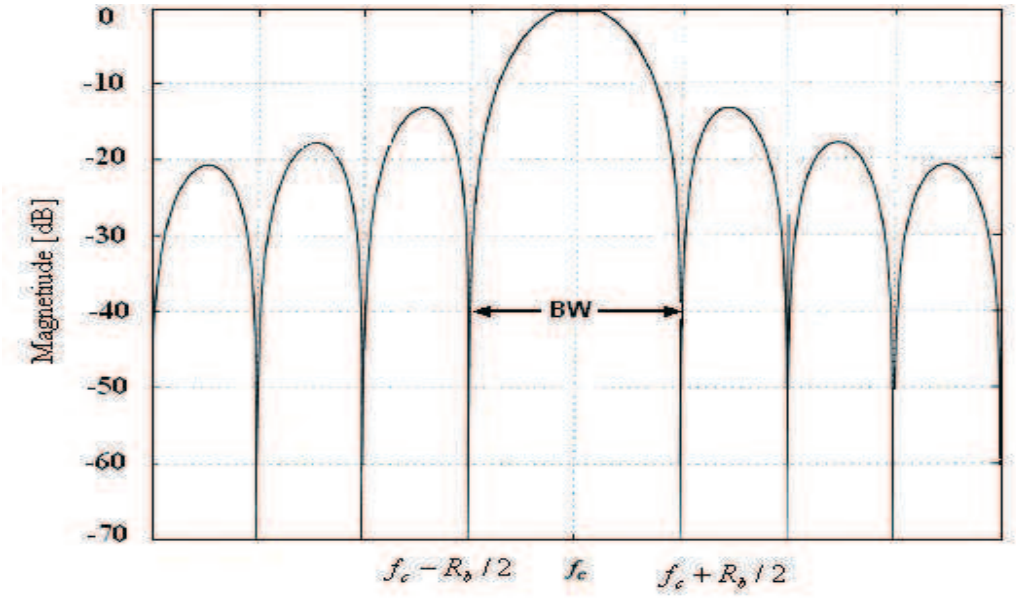


Figure (2.18) the Spectrum density for QPSK Signal

However, we describe M-PSK modulation, which is appropriate for our application for biodevices topology. The 8PSK is usually the highest order PSK constellation used, with more than 8 phases, the error-rate becomes too high and there are better, though more complex, modulations available such as quadrature amplitude modulation. Although any number of phases may be used, the fact that the constellation must usually deal with binary data means that the number of symbols is usually a power of two.

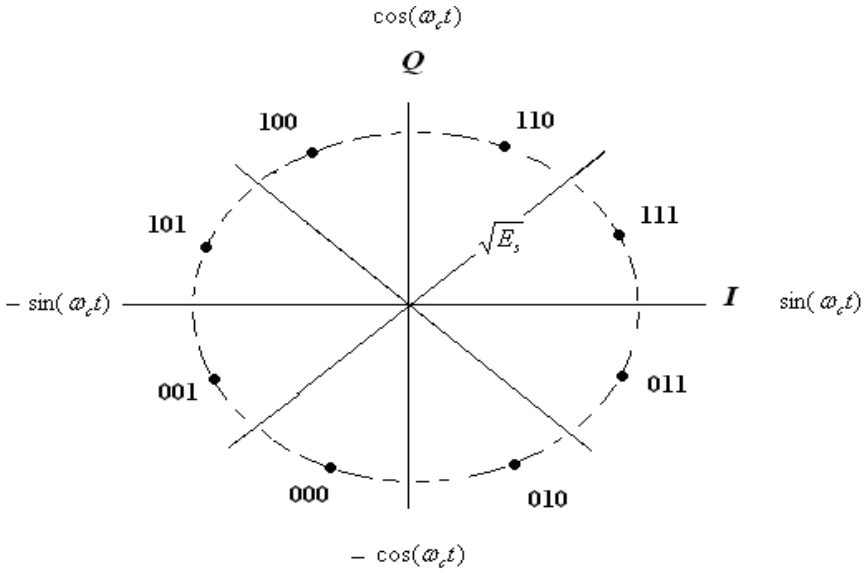


Figure (2.19) the constellation diagram for 8-PSK

2.3.4 Demodulation of QPSK

The demodulation techniques for QPSK are similar to BPSK demodulation as they are modified by the Costas loop [129]. The most popular and simple techniques for demodulating the QPSK can be described as; the Costas loop, re-modulation, and multiply filter divide method. While the re-modulation is stochastically equivalent to the hard limited Costas loop, the multiply filter divider method is always used in high data rate. However, many applications use the Costas loop, which may extend to lock onto a modulated QPSK signal with modifying the hardware-limited signal as shown in Figure (2.20). The two low pass filters in the I /Q branches of the QPSK demodulator are followed by a limiter, which directly changes the filter output voltages to the highest level or lowest when there is a phase error. Provided that two independent binary data x (t) and y (t) modulate two orthogonal components of the carrier, where x (t) and y (t) have the values of (+1) or (-1) representing binary one or zero respectively. Practically, there are modern digital demodulators, which offer more reliability and simple design for either BPSK, or QPSK demodulators [118], [129].

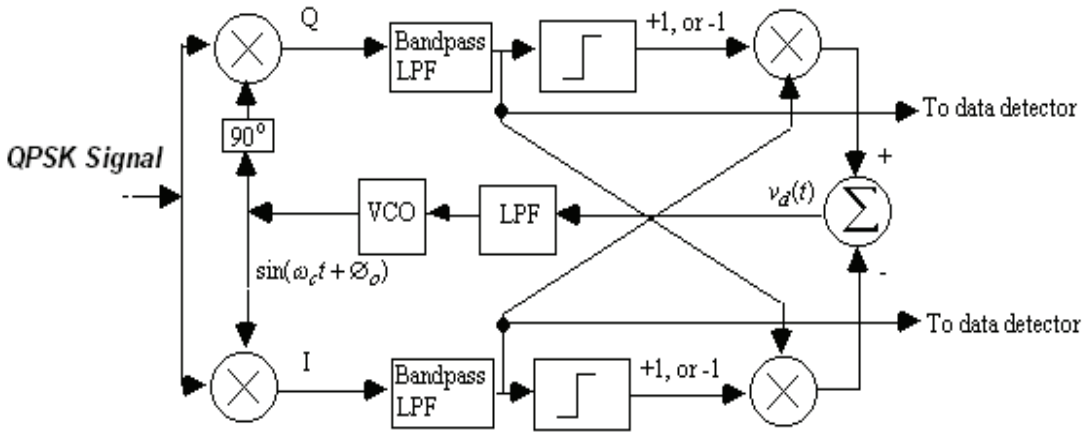


Figure (2.20) the block diagram of the QPSK demodulator

However, the main important factor for demodulator is measuring the BER typically to evaluate the demodulator performance efficiency and reliability. In order to achieve the same bit-error probability as BPSK the QPSK uses twice the power, since two bits are transmitted simultaneously, the MATLAB simulation, which compares BER between the BPSK and QPSK as shown in Figure (2.21).

Hence, the symbol error probability for QPSK can mathematically be expressed in equation (2.19), where (P_b) is the bit error rate and (Q) represents the complementary error function the [32], [95] as:

$$P_e = 1-(1-P_b)^2 \tag{2.19}$$

$$\because \quad P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right)$$

$$P_b = 2Q\left(\sqrt{\frac{E_b}{N_0}}\right) - Q^2\left(\sqrt{\frac{E_s}{N_0}}\right) \tag{2.20}$$

The probability of the symbol error for QPSK can be approximated as:

$$P_b \approx 2Q\left(\sqrt{\frac{E_b}{N_0}}\right) \tag{2.21}$$

- **Power Efficiency for M-array:**

The power efficiency of M-array signal can be mathematically estimated, defined as power efficiency (η_p) [9], [27]. In particular, it compares the nearest neighbours' approximation as in equation (2.22), where the analogue of M-array signal can defined as power efficiency as in equation (2.23).

$$P_e = N_{d_{\min}} Q\left(\frac{d_{\min}}{2\sigma}\right) \tag{2.22}$$

$$\eta_p = \frac{d_{\min}^2}{E_b} \tag{2.23}$$

We can rewrite the equation (2.22) which gave the nearest neighbours approximation as expressed in equation (2.24):

$$P_e = N_{d_{\min}} Q\left(\sqrt{\frac{\eta_p E_b}{2N_o}}\right) \tag{2.24}$$

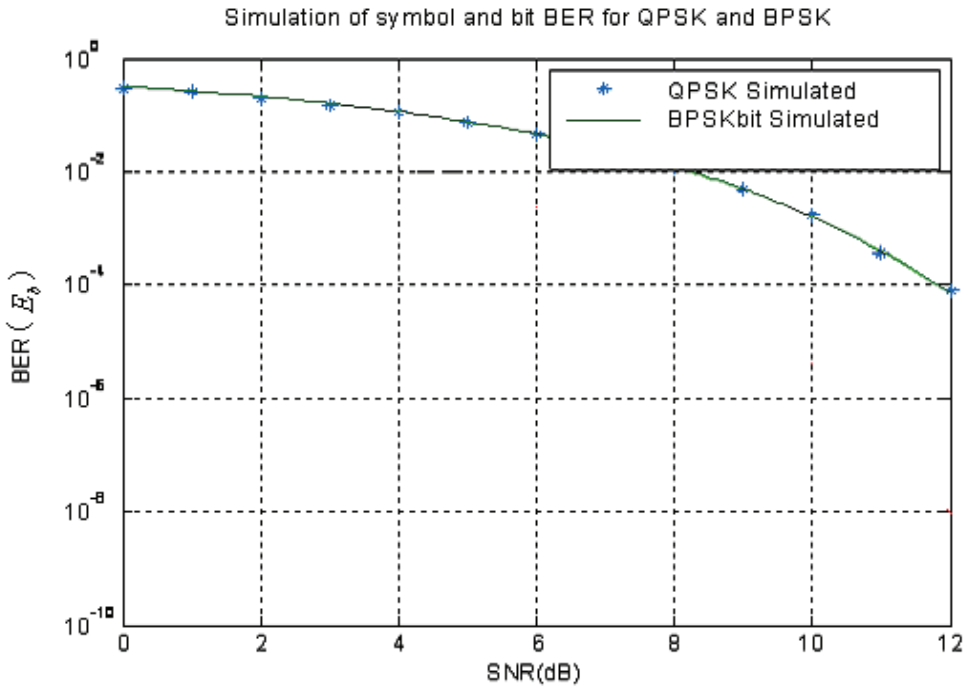


Figure (2.21) Simulation for the BER comparing between BPSK and QPSK

2.4 Quadrature Signals Generation Techniques

There are several techniques for generating the desired phase shifter with different circuit topologies, to generate sine and cosine with 90^0 shift. In this section, the most common circuits and phase generators in wireless techniques will be briefly described with their characteristics, advantages and limitations. Typically as background for our proposed digital modulator, we investigate the appropriate alternative topology applied for biodevice applications.

2.4.1 Direct Digital Synthesizer (DDS)

Direct Digital Synthesizer "DDS" performs the same function as a numerical controlled oscillator (NCO) [55]; basically it is a technique using digital data and mixed with analogue signal, it is used especially for a precise fast frequency and phase tunable output [189] [83]. It generates signals at different phase carriers waves one ($\sin(\omega t)$) or ($\cos(\omega t)$) [23] as shown in Figure (2.22), the architecture block diagram of DDS. The phase is calculated between increment points (memory location) skipping technique and a constant interpolation of the stored signal, which runs at a constant update clock rate as the increment phase points (number of sampling per

waveform cycles), and the output frequency is increased, as shown Figure (2.23). However, the DDS is easily reconfigurable to change the channel spacing and bandwidth, and allows the implementation of several digital schemes.

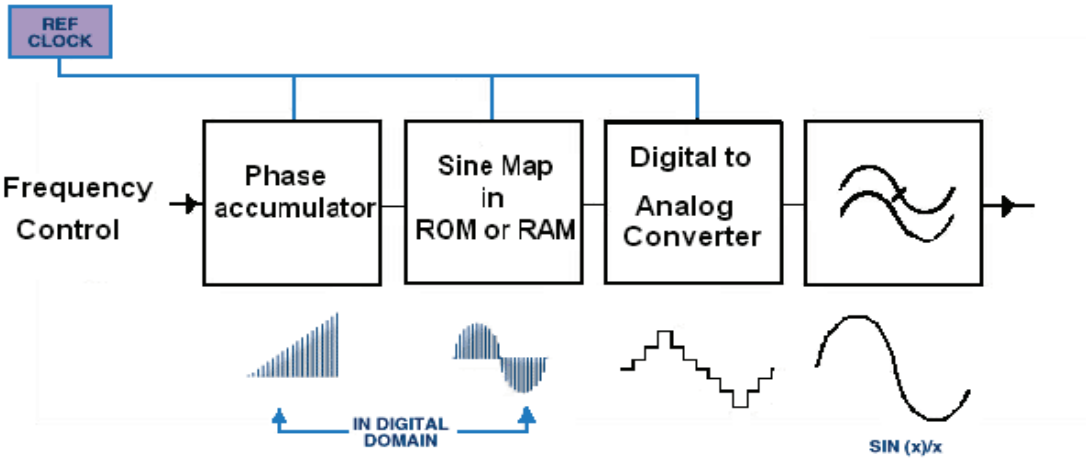


Figure (2.22) the architecture of DDS Block diagram

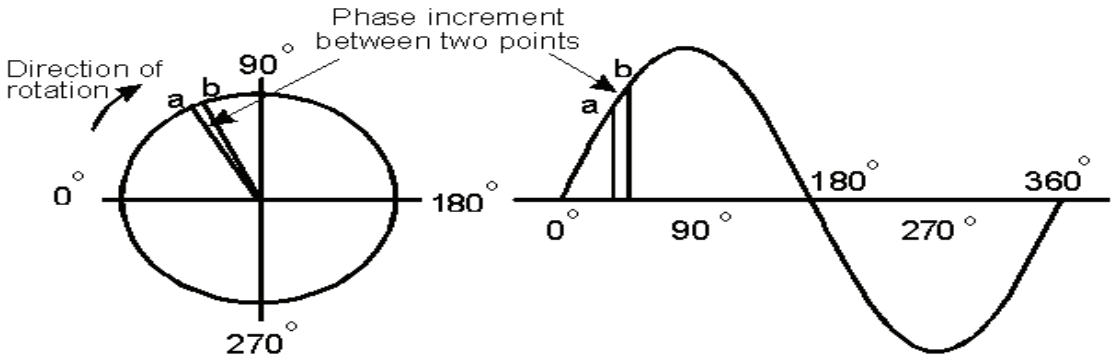


Figure (2.23) the Phase changing diagram

2.4.2 PLL Using Voltage Control Oscillator

Phased lock loops (PLL) have been used either in analog or digital implementations [191]. Synthesized for digital applications and data synchronization, frequency synthesis modulators and demodulators act as multipliers for generating the desired carrier frequency [124] [220]. However, the general architecture of the PLL is shown in Figure (2.24); it is composed of a voltage-controlled oscillator (VCO) [106], phase detector, frequency divider and low pass filter.

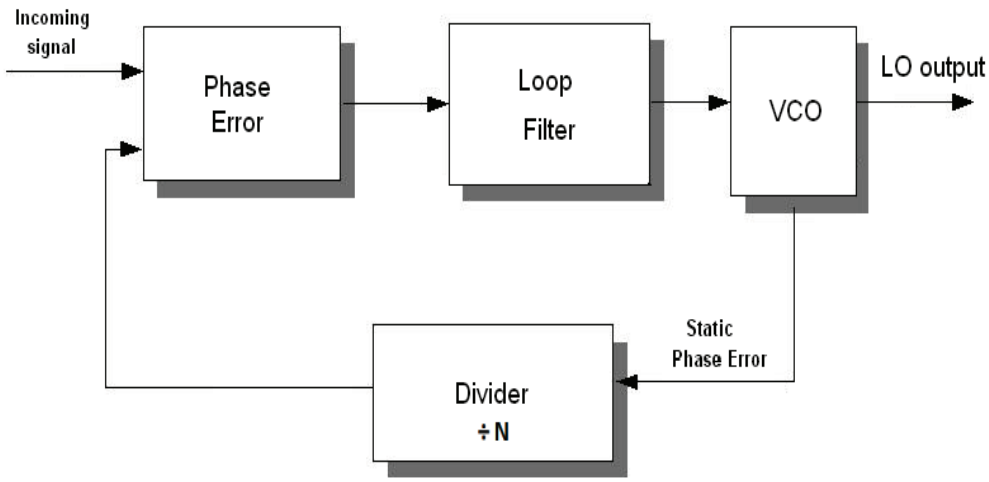


Figure (2.24) the principle architecture for PLL diagram [220]

2.4.3 LC-VCO Tuning Oscillator

Many biomedical transmitter or receiver circuits use the LC-VCO. This can provide good performance at low cost and low power consumption [106]. The low noise VCO can provide a wide tuning range with low power consumption and low phase noise. The LC oscillator has loosely, a tank combined with a noiseless energy restorer that keeps constant oscillation amplitude. This is a most important factor for LC-VCO circuits and decreases the power dissipation and phase noise [152] [170]. The circuit diagram for the LC VCO circuit is demonstrated in Figure (2.25), where the phase noise can be calculated by the formula [173]:

$$L(\Delta f) = 10\log\left[\frac{2KT}{P_{diss,\tan K}}\left(\frac{f_0}{2Q_{\tan k}\Delta f}\right)\right] \tag{2.25}$$

Where we define Boltzmann's constant (K), the ($P_{diss,\tan k}$) is the signal power in watts, and (T) is absolute temperature in degrees Kelvin,($Q_{\tan k}$) is the quality factor for LC circuit. The performance of the VCO is expressed by the widely used Figure of Merit(FOM), which is defined in equation (2.26) as:

$$FOM = L\{\Delta f\} - 20\log\left[\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_D}{1mW}\right)\right] \tag{2.26}$$

where($L\{\Delta f\}$)is the measured phase noise at the frequency offset (Δf) from the oscillation

frequency of (f_0) and (P_D) is the power disspation in (mW).

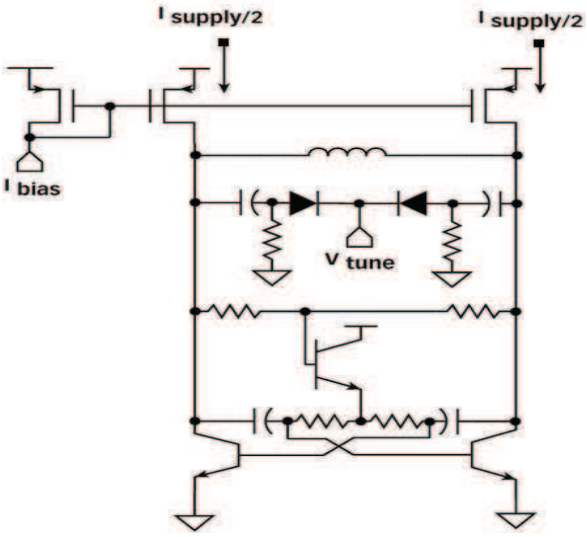


Figure (2.25) the LC-VCO principle of circuit diagram

2.4.4 Ring Oscillator

The other kind of simple oscillator used in biomedical applications is the ring oscillator. The association in closed loop, of an odd number of inverters, constitutes the realization of a ring oscillator. Use of this oscillator type avoids the use of inductances for frequencies up to several MHz [158]. The principle of the ring oscillator is described in Figure (2.26).

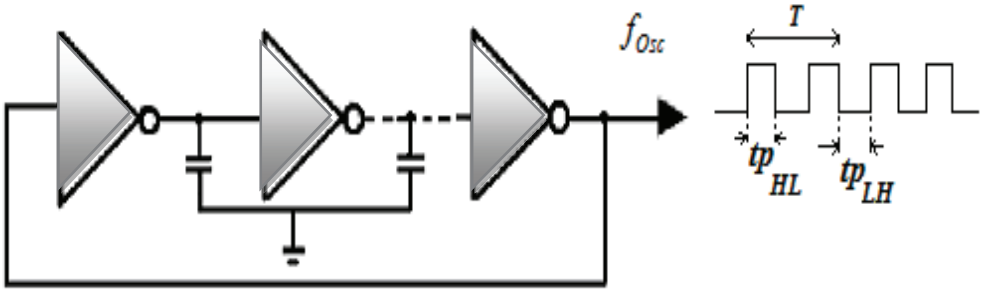


Figure (2.26) the *ring* oscillator principle

The oscillator is achieved by the association, in closed loop, of an odd number of inverters interlaced by capacitance as shown in the above figure. The number of inverters and capacitance values permits us to adjust the oscillation frequency to the desired value.

This frequency can be calculated by the mathematical expressions in equation (2.27), (2.28), (2.29) and (2.30) respectively, where (tp_{HL}) and (tp_{LH}) represent delay times respectively to the fall and the rise time of every inverter, and V_{DD} is represent the source voltage.

$$f_{Osc} = \frac{1}{N.(tp_{HL} + tp_{LH})} \tag{2.27}$$

$$tp_{HL} = \frac{4C}{K_p . \frac{W_P}{L_P} V_{dd}} \tag{2.28}$$

$$tp_{LH} = \frac{4C}{K_p . \frac{W_n}{L_P} V_{dd}} \tag{2.29}$$

$$f_{Osc} = \frac{3.K_n (\frac{W_n}{L_p}).V_{dd}}{16.N.C} \tag{2.30}$$

2.5 Quadrature Phase Shifter and Mixers

2.5.1 Types of Phase shifter

2.5.1.1 Balance phase shifter

Conceptually, both the modulator and demodulator in analogue schemes are required to generate $\pi/2$ or 90^0 out of phase signals in each quadrature carrier pair as demonstrated in Figure (2.27). The accuracy of splitting the phase signal will affect the modulator's characteristic performance [124]. There are varieties of baluns applied in modulators and mixers, to convert an unbalanced single input carrier signal to a pair of balanced signals.

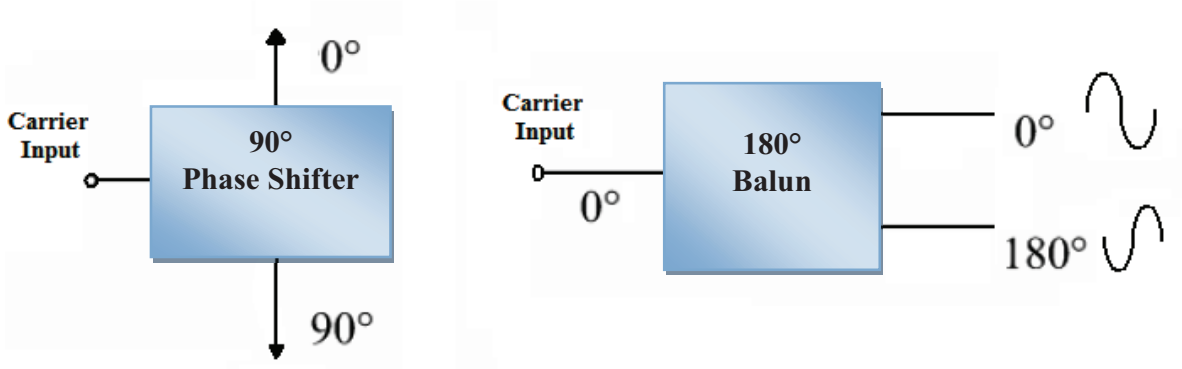


Figure (2.27) the balun phase shifters block diagrams

One type of simple balun is the central tap transformer that is illustrated in Figure (2.31), which works at low frequency up to a few GHz, working on the principle of magnetic induction. The input signal is split between the output signals with a 180° phase shift with zero dc power. The disadvantage of the balun is that it is physically large for medical applications especially in implant device; hence, it is not appropriate for this work.

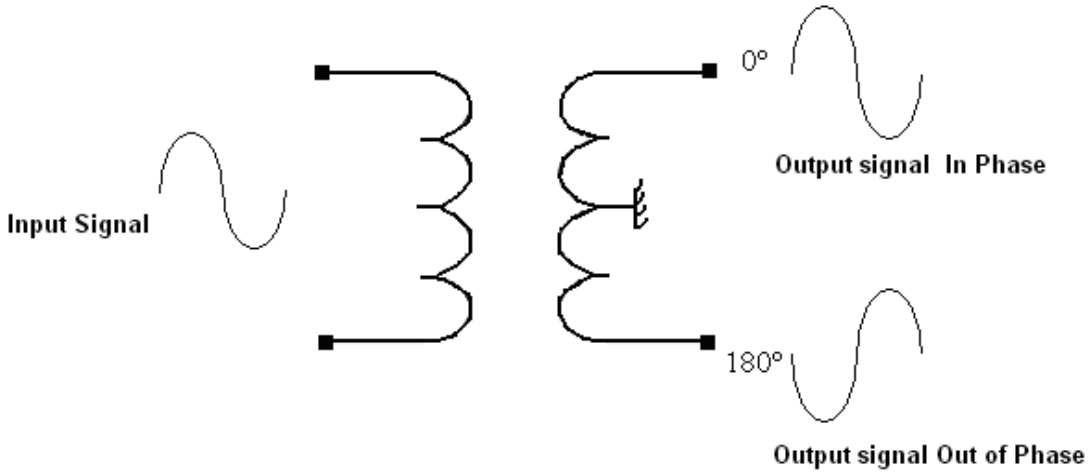


Figure (2.28) the diagram of a simple balun using a transformer tap centre

2.5.1.2 RC-CR

The phase shift for the carrier wave can be provided by different topologies of circuit design, ultimately considering low phase and amplitude error. The simplest is (RC- CR) resistance, capacitor network, which has a small footprint in the circuit and zero DC power consumption. It has a wide margin for overcoming phase errors [97]. The integrating and differentiating (CR) circuit is shown in Figure (2.29). The RC phase shifter consists of a pair of ***R*** resistance and ***C*** capacitor, with the values chosen to yield a transfer function that has constant magnitude for all the frequencies and provides phase difference between their output signals of 90^0, which provides a simple technique to shift the carrier signal by $\pm 45^0$. The phase difference between the two outputs is 90^0 for all desired band frequencies, whereas the amplitudes are equal only at a cut off frequency $\omega = 1/RC$.

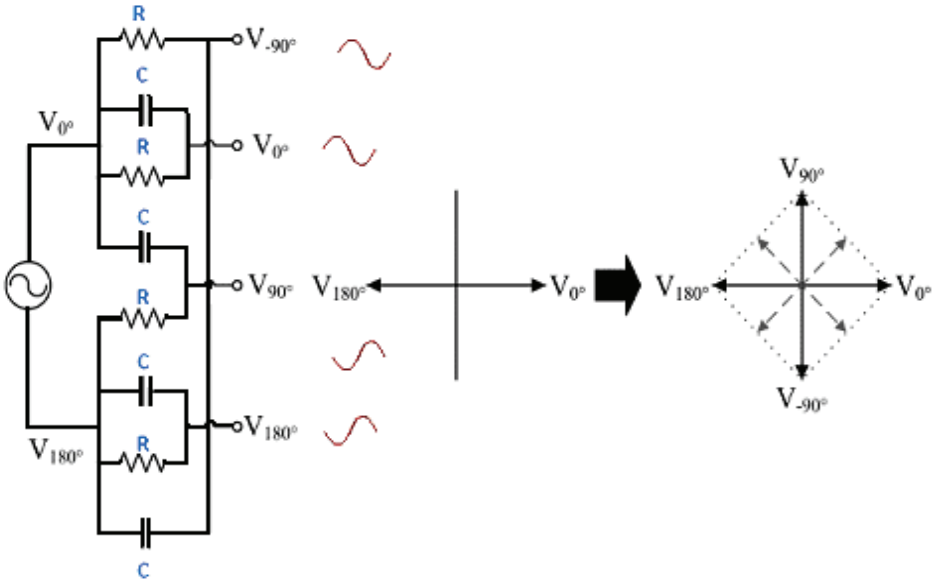


Figure (2.29) shows the RC-Polyphase network diagram

2.5.1.3 RC- polyphase network

In general, the polyphase network has an all pass response with the desired 90^0 phase difference appearing at the cut off frequency of $\omega_c = 1/(RC)$, where the difference inputs are shifted by $\pm 45^o$ toward each other before they are combined [66]. However, to use integrated polysilicon resistance exhibits a large tolerance more than 20%, for small resistance values, whereas high tolerances are critical, as discrepancies will change the cut off frequency introducing phase errors at the desired frequency. The variable resistance of an NMOS transistor based in the triode region is used with the resistance controlled by a tuning voltage V_{Tune} applied to the gate of an NMOS transistor as shown in Figure (2.30). Figure (2.31) shows the RC circuit of the polyphase network.

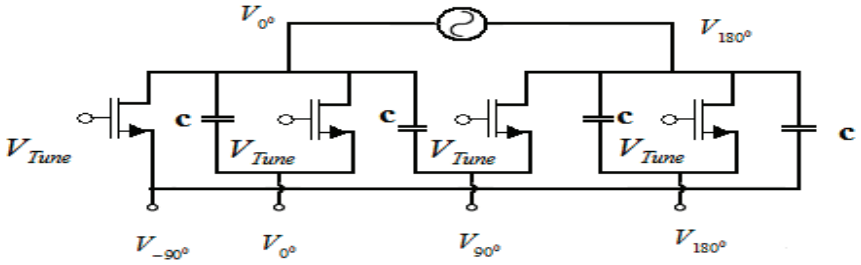


Figure (2.30) the RC-polyphase network diagram

The effective resistance (R) is approximately given by:

$$R = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{Tune} - V_T)} \tag{2.31}$$

Where (μ_n) is the electron mobility, (C_{ox}) is the gate oxide capacitor per unit area, (W) and (L) are the width and length of the transistor, (V_T) is the threshold voltage. Obviously, from this equation (2.31) he resistance value is inversely proportional to the tuning voltage (V_{Tune}) and it can vary to adjust the cut-off frequency.

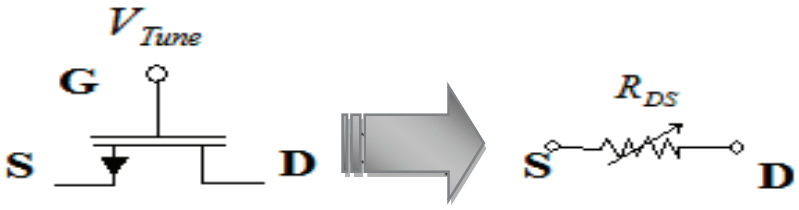


Figure (2.31) the NMOS FET resistance working as variable resistor

2.5.1.4 Active Balun

The active baluns used the FET transistor to create a signal out of phase 180^0 from the input signal, which can be very compact at low RF frequencies comparing to the transformer tap centre. Generally, the FET transistor will inherently add the thermal noise to the output signal about $1/f$ [92]. This will draw dc current and increasing the consumption power of the modulator. The following is a simple active balun using a single FET transistor, shown in Figure (2.32).

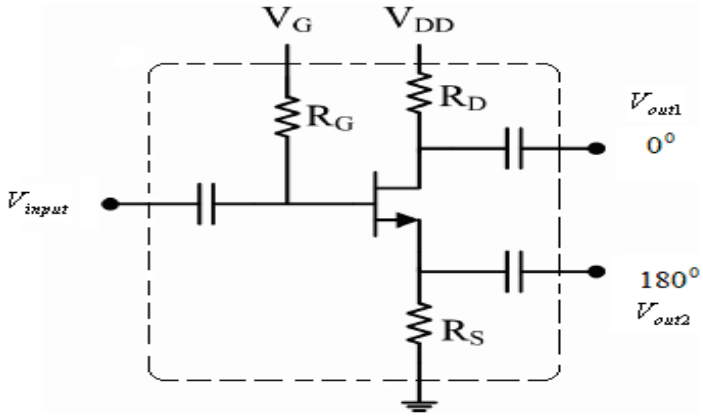


Figure (2.32) the single FET phase shifter circuit

The input signal to the FET is transferred in phase to the source and 180° out of phase at the drain in low input frequency signal. The voltage gain of the FET can be analyzed as the voltage outputs V_{out1} and V_{out2}. The relation between V_{out1} and V_{input} can be expressed in equation (2.32) as:

$$\frac{V_{out1}}{V_{input}} \approx g_m\left(R_s \parallel \frac{1}{g_m}\right) = \frac{R_s}{R_s + \frac{1}{g_m}} \tag{2.32}$$

The same process for the relation between V_{out2} to V_{input} can express in equation (2.33) as:

$$\frac{V_{out2}}{V_{input}} \approx \frac{\frac{1}{g_m}}{R_s + \frac{1}{g_m}}(-g_m R_d) = -\frac{R_d}{R_s + \frac{1}{g_m}} \tag{2.33}$$

where g_m represents the transconductance of the FET and R_s represents the resistance at the transistor source; finally the R_d is the resistance in transistor Drain. Obviously, these equations will give phase independent of the component values. For accurate equal amplitudes, the condition $R_s = R_d$ must be satisfied. Moreover, there are other parasitic capacitances in the FET, which can contribute further to phase imbalance at higher frequencies as depicted in Figure (2.33).

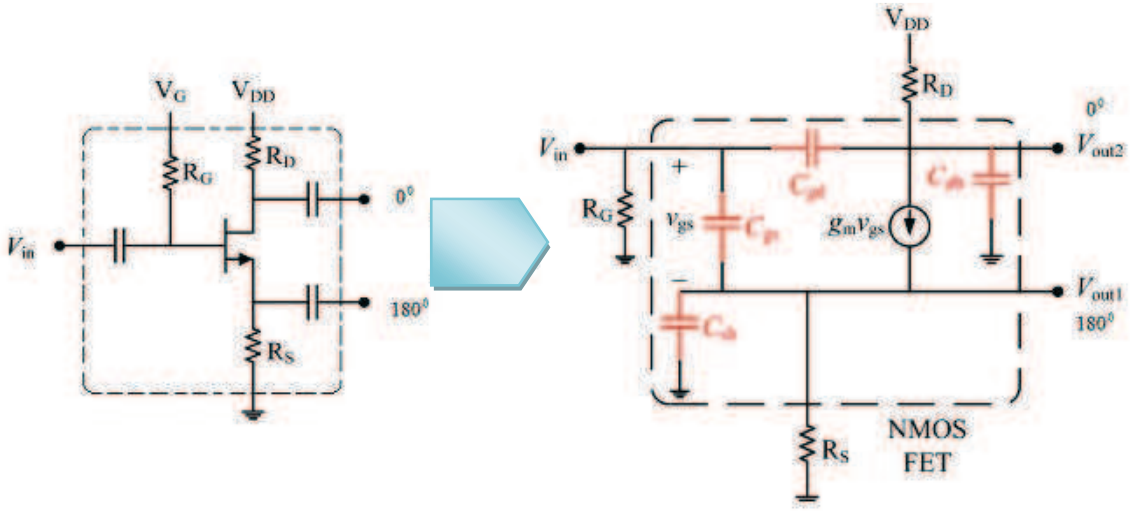


Figure (2.33) Single FET parasitic capacitance at high frequency

2.5.1.5 CG-CS Active Balun

The active balun has better performance and less error in phase. The transistor configuration used is a common-gate, common-source (CG-CS). The common-gate transistor amplifies the input carrier signal in phase, while the second common-source amplifies and reverses the phase; this is shown in Figure (2.34).

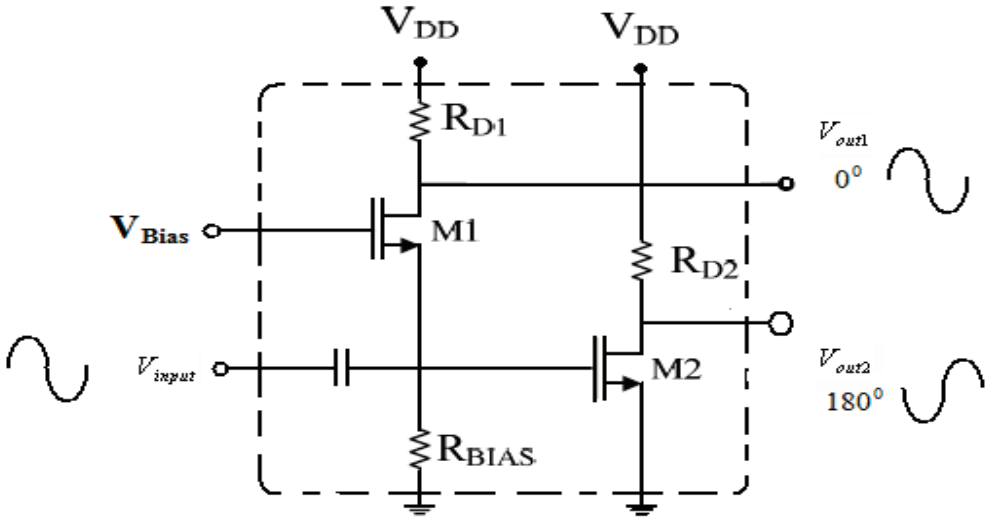


Figure (2.34) the CG-CS Active Balun FET phase shifter circuit

With matching the gain of amplifiers, the outputs can be of equal amplitude. The input impedance for the first stage common-gate FET is approximately given by the relation $1/g_m$, which yields a low input resistance close to the (50Ω). The biasing source resistance R_{Bias} should be considered in the design to avoid affecting the input impedance or attenuating the input signal [54, 97].

2.6 Modulator Mixer

In communications, the mixer is the main part in the modulators, which converts a signal IF to another frequency RF signal in the up-converter case. A mixer can be up-converter or down converter by multiplying by local oscillator LO; there are many techniques to implement the mixers. We can classify them into two types, active mixers and passive ones. The active mixers have an associated gain, whereas the passive mixers can achieve a fixed gain or have loss.

2.6.1 Active Modulator Mixer

In active modulator mixers, the Gilbert cell mixer is a very common mixer applied in modulators, which lends itself particularly well to monolithic integration and has several advantages, including high port-to-port isolation and spurious signal cancellation because of its signal and double balance structure [71] [90]. However, more stable mixers are double balanced mixers, also known as Gilbert Mixers, which are preferred over the single balanced implementations. The Gilbert cell eliminates local oscillator LO-to- intermediate frequency IF, and RF-to-IF feed through which can increase linearity, furthermore susceptibility to supply voltage noise can be decreased [10] [34]. In the real implementations for mixers, the LO input signal can be a square wave signal or sinusoidal signal. This may due to high abrupt switching characteristics for the CMOS transistors, which improve performance and reduce the noise. The local oscillator LO sinusoidal signal is used because it has a very steep slope at high frequencies. Generally, the Gilbert mixer is shown in Figure (2.35).

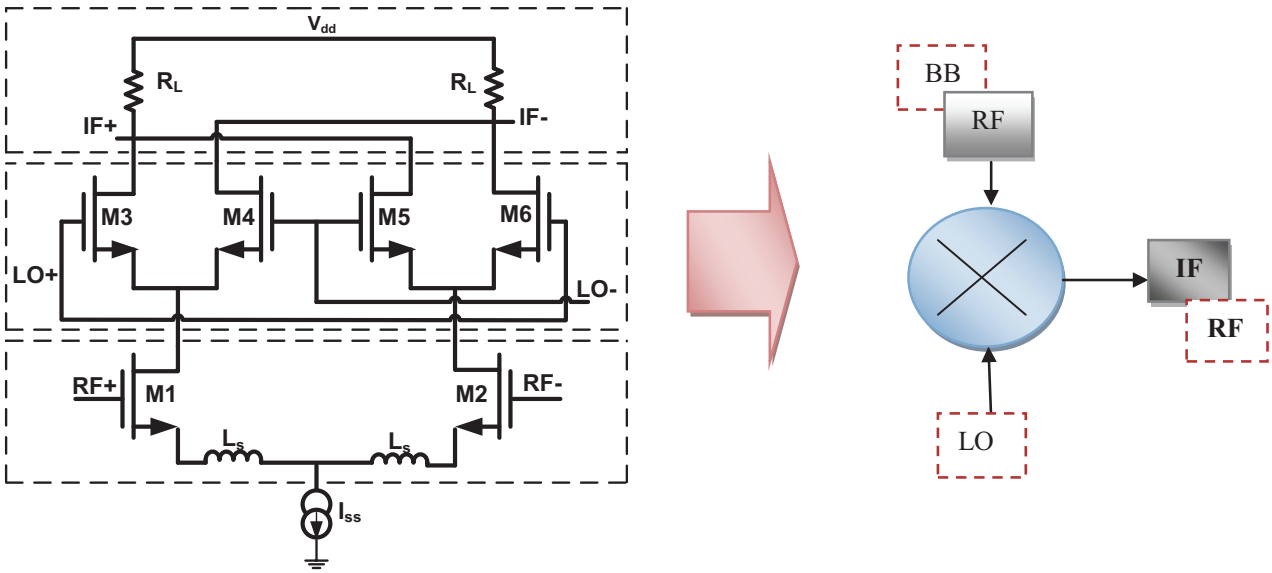


Figure (2.35) the Gilbert mixer working in RF circuit

2.7 Chapter Summary of Modulation Schemes

We have explored the basic principle of analogue and digital modulation categories in this chapter, and investigated different techniques used in a wireless communication. Most of the modulations, which are commonly used in wireless applications, were reviewed and they may be suitable for biomedical implantable devices. In general, we have focused on the appropriate digital modulation and demodulation techniques applied either in the reader unit or at the implant device. However, we can classify the conclusion of this chapter into three sections:

- **Analogue modulation schemes**

We conclude that all types of analogue or hybrid analogue/digital n-PSK modulators work with phase shift carrier angle (ϕ), as the key element for the digital modulation in this work. The phase shifter is the most important part in the modulator, to acquire two discrete signals *sine* and *cosine*. In practice, most common applications use the Direct Digital Synthesizer or Numerical Control Oscillator to generate the RF carrier signal. The conventional analogue modulators have high circuit complexity and high power dissipation; these disadvantages are unsuitable for implantable medical purposes. Regarding the advantage of digital modulation, it offers a digital synthesis flexibility, reconfiguration, and upgrade, when compared to analogue schemes. We can conclude that most of the analogue modulations are not appropriate for implantable purposes, as the digital modulation is the target in this thesis.

- **Digital modulation schemes**

The digital schemes, which are used in biomedical devices, are more reliable than analogue modulation as they have many advantages such as less power consumption and hardware implantation, in addition to less circuitry size.

- **Summary of the modulations applied for biomedical purposes**

We conclude with the most common factors to design a digital modulator for medical implant devices, where the dissipation power consumption by modulator is in the range of (0.55~ 0.75mW) from the total of the wireless received power at implant device, and the operating voltage is in the range of (1.8~3.3 V). The second challenge point in this work is to design a higher data rate modulator for coding the acquisition data returned from the body, which is a

function of the modulator design and the carrier frequency for communication between reader and implant device. Generally, there is a comparison in Table (2.1) below of the most common parameters between analogue and digital modulations, as published, and these were discussed in chapter one. Finally, these introductory analyses for our proposed modulator design will be the background for coding data for medical implant devices. Combining the hardware with the software, which is capable to reconfigure a digital modulator, will be discussed in chapter four in detail.

	Power Carrier	Data Rate	Operation Voltage	Communication distance	Consumption power
AM	Full	Low rate	3.3~5V	Unknown	Unknown
FM	Null	Low rate	3.3 V	Up to 9 cm	Unknown
FSK	Full	Low rate	3.3V	Up to 3.5 cm	Unknown
ASK	Full	Up to kbps	2.5~3.3V	1~2 cm	Unknown
BPSK	Null	Up to Mbps	2.5~3.3V	~2 cm	Unknown
QPSK	Null	Up to Mbps	1.8~3.3V	Unknown	Unknown
DPSK	Null	Up to 2Mbps	4.5~5V	Up to 2.5cm	~8.4mW

Table (2.1) comparison for most modulation types in wireless implantable electronic medical devices

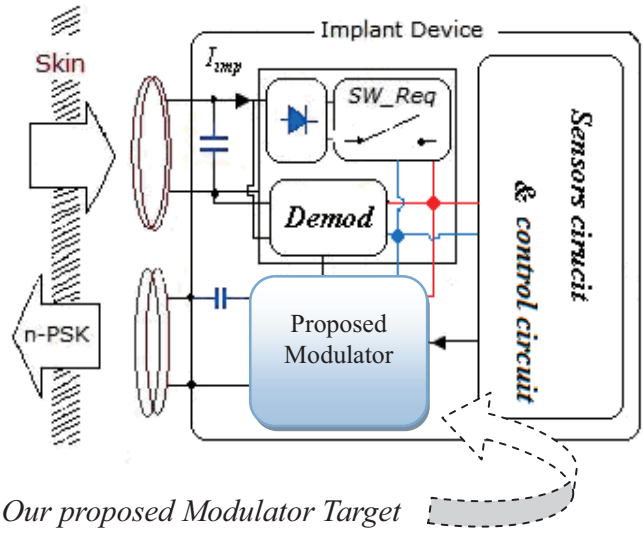


Figure (2.39) the proposed modulator target design inside the implant device

Chapter

3

Inductive Coupling link Power Amplifier And Data Transmission for Transcutaneous Telemetry

Inductive Coupling link, Power Amplifier and LC Antenna Design

3. Inductive Coupling Link

3.1 Theory and Background for Inductive Coupling link

WIRELESS inductive coupling is an attractive developing technology for biomedical applications, which use magnetic coupling as the communication environment, that is common with RFID techniques [1], [126]. Practically, the RF short-range communication transmits a low power, which is less than a milli watt, radiated RF power signal from reader coil antenna, which is mostly designed to offer fixed sinusoidal carrier amplitude, that provides a stable wireless transfer power. The stability of the RF signal gives a high readability for DC voltage at the implant device in terms of the distances from the reader coil [121] [122]. However, the biodevice system is composed of two coils: one implant integrated and isolated inside the human body, the other located outside the body (Reader). To have better power transfer efficiency of inductive coupling link, both sides of the link are tuned at the same resonant frequency f_o. In most cases, the primary circuit is tuned in series resonance to provide a low impedance load for driving the transmitter coil, where the secondary circuit is almost invariably parallel, and uses an LC circuit for better driving of a nonlinear rectifier load. Figure (3.0) demonstrates four resonance possibilities for connections in a passive system. Many formulas approximate for how many turns are required to achieve a specified inductance ***L***. For example, the equations in Table (3.0) give the (N) turns based on loop radius (a), the loop height (h), the loop width (b), (d) wire diameter (R), (r) radius of loop coil and magnetic inductance ***L***. Unfortunately, these equations are only an approximation for ideal conditions. In practice, the number of turns can change based on the properties of wire being used and the shape of the coil. An approach that is more practical is to measure the inductance during construction and add turns until the specified inductance is reached. However, measuring inductance accurately requires a highly specialized and expensive inductance meter [7] [6] [12]. Practically, the resonance frequency f_o can be calculated in the equation (3.0) [2] [3] and [4].

Formulas	Reference
$L = N^2 R\mu_0\mu_r[\ln(\frac{8R}{a}) - 0.2]$	[103]
$L = 2.9\ln\left(\frac{9}{D} - K\right)N^{1.9}$	[133]
$L = \frac{r^2N^2}{(2r+2.8d)*10^5}$	[176]
$L = \frac{0.3\,1(aN)^2}{6a+9h+10b}$	[205]

Table (3.0) the mathematical inductor formulas

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{3.0}$$

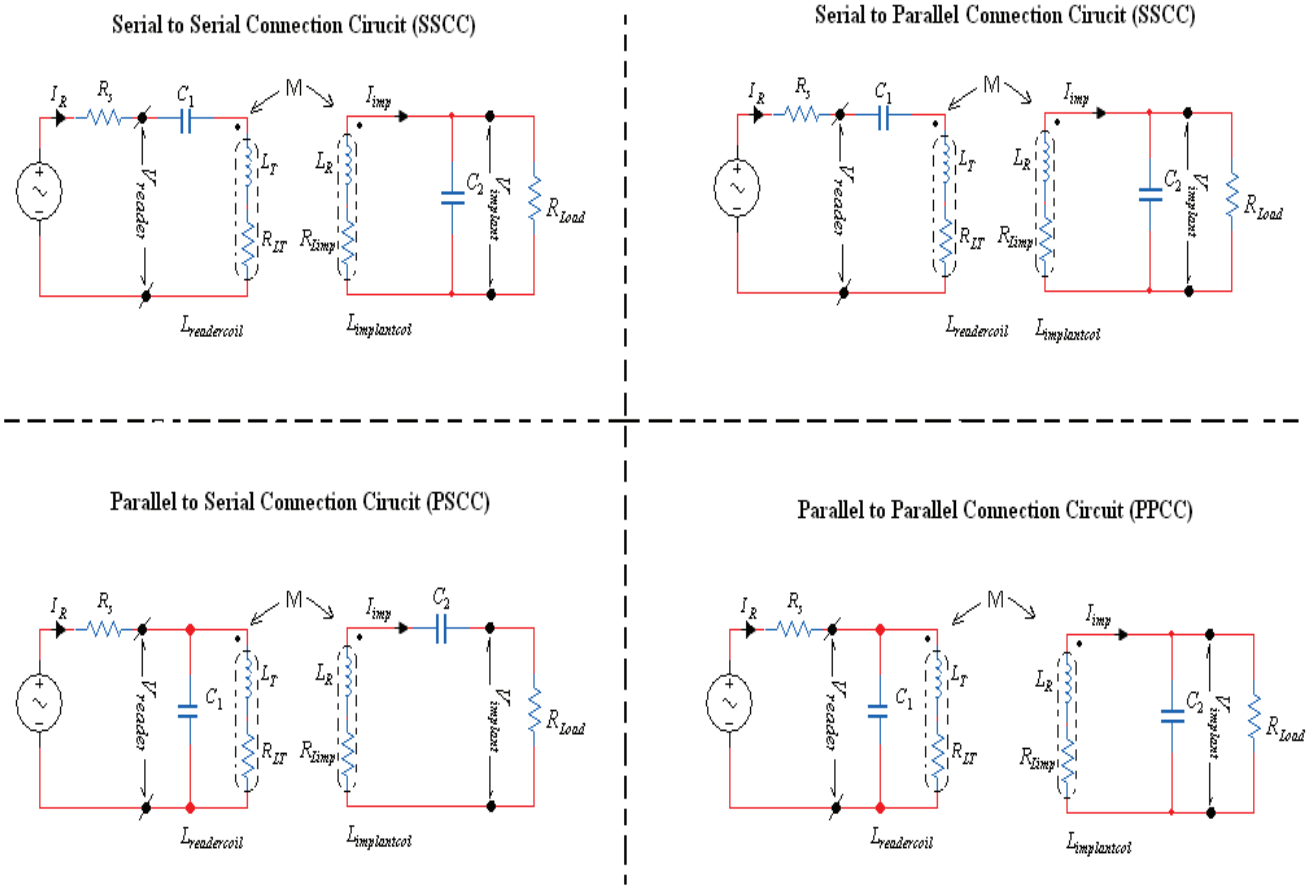


Figure (3.0) the four possible resonance circuits in inductive coupling

3.1.1 Theoretical Derivations

There are several issues to be considered in the design of an inductor for generating magnetic fields. The mathematical analysis and simulation are most important for designing an ideal inductive coupling for estimating the received power. Different mathematical analysis methods have been investigated for solving and deriving the equations for calculating the received power at the implant device. These methods are for evaluating the received power by a load R_{Load} at the implant circuit. In addition, the load resistance is varying over a wide range, at different values for optimum received power. There are many mathematical analysis methods, which can be considered for calculating the received power, and magnetic coupling coefficient [5] [6]. In this chapter, different types of methods are investigated for solving equations to calculate the received power for inductive coupling at the load resistance. Four different types of analysis methods are investigated, as shown in Table (3.1). These theoretical methods are used to calculate the approximation of the received power at the load resistance (R_{Load}) that is equivalent to the implant circuit. Figure (3.1) illustrates the lumped equivalent of the inductive coupling circuit.

A. Mesh coupling analysis circuit	**B. Loose coupling analysis**
C. Reflected impedance analysis	**D. Network circuit analysis**

Table (3.1) investigated mathematical methods for inductive link calculation

A. Mesh Coupling Analysis Circuit

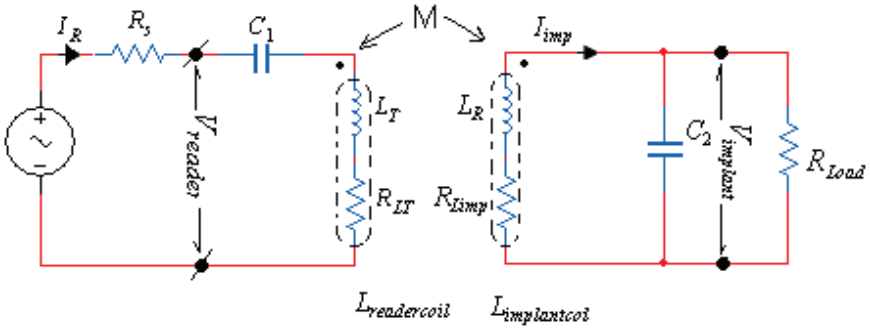


Figure (3.1) the basic lumped equivalent inductive coupling circuit

We describe the mesh equation analysis as the first method for deriving the equations and calculating the received dissipated power by load resistance (R_{Load}). We supposed the reader voltage and the implant voltage could be calculated in equations (3.0) and (3.1) respectively:

$$V_{reader} = R_s + j(\omega L_{reader} - \frac{1}{\omega C_{reader}}) * I_{reader} \pm j\omega M I_{implant} \tag{3.1}$$

$$V_{implant} = \pm j\omega M I_{reader} + Z_{implant} I_{implant} \tag{3.2}$$

where the implant impedance $Z_{implant}$ can be expressed by:

$$Z_{implant} = \frac{R_{Load}}{1 + \frac{R_{load}(-\omega^2 L_{implant} C_2)}{j\omega L_{implant}}} \tag{3.3}$$

By dividing the denominator and numerator in equation (3.3) by ($j\omega L_{implant}$)

$$Z_{implant} = \frac{R_{Load}}{1 + \frac{R_{Load}(-\omega^2 L_{implant} C_2)}{j\omega L_{implant}}} \tag{3.4}$$

Applying to the equations (3.1) and (3.2) Cramer's ruler for the matrix can be written as:

$$\begin{bmatrix} V_{reader} \\ V_{implant} \end{bmatrix} = \begin{bmatrix} Z_{reader} & \pm j\omega M \\ \pm j\omega M & Z_{implant} \end{bmatrix} \begin{bmatrix} I_{reader} \\ I_{implant} \end{bmatrix} \tag{3.5}$$

At the resonance condition the inductor reactance and reactance of the capacitor are both equal, where $j\omega L_{implant} = \frac{1}{j\omega C_2} = 0$. We substitute into the equation (3.3); this yields the implant impedance:

$$Z_{implant} = R_{Load}\ \Omega \tag{3.6}$$

Form the equation (3.5) we can derive the currents and the voltage at the load resistance to get the power consumption delivered by Load, and the reader current can be driven as:

$$I_{reader} = \begin{bmatrix} V_{reader} & -j\omega M \\ 0 & R_L \end{bmatrix} = \frac{V_{reader} R_L}{R_{reader} R_L + \omega^2 M^2} \tag{3.7}$$

The implant current can be calculated in equation (3.8) as:

$$I_{implant} = \begin{bmatrix} R_L & V_{reader} \\ -j\omega M & R_L \end{bmatrix} = \frac{V_{reader}\ R_L}{R_{reader}R_L + \omega^2 M^2} \tag{3.8}$$

where the implant load power can be given in the equation below:

$$P_{implant} = (I_{implant})^2 . R_{load} \tag{3.9}$$

B. Loose Coupling Analysis

The next mathematical method is the loose coupling analysis circuit, where as shown in Figure (3.2), the circuit is serial to parallel connection (SPCC). This can be obtained by modifying the lumped equivalent circuit module in Figure (3.2) as shown in Figure (3.3).

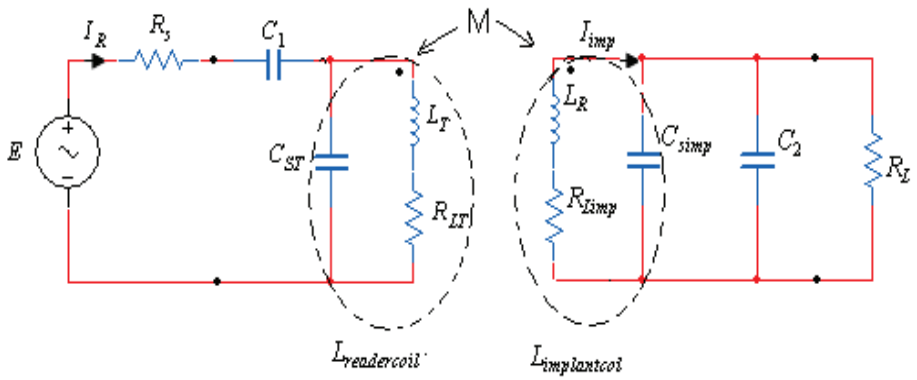


Figure (3.2) the basic lumped equivalent inductive coupling circuit

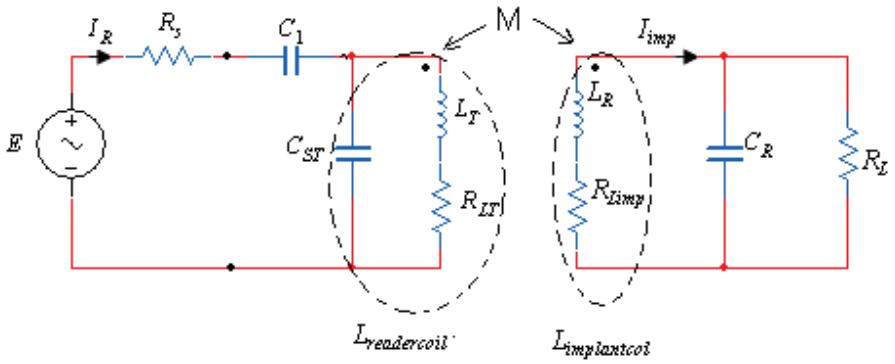


Figure (3.3) the modified circuit where ($C_R = C_{simp} + C_2$)

The impedance of the reader circuit can be approximated as:

$$Z_{reader} = R_s + \frac{1}{j\omega C_1} + \frac{(R_{LT} + j\omega L_T)(\frac{1}{j\omega C_{SR}})}{(R_{LT} + j\omega L_T + \frac{1}{j\omega C_{SR}})} = R_{eq} + jX_{eq} \tag{3.10}$$

Where, the real and imaginary parts are defined by equivalent impedance, *Req* and *Xeq*.

$$R_{eq} = \frac{R_s[(1-\omega^2 L_T C_{SR})^2 + (\omega R_T C_{SR})^2] + R_{LT}}{(1-\omega^2 L_T C_{SR})^2 + (\omega R_{LT} C_{SR})^2} \qquad X_{eq} = \frac{\omega L_T (1-\omega^2 L_T C_{SR}) - \omega R^2 C_{SR}}{(1-\omega^2 L_T C_{SR})^2 + (\omega R_{LT} C_{SR})^2} - \frac{1}{\omega C_1} \tag{3.11}$$

However at resonance condition $X_{eq} = 0$ and $\omega = \omega_o$, where the tuned capacitor C_1 is given as:

$$C_1 = \frac{(1-\omega_o^2 L_T C_{SR})^2 + (\omega R_{LT} C_{SR})^2}{\omega_o (L_T - \omega_o^2 L_T^2 C_{SR} - R_R^2 C_{SR}} \tag{3.12}$$

Instead of the reader coil with the parasitic capacitor ($C_{SR} = 0$), at low frequencies, that yields ($C_1 = \frac{1}{\omega_o^2 L_r}$), as usual for a series RLC circuit. The impedance of the equivalent circuit on the implant coil part is given by:

$$Z_{imp} = \frac{1}{\frac{1}{R_{Limp} + j\omega L_{imp}} + j\omega C_R + R_L} \tag{3.13}$$

$$R_{eq} = \frac{R_{imp} R_L (R_L + R_{imp}) + 2\omega^2 L_{imp} R_L}{(R - \omega^2 L_{imp} C_R R_{Lr} + R_{Lr})^2 + (2\omega L_{imp} + \omega C_R R_{Lr} R_L)^2} \tag{3.14}$$

$$X_{eq} = \frac{\omega R_L^2 (L_{imp} - C_R R_{Lr}^2 - \omega^2 L_{imp} C_R)^2}{(R - \omega^2 L_{imp} C_R R_{Lr} + 2R_{Lr})^2 + (2\omega L_{imp} + \omega C_R R_{Lr} R_L)^2} \tag{3.15}$$

At resonance, ($X_{eq} = 0$) and ($\omega = \omega_o$), this yields the ($C_R = \frac{L_{Lr}}{\omega_o^2 L_{Limp}^2 + R_{Lr}}$) where the value of the capacitor is ($C_R = C_{simp} + C_2$). By applying KVL for the reader, circuit Figure (3.3)

$$V_{reader} = R_s + \frac{I_r}{j\omega C_1} + I_{Lr}(R_{Lr} + j\omega L_r) - j\omega M I_{imp} \tag{3.16}$$

$$I_{Lr} = I_r - \frac{I_{Lr}(R_{Lr} + j\omega L_r) - j\omega M I_{Limp}}{\frac{1}{j\omega C_1}} \tag{3.17}$$

Substituting the Equations (3.16) and (3.17) gives:

$$V_{reader} = R_s + I_{Lr}(R_{eq} + j\omega_{eq}) - j\omega M I_{imp}(1 + \frac{C_r}{C_1}) \tag{3.18}$$

Where $R_{eq} = R_{L_r}(1+\frac{C_r}{C_1})$ and $X_{eq} = \omega L_r - \frac{1}{\omega C_1} + \omega L_r \frac{C_{sr}}{C_1}$

Applying Cramer's rule for the array matrix, we may write to determine the currents of the circuit (I_r) and ($I_{implant}$) for the coupling circuit of Figure (3.3):

$$\begin{bmatrix} V_{reader} \\ \\ 0 \end{bmatrix} = \begin{bmatrix} \mathrm{Re}\,q + jXeq & -j\omega M(1+\frac{C_{st}}{C_1}) \\ \\ -j\omega M & Rimp + j\omega L_r + \dfrac{\frac{R_L}{j\omega C_R}}{\frac{1}{j\omega C_R} + R_L} \end{bmatrix} \begin{bmatrix} I_{L_r} \\ \\ I_{L_{imp}} \end{bmatrix} \tag{3.19}$$

$$\begin{bmatrix} Vreader \\ \\ 0 \end{bmatrix} = \begin{bmatrix} R_{eq} + jX_{eq.} & -j\omega M(1+\frac{C_{st}}{C_1}) \\ -j\omega M & R_{eq_{imp}} + jX_{eq_{imp}} \end{bmatrix} \begin{bmatrix} I_{Lr} \\ \\ I_{im} \end{bmatrix} \tag{3.20}$$

where ($R_{eq_{imp}} = R_{Limp}(1+\frac{R_L}{1+\omega^2 C_R^2})$) and ($X_{eq} = \omega L_{imp} - \frac{\omega C_R}{1+\omega^2 C_R^2}$) apply the matrix, inversion to the equation (3.20):

$$\begin{bmatrix} I_{Lr} \\ \\ 0 \end{bmatrix} = \frac{1}{A_{imp} + jB_x} \begin{bmatrix} R_{eq_{imp}} + jX_{eq_{imp}} & j\omega M \\ j\omega M(1+\frac{C_{st}}{C_1}) & R_{eq_{reader}} + jX_{eq_{reader}} \end{bmatrix} \begin{bmatrix} V_{reader} \\ \\ 0 \end{bmatrix} \tag{3.21}$$

where ($A_{imp} = R_{eq_{imp}} R_{eq_{reader}} - X_{eq_{imp}} X_{eq_{reader}} + \omega^2 M^2 (1+\frac{C_{st}}{C_1})$) and ($B_X = X_{eq_{imp}} R_{eq_{imp}} + X_{eq_{imp}} R_{eq_{reader}}$) after analysis of the matrix we get the implant current by:

$$I_{implant} = \frac{j\omega M V_{reader}(1+\frac{C_{SR}}{C_1})}{A_{imp} + jB_X} \tag{3.22}$$

The voltage across the load resistance can be given by:

$$V_{RL} = I_{Lr} \frac{\frac{R_L}{j\omega C_R}}{\frac{1}{j\omega C_R} + \frac{1}{R_L}} = \frac{j\omega M V_{reader}(1+\frac{C_{ST}}{C_1})}{A_{imp} + jB_X} \frac{R_L}{1+\omega^2 C^2} \tag{3.23}$$

From the above analysis, the power dissipated by the load resistance (at the implant circuit) can be calculated as given in the equation:

$$P_{implant} = \frac{V_{RL}^2}{R_{Load}} \tag{3.24}$$

C. Reflected Impedance Concept Analysis

The third method for solving the coupling analysis circuit is by using the reflected impedance concept. That gives the primary current circuit (I_{reader}) and the secondary current at implant circuit ($I_{implant}$), since both reader and implant circuits are resonant and, under this condition, the received power has been optimised at the load resistance. Figure (3.4) shows the lumped equivalent inductive coupled circuit for the reflected impedance analysis.

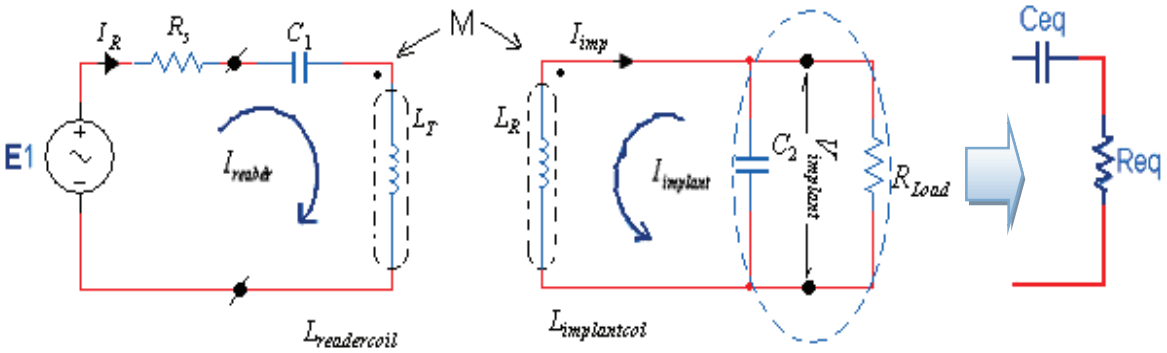


Figure (3.4) the lumped equivalent circuit for reflected impedance

The loop equation for the reader circuit is:

$$V_{reader} = Z_1 * I_{reader} \mp j\omega M I_{implant} \tag{3.25}$$

where $Z_1 = R_s + j(\omega L_{reader} - \frac{1}{\omega C_{reader}})$

$$V_{implant} = 0 = \pm j\omega M I_{reader} + I_{implant} * (Z_L + j\omega L_{imp}) \tag{3.26}$$

we can obtain the implant current ($I_{implant}$) from the equation (3.26):

$$I_{imp} = \pm I_{reader} \frac{j\omega M}{Z_L + j\omega L_{imp}} \tag{3.27}$$

where we substitute the equation (3.27) in the equation (3.26) that yields:

$$V_{reader} = Z_1 * I_{reader} \mp j\omega M(\pm I_{reader} * \frac{j\omega M}{Z_L + j\omega L_{imp}}) \tag{3.28}$$

$$V_{reader} = I_{reader}(Z_1 + \frac{\omega^2 M^2}{Z_L + j\omega L_{imp}}) \quad \Rightarrow \quad = I_{reader}(Z_1 + Z_{ref}) \tag{3.28}$$

The reflected impedance can be expressed as:

$$Z_{ref} = \frac{\omega^2 M^2}{Z_L + j\omega L_{imp}} \tag{3.29}$$

Mathematically, the load impedance at implant circuit can be given by:

$$Z_L = \frac{R_L}{1+\omega^2 C_2{}^2 R_L^2} - j\frac{\omega C_2 R_L^2}{1+\omega^2 C_2{}^2 R_L^2} \tag{3.30}$$

The equivalent circuit for the implant part is substituted by (Z_{ref}) as shown in Figure (3.5).

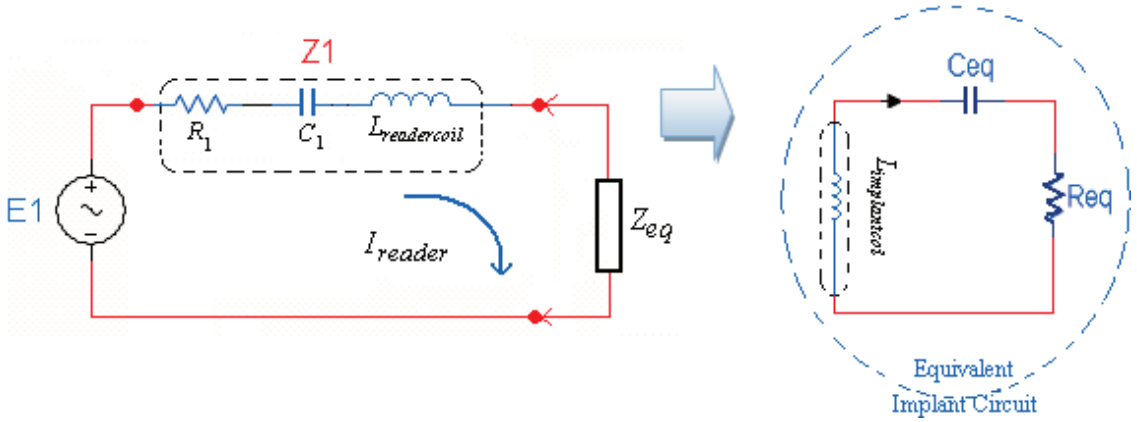


Figure (3.5) Equivalent impedance circuit at load part

To calculate the total impedance of the circuit, we are using the equation (3.31) and the equation (3.32) that yields the total impedance of the circuit as expressed in equation (3.33).

$$Z_{total} = Z_1 + Z_{ref} \tag{3.31}$$

$$Z_{total} = [R_s + j(\omega L_{reader} - \tfrac{1}{\omega C_{reader}})] + \frac{(\omega^2 M^2)}{Z_L + j(\omega L_{imp})} \quad \Omega \tag{3.32}$$

$$Z_{total} = [R_s + j(\omega L_{reader} - \tfrac{1}{\omega C_{reader}})] + \frac{(\omega^2 M^2)}{\frac{R_L}{1+\omega^2 C_2{}^2 R_L^2} - j\frac{\omega C_2 R_L^2}{1+\omega^2 C_2{}^2 R_L^2} + j(\omega L_{imp})} \tag{3.33}$$

The reader current can be calculated from the equation (3.29) and the equation (3.33):

$$I_{reader} = \frac{V_{reader}}{Z_{total}} \quad \text{Amp} \tag{3.35}$$

The implant current

$$I_{implant} = \frac{E_2}{Z_2} \quad \text{Amp} \tag{3.36}$$

D. Network Circuit Analysis

The last mathematical method for analysing the inductive coupling circuit is by applying the network circuit analysis method, as shown in Figure (3.6). This considers the internal resistance of the coil R_{coil} ; the circuit was converted to the equivalent for more simple analysis as demonstrated in Figure (3.7). However, this circuit is divided into four complex impedance circuits, for calculating the voltage and the current passed through the load impedance (R_{Load}).

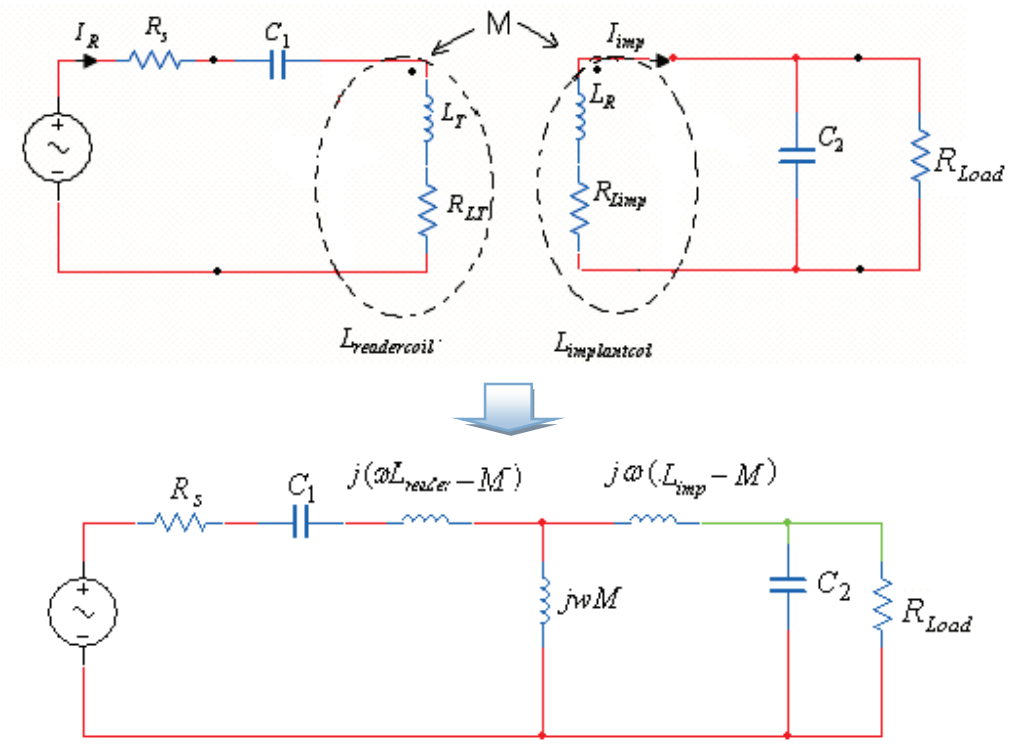


Figure (3.6) the inductive circuit converted to the equivalent circuit diagram

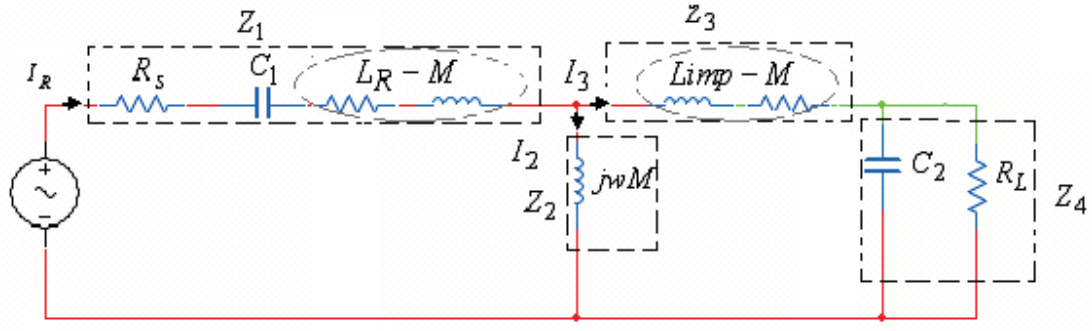


Figure (3.7) the equivalent circuit can be simplified as shown

The mathematical steps below describe the derivation of the equations for analysis and calculate the circuit impedances as:

$$Z_1 = (R_s + R_{LR}) + \frac{1}{\omega C_1} + j\omega(L_R - M) \tag{3.37}$$

$$Z_1 = (R_s + R_{LR}) + j[\omega(L_R - M) - \tfrac{1}{\omega C_1}] \tag{3.38}$$

$$Z_2 = jX_M \tag{3.39}$$

$$Z_3 = R_{LR} + j\omega(L_{imp} - M) \tag{3.40}$$

$$Z_4 = \frac{R_L - j\omega C_2 R_L^2}{1 + \omega^2 C_2^2 R_L{}^2} \tag{3.41}$$

$$Z_4 = \frac{R_L}{1 + \omega^2 C_2^2 R_L{}^2} - j\frac{\omega C_2 R_L^2}{1 + \omega^2 C_2^2 R_L^2} \tag{3.42}$$

The total impedance Z_T of the circuit can be calculated in an equation as:

$$Z_{total} = Z_1 + [Z_2 \| (Z_3 + Z_4)] \tag{3.43}$$

$$I_1 = \frac{E}{Z_{total}} \tag{3.44}$$

$$I_2 = I_1 \frac{(Z_3 + Z_4)}{(Z_2 + Z_3 + Z_4)} \tag{3.45}$$

$$I_3 = I_1 \frac{Z_2}{Z_2 + Z_3 + Z_4} \tag{3.46}$$

Referring to figure (3.7), we can calculate the voltage (V_4) cross the circuit Z4 as:

$$V_4 = I_4 * Z_4 \tag{3.47}$$

Obviously, since we get the voltage V_4 we can calculate the power dissipated by the load resistance, given in the equation below:

$$P_{implant} = \frac{(V_4)^2}{R_{load}} \tag{3.48}$$

3.1.2 Hypothetical Methods Simulation and Measurements

A. MATLAB Simulation

Four methods have been simulated to calculate the dissipated power by the load impedance at implant circuit. The optimum received power was calculated by the mesh coupling analysis circuit, loosely coupled reflected impedance analysis, and network circuit analysis. The MATLAB model has been mathematically validated by simulation and verification of the inductive coupling design and calculation for the optimum power transfer over wireless coupling link. Our coil values are selected by the design parameters for the perfect inductance with respect to the chosen centre frequency at 135 kHz. The reader coil is given as $L_{reader} = 450\mu H$, where the implant is $L_{implant} = 450\mu H$. The analyses were performed with different loads (R_{Loads}), the simulation values given were between 6500~ 8500 Ω for the selected coils. Figure (3.8) demonstrates the optimum captured wireless power, which can be dissipated by the load resistance.

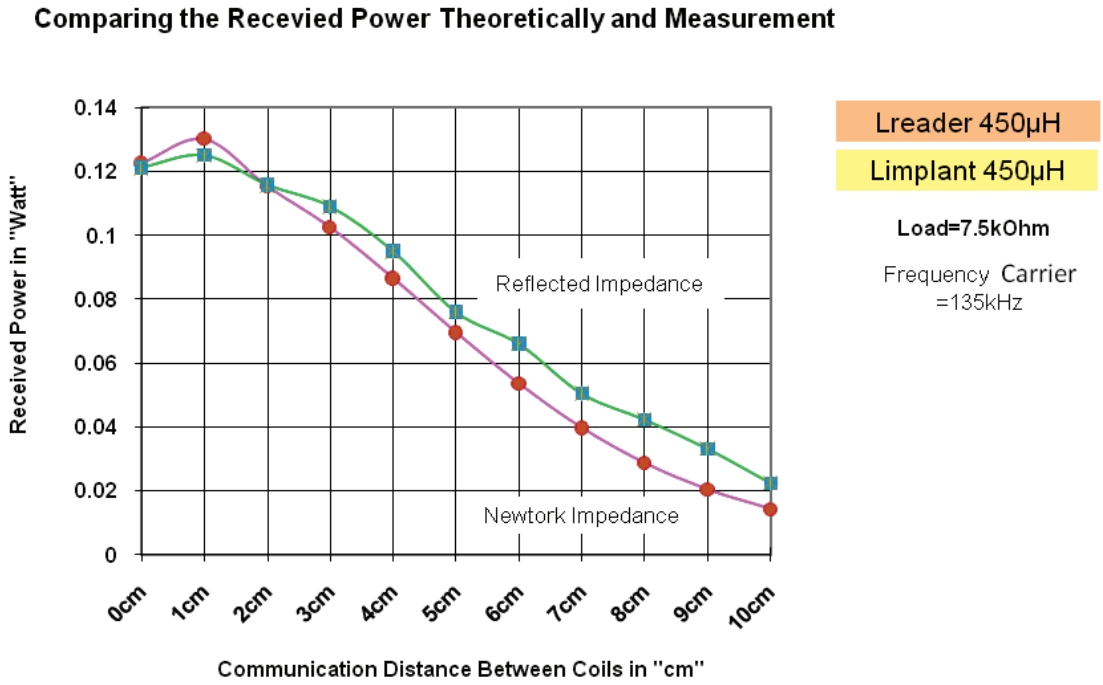


Figure (3.8) the MATLAB/ Simulation and measurement comparison for Optimum received Power with different methods

B. Lab Bench Measurements

The prototype inductive coupling link has been evaluated by lab measurements. Comparing the four theoretical methods calculations from Figure (3.8) it can be seen that there were slight differences between the reflected and network analysis methods, while the other two methods showed a significant difference in the calculation for the estimated wireless received power. Practically, the coil is a critical element of the design for both links. Although many methods and simulations were conducted, to choose the best inductor in this work for the prototype, the optimum method was the inductive coupling circuit. The Lab measurements obtained at $L_{implant}$ and $L_{implant}$ is equal to $450.8\mu H$ where appropriate coils are selected to get the best transfer power and optimum mutual coupling. Obviously, in Figure (3.9) the theoretical received power decays at a constant rate, where the measured values are given better at closed positions and reducing at separation distance from 1~7cm. This has clarified that the robust link is not possible when there is a large distance between two antenna coils. However, as the received power is a function of many parameters, we simulated and compared the received power between four different computation theories to improve the inductive coupling design as shown in Table (3.2), which demonstrates the theoretical power efficiency.

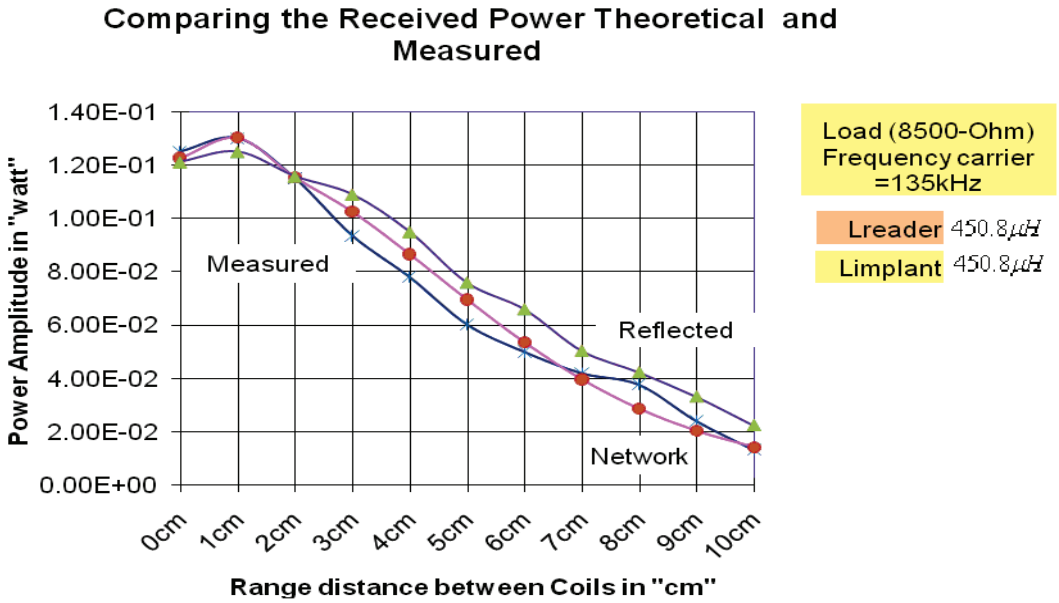


Figure (3.9) shows a comparison of theoretical methods and measured received power at Load (8500Ω)

Theoretically Calculated Methods for Received Power " R_{Load} "								
Distance	Loosely Coupling Analysis Circuit		Mesh Coupling Analysis Circuit		Reflect Impedance Analysis Circuit		Network circuit analysis	
	Watt	η [%]	Watt	η [%]	Watt	η [%]	mW	η [%]
0cm	90.56	36.3588	95.78	38.465	99.806	40.081	100.16	40.221
1cm	84.282	35.36	85.262	35.779	85.582	35.911	84.980	35.660
2cm	75.894	29.352	76.554	26.767	76.304	29.501	75.997	27.817
3cm	60.164	22.021	61.100	22.186	61.364	22.461	61.104	22.187
4cm	41.566	15.088	41.966	15.238	42.166	15.310	42.60	15.468
5cm	25.932	9.292	26.632	9.545	26.022	9.3380	26.532	9.509
6cm	15.341	5.656	16.541	6.362	15.941	6.1311	15.944	6.132
7cm	8.941	3.432	9.141	3.515	8.991	3.458	9.041	3.564
8cm	5.253	2.068	6.053	2.383	5.593	2.201	5.953	2.343
9cm	3.147	1.256	4.217	1.687	3.507	1.402	4.147	1.656
10cm	1.932	0.788	3.132	1.278	2.532	1.033	2.132	0.870

Table (3.2) a comparison of the methodological analyses

However, the experimental measurements were performed with different coil designs for optimum received power with different load resistances. A sample coil at (450.8 µH) is demonstrated in Figure (3.10). The optimum received power over separation distance at maximum 10cm, where the reader coil was designed at 10cm in diameter and implant coil is 3cm.

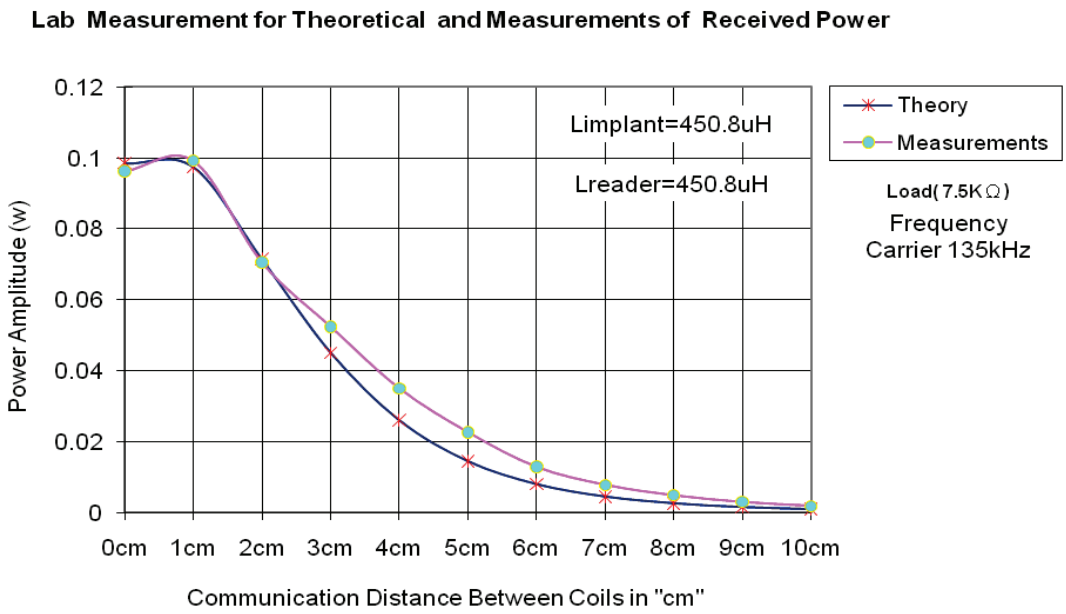


Figure (3.10) the optimum received power for the choice of coil at reader and implant

In addition, the transmitter coil was designed with 10-gauge wire size, which was chosen since it has the highest self–resonance frequency compared to other gauge sizes. The self-inductance of coil is 450μH, the winding resistance about (0.8Ω) and the estimated parasitic capacitance is (100pF). However, the reader and implant coils designed in the Lab test bench are shown in Figure (3.11) and the reader unit is shown in Figure (3.12) respectively.

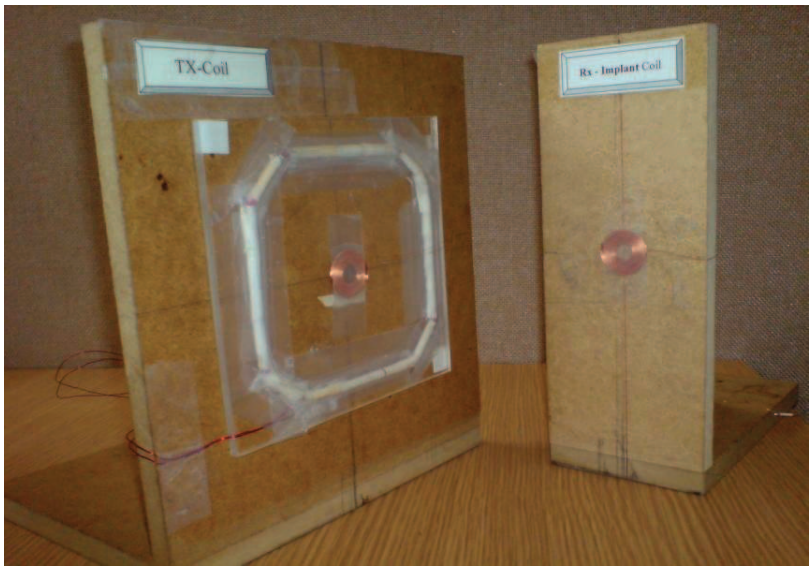


Figure (3.11) Fabricated transmitter and receiver coils

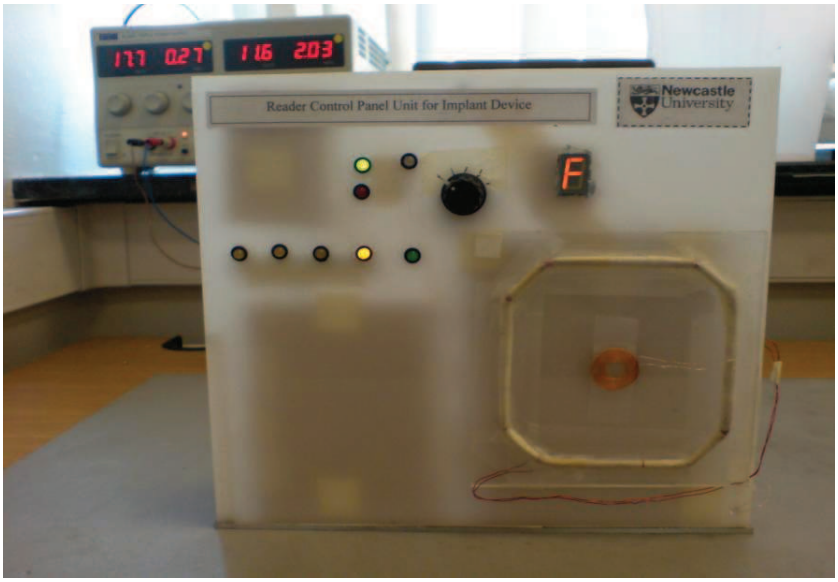


Figure (3.12) Reader unit for inductive coupling link with coils

3.1.3 Inductive Coupling Link Efficiency

3.1.3.1 Mutual and Coupling coefficients for Inductive link

The magnetic field is the key parameter in a proximity communication system that uses inductive coupling, which is one of the possible system to communication for biomedical implants. The maximum magnetic flux that is passed through the implant coil is obtained, when the two coils reader and implant are placed in parallel with respect to each other. This situation results in maximum range reading and maximum induced voltage in the implant coil. However, the coupling coefficient between the two coils is maximized in the above condition. The reading distance has physical limitations: one of the limitation factors in low passive wireless coupling is misalignment, where the maximum reading distance is determined by RF power and signal interference. Typically, the reading distance is only a few centimetres. Because increasing the power and frequency is not always practical, the common solution to increasing the reading distance is by modifying the coil used for magnetic inductive coupling. Generally, the bigger radius of the loop antenna will result in a greater reading, but is limited in physical size. Many investigation efforts are in progress to improve the received power in the implant coil. Figure (3.13) demonstrates the relation of magnetic coupling between two coils reader and implant, as a function of distance and alignment of angle.

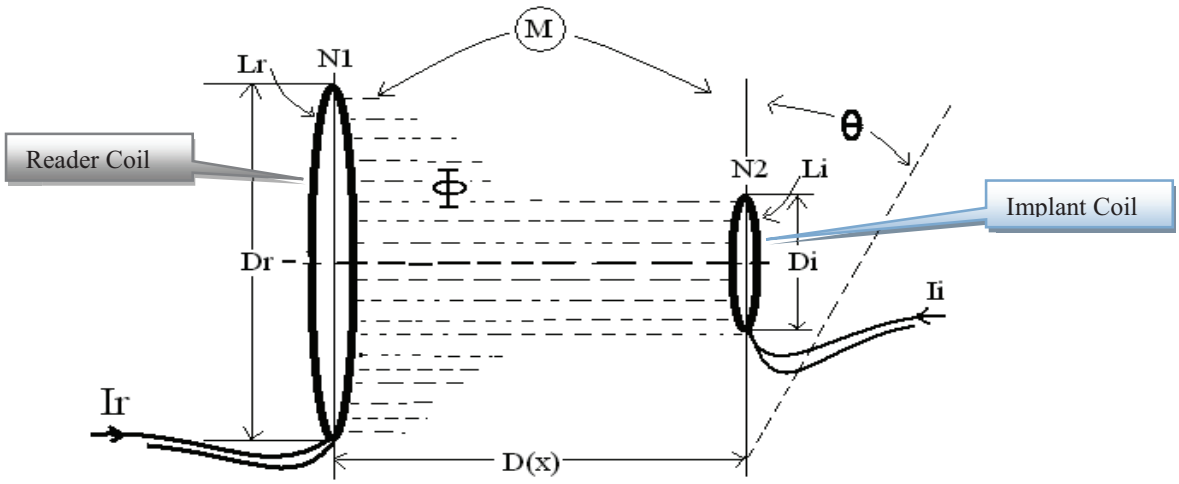


Figure (3.13) the geometry for inductive coupling and orientation between two coils

Practically, the electro-magnetic interference will become too great for a large loop coil to function correctly. The main challenge of coil antenna design is to determine the optimal number of turns: the number of turns determines the magnetic inductance of the loop coil. However, the loop coil antenna of the transmit reader emits an electromagnetic field of the strength ($H(x)$), produced by current (I_R), this can be defined in a mathematical equation as:

$$H(x) = \frac{I_r N_r R_r^2}{2(R_r^2 + x^2)^{3/2}} \quad [\tfrac{A}{M}] \tag{3.50}$$

The magnetic field density is expressed in the equation as:

$$B = \mu_0 H \tag{3.51}$$

Where substituting equation (3.48) in equation (3.49) it yields:

$$B(x) = \frac{\mu_0 I_r N_r R_r^2}{2(R_r^2 + x^2)^{3/2}} \quad [T] \tag{3.52}$$

Firstly, the transmitter coil antenna is tuned at the centre frequency and matched with the source. The maximum transmission efficiency is typically independent of the tuning distance; if the circuit is detuned from the resonance frequency, it will drop dramatically. Figure (3.14) shows the geometry of magnetic coupling analysis design for the reader coil.

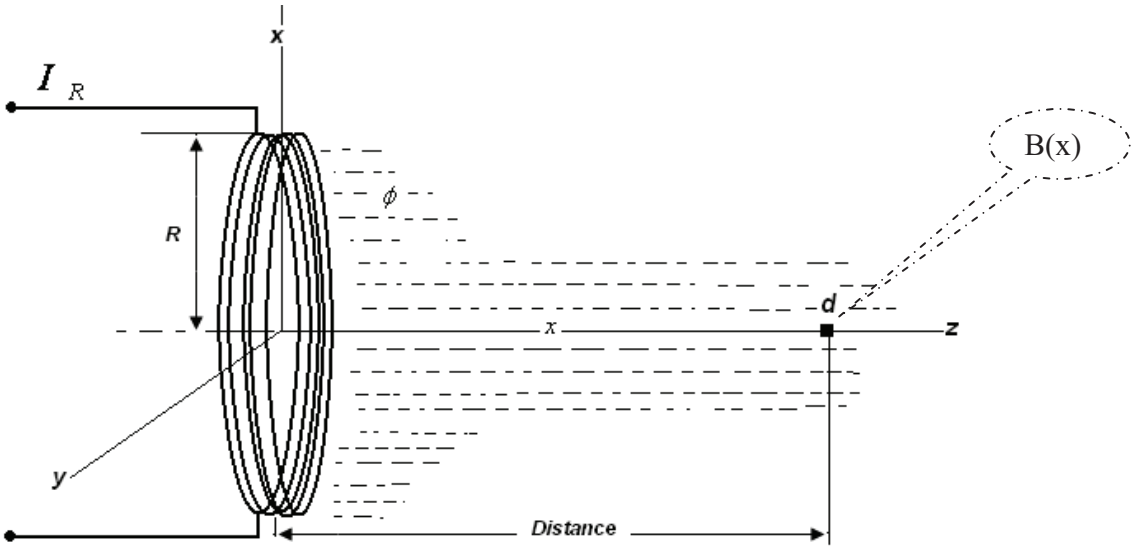


Figure (3.14) the loop coil geometry compared to magnetic flux

Obviously, the geometry of the coupling link needs to consider the coil sizes for biomedical applications. Figure (3.15) demonstrates the percentage of the size relation between reader and implant coils. Theoretically, there are several formulas for computing the mutual inductance and coefficients of coupling, when considering the orientations of the coils. The magnetic flux ϕ which produces the induced voltage on the implant coil gives the equations below (3.53) and (3.54) shows the computed mutual coupling (M) formulas [108],[115]. The second factor is the coupling coefficient (K) between two coils reader and implant; it is expressed in equation (3.55) and (3.56) respectively.

$$M_{21} = \frac{\Phi_{A2}}{I_{Reader}} = \frac{1}{I_{\text{Reader}}} \iint_{A2} \vec{B}\, d\, \vec{A}_2 = \frac{\mu_0}{I_{\text{Reader}}} \iint_{A2} \vec{H}_2 d\, \vec{A}_2 \tag{3.53}$$

$$M(x) = K(x)\sqrt{L_{reader} * L_{implant}} \tag{3.54}$$

$$K = \frac{Rred^2 * Rimp^2 * \cos\theta}{\left(\sqrt{Rred * Rimp}\right) * \left(Rred^2 + X^2\right)^{3/2}} \tag{3.55}$$

$$K = \frac{\mu_0 \times r_R^2}{2\left(Rred^2 + X^2\right)^{3/2}} \frac{S_i \cdot N_R \cdot N_i}{\sqrt{L_i * L_R}} \tag{3.56}$$

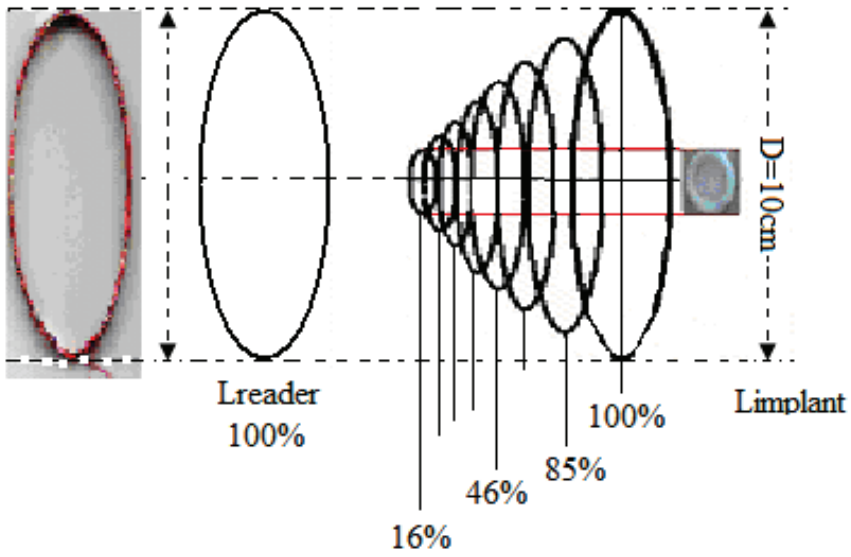


Figure (3.15) the comparison of coupling coefficient between the implant and reader coils

3.1.3.2 Lab Characterization Measurements for Mutual Coupling

The lab measurements for optimum coupling coefficient between reader and implant over different distances is demonstrated in Figure (3.16). It shows the diameter of the reader coil and the modified implant coil diameter fixed at 3cm, for measuring the optimum diameter size of reader coil. The best inductance has been approximately 450.8µH, where the best diameter has been given between (8 ~12 cm). Table (3.3) illustrates the mutual and coupling coefficient between theory and measurement for optimum design of the system.

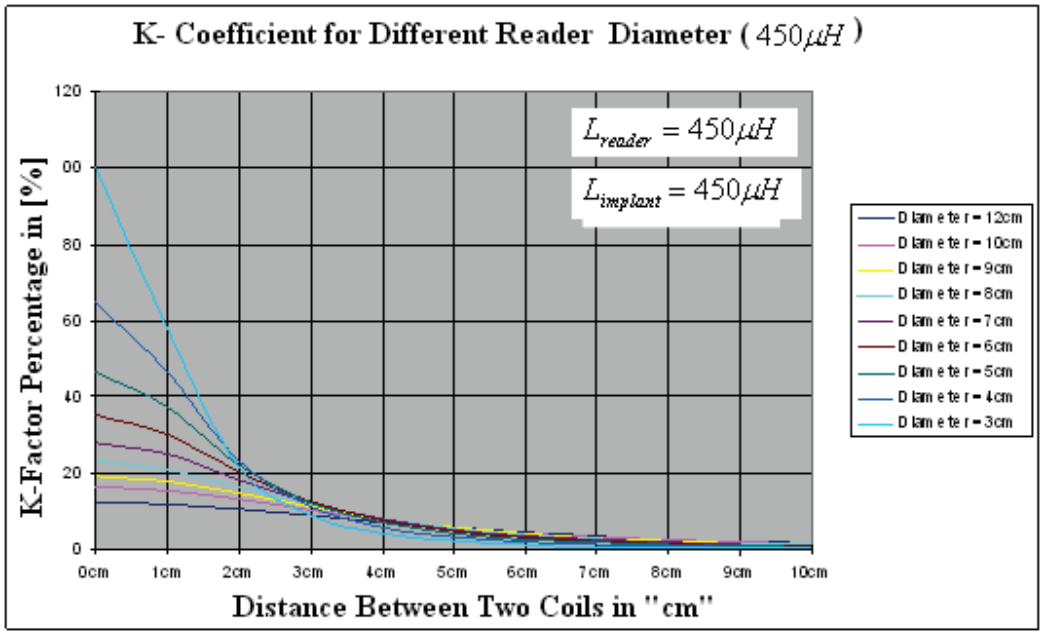


Figure (3.16) the coupling coefficient percentage between coils

L_{reader}	Coefficient K(5cm)		Mutual Inductance M(5cm)		$L_{implant}$
	Calculated	Measured	Calculated	Measured	
65.4 µH	5.68%	19.4%	3.58µH	12.4 µH	62.7 µH
95.5µH	6.90%	25.7%	5.10µH	15.8µH	95.6µH
350µH	5.350%	20.75%	16.5µH	25.9µH	350µH
459µH	5.809%	25.95%	26.5µH	39.9µH	453.8µH
550µH	8.60%	26.01%	18.90µH	125µH	556µH
650µH	6.70%	24.09%	24.95µH	250µH	655µH
933.1µH	8.95%	25.19%	30.01µH	150µH	953.1µH

Table (3.3) comparison of theory and measured values of the mutual inductance and coupling coefficient for inductive link at distance (5cm) for different inductances

3.1.3.3 Lab Measurements for Wireless Received Power

For comparison, the simulation and measurements were made to evaluate the optimum inductance value tuned at our choice carrier frequency 135 kHz. The testing was performed over various coils, the practical measurements were for the inductance between 62~650µH that demonstrates the optimum received power at 650µH. In the first condition, the reader coil was fixed at 64µH, whilst the better wireless received power was at 650µH at implant coil as shown in Figure (3.17). In second condition, the implant coil was fixed at 933.4µH, where the better wireless received power was at 657.6uH, as shown in Figure (3.18).

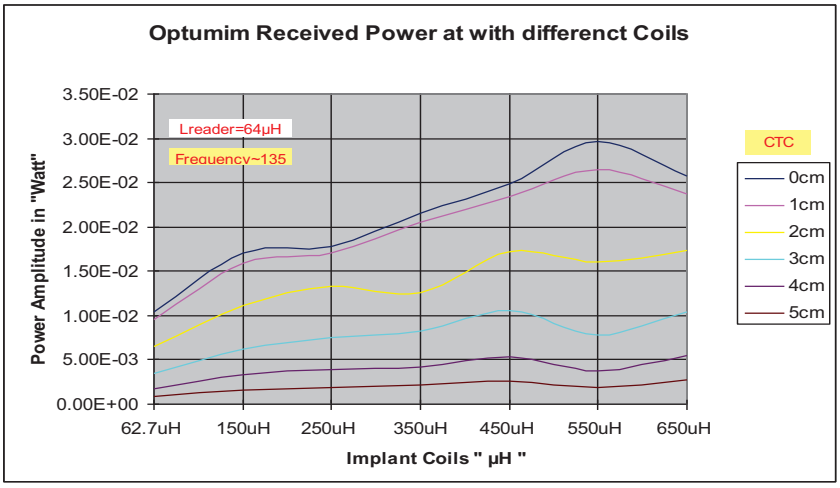


Figure (3.17) the best receiving power over different implant coils

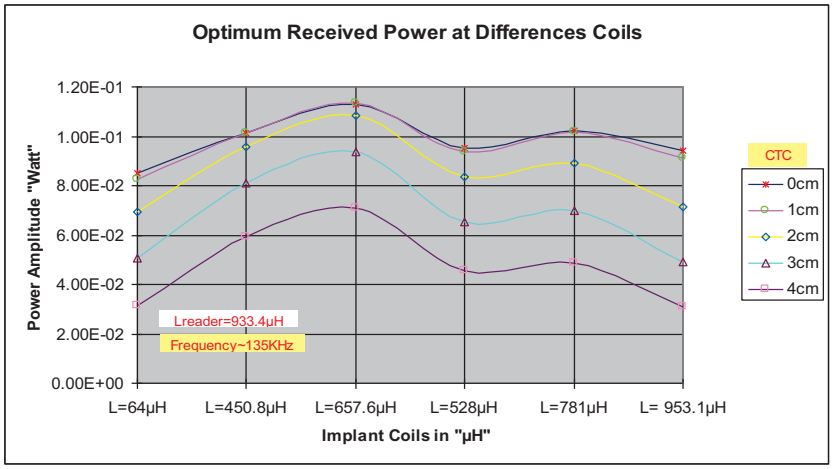


Figure (3.18) the best receiving power over different reader coils

From the previous measurements, we chose the coils values between 425~465µH for this work. These values were considered in the calculation for the best inductance value for the reader and the implant coils design. Figure (3.19) shows the load measurements and matching impedance for the implant-tuned circuit, which where tested under different loads from (50-20kΩ) over short distance up to 10cm. The second measurements were performed by selecting the coils driven with the power amplifier: the improvement area for the received power driven by Class F power amplifier was as shown in Figure (3.20), giving up to 0.95 Watt at 5cm.

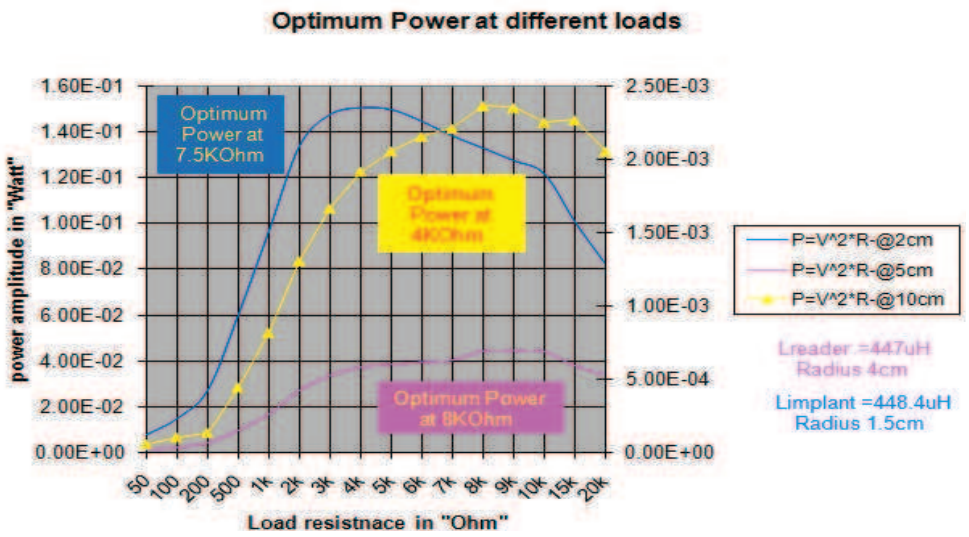


Figure (3.19) Measurements for maximum receiving power over different Loads

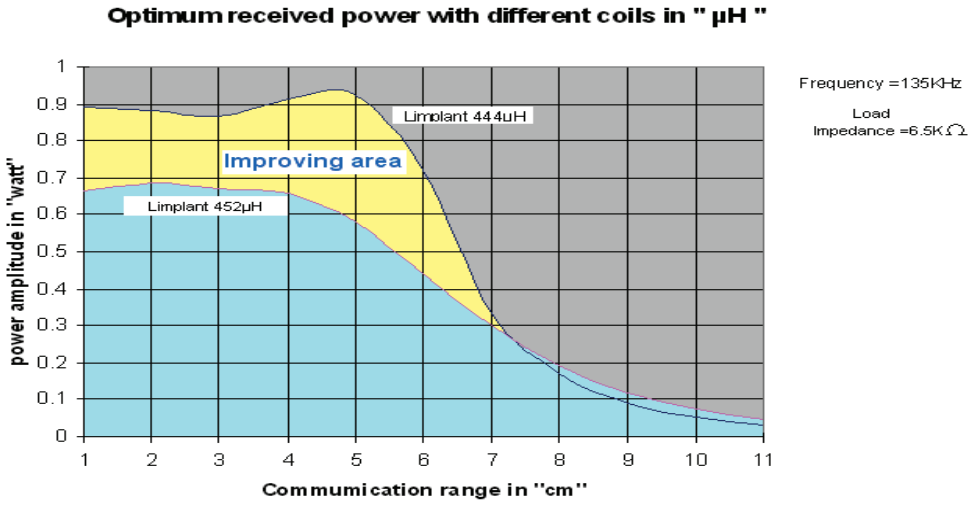


Figure (3.20) the improvement receiving power with driven with class F power amplifier

3.1.4 Misalignment Investigation for Inductive Link

Biodevice applications, which use magnetic coupling for communication, can suffer from many problems, such as short-range, loss of coupling and attenuated power. One of the main problems of the inductive coupling is the misalignment between coils. To achieve the best results, a high RF received power, and matched impedance is needed. In addition, the orientation angle for coils and the magnetic field is restrained by many factors, such as azimuth and elevation angles for the implant due to coil movement , which was studied for different rotating possibilities for implant coil angles (0°, 45°,) and (90°), as demonstrated in Figure (3.21). Generally, for reducing the misalignment between coils and improving the receive power, the suggested solution is to split the implant coils into two parts, as shown in Figure (3.22), as this that will harvest the most magnetic flux intensity.

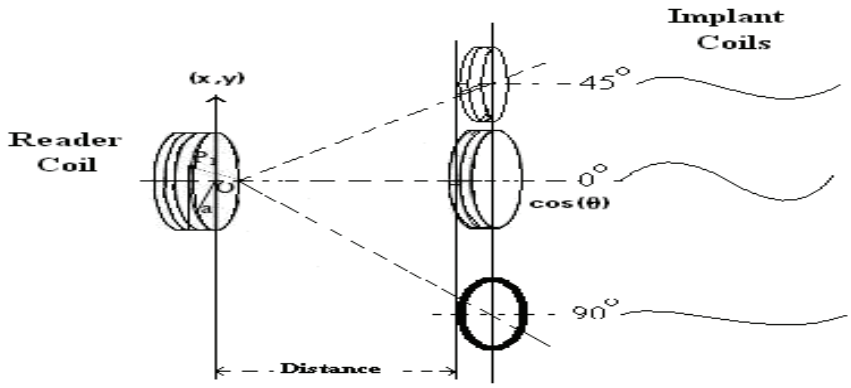


Figure (3.21) the misalignment analysis between two coils

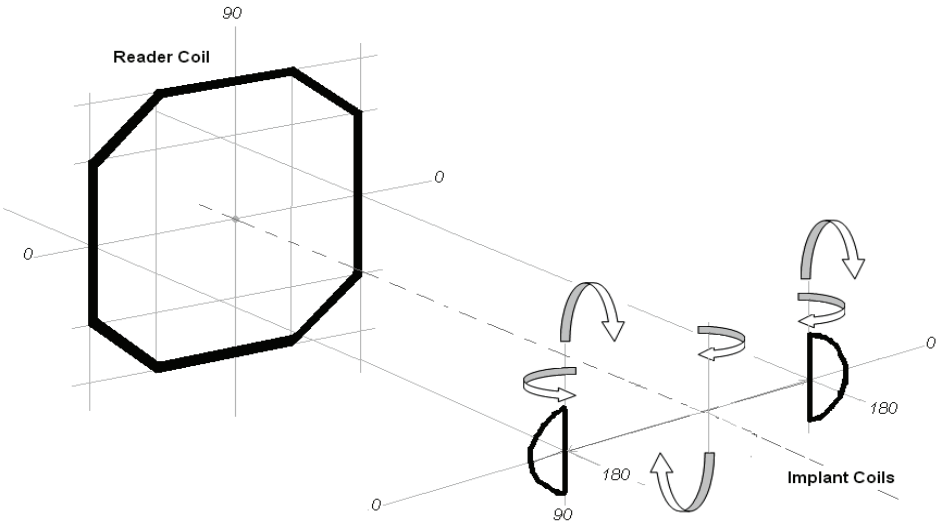


Figure (3.22) Optional solution for splitting the implant coils in to two parts

3.1.4.1 Misalignment Analysis and Lab Measurements

The prospective design in Figure (3.22) was analyzed and created into a circuit. The lumped equivalent circuit module for the reader and dual implant coils are shown in the Figure (3.23), where the magnetic coupling coefficient and the mutual coupling shared the transmitted magnetic flux from the coil reader. We analyzed these relations of magnetic coupling coefficients in mathematical form. By analysis of the coupling coefficient between three coils, the coupling relation between L_{reader} and L_{impl1}, L_{impl2} can expressed in the equation:

$$\frac{M_1}{L_{reader}} = \frac{N_{impl1}}{N_{reader}} K_1 \quad \text{and} \quad \frac{M_2}{L_{reader}} = \frac{N_{impl2}}{N_{reader}} K_2 \tag{3.62}$$

The mutual coupling relation of coil L_{impl1} and L_{impl2} is given by the equation:

$$\frac{M_3}{L_{impl1}} = \frac{N_{impl1}}{N_{reader}} K_1 \quad \text{and} \quad \frac{M_4}{L_{impl2}} = \frac{N_{impl2}}{N_{reader}} K_2 \tag{3.63}$$

From the above equations, we can substitute and get the mutual inductance between coils as:

$$\frac{M^2}{L_R L_{im1}} = K_1^2 \Rightarrow M_1^2 = K_1^2 L_R L_{im1} \Rightarrow M_1 = K_1 \sqrt{L_R L_{im1}} \tag{3.64}$$

$$\frac{M_2^2}{L_R L_{im2}} = K_2^2 \Rightarrow M_2^2 = K_2^2 L_R L_{im2} \Rightarrow M_2 = K_2 \sqrt{L_R L_{im2}} \tag{3.65}$$

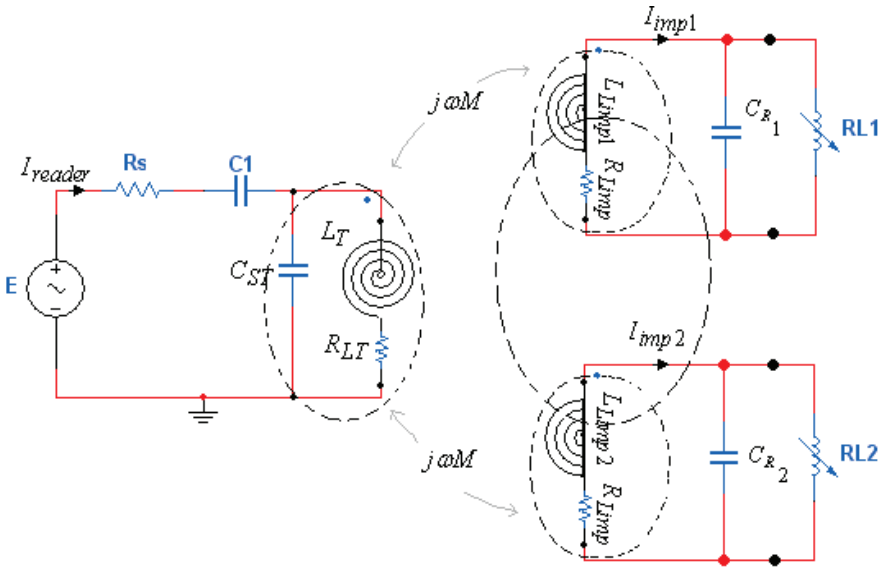


Figure (3.23) Lumped equivalent circuit with dual for inductive coupling module

Lab measurements were performed for the proposed coils as demonstrated in Figure (3.24), for misalignment, which are using two separated coils to test and improve the efficiency of wireless received power. Both coils A and B were identical 450.8µH, where the reader coil was equal to them in inductance ~ 950µH. The results shown in Figure (3.25) obviously indicate that the wireless received powers are constant and compensated by one of the coils, which provides a stable power at the implant. However, new techniques have been performed and are described in Appendix A.

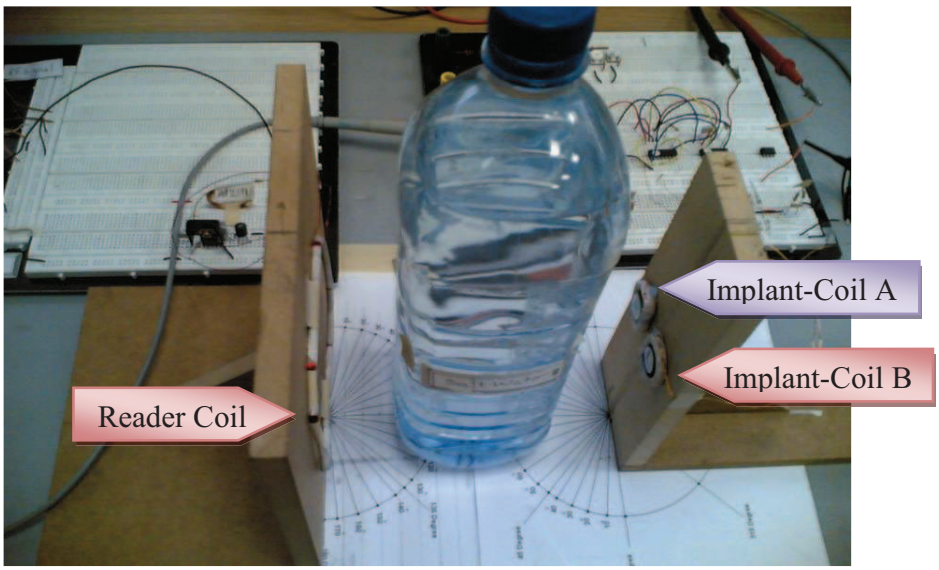


Figure (3.24) the RF inductive coupling lab measurements for dual coils

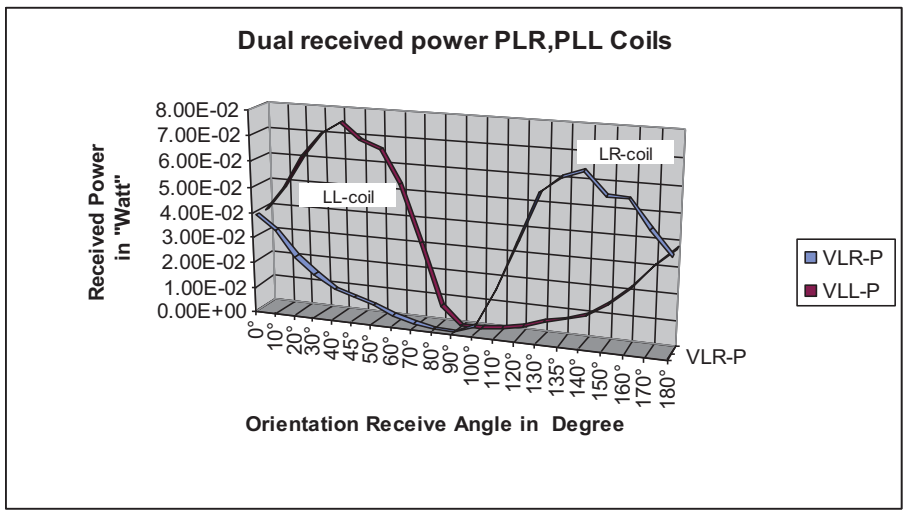


Figure (3.25) the RF inductive coupling Lab test for dual coils

3.1.5 Implant Coil Surgical Investigation

There are many uses for surgical implant devices inside the body, which are dependent on the device and the purpose. The epidermis of the body is sensitive to the exterior world, like heat, touch, etc. Coils for implants are inserted between epidermis stratums, which affects the absorption of electrical and magnetic energy. The high magnetic field ensures minimum local tissue heating exposure, and absorption by body organs, such the eye and the brain. The coils are carefully located at contorting less sensitive surgically safe areas. These factors are affected by the attenuation of the electromagnetic field through the patient's skin and therefore attenuation needs to be calculated with respect to frequency. However, this was discussed, in chapter one, in the absorption relation to frequency and the possibilities for minimum SAR. We illustrate in Figure (3.26) below the possibility of surgical implants and manipulating coil alignment, which use the same location for pacemaker devices that combine between the UHF and Low Frequency solutions.

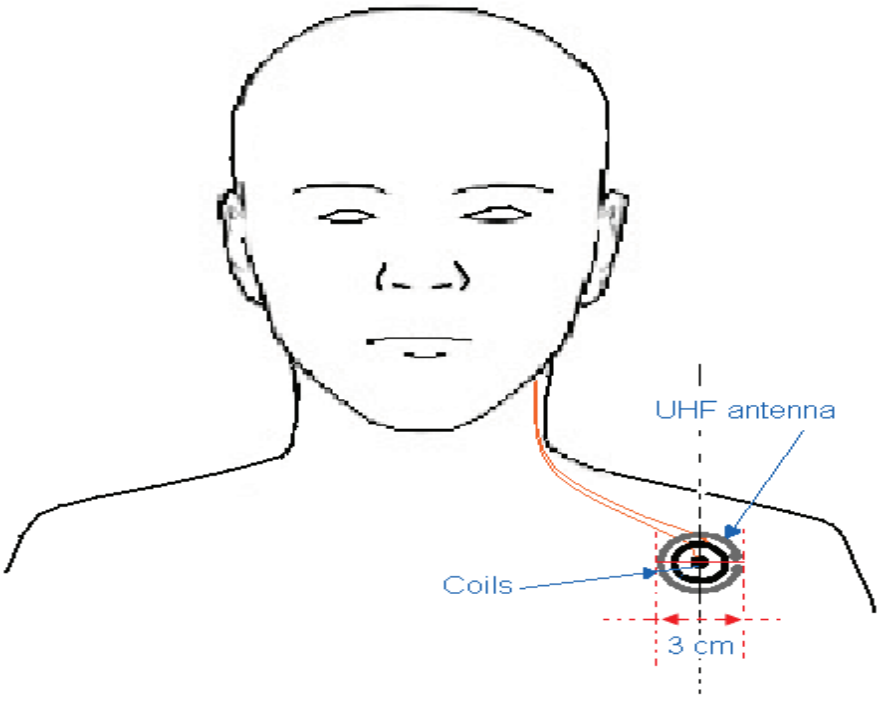


Figure (3.26) demonstrates the combined solution for implant coil location

Generally, the location of the implant is critical, and subject to the size and function of the device. For example, the pacemaker or brain implant device are located under the skin on the right side of the chest. The coils are carefully located at contorting less sensitive surgically safe areas, which includes considering the factors affected by the attenuation of the electromagnetic field through the patient's skin. However, we described in the Figure s (3.27), (3.28) and (3.29), the minimum possibilities of surgical implants and manipulation coils alignment respectively.

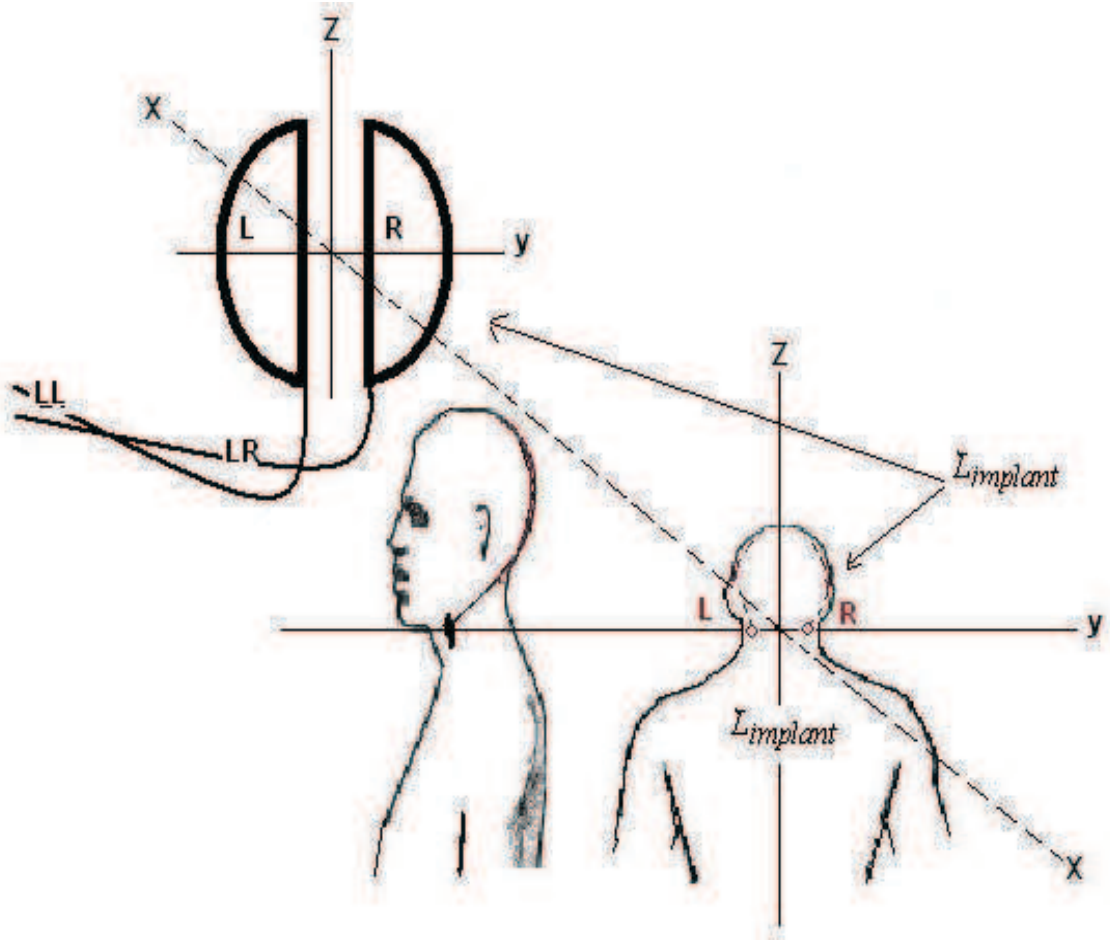


Figure (3.27) illustration of the first possibility for dual implant coils locations in the back

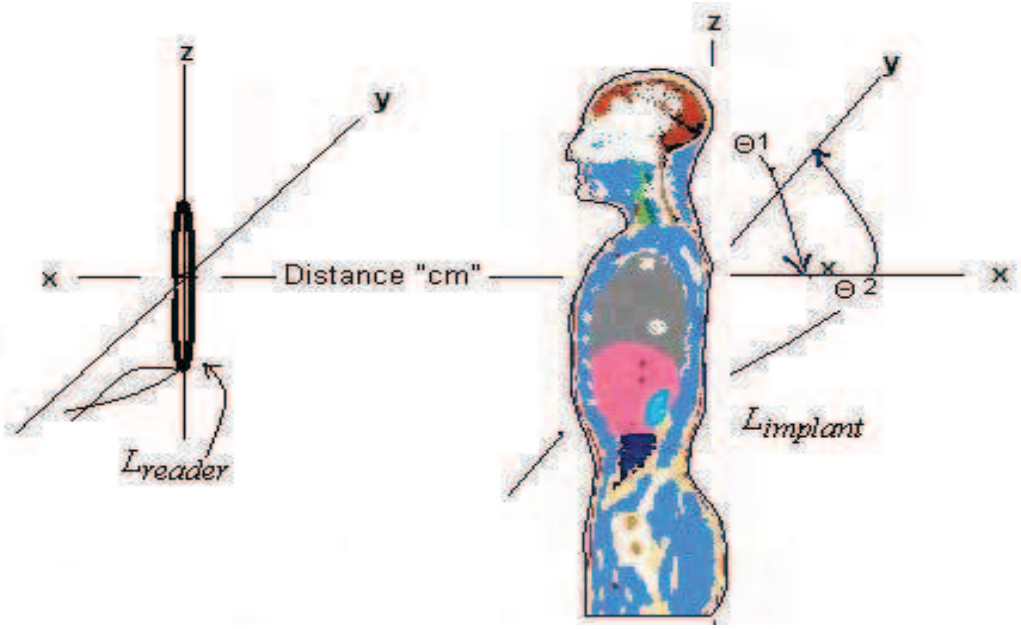


Figure (3.28) the second possibility for implant coils at the front

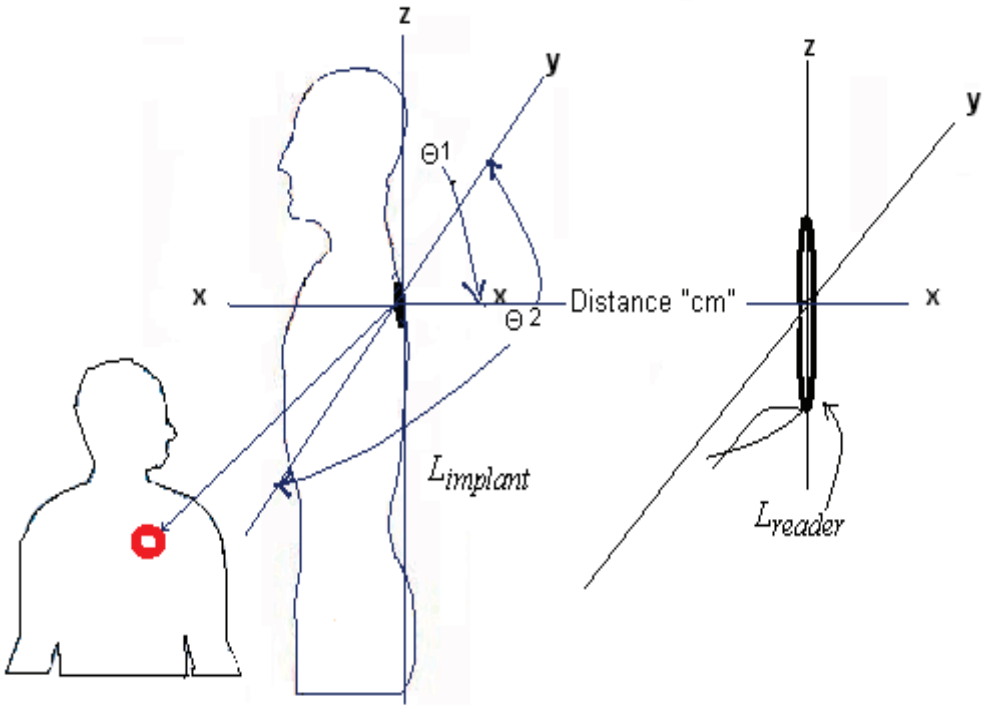


Figure (3.29) the third possibility for single implant coils on the back

3.1.6 Conclusion of Inductive Coupling Link

This chapter culminates with the key design in our work the inductive coupling link. A wide range of papers that have been published in this area have studied and investigated the inductive coupling link topologies, covering the coils theory simulation and evaluated measurements. The most important element of inductive coupling is how to design the appropriate inductor and choose the right value for optimum coupling with appropriate design for biomedical purposes. In practical measurement, it is noted that the spiral flat coil at the reader has spread the magnetic flux generated by the transmitter coil and gives less communication distance compared to other shapes, where it is appropriate in the implant part. The spiral coil harvests the electromagnetic field more than other shapes, described in this chapter and that offers stable DC voltage in the implant. The lab test measurements were evaluated with coils in the range 60µH~950µH; we obtained the best values for the reader coil between 425 µH and 650 µH. In addition, extra work and measurements was done for synthesis of a better coil at values 650µH~950µH in the reader section with different diameters and shapes.

The results were given for the optimum RF transmitted and perfect received power where the two coils are identical. However, the best coil is 450 µH for both reader and implant coils, at 10cm and 3cm in diameter respectively in this work. This provides the optimum performance with the power amplifier; in addition, the test measurement was performed to evaluate the characteristic of the implant coil under different loads, at different distances maintained over 5cm~10cm between coils. The bio-coil was evaluated for performance under conditions for implantation in water bearing (bottle) saline; where it was introduced between the two coils, this result in no loss of the power transfer. A saline water bottle was used to simulate the body environment. Extra investigation for inductive coupling link is described in appendix A.

The energizing and communication between the reader and implant moving as part of the body was accomplished through antenna coils. The efficiency of the transfer voltage can be increased significantly with the high Q of resonances circuits tuned at serial to parallel circuit. A second solution was synthesized for a tracking control system that auto adjusts for optimum condition for magnetic coupling and orientation of coils, which will be discussed in chapter five.

3.2 Power Amplifiers

3.2.1 Introduction to Power Amplifiers

The power amplifier plays an important role in low and high frequency bands. It amplifies the input signal to a certain power level, which drives the transmit circuit. The power efficiency is one of the key factors in the design of the power amplifier (PA). Ultimately, when it comes to the power efficiency class E and F, amplifiers have a better output efficiency compared to these conventional amplifiers, such as class A, B, C, and D [180]. A concise comparison of the efficiency between different types of power amplifiers is shown in table (3.2.1). However, we studied the principles of the power switch amplifiers that have been designed and which are appropriate for the biomedical purpose. Generally, the class ***D*** power amplifier is a switching amplifier that converts a low-level analogue input signal into a high power, and it consists of three main stages: the input switching stage, the power amplification stage, and the output filter stage, as illustrated in Figure (3.30). To achieve this technique a Pulse width modulation (PWM) takes the input signal, and converts it into a higher (triangular waveform) switching waveform, which uses a comparator. When the voltage at the inverting input is bigger than at the non–inverting input, the output voltage is low, and when the voltage at the inverting input smaller than that at the non-inverting input, the output voltage becomes high [125]. In addition, the PWM technique was used in the control part in our work in chapter five. Finally, the output of the comparator was connected to the power amplification stage; this was an external MOSFET in a full-bridge configuration. The MOSFET was either full ON or full OFF and the power dissipation was minimal, allowing maximum power to be delivered to the TX circuit. The switch frequency was much higher than the input signal band, which allowed high frequency out-of-band.

Power Amplifier Types	Efficiency
Class A	~ 35%
Class B	~ 50%
Class C	~ 65%
Class D	~ 80%
Class E	~ 90%
Class F	~ 95%

Table (3.2.1) comparison of the class power amplifier's efficiency

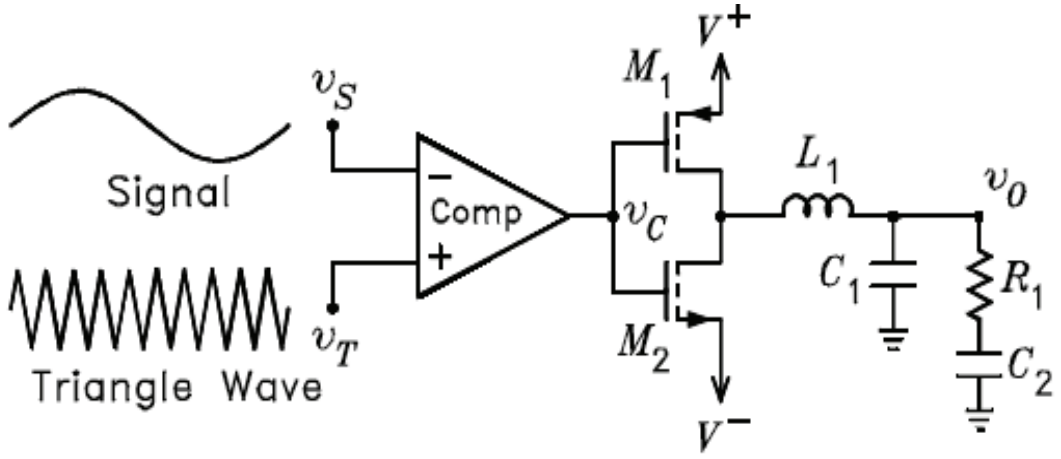


Figure (3.30) illustrating the principle of Class D power amplifier

The output stage had a passive filter to remove high and spurious frequencies. In addition, this passive load network was designed to minimize current and the voltage overlapping.

3.2.2 Class (E) Theory and Design

In general, class **E** power amplifier technique is commonly used in wireless power transmission for biomedical and biotelemetry applications. The implant system needs a highly efficient power amplifier to transmit the RF power signal, which modulates according to the control information from the reader, into the implant device. Hence, the class **E** is a more suitable PA as an element driver for the transmitter coil, with theoretical 100% efficiency (only ideal switch): the actual efficiency is about 90~ 95% [145]. A simple class E consists of a single pole MOSFET transistor switch with a shunt capacitor $C1$ parallel with series circuit R1, L1, C2 that achieves a constant current from the supply source. Furthermore, rising and falling voltage waveform is required for PA operation. In addition, it added the parasitic drain source capacitor of the MOSFET transistor C_{ds}. The periodic pulse signal or PWM circuit that drives the MOSFET transistor is demonstrated in Figure (3.31). The high efficiency of class-E can be achieved by reducing the transistor switching losses; the transistor is turned ON when the drain voltage has come back to zero, reducing the turn ON loss zero voltage switching. The drain voltage is also raised from zero at the time of turn ON, which allows for slight returning without losing efficiency. These two above states are the operation for PA presented in Figure (3.32), which describes the waveforms of the voltage and the current in switch time [146].

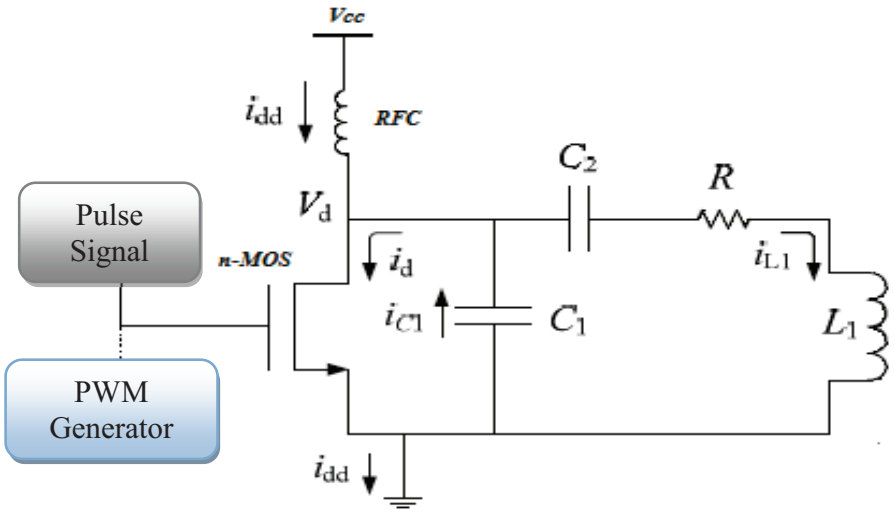


Figure (3.31) the principle circuit of the Class E amplifier

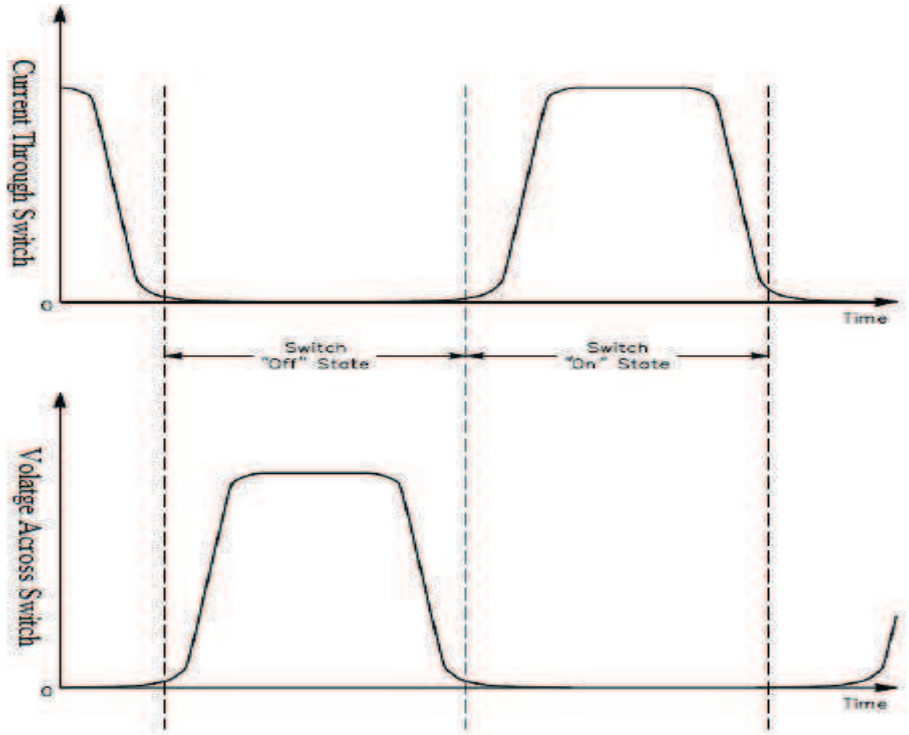


Figure (3.32) waveforms of the voltage and current switch conditions [145]

For the design of the Class-E amplifier consider the switch Q is OFF and the voltage (V_q) can be expressed as:

$$V_q(t) = \frac{I_d}{\omega_s C_q}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)) \tag{3.66}$$

Where (ω_s) is the carrier frequency, (I_d) is the dc portion of the drain current, and (a) is constant, the voltage (C_q) is given by solving the equation:

$$C_q \frac{dV_q}{dt} = I_d(1 - a\sin(\omega t + \phi)) \tag{3.67}$$

In order to avoid power dissipation due to either shorting of the capacitor, or voltage drop, which is crossed it, during the switching or when the MOSFET turns ON. For the switching transistor there are two other conditions can be declared as.

$$V_q(\frac{T_s}{2}) = 0 \qquad and \qquad \frac{dV_q}{dt}(\frac{T_s}{2}) = 0 \tag{3.68}$$

Using the equations to solve for the constants, these have been calculated as below:

$$a = \sqrt{1 + \frac{\pi^2}{4}} \approx 1.862 \quad and \quad \phi = -\arctan(\frac{2}{\pi}) \approx -32.48^0$$

The capacitor voltage (V_q) and it is current (I_d) can be defined as:

$$V_q(t) = \frac{I_d}{\omega_s C_q}((\omega_s t) + a(\cos((\omega_s t) + \phi) - \cos\phi)) \qquad in \quad 0 \le \omega_s t \le \pi \tag{3.69}$$

$$V_q(t) = 0 \qquad in \quad 0 \le \omega_s t \le \pi \tag{3.70}$$

$$I_q(t) = 0 \qquad in \quad 0 \le \omega_s t \le \pi \tag{3.71}$$

$$I_q(t) = I_d(I - a\sin(\omega_s t + \phi)) \qquad in \quad \pi \le \omega_s t \le 2\pi \tag{3.72}$$

From the above equations (3.69) and (3.72), we can calculate the load impedance at the resonance frequency as:

$$Z_l = \frac{V_{ql}}{i_{ql}} = \frac{0.28}{w_s C_q} e^{j49^0} \tag{3.73}$$

According to the circuit R_{load}, L_1, C_2 at the power amplifier, Figure (3.33) shows the principal load circuit of the network, which can be analyzed as a series input impedance for

simplifying the calculation. Eventually, the load impedance of the impedance network circuit can be mathematically calculated as:

$$Z_{load} = j\omega_s L_{load} + \frac{1}{jw_s C_{load}} + R_{load} \tag{3.74}$$

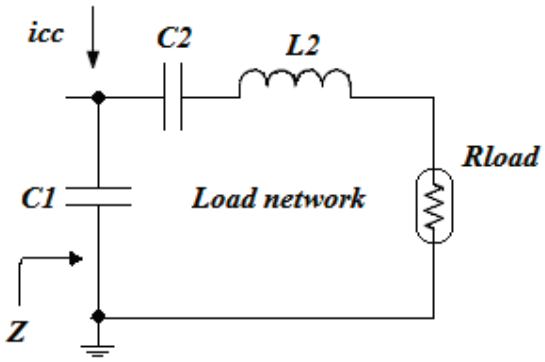


Figure (3.33) the load network circuit of Class-E PA

The component values of the load network can be obtained by matching the real and imaginary parts of the equations (3.75) and (3.76) respectively:

$$C_q = \frac{1}{2\pi f_0 R(\frac{\pi^2}{4}+1)(\frac{\pi}{2})} \qquad and \qquad L_{load} = \frac{Q_L R}{2\pi f_0} \tag{3.75}$$

The choke inductor RFC can be expressed mathematically as:

$$L_{RFC} = \frac{1}{(k\omega_s)^2 C_q} \tag{3.76}$$

where the ***k*** factor is the resonant ratio, to obtain a high power output drain efficiency, we can choose the value of the quality factor of coil (***Q***=100), and the value of (***k***=1.412). However, the quality factor of the load network affects the bandwidth of the RF transmitting signal at the reader. According to these facts, we can write the equation to calculate the values of CE-PA circuit, the load network component as:

$$L = 0.732\frac{R}{\omega} \quad and \quad C = \frac{0.685}{\omega R} \tag{3.77}$$

$$L_0 = \frac{1}{\omega^2 C} \quad and \quad C_0 = \frac{1}{\omega R Q_L} \tag{3.78}$$

The Quality factor of a self-inductance can be obtained by the equation below:

$$Q_{Coil} = \frac{\omega L_0}{R_{Coil}} \tag{3.79}$$

The Quality factor of the tuned circuit (Load Network) can be obtained by the equation below as;

$$Q_{network} = \frac{\sqrt{\frac{L_2}{C_1 + C_2}}}{R} \tag{3.80}$$

We substitute the values in the equations (3.79) and (3.80), where the carrier centre frequency is working at (135 KHz). This gives the elements values for Class E-PA circuit tabulated in table (3.2.3) to compare between the theory and measured values. In practice the internal resistance of the coil (R_{Coil}) is added in the calculations of the R-value.

	L	**C**	C_o	L_o
Calculated values	$150\mu H$	25nF	3.08nF	$450\mu H$
Simulated values	$150\mu H$	23nF	2.8nF	$450\mu H$
Measured values	$150\mu H$	32nF	3.7nF	$460.8\mu H$

Table (3.2.2) shown the values of CE-PA

3.2.3 Class (F) Theory and Design

The second PA is the class **F** that is commonly used to amplify the RF signal, which is given a high efficiency and low power consumption and dissipation: it can achieve a higher power compared to other traditional class amplifiers [35] [32]. The fundamental operation of a class **F** amplifier is similar to Class **E** PA as a switch power amplifier. The input square wave signal drain voltage is rich in odd harmonics, predominantly the 3rd and 5th harmonics that resonate at ($3 f_0$ and $5 f_0$); the tuned filter network will remove the odd harmonics and the output RF signal, that provides a sine wave. Generally, it consists of three parts, the input matching circuit, switch transistor, and RFC filter network circuit. The output filter is used to control the harmonic content of its drain voltage or drain current waveforms thereby shaping them to reduce power dissipation by the transistor, thus allowing removal with a simple filter. The passive load network is designed to minimize current and voltage overlapping and for overall efficiency, the switch frequency is much higher than the input signal band, which allows high frequency out of band components to be removed with a simple filter.

The architecture of class **F** power amplifier circuit has been shown in Figure (3.34).

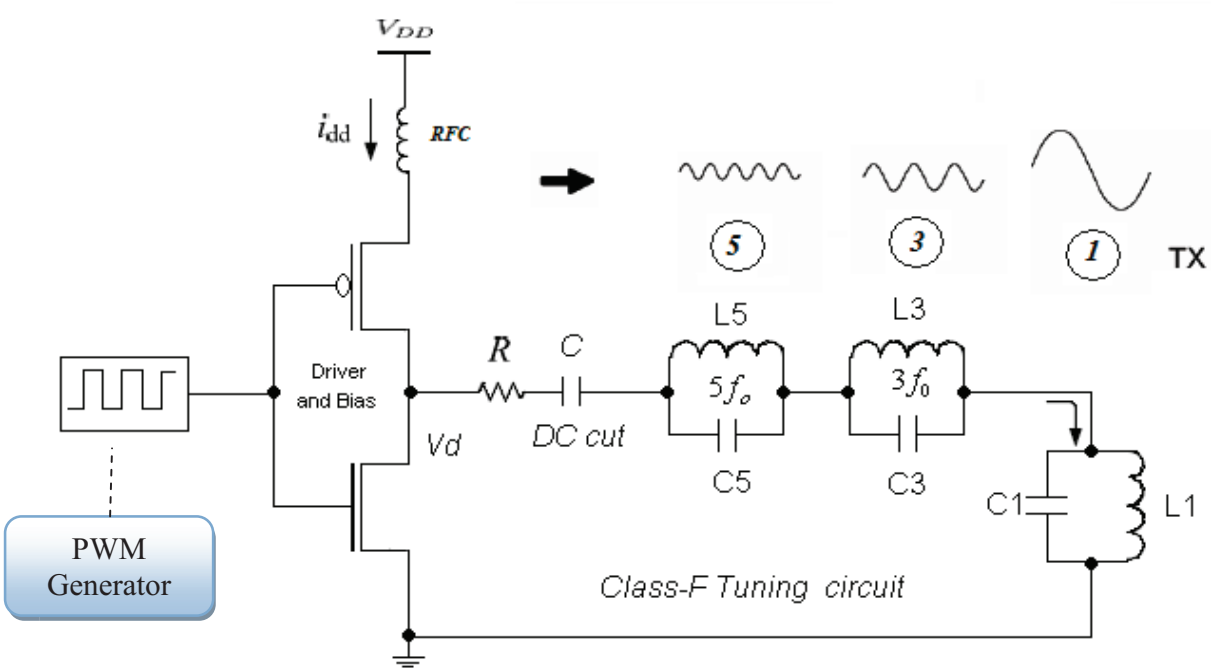


Figure (3.34) the principle components of Class **F** amplifier circuit

The tuned circuit at the fundamental resonance can be defined in the mathematical expression as the **L1C**2 tuned at central frequency. However, the power amplifier components can be defined in the mathematical expression as:

$$L_N = \frac{L_1}{2N-1} \tag{3.81}$$

$$C_N = \frac{C_1}{2N-1} \tag{3.82}$$

The 3rd Harmonic can be calculated for the tuned circuit as:

$$L_2 = \frac{L_1}{3} \tag{3.83}$$

$$C_2 = \frac{C_1}{3} \tag{3.84}$$

The fundamental **LC** tuning tank circuit can be calculated for the tuned circuit as:

$$L_1 = \frac{R}{\omega_0 Q} \tag{3.85}$$

$$C_1 = \frac{Q}{\omega_0 R} \tag{3.86}$$

The accurate removal harmonics from the input square wave signal gives the accurate sine wave output form with the LC tank circuit components. The transmitter coil voltage and the current in Figure (3.38) can be defined as:

$$V_{Coil} = \frac{2V_{DD}}{\pi} \sin \omega_c t \tag{3.87}$$

$$I_{Coil} = \frac{2V_{DD}}{\pi..R} \cos \omega_c t \tag{3.88}$$

The power consumption estimation for the coil driver can be given in a mathematical equation as:

$$P_{Carrier} = \frac{8}{\pi^2} \frac{V^2{}_{DD}}{4.R} . \sum_{K=N+1}^{\infty} \frac{1}{(2K-1)^2} \tag{3.89}$$

3.2.4 Automatic Frequency Control for Class F Power Amplifier

3.2.4.1 Method (A)

In practice, there are different methods which can be implemented for monitoring the RF transmitter, using the feedback control techniques. There follows a design of a simple control system to auto-correct the RF signal using VCO frequency that offers the stability of output power, for Class F- PA. It provides constant voltage at the implant device. This method is simple to implement for reducing the reader Hardware. The feedback system consists of an amplifier for the RF signal passed through a square circuit (multiplier) filtered at the centre frequency. The RF signal is converted into the digital signal, which converts the captured transmit signal into the digital form. The phase comparator is used to compare the digital TX signal with respect to the fundamental transmit pulse signal by VCO. We selected the PLL (HEF4046) [211], for synthesis of the fundamental frequency oscillation square signal at 135 kHz, the basic proposed control system using PLL techniques is shown in Figure (3.35).

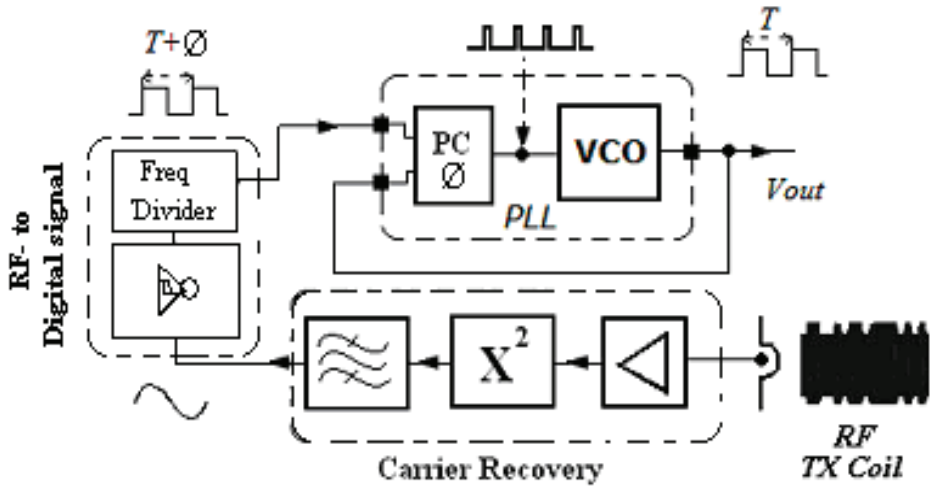


Figure (3.35) the proposed Feedback Control block diagram for Class-F- PA

Therefore, to analyse the feedback interface signal to VCO, we defined the phase comparator K_d and VCO K_0 signals, and the output $e(t)$ error pulse phase difference, as demonstrated in Figure(4). The mathematical analysis can be expressed in equation (3.36).

$$e(t) = r(t) \times y(t) \tag{3.90}$$

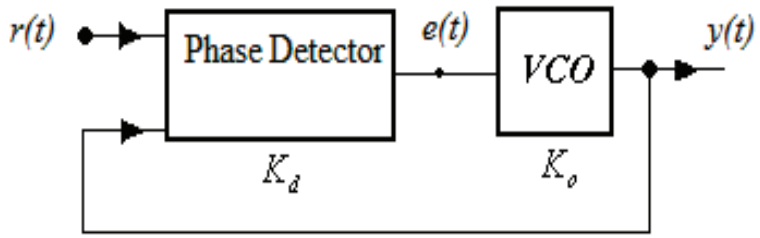


Figure (3.36) showing the analysis feedback signal for PLL –VCO

3.2.4.2 Method (B)

The misalignment in reader coil or the shifting in fundamental frequency at the transmit reader effects are respectively, that it affects the received power and reduces the efficiency of the implant device. In this work, we have introduced the PWM techniques, used in class **D** power amplifier. This technique could be useful for auto-RF frequency correction for transmitting RF power. There are two different techniques for generating a PWM signal, with the microcontroller

and programmed VHDL code in FPGA; both proposed methods are for designing a robust controller for class **E** power amplifier with PWM. However, we can compare this to the conventional methodology using PLL–VCO for transmitting amplified RF signal. The modified block diagram in Figure (3.34) for the Class-**F**- power amplifier is shown in Figure (3.37). The pulse width of the PWM waveform varies proportionally to the input signal and the output voltage signal. A Class-F PA controller adjusts the supply voltage of the Class-**F** power amplifier. The output voltage of the controller is equal to ($V_s = D_c \times V_{cc}$) where the duty cycle (D) of the PWM pulse is controlled by the PWM generator which is proportional to the RF input signal. However, the application of this facility in microcontroller for generating the PWM signal offers flexibility for updating the data and auto-correction for PWM signal output and the stability for the RF power amplifier. Significantly, that improves the implant performance condition, which is the main goal for our proposed work. The practical implementation and the discussion for controlling concept of feedback with PWM will be covered in chapter Five.

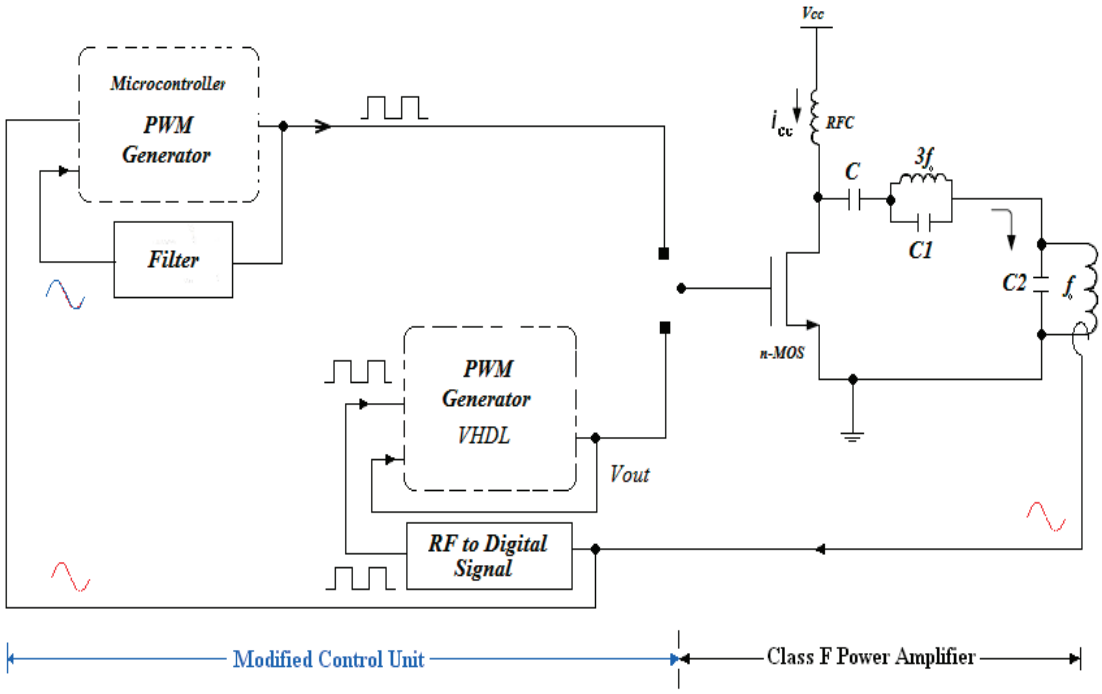


Figure (3.37) modified the block diagram of the Class-F- power amplifier

3.2.5 Simulation and Lab Measurements for Power Amplifiers

A. Simulation of Class-E Power Amplifier

The module of class **E** power amplifier was simulated with the MATLAB/Simulink environment, for evaluating the performance of the CE-PA. This is illustrated in Figure (3.38), where the carrier frequency located in this work is 135 kHz pulse signal, with a constant drain supply voltage at 5V. Eventually, for simulating the power amplifier in MATLAB/Simulink, the transfer function of tank circuit needs to be evaluated, and this can be expressed in the transfer function in equation (3.91).

$$\frac{V_{out}}{V_{input}} = \frac{[S^3 LC_1 + SRC_1 + C_1/C_2 + 1]SC_1}{R + SL + 1/SC_2} \tag{3.91}$$

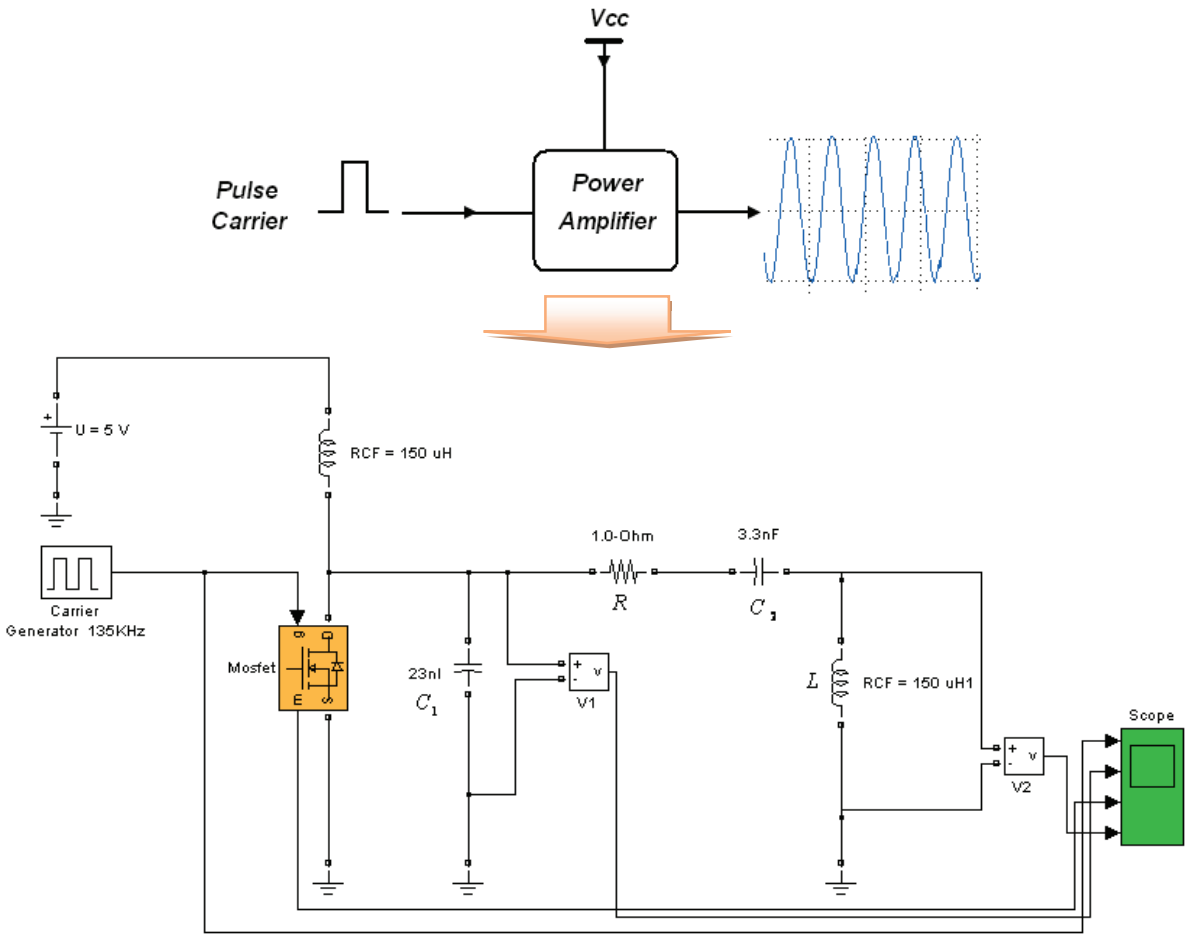


Figure (3.38) the simulation of Class-E- PA with MATLAB/Simulink

B. Simulation of Class-F Power Amplifier

The module of the class **F** power amplifier was also simulated with the same tools MATLAB/Simulink environment, for evaluating performance for CF-PA as demonstrated in Figure (3.39) the carrier frequency is the same as class **E**, which is 135 kHz. The simulation waveforms results are shown in Figure (3.40); the top signal is the input pulse signal oscillating at 135 kHz, where the bottom is the output of PA.

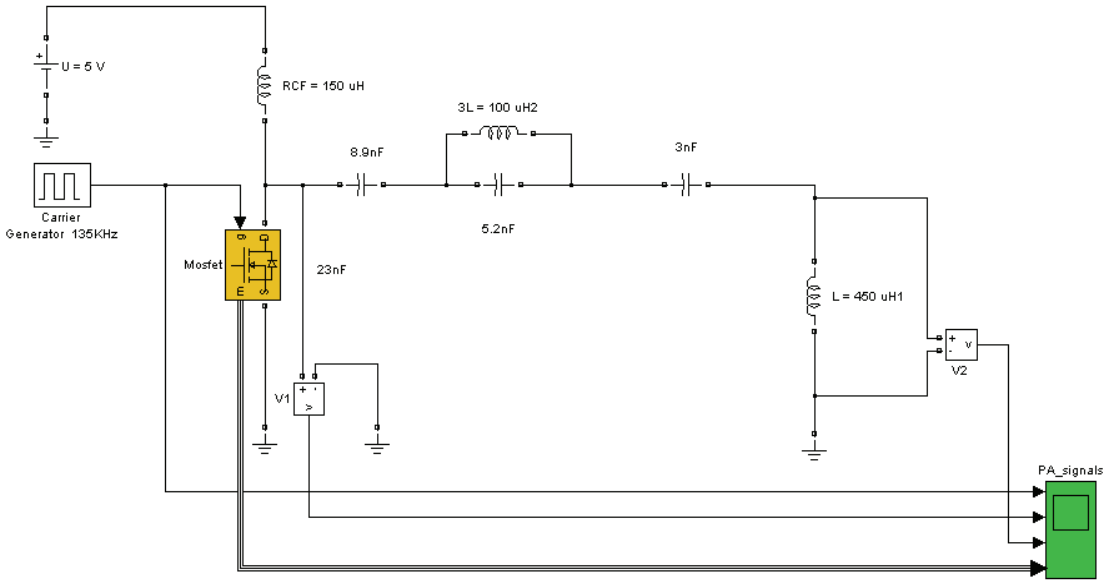


Figure (3.39) Showing the simulation of Class-F- PA with MATLAB/Simulink

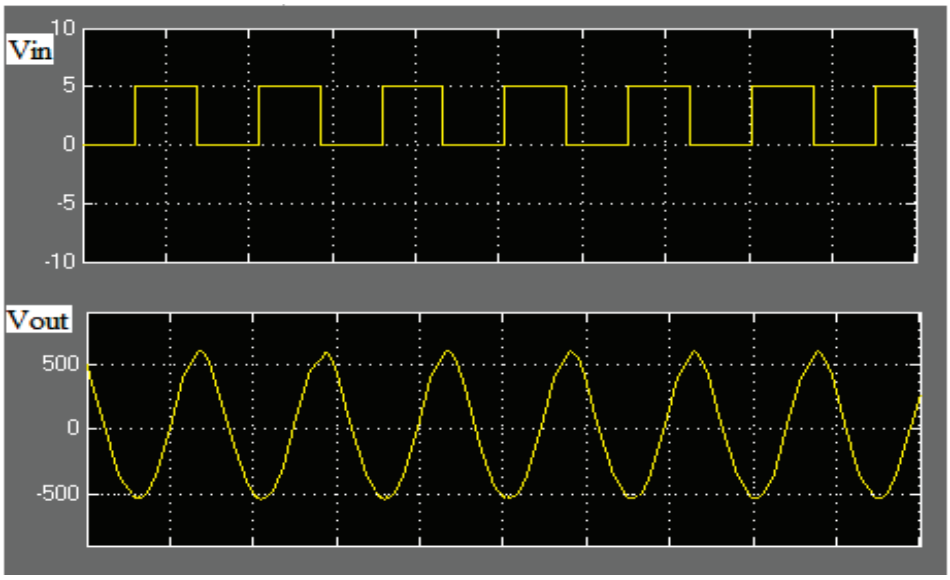


Figure (3.40) showing the simulation result waveform of Class F –PA at Frequency 135 kHz

C. Lab measurements of the Class-E Power Amplifier

This section provides the measurements which were collected using prototype Class E-PA, designed and tested for comparing the performance with the simulated Class E-PA results. The simulation waveform result for the class E-PA is shown in Figure (3.41), where the tuned carrier frequency is approximately between 133~135 kHz, with amplitude (340 V_{PP} or V_{rms} 120V) at the drain supply voltage constant at 5V. However, the simulation waveform result is shown in Figure (3.42) for the output power amplifier at the reader coil, where the measured transmit, power in this case is (2 Watt).

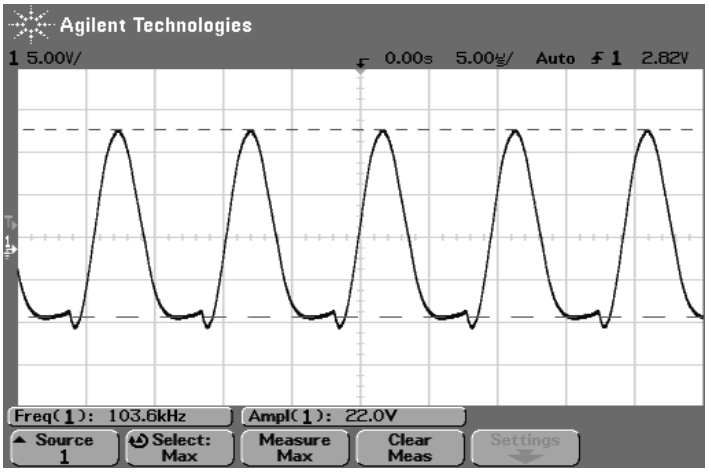


Figure (3.41) the switch (Transistor) voltage of the power amplifier

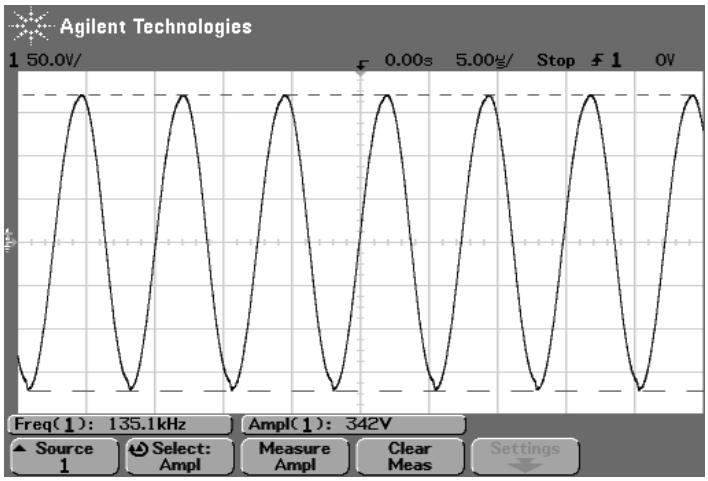


Figure (3.42) the output voltage of Class-**E** power amplifier

D. Lab measurements of the Class-F Power Amplifier

The second measurement for our proposed prototype power amplifier was Class E-PA. It has been tested using an Agilent scope and spectrum analyzer in order to analyse the parameters of the RF transmitted signal with the measurement waveform result, shown in Figure (3.43); the spectrum of transmit signal is demonstrated in Figure (3.44). The tuned carrier frequency is approximately ~134 kHz, with RF amplitude at (397 V_{PP}) or (140 V_{rms}), where the lab measurement output for transmitted power is approximately (3Watt).

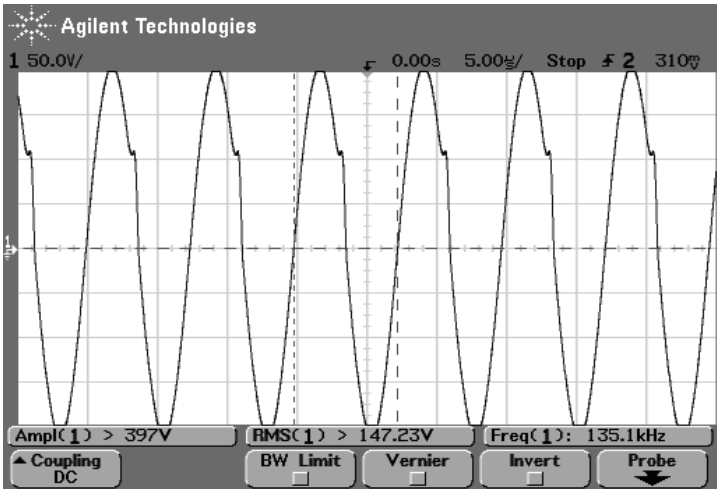


Figure (3.43) the output voltage of Class-F power amplifier at reader coil (Tx RF signal)

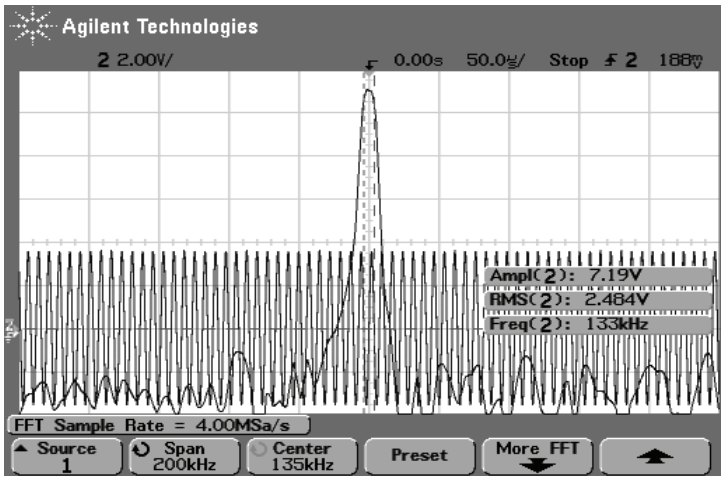


Figure (3.44) the spectrum of carrier frequency at 135 kHz

3.2.6 Comparing Measurements Results for Power Amplifiers

The class **E**-PA and classes F-PA influenced the practical measurements for wireless received power at implant, as shown in Figure (3.45). The transmitted power for Class F-PA compared to Class E-PA was slightly improved at the implant device, where the range communication distance also improved. The second measurement was performed to test the monitor control system for RF power amplifier, which was compared with and without frequency control circuit as demonstrated in Figure (3.46).

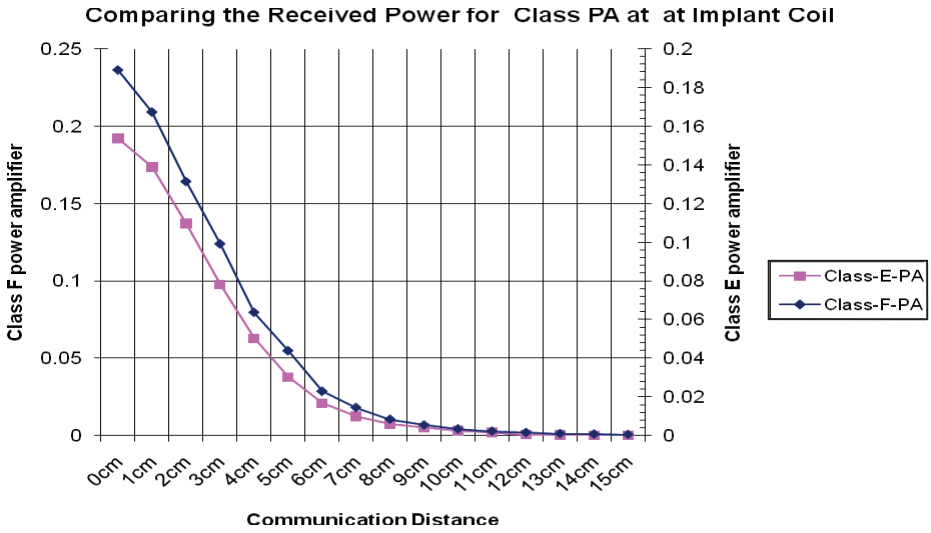


Figure (3.46) the comparing of received Power between Class **E** and **F** power amplifiers

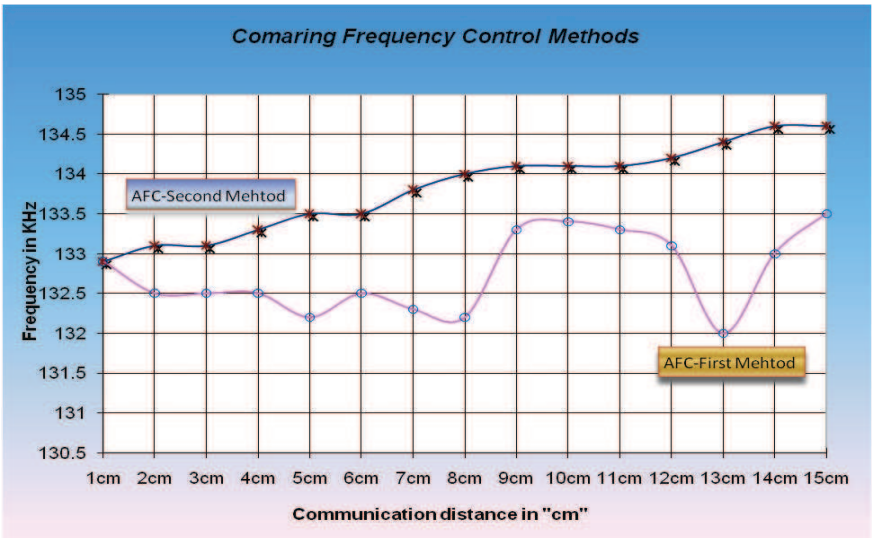


Figure (3.47) the comparison of AFC control systems for Class PA

3.2.7 Summary of Power Amplifiers

This section concludes with a summary of the second important element, which is the power amplifier. We reviewed the most common power amplifiers used in wireless applications such as RFID. Our main goal was to synthesize a highly efficient amplifier, which is reliable for medical purposes. Eventually many parameters have to be considered in the design such as the temperature, frequency stability and maximum transfer power. We chose the switching power amplifier in our work, as it was appropriate for the applications in this thesis. Principally, we studied and investigated the most common switch power amplifiers in detail and simulated them with MATLAB/Simulink tools. However, the two-switch power amplifiers class-**E** and class-**F** were selected by combining these two power amplifiers in a hybrid design, to reduce the hardware layout and improve the performance efficiency of the transmitter power amplifier. The first prototype for the feedback control system was synthesized with the PLL technique; additionally circuits were designed to convert the transmitted RF signal into a digital RF signal. We introduced the PWM techniques to control the transmit RF-signal using the microcontroller or FPGAs to generate the pulse width modulation pulse width. Generally, the full details for hybrid power amplifier design and controller circuits will be explained in chapter five. The preliminary measurements for RF power amplifier without controller showed instability at the reader coil. The frequency was changed with respect to distance, especially when the coils were moved closer together (1-2cm apart), where the carrier frequency shifted from 135 kHz up to 142 kHz. In addition, from the measurement we obtained the results that the power amplifier was also affected by this movement objective around the transmitter coil, or any other coupled coil near it.

Finally, a summary of the measurements for our proposed chosen switch power amplifiers. Shows that the first amplifier is class **E,** which is used for transmitting ASK signal, whilst it provides the essential power for the implant device. The second proposed PA is class **F,** which is synthesized for providing the RF power signal for the implant device. The implant received continuous RF power from both amplifiers, according to the transmit data from the reader.

3.3 Implant Received Power Simulation and Measurements

3.3.1 RF-DC Received Power Investigations

A wireless inductive coupling link is a common way for communication via electromagnetic fields in biomedical telemetry. It transfers the RF power and data wirelessly between reader and a battery-less implant [82], [100]. The biomedical devices require very efficient RF signal converter or rectifier into DC voltage, which provides the essential DC voltage for medical sensors or electronic circuits. Predominantly, the essential required voltage for the sensors and electronic device are delivered to the implanted unit by RF transmitted signal, over a short distance of a few centimetres. However, the most common technology used a signal diodes rectifier or MOSFET transistors in bridge rectifier connection. We investigated most of the circuits, which are designed with passive devices, and tried to mathematically analyze and simulate them. The appropriate rectifier circuit design for biomedical device "microcircuits" as studied. In addition, the matching impedance between the tuned circuit and rectifier circuit was the main reason for loss of power, which reduced the stability and the variation of the response time of the rectifier. However, there were further factors contributing to the loss of power such as misalignment of coils and detuned antenna at the carrier frequency, increase of the reading distance, and poor circuit design. The block diagram in Figure (3.55) shows different circuit types used for power rectifying based on wireless communication, or RFID and the biomedical implant devices topologies.

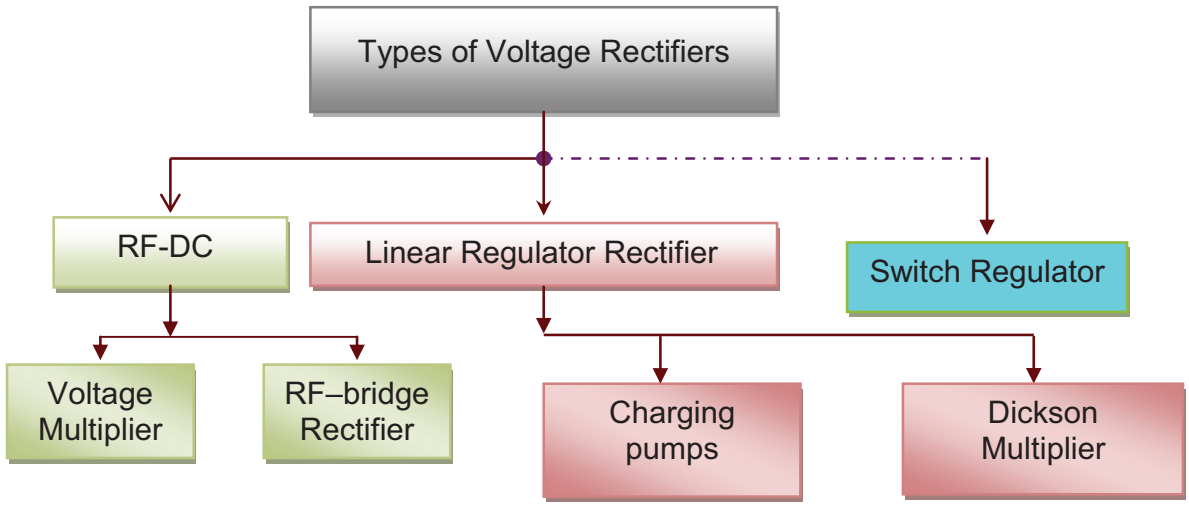


Figure (3.55) illustrates the different types of power rectifying topologies applied for biomedical device

3.3.2 Voltage Multiplier

There are many passive techniques using the voltage multiplier (VM) which double the output voltage and stabilize it. There are different circuit topologies for performing the VM: the most common type of voltage multiplier is the half-wave series multiplier, and it is called the voltage Doubler or voltage Tripler [153]. Generally, the basic VM circuit is composed of capacitors and diode connected in several stages as a network, to step up the voltage amplitude in passive devices and rectifies the RF signal from AC to DC voltage, as shown in Figure (3.56). However, this technique is not suitable for all the biodevices applications, because the capacitors and diodes sizes consume a large space in the implant circuit. In addition, the stability and DC voltage out is not appropriate as a wireless source for circuits in passive implant devices.

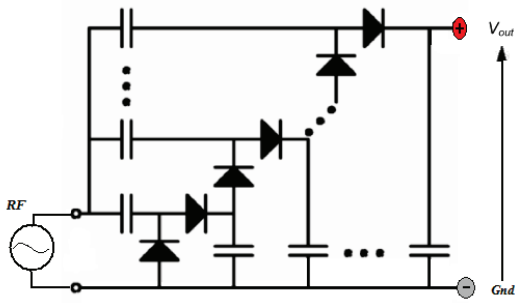


Figure (3.56) the voltage doubler circuit [153]

The circuit in Figure (3.56) was developed and modified to use the N-MOSFETs, designed for passive RFID tags in the metal CMOS technology [178], [154]. One of the disadvantages in this topology is that it is not appropriate for far field communication and the power loss in the voltage multiplier is unavoidable. However, the efficiency of the VM so far reported is about 15%~30%, which is a result of conduction loss and dynamic loss.

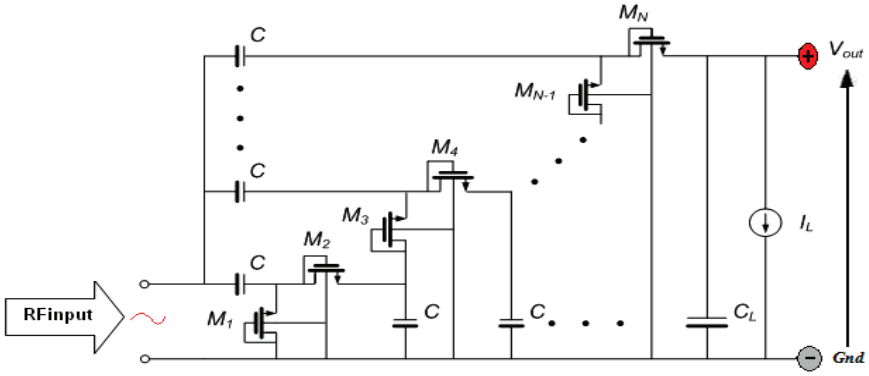


Figure (3.57) voltage multiplier based on NMOSFET [178]

The second type of voltage multiplier uses the CMOS bridge technology cells, which are applied in several stages, with each cell made up of four transistors. In order to minimize the power consumption of the multiplier circuit the equivalent input capacitance of the VM must also be minimized [151]. The block diagram of Voltage Multiplier has been described in Figure (3.58). However, the technique is used in many RFID applications, which may be appropriate for biodevice circuits.

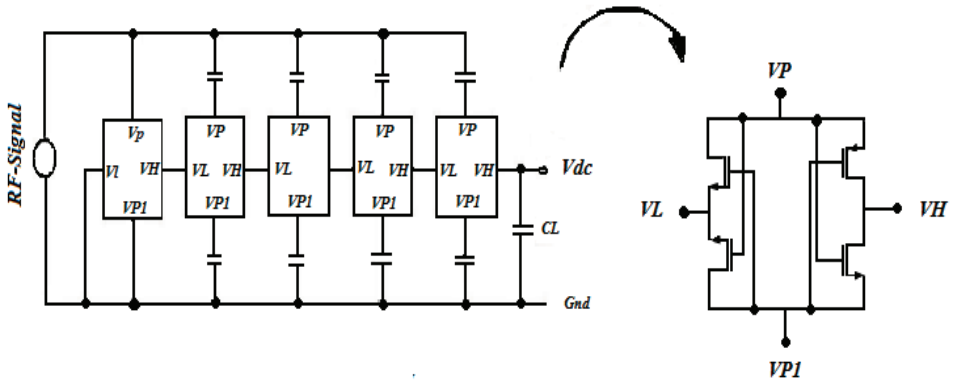


Figure (3.58) the bridge voltage multiplier cells circuit [151]

3.3.3 Schottky Diode Rectifier

The Schottky diodes are fabricated using a Titanium (Ti/Al/Ta/Al)-silicon (n-type) junction in a 0.35µm standard CMOS process [48] [127]. The larger the area, the smaller the turn-on voltage for a given current drive requirement, and the efficiency will be higher. However, a large capacitance would limit the maximum operating frequency of the multiplier. To design a Schottky diode bridge, it is necessary to consider the size of coupling capacitors. The bridge rectifier circuit for passive biomedical device is shown in Figure (3.59)

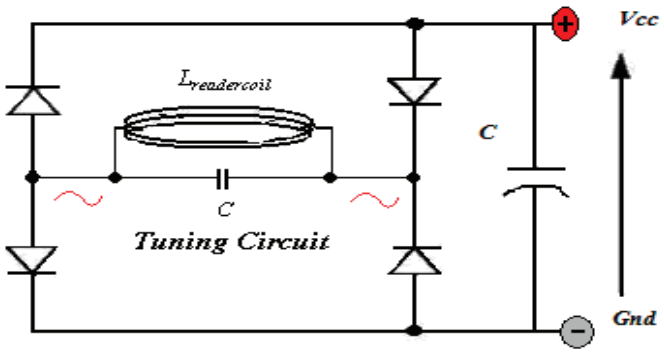


Figure (3.59) illustrates the measurement of AC & DC voltage without Load

3.3.4 RF-DC_CMOS Bridge Rectifies

The structure of the MOSFETs Bridge is illustrated in Figure (3.60) which consists of two n-MOS and two p-MOS FETs [1][128]. The output voltage is according to the level of the received RF signal. This technique has suffered from the response time where the received RF signal is low and drop of the output voltage below the threshold case causes this kind of RF-rectifiers to reduce the implant device efficiency.

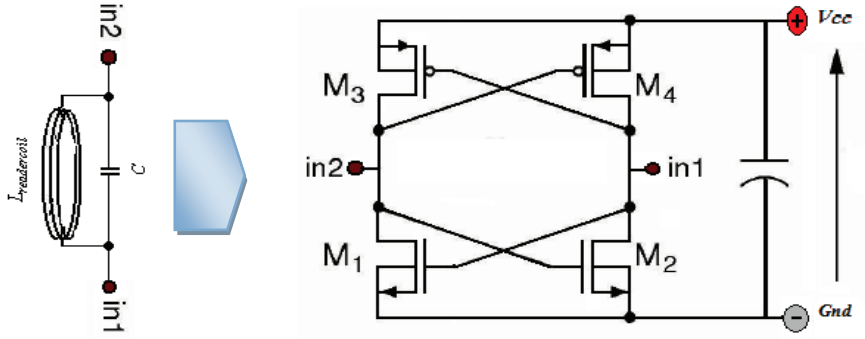


Figure (3.60) the RF-DC CMOS Bridge rectifier circuit

3.3.5 Dickson Voltage Multiplier

The Dickson multiplier was used to gain of the voltage from the bridge circuit as shown in the schematic in Figure (3.61). In most new circuits, the diodes are silicon-titanium schottky diodes. These diodes have very low series resistance, and low schottky junction capacitance of approximately (500 fF). However, it is essential for these diodes to be connected to the antenna pins using poly-poly capacitors to reduce the loss power [152].

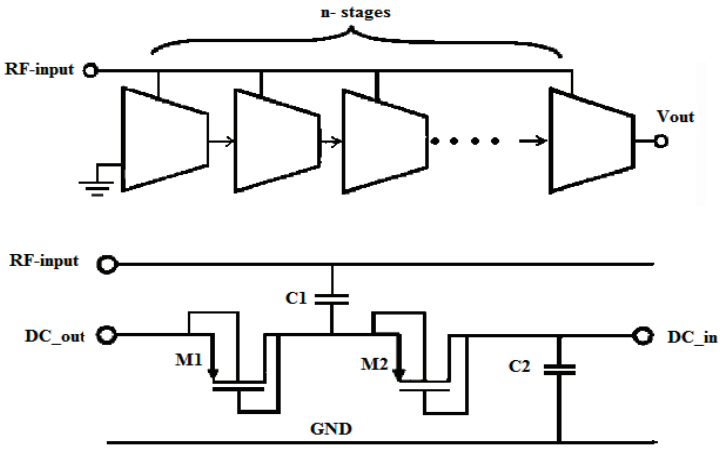


Figure (3.61) the block of Dickson Multiplier [155]

The output voltage of the charge pump diode is calculated in the equation (3.92), where the (V_t) is the voltage drop by the diode, (diode connected MOSFET as the charge device in place of the diode) and ***N*** is the number of stages:

$$V_{out} = (V_{dd} - V_t) * N \tag{3.92}$$

As shown the above equation the voltage gain ($V_{dd} - V_t$) decreases and the output voltage becomes lower than the value obtained by the diode–connected MOSFET charge pump. Therefore, the output voltage of the Dickson charge pump cannot be a linear function of the number of stages and its efficiency decreases as the number of stages increases. To increase the Dickson charge pump efficiency it can be constructed using coupled voltage doublers consisting of four power FETs (n-MOS), and four power FETs (p-MOS) [45] [46] definitely, which occupy a large area and auxiliary needs circuits, which are not appropriate for implant medical devices.

3.3.6 Voltage Regulator

Optimum performance of the converter is obtained through a compromise of achieving the correct output voltage and using as little power as possible. The voltage regulator must be used to regulate the input voltage fed to the chip to achieve the desired operating conditions. The linear technique can be used for controlling the output voltage, and the band gap based reference voltage can be compared to the output voltage and used for controlling the regulator feedback loop [2] [4]. Practically, there are different topologies based in the voltage regulator such as basic series regulator, basic shunt regulator, and regulator with fold back current limiting. One of the disadvantages of a voltage regulator is that it has high a dissipation of power and quiescent current as a linear, where the power is limited, especially in implant devices. In Figure (3.62) we can see the circuit of a voltage regulator.

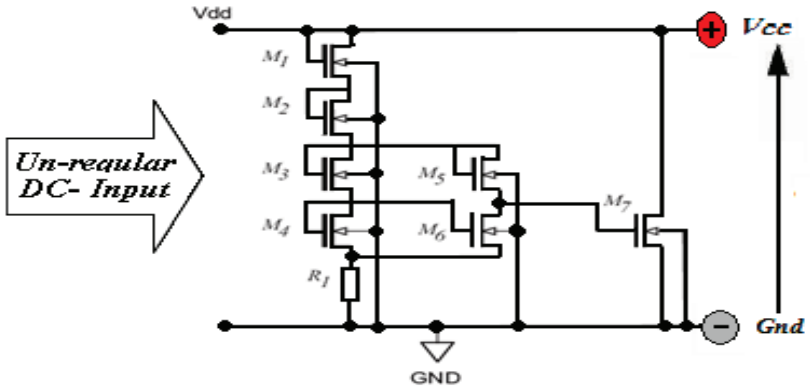


Figure (3.62) the circuit of voltage regulator [4]

3.3.7 Charging Pump Voltage Converter

The charging pump voltage converter is a DC-to-DC convertor (also called switch capacitor voltage conversion) [135], which uses the capacitors to accomplish energy storage to create a high voltage. The charge pump circuits are composed of several stages, which are capable of high efficiency in the range of 90%. Generally, the local oscillator operates up to several megahertz. However, it needs few external components to hold the charges and begin transfer in the voltage conversion process, since it does not use inductive components, thus EMI generation is kept to a minimum which reduces the noise. The switching cycle of the first input half voltage is charged during the second half of the switching cycle and the input voltage is stored on the charge pump capacitor, it is inverted and then applied to an output capacitor then the load. Thus, the output voltage is essentially the negative of the input voltage, and the average input current is approximately equal to the output current. The switch frequency has an impact on the size of the external capacitors required, and higher switch frequencies allow the use of smaller capacitors. The block diagram of the charge pump is shown in Figure (3.63). Obviously, this technique could be appropriate for biomedical devices [136].

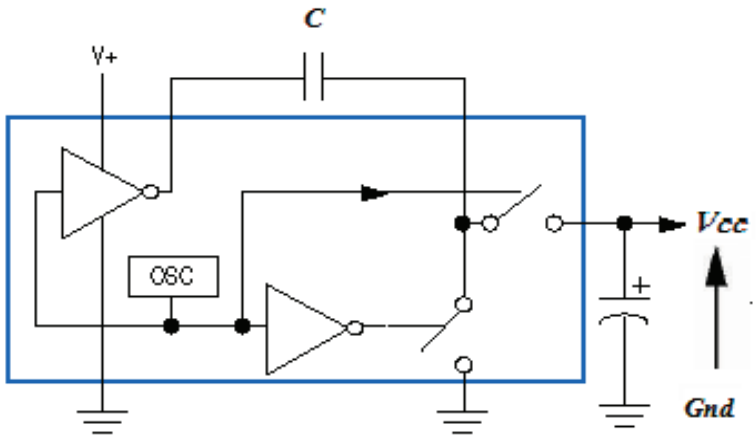


Figure (3.63) demonstrate the circuit of charging pump [136]

3.3.8 DC-DC switch converter

The other important element type used in biomedical devices is the DC-DC switch regulator, which is the critical component in the implant device, for provides the stable DC voltage.

The simple DC-DC design can reduce the size; in addition, high power can be delivered with less self-power consumption for the implant circuits [181]. Investigating the simple DC-DC design controlled by FPGA or CPLD for stabilizing the DC voltage received from the bridge circuit, we can see in Figure (3.64) the basic design for the dc-dc charging pump circuit.

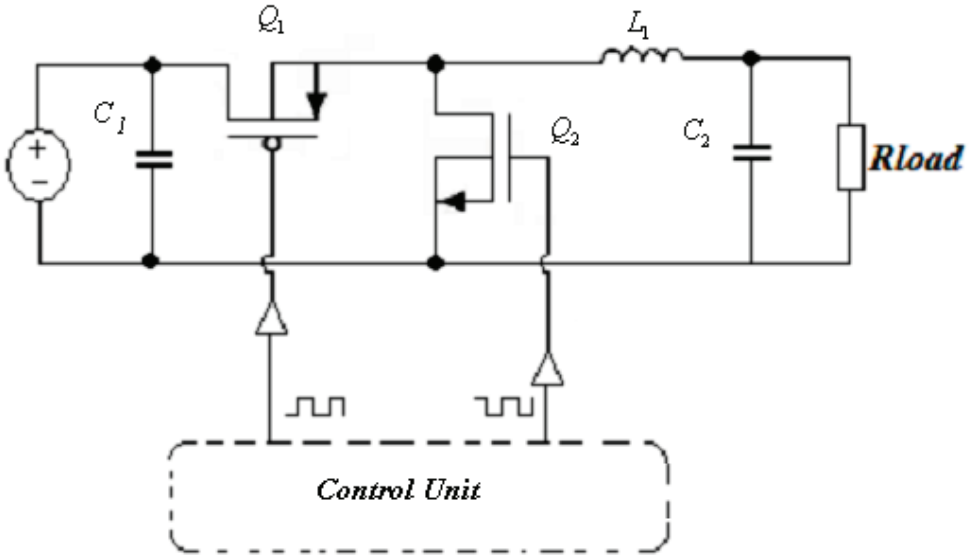


Figure (3.64) the circuit of **dc-dc** charging pump [181]

The converter is driven by switched gate control–pulses for gate-G1 and gate-G2, which are complementary to each other. However, when the gate-G1 is high, the ***Q1*** is turned ON and ***Q2*** is OFF, and as a result the current of the inductor **L1** ramps-up and the capacitor **C2** is charged, and produces a voltage, which also goes up. Consequently, when the gate-G1 goes OFF and the gate-G2 is ON, the capacitor **C2** is discharged. The process is repeated and the cycle of the control signal determines the output voltage. However, the completed circuit of the RF-DC and DC-DC converter is shown in Figure (3.65). In addition, the load circuit is determined according to the number of electrodes and the implant component, which is connected to the DC-converter. Conversely, there are other topologies used for better efficiency for controlling light and heavy load. In the implant, the space and size are limited additional circuits could increase the power consumption and reduce the efficiency of the performance for the implant. For example, Discontinuous Conduction Mode (DCM) is use for the light load [120] [186].

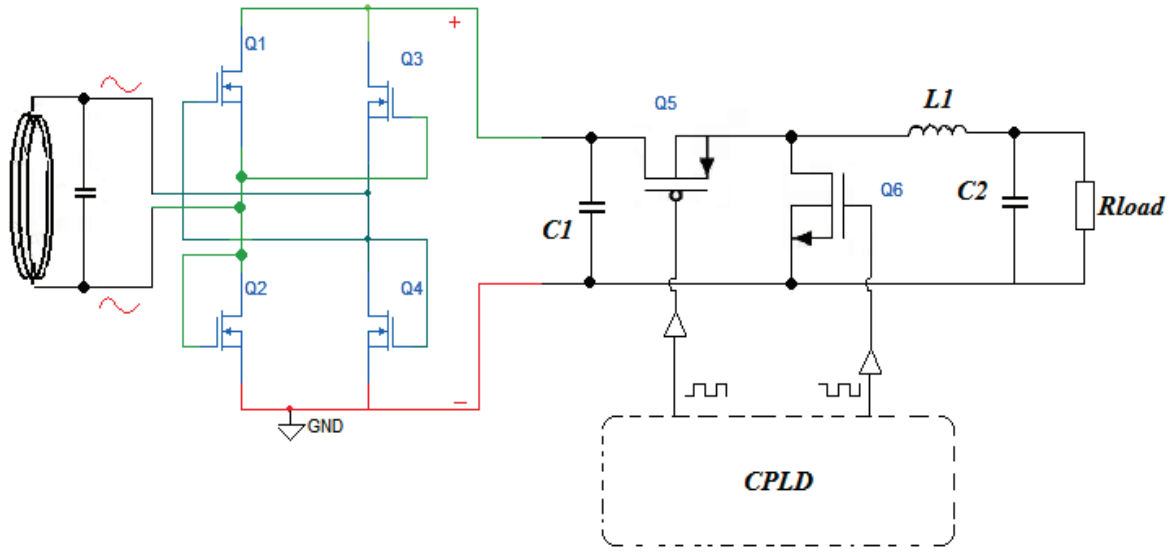


Figure (3.65) demonstrate the RF-Dc to Dc switch converter

3.3.9 Switch Regulator

The main goal of the switch regulator design is to have as much current delivering capability as possible. It is designed to consume as little power as possible itself. The principle of the switching regulator circuit is shown in Figure (3.66). Obviously, the basic circuit is composed of a few components, compared to the linear regulator. For example, the circuit works according to the switch conditions, as ON or OFF, where the switch is ON closed circuit the coil **L** tends to have rising current that generates an electromagnetic field inside its core. In this situation the diode, **D,** is open, when the switch is re-opened the coil **L** discharges and the diode becomes conducting for a closed loop circuit. However, the consumption current of the switch is about 60µA, which is ¾ of the total current consumption of output voltage. The small capacitor and transistors of the voltage switch regulator have been designed on the prototype along with overload protection circuit, which will limit the maximum induced voltage from the RF coils and avoid creating a high field that may interfere with the normal physiological activities in the body. In practice, there are different techniques for switch regulator such as step-UP converters or step-Down converters, from different brands for Switch Regulator (SW) [213], which use step- Up switch regulator from the Linear Technology package (LT 1930) [194].

We studied and investigated this topology for medical application. However, the practical circuit is shown in Figure (3.67) connected with bridge signal diodes.

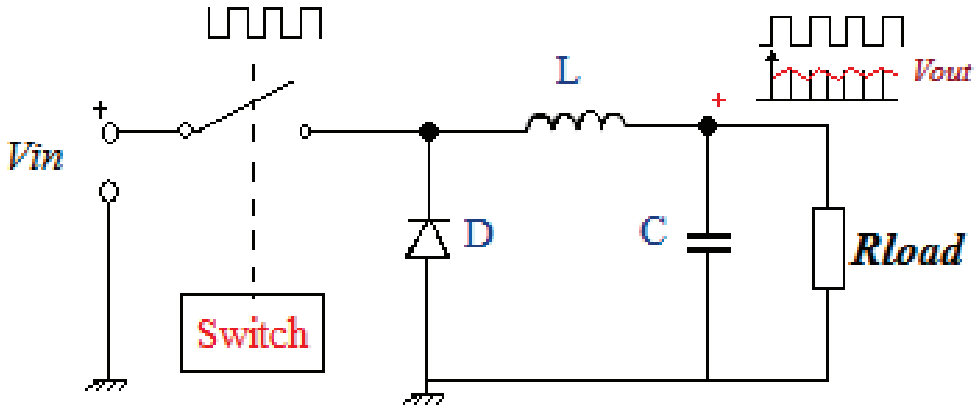


Figure (3.66) the principle of switch regulator circuit

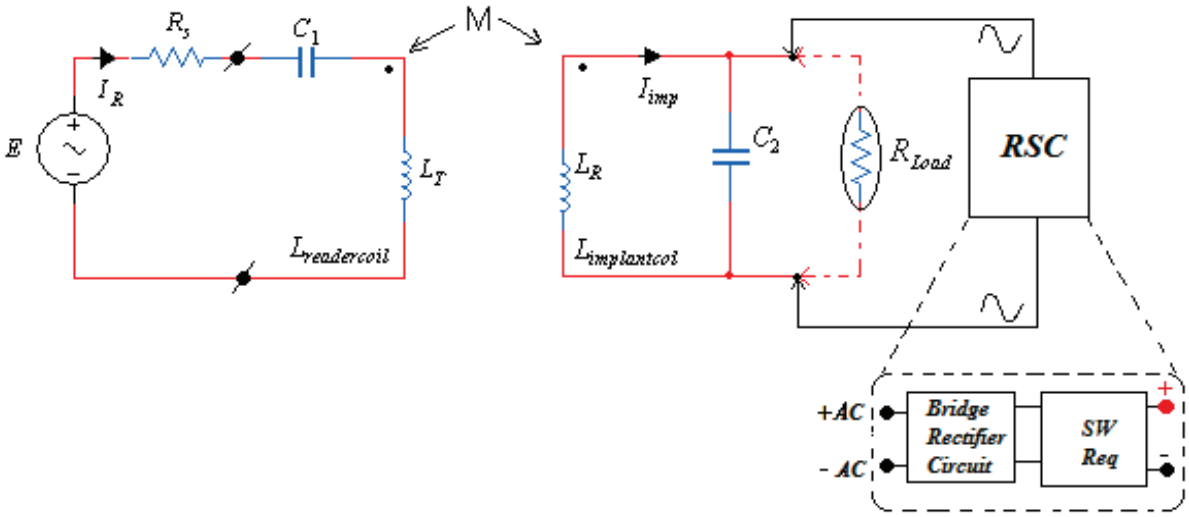


Figure (3.67) the switch regulator connected with the inductive coupling circuit

3.3.10 Simulation of the RF-DC Rectifiers

A. RF-DC Rectifier

In practice, there are many tools and packages provided by the brands, and power rectifier designs. The radiated RF power received by a small inductive loop coil at the implant device is

less than milli Watts. The RF-DC rectifier uses Voltage doubler techniques built with the MATLAB/Simulink environment to evaluate the performance of the circuit design. The RF carrier frequency is 135 kHz. However, the VD circuit is shown in Figure (3.68). The simulation of the waveform results for the circuit is illustrated in Figure (3.69). One of the disadvantages of this technique is that sensitive to time responses (charge time), and also the power drops down according to communication distance and load circuit. However, the circuit was built in and tested, which had gave the same results as the simulation.

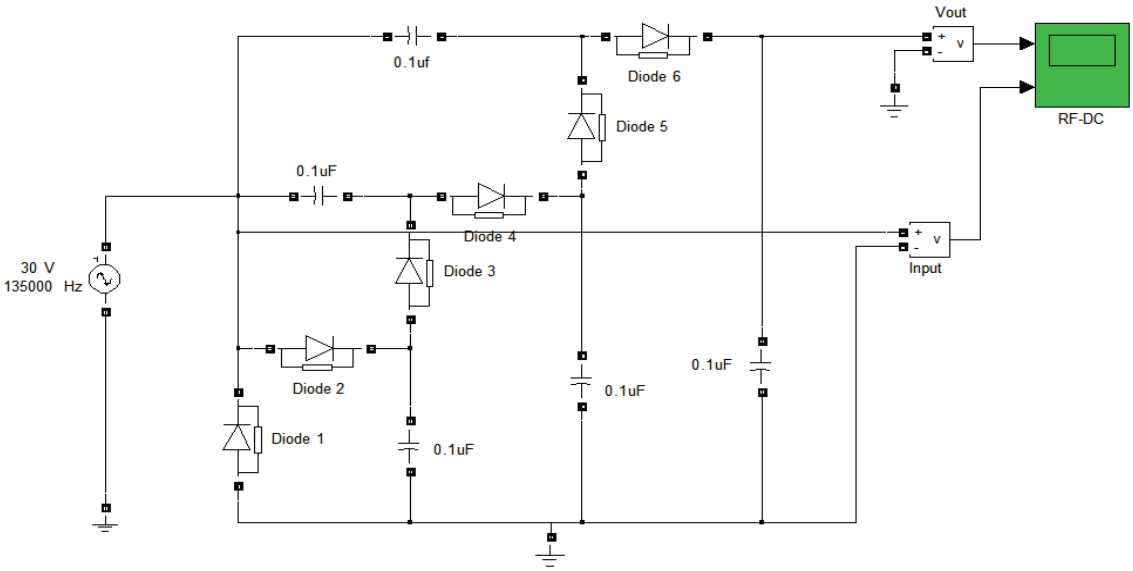


Figure (3.68) the simulation of the voltage doublers circuit with MATLAB/Simulink

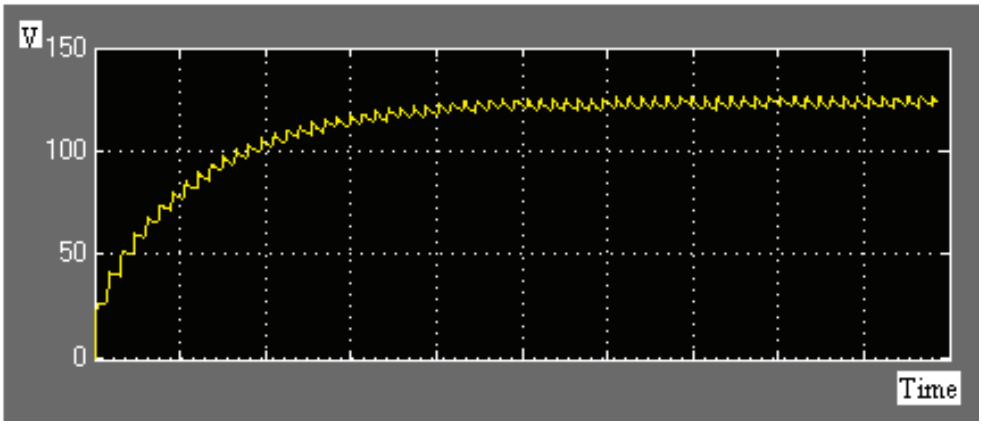


Figure (3.69) Simulation Result for voltage doubler output waveform

B. DC-DC Switch Rectifier

The simulation circuit was processed with MATLAB/Simulink for 50% duty cycle, the values of the circuit were selected as shown in Figure (3.70), where the circuit values were (VIN=5V, L=10uH, C1=10uF, C2=10uF) and the oscillator frequency was 1MHz. However, the lower control frequencies will reduce the processing time, where the voltage reaches the steady state at 1ms, so the output voltage was changed according to duty cycle of the control pulses; as the duty cycle becomes large, the output voltage increases. The simulation results of the DC-DC converter are shown in Figure (3.71). In practice, it can generate the appropriate frequency by CPLD or FPGA and control of the duty cycle.

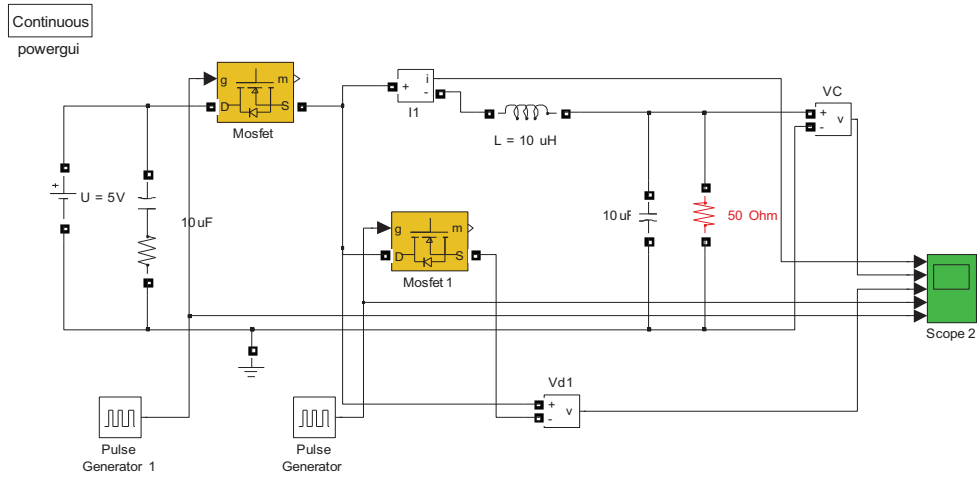


Figure (3.70) Simulation of the DC-DC converter block diagram

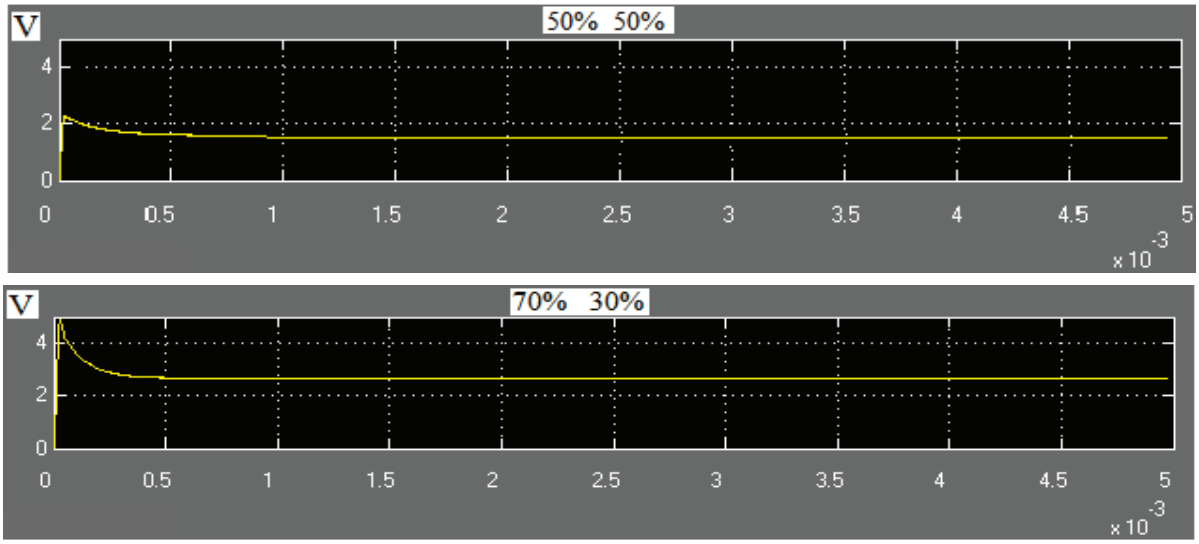


Figure (3.71) Simulation waveform of the DC-DC converter according to duty cycle

3.3.11 Experimental Lab Measurements Results

Different types of power rectifier circuits were simulated and synthesized, in order to choose the best techniques for this work. In the lab experiment, we used the signal germanium diode in our prototype design as a high voltage signal diode to rectify the RF signal crossed by magnetic flux Φ, which is proportional to the distance between reader and implant coils. The resonance frequency of the circuit is tuned at ~135 kHz, and the measurements for the optimum received power at the implant part are shown in Figure (3.72). The second target is the design of an appropriate DC-DC converter, so we investigated different circuits for our purpose. The best solution for our work used Switch Regulator (SW) topologies. This is demonstrated in Figure (3.73) which shows the comparison of the measurement results between the RF-DC rectifier, voltage regulator and step down switch regulator over short distance.

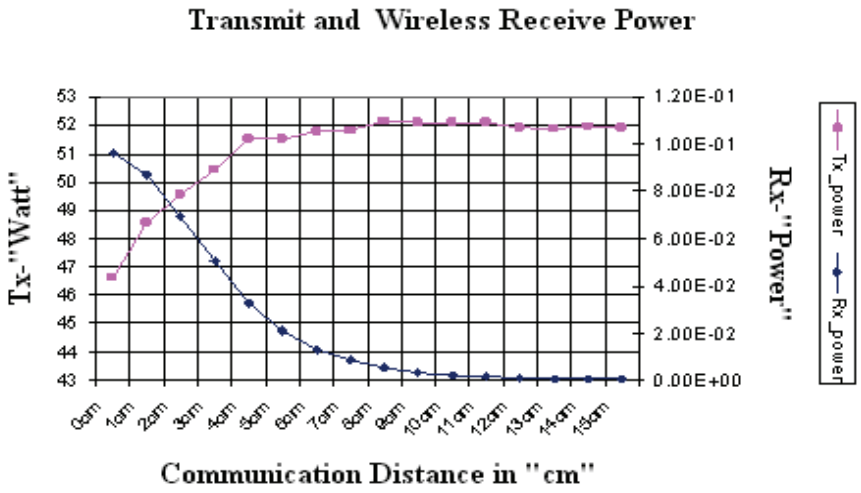


Figure (3.72) comparison measurements for DC-voltage at implant device

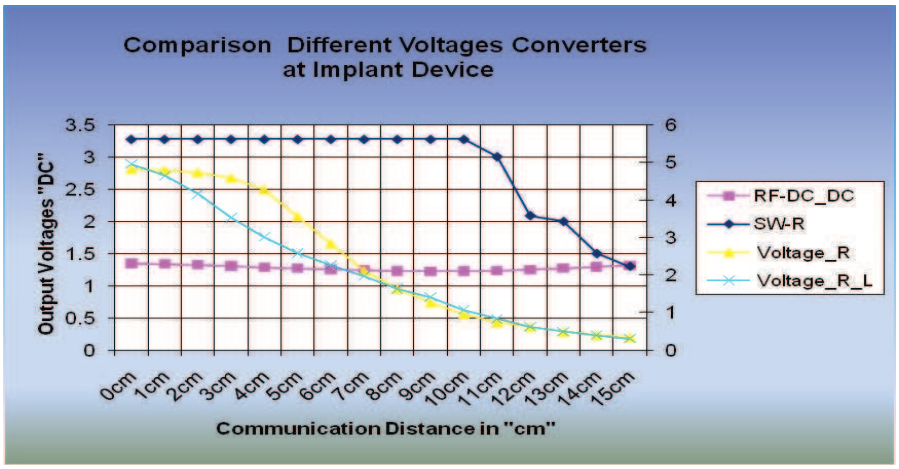


Figure (3.73) the measurement of AC & DC voltage without Load

3.3.12 Summary of Received Power Rectifiers

In implanted biomedical devices technology, the wireless received power is valuable, and needs an efficient circuit for converting the incident electromagnetic into voltages. Hence, the power rectifier circuit is the critical element implant design, and many innovations for integrated power rectifier solutions have been explored for RFID purposes. The RF to DC circuits were synthesized for biomedical devices such as voltage Doublers, Voltage Multiplier, Dickson Multiplier and Switch Regulator topologies to be used in biomedical devices. We investigated these different methodologies for rectifying the wireless RF signal in to DC voltage, which were simulated and bench tested for better design performance. However, we compared the best solution for rectifying the wireless RF signal and selecting the full-wave rectifier. Obviously, this has the benefits of a voltage-doubling rectifier, which minimizes the total area needed for the filtering capacitor. On other hand, there are disadvantages in using four diodes instead of one or two, as the efficiency is degraded due to power loss in the diodes. Generally, the regulator provides very small power and the voltages are unstable, and we know that stability and low power dissipation are the targets for DC voltage circuits in passive implant devices. In lab bench measurements, the RF-DC CMOS circuit was tested, which provides low voltage and suffers from poor matching between the LC-tank tuning circuit and the rectifier. Obviously, from the graphs it can be seen that the CMOS bridge circuit has low output efficiency. The Switch Regulator provides a very steady voltage at different distances up to 15 cm “without load” and 3.3Volt, and the power dissipation is less than “4.5µW”. In addition, it has a small footprint size in implant devices. Finally, the table (3.2.4) summarises most of the RF rectifier’s studied and investigated in this work.

Table1 (3.2.4) summary of most of the power rectifier
DC circuits for electronic medical devices

Techniques	Output DC Voltages	Max Input Voltage	Power dissipation	Power Efficiency
Dickson multiplier	Up to 1.6V	--	--	~7%
Voltage Multiplier	Up to 2.5V	35Vpp	~5µW	~16%
Voltage Regulator	3.3 V	25V	~35µW	~5%
DC-DC switches converter	3.3V	55V	--	~15%
Charging pump converter	Up to 3V	100V	--	~9%
Switch Regulator	3.28V	75V	2.5 µW	~35%

3.4 Low Frequency using Inductive-coupling Topology

3.4.1 LSK-modulation Investigation and design

To design an efficient passive inductive coupling, capable of transmitting data, the appropriate modulation techniques to be used over the transcutaneous wireless coupling need to be considered. Demands are relentless for a higher transfer rate for bidirectional communication as control signals or gathering the acquisition returned data from the body. This requires an efficient modulator scheme to achieve a higher transfer data rate and low power consumption for biomedical purposes. Generally, Figure (3.77) demonstrates the typical digital schemes applied to biodevices in our work. In addition, we have tried investigate different types of techniques to amplify and transmit the RF signal such as LSK 'Load Shift Keying' [136]. The first module is designed by using ASK modulation technique in our prototype biodevice system. The reader unit contains the ASK modulator and the auxiliary parts, the RF power amplifiers are driven by the class E and F tuned in series resonance circuit L_1C_1, where the received data has a parallel resonance circuit L_2C_2. However, the implant part consists of two coils, L_3C_3 coupled power spiral coil tuned in parallel resonance, and transmitter coil data L_4C_4. The LC transmitter driver, modulated by data using CPLD/FPGAs, programmed with VHDL code, generates either BPSK or QPSK; digital signal and the digital demodulators BPSK and QPSK, both are programmed in VHDL on the CPLD chip. Practically, the ISM is a limited frequency band, where the carrier has become higher and the parasitic capacitance affects the transformer coupling behaviour. Considering this in calculation of the values of coils and capacitors, this can be seen in Figure (3.78).

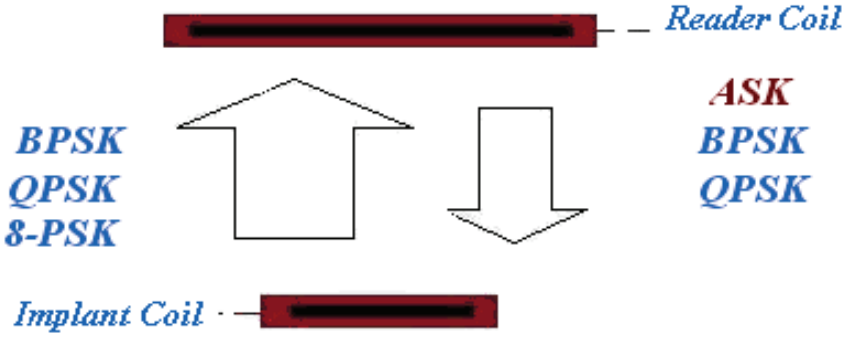


Figure (3.77) Proposed digital schemes over inductive link system

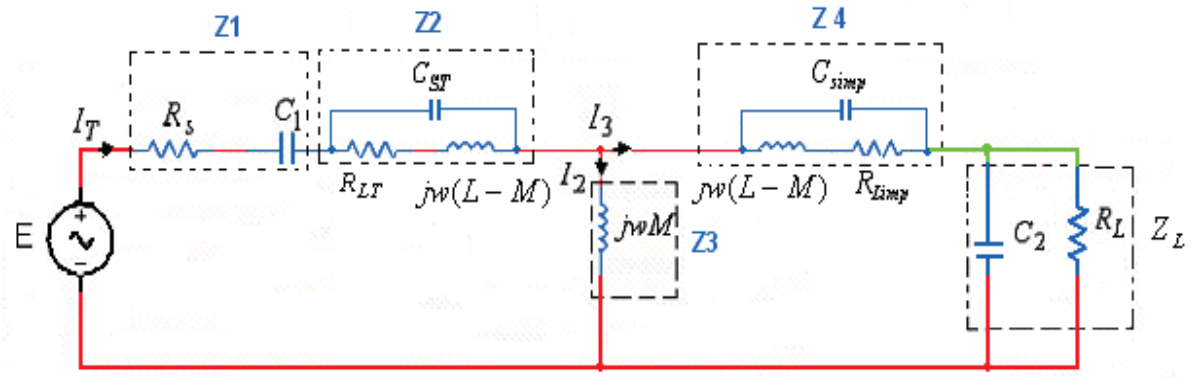


Figure (3.78) the equivalent coupling circuit

The parasitic capacitances are added for calculation, which are associated with components of the coupling transformer circuit. Hence, the quality factor of both tuned circuits is the key parameter for passive telemetry system performance and the power efficiency is subsequently critically affected by the coils quality factor ***Q***. Practically, for better performances, the ***Q***-factor for the transmitter circuit should be twice the bandwidth frequency [169]. However, the impendence at resonance frequency (f_o) at implant circuit is provided in equation (3.88).

$$Z_L = \frac{R_L}{1+\omega_o{}^2 C_2^2 R_L{}^2} - j\frac{\omega_o C_2 R_L^2}{1+\omega_o{}^2 C_2^2 R_L^2} \tag{3.88}$$

The quality factor for the self-coil can calculate by equations (3.89) and (3.90) it can expressed mathematically as [145], [153]:

$$Q_{imp} = \frac{\pi^2 d^2 f_o L}{\rho \ell} \tag{3.89}$$

$$Q_{imp} = \omega_o C_2 R_L \tag{3.90}$$

In practice, the reader needs a bandwidth that is at least twice the data rate, and Q factor of the LC circuit twice of the bandwidth BW of TX signal, that for full recovery of data at implant device [45].

$$Bandwidth \geq 2Q \tag{3.91}$$

3.4.2 Simulation and Lab Test Measurements

3.4.2.1 Data measurements Over Inductive Coupling Link

In the previous part, we discussed in detail the lab measurements for an inductive coupling link as the provider of power and data via an electromagnetic signal. In this section, we evaluate the inductive link for data transmission only, the lab measurements were performed with inductive link measured as function of communication distance. However, the MATLAB/Simulink simulation spectrum of TX signals for n-PSK modulators are demonstrated in Figure (3.79), which compares between BPSK, QPSK and 8PSK. The Lab test measurement for the proposed modulators over inductive coupling link is illustrated in Figure (3.80).

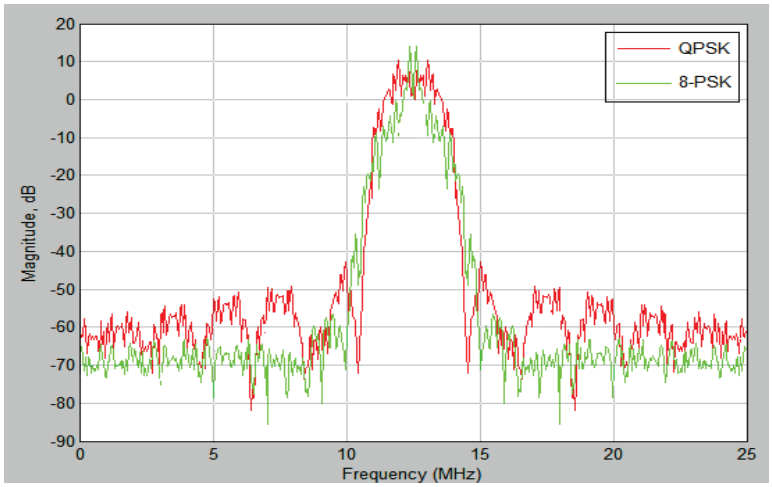


Figure (3.79) the simulation spectrum of n-PSK transmitted signals at carrier 12.5MHz

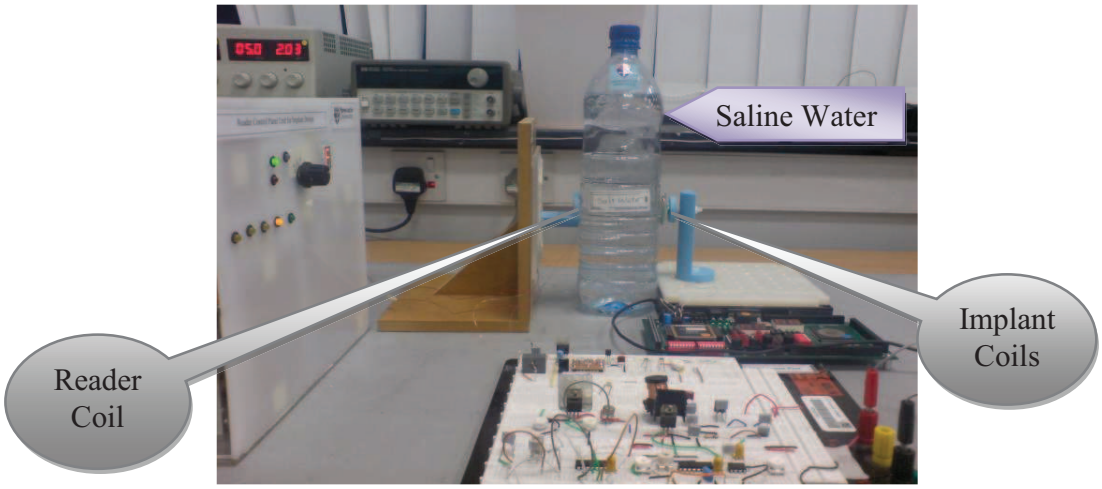


Figure (3.80) bench test measurements for the proposed VHDL Modulator over inductive coupling link

3.4.3 Conclusion

Chapter three reviews the communication data between the implant and reader part. Different techniques have been investigated and evaluated for our work, and their many categories are covered in this chapter, such as inductive coupling, power amplifiers, received power rectifiers and wireless data transmission over inductive link. We can classify them in this summary as:

- Inductive coupling link

The antenna coils for inductive coupling have different designs, and optimization challenges to achieve a high power transfer and coil size miniaturization. Usually, the implant coil is wound as a wire loop coil, where the reader coil is made of micro strip board or etched copper or aluminium and may be called a track loop coil. A Lab test measurement was performed to evaluate the characteristics of the data implant coils under different loads, at different distances maintained with over (5cm~10cm) between the transmitter and received coils antenna. The desired loop inductive or loop antennas in biomedical design often needs to consider the quality factor and are fabricated in minimum size at ISM frequency. However, additional information is located in appendix A for coils design.

- Wireless data transmission over electromagnetic field

We investigated PCB antennas in our work, as appropriate solutions in high frequency. This technique has disadvantages because the free space area behind the antenna track is unused (ground plane area), where at higher frequency this could disturb the transmitting of the information if designed under the PCB antenna and that increase the parasitic capacitance and causes interference in the circuit. In addition, this reduced the functionality of implant device, which using the micro strip antenna for transmitting the data from the implant device into the reader unit. However, this technique it is not appropriate for this work, and so is not considered in this thesis.

Chapter

4

Proposed VHDL Modulator Synthesis and Evaluation for Biomedical Electronic Device Applications

Proposed VHDL Modulators Synthesis and Evaluation

4. Biomedical Transmission Background

The bio-device field has growing rapidly in recent years, as there has been a demand for relent push for higher rates of data transmission and increase in medical functionality. This chapter will cover the new proposed technique achieved using either FPGA or CPLD to modulate data with VHDL programming code. The new telemetry system has been developed in order to fit the common characteristics of future high performance radio powered implantable stimulators. Typically, these require a high bandwidth for transfer of data to control a higher number of electrodes. Generally, the function of the neural prosthetic device is comprised of a hardware system that records the neural activity from the brain, or neural system, which decodes the control signals that can used to move the robotic devices or muscles. Eventually, modulation such as a Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) are use to increase the bandwidth and the improve the spectrum efficiency in wireless communication. However, selection of the biodevice frequency working in the unlicensed ISM band is important as a carrier frequency, which is selected to reduce the noise and interference of the implant device circuit. Figure (4.0) shows the most popular basic analogue and digital modulations have been reviewed, which are published for biodevice applications, previously revealed in chapter two in detail.

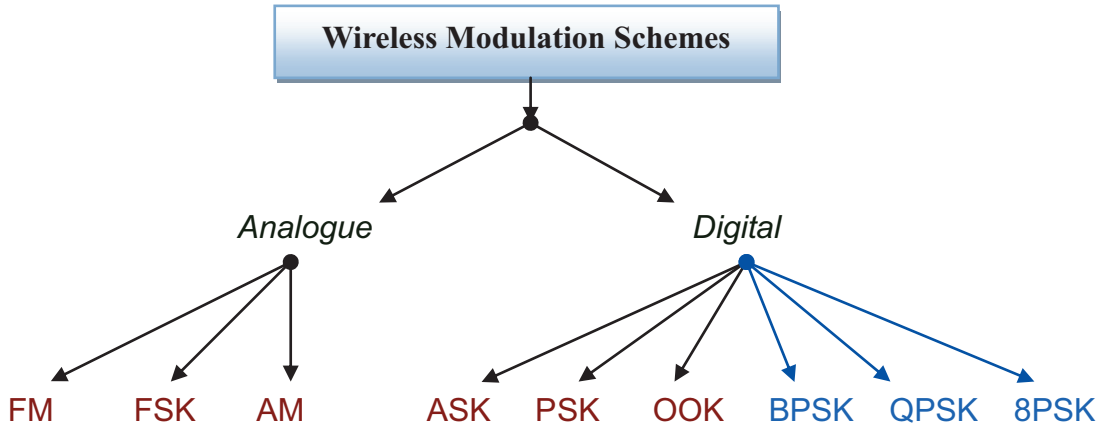


Figure (4.0) the most modulation schemes applied for biomedical devices

4.1 The Biomedical Applications Using FPGA/CPLD Technology

The FPGA and CPLD are an important technology in modern wireless communication, such as mobiles and wireless devices. The FPGA or CPLD can implement a full digital synthesizer that combines the hardware and software and offers superior speed; this facility tends to minimize the hardware design and reduce the power consumption of the system. These advantages may be useful in biomedical applications, where the size and the consumption of power are the significant challenges especially in implantable devices. Conversely, this technique is required in medical applications even at the reader or implant parts. Many researchers and companies, who are working toward the biomedical applications and a few reports, have published in this area. The demands placed on wireless communication circuits in biomedical devices are for low power dissipation, low noise, and high reliability. The Very high Speed Integrated Circuit Description language (VHDL) language has advantages for synthesizing the digital circuits and this technology may used for practical biomedical applications such as biotelemetry, telemedicine and healthcare. One of these applications in our work is introducing a new algorithmic synthesis for pacemakers, or brain implant devices, our proposed digital modulator for wireless inductive communication applications, which may be appropriate for use with CPLD technologies, which is shown in Figure (4.1).

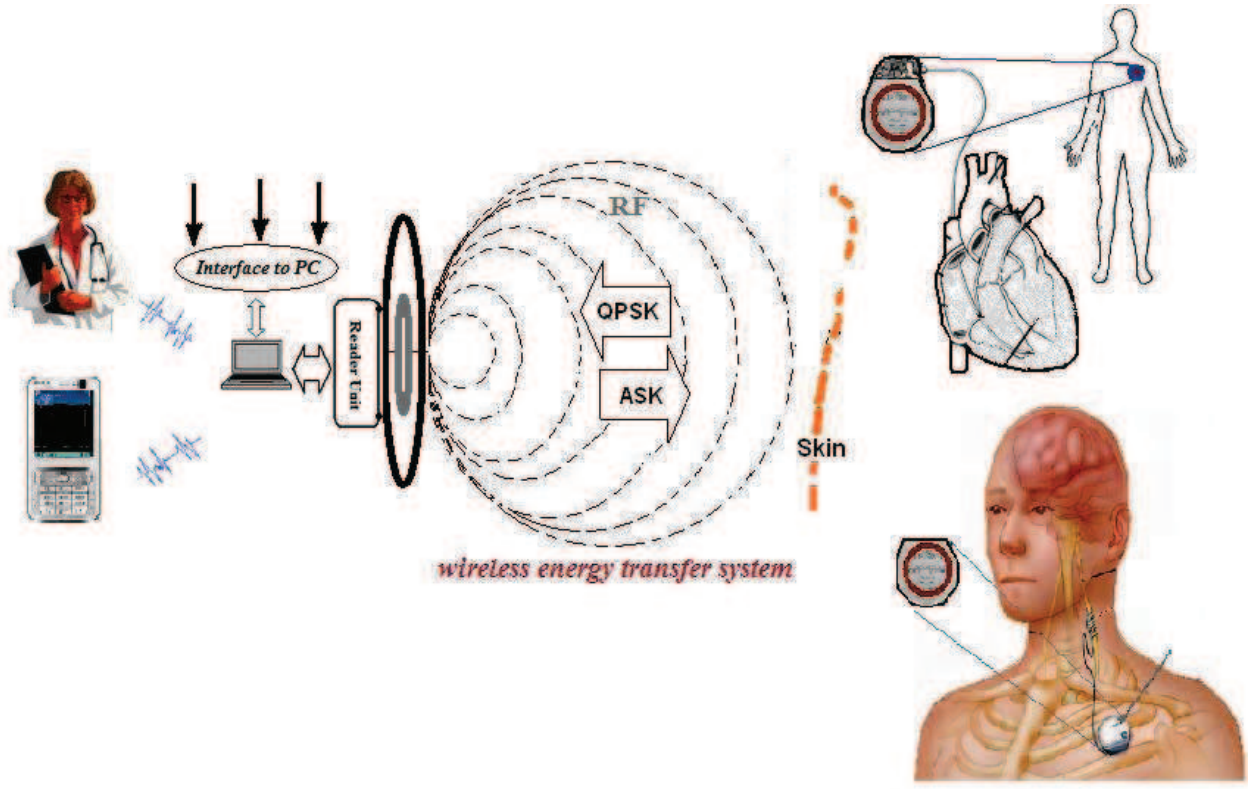


Figure (4.1) Proposed bioelectronics implant wireless interface system for pacemaker

4.2 Investigation of the Low Power Device

Many wireless applications today, which require a low power programmable logic solution, are a challenge because they require us to select an appropriate device. We studied and investigated different technologies, which work at ultra low power consumption; there are many brands for FPGAs/ CPLD technology on the market. These different technologies will be discussed, and three devices will be selected from different brands such as Actel, Altera, and Xilinx [198] [202] and [208]. Generally, the new ultra CPLD is provided by Altera MAX II CPLD, where as the cool runner is made by Xilinx, and the Actel provides the FPGA ultra low power. The static power comparison between three vendors is shown in Figure (4.2) and the dynamic power is the main key for circuit design especially for biomedical purpose as demonstrated in Figure (4.4). Generally, the different power components must be considered when selecting and evaluating different FPGAs or CPLDs brands as shown in Figure (165) below.

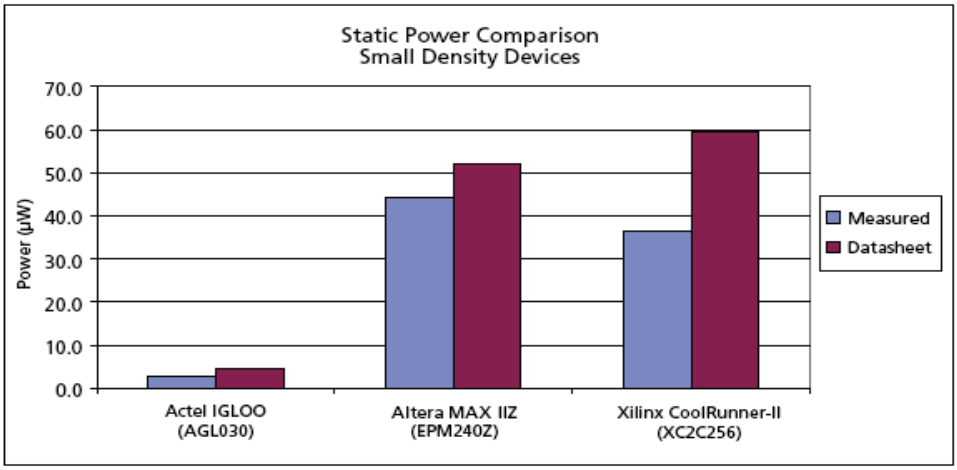


Figure (4.2) comparison of static power for FPGA and CPLD [198]

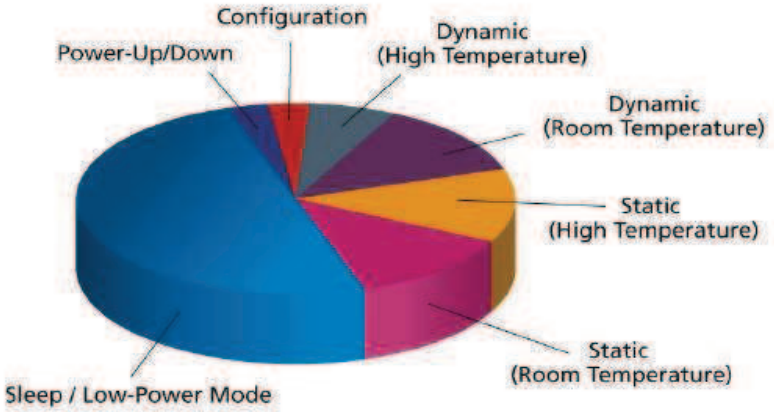


Figure (4.3) total consumption powers with FPGAs/CPLD [208]

4.3 Dynamic Power Calculation for FPGA/CPLD

For biodevice applications, the reduction of power dissipation makes a device more reliable, by minimizing the process time and current on the chip. It is important to consider not only how to calculate the power consumption, but also it is necessary to understand how factors such as input voltage level, input rise time, power-dissipation capacitance, and output loading affect the power consumption of a CPLD or FPGA devices [198], [202]. Typically, these include the components for input receivers, which must be de-rated if driven from TTL rather than CMOS external drivers as shown in Figure (4.4). We investigated different brands for CPLD, which have lower dynamic power consumption generally, and the power is found as the sum of all three components. In general, the power is analyzed in three portions static, dynamic and maximum allowed power. The static power of each component in the CPLD or FPGA is provided in the device data sheet. Generally, the total power estimated can be calculated as based on the number of specific components used. However, the goal of this investigation is to examine each design step and component of the modulator power consumption with the purpose of providing techniques to reduce wasteful power consumption. These techniques cover system partitioning, chip design, and implant layout.

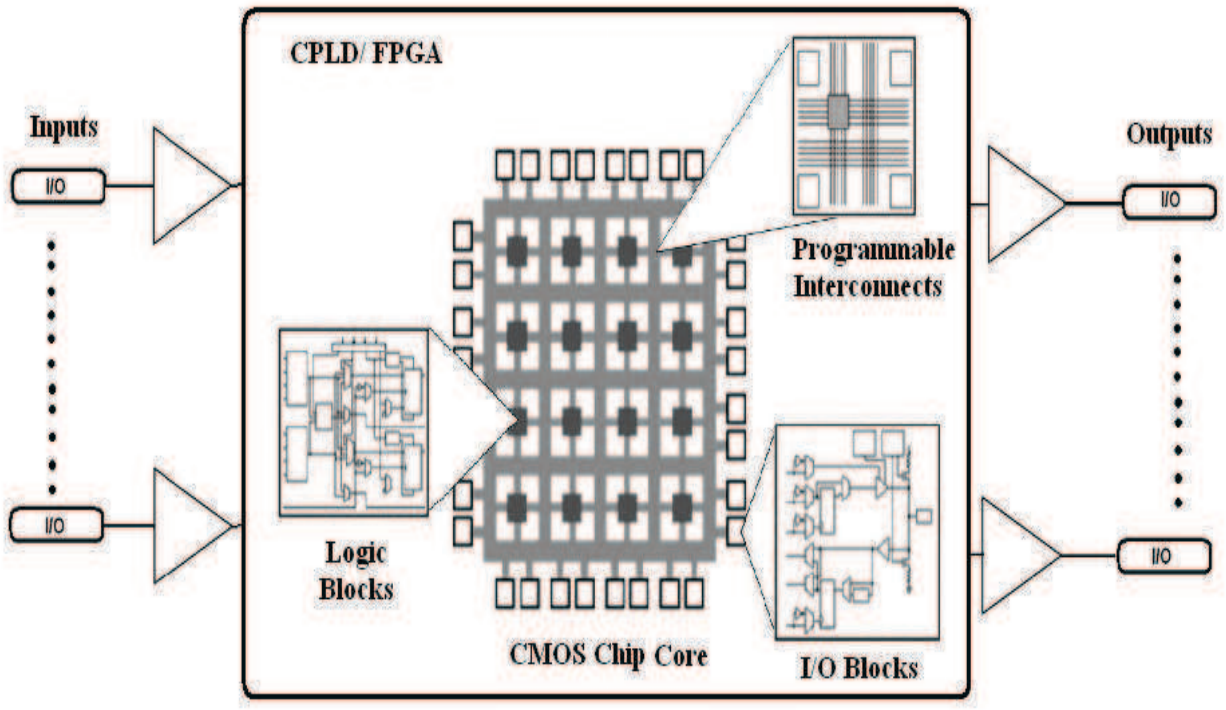


Figure (4.4) power component of typical CPLD/FPGA devices [198]

4.3.1 Configuration of CPLD and FPGA Devices

Most of the FPGA and CPLD are required to upgrading and re-configuration the device from time to time. The FPGA technology does not hold the design even if the power is off, as this needs an external flash memory to save the code design and configuration process. The configurations of these FPGAs or CPLD are normally handled with special electrically alterable configuration PROMs, serial EEPROMs or with SRAMs that load the FPGA or CPLD with their design at system power up. However, most brands for FPGAs and CPLD technologies use interface Joint Test Action Group JTAG techniques to configure the FPGA or CPLD [197] [201]. Practically, the general JTAG connectors come in different forms, but do the same function. Figure (4.8) describes the most common different JTAG connectors for configuration of the FPGA and CPLD devices, typically from different brands. In addition, Altera is introducing a new technique for upgrading the device in real time; when the device is in operation, this is called in-system programmability (ISP). This feature enables quick in-field product updates without requiring the device to turn off to initiate reconfiguration. The separation of the flash configuration block and the programmable logic block in MAX II CPLD is controlled with a special pin at the device. The updated design can immediately be loaded into the device or can instruct it to wait for the next power cycle. Additionally, real-time ISP allows multiple designs to run on a single device and updates to occur independently without affecting each other. In the remote update, the application shown in Figure (4.5), the FPGA configuration design can be updated with only momentary disruption to the microcontroller I/O expansion.

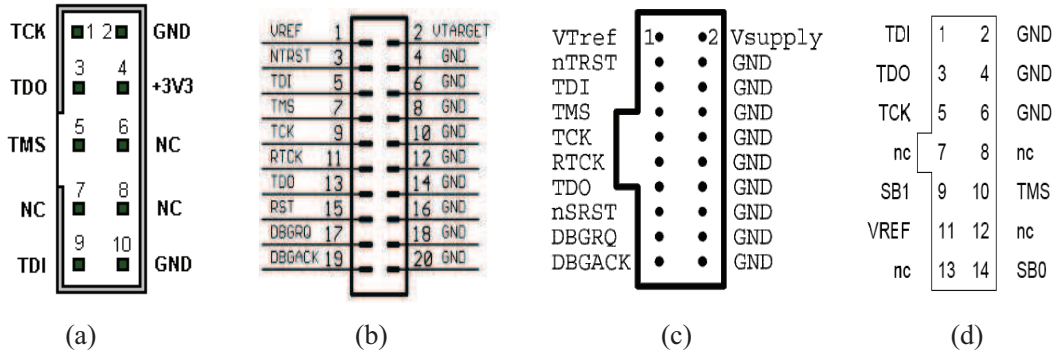


Figure (4.5) Shows JTAG connectors (a) Altera, (b) Xilinx, (c) Atmel, (d) Actel

4.3.2 JTAG Wireless Interface Investigation

The difficult task at biodevices is re-configuration of the device where it is implanted inside the body. This involves a dangerous break in the working of the modulator if the configuration malfunctions in the device. Practically, JTAG wireless technology is not widely used in wireless protocols communication; this could be solved by replacing the four wires JTAG port with a radio channel, for testing and configuration purposes. However, for biomedical devices these have been already configured before the device is implanted inside the human body. The other solution uses self-configuration for the devices, which already have flash memory. Figure (4.6) demonstrates the general concept for wireless configuration based on CPLD topology for re-configuration of the device, which can be replaced with a wireless solution, instead of using USB interface or byte blaster [207]. Furthermore, this technique offers a practical solution for modifying and upgrading the modulator, (inside the body), where the device is implanted after the surgical implementation.

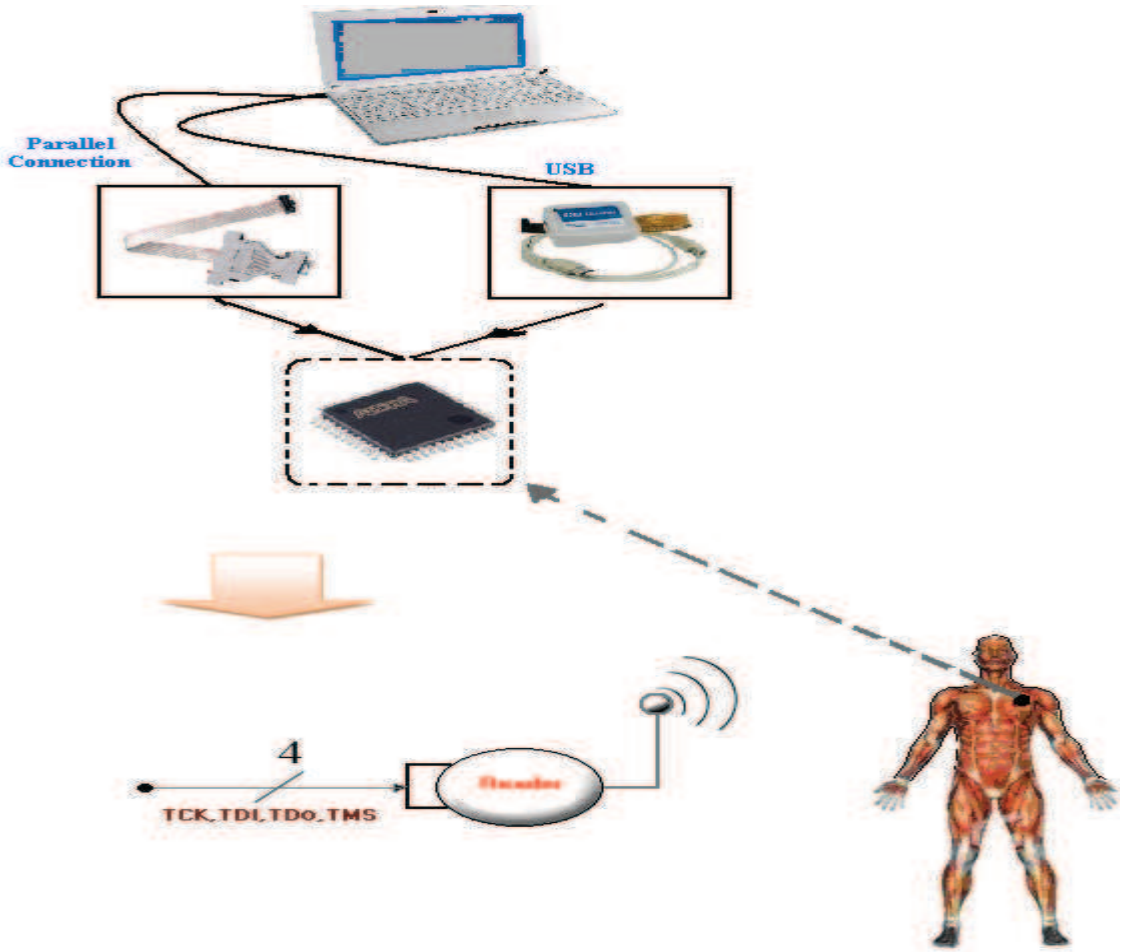


Figure (4.6) the prospective wireless protocol for the re-configurated device

4.4 BPSK-VHDL Direct Digital Modulator

4.4.1 Modulator Methodology Design

In modern digital communication, the BPSK modulation is the most popular applied in modern wireless communication. In wireless applications, such modulation may also be used for medical purposes, such as satellite telemetry, biotelemetry, telemedicine and healthcare. Furthermore, endoscopy, retina and brain telemetry devices are mainly developing with a high data rate. There is a high demand for a higher data rate, because of increasing the electrode numbers for reading the nerve signal information or controlling data. In such applications BPSK has advantages over FM, AM, ASK and FSK modulations [115] [10]. The advantage of BPSK is having fixed carrier signal amplitude that provides stable power transfer and independent data modulation. This is suitable to provide a constant RF signal into an implant device. The advantage is high readability for DC voltage supply at different distances between reader coils and implant part. We propose in this part of thesis to develop VHDL code to generate a digital BPSK signal for improving modulator performance and increasing the data rate [131]. Compared to the other analogue modulators, this type of modulator provides digital synthesis and the flexibility to reconfigure and upgrade with the two most often used languages VHDL-and Verilog-based [16] [42] and [25] [119]. The analogue Binary Phase shift Keying signal can be represented mathematically in equation (4.1), while the input data and transition for carrier wave is shown in Figure (4.7).

$$S_{BPSK} = m(t)\sqrt{\frac{2E}{T_b}}\cos(\omega_c t + \phi) \tag{4.1}$$

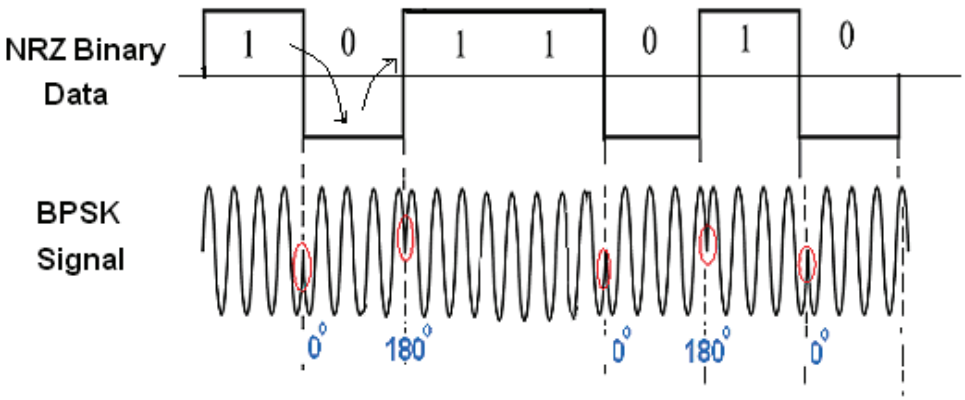


Figure (4.7) the BPSK waveform with respect to (NRZ) data state

As demonstrated in Figure (4.13), the digital data is converted from analogue or already generated in digital form and, this is required to convert to the analogue modulator performance. For this technique, it is essential to convert the binary data $m(t)$ into NRZ signal that maps the logic (0) to -1V (nominal) and logic (1) to + 1V. This data signal controls the transition shift $(0),(\pi)$ for the carrier signal. That results in high power consumption for these types of analogue modulators, reduces their efficiency and limits their biomedical application. This also increases the hardware complexity of the circuit and produces a large physical device. The proposed modulator was developed with a VHDL description code to generate carrier shifts (0) and (180°) which are controlled by the input binary data to perform the transition of the BPSK signal. The modulator consists of digital and analogue parts as depicted in Figure (4.8). The proposed modulator output signal at multiplexer (*Mux*) is in digital modulated form. It can be expressed as:

$$Mux_{out} = carr_0 \cdot PN + carr_\pi \cdot \overline{PN} \tag{4.2}$$

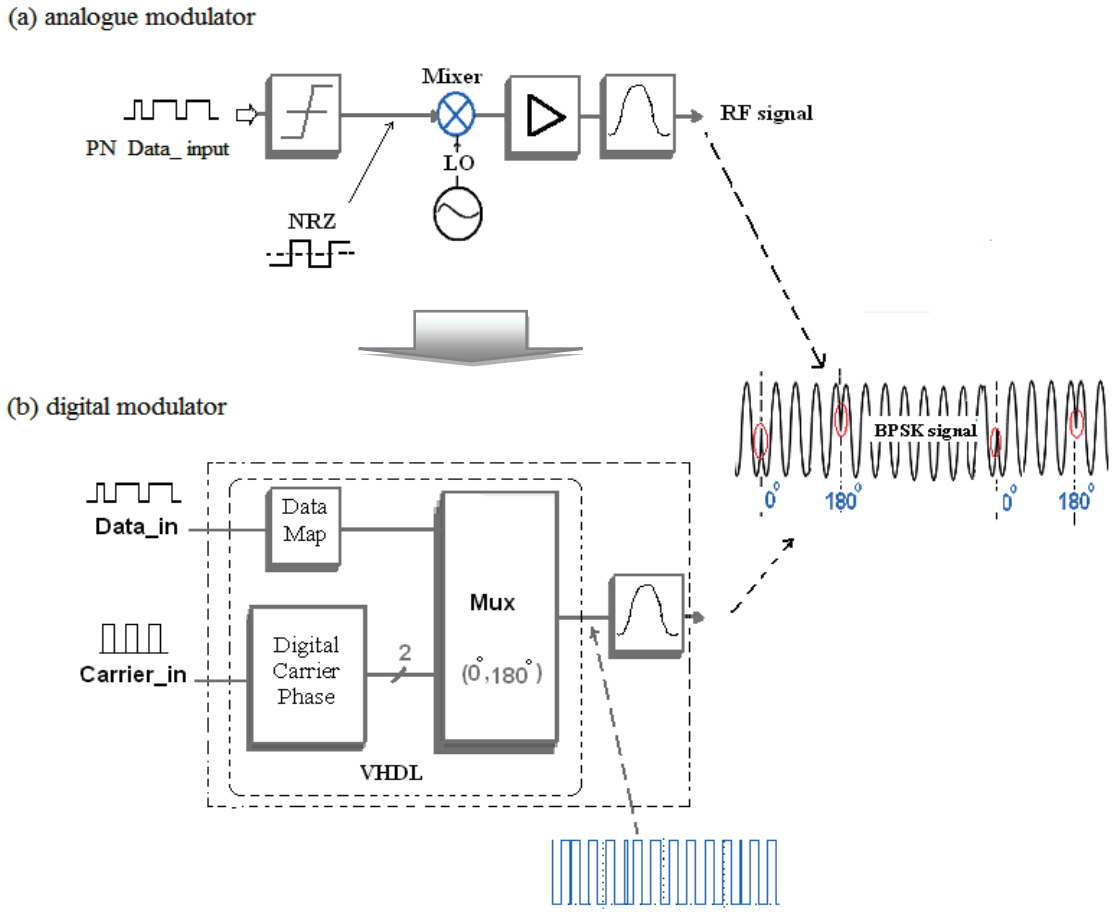


Figure (4.8) Block diagram of the proposed digital BPSK Modulator Compared to Analogue

The filter is essential for the modulator to complete the process (off-chip); the output signal produced by the filter has an analogue form. In this work, we investigated two types of filters, the first is low pass filter (LPF) and the second is band pass filter (BPF). The BPSK VHDL modulator output signal fed into the test filters; this will be discussed in this chapter in detail. Generally, the output is selected by the multiplexer then filtered with either a passive band pass filter or low pass filter to eliminate the high frequencies and the harmonics which are associated with the square wave signal, in order to provide the transmit analogue signal (Tx). The simulated random data signal (Data_in) that is generated by a PN sequence can be represented by the Fourier series analysis as expressed in equation (4.3), where the input carrier signal is a periodic pulse train signal, which mathematically can be expressed in equation (4.4) [171], [40] and [27].

$$PN(t) = \sum_{n=-\infty}^{\infty} C_n p(t - nT_c) \tag{4.3}$$

$$Carrier(t) = \frac{4}{\pi} \sum_{k-1}^{\infty} \frac{\sin((2k-1)\omega_c t))}{(2k-1)} \tag{4.4}$$

The module system was synthesized and simulated with the MATLAB/Simulink environment [162] [28], and synthesized with VHDL programming code, and performance was evaluated by the hardware measurements. Figure (4.9) demonstrates the three methods considered for generating and evaluating the proposed digital modulator for the characteristic performance.

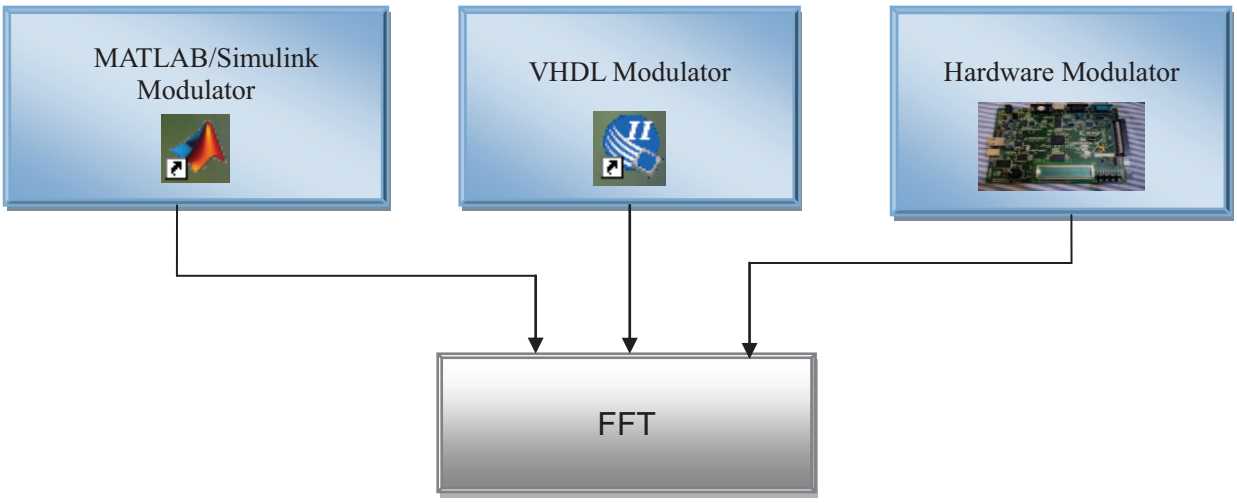


Figure (4.9) Diagram of evaluation methods for proposed modulator

4.4.2 Module Modulator Simulation

4.4.2.1 BPSK Modulator MATLAB/ Simulink Simulation

The BPSK modulator was designed and simulated with the MATLAB/Simulink environment to verify and validate the modulator specifications compared to the analogue modulators. For further work, the demodulator was constructed using the same tools to examine the performance of our proposed digital modulator. The modulator consists of a carrier source to produce a periodic pulse signal ($f_{carrier}$), that feeds into the carrier phase shifter which generates two discrete states (0^o), (180^o), and is then interfaced to the multiplexer. The data source is generated by PN_sequence, the data mapping in BPSK is used only the Q signal. Subsequently, the output is selected by multiplexer, which provides a digital BPSK signal, and this signal is filtered with an analogue filter before being transmitted. This passes the fundamental frequency ($f_{carrier} \pm data$) and eliminates the high frequencies associated with the modulated signal. The presence of noise is simulated by adding an additive white noise (AWGN) channel. The architecture block diagram of Tx_Mod is shown in Figure (4.10). The simulated random data signal (Data_in) is generated by a PN-sequence that represents the data source for proposed modulator, at a bit rate of 2Mbps for simulation purposes.

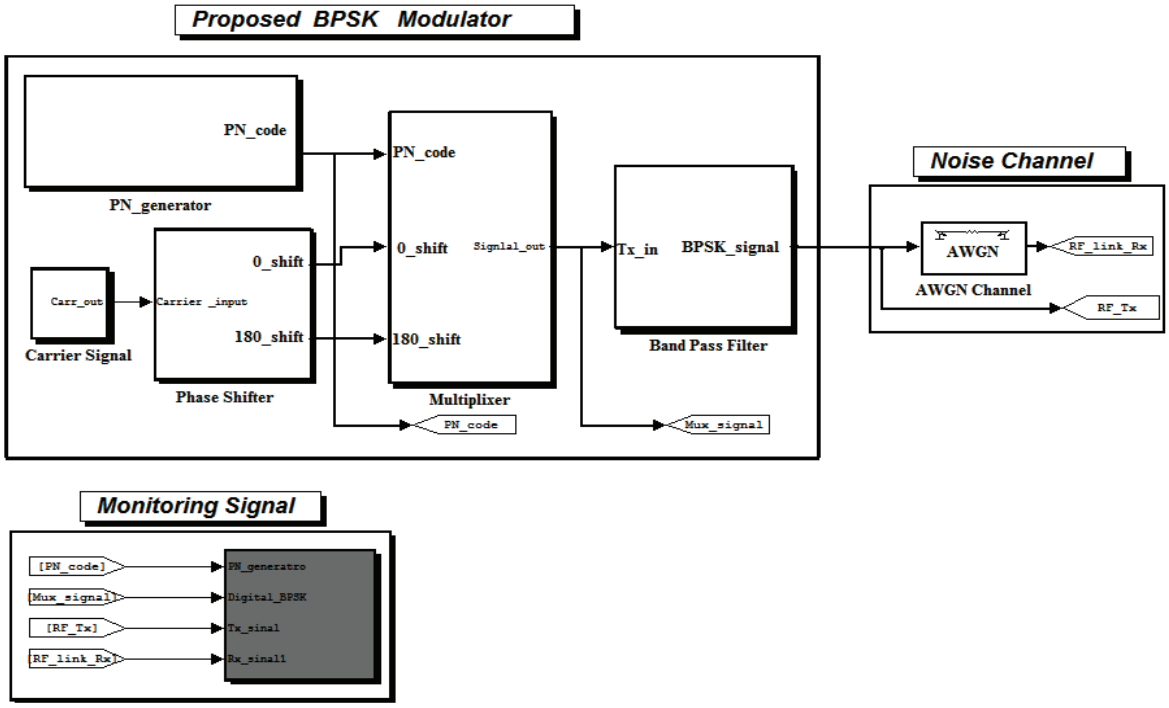


Figure (4.10) the simulation environment with MATLAB/Simulink
for proposed BPSK modulator

The simulation result of the MATLAB/Simulink modulator is presented below in figures. Clearly, the spectrum of the transmitted RF signal presented in CH1, and the received RF_signal presented in CH2, and the presentation of noise (AWGN) is shown in Figure (4.11). The simulation results for modulator and demodulator are shown in Figure (4.12a), which presents the RX-BPSK signal. Whilst the signal in Figure (4.12b) presents the recovered carrier signal, and the demodulated data has presented in Figure (4.12c), the transmitted PN code sequence is presented in Figure (4.12d). In Figure (4.12e) is shown the demodulated received data. Finally, the simulation result for the Bit Error Rate (BER) of the designed demodulator is shown in Figure (4.13). Obviously, that presents the comparison between the theoretical calculation and the simulated TX signal from the proposed BPSK modulator.

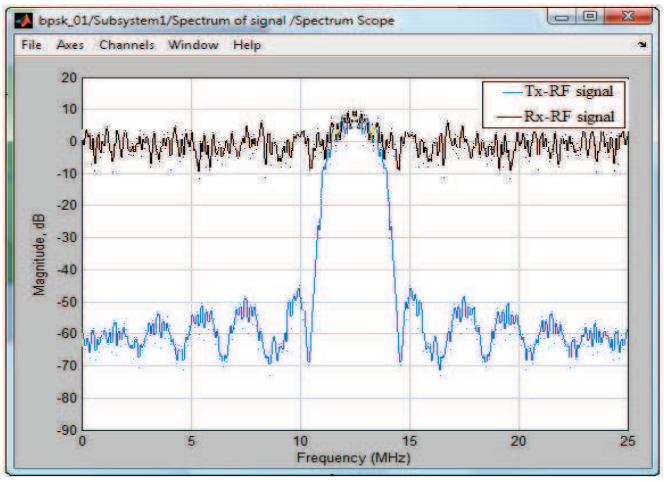


Figure (4.11) The Spectrum of BPSK transmits Receives signals at carrier 12.5MHz

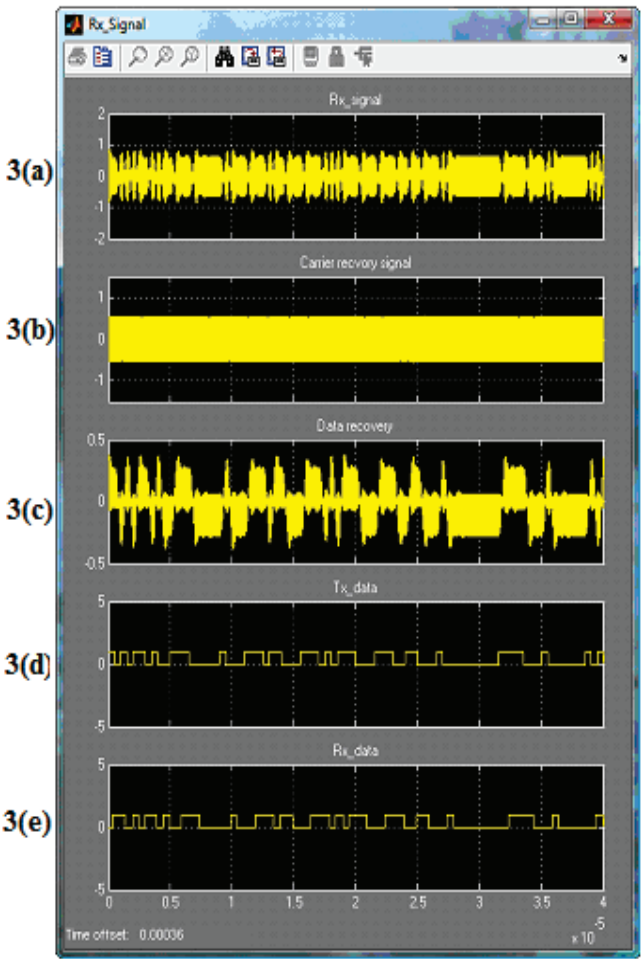


Figure (4.12) the proposed digital BPSK Mod/ Demodulator in MATLAB/Simulink

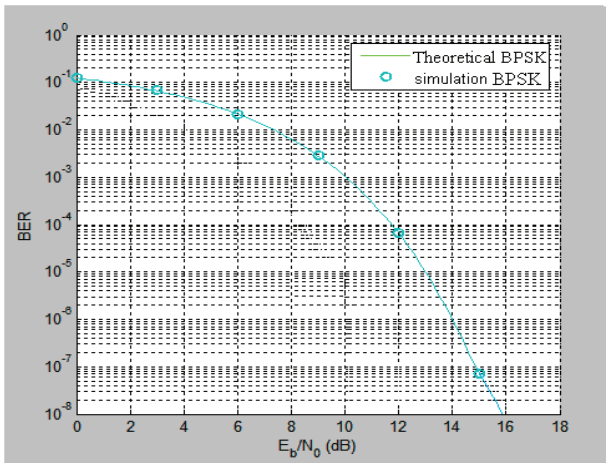


Figure (4.13) The BER simulation diagram of Demodulator signal from the proposed BPSK Modulator

4.4.3 VHDL BPSK Modulator Design and simulation

The new simple VHDL Binary Phase shift Keying (BPSK) modulator has been synthesized for transcutaneous biomedical devices applications. It is programmed with the Hardware Description Language VHDL code to generate the behavioral BPSK digital signal. The carrier frequency is about (12.58 MHz), which was generated from the local clock, which was working at 25.175MHz. The data information had reduced into 2 MHz and then fed into the PN-code generator, which is considered as information source. The behavioral simulation is shown in Figure (4.14), where the waveform simulation is presented in Figure (4.15).

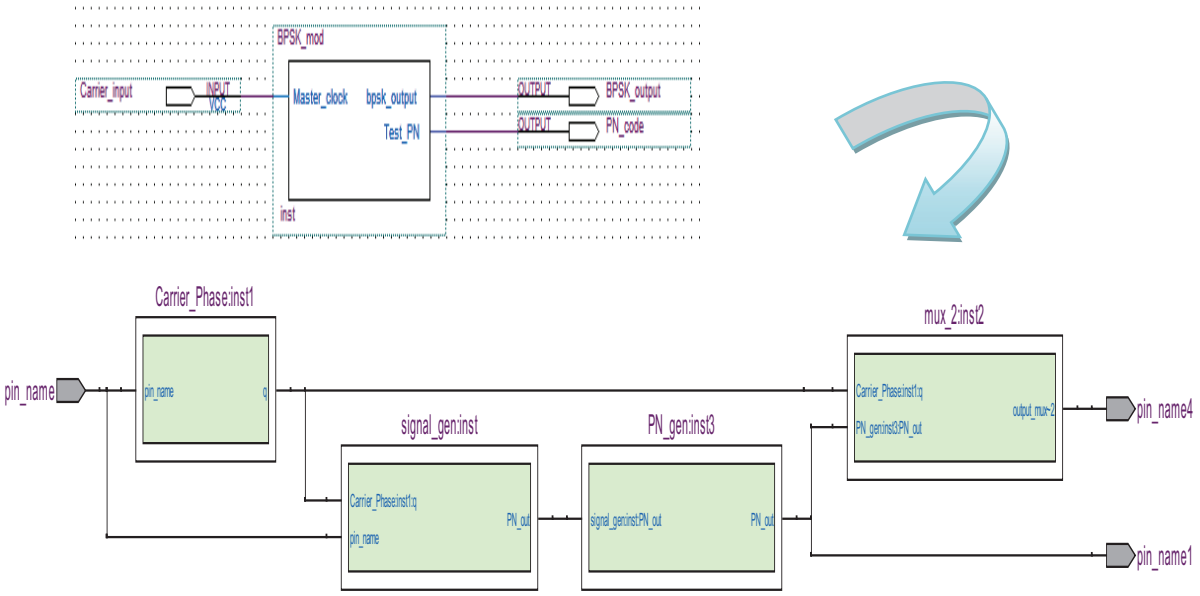


Figure (4.14) the proposed VHDL BPSK modulator

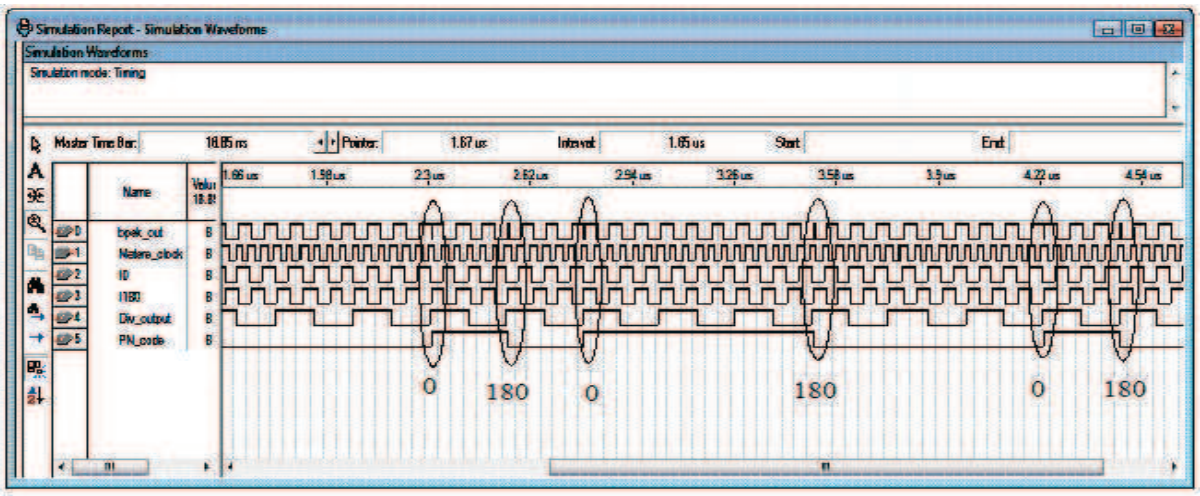


Figure (4.15) the waveforms simulation of the BPSK Proposed Modulator

4.5 QPSK-VHDL Direct Digital Modulator

4.5.1 Module Method Design

Demand for a high data rate for the data returned from the body is increasing, and require an efficient modulator to achieve both a high data rate and low power consumption. In such applications, the QPSK modulation has advantages over other schemes, and double symbol rate with respect to the BPSK over the same spectrum band. This is contrast to analogue modulators for generating the QPSK signals, where the circuit complexity and power dissipation are unsuitable for medical purposes. This type of modulator provides a digital synthesis and the flexibility to be re-configured and upgraded with two of the most often used languages, VHDL and Verilog (IEEE standard), based as hardware structure languages described in [17] [31] and [42]. All analogue or hybrid analogue/digital QPSK modulators work with the phase shift of the carrier (φ), as the key of the modulation [129] [132]. The phase shifter is the most important element in the modulator to acquire two discrete signals $\sin(\omega t)$ and $\cos in(\omega t)$. Practically, it uses a direct digital synthesizer (DDS) or numerical control oscillator (NCO) to generate the carrier signal [189] [172]. However, in analogue modulation it is essential to use the NRZ format to map *I* and *Q,* that produces analogue QPSK signal, which can be represented mathematically in equation (4.5) and I/Q are defined in equations (4.6) and (4.7) respectively:

$$QPSK(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) \tag{4.5}$$

$$I(t) = \sqrt{\tfrac{2E}{T}}\cos[(2i-1)\pi/4] \tag{4.6}$$

$$Q(t) = \sqrt{\tfrac{2E}{T}}\sin[(2i-1)\pi/4] \tag{4.7}$$

where: f_c *is the frequency carrier*
I (t) is the in phase of data
Q (t) is the quadrature of data
i is the number of M (M=2, marks this a BPSK,M=4 is QPSK)

These types of conventional modulators are not suitable for medical applications, which are essentially working with the input data in NRZ signal form. The proposed QPSK VHDL modulator was programmed to generate a carrier phase shifter, to acquire four discrete states (0º, 90º, 180º, and 270 º), where the input data was split into two separate streams in-phase ***I***, and quadrature phase ***Q,*** to map the carrier signal, which was interfaced to the multiplexer.

The output is selected by multiplexer to provide a digital QPSK signal, which passes via a passive filter before being transmitted that eliminates the high frequencies. Figure (4.16) demonstrates the proposed VHDL QPSK modulator compared to an analogue modulator. The digital QPSK signal of the multiplexer output can be represented in equation (4.8) below:

$$Mux_{out} = \bar{I}\,\bar{Q}\cdot C_0 + \bar{I}\,Q\cdot C_{90} + I\,\bar{Q}\cdot_I C_{180} + I\,Q\cdot C_{270} \tag{4.8}$$

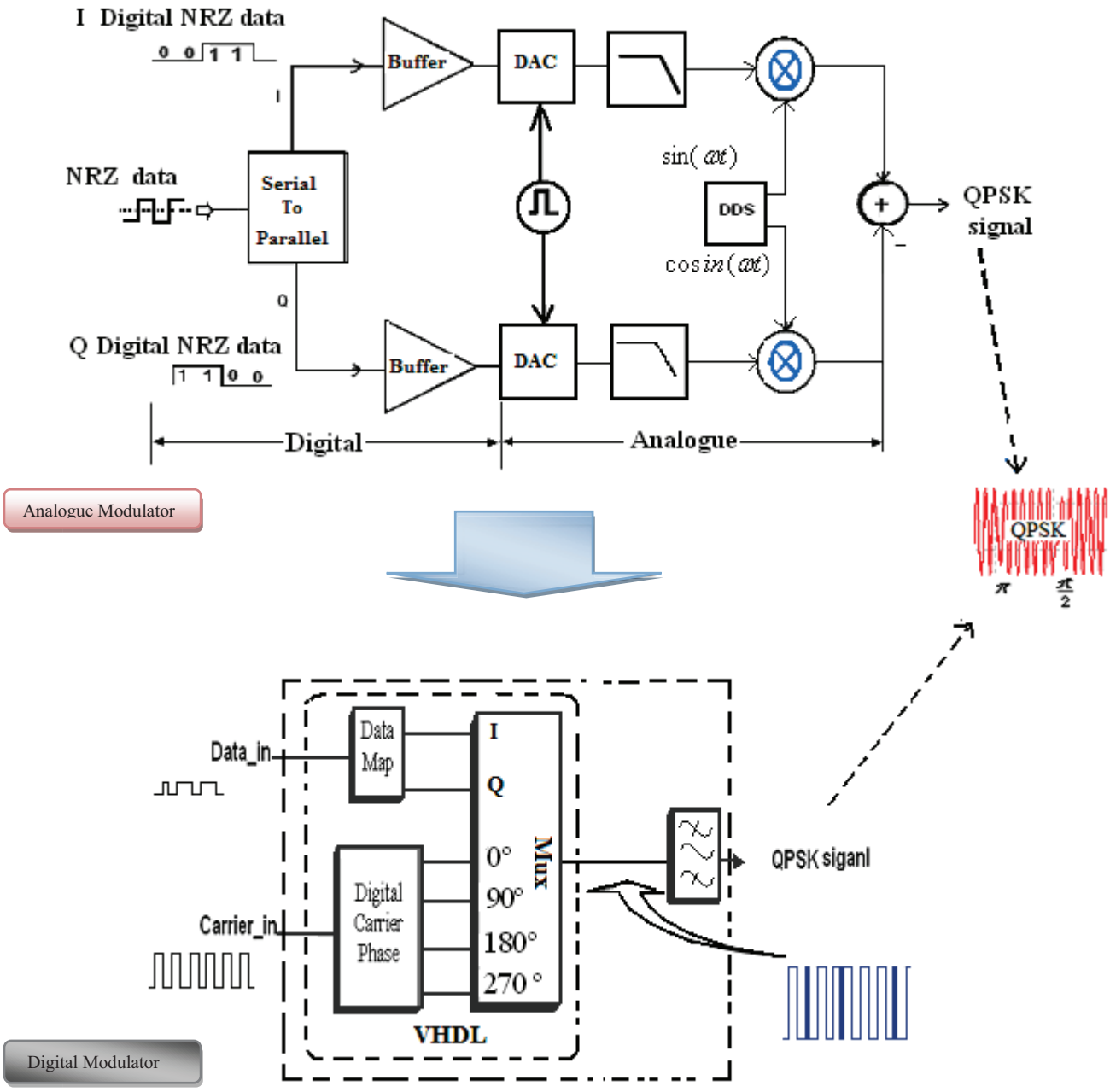


Figure (4.16) Block diagram of the proposed digital VHDL QPSK Modulator Comparing to Analogue QPSK modulator

To simplify the modulator design, were studied the principle of the QPSK analogue modulator, that is the main challenge for converting and designing the modulator in simple digital form. However, in analogue modulation when generating the QPSK signal and data are in NRZ signal format, it is essential to map the data into ***I*** and ***Q*** streams, which are influence the carrier signal according to the transition of the input data. These types of techniques are not suitable for biomedical applications; it is conventional modulators, which are essential when working with the input data in NRZ signal format. To convert the carrier, it is synthesized with a periodic pulse signal, which generates four discrete states (0°, 90°, 180°, and 270°), whilst the data mapping is described in different concepts. Figure (4.22) describes the first concept (A). The direct digital modulator is controlled by two streams ***I*** and ***Q*** of the carrier (0°, 270°) and inverted data is the controlling carrier (90°, 180°), then two carriers are combined together and subtracted in order to produce the QPSK signal. The critical point in this process is difficulty of converting the adder/substractor in full design of modulator in digital form. The second design concept (B) is presented in Figure (4.18), which describes the generation of the carrier signal method and the selectable switches to discrete phase shifts of the carriers. The data are mapped for generating I and Q streams, then interfaced into switches for transition of the carriers: the switches are represented by multiplexer, which produce a full QPSK digital signal.

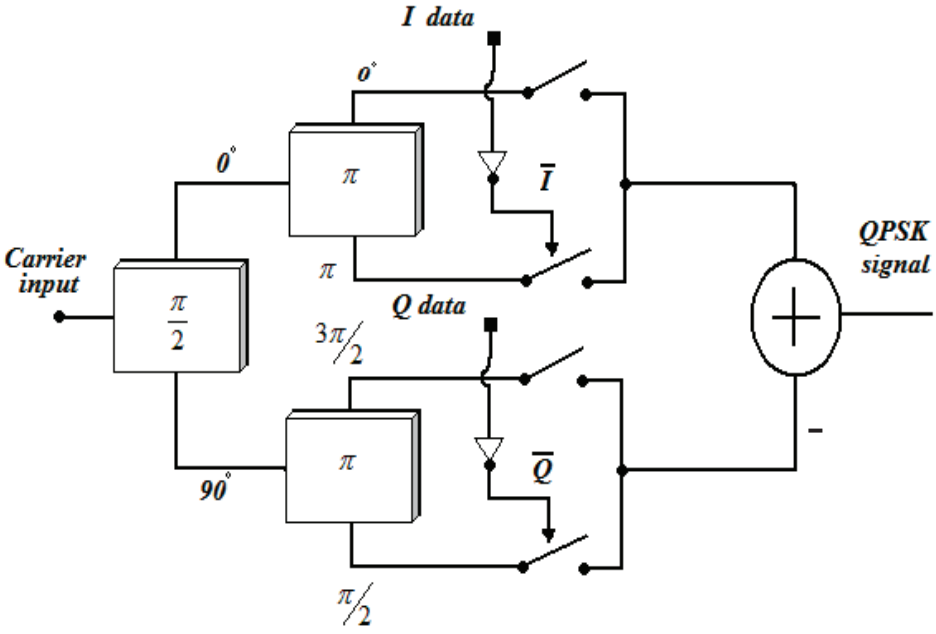


Figure (4.17) the concept (A) for generating direct QPSK digital modulator

The third design concept is shown in Figure (4.19), which shows how the carrier signals and data are generated individually; each phase of carrier signal is controlled by a single mapping of data then combined by multiplexer, to generate the desired digital QPSK signal.

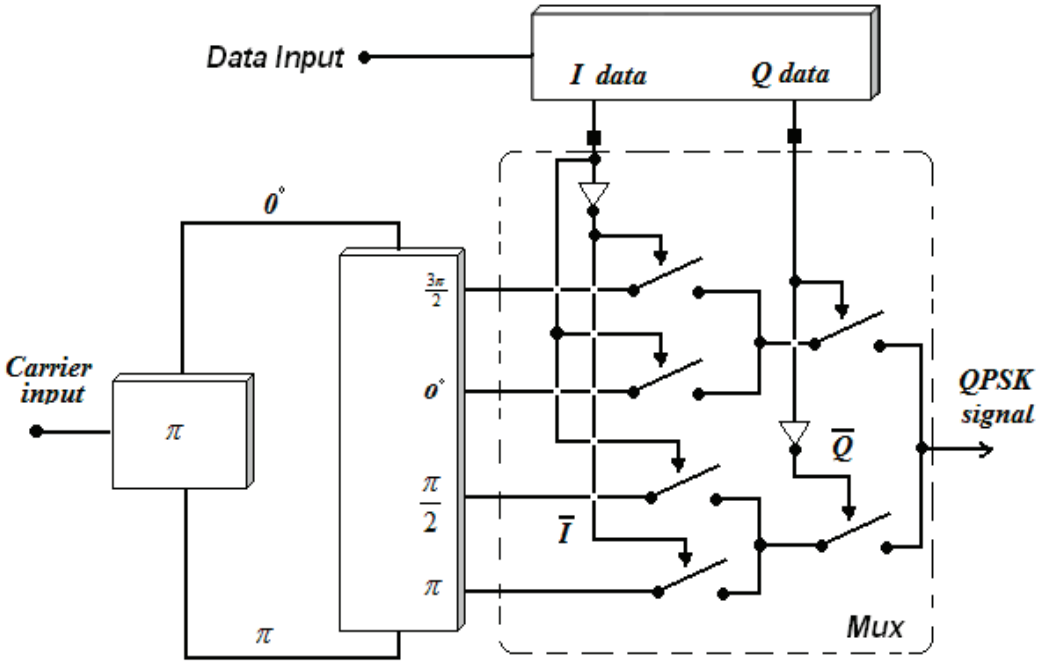


Figure (4.18) the concept (B) for generating
Direct QPSK digital modulator

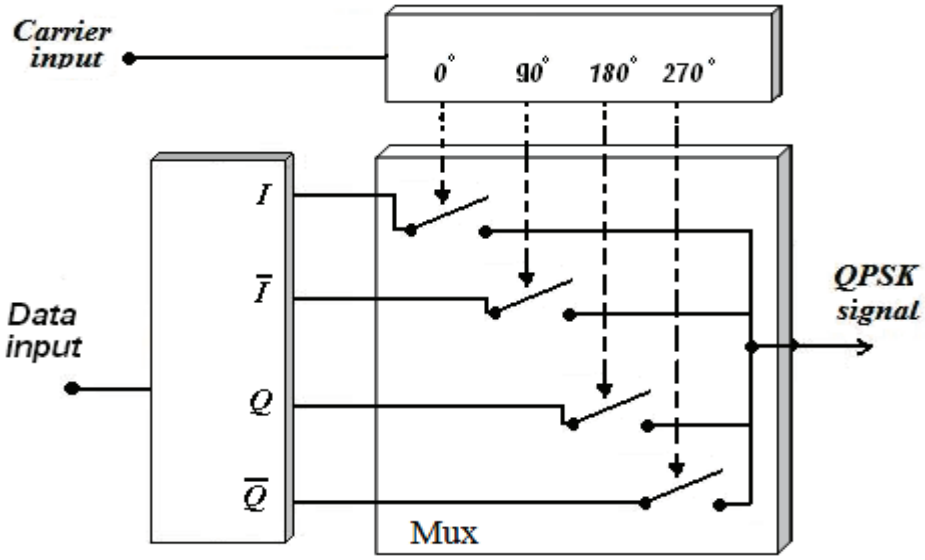


Figure (4.19) the concept (C) for generating the
Direct QPSK digital modulator

4.5.2 Module Simulation

4.5.2.1 QPSK Modulator MATLAB/ Simulink

The QPSK modulator was synthesized and simulated with MATLAB/Simulink to verify and validate the modulator characteristic and specifications. The modulator consists of the carrier source to produce a periodic pulse signal($f_{Carrier}$), applied to the carrier phase shifter which is shifts the input into four different phase signals (0°), (90°),(180°),(270°) these four signals are interfaced into the multiplexer. Whilst the data source is generated with PN-sequence, it feeds into data mapping to generate I and Q signals that control the four phase different signals. The output is selected by the multiplexer, which provides a digital QPSK signal. This signal was filtered with an analogue filter before it was transmitted. Most importantly, it needs to pass the fundamental frequency ($f_o \pm data$), in addition to eliminates the high frequencies associated with the square signal. The architecture block diagram of the proposed Tx_Mod is shown in Figure (4.20), where the simulated random data signal (Data_in) is generated by a PN sequence.

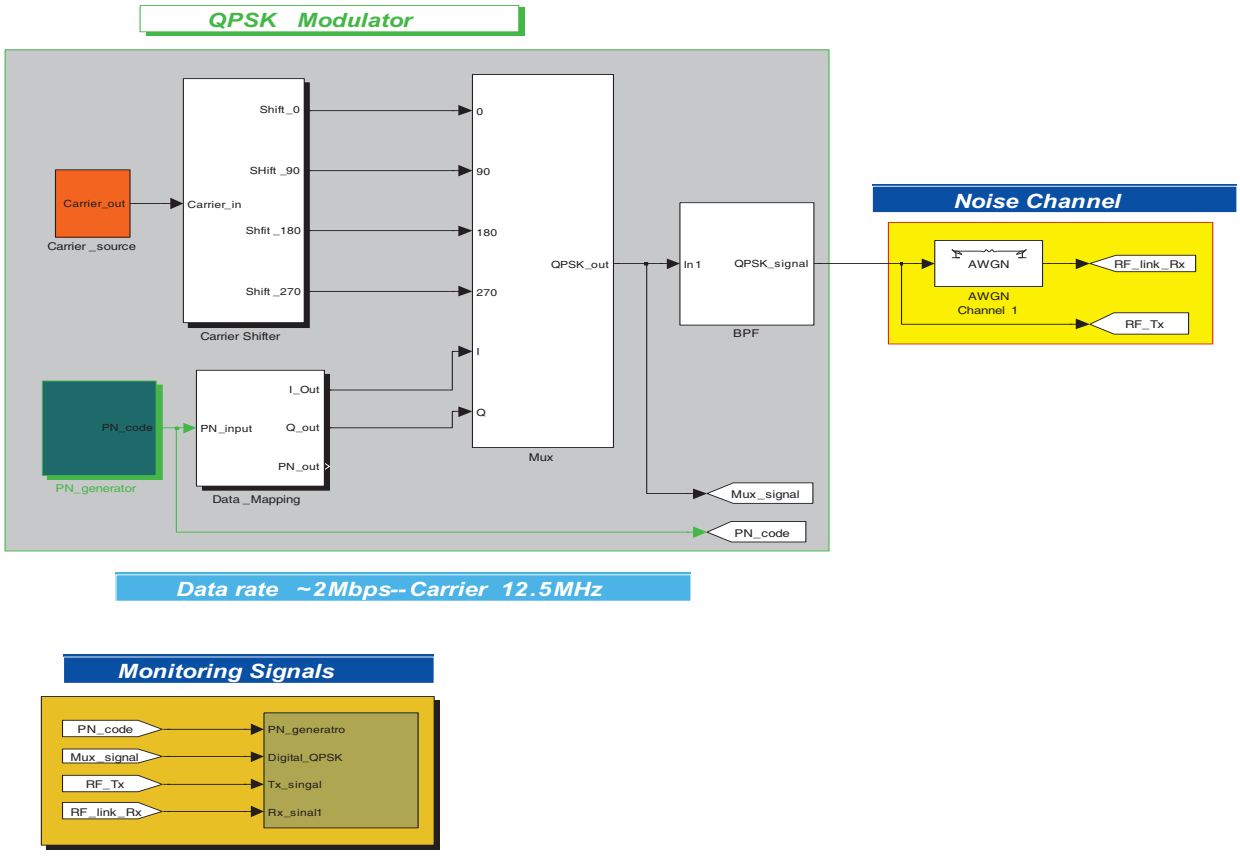


Figure (4.20) the simulation environment in MATLAB/Simulink
for the proposed QSPK digital modulator

The result of simulink simulation for proposed modulator has shows in Figure (4.21) and the spectrum for the transmitted signal has demonstrated in the Figure (4.22).

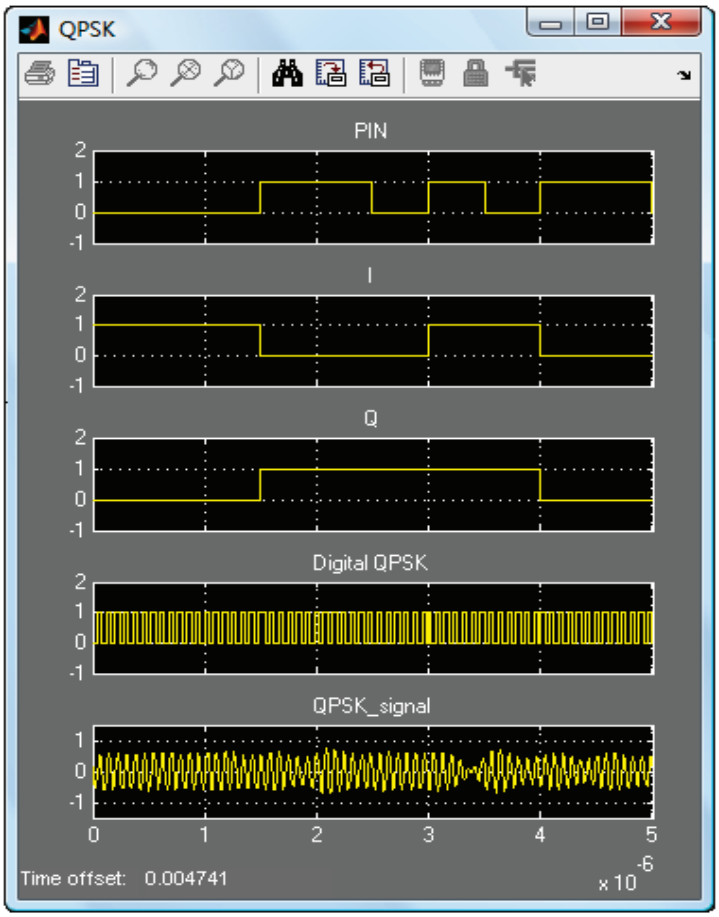


Figure (4.21) the QPSK waveform with respect to data state

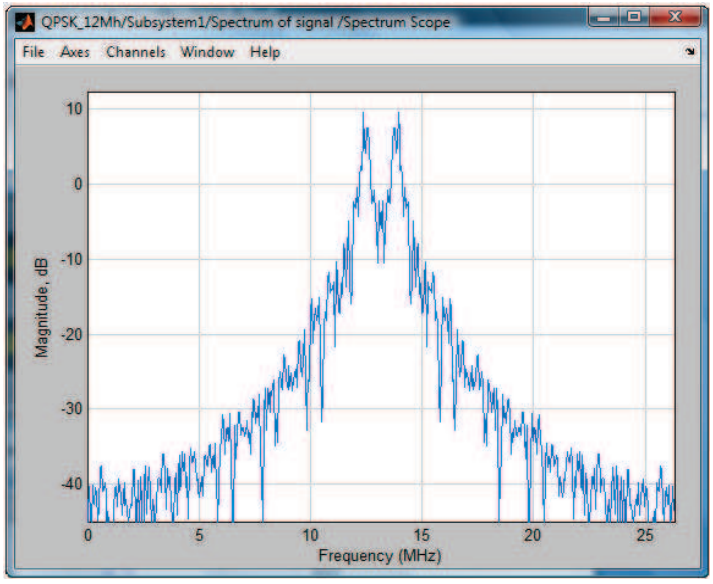


Figure (4.22) the spectrum of QPSK transmission and receipt of signal at Data rate 2Mbps, carrier 12.5MHz

4.5.2.2 Synthesis of VHDL QPSK Modulator and Simulation

The proposed modulator was built using the Altera UP2 development kit board, programmed with the VHDL language for module design and analysis of the proposed QPSK modulator. In VHDL, there are two programming techniques to be described: these modulators as direct logic synthesis the structural and behavioural code. The simulated result of this modulator has been presented in two methods structural/behavioral. Figure (2.23) demonstrates the structural design of the digital proposed modulator, demonstrates the output signals indicating the carrier phase shifter (0°, 90°, 180°, 270°), this carrier frequency 12.5 MHz is generated by the local clock signal on the board, which operates at 25.175 MHz. While the data source was generated with PN_sequence generator, it feeds to data mapping to generate ***I*** and ***Q*** signals to influence the four different phase carriers. The output was selected by multiplexer, which provides a digital QPSK signal. However, the behavioural code generated is shown in Figure (4.24), the frequency divider reduced to 2 MHz then used to generate the PN-sequence data (behavioural description). The output of PN code signal is interfaced to data mapping **I** and **Q**, these the carrier signal and data are interfaced into multiplexer to select the QPSK digital signal. However, the digital output signal passes through the LPF for harmonics separation (Off chip), which will be discussed in the filter section.

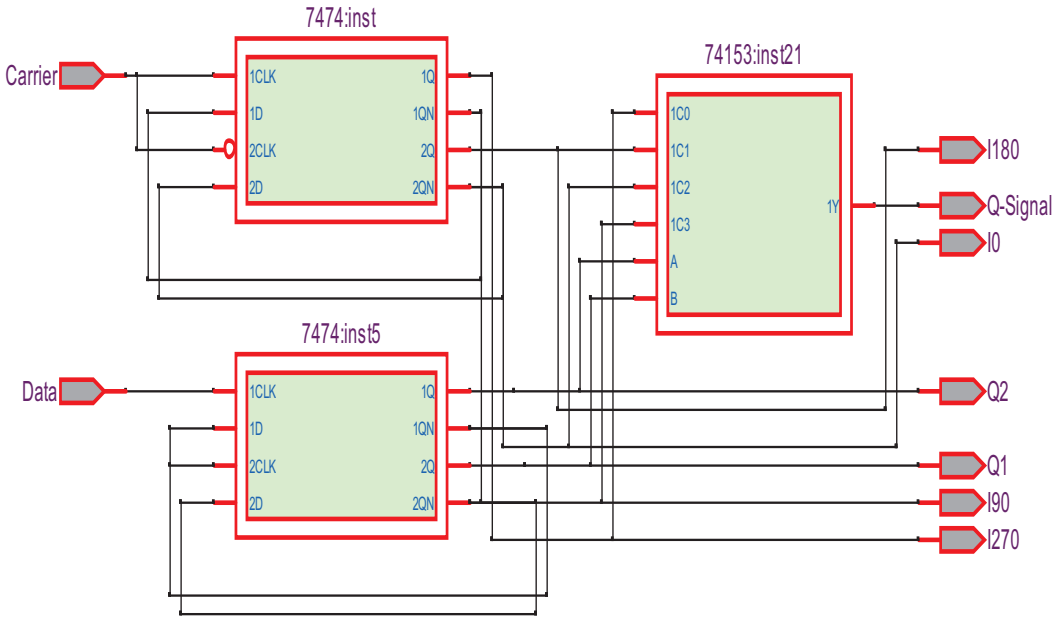


Figure (4.23) Structural VHDL-code simulation for the QPSK modulator

The simulated result of this QPSK digital modulator is presented in Figure (4.25) which demonstrates the output signal waveforms indicating the transitions (90°) (180°) of the carrier signal (output of multiplexer), due to the data influence.

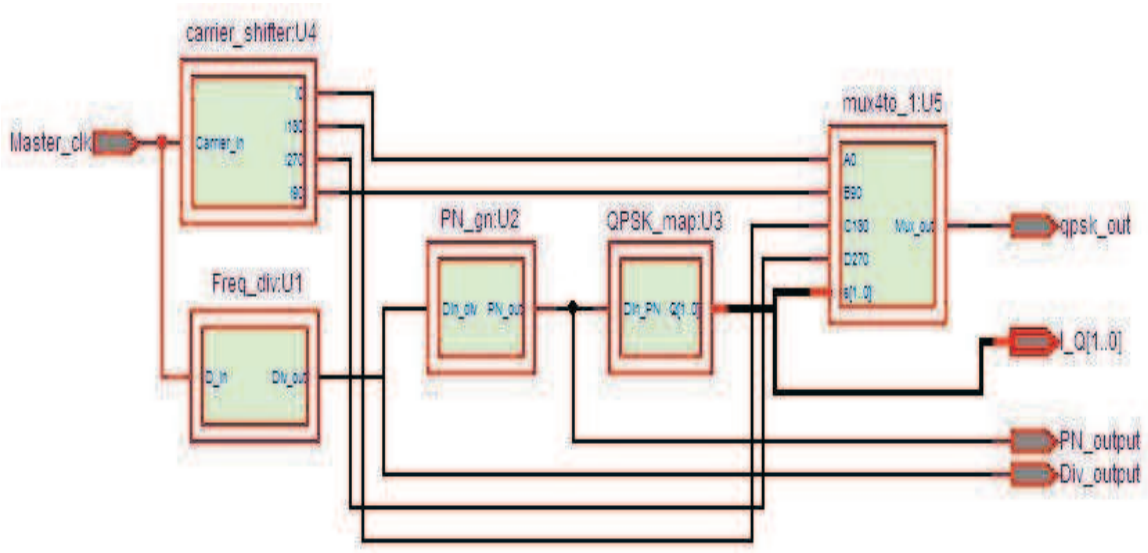


Figure (4.24) the behavioral VHDL modulator simulation

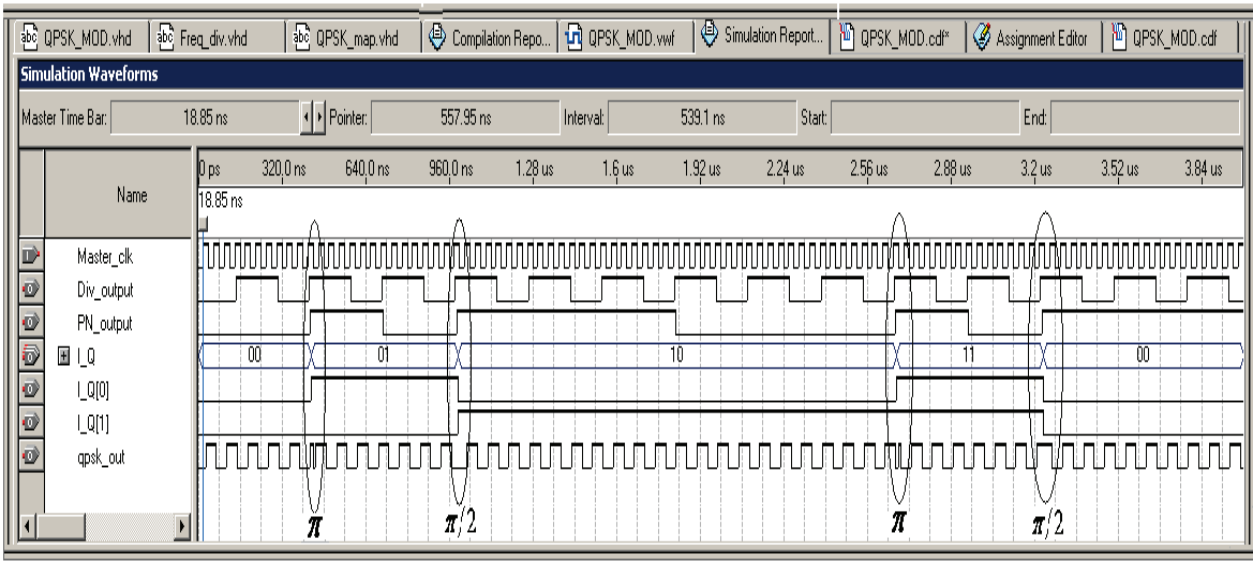


Figure (4.25) the simulation waveforms of VHDL QPSK modulator

4.5.2.3 Carrier Phase Shifter Modulator efficient Design

The carrier signal is the critical element in the design of the digital modulator, which affects the efficiency and the performance of the modulator. For a robust modulator design in digital techniques, the errors and delay in carrier signals are most important in the design.

The carrier phase shifter was programmed with VHDL code in structural design. The structural and behavioral blocks diagrams of the VHDL code for the carrier phase shifter are shown in Figure (4.26) and Figure (4.27) respectively. The simulation results for the synthesis of the carrier shifters suffer from the delay in signals. The waveforms of the carrier outputs signals are demonstrated in Figure (4.28). However, the delay time is critical in the inverted shift signals (180º) and (270º), this delay affects the transition of the output signal for the modulator. Obviously, the time delay in the phase shift carrier was calculated, and was about 5ns. This delay was due to inverters output of the carrier in the waveforms. However, the phase delay in carrier signals was measured to minimize the phase error.

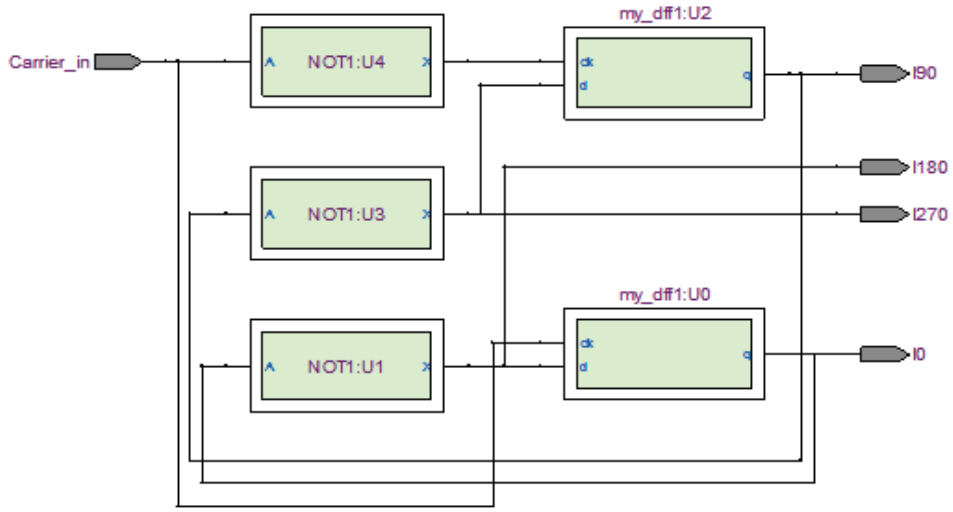


Figure (4.26) Structural VHDL Simulation for carrier phase shifter

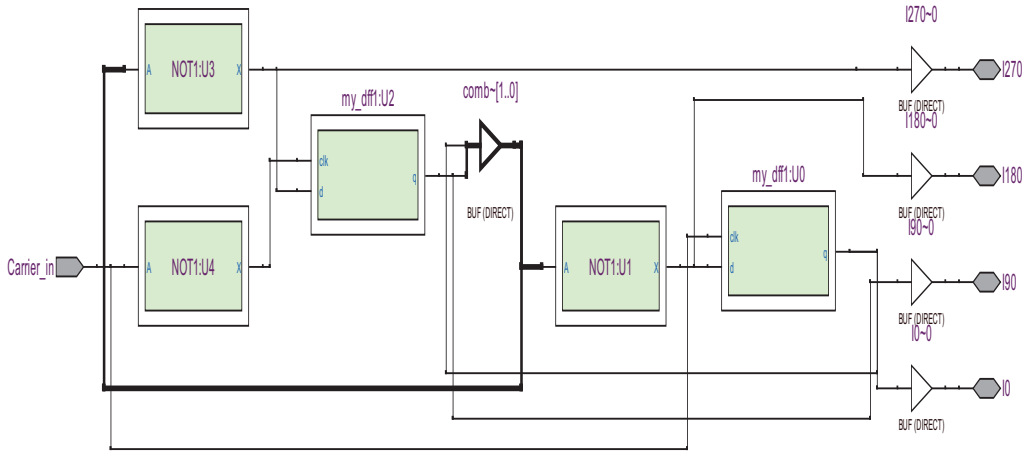


Figure (4.27) Behavioral VHDL Simulation for carrier phase shifter

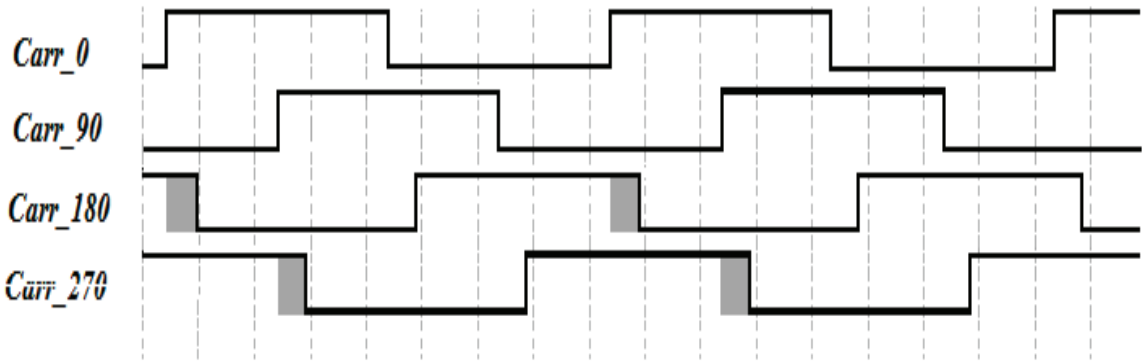


Figure (4.28) the waveforms delay in carrier phase shifters

The modified design is presented in Figure (4.29), which cancelled the delay at outputs (zero delay) by modifying the VHDL code; the output waveforms result are demonstrated in Figure (4.30). The modified delay for the phase shifter code is illustrated in Appendix (B).

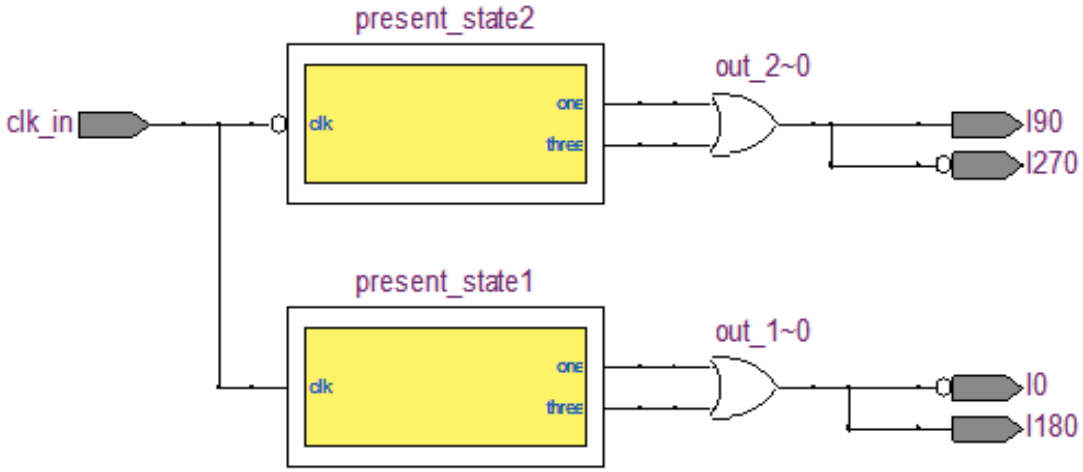


Figure (4.29) behavioral Simulation of VHDL carrier phase shifter

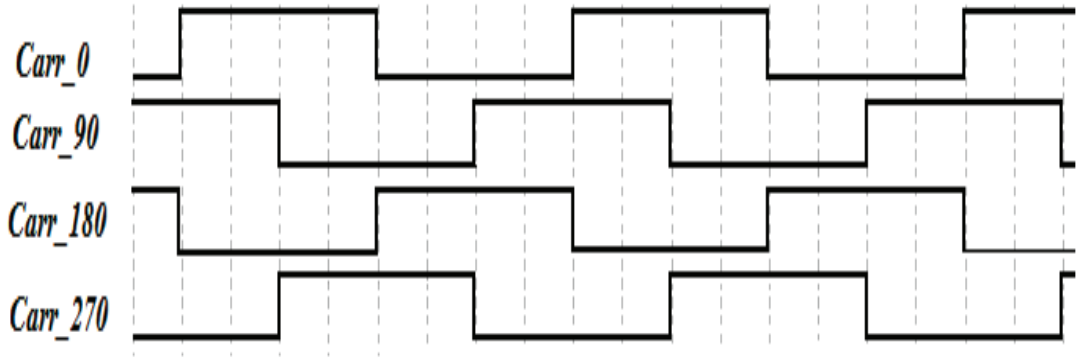


Figure (4.30) the simulation waveforms for modified carrier phase shifter

4.6 8-PSK Modulator Digital

4.6.1 Module Method Design

The higher level of direct digital modulations is the 8PSK. As a result of extending the symbol rate, the separation between phase states becomes smaller and susceptibility to noise increases. The 8PSK modulator is described as deploying, the highest order PSK constellation. The challenge in digital modulation schemes is for a perfect synthesis design to minimize the processing circuit with compatible hardware. In practice, there are different topologies to synthesize the 8PSK modulator, which is mostly used in mobile communication and in modern telecommunication. The modulator block diagram is shown in Figure (4.31), which is possible for synthesis with the FPGA technologies. The signal constellation usually deals with binary data that means the number of symbols, the symbols probabilities constellation diagram for the 8PSK modulator as shown in Figure (4.32).

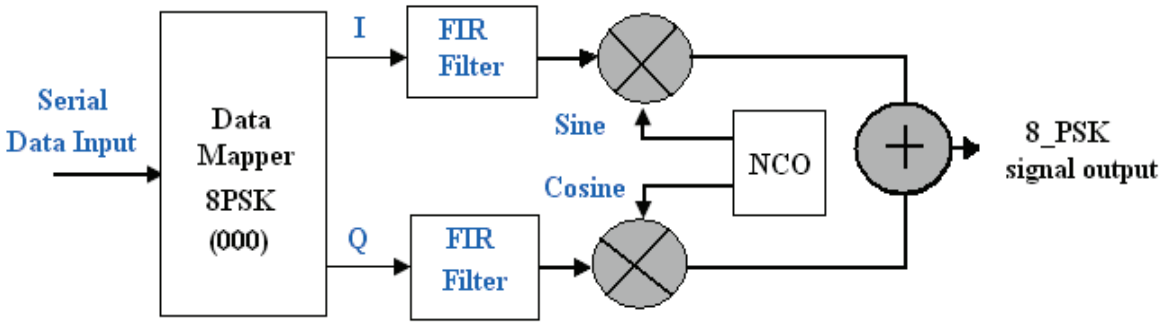


Figure (4.31) the diagram for 8psk modulator

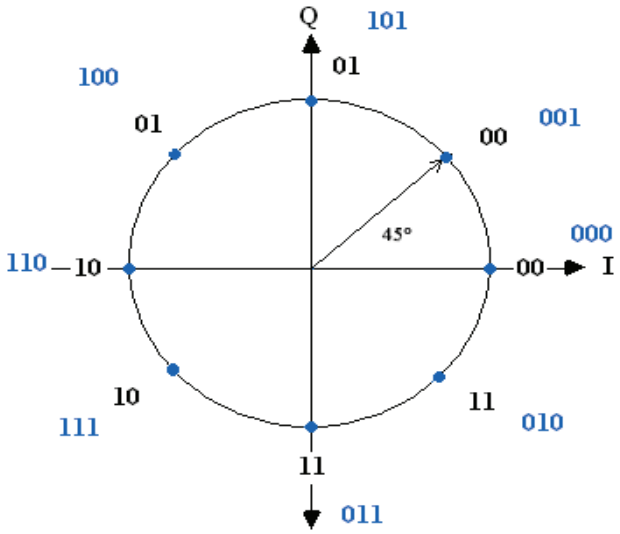


Figure (4.32) the constellation diagram of 8PSK modulator

4.6.2 Module Simulation

4.6.2.1 8PSK Modulator MATLAB/Simulink

The 8psk proposed digital n-PSK modulator was evaluated when generating a digital signal. This modulator was simulated with MATLAB/Simulink environment to validate the modulator specification of digital scheme. Generally, to compare the digital modulators, the three most common three schemes were overviewed. The first modulator is BPSK, which is composed of digital carrier phase shifter for discrete the phases (0°) and (180°), both signals are controlled by the input binary data to perform the transition of the BPSK signal. The second proposed modulator is QPSK, which consists of the carrier phase shifter, which shifts the input carrier into four different phase signals (0°), (90°), (180°) and(270°), and these are interfaced to the multiplexer. Whilst the data source is generated with PN-sequence, it feeds into data mapping to generate I and Q stream signals. The output is selected by the multiplexer, which provides the digital QPSK signal. The third proposed modulator is 8PSK, which is composed of eight discrete signals as (0°,45°, 90°,135°), (180°,225°, 270°, 315°). These carrier signals are controlled by the binary input data through a counter to generate ($2^n = 8$ where n=3), that performs the transition of the eight carrier signals data mapping. It is then interfaced into eight inputs multiplexer, and the output provides an 8PSK digital signal. However, we demonstrate in Figure (4.33) the principle of the proposed direct digital modulator 8-PSK. This type of technique simplifies the modulator to synthesize with FPGA or CPLD technologies, and may be useful for biomedical proposes. The multiplexer output for the digital 8PSK signal can be expressed in equation (4.9) below as:

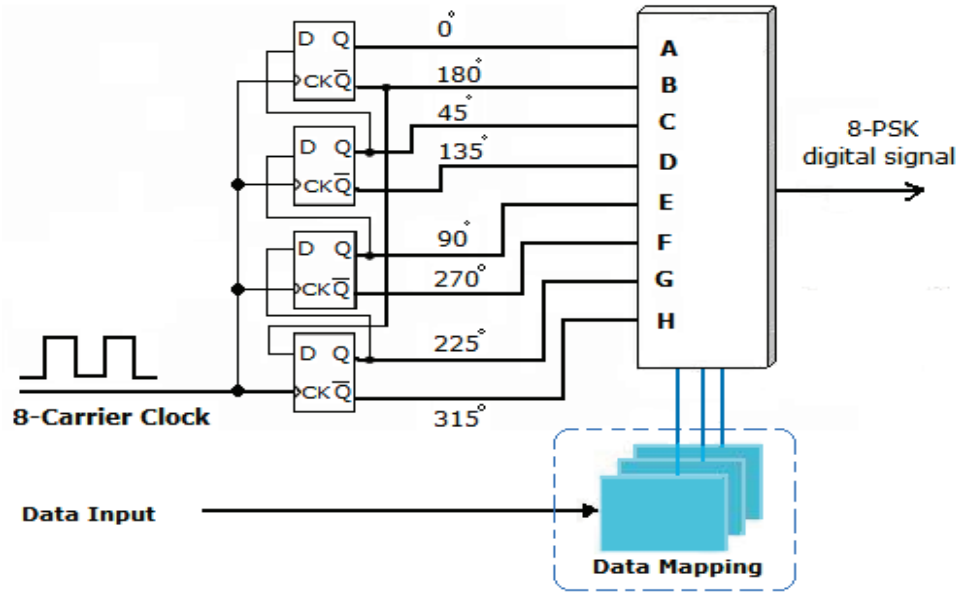


Figure (4.33) the principle of direct digital modulator 8PSK in FPGA/CPLD

$$Mux_{out} = C_0 \bar{D}_0 \bar{D}_1 \bar{D}_2 + C_{180} \bar{D}_0 \bar{D}_1 D_2 + C_{45} \bar{D}_0 \bar{D}_1 \bar{D}_2 + C_{135} \bar{D}_0 \bar{D}_1 \bar{D}_2 + C_{90} \bar{D}_0 \bar{D}_1 \bar{D}_2 + C_{225} \bar{D}_0 \bar{D}_1 \bar{D}_2 + C_{270} D_0 D_1 D_2 \quad (4.9)$$

The carrier phase shifter generates the eight phase clocks as (0°,180°,90°,135°, 45°, 225°, 270°, 315°), where the data mapping provides the essential transitions of the carrier. The multiplexer is a selectable switch which is interfaced from the carrier phase shifter and mapped data; the output provided is an 8psk digital signal. In practice, the modulator was synthesised in simulink as shown in Figure (4.34). However, the critical element for design a digital modulator is the carrier phase shifters, which generate the phase difference between carrier signals with minimum delay, where the delay is reduces the modulator efficiency in digital processing. The clock frequency for this type of phase shifter needs to be four times higher than the shifted frequency, where the carrier divided by ($\pi/4$) to generate the phase shift between each carrier such as: sin($\omega t + \pi/4$) ~ sin(ωt +7π/4). Furthermore, to generate the frequency 12.58MHz it needs the frequency to be about 50MHz. The FFT spectrum of the modulator is demonstrated in Figure (4.35). The simulation result for the 8PSK output waveforms of the proposed digital scheme is demonstrated in Figure (4.36).

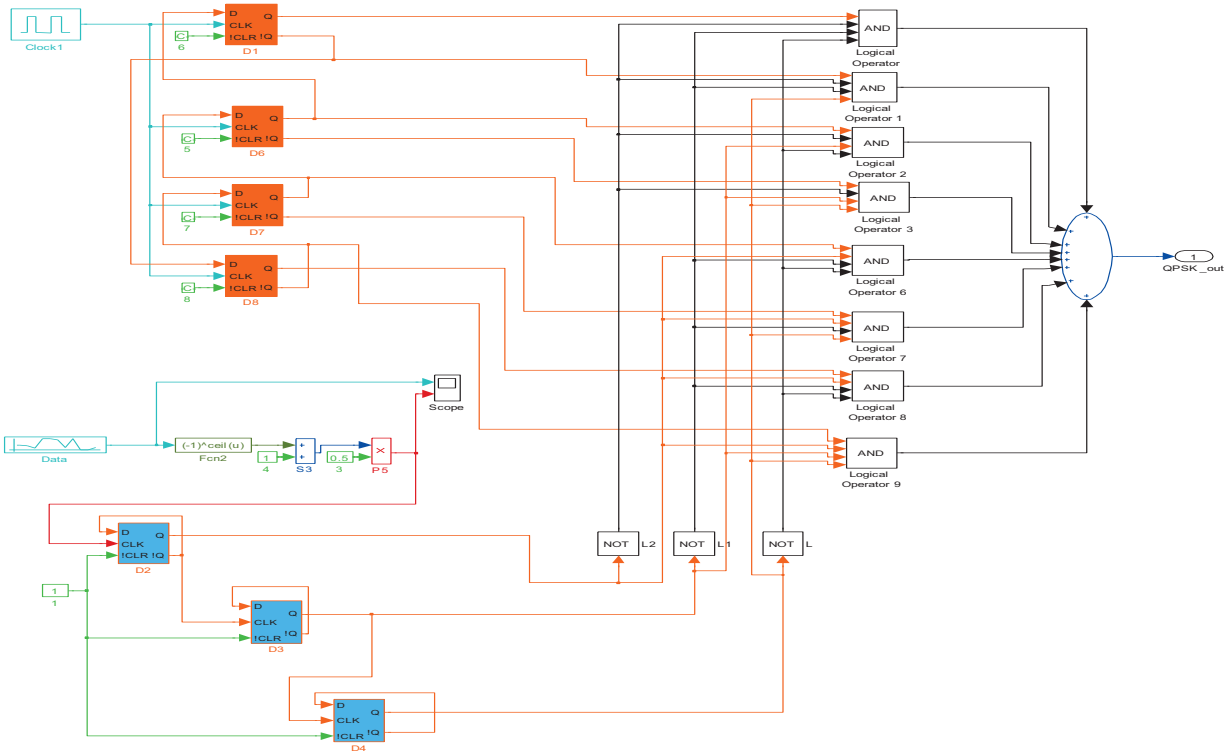


Figure (4.34) the simulation environment in MATLAB/Simulink
For proposed 8PSK modulator

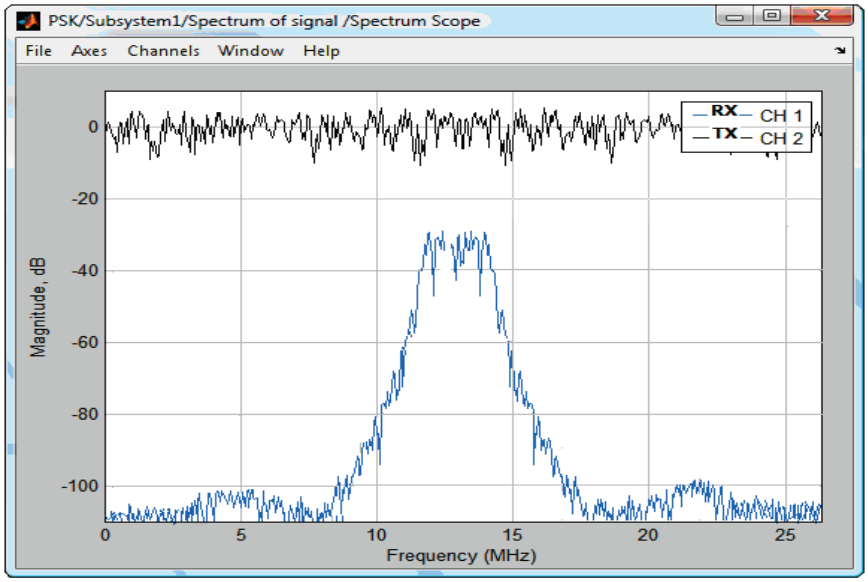


Figure (4.35) the spectrum of 8PSK transmission and receipt of signals at Data rate 2Mbps, carrier 12.5MHz

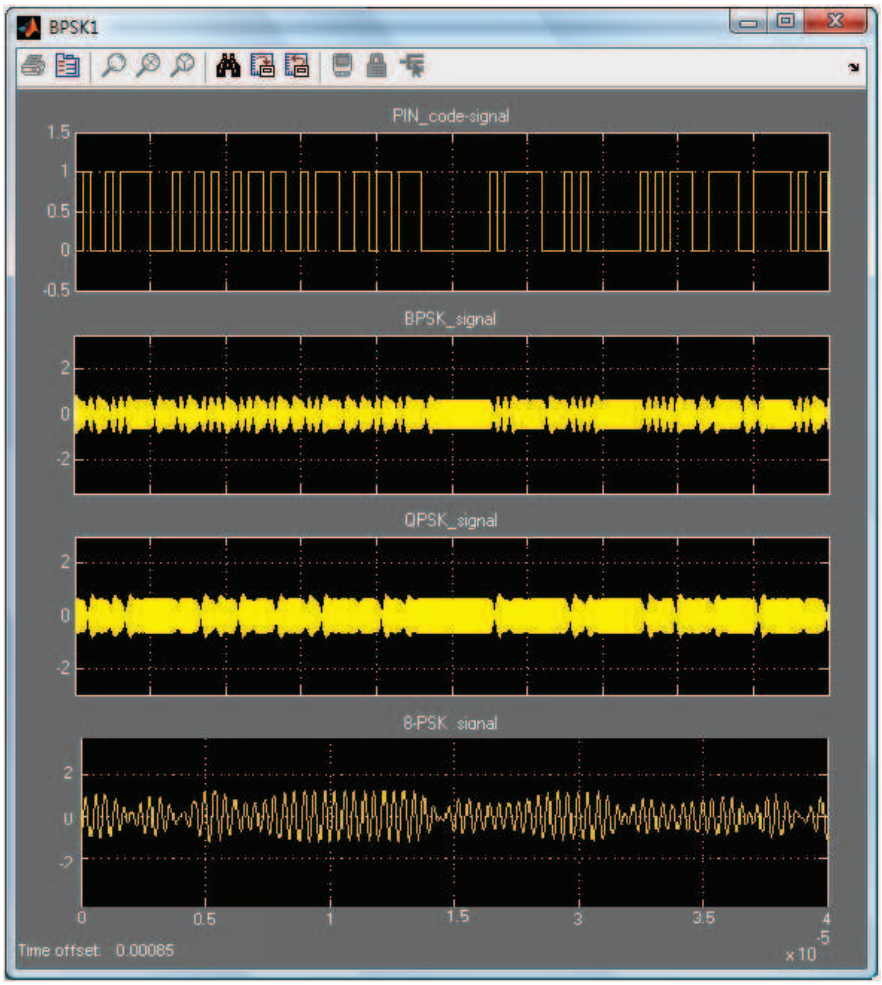


Figure (4.36) the simulation waveform results for Proposed 8PSK modulator

4.6.2.2 VHDL 8PSK Modulator Synthesis and Simulation

The 8PSK modulator was programmed with the VHDL code, and compared with two different synthesized methods, the structural and behavioral descriptions. The behavioral programming code simulation method of the 8PSK modulator is shown in Figure (4.37). The carrier frequency was generated from the local clock signal on the board, which operated at 25.175 MHz. The information signal was reduced to 2 MHz by the frequency divider, and then fed into the random PN_sequence generator to generate a sequence of data for simulation purposes. The simulation waveform result for the module is shown in Figure (4.38), which demonstrates the transition of the digital signal for 8PSK modulator output.

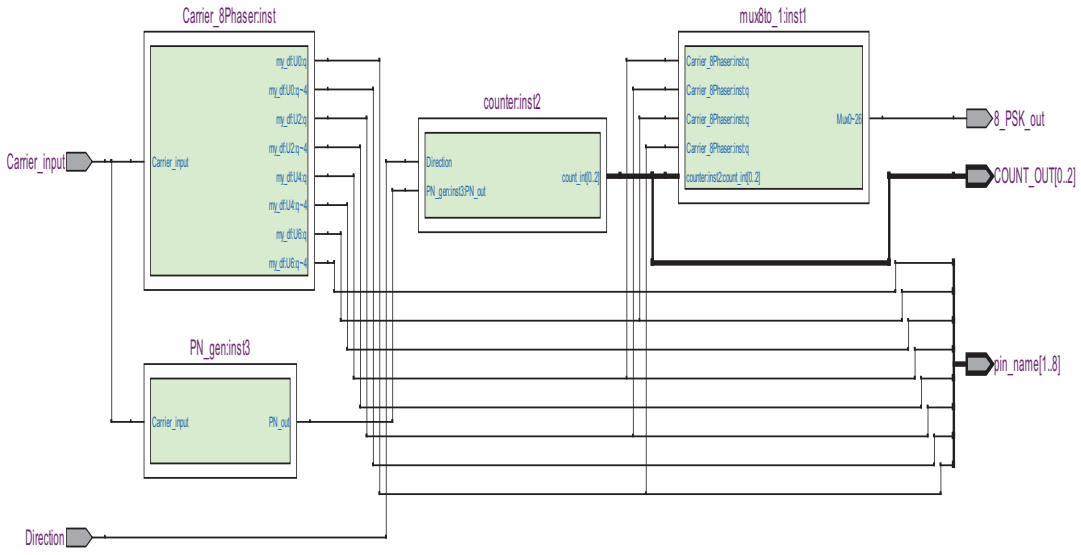


Figure (4.37) behavioral simulation for VHDL digital 8PSK modulator

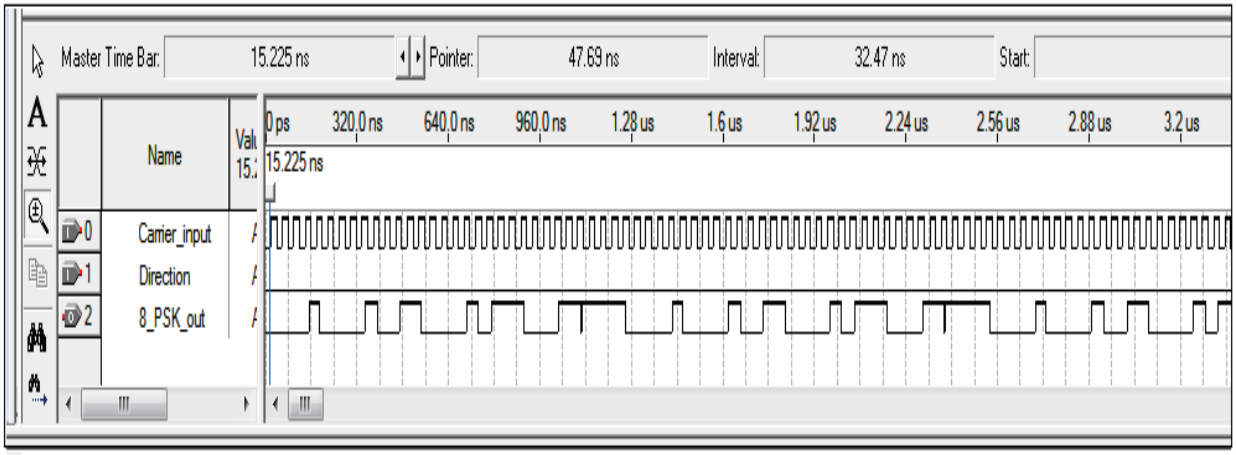


Figure (4.38) waveform simulation for 8PSK VHDL modulator

4.7 Experimental Lab measurements for VHDL modulators

4.7.1 BPSK modulator

The Altera development kit conducted the measurements performance for the proposed BPSK modulator, to test the VHDL code modulator and compare the performance with the simulated BPSK modulation. The desired carrier frequency 12.5 MHz was generated from the master clock on the circuit board operating at 25.175 MHz. The carrier phase shifter acquires two discrete phases (0º), (π), the PN-sequence code source generated with VHDL code inside the CPLD chip at 2Mbps. The Agilent digital demodulator (E8048A VXI) was used to receive the filtered RF BPSK signal. The lab measurement result is shown in Figure (4.39) for the spectrum transmitter signal. However, the measurements for the received signal were demodulated with Agilent (E8408A) after being passed through passive LPF for harmonics separation; the results are shown in Figure (4.40), the constellation diagram of the BPSK at demodulator.

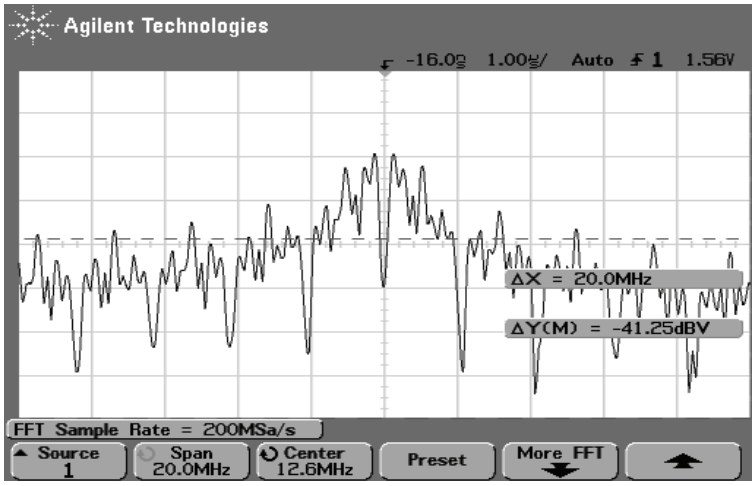


Figure (4.39) The Spectrum of BPSK transmitted signal at carrier 12.5MHz

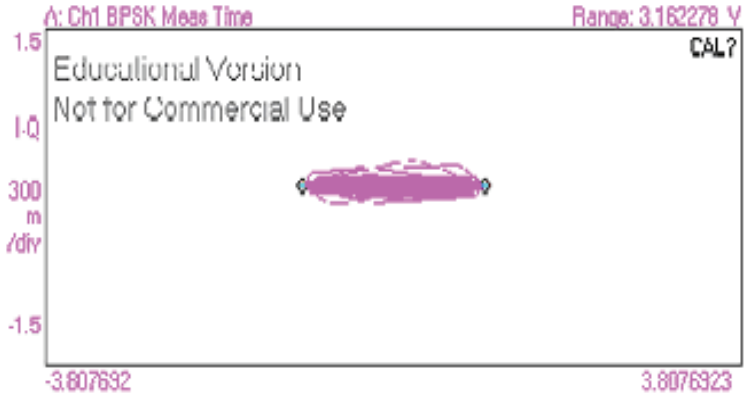


Figure (4.40) the constellation diagram of BPSK at demodulator using Agilent digital demodulator (E8408A)

Furthermore, the measurements were done over the inductive coupling link to test the proposed modulator, as shown in Figure (4.41), which demonstrates the Lab test bench for the BPSK VHDL modulator. The measurement result is illustrated in Figure (4.42) which shows the spectrum of the received signal through wireless coupling (a) and demodulated data (b).

Figure (4.41) the preliminary lab measurements with (E8408AVXI)
For the proposed BPSK VHDL modulator at over inductive link

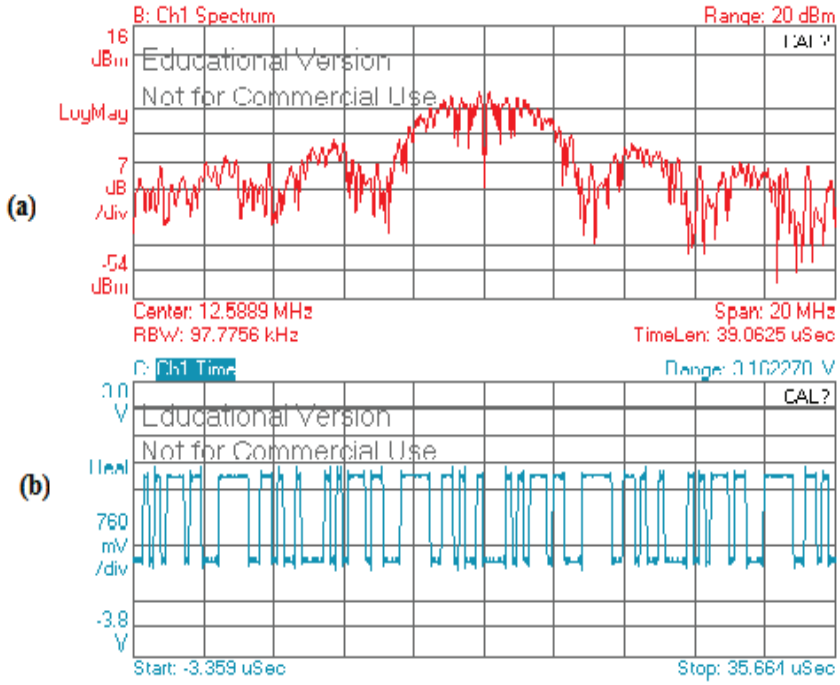


Figure (4.42) (a). The spectrum of Rx signal (b). Demodulated data (2Mbps)
received from the proposed VHDL modulator over inductive link

4.7.2 QPSK Modulator

The second lab measurement was provided for the QPSK modulator, conducted by the Altera development kit board, to evaluate the VHDL code modulator. The acquired four discrete states $(0, \pi/2, \pi, 3\pi/2)$ for the carrier phase shifter were tested, to evaluate any phase error for the phase shifter signals. The source of data was generated with VHDL code inside the CPLD at 2Mbps. However, the measurement spectrum of the Tx-QPSK modulator is demonstrated in Figure (4.43) after the modulated digital signal was passed through the passive LPF. Conversely, the performance was measured using Agilent education version to demodulate the received signal using a QPSK Demodulator. The demodulated information data, which was transmitted by VHDL modulator, is shown in the constellation diagram for QPSK Rx signal in Figure (4.44).

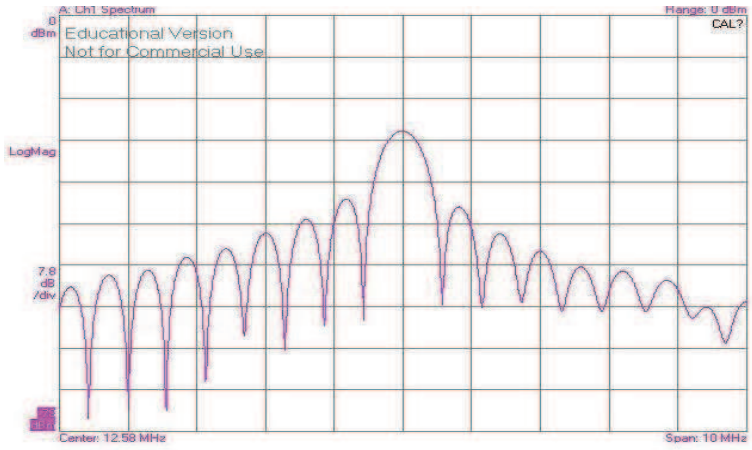


Figure (4.43) The TX Spectrum of the QPSK transmitted Signal at carrier 12.58MHz

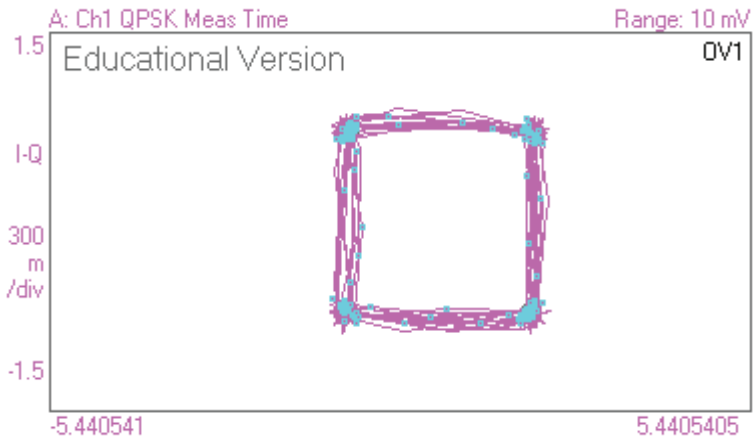


Figure (4.44) Constellation diagram of QPSK demodulator, received from the proposed VHDL QPSK modulator

The second lab measurements for the proposed VHDL QPSK modulator where conducted over a wireless inductive link, as depicted in Figure (4.45). The spectrum of the Rx QPSK demodulator (a) from the VHDL QPSK modulator, received over the inductive coupling link is illustrated in Figure (4.46), and (b) presents the demodulated information at 3Mbps.

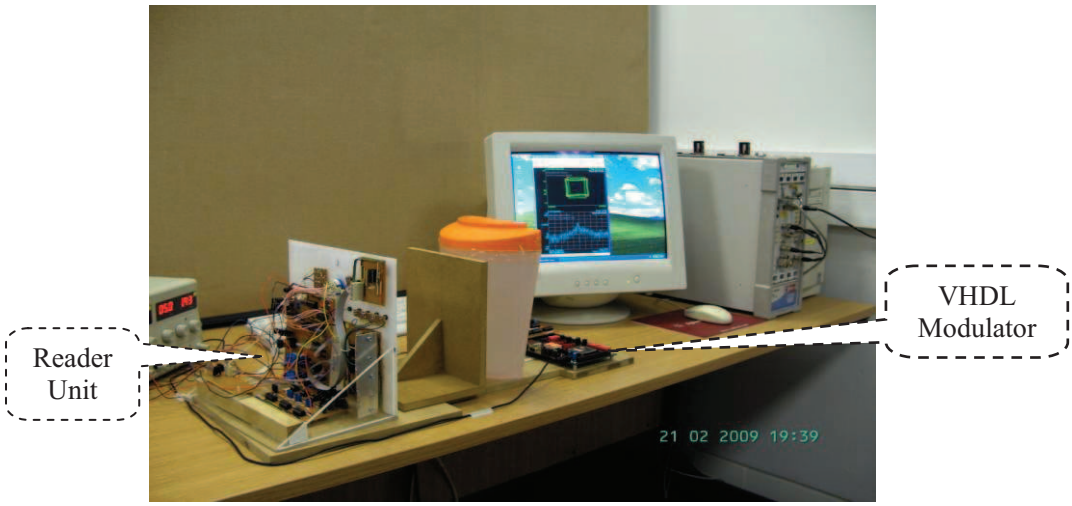


Figure (4.45) The Lab measurement for QPSK VHDL modulator over Inductive coupling link With Agilent, demodulator (E8408A)

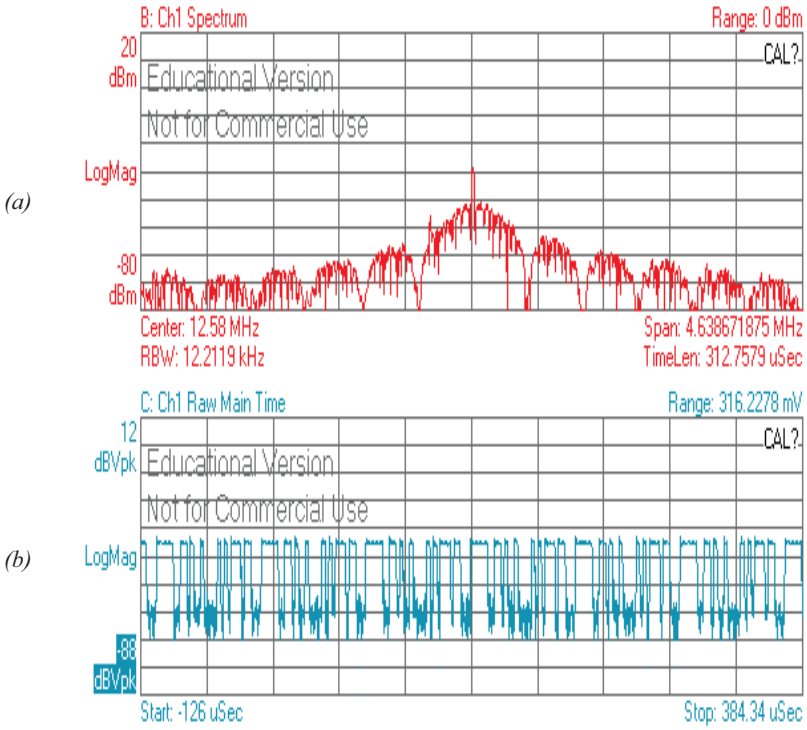


Figure (4.46) (a). The spectrum of Rx signal (b), demodulated data (3Mbps) Received from the proposed VHDL modulator at over inductive link

4.7.3 8PSK modulator

The third lab test measurements were performed for the 8PSK modulator, and were evaluated with MATLAB/simulation. The carrier frequency used the local clock signal, which operates at 25.175 MHz, and uses 6.2937 MHz for the carrier and 2MHz to generate the PN-sequence as data source. The carrier phase shifter was measured individually for the efficiency performance and phase delay testing. In addition, the data mapping was tested before being synthesized in the completed 8PSK modulator. In this section, the measurements performance conducted using the same previous tools for testing the VHDL code for 8PSK digital modulator. The Agilent digital demodulator (E8408AVXI) used to receive the RF 8PSK signal, and analyzed using the parameters of the transmitted signals. Generally, the spectrum of the generated VHDL-behavioral code of the 8PSK modulator is illustrated in Figure (4.47), where the measured the constellation diagram is illustrated in Figure (4.48).

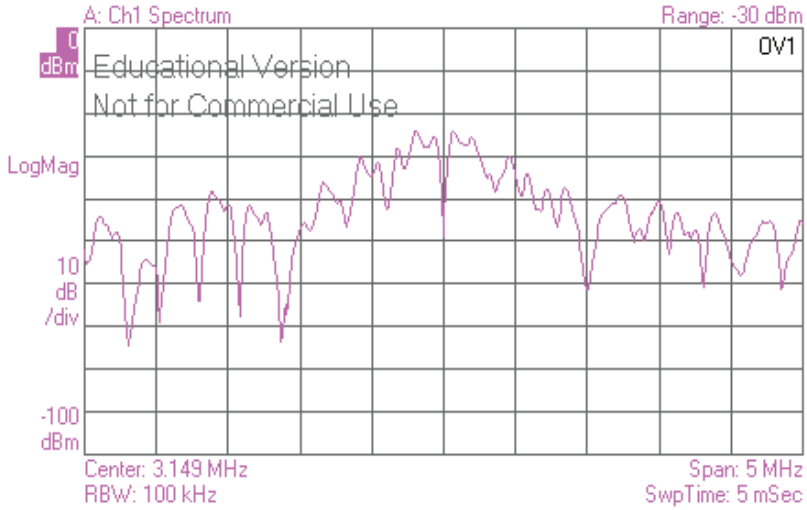


Figure (4.47) The TX Spectrum of the 8PSK transmitted Signal at carrier 12.50MHz and data 2MBps

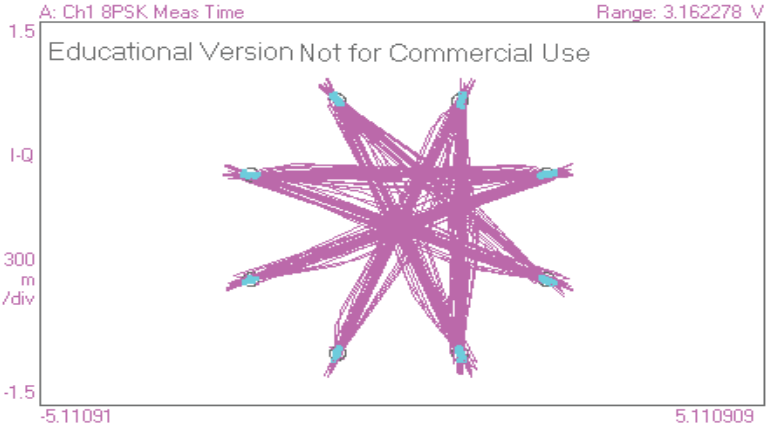


Figure (4.48) Constellation diagram of 8PSK demodulator Received from the proposed VHDL 8PSK modulator

4.8 Filter Investigation For Medical Purpose

Wireless transmission, cannot transmit the digital signal directly through a band-limited channel with original format without harmonics separation [173] [40]. The outputs have BPSK, QPSK or 8PSK digital modulated signals (Square Wave Form). Therefore, we needed to investigate and synthesize an analogue passive filter for this purpose, with zero power consumption. Two types of filter investigated, the Low pass Filter **LPF** and the Band Pass Filter **BPF**; they are appropriate for our work. In the simulation, the Butterworth LPF gave a better performance than other types of LPF, to eliminate the frequencies harmonics from the modulated digital signal, and consequently the Chebyshev II BPF is gave a better performance than other types of BPF as the second choice for appropriate filters for biodevices applications. However, the output signals yields by the filters were in analogue form, as demonstrated in Figure (4.49), where the VHDL modulated digital signal is presented in equations (4.8) and (4.9). This square input signal is filtered to pass the fundamental frequency ($f \pm data$) and remove the harmonics and DC component.

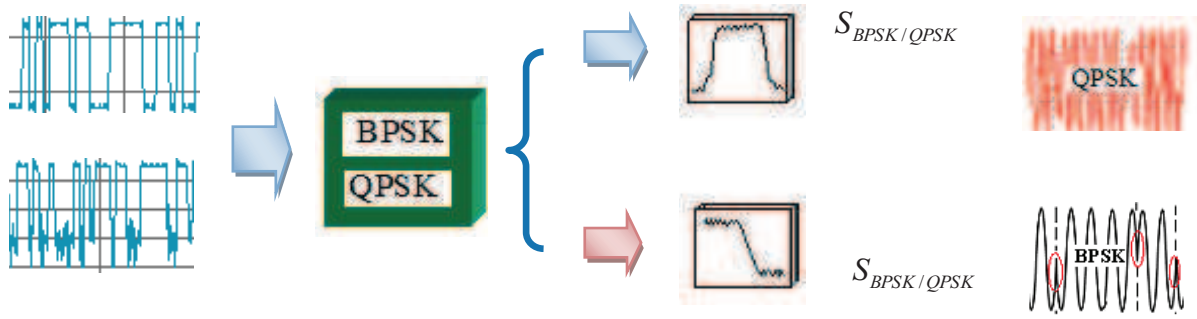


Figure (4.49) Two filters types used for harmonics eliminatation

$$Mux_{out} = carr_0 \cdot PN + carr_\pi \cdot \overline{PN} \tag{4.8}$$

$$Mux_{out} = \bar{I}\,\bar{Q} \cdot C_0 + \bar{I}\,Q \cdot C_{90} + I\,\bar{Q} \cdot_I C_{180} + I\,Q \cdot C_{270} \tag{4.9}$$

Three different types of digital modulators BPSK, QPSK, 8PSK were synthesised, and these schemes need an appropriate filter. It is essential to use an analogue passive filter “off-chip” to separate the harmonies and DC component, and reduce the circuit size and complexity, where the filter is implanted with the modulator in biomedical devices. Figure (4.50) shows different methods for the filtration. However, one of the disadvantages of digital filters is they need additional oscillation as sampling frequency, which increases the power consumption and size.

Additional investigation of the VHDL LPF showed that it needs a great deal of logic design and the kind of the CPLD chip that increases the power consumption [179]. Hence, as our target is a passive analogue filter, the simulation result is given for the Chebyshev I & II, if we select the BPF compared to others. The optimum LPF performance was the Butterworth type. Generally, the other types of filters are presented in table (4.0), rated as the best characteristic performance (BCP), or less characteristic performance (LCP), and weak characteristic performance (WCP), and not perfect performance (NPP), which compares the attenuation for harmonics separation (HS), that is the function in the filter order design.

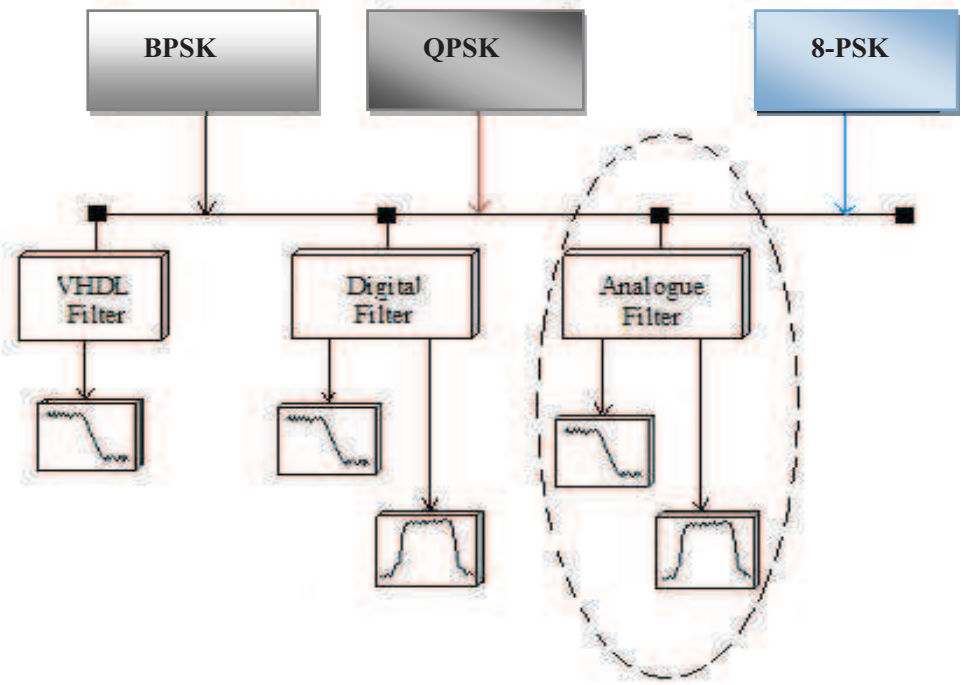


Figure (4.50) Different methods filters types used for harmonics elimination

	Investigated Filter Types for LPFilter and BPFilter									
	Butterworth		Chebyshev I		Chebyshev II		Elliptic		Besself	
	Carrier suppression	Harmonics suppression	Carrier suppression	Harmonics suppression	Carrier suppression	Harmonics suppression	Carrier suppression	Harmonics suppression	Carrier suppression	Harmonics suppression
LPF	-18dB	-12dB	-15dB	-20dB	-15dB	-20dB	-15dB	-15dB	-10dB	-15dB
BPF	-20dB	-20dB	-15dB	-18dB	-18dB	-25dB	-10dB	-15dB	-10dB	-18dB

Table (4.0) comparison of the simulation results for harmonics elimination for pulse modulated Carrier at frequency 12.58 MHz, using different filter types

4.8.1 LP Filter Design and Simulation

An LP filter was investigated and deemed appropriate for our purpose; the Butterworth LPF showed given enhanced performance compared to other types of LP-filters, to eliminate the harmonics from the BPSK or QPSK digital modulated signals. Generally, the block diagram of the passive filter with digital modulator is demonstrated in Figure (4.51). The transfer function of the filter is the main important factor for the filter design, which describes the filter specification. In a practical design to reduce the component circuits of the filter, we synthesized a low pass filter, which considered the data bandwidth and created less distortion by the filter. The proposed circuit diagram is shown in Figure (4.55), where the transfer function is expressed in equations (4.10), (4.11) and (4.12).

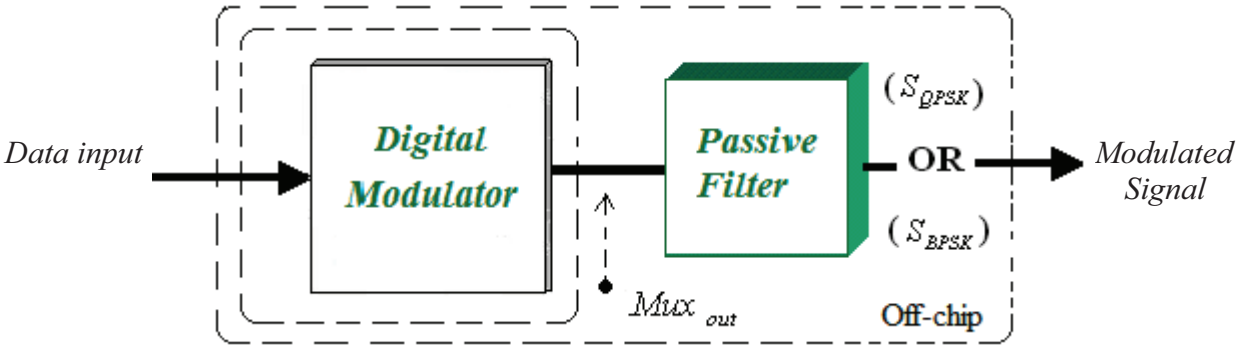


Figure (4.51) the proposed passive filter design with digital modulator

$$H(j\omega) = \frac{S_{QPSK}(j\omega)}{Mux_{out}(j\omega)} \tag{4.10}$$

$$H(j\omega) = \frac{S_{BPSK}(j\omega)}{Mux_{out}(j\omega)} \tag{4.11}$$

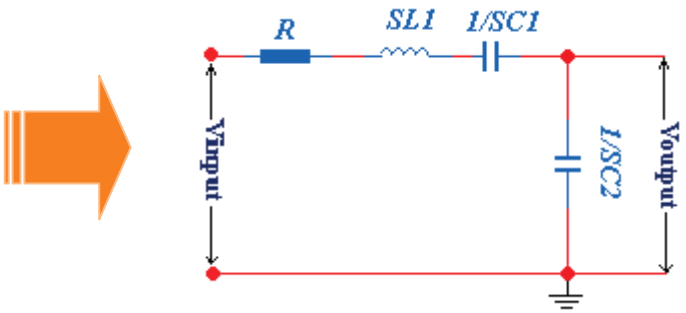


Figure (4.52) the second-order for LPF filter circuit

$$H(s) = \frac{1}{S^2 LC_2 + SRC_2 + C_2/C_1 + 1} \tag{4.12}$$

The simulation indicated different performance between Butterworth and Chebyshev LPF, when considering the input impedance of the source instead of load impedance. There are three different cases as shown in (4.13). In communication circuits, the matching load impedance is 50Ω, with the antenna part, which is obtained by the maximum transfer power. Generally, the block diagram for matching impedance with antenna is shown in Figure (4.53).

$$\left.\begin{array}{l} \textit{Input impedance is higher than} > \textit{Load} \\ \textit{Input impedance is lower than} < \textit{Load} \\ \textit{Input impedance is} = \textit{Load} \end{array}\right\} \qquad (4.13)$$

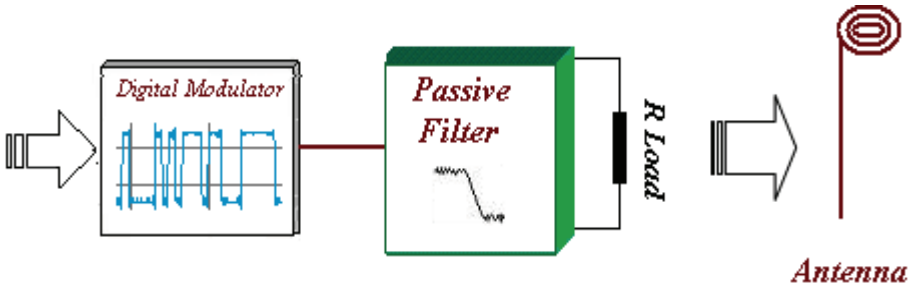


Figure (4.53) the matching simulation between filter and antenna

Our prototype analogue filter was synthesized with a Butterworth 4th order to filter the input of both BPSK and QPSK digital signals. The MATLAB/Simulink simulation is demonstrated in Figure (4.54), and demonstrates the response of the LPF filter compared with the Butterworth and Chebyshev **I** filters in 4th order design.

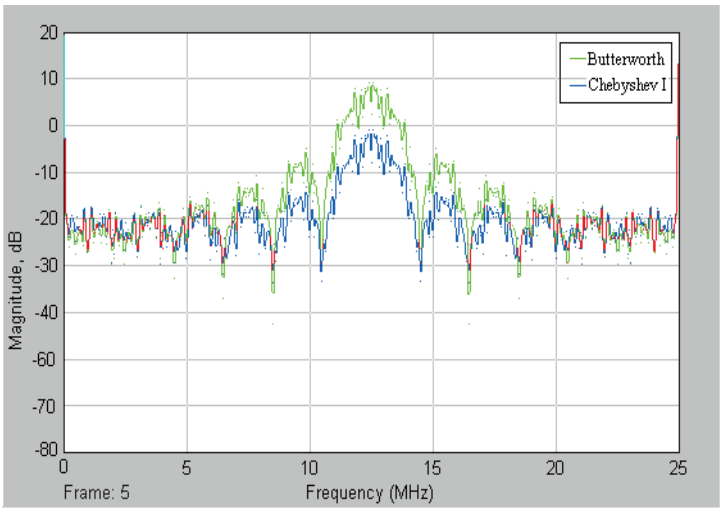


Figure (4.54) The LPF simulation with MATLAB/Simulink

4.8.2 BP-Filter Design and Simulation

The BPF was the second choice for our work. Generally, the basic function of the filter is demonstrated in Figure (4.55). Different types of band pass filters are appropriate for our work; the Chebyshev I, II and Elliptic are the three filters, which were investigated. Our selected filter was an analogue passive Chebyshev II BPF Filter, LC filter 4^{th} order. The simulation result with MATLAB/Simulink FFT is presented in Figure (4.56), which compares the Chebyshev I, Chebyshev II and Elliptic performance and specification, showing that they give they a high separation, over 50dB.

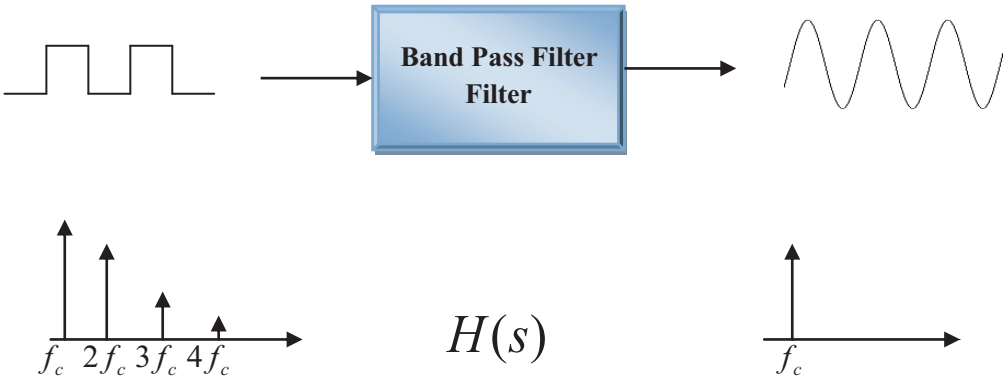


Figure (4.55) The BPF principle for attenuation of the harmonics

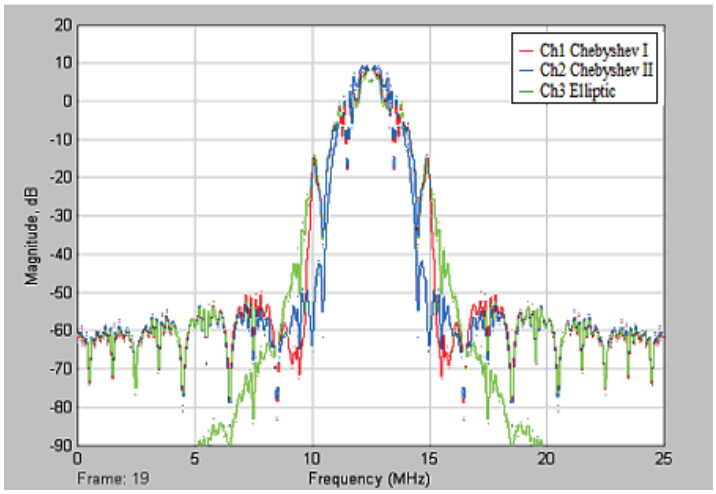


Figure (4.56) The BPF simulation with MATLAB/Simulink for (Chebyshev I, Chebyshev II, Elliptic)

Further, the simulations were performed with MATLAB/simulink to evaluate the filters specification for digital modulators signals. The five types of investigated filters were simulated and the analogue output signals are depicted in figure (4.57).

These are the analogue waveform signals after being filtered.

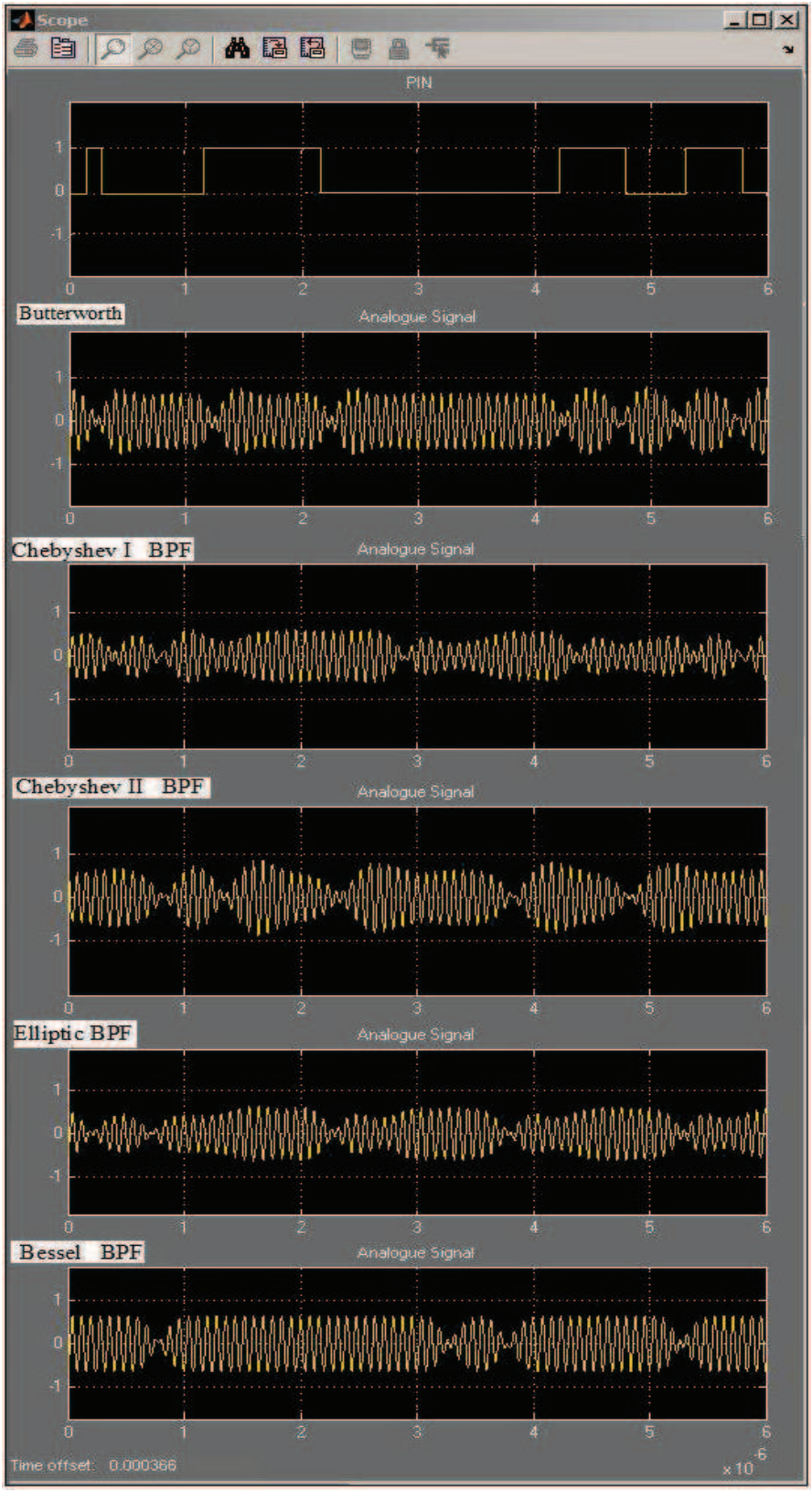


Figure (4.57) filtered analogue waveforms simulation with MATLAB

4.8.3 Filter Lab Measurements Results

We have investigated two prototype filters, the LPF and BPF, in simulation the BPF showed a better performance characteristic then LPF, especially with modulated signal. Conversely, the Lab test bench is illustrated in Figure (4.58). The Agilent (E8257D) function generator was interfaced to the Altera board that can generate a random PN-sequence as a data source. The second option is interfaced with a generator circuit for PN-sequence or programmed with VHDL code. The Agilent digital demodulator (E8048A) was used as a demodulator to demodulate the transmitted modulated signals from (BPSK) or (QPSK), in order to examine the performance of the proposed modulators. However, the Agilent scope (DS0818004A) was used to capture the inputs signals before they were filtered; the desired carrier signal was generated from the master clock on the circuit operates at 25.175 MHz. Generally, the function generator (Agilent E8257D) was used to generate a higher frequency in ISM band for testing purpose. However, in this section, we provide the lab test measurements for the proposed filters, to test the proposed VHDL code modulators. The waveform measurement result for the BPSK modulator is shown in Figure (4.59;, the top signal represents the PN code input signal, while the second signal represents the BPSK digital signal, and the third signal the filtered transmitted signal via LPF.

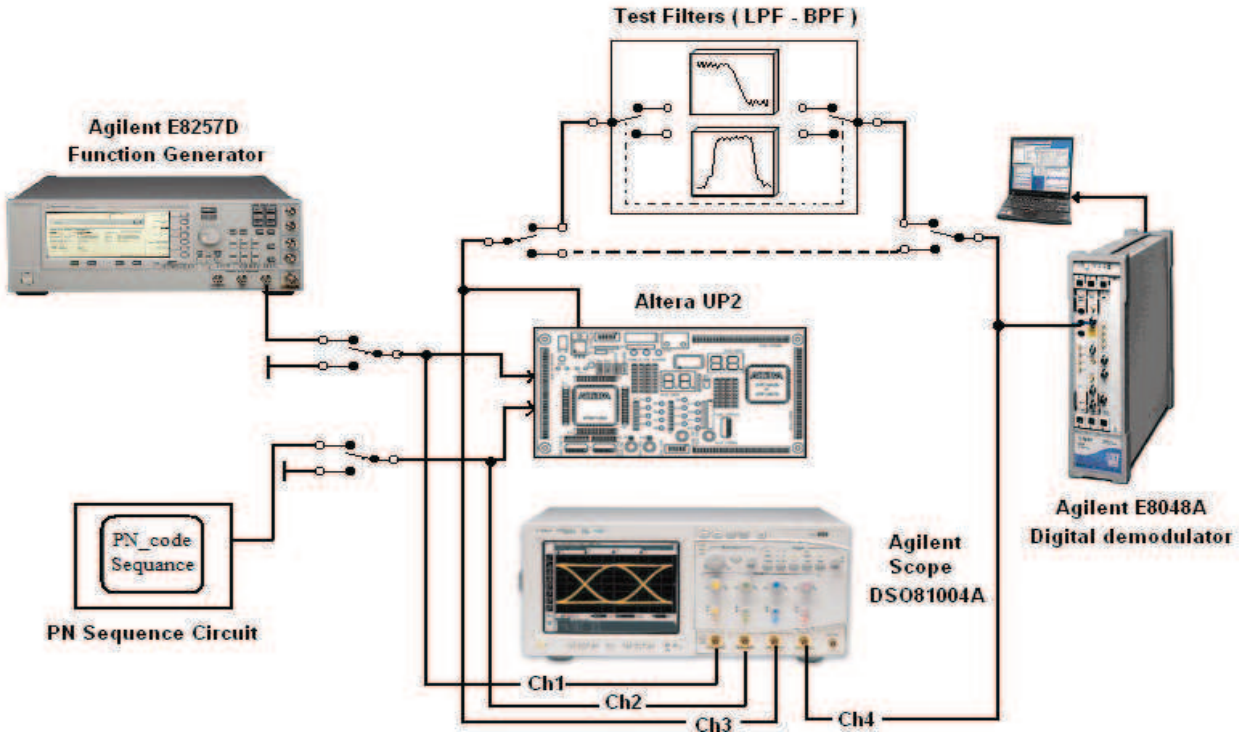


Figure (4.58) LAB measurment for filters (LPF,BPF) for TX-QPSK digital signal

The second waveform measurement results for the QPSK digital modulator, the QPSK digital signal filtered by LPF, and the output analogue signal are presented in Figure (4.60). The LPF was synthesized at $f_{cut} = f_{Carrier} \pm data$; the calculated values are critical for the cut-off frequency without any distortion by the transmitter signal.

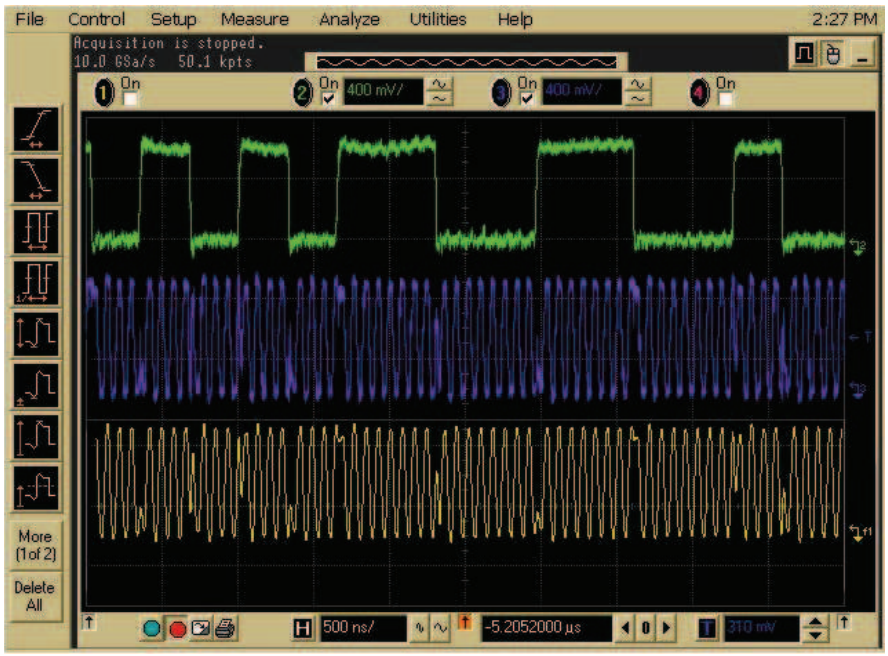


Figure (4.59) the output of VHDL BPSK modulator (Digital signal) and filtered signal at 12.5 MHz

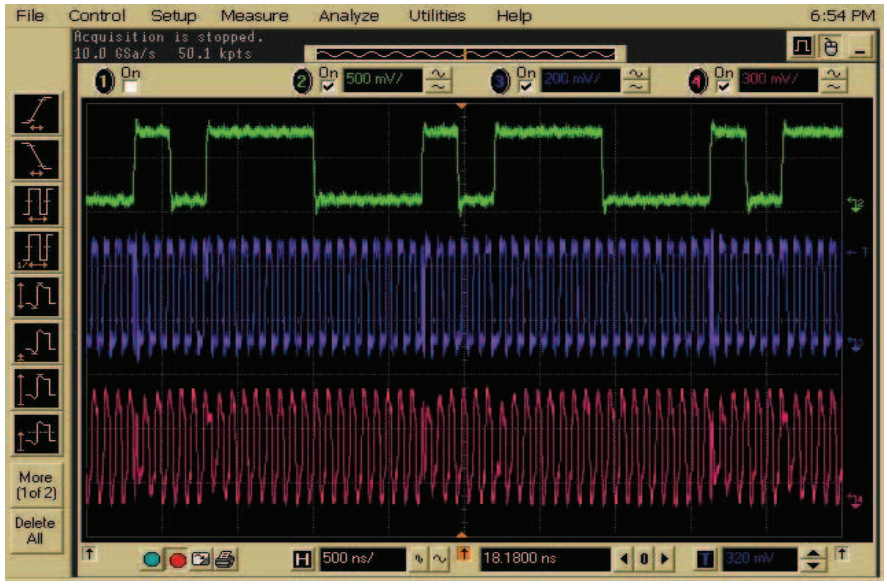


Figure (4.60) the output of the VHDL QPSK modulator filtered the QPSK TX signal by LPF

4.9 Summary and Results

This chapter concludes the new design for our proposed digital modulators, implemented with a practical and simple direct modulators solution for biomedical applications. The synthesised technical approach for direct digital modulators will increase the data rate and improve spectrum efficiency. A summary is as follows:

- **Synthesised Digital Modulators**

It is a challenge to convert the analogue modulator into digital forms and simplify the modulator, to be synthesised in the digital process and reduce the hardware circuit. However, the modules simulated in MATLAB/ Simulink environment have been successfully designed with VHDL programming code using Altera development kit. The target proposed VHDL modulator generates the QPSK signal directly from binary data, to be mapped for I and Q signals that control the carrier signal with a VHDL multiplexer code. The QPSK modulator was tested over the wireless inductive coupling, which gives better received data wirelessly up to 3Mbps over a distance of about 6.5cm. This technique offers a high data rate transmission over magnetic coupling link for biomedical devices, which requires a higher rate measured in real time. The lab measurement results for our proposed digital modulators BPSK, QPSK, and 8PSK are shown in Table (4.1). Practically, different CPLDs have been investigated as lower power consumption chips; the new ultra power is CPLD, which is provided by Altera MAX II CPLD (EPM240).

Modulator Characteristic	BPSK-Modulator	QPSK-Modulator	8PSK-Modulator
EVM	21.658% rms	2.9447% rms	13.643% rms
Phase Error	9.908 deg	0 deg	2.4383 deg
Frequency Error	51.509 KHz	75.950 KHz	4.9610KHz
Data rate over Magnetic coupling	1.3Mbps	2.5Mbps	3.5Mbps
Total micro cells Altera (EMP3064)	10%	19%	25%
Power consumption of the modulator	3.8mW	4.3mW	5.9mW

Table (4.1) the lab measurements results for the specifications of digital modulators

- Filter Design for Biomedical Applications

In general, the filter is the critical element in our design, where the size is important in the implant device, as the filter is implanted with the modulator in biodevices. Eventually, the passive filter was designed and simulated with MATLAB/Simulink. The LC Low pass Filter (LPF) and the Band Pass Filter (BPF) were investigated, simulated and synthesized. The simulation results for LPF Butterworth type showed better harmonics attenuation performance at about -25dB, compared to the Chebyshev I, and the Chebyshev II and Elliptic, which were simulated with the QPSK digital signal. Whilst the second choice was the Chebyshev II BPF Filter, which gave a better performance over other types of filters, as it had a high separation for the harmonics, over 50dB. Table (4.0) shows the simulation-summarised results for filter specifications for harmonics and carrier separations. However, the experimental measurements were presented at the carrier frequency 12.50MHz, and data rate up to 3.5Mbps, which presented better performance with bandwidth and carrier harmonics suppression over > 50dB for our prototype filters.

Finally, different topologies have been investigated for filters, for example the digital filter has disadvantages, such as needing additional oscillation in sampling frequency, which increases the power consumption and size. Whereas the filters implementation with VHDL is limited with only LPF and required twice frequency for the sampling process and considerable power, the VHDL filter has disadvantages when working in low frequencies and using high gate counts inside the CPLD. Conversely, these types of filter are not considered in our work, compared to passive filters.

Chapter

5

Biodevices System Design, Management and Measurements

Chapter Five

5. Biodevice System Overview

The biodevices communication system is magnetic proximity coupled between the reader and the implant part, which are tuned at the resonance frequency (f_o). In this work we choose the frequency 135 KHz as the RF power carrier. Generally, the reader is usually fixed part system, where the implant is the movement part within the human body. The reader coil provides an electromagnetic field toward the implant coil which is inside the human body. This magnetic field is modulated by an ASK modulator that is for transmitting the control data to the implant device. The induced AC voltage at the parallel tuned circuit LC is rectified from the RF received signal to provide the required DC voltage. However, for the maximum magnetic flux to be harvested by the implant coil, both coils have to be placed in parallel with respect to each other. The mutual coupling between the two loops coils are maximized in this condition, that gives the optimum magnetic flux Φ. In practice, there are several factors that could be affecting the efficiency of the system such as the orientation of the antenna coils and misalignment. Generally, we demonstrate in Figure (5.0) the biomedical system block diagram.

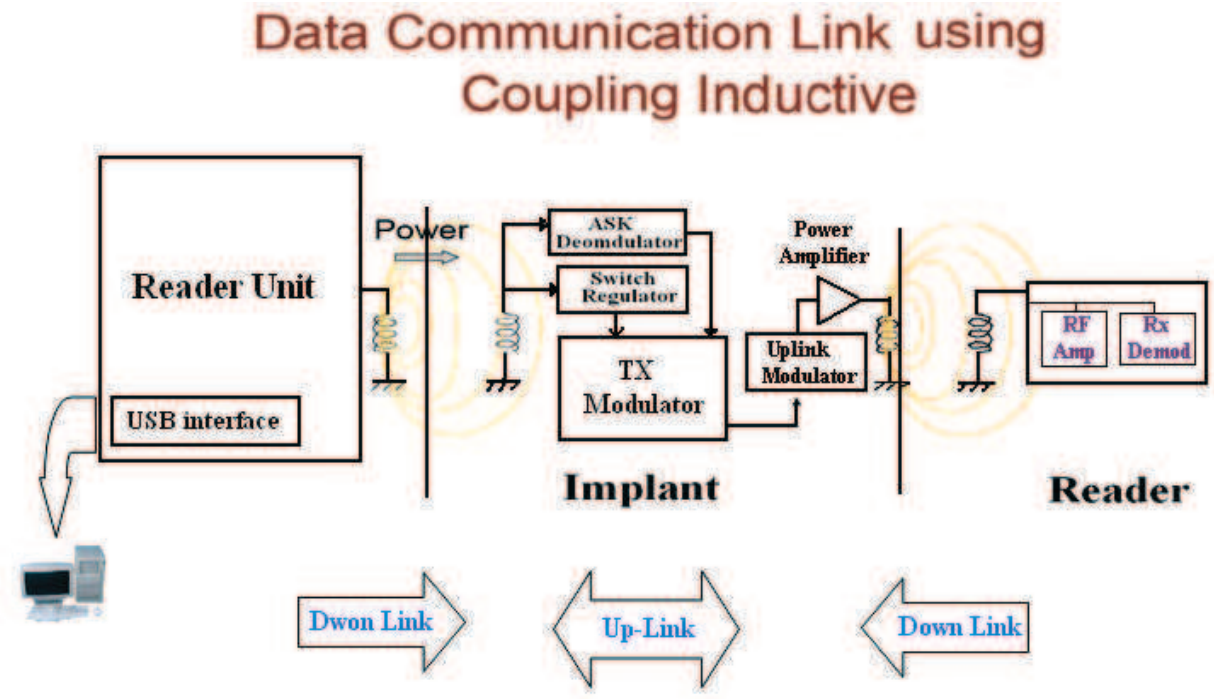


Figure (5.0) the block diagram of the biomedical system

The completed module has been synthesized and testing with different test equipments for evaluating the performance, for our proposed modulator technique as depicted in Figure (5.1).

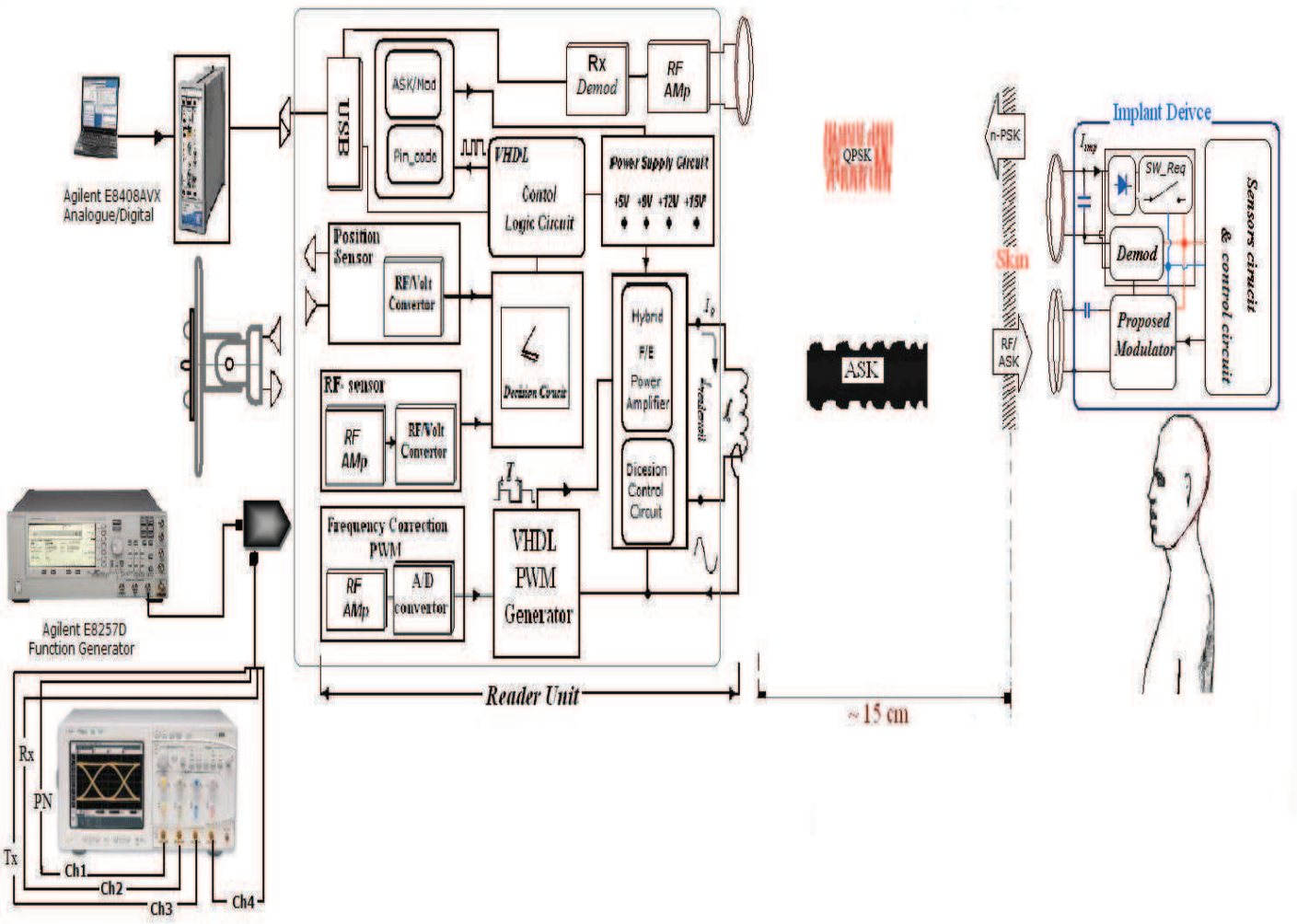


Figure (5.1) the prototype module for the biodevice system using
Inductive coupling link communication

5.1 Biodevices system and Experimental Lab Measurements

5.1.1 Downlink Reader Unit

In this section, where demonstrate the downlink part, which is the most important unit for delivering the RF electromagnetic power, into the implant through a wireless coupling link. The command information is conveyed to the implant, which is controlled remotely from outside the body. The Amplitude Shift keying (ASK) has been widely used in the wireless applications, such as RFID and Biomedical devices.

This is because it is a simple scheme and implies practical modulation and demodulation hardware. Comparing to the other schemes such as AM, FM or FSK where the demodulators are more complicated and consume a high power, as the demodulator is sharing the wireless received power with other circuits at the implant. The demodulator at the implant device is the most important element that is essential to be designed as a simple circuit and promoted for the low power consumption. In this chapter we will be introduce the ASK modulator as an alternative simple demodulator at the implant device comparing to the complexity of the demodulators used in biomedical devices. The amplitude of carrier frequency is modulated according to the logic state **0** or **1** of the data to be transmitted, where the depth modulation index can defined as a relation between the amplitudes of ASK signal as shown in Figure (5.2). The modulation index can be controlled by varying the relations between amplitudes (A+B) and (A-B), which represent the maximum and minimum amplitudes of the modulated signal. Generally, by changing ***A*** the amplitude and the duty cycle for the Fourier coefficient which of pulse signal ***D*** , that gives the change in modulation index as expressed in the equation (5.1), where the duty of pulse is ***D*** it can expressed in equations (5.3)and (5.4). However, the ASK modulator drives a class ***E*** power amplifier and is designed at 10% of modulation depth that provides a stable power transfer and independent data of modulation. In addition, this provides a constant RF signal into implant device; these advantages give high readability for DC voltage over different distances from the reader.

$$Modulation\ index = (A-B)\times(A+B)/100\% \tag{5.1}$$

$$DutyRatio = A/n\pi * \sin(n\pi D) \tag{5.2}$$

$$D = K/T \tag{5.3}$$

Where (K) is the pulse width, and (T) is the duration period time

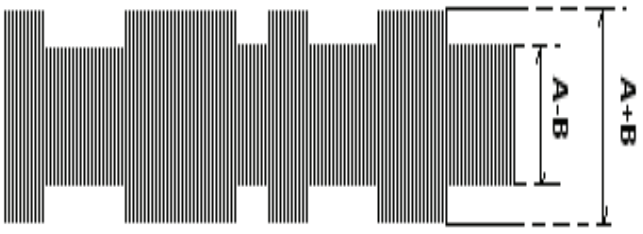


Figure (5.2) the modulation depth for ASK modulator

5.1.1.1 Lab Measurements for ASK Modulator

The architecture block diagram of the proposed ASK modulator is demonstrated in Figure (5.3). Hence, the PN-sequence influences the switch transistor, which control Q2 and Q3 to drive the voltage into the class ***E*** power amplifier. The lab measurements are illustrated in Figure (5.4) which shows the input PN-sequence data (b), and the RF transmitted modulated signal (a). The ASK transmitted and received data are illustrated in Figure (5.5). In addition, the measurements of data have given up to 50Kbps, at carrier frequency 135 KHz.

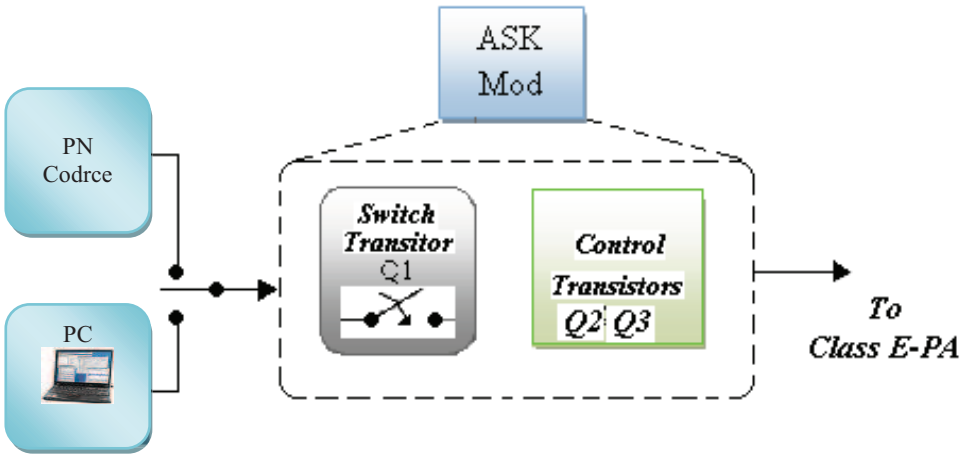


Figure (5.3) the block diagram of ASK modulator

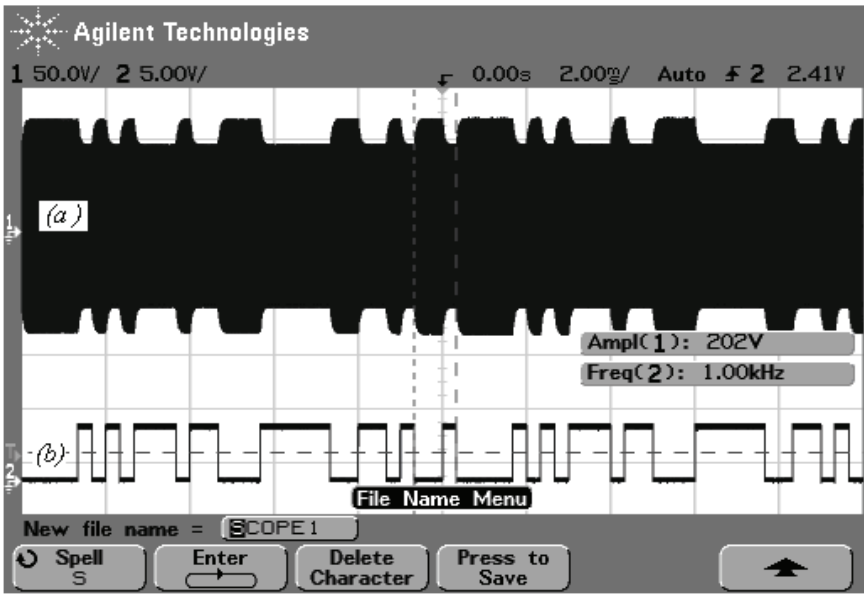


Figure (5.4) illustration of the ASK modulator (a),
TX-PN code signal (b)

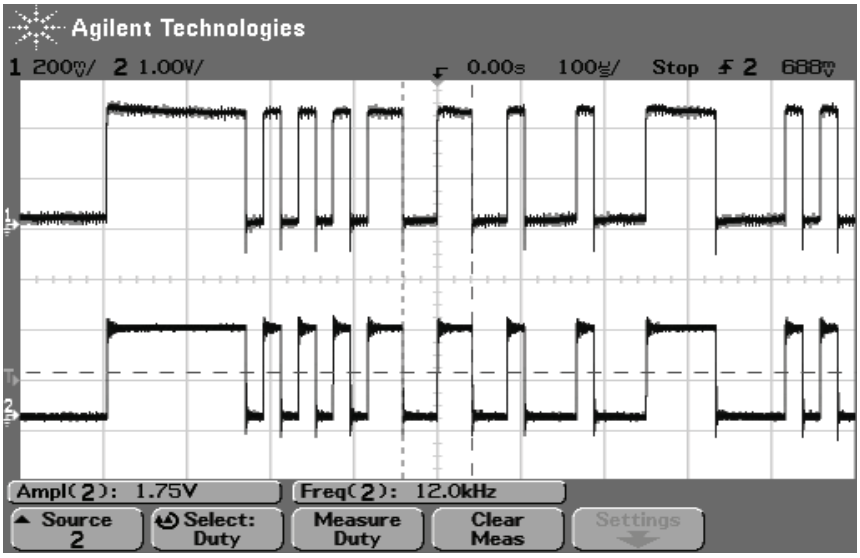


Figure (5.5) Tx PN data (a), (b) Demodulated data output

5.1.1.2 Hybrid Power amplifiers Class F/E

We introduce a new hybrid power amplifier (HPA) that uses the PWM technique to improve the power efficiency of the PA, and reduces the hardware implementation at the reader unit. The Hybrid-PA combines the tuning network circuits and uses a selectable switch to choose the desired amplifier. In our work we synthesized an ASK modulator for driving Class E-PA, which additionally provides wireless power, whether data is present or not. The control logic circuit has been designed to control the change over switches. It needs a control logic circuit (CLC), which is capable of controlling the selectable amplifier. Typically, the CLC drives the relay circuit. In addition, the feedback loop circuit captures the transmitted RF signal modulated or un-modulated, to monitor the carrier frequency signal, and perform the changeover between both amplifiers. The architecture block diagram of the proposed control system is demonstrated in Figure (5.6). The truth table demonstrates the state logic, where the circuit was synthesized and simulated in VHDL Table (5.0).

Enc-E/F	PC	Relay1	Relay2	Relay3	Relay4
E-On	-	1	1	1	PN/PC
E-Off	-	0	0	0	PN/PC
F-On	-	1	1	1	PN/PC
F-Off	-	0	0	0	PN/PC

Table (5.0) the truth table of the proposed control circuit

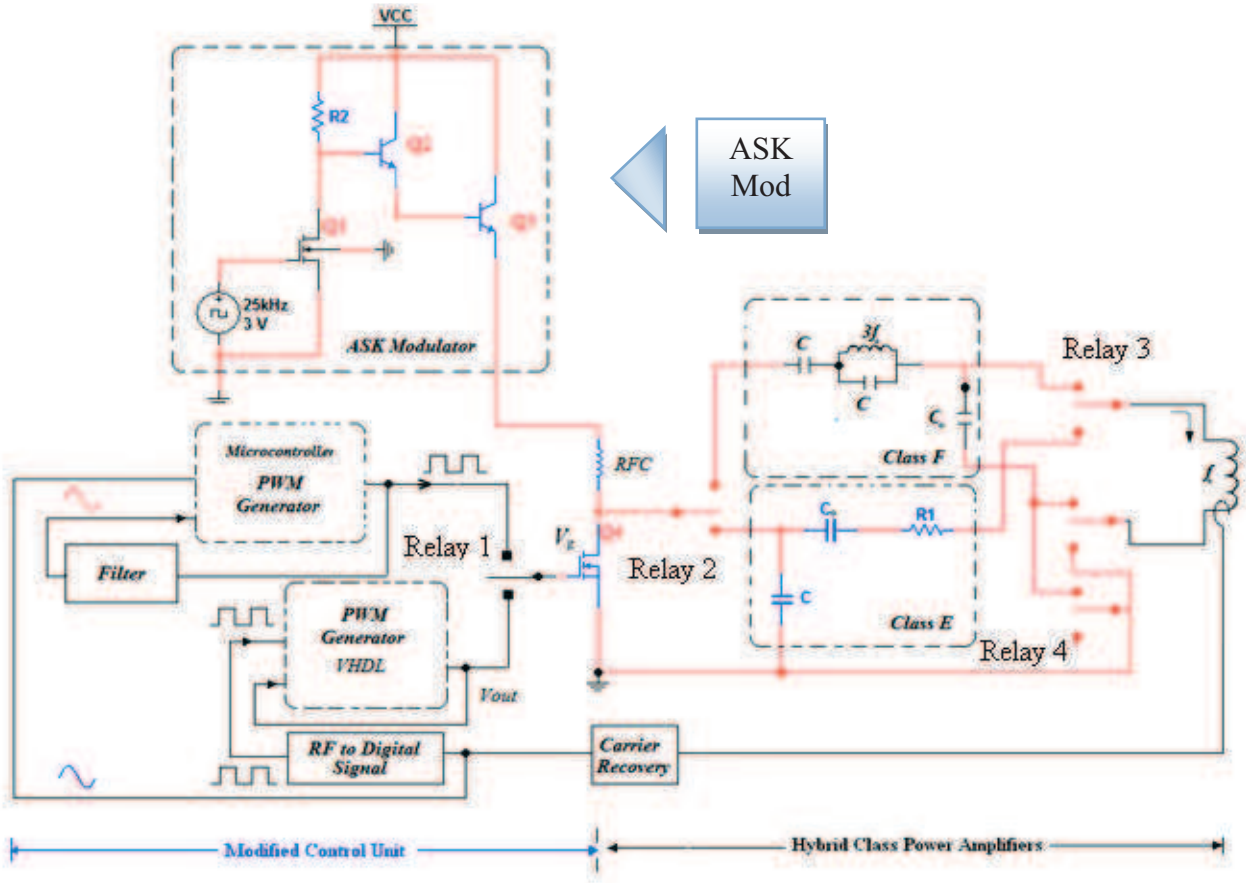


Figure (5.6) diagram of the hybrid Class E/F power amplifiers circuit

Eventually, the control command data can be interfaced from the PC to the reader through the ASK modulator, and also it can select one of the power amplifiers class E or F. However, the main goal of synthesis the hybrid power amplifier is to reduce the hardware circuit and better improves the transmitter's power efficiency. The control logic circuit can be implemented with a VHDL digital design, but generating the ASK signal is difficult to perform with the ASK modulator designed in digital form. However, the circuit can be divided into three parts: the ASK modulator, the RF carrier generator at 135 kHz and power filters networks and the control auxiliary circuit which performed the control logic for the class power amplifiers selection **E** or **F**. Additionally, the PN-sequence and the control logic was modified and synthesized with VHDL for reducing the hardware circuits.

5.1.1.3 Control Logic Circuit (A)

The logic control circuit was implemented with VHDL code to perform the function of table (5.0), that is, reducing the hardware circuits and it can be re-configured and updated.

Obviously, the control unit was synthesized with a microcontroller the first time and then we modified the design with CPLD, as appropriate for our application. However, the complete control circuit was synthesised with VHDL code and then simulated and loaded in CPLD to test the code of the circuit. Figure (5.7) shows the Inputs/Outputs implemented with CPLD, which are interfaced to the Error Detection Circuit (EDC).

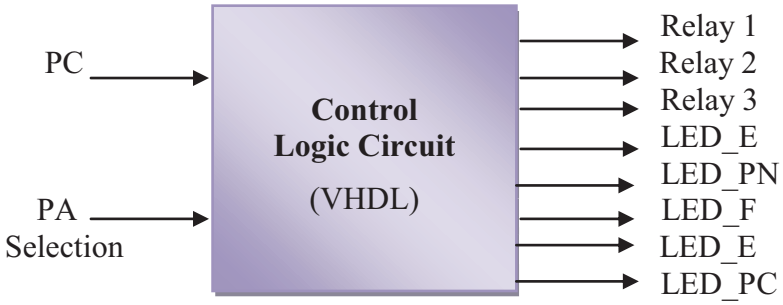


Figure (5.7) the Inputs/Outputs implemented with CPLD (EPM7128SL84-15)

5.1.1.4 Design of the control logic circuit with VHDL (B)

In the reader unit, there were many logic circuits to control the performance of the reader function with the implant device. The logic circuits were implemented with a CPLD chip by programming it in VHDL code; this was to reduce the hardware design, in addition to providing a fast implementation for the control circuit performance. The inputs were interfaced to a CPLD chip from the decision circuit to provide the essential transition logic for the control circuit. This provided selectable logic according to the distance and the orientation of the transmit coil, which changes the essential supply voltages for the power amplifiers. The block diagram of the complete control circuits is shown in Figure (5.8). The block diagram of the decision unit interface to the inputs and outputs CPLD chip is demonstrated in Figure (5.9) where the implementation of the truth Table (5.2) for the decision unit.

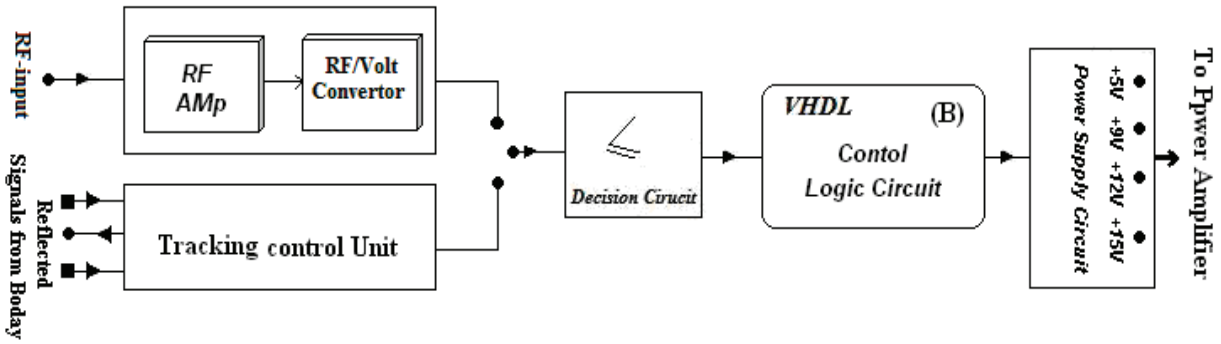


Figure (5.8) the complete control units for voltage source to power amplifiers

The RF received signal was amplified and converted in to DC voltage, according to the intensity of the RF signal and the distance between the two coils. This output DC voltage was controlled by decision circuit. The VHDL code generated the control logic circuit as shown in Figure (5.10); the outputs were interfaced to voltage power supply circuit. That provided the appropriate output DC voltage according to the distance between coils and the orientations as (D0 ~ +5V), (D1 ~+9V), (D2 ~ +12V), and (D3 ~ +15V). The error detection circuit monitoring the input logic states and outputs from the decision circuit used four inputs excusive OR gate built in VHDL chip (EMP 7128-84) as shown in Figure (5.10).

$$out_1 = \bar{x}_0 \cdot x_3$$

$$out_2 = x_1 \cdot \bar{x}_2 + \bar{x}_1 \cdot x_2$$

$$out_3 = x_1 \cdot \bar{x}_2 + \bar{x}_1 \cdot x_2$$

$$out_4 = \bar{x}_3 \cdot x_0$$

Logic outputs of the decision circuit

Figure (5.9) the Inputs/Outputs implemented with CPLD

Output Logic				Distance			
X0	***X1***	***X2***	***X3***	***D0***	***D1***	***D2***	***D3***
1	0	0	0	+5	0	0	0
0	**1**	0	0	0	+9	0	0
0	1	**1**	0	0	0	+1 2	0
0	1	1	**1**	0	0	0	+15

Table (5.2) Truth table of the decision proposed Control circuit

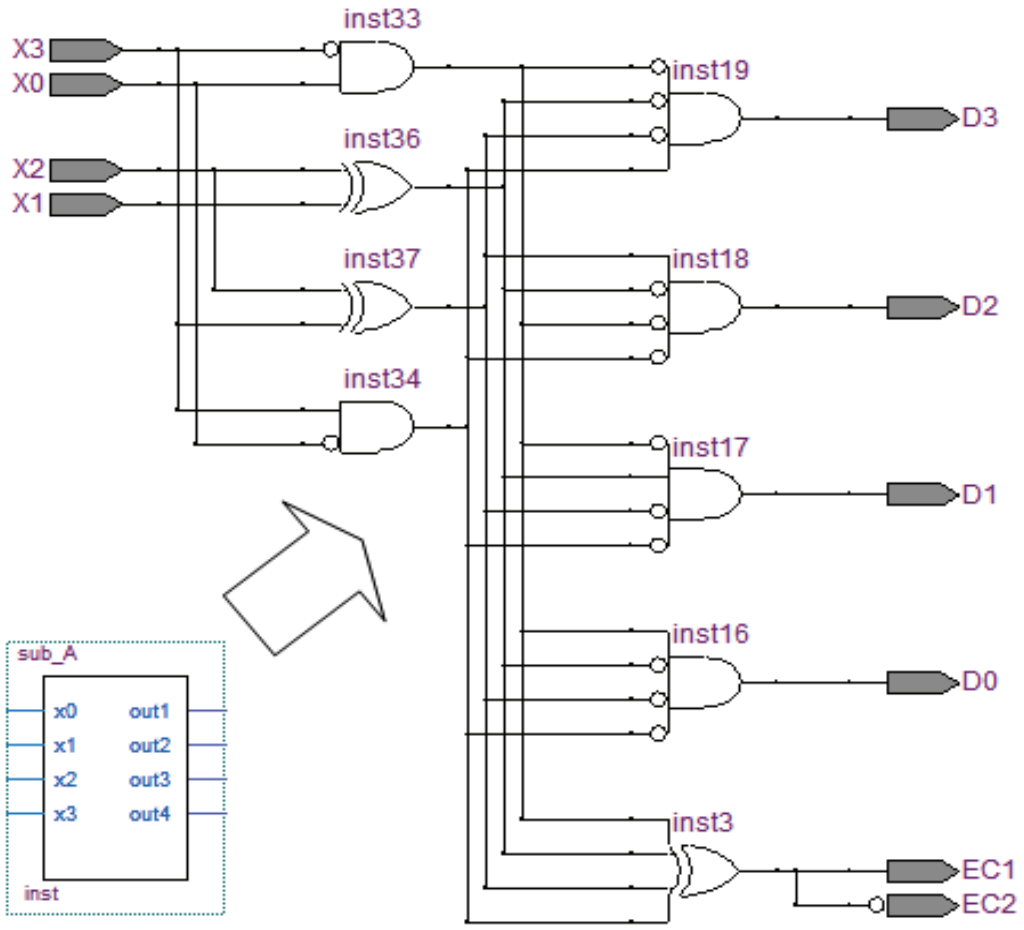


Figure (5.10) the code Inputs/Output with VHDL for the logic control circuit

5.1.1.5 PN-Code Sequence Generator Background

We used the PN-sequence as the data source in the reader part to simulate the command information, and to check the bit errors easily. The serial data stream was divided by a selected polynomial and the division remainder was transmitted at the end of the data stream as a Cyclic Redundancy Check Character (CRCC) [166]. Figure (5.11) demonstrates the example of the PN-sequence for 16 polynomial codes. The polynomial can be generated by changing the binary select codes; this is given as example in Table. (5.3) below; at the receiver the same calculation should be performed to reproduce the sent data. If there were no errors in transmission, the new remainder will be zero. There are many common polynomial error detection techniques, as a read forward and reverse on the CRCC-16 and CRCC-CCITT functions.

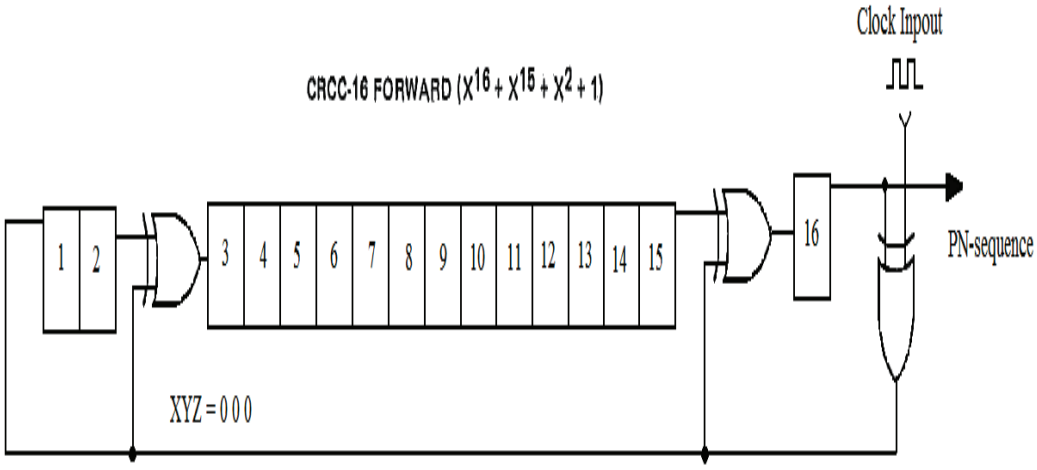


Figure (5.11) the technique for generates PN-sequence data [166]

Code selected			Polynomial generation	
X	Y	Z		
0	0	0	Fwd CRCC -16	$X^{16}+X^{15}+X^{2}+1$
0	0	1	Bawd CRCC -16	$X^{16}+X^{14}+X+1$
1	1	0	Fwd CRCC-CCITT	$X^{16}+X^{12}+X^{5}+1$
1	1	1	Bawd CRCC-CCITT	$X^{16}+X^{11}+X^{4}+1$
0	1	0	LECC-16	$X^{16}+1$
1	**0**	**1**	LRCC-8	$X^{8}+1$

Table (5.3) different PN-sequence techniques for error calculation

5.1.1.6 PN code generation with VHDL code

The PN-sequence algorithm was synthesized in VHDL code; there are many techniques to implement the code sequence. That is used as data source either in the reader part or implant to simulate the command information or as data source, and to check the bit errors easily. The synthesis of VHDL code for PN generators is demonstrated in Figure (5.12) and Figure (5.13) respectively, which uses two different codes to generate the PN sequence. Obviously, the first code uses the present state to reduce the logic gates to generate the PN-code. When compared to the second code, it reduces the consumption of power for the whole design inside CPLD. However, the VHDL code for PN sequence discussed in appendix B, along with the hardware circuit fabricated to generate the PN sequences data, and additional information is discussed in appendix C.

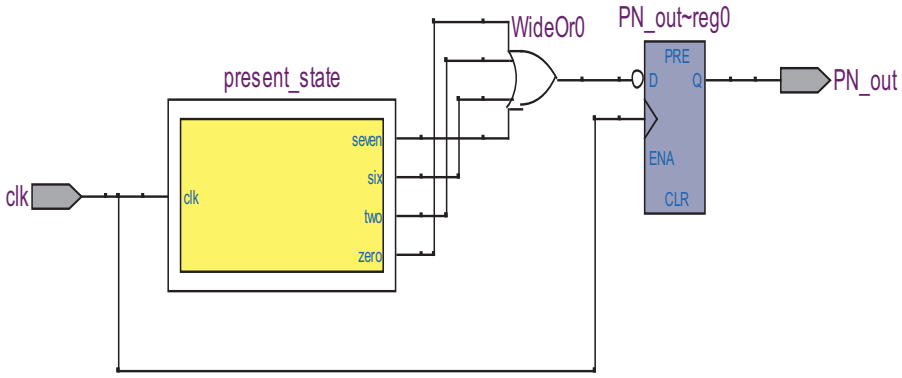


Figure (5.12) the PN sequence generated by VHDL code (**A)**

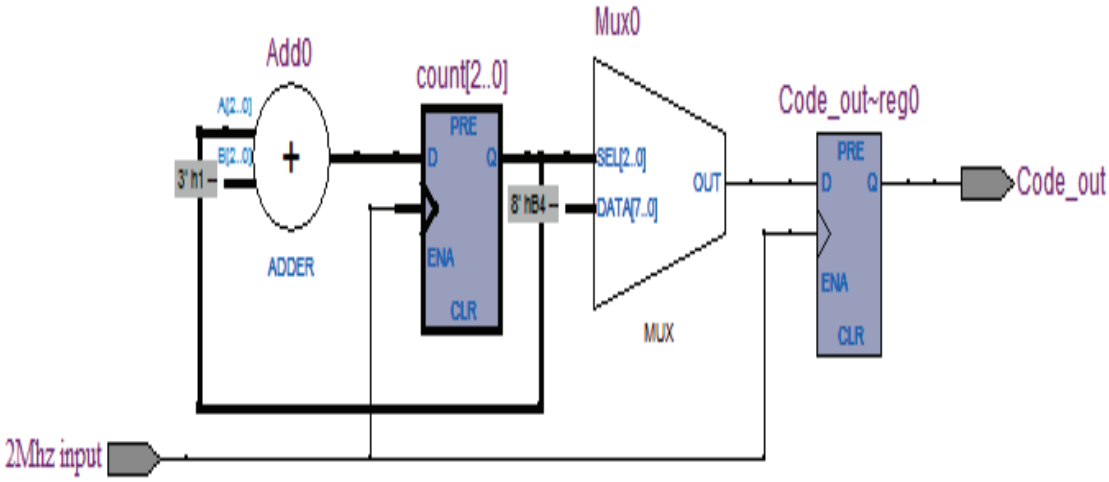


Figure (5.13) the PN sequence generated by VHDL code (**B)**

5.1.2 Prototype Implant Device (PID)

The second part in this chapter is the Up-link part, which is the important element in our work, where we evaluate our design for a high data modulator for biomedical applications. The implant device received the wireless RF power signal, which was delivered from the reader in magnetic modulated form. As described in the reader unit earlier, the Amplitude Shift Keying (**ASK**) was selected to transmit the information commands from the reader. It was recovered by the ASK demodulator in the implant device. However, the demodulator techniques in biodevices are still under investigation and challenges exist for many researchers to minimize the power and size, for improving the performance of the implant device.

Our prototype PID consists of the RF rectifying signal to the DC voltage using signal Shtoky diodes, followed by switch regulator (SWR). This is attached to the ASK demodulator to encode the modulated signal from reader. The output voltage provided by SW was at about (3.28V) 5cm, apart, the maximum delivered current from switch regulator is about (15mA) as tested. The PID block diagram is demonstrated in Figure (5.14). The proposed modulator was synthesized with Altera chips (EPM 3032, EPM3064) and configured for our codes to generate the (BPSK) (QPSK) and (8PSK). However, the accessories part of the implant was substituted by code as simulated data. However, the practical design work was done to design a digital demodulator instead of analogue demodulator, which is described in appendix-C, and which was also discussed in chapters two and four. The prototype for the implant device was designed and evaluated in Lab measurements for the proposed modulators (BPSK, QPSK) and (8PSK). We have described the general layout of the implant prototype device in Figure (5.14), which uses the inductive coupling link, for both directions of the communications. The maximum received power that was measured at the implant was about (95mW) at fixed voltage (3.28V) over communication distance about 4.5 cm.

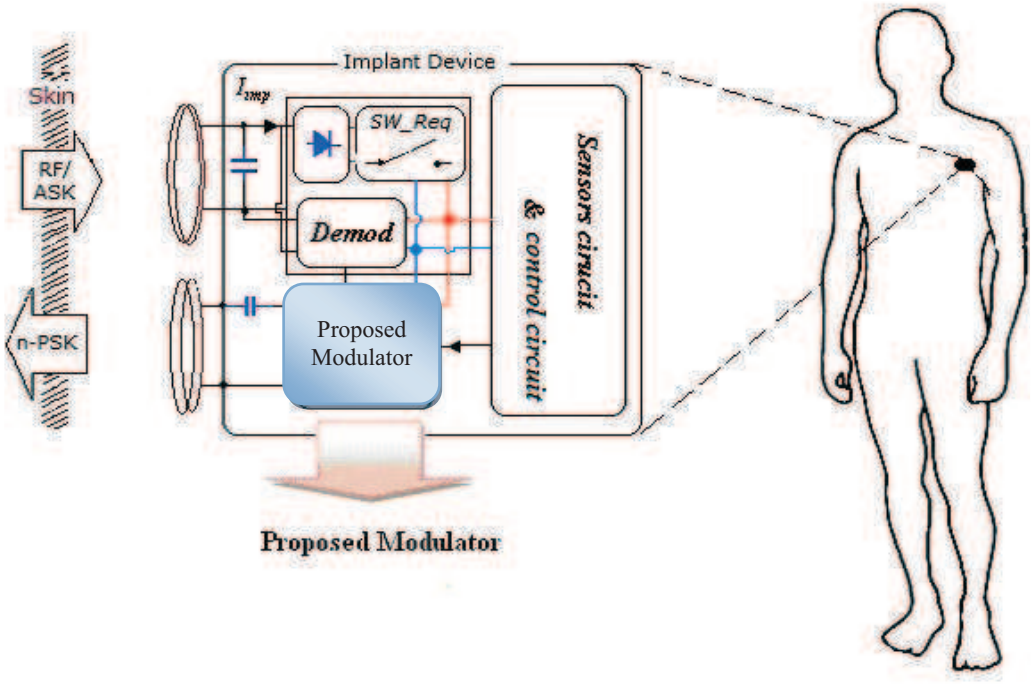


Figure (5.14) the target proposed modulator at implant device

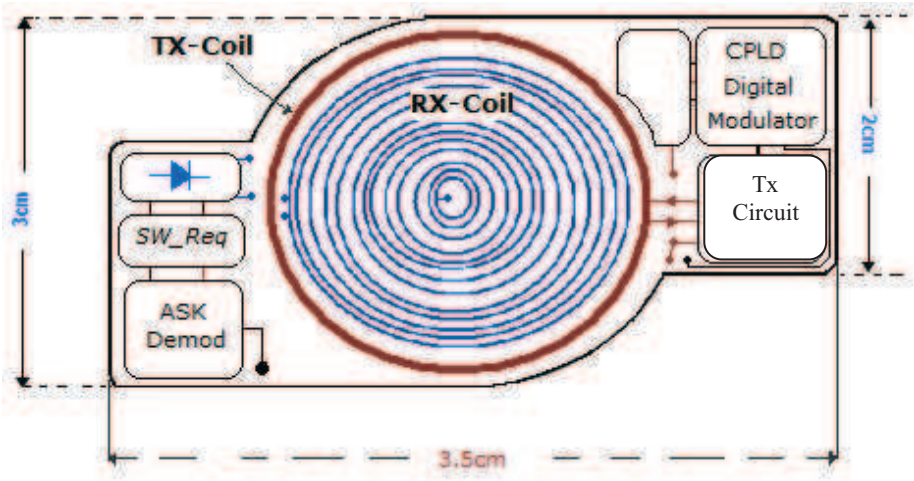


Figure (5.15) the general layout diagram for the implant device

Modulation Types	*Data Rate*	*Oepration Volatge*	*Communication distance*	*Consumption of Power*
BPSK	Up to 2.5Mbps	2.8~3.3V	~10 cm	~3.4mW
QPSK	Up to 3.5Mbps	2.8~3.3V	~9 cm	~4.4mW
8-PSK	Up to 3.5Mbps	2.8~3.3V	Up to 5cm	~5.4mW

Table (5.1) the measurement results for our proposed modulators

5.1.2.1 ASK Demodulator receiver (RX)

The ASK modulation was described as an alternative simple scheme from demodulation, which is simple to implement in the implant device. Principally, the ASK demodulated received signal delivered from the class E power amplifier is demodulated by an envelope detector after a tuned circuit at RF resonant frequency. Then it passes through a low pass filter (LPF); due to a high input signal at short range, it may not be necessary to amplify the demodulated received signal. Thus, a simple Schmitt-Trigger was able to provide and shape the output of the demodulator which was then buffered. In our practical circuit, we used the MOSFET as a low pass filter followed by Schmitt trigger and inverter. The block diagram of the common ASK demodulator is shown in Figure (5.15) and the circuit diagram of the ASK demodulator is demonstrated in Figure (5.16) [104] [113]. The Lab measurements for the RF ASK modulated signal and the received signal, which are inductively coupled, is illustrated in Figure (5.17) at 10% of modulation index. However, the information data signal was interfaced from a variable PN sequence generator circuit, and then modified with PN-VHDL code.

The measurement results for the transmitted PN-sequence and the received data were tested over different values up to (50Kbps) over the magnetic coupling at carrier frequency signal 135 KHz, which is demonstrated in Figure (5.18), showing the TX-PN-sequence and demodulated PN signal at the implant part. Finally, the ASK demodulator circuit consumed about (1.2 mW) at voltage (3.28 V) from the total wireless received power, and this consumption affected the implant efficiency, as the demodulator design still needs to be improved for low consumption power.

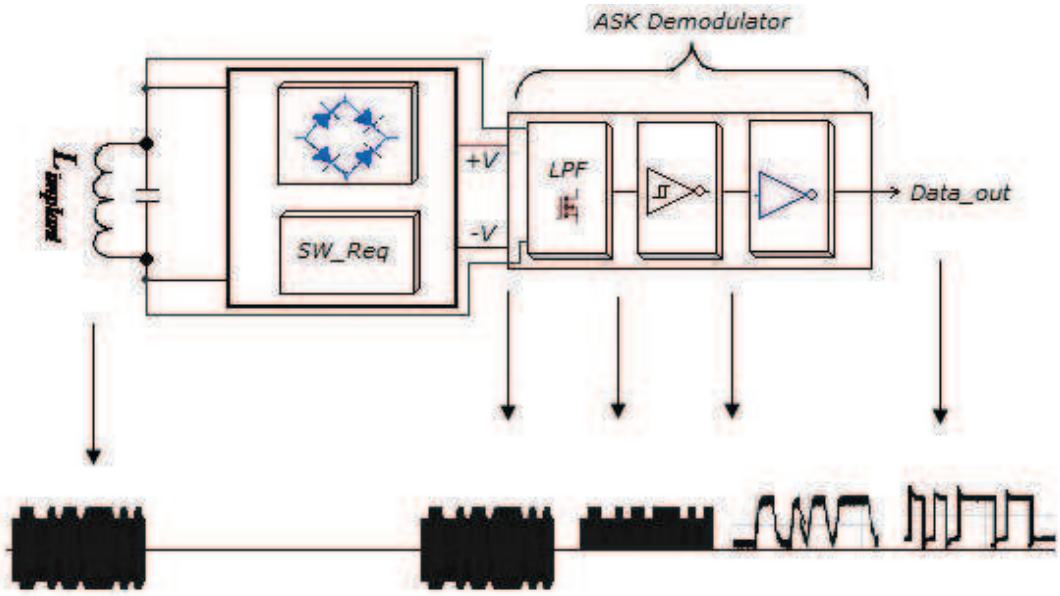


Fig (5.16) the ASK Demodulator used at the implant device

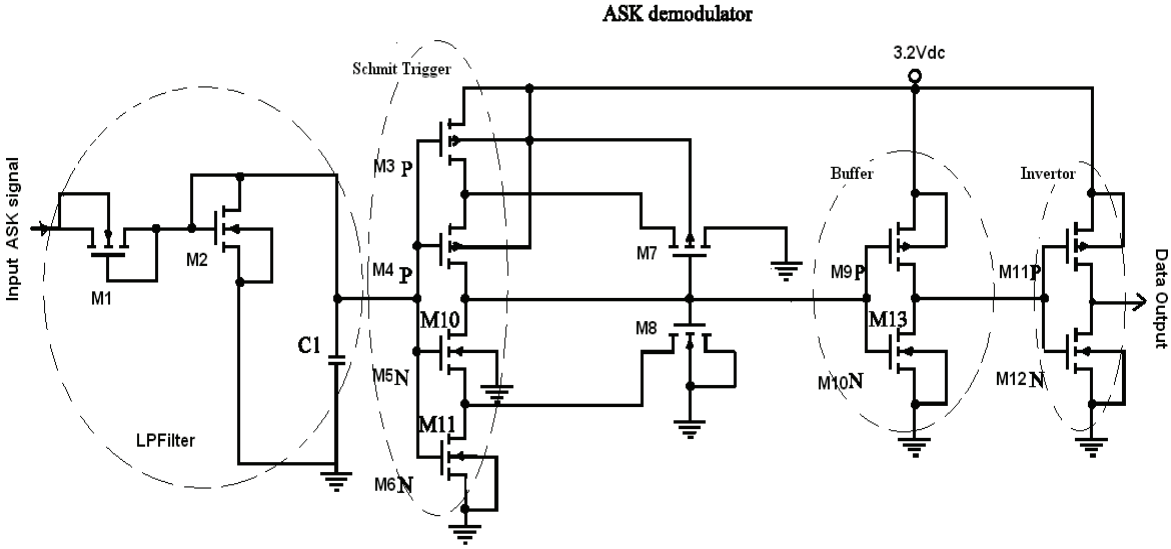


Figure (5.17) the ASK Demodulator circuit using MOSFET

(a)

(b)

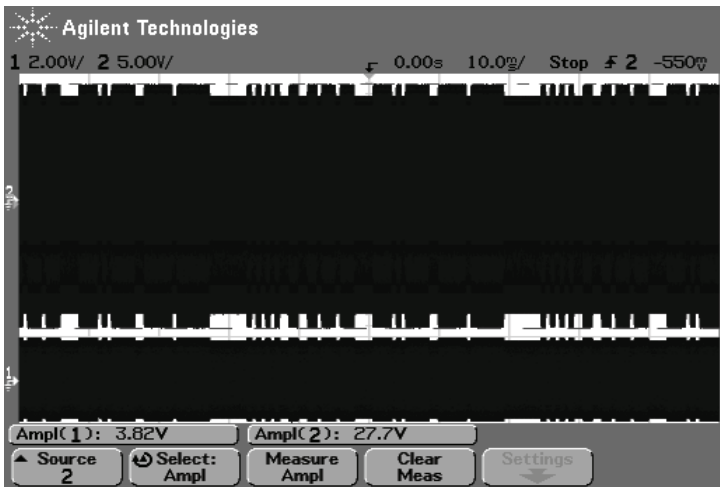


Figure (5.18) Waveforms of ASK RF Tx signal (a), (b) Rx- received signal at implant device at distance (5cm)

(a)

(b)

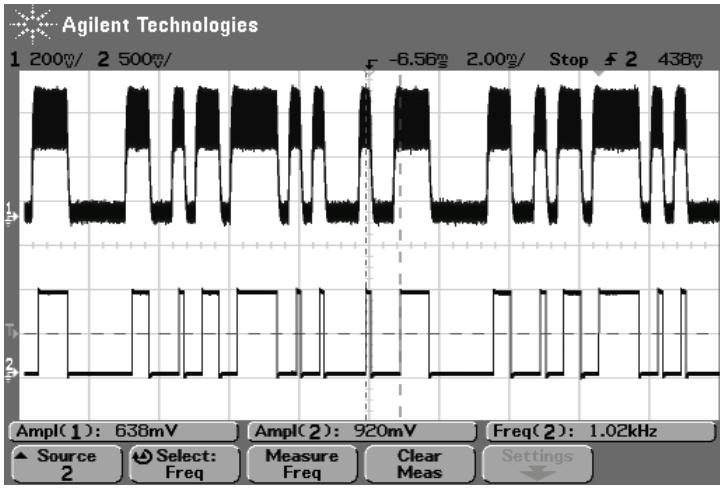


Figure (5.19) (a) LPF output demodulated signal (b) PN output data

5.1.3 Control System Unit (Reader)

The control system was synthesized and evaluated with Lab measurements for the ASK Modulator/Demodulator, and these signals are shown in Figure (5.18). The results for ASK transmitted and received data was measured at 12kbps (tested up to 50kbps) over carrier frequency 135 KHz. The rest of the reader is demonstrated in the block diagrams in Figure (5.1), which consists of several parts: (1). Frequency control system (2). Position detection system (3) RF sensor (4). the hybrid power amplifier system. Generally, the hardware reader circuits are shown in Figure (5.20).

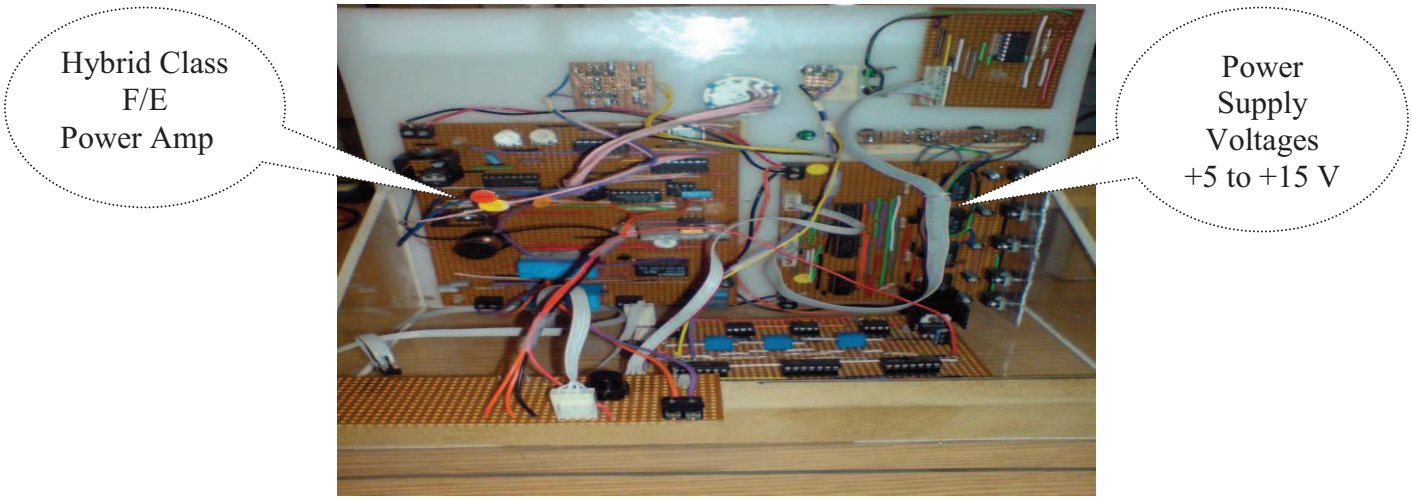


Figure (5.20) the hardware of the part of Reader for the proposed control unit

5.1.3.1 Frequency Control System (A)

In practice, there are various methods that can be implemented to monitor the RF transmit signal. The feedback control technique is the common way for monitoring or controlling in power amplifiers and may be useful in wireless communication applications. The simple control has been designed using the PLL technique to auto-correct the RF transmit signal that offers output power stability for the power amplifier. In addition, the feedback control techniques can provide a stable constant voltage at the implant device. This method is a simple design to reduce the reader hardware circuitry and complexity. The feedback system consists of an amplifier to gain the RF signal, then passes through a square circuit (multiplier), and is then filtered at the centre frequency $2f_o$ and passes through the converter to the digital form. The phase comparator was used to compare the converted digital TX signal, with respect to fundamental transmit pulse signal f_o, and detect the phase shift for driving the VCO. We chose the PLL (HEF4046) to synthesise the fundamental frequency of the oscillation square signal at carrier frequency 135 kHz [220]. The proposed control system using PLL technique is shown in Figure (5.20) where in Class ***E*** case it was used to transmit the ASK signal, whilst in class ***F*** it was used as RF power signal generated as described in (5.4):

$$RF_{Tx\_Coil} = Gain\begin{cases}\cos(\omega_c t) & Class\ F \\ S_{ASK} & Class\ E\end{cases} \tag{5.4}$$

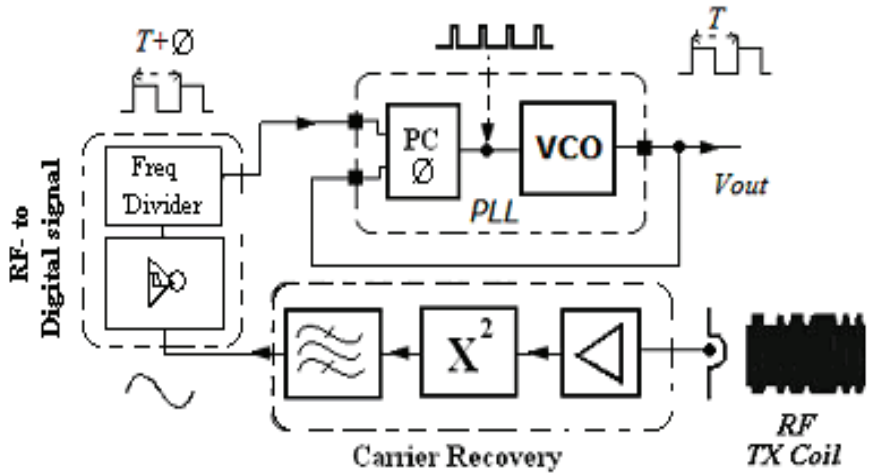


Figure (5.21) the first control method using PLL (HEF4046)

Therefore, to analyze the feedback interface signal to PLL, where(K_d) defines the phase comparator and VCO (K_o) signals, the $e(t)$ is the output error pulse phase different, as demonstrated in Figure (5.21) the mathematical analysis can be expressed in equations (5.5), (5.6), (5.7) respectively, where $G(s) = K_d.K_o$

$$e(t) = r(t) \times y(t) \tag{5.5}$$

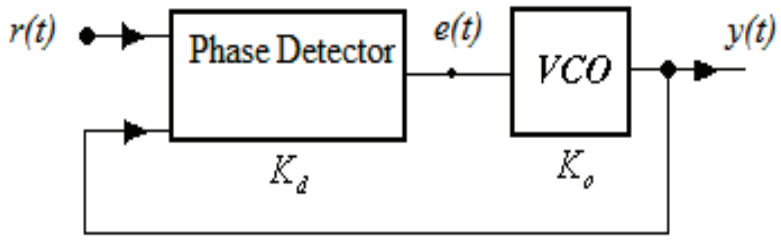


Figure (5.22) the feedback control method using PLL

The transfer function of the PLL system can be expressed as:

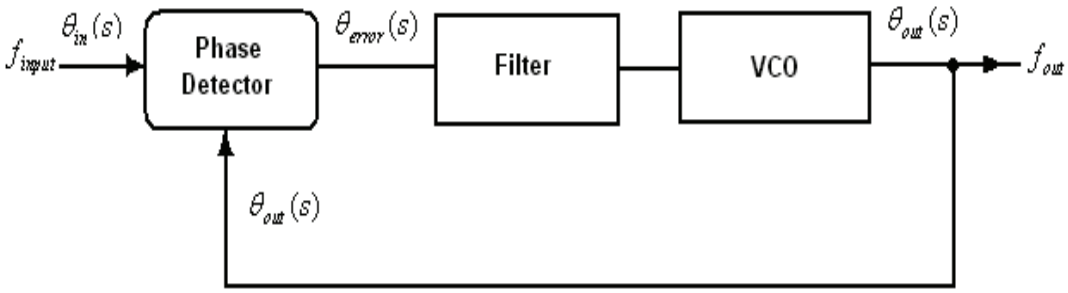


Figure (5.23) the PLL feedback system

$$\theta_e(s) = \theta_{in} \times \theta_{out}(s) \tag{5.6}$$

$$\theta_e(s) = \frac{1}{1 + G(s)} \tag{5.7}$$

The detailed circuitry of the PLL –VCO (HEF4046)-[220] is given in Figure (5.23) as:

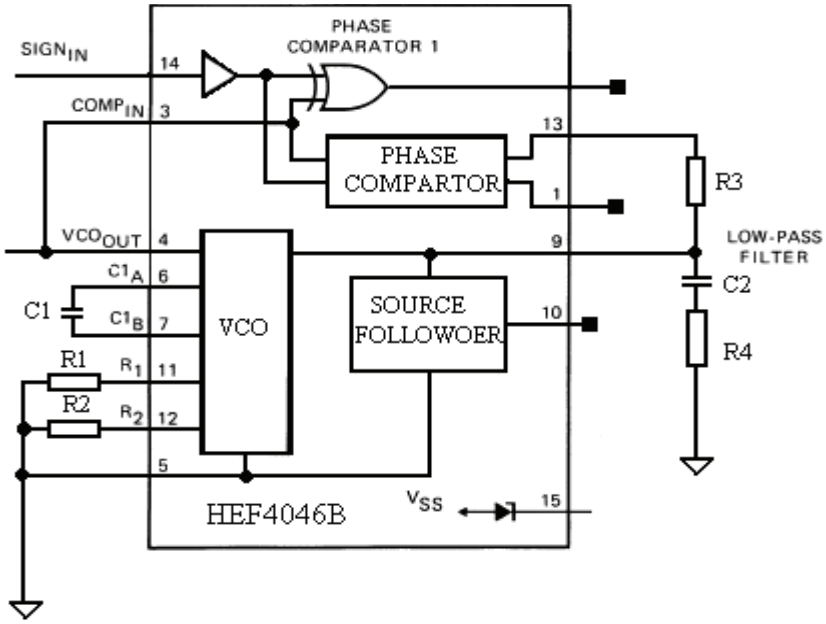


Figure (5.24) Detailed PLL HEF4046B control system

However, the Lab measurements for the PLL are illustrated in Figures (5. 24), (5.25) and (5.26) respectively.

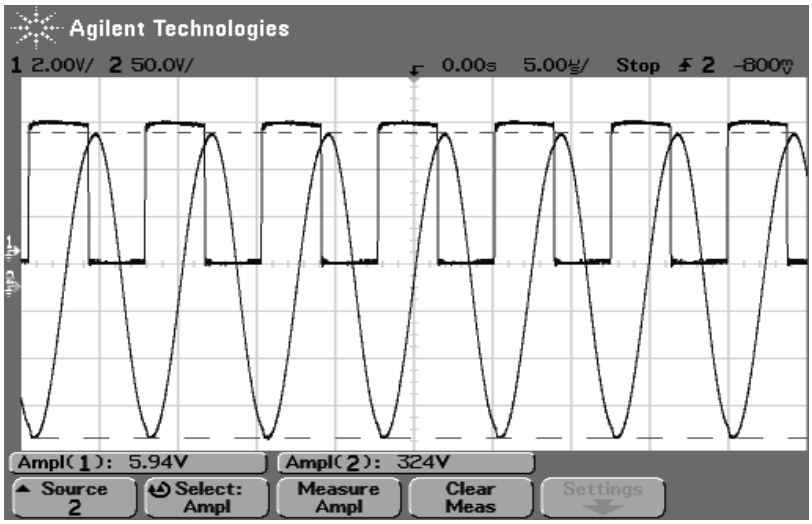


Figure (5.25) RF carrier signal (sine wave) and converted carrier digital signal

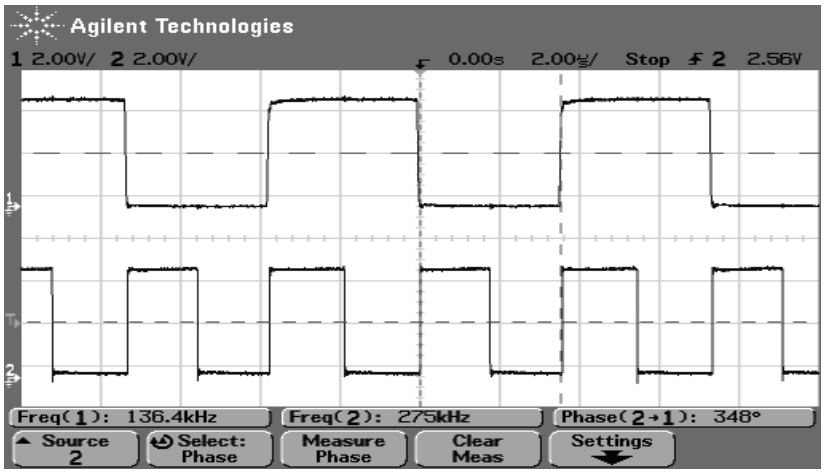


Figure (5.26) comparing the converted digital pulse and the reference pulse

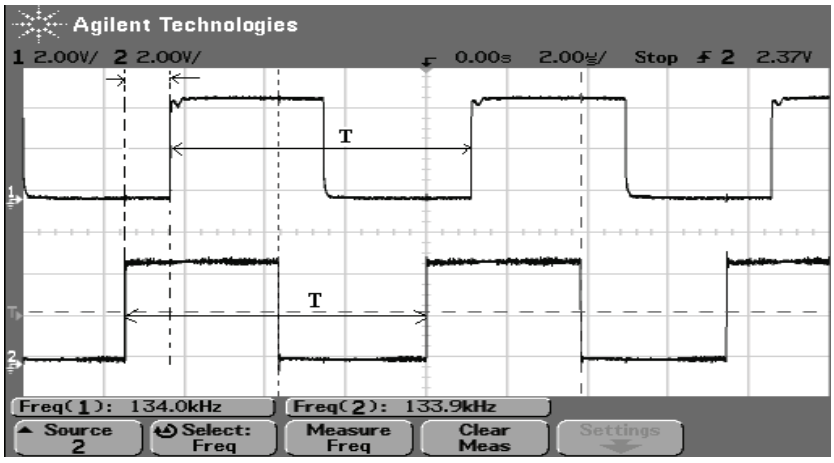
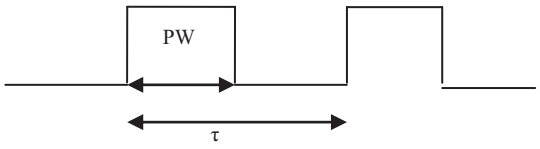


Figure (5.27) Phase error between original and converted digital signal

5.1.3.2 Frequency Control System (B)

The second practical solution method was synthesized to generate the PWM signal using an FPGA technique. The PWM technique can be used to provide a logic (1) and logic (0). In this work, the PWM was used as carrier pulse signal. Several methods were investigated for generating the PWM signal, but synthesis by two methods was programmed in FPGAs. The main critical design part was the feedback signal to synchronize the output PWM signal; the PWM error was detected by the phase comparator between both signals. Generally, the first proposed design is illustrated in Figure (5.28). Generally, the design was modified to correct the output PWM signal to perform the duty cycle at 50% at the tuned frequency 135 KHz, and according to the equation (5.8). The feedback technique in this design was modified to auto-correct the frequency and fix the duty cycle of the output PWM signal, where the feed back

provided the synchronization between the RF power amplifier and the pulse generated at centre frequency. However, to generate PWM signals by VHDL code it was essential to control the data value, which is loaded to the up/down counter, where the input data was fixed in this work at the binary (10000000) to provide pulse width at 50%. In addition, the clock signal was internally generated and compared to the received pulse signal from RF digital convertor. The PWM needed to double the frequency of the carrier pulse to produce 135 kHz. The PWM signal was generated by VHDL code and synthesized in CPLD (EPM7128SLC84-7), that drives the Class ***E*** power amplifier where it was used to transmit ASK signals, the result for PWM code generator is shown in Figure (5.29), and the PN-sequence was interfaced from external PN sequence, circuit to CPLD in the Altera development board. The ASK modulator signal was evaluated and tested with the VHDL pulse signal at the carrier frequency 135 kHz. The transmitted TX ASK signal is illustrated in Figure (5.30) at a data rate of about (5.9kbps). In the completed work, the PN-sequence was synthesized with VHDL code.



$$where \quad m = \frac{\tau}{255 \times Ts} \qquad (5.8)$$

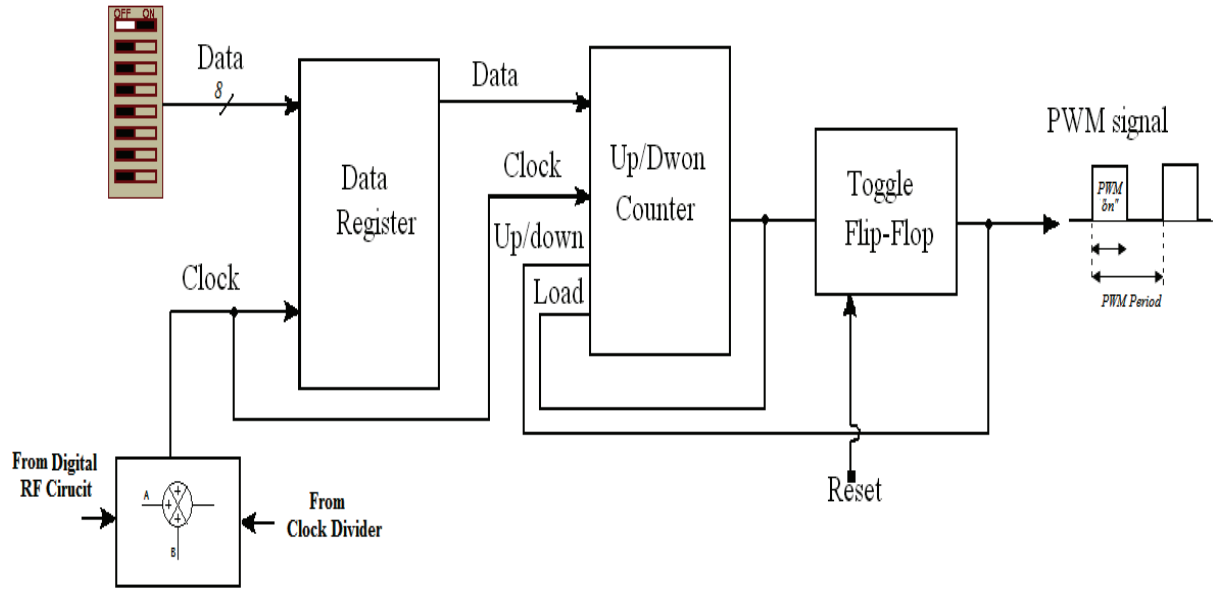


Figure (5.28) the second control method using PWM code by VHDL

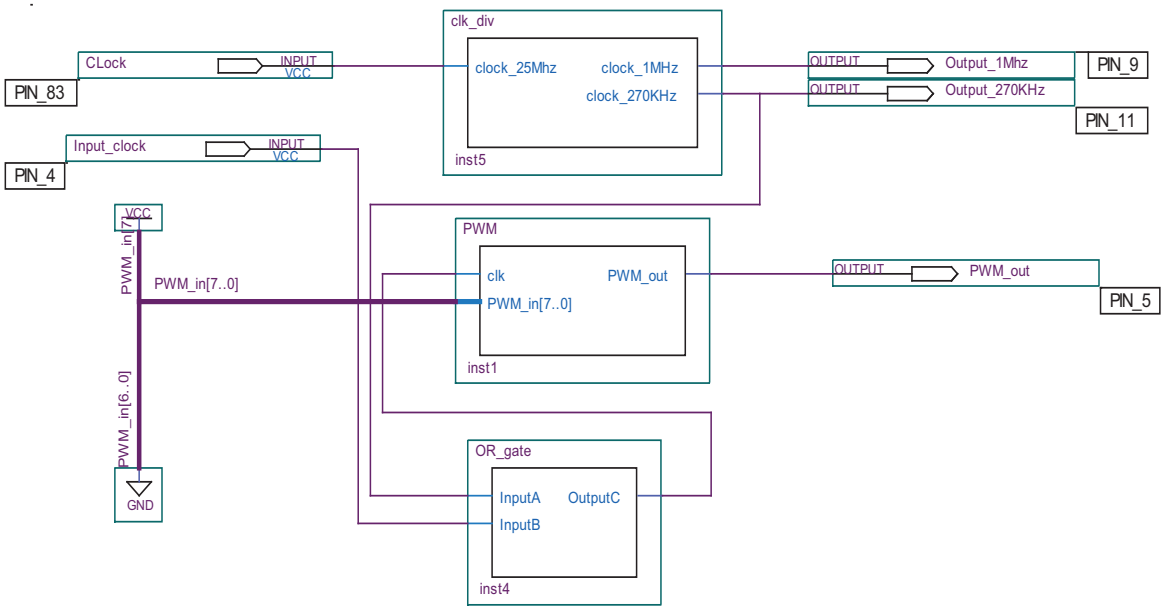


Figure (5.29) the simulation result generating VHDL code for PWM signal

(a)

(b)

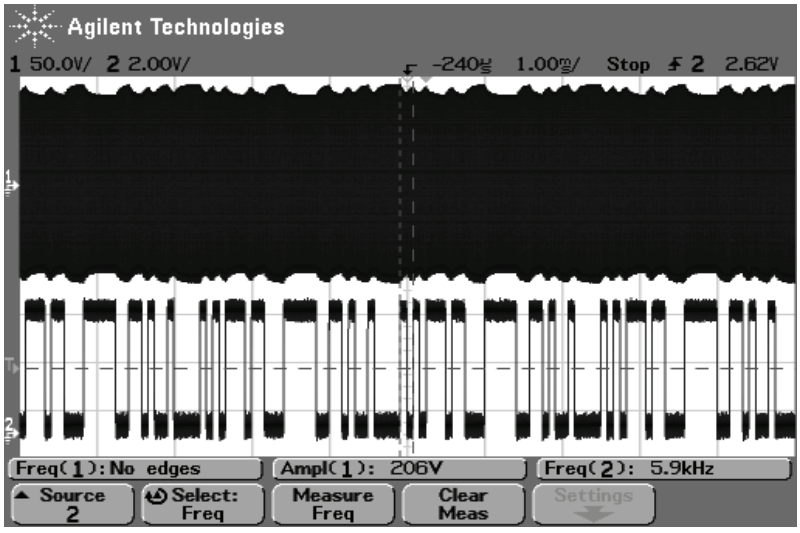


Figure (5.30) (a) the TX-RF ASK transmitted by Class E-PA
and (b) controlled PN-signal

5.1.4 Measurements for TX&RX for n-PSK Signal Over The Inductive Coupling

The proposed modulator was conducted with an Altera CPLD chip, to evaluate our digital modulator design. The first modulator code was implanted to generate a BPSK, which was driven by PN-sequence signal as information source at (2Mbps). The measurement results are illustrated in Figure (5.31), where the same information data was interfaced to the QPSK modulator; the transmitted and the received signals are demonstrated in Figure (5.232).

Figure (5.31) TX and RX for BPSK signal generated by VHDL code: (a) PN-sequence Code, (b) Tx- BPSK signal,(c) RX-BPSK signal

Figure (5.32) the TX and RX for QPSK signal generated by VHDL Code (a) RX-QPSK signal, (b) TX QPSK signal

5.2 Summary of The Biodevices System

In this chapter, we conclude the hardware overview of our prototype system, and Lab evaluated measurements for the complete system. It explains and displays the new technical approach solution for biomedical applications and tries to compare different digital modulators as synthesized in this thesis. However, different methodologies have been investigated and re-synthesized for improving the system and reducing the hardware complexity.

We improved the power amplifier and reduced the power consumption and maximized the transmit power, to increase the power efficiency. In addition, the first class power amplifier ***E*** has been specified for transmitting the RF-ASK modulator measured TX power at (46.63 dBm) Rx-power (14dBm) power efficiency (30%) and carrier frequency 134 KHz at data rate ~ 50Kbps. The second power amplifier **F** has been specified for RF power carrier measured TX power at (42 dBm) Rx-power (26.41dBm) power efficiency (66.025%) and carrier frequency 135 KHz. In practice, the consumption of power measurements for the ASK demodulator circuit is about 30% of the total wireless received power, and this high consumption of power affects the performance efficiency of the implant device and reduce the communication distance. It is still necessary to improve the ASK modulator design as a part of future work for compatible smart design.

The feedback signal techniques have been investigated to synchronize the generated output pulse signal and the transmitted RF signal, which has an auto-correction frequency using PWM technique. This offers high frequency stability at the implant device and constant level DC voltage from the received wireless power, where the carrier signal maintains a constant. Practically, the class **F**-PA has delivered higher power than class **E**-PA; our measurements results in chapter 3 have illustrated the comparison between both amplifiers. The second test measurements were evaluated for transmission data over inductive link, and the results have been presented for the carrier frequency of 12.50 MHz, whilst the measured data rates were tested at 1.5, 2 Mbps for the BPSK modulator and up to 3 Mbps for the QPSK modulator. However, the main advantages of this design are to create a high data rate, which reduces communication time between the reader and the implant, and improves the diagnostic time in real time communication at high speed. The PWM is widely used in new modern control techniques by using microcontrollers.

In new applications, it may be programmed by VHDL code using Field Programmable Gate Arrays (FPGA), which generate a PWM signal. Consequently, the whole project has been synthesized in VHDL to reduce the hardware circuit complexity and consume less power; in addition, it can be reconfigured. The results are summariesed in Table (5.2) and show the comparison between two methods for monitoring the RF frequency or monitoring frequency control (MFC) with Class ***E*** power amplifier. The measurement was performed without modulated data for accurate measurement; in this case, we choose the distance at 3cm. The second measurements have been performed for the Class ***F*** power amplifier, which compared the methods for MFC as shown in Ttable (5.3). Generally, the PLL-VCO can be converted to purely digital design for use in Field Programmable Gate Arrays that design most of the project in the same chip. Obviously, from the Tables the second method using PWM technique offers better performance stability for transmitting RF power than using the VCO-PLL.

Frequency Control System	*Carrier Frequency Stability (f_o)*	*Power Efficiency %*	*Transmitted Power At TX coil*	*Rx-Power in dBm At 3cm*
VCO-PLL	132.5 KHz ±1.4%	0.170 %	365Vpp	17.7 dBm
VHDL (A)	131.1KHz ±1.3%	0.504 %	397Vpp	14.4 dBm

Table (5.3) the comparison measurement results for our different frequency controller for Class ***F***

Frequency Control System	*Carrier Frequency Stability (f_o)*	*Power Efficiency %*	*Transmitted Power At TX coil*	*Rx-Power in dBm At 3cm*
VCO-PLL	133.5 KHz ±1.4%	0.550 %	397Vpp	29.5 dBm
VHDL (A)	134.5 KHz ±1.0%	0.904 %	397Vpp	30.7 dBm

Table (5.2) the comparison measurement results for our different frequency controller for Class ***E***

Chapter

6

Conclusion of Thesis Results and Future Work

Chapter 6

Thesis Conclusion

This thesis has presented an investigation of wireless inductive coupling for transmitting a high data rate telemetry signal in biodevice applications. The proposed system has been built in hardware and combined with software, which used VHDL (IEEE standard), as a hardware structure description language which can offer digital synthesis and the flexibility to re-configure and upgrade the system. The proposed new VHDL digital modulator for electronic medical devices applications may be used for many biomedical devices such as wireless pacemaker and wireless brain implant device. Presented in this work are most of the biomedical applications, the modulation techniques and transmission coding methods over wireless inductive coupling links. Attempts are made to simplify the mathematical analysis and hardware circuits. Previously, each chapter has been concluded individually, however the whole thesis is summarised in this chapter. The conclusion of the thesis can be classified in to two sections as:

6.1 Down-Up-Link system

In this thesis, different types of modulation schemes are considered for down link communication from the reader system toward the implant device. Many factors are found to affect the design, such as coil misalignment, simplicity of design, coil specifications and limitations on frequency and power. Most of the published works in this area used the ASK modulation method which is simple to implement for a modulator or demodulator, typically over an inductive coupling link. However, the technologies for inductive coupling and the data acquisition from the body are still under investigation by many researchers, dedicated to the problem of increasing the data rate over the inductive coupling link from the implant device. Consequentially, work is needed to improve the communication distance between the readers and implant coils and reduce the implant size. The second chapter has covered most of the studied cases and the published work on the biomedical applications area. It described most of the growth disorders and ailments of the human body such as; epilepsy, paralysis, Parkinson diseases, and nervous system disorders.

Predominantly, these are results of malfunction of the human body or may be due to physical failure or damage to the organ functions; such as in the heart, kidney and brain. However, most of these give rise to signals, which can be recorded, monitored or captured from the human body for diagnostic and monitoring purposes. The third chapter has covered the inductive coupling link, which is the main target of this work, for transmitting the RF power from the reader unit and the command or telemetry data in both directions. The wireless topology offers advantages over other techniques including a reduced infection risk, providing a safe solution for the patient, and improved mobility. A substantial number and wide range of papers published in this area have reported studies and investigations of the magnetic inductive coupling. In practice, the most critically important element in this design is how to choose the inductance value of coils for the optimum coupling with appropriate coil size design for medical purposes. The best inductance for the reader coil, was simulated and measured to determine the optimum coupling between coils between the values (425~650μH). The lab measurements provided comparisons with a differently designed inductor coil which was a loop antenna instead of spiral design for the RF power coil at inductance value ~ 450μH. The disadvantages of spiral coils are the spreading and distribution of the magnetic flux and reduction of the communication distance. On the other hand, the flat spiral coil was appropriate for the implant part, which harvests the magnetic field more efficiently than other coils such as loop or circular coils. The maximum transmitter power was measured at 3 Watts at reader amplifier output and the wireless received power was 0.15 Watts at the implant device.

UHF technology was investigated since it could be useful for high transmission rates, though many factors such as interference, circuit size, safety regulation limits (SAR), and oscillator design are disadvantages for biodevices applications when working at such high frequencies. This is discussed in chapter three in detail. The biodevice system which has been designed and developed here can be used for various implant applications. In the second chapter the basic principles of analogue and digital modulation categories that are commonly used for wireless applications are described. The target scheme here is Quadrature digital modulation for generating n-PSK. Typically, the digital schemes used for biomedical devices are more reliable than the analogue modulation.

A practical solution approach was introduced for the biodevice applications, which used new simple synthesised direct digital modulators (n-PSK) to increase the data rate.

The digital modulators (BPSK, QPSK and 8PSK models) have been designed and simulated in the MATLAB/Simulink environment, and have been successfully synthesised with VHDL programming code. The experimental measurements were presented at carrier frequency 12.50 MHz and the data rate has been evaluated up to ~ 3 Mbps. In practice, this presented a better performance with high data rate over wireless inductive coupling. The output of the multiplexer produced a BPSK or QPSK digital (square) signal waveform, however the digital signal cannot be transmitted directly without filtering for harmonics separation. A passive filter was used for removing the harmonics from the digital modulated signal. This was designed and simulated to determine the optimum passive filter design in the implant device. The simulation results show better BPF performance for selection of the Chebyshev I & II types, compared to the others tested. On the other hand the Butterworth LPF type gives optimum performance. Digital filters were considered, however, the disadvantage of using the digital filter is that it is needs higher sampling frequencies, which increased the consumption of power and the size. Furthermore, these are not considered in this work as the consumption of power is excessive in comparison to a passive filter which has zero power requirement.

The prototype of the biodevice system has been developed and measurements are shown in chapter five. Summaries in this chapter of the evaluations of lab measurements for the system have explained the results in detail and displayed the technical performance of the new modulator for biomedical applications. This technique can offer a high transfer data rate from the implant device, which requires a higher rate for the up-link digitized electrode signals where there is a need to measure in real time. The clinical demand for acquisition data that is returned from the body is increasing and requires an efficient modulator to achieve high transfer rate and low power consumption to read the signals from the electrodes.

In addition, significant improvement has been made in this work with the design of the RF power transmitter by synthesizing a hybrid power amplifier for improving the power efficiency of the wireless coupling link. This generates a constant transmitted RF magnetic field, by using a feedback topology for auto-control of the coupling system.

In addition, it offers a constant DC voltage at the implant device. Three different methods have been investigated for the stability control of the transmitter RF power using PWM techniques. Finally, the control feedback system was synthesized by programming VHDL code, which is very appropriate for this work, reducing the hardware and providing robust design. The results demonstrate that using the FPGA provides an advantage over other methods.

6.2 Suggestions for Future Work

At the end of the PhD activity, here is a brief wrap-up of many goals accomplished. The main contribution of this work is to advance the state of the art in biodevice telemetry applications with a new digital approach. Where the power and hardware are important in biodevice circuits design, several different enhanced topologies have been synthesized for medical purposes. However, the advantage of the work is that it may be a basis for wireless communication modulation, used to convey high data rate signals. The need for such information transmission is increasing in hospitals. It is called “BIOSTEC” which includes Bio-signals, Bio-medical devices, and Bio-health. Design of an economical wireless telemetry system that is interfaced with the medical devices and network, via appropriate adapters such as PCs or mobile phones, could give to the patient the flexibility to use the devices in a portable unit. However, there are many researchers still investigating the human body and trying to understand and analyze prosthesis performance and disease effects, by using diagnostic or monitoring signals. For example, the EEG and EMG are involved in understanding the electrical brain activity with nervous system behavior, where the human body has a complex behavior to understand. Potentially, processing of these signals within implant circuitry using modern electronics could aid treatment for patients and help to improve their lives.

Finally, the future goal still exists to further investigate the optimization of the implant coil to improve the received power and increase the performance efficiency of the system. The objective of this work is the adoption of a new VCO structure, suitable as clock source for a direct digital modulator for a CPLD modulator in an ISM unlicensed frequency UHF band (nominally 402~ 405 MHz). Potentially this can be achieved by using the VCO in an up-converter to produce the transmitted RF signal. That addition would move the design towards a complete implant design with almost all functionality combined in a single digital integrated circuit.

List of Abbreviations and Symbols

A B C D E F G H I J K L M N O P Q R S T U V W X Y Z

A

A C	Alternating Current
ADC	Advanced Design System
ASK	Amplitude Shift Keying
ADS	Advanced Digital System
AM	Amplitude Modulation
AWGN	Adding White Gaussian to Signal
AMI	Alternate Mark Inversion
α	Attenuation

B

B	Magnetic flux density
BW	Band width
BER	Bite Error Rate
BPSK	Binary Phase Shift keying
BFPK	Binary Frequency Shift Keying
BPF	Band Pass Filter
BALUN	Balance /Unbalance
BJT	Bipolar Junction Transistor
BIOSTEC	Biomedical Signals Telecommunication

C

COMS	Complementary Metal oxide Semiconductor
CIC	Cascaded Integrator Comb
CW	Carrier Wave
CPU	Central Process Unit
CCD	Charge Coupling Device
CID	Complete Implant Device
CPLD	Ccomplex Programmable Logic Device
CRCC	Complementary Redundancy Circuit
CLC	Control Logic Circuit
CCITT	Committee Consulting International Telephony
CE-PA	Class E Power Amplifier
CF-PA	Class F Power Amplifier
CPS	Circuit Position System

D

DEPSK	Differential Encode Phase Shift Keying
DDM	Direct Digital Modulation
DPS	Digital Phase Shift
DDS	Direct Digital Synthesizer
DC	Direct Current
DPWM	Direct Pulse Width Modulation
DPIM	Digital Pulse Position
DPP	Digital Pulse Inverter Modulation
DPWM	Digital Pulse Width Modulation
DPIWM	Digital Pulse Inverter Width Modulation
DPPM	Digital Pulse Position Modulation

	DLL	Digital Local Loop
	DAC	Digital to Analogue Converter
E		
	EKG	Electrocardiogram
	EMG	Electromyography
	EGG	Electroencephalograph
	EOG	Electrooculography
	ECG	Electrocardiograph
	EFS	Electrical Field Strength
	EMI	Electromagnetic Interface
	EEG	Electroencephalography
	EMF	Electromagnetic Force
	EEPROM	Electrically Erasable Program Read-Only Memory
	η	Efficiency
F		
	FSK	Frequency shift keying
	FCC	Federal communication commission
	FS	Frequency Synthesizer
	FM	Frequency Modulation
	FET	Field Effect Transistor
	FPGA	Filed Programming Gate Array
	FDM	Full Digital Modulator
	FFT	Fourier Frequency Transfer
G		
	GND	Ground
	GMSK	Gaussian Minimum Shift Keying
	GFSK	Gaussian Frequency Shift Keying
H		
	HPA	Hybrid Power Amplifier
	HDR	High Data Rate
I		
	I	In-phase
	IC	Integrated Circuit
	IEEE	Institute of electrical and electronics engineers
	ISM	Industrial standard medical
	ISI	Inter symbol Interference
	ITU-R	International Telecommunication Union -Radio
	IF	Intermediate Frequency
	ISP	In system programmability
	IET	Institute of Electrical Technology
J		
	JTAG	Joint Test Access Group
	JAM-STAPL	JAM-Standard Test and Programming Language
K		
	KVL	Kirchhoff Voltage Low
	K	Coupling coefficient

L

LC	Inductance and Capacitance
LSB	Low Side Band
LPF	Low Pass Filter
LO	Local Oscillator
LNA	Line Noise Amplifier
LED	Light Emitting Diode
L	Inductance
λ	Lambda

M

M	Mutual Coupling
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUX	Multiplexer
MCF	Monitoring Frequency Control
MSK	Minimum Shift Keying
μ	Permeability
Φ	Magnetic Flux

N

Nr	Coil reader number
NRZ	None Return To Zero
NRZI	None Return To Zero Inverted
NRZL	None Return To Zero Level
LNF	Low noise frequency
NCO	Numerically Controlled Oscillator
NMOS	Negitive Metal Oxide Semi Conductor

O

OOK	On-Off Keying
Ω	Ohm
W	Omega
OPPM	Overlapping Pulse Position Modulation

P

PA	Power Amplifier
PCM	Pulse Code Modulation
PCB	Printed Board Circuit
PSK	Phase Shift Keying
PTL	Pass Transistor Logic
PWAM	Pulse width amplitude modulation
PAM	Pulse Amplitude Modulation
PPM	Pulse Position Modulation
PWM	Pulse Width Modulation
PLL	Phase Looked Loop
PSM	Pulse Shape Modulation
PEMF	Pulse Electromagnetic Frequency
PIM	Pulse Impulse Modulation
PSCC	Parallel to Serial Connection Circuit
PPCC	Parallel-to-Parallel Connection Circuit
PN	Pseudo Sequence

	PC	Personal Computer
	PID	Prototype Implant Device
	PIM	Pulse Interval Modulation
	PFM	Pulse Frequency Modulation
	ε	Permeability
	π	Pie
Q		
	Q	Quality Factor
	Q	Quadrature Phase
	QAM	Quadrature Amplitude Modulation
	QPSK	Quadrate Phase Shift Key
R		
	RFID	Radio Frequency Indication
	RZ	Return To Zero
	REFCLK	Reference Clock
	RF	Radio Frequency
	R	Resistance
	Rx	Receiver Signal
	RL	Relay
	RC	Rresistance Capacitor
T		
	TX	Transmitter Signal
S		
	SWR	Standing Wave Ration
	SAR	Specify absorption rates
	S/N	Signal to Noise ratio
	SWR	Switch Regulator
	SSCC	Serial to serial Connection Circuit
	SPCC	Serial to Parallel Connection Circuit
	SBD	Silicon Titanium Schottky Diode
	SOG	Spin-On Glass
	SEM	Scanning Electron Microscope
	SRAM	Static Random Access Memory
	SMT	Service Mount Technology
T		
	TWIT	Transcutaneous Wireless Implant Telemetry
	TTL	Transistor Logic
	TCK	Test Clock
	TDI	Test Data Input
	TMS	Test Mode Select Input
	TDO	Test Data Output
	TX	Transmit Signal
U		
	UHF	Ultra High Frequency
	UEA	Ultra Microelectrodes Arrays
	USB	Upper Side Band

V

VSWR	Voltage Standing Wave Ratio
VHDL	Very High Design Language
VCO	Voltage Control Oscillator
VR	Variable Resistance
VM	Voltage Multiplier

W

W	Width
W	Watts
WCP	Wireless Coupling Power
WSE	Wireless Capsule Endoscope
ω	Regular Frequency

Z

Z	Impedance

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Appendixes

Appendix A

Inductive Coupling Link

Appendix B

VHDL Code

Appendix C

Extra Hardware Implementation

Appendix

A

Inductive Coupling Link

Appendix - A

1. Synthesis and Simulation of the Reader and Implant Coils:

1.1 Preliminary design and consideration

The frequency has chosen for the reader unit is in low frequency the preliminary calculation was performed with the frequencies 125kHz, 135kHz and 145kHz. The appropriate frequency is selected to be use as RF power carrier frequency for the biomedical system in this thesis. In addition, to reduce the interference and the closed frequencies for the implant frequency such as RFID system, we selected the RF carrier frequency is 135kHz. However, several strategies for select the inductance values to the reader and the implant coils are investigated. To provide better performance for the magnetic coupling between these coils; firstly, the coil calculation and the simulation to fabricate our coil, which followed these steps as;

1. Design the coils in between [60µH~950µH].
2. Calculate the magnetic field B(x) at different distances.
3. Calculate the magnetic field B(x) with respects to reader current (I).
4. Calculate and plot the B(x) with respect to L (µH).
5. Choose the best coil with optimum magnetic field generation B(x.).
6. Choose the R-load in range [50~20kΩ].
7. Calculate the maximum Rx power to (RL) with respect L [µH].
8. Choose the optimum Rx power with respect to R-load over communication distance.
9. Repeat the procedure steps with all values of coils L (µH).
10. Choose the optimum coils0 for the received RX power.

The flow chart in Figure (A1.0) is demonstrated the design steps to program the MATLAB code, and how to calculate the inductance for the reader and the implant coils, that to provide the optimum performance at the chosen resonance frequency. The second design point is how to calculate the estimation power dissipation by the R_{load} at the implant part, where load resistance is varied according to the communication distance and matching with the LC tuned circuit. However, the load resistance was change according to distance between two coils. For this condition the accurate values was chosen by measurement to provide the optimum wireless received power, this matching condition between the implant tank circuit and the load, and

maximum resonance condition. The second flow chart (A1.1) is shown the programming steps design for calculate the optimum received power over distance range. The flow chart in Figure (A1.0) demonstrates the first steps for calculate the optimum diameter for the reader coil that for generates the magnetic flux at different distance in centimetre. The parameters values were chosen between 60 µH up to 950µH, and the coil diameter is in the range (3 cm~15 cm). However, the flow chart below has converted into MATLAB programming code to perform the mathematical calculation design for the optimum reader coil. The second design point is fabricate the coils, then measured them, and compared to the simulation values, the essential parameters that are calculated for the inductive link design. However, there are several design tools for calculation the inductance value approximation, to compare the accurate method with the measured one.

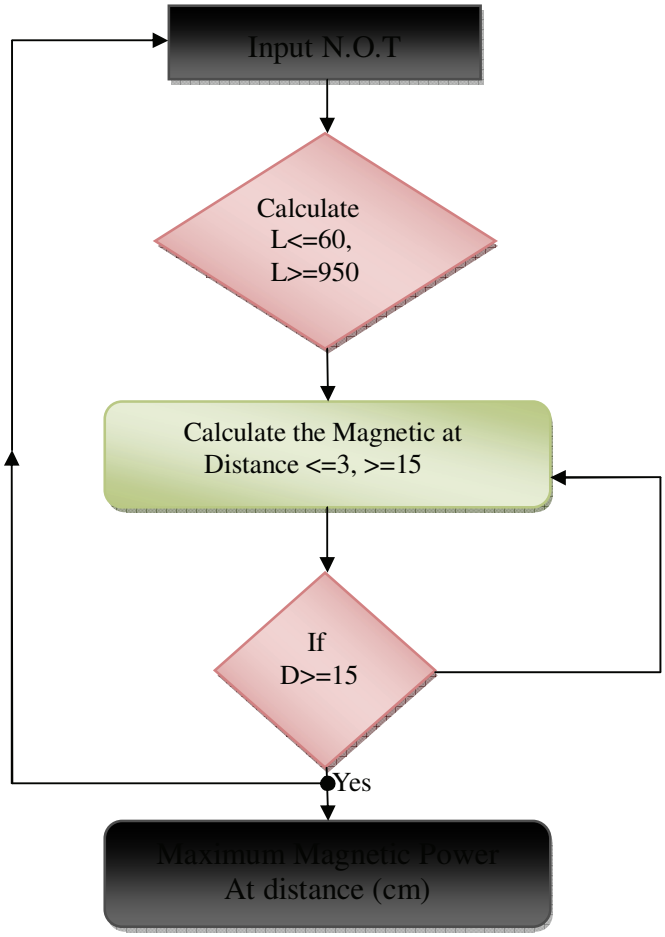


Figure (A1.0) flow chart to calculate the power dissipation by the load resistance

In the second simulation step, were the desired coils are terminated with the inductive coupling link, which is acting as open transformer for delivering the maximum wireless power for the implant coil. The diameter of the implant coil is critical and limited by the wire coil and the shape size. In our work, we chose the coil diameters between (2.5cm ~3.5cm), practically, the lower wire diameter provides a high internal resistance and higher inductance. The dissipation power by the load represent the maximum delivered power that can be provides from the reader coil through the magnetic wireless coupling.

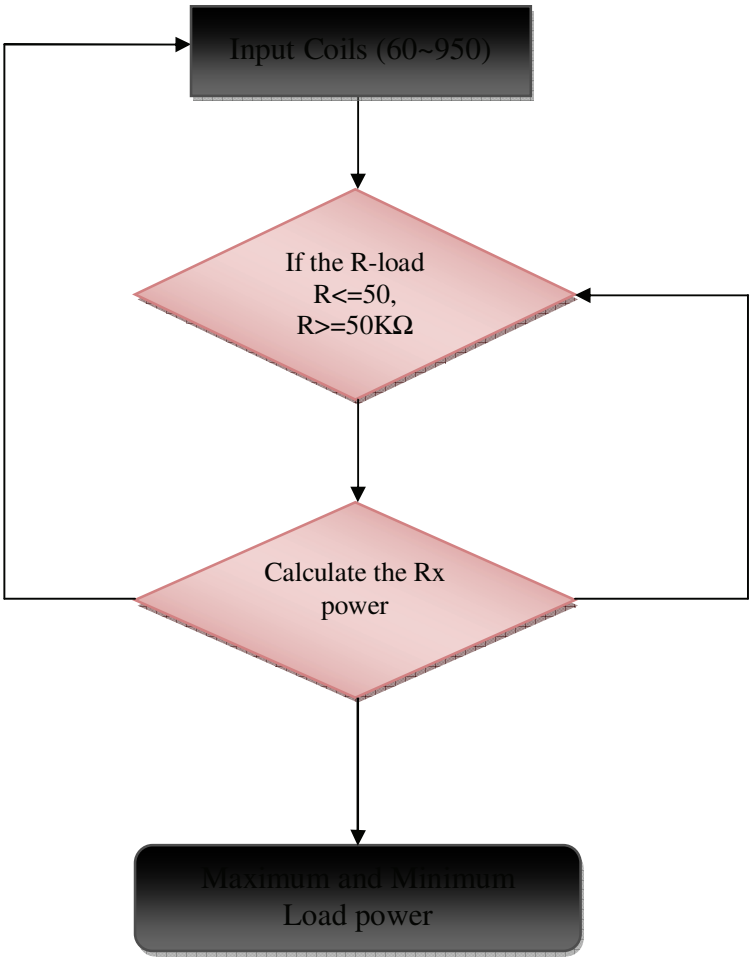
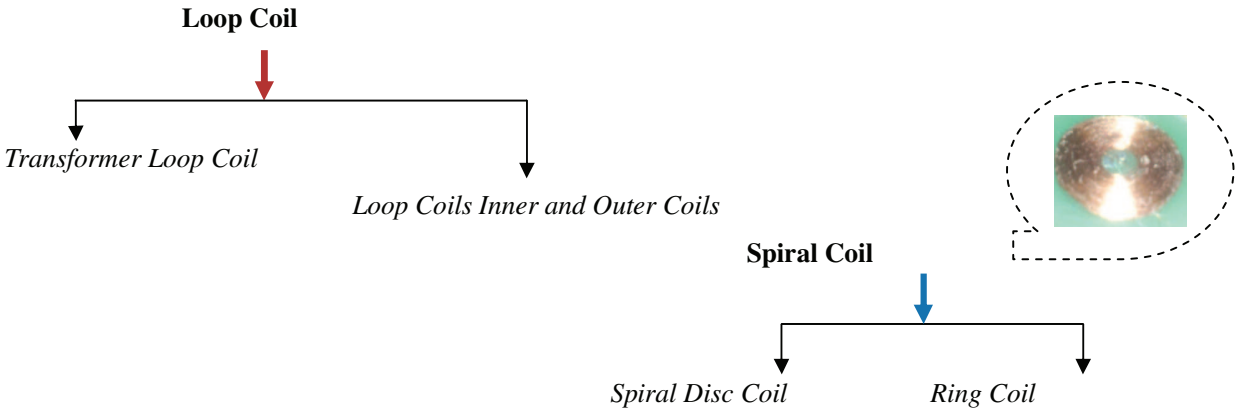


Figure (A1.1) flow chart to calculate the load power
Compared to different Coils

2. Biomedical Coils Design

2.1 Reader Coil Design

Several different types of coils are investigated for the reader unit. The reader coil is an important element to communication between the external world and the biodevices system. The magnetic inductive coupling is based to the transmission link between to coils, where the reader coil was synthesized with different types of shapes and wires. Those are for comparison the best coils and perform the maximum wireless transmission power coupling. Generally, the coil can be classified in three types: RF coil power and data coil or combined between these coils. However, samples of these coils are fabricated, and tested as shows in Figures (A1.2) (A1.3). Practically, sample of these coils are not suitable to provide the wireless RF power, especially the spiral coil design to the reader part, which is spread out the magnetic flux and is very weak RF power. Whilst, is a perfect a shape for in the implant part, which is harvesting most of the magnetic flux compared to other coils. We selected two types of coils; loop coil at reader and spiral coil at the implant.



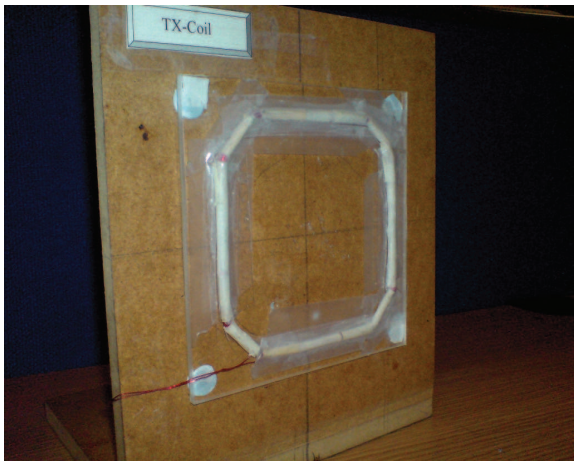


Figure (A1.2) tested TX power coil at reader shape used in our work

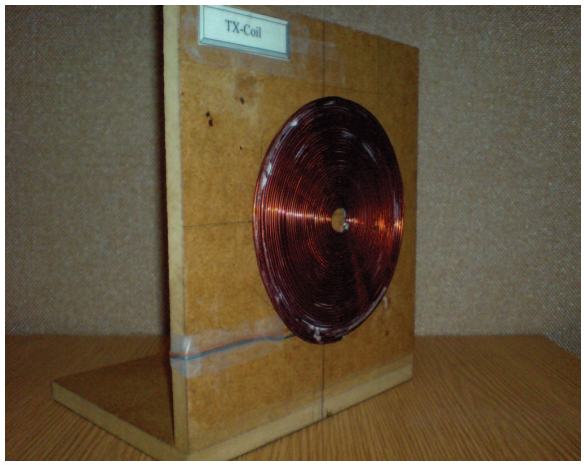


Figure (A1.3) the spiral coil at reader part Loop as TX coil (Not used)

The simulation and the calculated designed for the perfect coil was evaluated in the measurements, over different values for the reader coils between 64 µH~963µH at the carrier frequency 135kHz. In this case, the reader coil was fixed at 933.4µH and the implant coil is changed with different values at diameter 30mm in size. The measurements results are shows in Figure (A1.4). The best coil was given at 528µH, the second measurements was performed by changed the reader coil and the fixed implant, which gives the best coil at 550µH, as shows in Figure (A1.5).

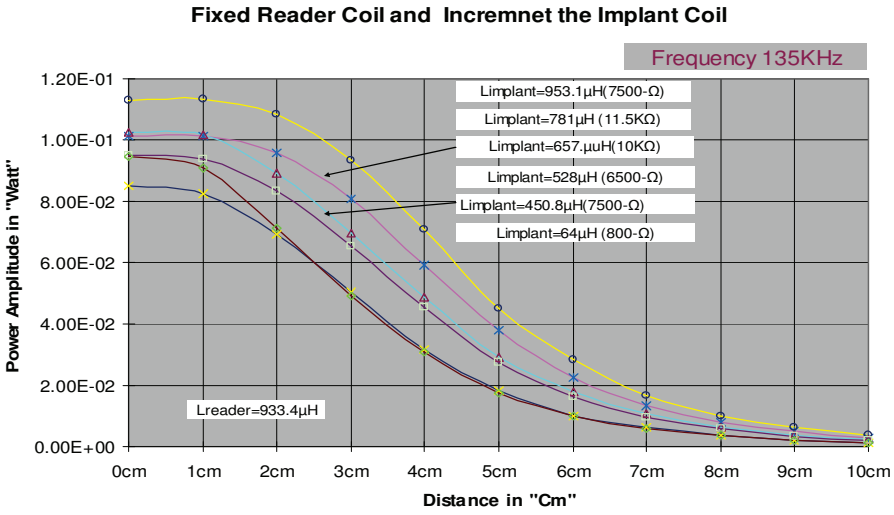


Figure (A1.4) Received RX power over different implant coils at fixed reader coil

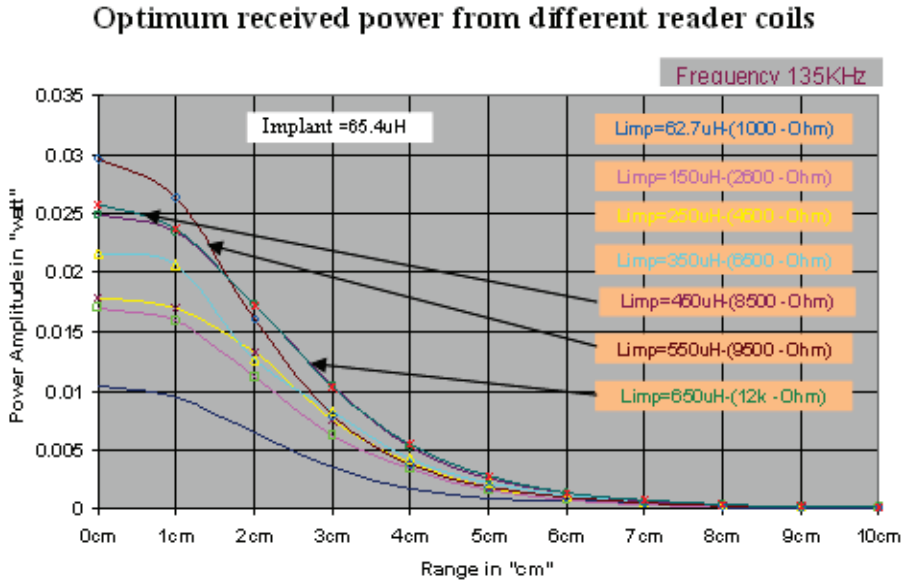


Figure (A1.5) Received Rx wireless power for the fixed implant Coil and changed the reader coil

2.2 An Introduction to Coils for Medical Applications

To design an ideal coil as a passive telemetry system for magnetic inductive coupling link and several factors are considered to analysis and synthesis the inductors. Alternatively, the implant coil is dependants on how magnetic field can be harvested with minimum size. We described in Figure (A1.6) the most common parameters that are affected in the mathematical calculation and the coil design, which is used as passive inductive link. However, more details are illustrated in Figure (A1.7), for the spiral coil design at the implant part. The implant coil is still under investigation for a perfect design. In addition, different tools are investigated for design the magnetic coupling such as COMSOL, QUENCH [221], [222].

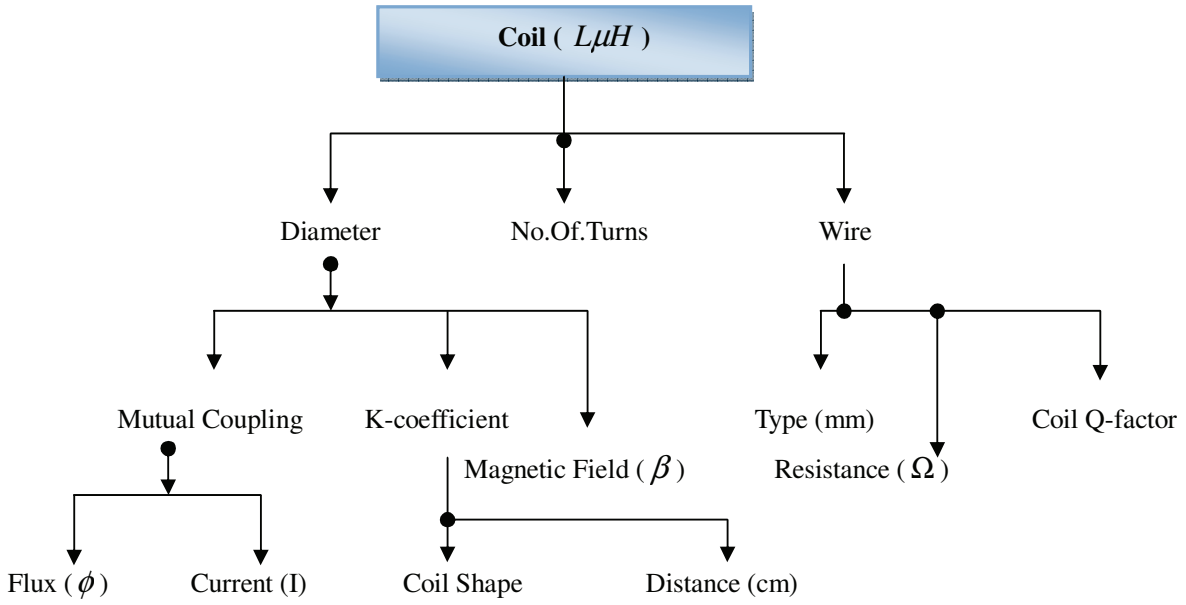


Figure (A1.6) Most common factor parameters for coil design

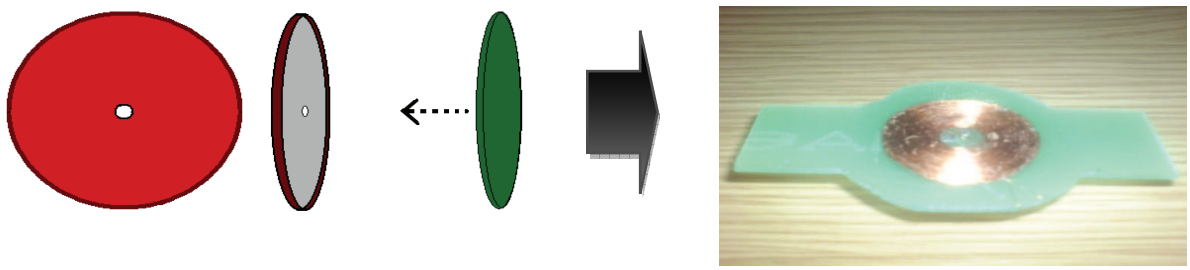


Figure (A1.7) The spiral coil design for implant in our work, 30mm diameter for the Rx- wireless received power

3. Additional Investigation for Misalignment Position:

Another technical solution has been investigated to solve the misalignment problem, in the near field communication. This problem is affected in the wireless received power this reduced the implant efficiency. Our proposed design used two separated identical coils, are located in the centre angles outside the body reader coils, both are transmitting the RF power at the same frequency, and received with a single implant coil. The implant coil sums the received RF signals; the amplitudes are double, Figure (A1.8) shown the basic idea for solving misalignment problem.

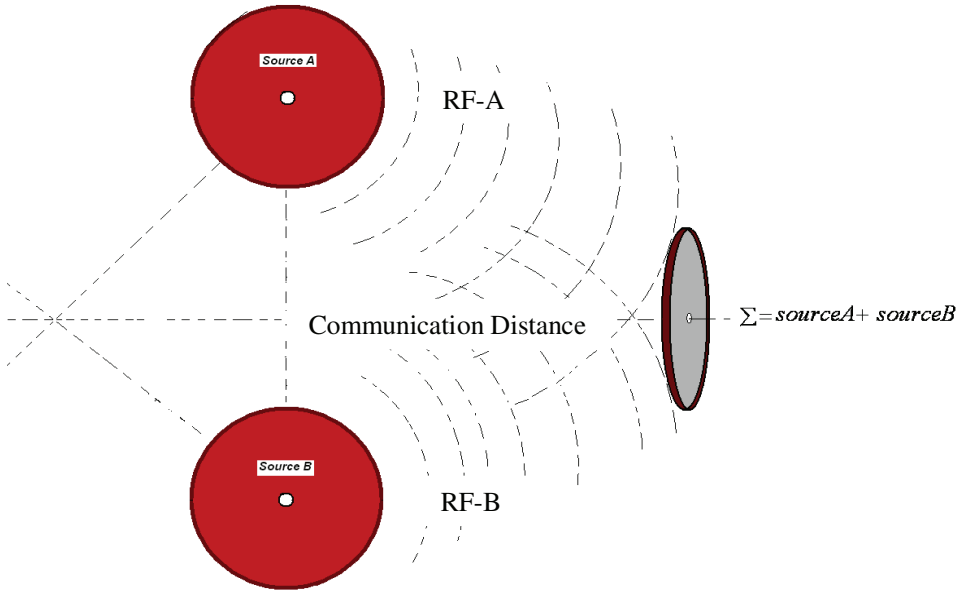


Figure (A1.8) the basic idea of using two identical sources

The first source is expressed in equation (1), where the second source can be expressed in equation (2) respectively.

$$source_1(t) = A_1 \cos(\omega t + \phi_1) \quad (1.0)$$

$$source_2(t) = A_2 \cos(\omega t + \phi_2) \quad (2.0)$$

The implant-received coil was added the received magnetic fields together, which produced AC voltages. The output can be express mathematically in equation below (3.0); the result of the voltages at the output of the implant coil is;

$$Output_{\Sigma} = A_1[\cos(\omega t + \phi_1) + A_2 \cos(\omega t + \phi_2)] \quad (3.0)$$

$$\because \quad \cos u + \cos v = 2\cos\left(\frac{u+v}{2}\right)\cos\left(\frac{u-v}{2}\right)$$

$$Output_{\Sigma} = A_1 + A_2\left[\cos\left(\left(\frac{(\omega t+\phi_1)+(\omega t+\phi_2)}{2}\right)\cos\left(\frac{(\omega t+\phi_1)-(\omega t+\phi_2)}{2}\right)\right)\right] \tag{4.0}$$

In case, where both sources are equals in phase the equation (4.0) can be rewritten as:

$$Output_{\Sigma} = \frac{2(A_1+A_2)}{2}\left[\cos(\omega t+\phi_1)+(\omega t+\phi_2)\cos(\omega t+\phi_1)-\cos(\omega t+\phi_2)\right] \tag{5.0}$$

If the phases of both signals are equals ($\phi_1 = \phi_2$), the output summation is given in equation as:

$$Output_{\Sigma} = A_1 + A_2\left[(\cos(\omega t+\phi_1)\cos(\omega t+\phi_1)\right] \tag{6.0}$$

The implant coil is working as PBF, which is removes, the second harmonics of the signal. The output will be producing a double voltage at the implant coil can expressed in equation (7.0) as:

$$Output_{\Sigma} = A^2\cos(\omega t+\phi) \tag{7.0}$$

3.1 Lab Measurements and Summary

The proposed idea has evaluated with the lab measurements; we can conclude the received power at the implant has affected by the received magnetic field, influence by both sources. Conversely, the orientation angles of both coils are critical to fixed, where the implant is movement part that needs to re-adjust the reader's coils angle. Figure (A1.9) is illustrated the comparison of each coil and the summation results for the received power that are compared with a single coil equivalent to the both coils values.

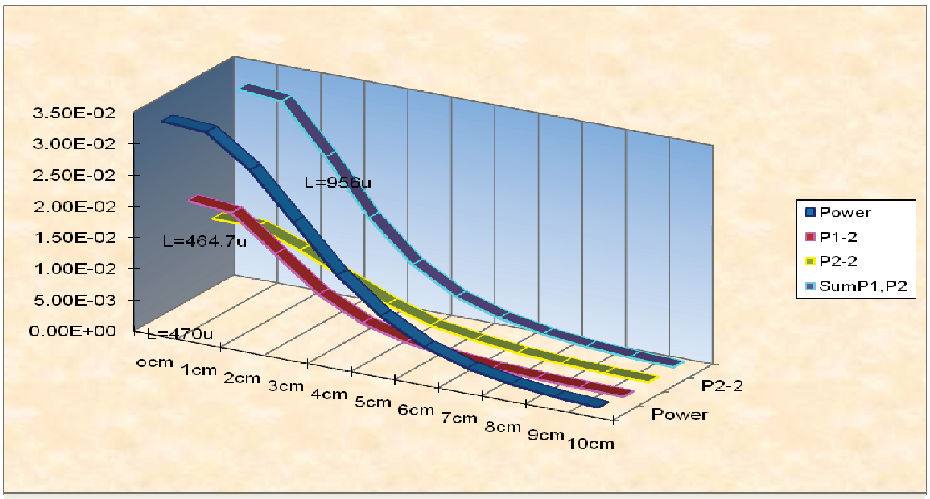


Figure (A1.9) the received power with two identical coils comparing to single coil

Appendix

B

VHDL Code

Appendix - B

1. Appropriate Topologies

The VHDL techniques demonstrated by many brands with different development kits. In this work, where try first with Altera development board as demonstrated in Figure (B1.0). The second board was tried with Xilinx board as shown in the Figure (B1.1) that is used to generate the VHDL programming codes and simulate it. The measurements was evaluated with the Altera development board for testing the proposed modulators with VHDL code and compared them with the simulated, for these codes the BPSK, QPSK and 8-PSK modulators.

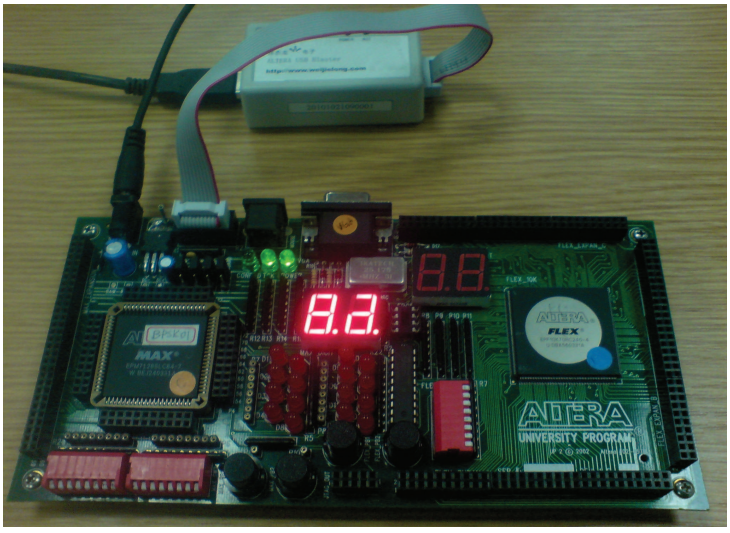


Figure (B1.0) the Altera development board FPGA/CPLD

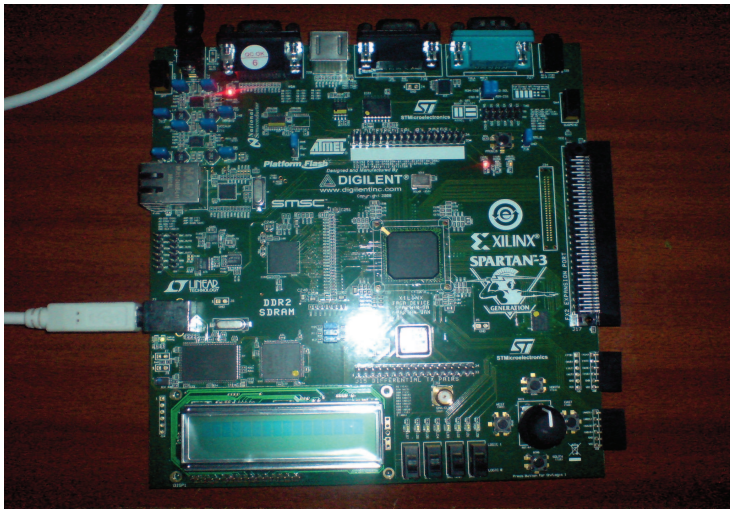


Figure (B1.1) the Xilinx development board FPGA /CPLD

2. The VHDL programming Codes for proposed Modulators:

We classify the modulators into three schemes: the BPSK, QPSK and 8PSK, each modulator has synthesized with two methods the structural and the behavioral design, to evaluate both methods. We implanted both methods with the hardware, to evaluate the appropriate method, to compare between them as the best performance modulator. However, the structural and behavioral methods have given the same performance in BPSK modulator, where it is not sufficient for the QPSK and 8-PSK modulators. Whilst the behavioral method given better efficiency for three modulators. Generally, both methods have programmed in VHDL code, started with top level of the modulator (inputs/outputs). The efficiency performance of the digital modulator is dependent on the accurately produced carrier signal, the carrier phase shifter it is also the critical element design, which affects in the performance of the modulator. If there is any error between the carrier phase signals, that affecting in the phase transition of the carrier signal. However, these problems have solved by calculating the delay, and re-design the carrier phase shifter, conversely that produced a perfect output signals with zero error. This appendix has covered most of the programming generated codes for modulators. Generally, the classifications of both methods are illustrated in diagram B (1.2).

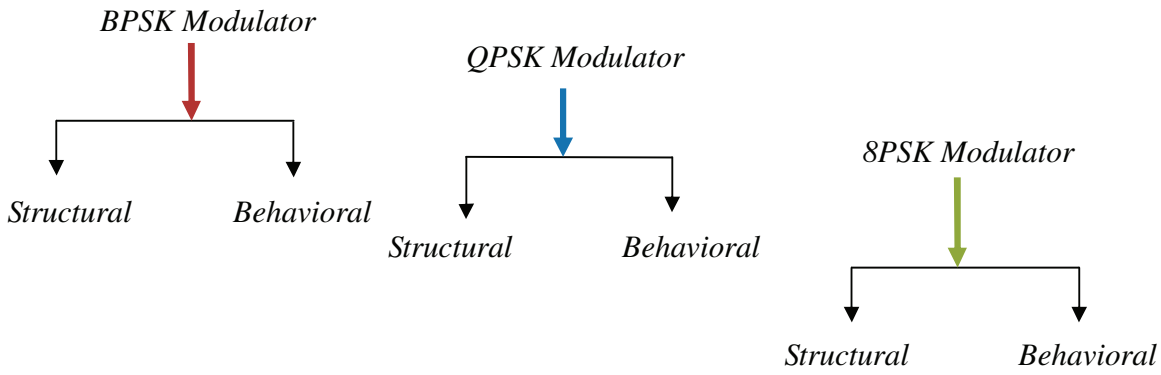


Figure (B1.2) the structural and behavioral methods for the three different schemes

2.1 The BPSK VHDL Programming Code (Structural)

```
-------------------------------------------------------------------------------------------------------------------------
--                                        Newcastle University                                                         --
--                                             School Of                                                               --
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--                                                                                                                     --
--                                                                                                                     --
--      Full Digital BPSK/ QPSK/8PSK Modulator Using CPLD/FPGA                                                         --
--      Author              : Gihad Elamary                                                                            --
--      Supervisor's        : Dr. Graeme Chester and      : Mr. Jeffery Neasham                                        --
--      Date and Yea r      : 2010                                                                                     --
--                                                                                                                     --
-------------------------------------------------------------------------------------------------------------------------

-------------------------------------------------------------------------------------------------------------------------
|                                TO Level of the BPSK / Digital Modulator (Structural)                                |
-------------------------------------------------------------------------------------------------------------------------

LIBRARY IEEE;
USE ieee.std_logic_1164.all;

 entity Carrier_Phase is
        port ( Carrier_in      : in  std_logic;
                  I0 , I180        : buffer  std_logic);
end Carrier_Phase;

architecture structral of Carrier_Phase is

 component NOT1
                                                  ---------------------- Component declaration for Not Gate
        port ( A       : in   std_logic ;
                  X       : out std_logic );
       end component;

 component my_dff1
                                                  -------------------------------- Component declaration DFF
        port ( d , clk    : in  std_logic ;
                  q          : buffer  std_logic);
       end component;
```
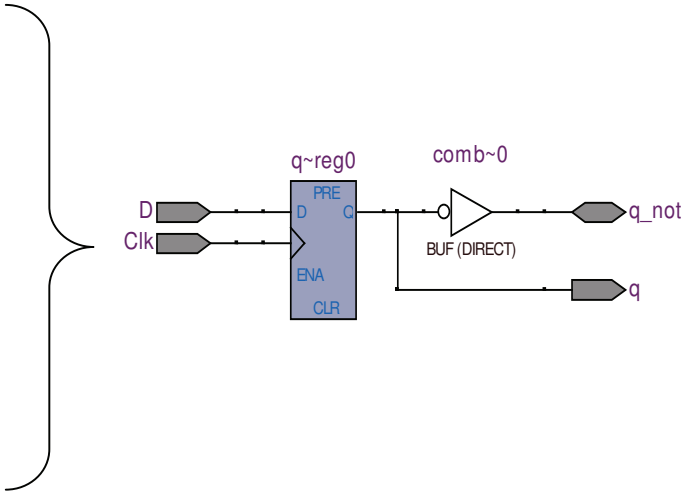

```
    signal  FF0 , FF0_NOT : std_logic;          ----------declaration of the signal used to interconnected

 begin

         U0 : my_dff1  port map ( clk => Carrier_in , q => FF0 , d => FF0_NOT );
         U1 : NOT1     port map ( A => FF0 , X => FF0_NOT );

        I0   <= FF0 ;
        I180 <= FF0_NOT ;

end structural;
```

----------DFF1 declaration

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;


entity my_dff1 is
            port ( d , clk   : in  std_logic;
                        q         : buffer  std_logic);
end my_dff1;

 architecture Behavior of my_dff1 is

   begin
            process( d , clk )
       begin

           if (clk'event and clk='1') then
         q <= d;
      end if;
  end process;
end behavior;
```



----------NOT Gate Declaration

```
library ieee;
use ieee.std_logic_1164.all;

 entity NOT1 is
     port( A    : IN   std_logic;
           X    : OUT  std_logic);
    end NOT1;

 architecture behavoural of NOT1 is
   begin
           X <= not A ;
end behavioral;
```

The simulation of the VHDL code has presented in Figure (B1.3), where the carrier frequency and the data are interfaced together from the external source board to the development Altera board. However, the practical structural modulator has synthesized with CPLD chip as demonstrated in Figure (B1.4).

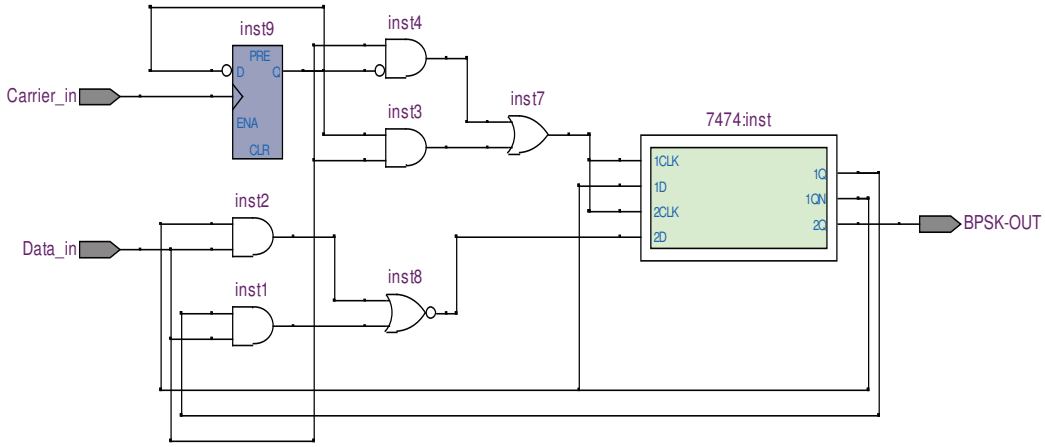


Figure (B1.3) the VHDL of the structural BPSK modulator module (A)

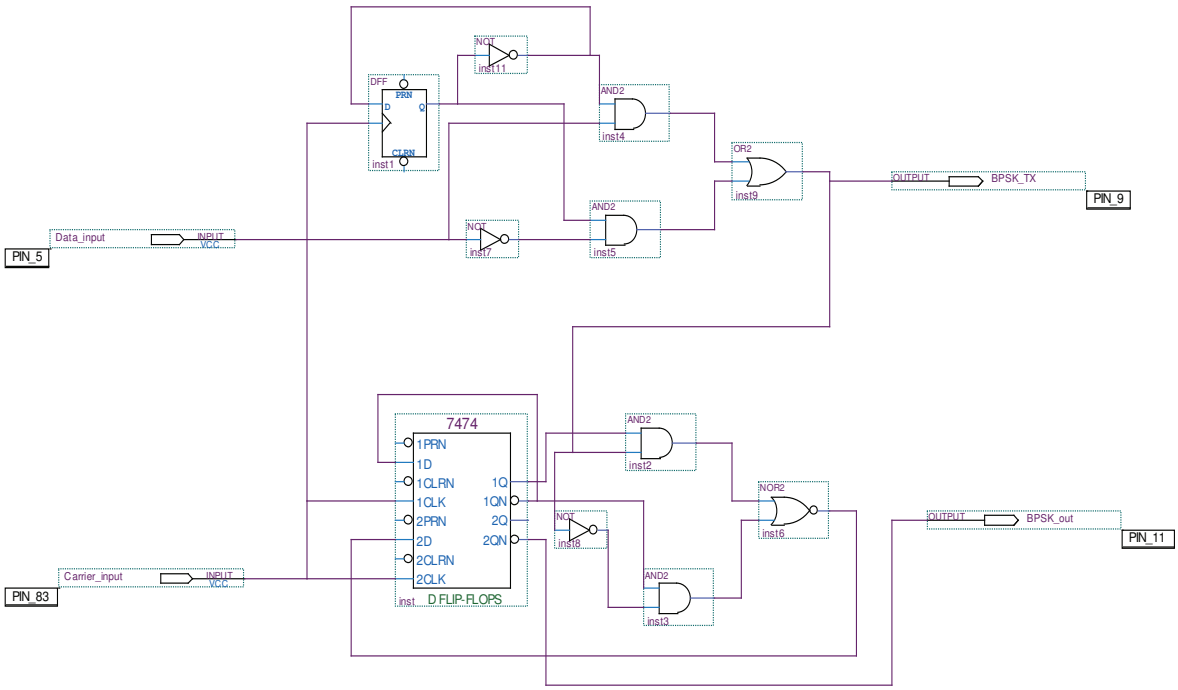
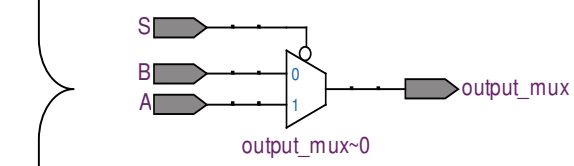


Figure (B1.4) the block diagram of the structural BPSK modulator Module (B)

```
--------------------------------------------------------------------------------------------------------------
|                                                                                                            |
|                    TO Level of BPSK / Digital Modulator (VHDL Behavioral code)                             |
--------------------------------------------------------------------------------------------------------------

LIBRARY IEEE;
USE ieee.std_logic_1164.all;

 entity BPSK_mod is                              ---------------------------- Declaration of modulator
          port( Master_clock       : in  std_logic;
                Rest               : in  std_logic;
                BPSK_output        : out std_logic;
                Test_PN            : out std_logic);
          end BPSK_mod ;

 architecture b_mod of BPSK_mod is

       signal  K0 , K1 , K2 , K3 : std_logic ;

component  mux_2                                 ------------------------------Component declaration
          port ( A , B                 : In      std_logic;
                   S                   : In      std_logic;
             output_mux                : buffer  std_logic);
          end component ;

component Carrier_Phase
          port ( Carrier_in            : in  std_logic;
                   I0 , I180           : inout std_logic);
          end component;

component  Freq_div2MHz
          port ( clk                   : in  std_logic;
                  Div_out              : buffer std_logic);
          end component;

component PN_gen
          port ( Clk                   : IN std_logic;
                PN_out                 : inout std_logic);
          end  component;

  begin

   U0 :    Carrier_Phase     port map ( Carrier_in => Master_clock , I0 => K0 , I180 => K1 );
   U1 :    Freq_div2MHz      port map ( clk => Master_clock , Div_out => K2 );
   U2 :    PN_gen            port map ( Clk => K2 , PN_out => K3 ) ;
   U3 : mux_2          port map ( A => K0 , B => K1 , S => K3 , output_mux => BPSK_output );

       Test_PN <= K3 ;
 end b_mod ;
```

VHDL code for Multiplexer

```
library ieee;
use ieee.std_logic_1164.all;

        entity mux_2 is
            port ( A , B        : In std_logic;
                   S            : In std_logic;
                output_mux      : out std_logic);
        end mux_2;

architecture behavior of mux_2 is
  begin
        process ( A , B , S )
  begin
       if  s='0' then
       output_mux <= A ;
  else
       output_mux <= B;
     end if;
  end process;
end  behavior;
```



VHDL code for the Carrier Frequency

```
library ieee;
use ieee.std_logic_1164.all;

        entity Carrier_Phase is
              port ( Carrier_in      : in  std_logic;
                     I0 , I180       : buffer  std_logic);
        end Carrier_Phase;

architecture structral of Carrier_Phase is

 component NOT1                          ---------------------------------- Component declaration
        port ( A                        : in std_logic ;
               X                        : out std_logic );
        end component;

 component my_dff1
          port ( d , clk                : in  std_logic ;
                 q                      : buffer  std_logic);
        end component;
```

```
signal  FF0 , FF0_NOT : std_logic;              ------declaration of the signal used to interconnected

     begin

  U0 : my_dff1    port map ( clk => Carrier_in , q => FF0 , d => FF0_NOT );
  U1 : NOT1       port map ( A => FF0 , X => FF0_NOT );

       I0   <= FF0 ;
       I180 <= FF0_NOT ;
end structural;

LIBRARY ieee;                                   ---------------------------------------- DFF1 declaration
USE ieee.std_logic_1164.all;

       entity my_dff1 is
            port ( d , clk   : in  std_logic;
                       q        : buffer  std_logic);
           end my_dff1;

 architecture Behaviour of my_dff1 is
       begin
          process( d , clk )
       begin
            if (clk'event and clk='1') then
            q <= d;
       end if;
    end process;
 end behaviour;



library ieee;                                   ----------------------------------------NOT Declaration
use ieee.std_logic_1164.all;

         entity NOT1 is
              port( A       : IN   std_logic;
                         X       : OUT  std_logic);
         end NOT1;
 architecture behavioral of NOT1 is

         begin
                  X <= not A ;
         end behavioral;
```

```
--------------------------------------------------------------------------------------------------------------
|                                  VHDL code for Frequency Divider -2MHz                                     |
--------------------------------------------------------------------------------------------------------------

library ieee;
use ieee.std_logic_1164.all;

      entity Freq_div2MHz is
            port ( clk          : IN  std_logic;
                   Div_out      : buffer std_logic);
      end Freq_div2MHz ;

architecture  behavior of Freq_div2MHz is

         type states  is ( zero, one, two, three, four, five, six, seven, eight, nine, ten, eleven );

 signal present_state , next_state : states;

       signal temp : std_logic;                  ---------------------------- Positive Edge clock process

         begin
               process (clk)
         begin
               if ( clk'event and clk ='1') then
                  present_state  <=  next_state;
         end if;
    end process;
       process ( present_state )                 ------------------- Positive edge FSM  for present state
 begin
      case present_state is

            when zero   => temp  <='0'; next_state  <= one ;
            when one    => temp  <='0'; next_state  <= two ;
            when two    => temp  <='0'; next_state  <= three ;
            when three  => temp  <='0'; next_state  <= four ;
            when four   => temp  <='0'; next_state  <= five ;
            when five   => temp  <='0'; next_state  <= six ;
            when six    => temp  <='1'; next_state  <= seven ;
            when seven  => temp  <='1'; next_state <=  egith ;
            when egith  => temp  <='1'; next_state  <= nine ;
            when nine   => temp  <='1'; next_state  <= ten ;
            when ten    => temp  <='1'; next_state  <= eleven ;
            when eleven => temp  <='1'; next_state  <= zero;

     end case;
 end process;
          Div_out   <= temp ;
end behavior;
```

VHDL code for the PN sequence

```
library ieee;
use ieee.std_logic_1164.all;

        entity PN_gen is
                port ( Clk          : IN std_logic;
                        PN_out   : OUT std_logic);
        end PN_gen ;
   architecture behavior of PN_gen is
             type states  is ( zero , one , two ,three , four , five ,six , seven );
             signal present_state , next_state : states ;
             signal out_1 :std_logic ;
        begin
                process (clk)
        begin

             if ( clk'event and clk='1') then
                  present_state  <= next_state;
                  PN_out <= out_1;
        end if;

 end process;
                  process ( present_state )
        begin
                  case present_state is
                 when zero   => out_1 <= '0'; next_state <= one ;
                 when one    => out_1 <= '1'; next_state <= two ;
                 when two    => out_1 <= '0'; next_state <= three ;
                 when three  => out_1 <= '1'; next_state <= four;
                 when four   => out_1 <= '1'; next_state <= five;
                 when five    => out_1 <= '1'; next_state <= six;
                 when six      => out_1 <= '0'; next_state <= seven;
                 when seven  => out_1 <= '0'; next_state <= zero;
       end case;

    end process;

 end behavior;
```

The simulation of the VHDL code for BPSK modulator has presented in Figure (B1.5), where each part of the modulator is simulated individual. The carrier simulation is shown in Figure (B4.6). However the multiplier has been illustrated in Figure (B1.7), where the frequency divider has been depicted in Figure (B1.8) finally, and the PIN sequence code generator is demonstrated in Figure (B1.9).

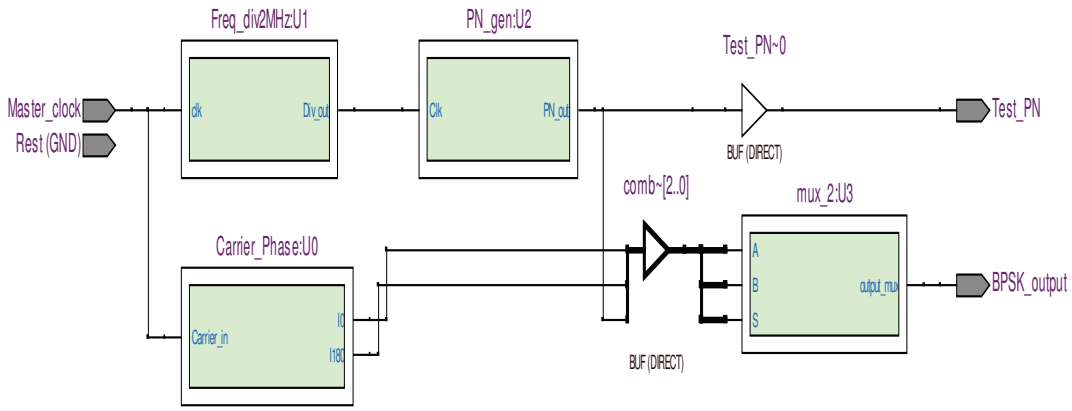


Figure (B1.5) the block diagram of the behavioral BPSK modulator

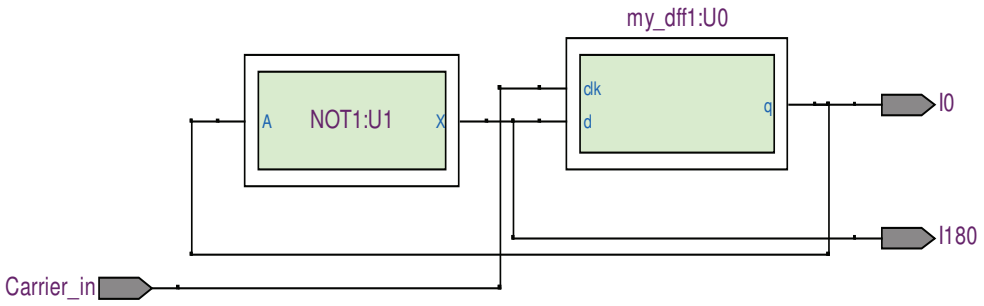


Figure (B1.6) the carrier simulation for generates (0,180)

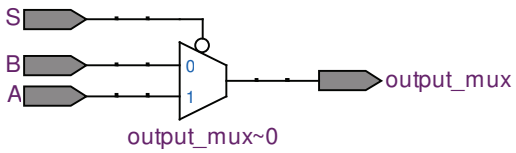


Figure (B1.7) the simulation behavioral of multiplexer

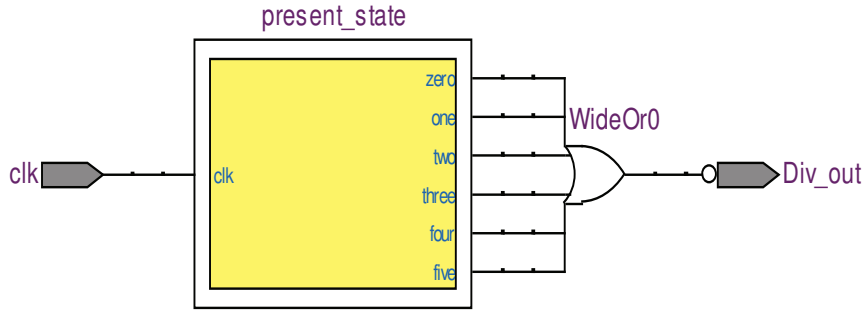


Figure (B1.8) the simulation behavioral of frequency divider

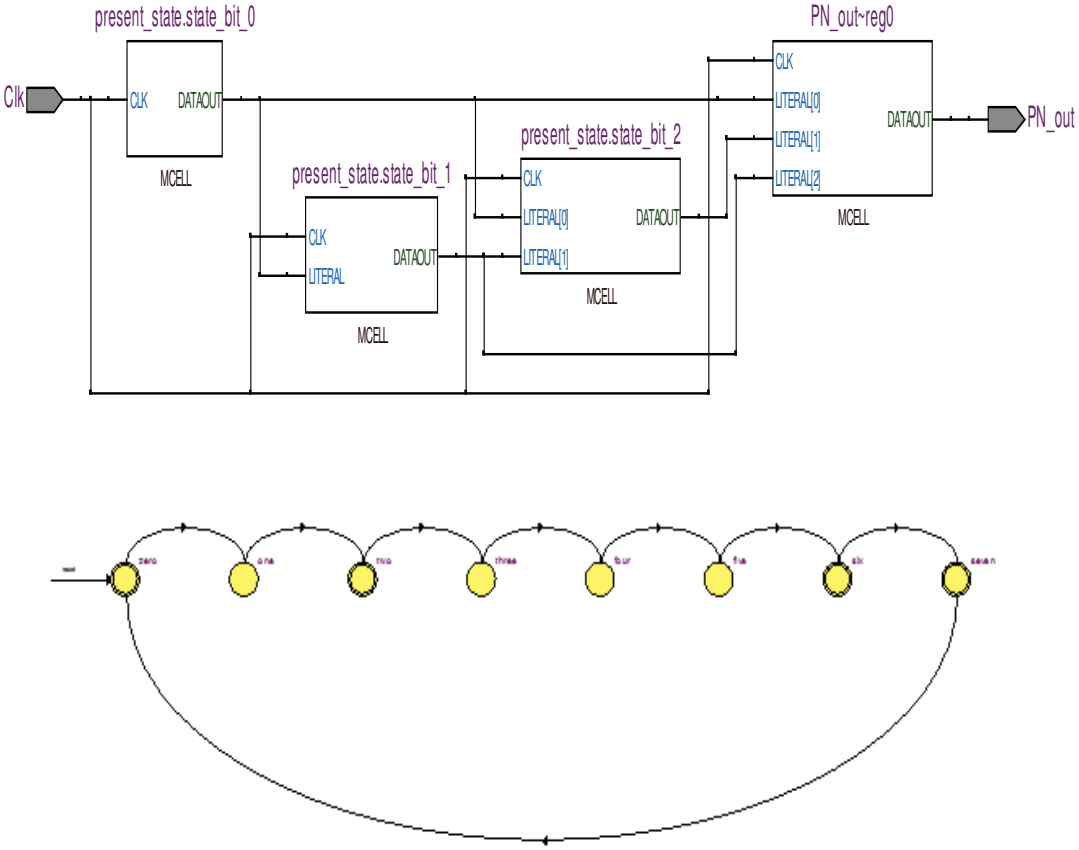


Figure (B1.9) the simulation behavioral of the PN sequence code and the states

End of Digital BPSK Modulator

The second proposed modulator is the QPSK; where try to synthesize the QPSK modulator by programming the VHDL code. The modulator has been designed using the previous methods structural and behavioral as:

```
-------------------------------------------------------------------------------------------------------------
|                                TO Level of QPSK / Digital Modulator (Structural)                          |
-------------------------------------------------------------------------------------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

    entity   QPSK_Modulator  IS                              ---------- Top level of Digital QPSK
               PORT( Data_in         : IN     STD_LOGIC;
                     carr_in         : IN     STD_LOGIC;
                   QPSK_out        : out    STD_LOGIC);
         end QPSK_Modulator;

 architecture  structure of QPSK_Modulator is

    component  Data_Mapping                                  ---------- Data mapping declaration
             port ( D_in    : in  std_logic;
                    I       : buffer std_logic;
                    Q       : buffer std_logic);
            end component;

 component  Carrier_Phase                                    ----- Carrier Phase shift declaration
             port ( Carrier_in      : in  std_logic;
                    I0 ,I90         : buffer  std_logic;
                    I180 , I270   : buffer  std_logic);
            end component;

 component mux4to_1                                          ------------- Multiplexer declaration
             PORT (A0, B90, C180, D270   : IN      STD_LOGIC;
                    S                          : INOUT   STD_LOGIC_VECTOR (1 DOWNTO 0);
                     mux_out                : buffer  STD_LOGIC );
              end component;

     signal  SC0 , SC1 , C2 , C3 , C4 , C5 : std_logic ;     ----------- internal connection signal

      begin

DM0 : Data_Mapping   port map ( D_in => Data_in , I => SC0, Q => SC1  );
CM1 : Carrier_Phase  port map ( Carrier_in => carr_in , I0 =>  C2 , I90 => C3 , I180 => C4
                                ,I270 => C5 );
MM2 : mux4to_1       port map ( mux_out => QPSK_out , S(0) => SC0 , S(1) => SC1, A0 =>
                                C2 , B90 => C3 , C180 => C4 , D270 => C5 );
   end structure;
```

```
--------------------------------------------------------------------------------------------------------------
|                                    Structure code for the Data Mapping                                     |
--------------------------------------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;

        entity Data_Mapping is                          -- Top Level Of Data Mapping for Modulator
              port ( D_in     : in  std_logic ;
                        I       : out std_logic;
                        Q       : out  std_logic);
              end Data_Mapping;

architecture structural of Data_Mapping is

        component NOT1                                  ------------------------ Component declaration
              port ( A   : in std_logic ;
                     X   : out std_logic );
              end component;

        component my_dff1
              port ( d , clk  : in      std_logic;
                        q         : buffer  std_logic;
                        q_not   : out     std_logic);
              end component;
----------------------Declaration of the signal used to interconnected ----------------------------------

             signal  FF0 , FF0_NOT , FF1 , FF1_NOT : std_logic;

             begin

        U0 : my_dff1   port map  ( clk => D_in , q => FF0 , d => FF0_NOT );
        U1 : NOT1      port map  ( A => FF0 , X => FF0_NOT );
        U2 : my_dff1   port map  ( clk => FF0_NOT , q => FF1 , d => FF1_NOT );
        U3 : NOT1      port map  ( A => FF1 , X => FF1_NOT );

             I <= FF0;
             Q <= FF1;

    end structural;
------------------------------------------- D Flip Flop declaration ------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.all;

       entity my_dff1 is
            port ( d , clk   : IN     std_logic;
                      q         : buffer std_logic;
                      q_not   : out    std_logic);
          end my_dff1;
```

```
architecture Behavior of my_dff1 is
            begin
                process( d , clk)
            begin
                 if ( clk'event and clk= '1' ) then
                q <= d;
            end if;
        end process;
                 q_not <= NOT q;
    end behavior;

--------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;

            entity NOT1 is                          ---------- NOT Declaration
                 port( A    : IN   std_logic;
                       X    : OUT  std_logic);
            end NOT1;
 architecture behavioral of NOT1 is
            begin
                 X <= not A ;
            end behavioral;
-------------------------------------Top Level of Carrier Phase Shifter----------------------------------
library ieee;
use ieee.std_logic_1164.all;
           entity Carrier_Phase is
               port ( Carrier_in      : in  std_logic;
                      I0 ,I90         : buffer  std_logic;
                      I180 , I270     : buffer  std_logic);
           end Carrier_Phase;
architecture structural of Carrier_Phase is
           component NOT1                       ---------- Component declaration
                port ( A   : in std_logic ;
                       X   : out std_logic );
           end component;
            component my_dff1
                port ( d , clk  : in  std_logic ;
                         q      : buffer  std_logic);
            end component;
```

```
----------Declaration of the signal used to interconnected----------

    signal  FF0 , FF0_NOT , FF1 , FF1_NOT , CAR_NOT  : std_logic;
  begin
      U0 : my_dff1    port map ( clk => Carrier_in , q => FF0 , d => FF0_NOT );
      U1 : NOT1       port map ( A => FF0 , X => FF0_NOT );
      U2 : my_dff1    port map ( clk => CAR_NOT, q => FF1 , d => FF1_NOT );
      U3 : NOT1       port map ( A => FF1 , X => FF1_NOT );
      U4 : NOT1       port map ( A => Carrier_in ,X => CAR_NOT );
          I0   <= FF0;
          I180 <= FF0_NOT;
          I90  <= FF1;
          I270 <= FF1_NOT;
  end structural;

---------- Top Level of Multiplexer 4 to 1 ----------

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

      ENTITY mux4to_1 IS

          PORT ( A0, B90 , C180 , D270 : IN      STD_LOGIC ;
                          S                : inout   STD_LOGIC_VECTOR (1 DOWNTO 0);
                    mux_out                : buffer  STD_LOGIC );
            END mux4to_1;
 ARCHITECTURE  multiplexer4x1 OF mux4to_1 IS

      BEGIN
          PROCESS ( S , A0 , B90 , C180 , D270 )
    BEGIN
          CASE S IS
                  WHEN "00"         =>    mux_out  <=  A0;
                  WHEN "01"         =>    mux_out  <=  B90;
                  WHEN "10"         =>    mux_out  <=  C180;
                  WHEN  OTHERS =>    mux_out  <=  D270;
          END CASE ;
  END PROCESS;
 END multiplexer4x1;
```

The simulation of the VHDL code for the structural QPSK modulator has presented in Figure (B1.10), where the carrier frequency and the data interfaced from the external boards. However, the practical modulator has synthesized with the CPLD chip has demonstrated in Figure (B1.11).

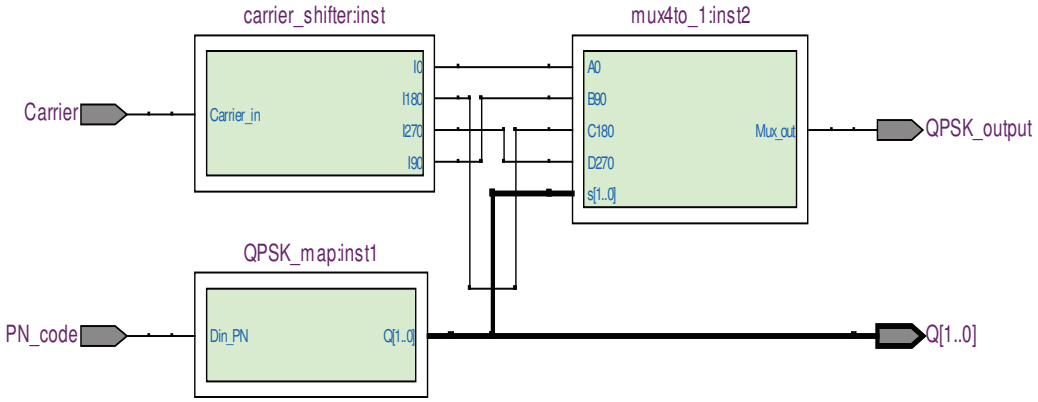


Figure (B1.10) Demonstrate the VHDL of the structural QPSK modulator

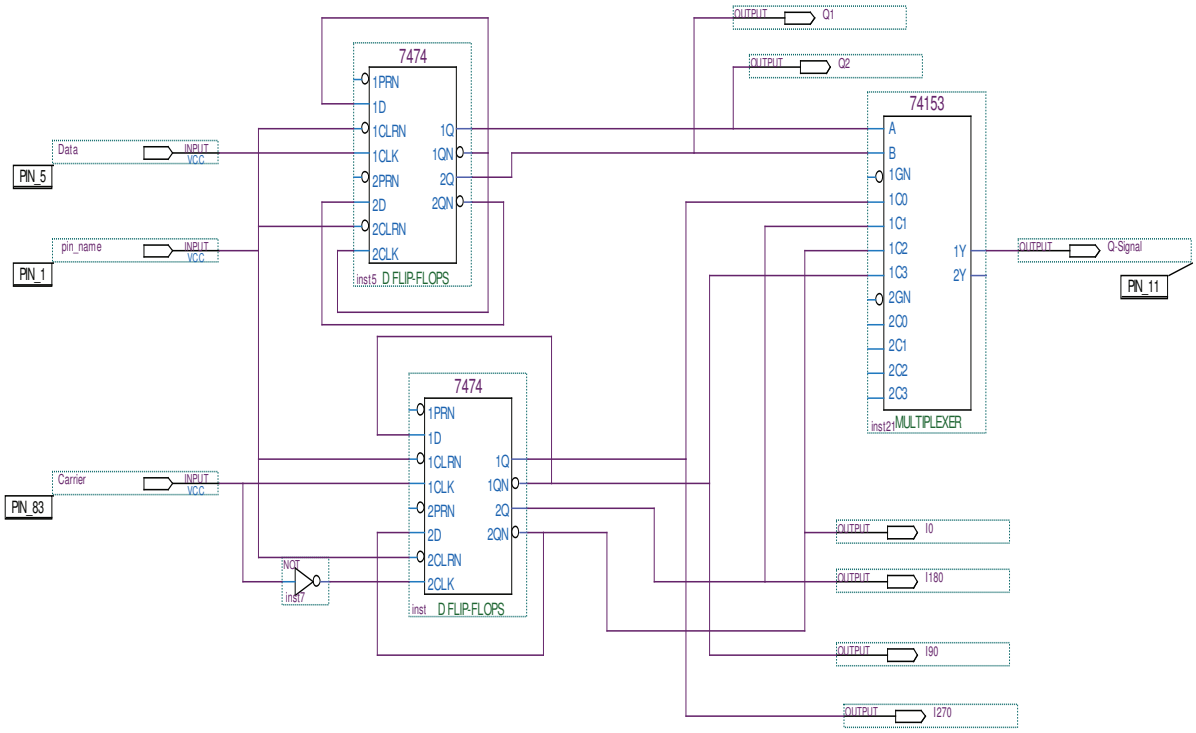


Figure (B1.11) the block diagram of the structural QPSK modulator

```
--------------------------------------------------------------------------------
|                  TO Level of QPSK / Digital Modulator (Behavioral)           |
--------------------------------------------------------------------------------

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;


        entity QPSK_MOD is
                port ( Master_clk    : in   std_logic;
                       Div_output    : out  std_logic;
                       PN_output     : out  std_logic;
                       I_Q           : out  std_logic_vector( 1 downto 0 );
                       qpsk_out      : out std_logic);
         end QPSK_MOD;

  architecture structural of  QPSK_MOD is

        component  Freq_div
              port ( D_in             : in  std_logic;
              Div_out                 : buffer std_logic);
        end component;

        component PN_gn
              port ( Din_div          : in std_logic;
                     PN_out           : buffer std_logic);
        end component;

        component mux4to_1
              port ( A0,B90,C180,D270   :IN   STD_LOGIC ;
                     s                  :IN   STD_LOGIC_VECTOR (1 DOWNTO 0);
                     Mux_out            :OUT STD_LOGIC );
               end component;

        component carrier_shifter
              port ( Carrier_in         : in      std_logic;
                     I0 ,I90            : buffer  std_logic;
                     I180 , I270        : buffer  std_logic);
             end component;

       component QPSK_map
              port ( Din_PN             : in  std_logic;
                     Q                  : buffer  std_logic_vector( 1 downto 0 ));
              end component;

     signal  SC0 , SC1 , SC2 , SC3 , SC4 , SC5 , SC6 ,SC7 , SC8 , SC9   : std_logic;
```

```
    begin
        U1 : Freq_div         port map ( D_in => Master_clk , Div_out => SC0 );
        U2 : PN_gn            port map ( Din_div => SC0 , PN_out => SC1 );
        U3 : QPSK_map         port map ( Din_PN => SC1 , Q(0) => SC8 , Q(1) => SC9 );
        U4 : carrier_shifter  port map ( Carrier_in =>Master_clk, I0 => SC4 , I90 => SC5 , I180
                                         => SC6 , I270 => SC7 );
        U5 : mux4to_1         port map ( A0 => SC4 , B90 => SC5 , C180 => SC6 , D270 => SC7 ,
                                         Mux_out => qpsk_out , s(0) => SC8 , s(1)=> SC9);


                    Div_output <= SC0;
                    PN_output  <= SC1;
                    I_Q(0)     <= SC8;
                    I_Q(1)     <= SC9;
 end structural;
```

| VHDL code for the Multiplexer |

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

        ENTITY mux4to_1 IS                          ---------- Top Level of Multiplexer 4 to 1

            PORT ( A0,B90,C180,D270   :IN   STD_LOGIC ;
                   s                  :IN   STD_LOGIC_VECTOR (1 DOWNTO 0);
                 Mux_out              :OUT STD_LOGIC );
          END mux4to_1;
 ARCHITECTURE  multiplexer4x1 OF mux4to_1 IS

    BEGIN
          PROCESS (s,A0,B90,C180,D270)
    BEGIN
          CASE s IS

                      WHEN "00"        =>   Mux_out  <= A0;
                      WHEN "01"        =>   Mux_out  <= B90;
                      WHEN "10"        =>   Mux_out  <= C180;
                      WHEN  OTHERS =>   Mux_out  <= D270;

          END CASE ;
    END PROCESS;
END multiplexer4x1;
```

VHDL code for the frequency divider at 2 MHz

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

        entity  Freq_div is
              port ( D_in          : in     std_logic;
                     Div_out     : buffer std_logic);
        end Freq_div;

  architecture behavior of Freq_div is

              signal count_2mhz           : std_logic_vector(4 downto 0 );
              signal clock_2mhz_int       : std_logic;

        begin
               process
        begin
              wait until D_in'event and D_in  = '1'
              if count_2mhz < 6 then
              count_2mhz <= count_2mhz + 1;
       else
              count_2mhz <= "00000" ;
       end if ;
              if  count_2mhz < 3 then
              clock_2mhz_int <= '0';
       else
              clock_2mhz_int <= '1';
   end if;
 end process ;
             Div_out  <= clock_2mhz_int ;
end behavior;
```

VHDL code for the Data Mapping

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

           entity  QPSK_map is
              port( Din_PN       : in  std_logic;
                    Q              : out std_logic_vector( 1 downto 0 ));
              end qpsk_map;
```

```
    architecture behaviour of qpsk_map is

            signal tmp : std_logic_vector (1 downto 0 );

        begin
            process (Din_PN)
        begin
            if (Din_PN'event and Din_PN= '1' ) then
            tmp  <= tmp + 1 ;
       end if;
  end process;
            Q <= tmp;
end behaviour;
```

| VHDL code for the Carrier phase shifter |

```
library ieee;
use ieee.std_logic_1164.all;

      entity carrier_shifter is
            port ( Carrier_in     : in     bit;
                   I0 ,I90        : inout  bit;
                   I180 , I270    : inout  bit);
      end carrier_shifter;

architecture structural of carrier_shifter is

      component NOT1
           port ( A   : in  bit ;
                  X     : out bit );
      end component;

     component my_dff1
           port ( d , clk  : in     bit ;
                  q        : inout  bit);
           end component;
 ----------------------------------declaration of the signal used to interconnected ----------------------------

     signal  FF0 , FF0_NOT , FF1 , FF1_NOT , CAR_NOT  : bit;

 begin

      U0 : my_dff1   port map ( clk => Carrier_in , q => FF0 , d => FF0_NOT );
      U1 : NOT1      port map ( A => FF0 , X => FF0_NOT );
      U2 : my_dff1   port map ( clk => CAR_NOT, q => FF1 , d => FF1_NOT );
      U3 : NOT1      port map ( A => FF1 , X => FF1_NOT );
      U4 : NOT1      port map ( A => Carrier_in ,X => CAR_NOT );

         I0    <= FF0;
         I180 <= FF0_NOT;
         I90   <= FF1;
         I270 <= FF1_NOT;

end structural;
```

```
------------------------ Declaration of the component ----------------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.all;
        entity my_dff1 is                                  ----------------------------------DFF  declaration

              port ( d , clk : IN  bit;
                     q       : buffer bit);
       end my_dff1;
architecture Behavior of my_dff1 is
  begin
        process( d , clk)
  begin
             if (clk'event and clk='1') then
             q <= d;
      end if;
    end process;
 end behavior;

library ieee;                                    ---------------------------Not gate declaration
use ieee.std_logic_1164.all;
    entity NOT1 is
             port( A    : IN   std_logic;
                   X    : OUT  std_logic);
    end NOT1;
architecture behavioral of NOT1 is

    begin
             X <= not A ;
end behavioral;
```

The modulator has been programmed with the VHDL code for generates the QPSK digital signal as shown in the Figure (B1.12). Where the each part of modulator has simulated individually, the carrier simulation has demonstrated in the Figure (B4.13), which are generates four different outputs in the same frequency but with different phases (0º, 90º, 180º, 270º). However, the multiplier has illustrated in the Figure (B1.24), where the frequency divider has shown in Figure (B1.15). Eventually, the PN sequence code generator and the data mapping are demonstrated in the Figure (B1.16) and (B1.17) respectively.

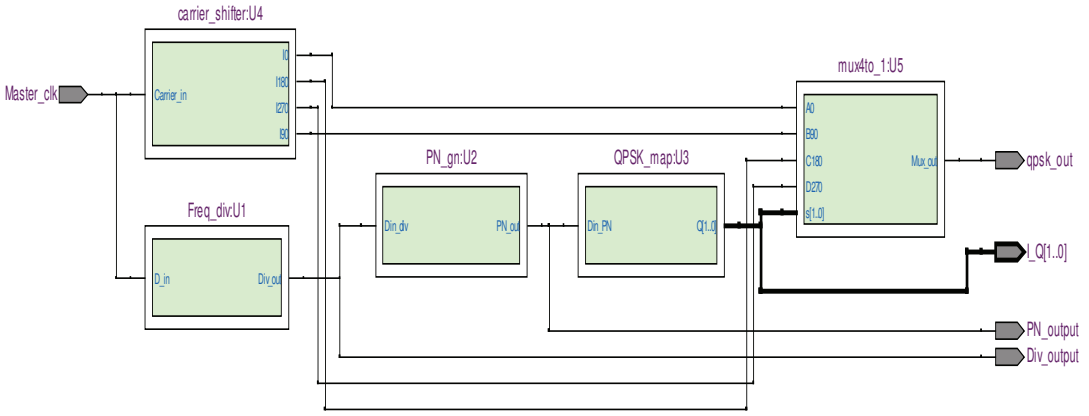


Figure (B1.12) the simulation behavioral for QPSK modulator

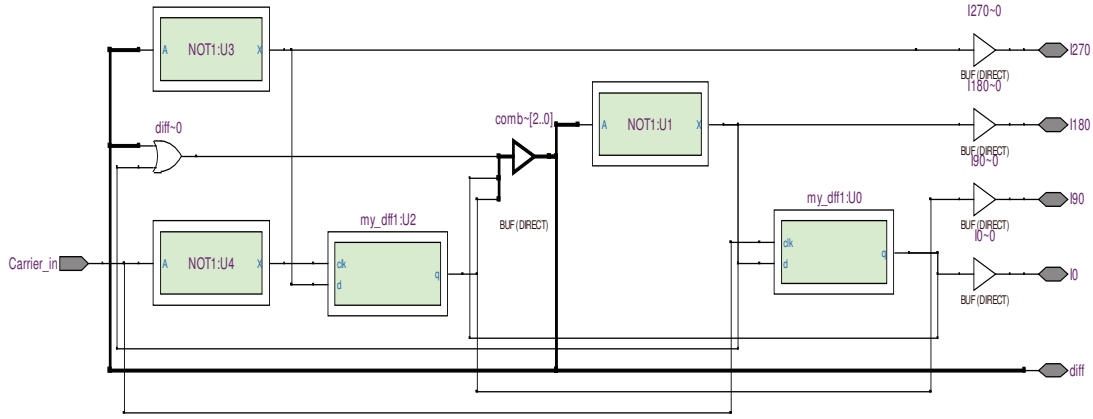


Figure (B1.13) the simulation behavioral code for carrier phase shifter

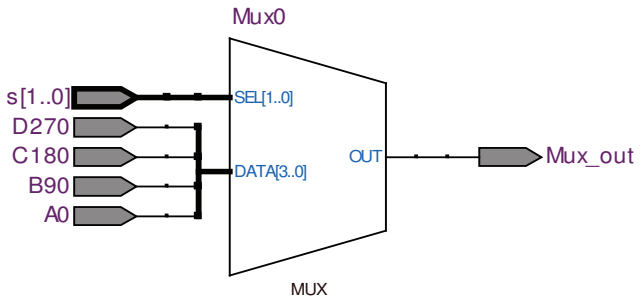


Figure (B1.14) the simulation behavioral of multiplexer (4 to 1)

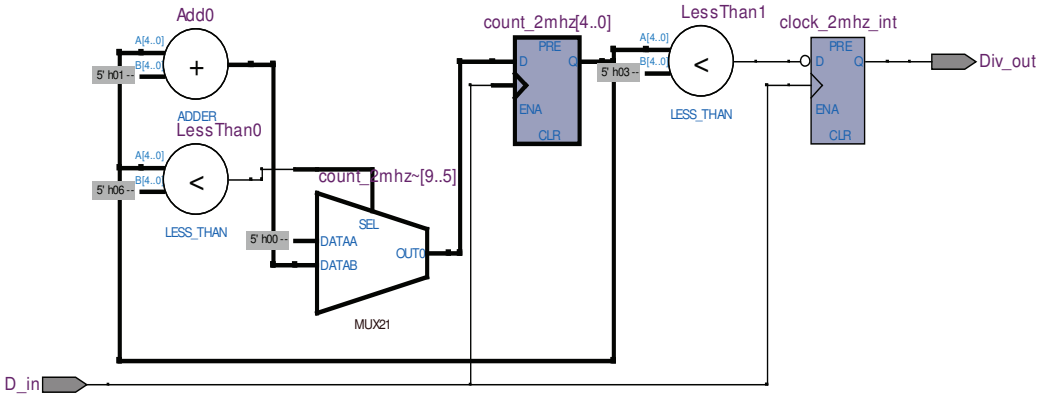


Figure (B1.15) the simulation behavioral for the frequency divider

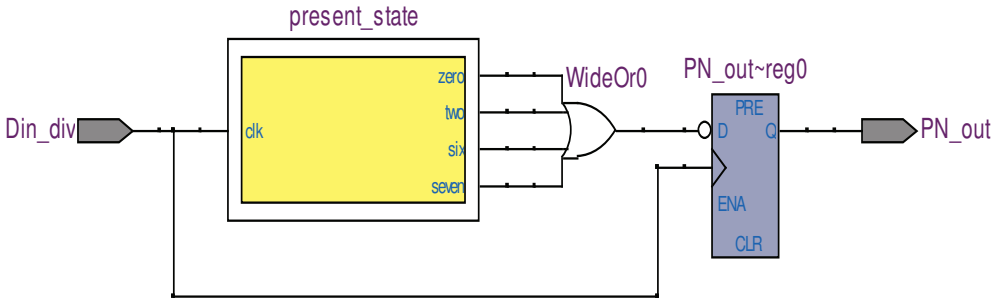


Figure (B1.16) the simulation behavioral of the PN –code sequence generator

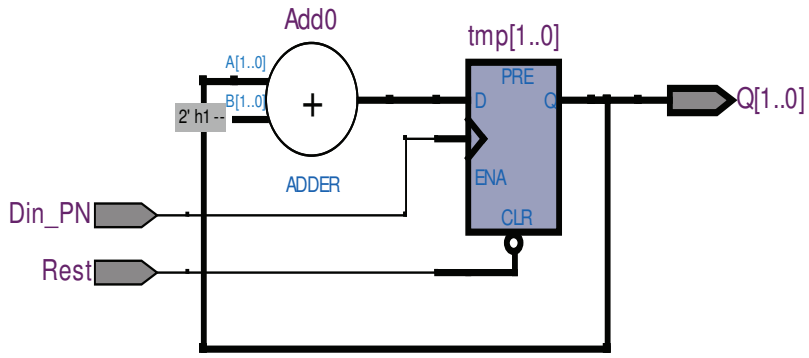


Figure (B1.17) the simulation behavioral of the data mapping for generates I/Q

End of the QPSK Modulator

The last modulator has been designed it is the 8-PSK modulator, which is synthesized the modulator by generates the VHDL programming code. It is also was designed with two methods structural and behavioral, the behavioral version is the more efficient one for this modulator.

```
-------------------------------------------------------------------------------------------------------------
|                        The Top Level of 8-PSK / Digital Modulator (Behavioral)                            |
-------------------------------------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
        entity Carrier_8Phaser is
            port ( Carrier_in                  : in   std_logic;
                   A0,A180 , A45 , A225        : out  std_logic;
                   A90,A270 ,A135, A315        : out  std_logic);
        end Carrier_8Phaser;
architecture structural of Carrier_8Phaser is
        component my_NOT1                              ---------- Component declaration
            port ( A      : in std_logic ;
                   X      : out std_logic );
        end component;
        component my_df
            port ( d , clk      : in     std_logic ;
                   q            : out    std_logic);
        end component;
 ---------------------- Declaration of the signal used to interconnected ------------------------------
   signal  FF0, FF0_NOT, FF1, FF1_NOT, FF2 , FF2_NOT, FF3, FF3_NOT : std_logic;
   begin
            U0 : my_df        port map  ( clk => Carrier_in , q => FF0 , d => FF1 );
            U1 : my_NOT1      port map  ( A => FF0 , X => FF0_NOT );
            U2 : my_df        port map  ( clk => Carrier_in,  q => FF1 , d => FF2 );
            U3 : my_NOT1      port map  ( A => FF1 , X => FF1_NOT );
            U4 : my_df        port map  ( clk => Carrier_in, q => FF2 , d => FF3  );
            U5 : my_NOT1      port map  ( A => FF2 , X => FF2_NOT );
            U6 : my_df        port map  ( clk => Carrier_in ,q => FF3,  d => FF0_NOT );
            U7 : my_NOT1      port map   ( A => FF3 , X => FF3_NOT );
     A0    <= FF0;
     A180 <= FF0_NOT;
     A45   <= FF1;
     A225  <= FF1_NOT;
     A90    <= FF2;
     A270  <= FF2_NOT;
     A135 <= FF3;
     A315 <= FF3_NOT;
 end structural;
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

        entity my_df is                                  ---------- DFF1 declaration
              port ( d , clk    : in     std_logic;
                     q          : out    std_logic);
        end my_df;

 architecture Behavior of my_df is

   begin
          process( d , clk )
   begin
          if (clk'event and clk='1') then
          q <= d;
     end if;
  end process;
end behavior;

library ieee;
use ieee.std_logic_1164.all;

         entity my_NOT1 is                               ---------- NOT Declaration
               port( A    : in   std_logic;
                     X    : OUT  std_logic);
         end my_NOT1;

 architecture behavioral of my_NOT1 is

        begin
              X <= not A ;
end behavioral;
```

| The VHDL code for carrier |

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

      entity counter is
            Port ( CLOCK          : in  STD_LOGIC;
                   DIRECTION      : in  STD_LOGIC;
                   COUNT_OUT : out  STD_LOGIC_VECTOR (2 downto 0));
      end counter;
```

```
architecture Behavioral of counter is
        signal count_int : std_logic_vector (2 downto 0) := "000";
     begin
              process (CLOCK)
       begin
             if CLOCK ='1' and CLOCK'event then
            if direction='1' then
            count_int <= count_int + 1;
  else
           count_int <= count_int - 1;
    end if;
  end if;
end process;
            COUNT_OUT <= count_int;
end Behavioral;
```

| VHDL code for the multiplexer (8 to 1) |

```
IBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
          ENTITY mux8to_1 IS                          ---------- Top Level Of Multiplexer 4 to 1
               PORT ( A0, A45,A90 , A135, A180,
                        A225, A270, A315          :IN   STD_LOGIC ;
                        s                          :IN   STD_LOGIC_VECTOR (2 DOWNTO 0);
                    Mux_out                       : OUT STD_LOGIC );
          END mux8to_1;
 ARCHITECTURE  multiplexer8x1 OF mux8to_1 IS
          BEGIN
                PROCESS (s,A0, A45, A90, A135, A180, A225, A270, A315)
          BEGIN
         CASE s IS
                          WHEN "000" =>   Mux_out  <= A0;
                         WHEN "001" =>   Mux_out  <= A45;
                         WHEN "010" =>   Mux_out  <= A90;
                         WHEN "011" =>   Mux_out  <= A135;
                         WHEN "100" =>   Mux_out  <= A180;
                         WHEN "101" =>   Mux_out  <= A225;
                         WHEN "110" =>   Mux_out  <= A270;
                         WHEN  OTHERS=>   Mux_out  <= A315;
          END CASE ;
   END PROCESS;
END  multiplexer8x1;
```

The above modulator was programmed with the VHDL code for generates the 8PSK digital signal was presented in the simulation code results in Figure (B1.18), where each part of the modulator has been simulated individually. However the PN-sequence code generator has illustrated in Figure (B1.19), where the frequency divider is depicted in the previous simulation. Whilst the carriers phase shifter simulation is shown in the Figure (B1.20). Ultimately, the multiplexer and the data mapping are demonstrated in the Figure (B1.21) and Figure (B1.22) respectively.

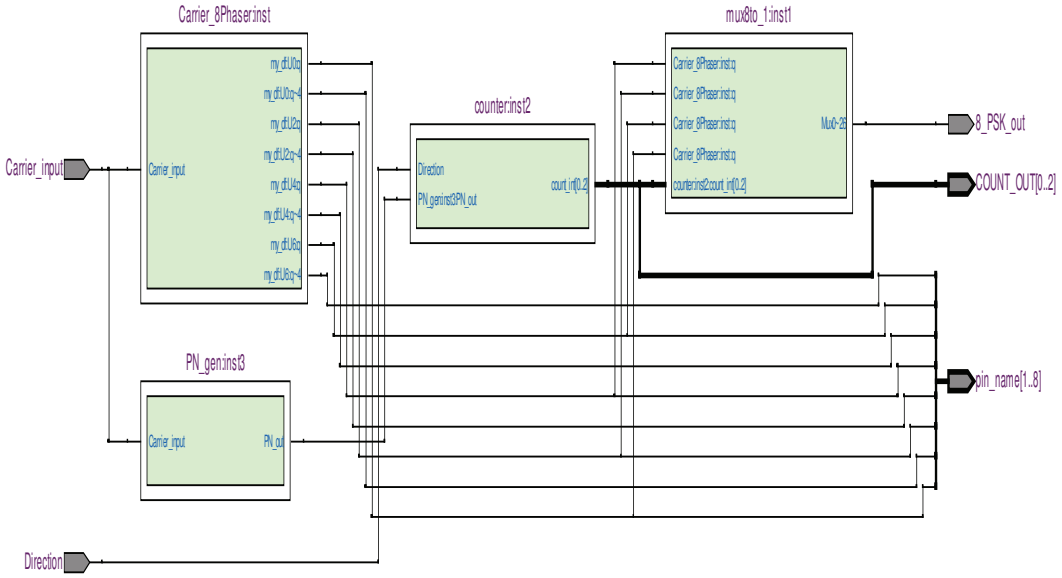


Figure (B1.18) the block diagram of the Behavioral the 8-PSK modulator

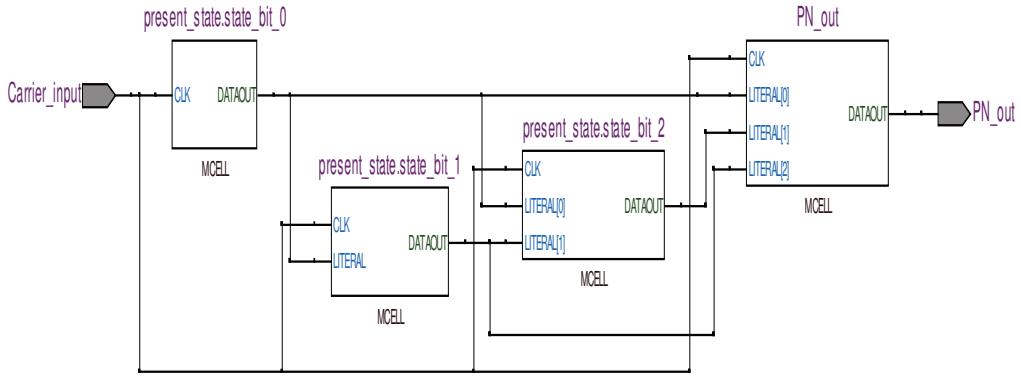


Figure (B1.19) the block diagram of the Behavioral the PN- code generator

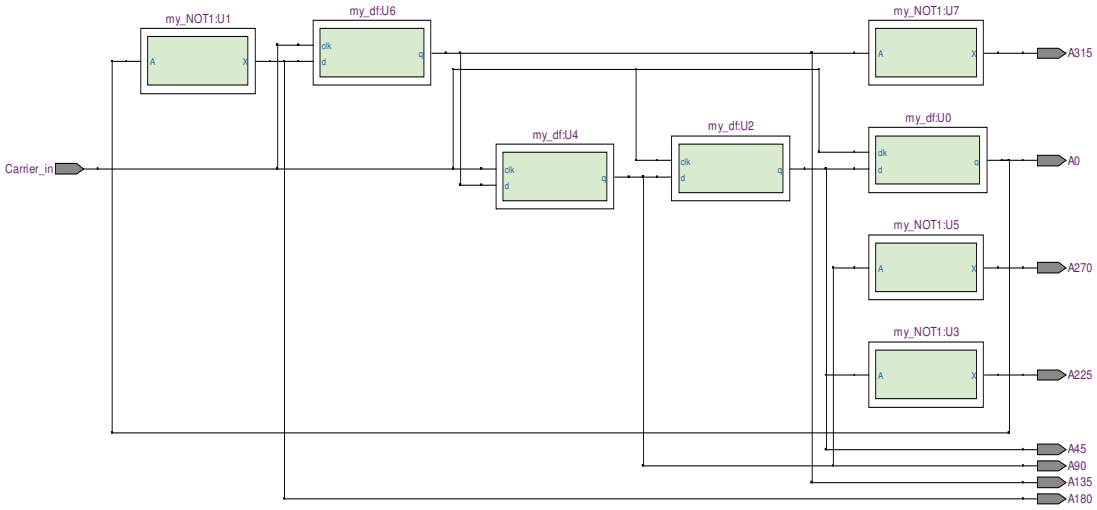


Figure (B1.20) the simulation behavioral of the carrier phase shifter

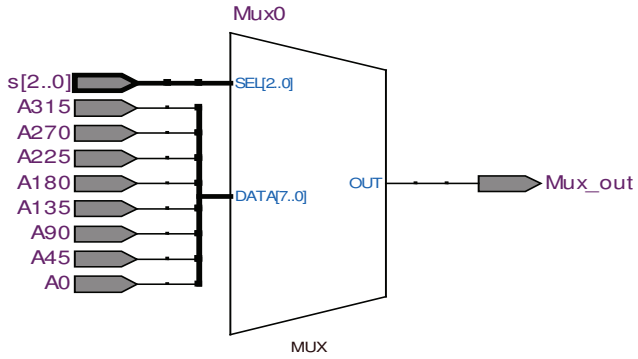


Figure (B1.21) the simulation behavioral of the multiplexer for (8 to 1)

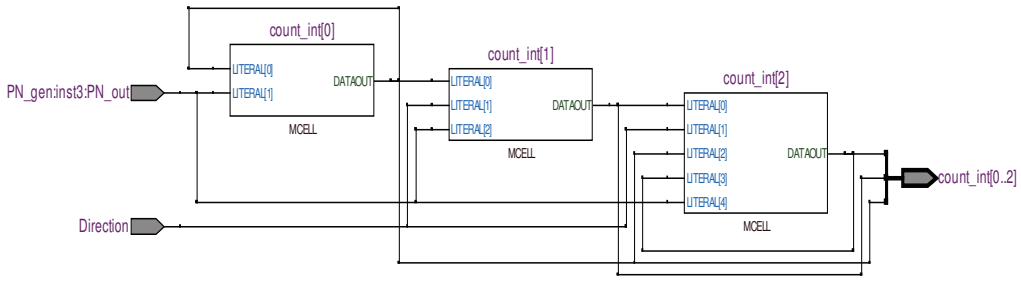


Figure (B1.22) the simulation behavioral for the data mapping

End of the 8PSK Modualtor

Appendix

C

Extra Hardware Implementation

Appendix - C

3. PN Code Generator Topologies:

The data source is generates a PN-sequence to transmitting a modulated random binary data over the inductive coupling link for test purposes. There are different topologies to implement the PN-sequence in circuit design, or generates as programmed code. The practical circuit was designed as shown in Figure (C1.0). The board generates five different codes as (1.70kbps, 390kbp, 90kbps, and 3Mbps); the waveform of the test circuit is demonstrated in Figure (C1.1).

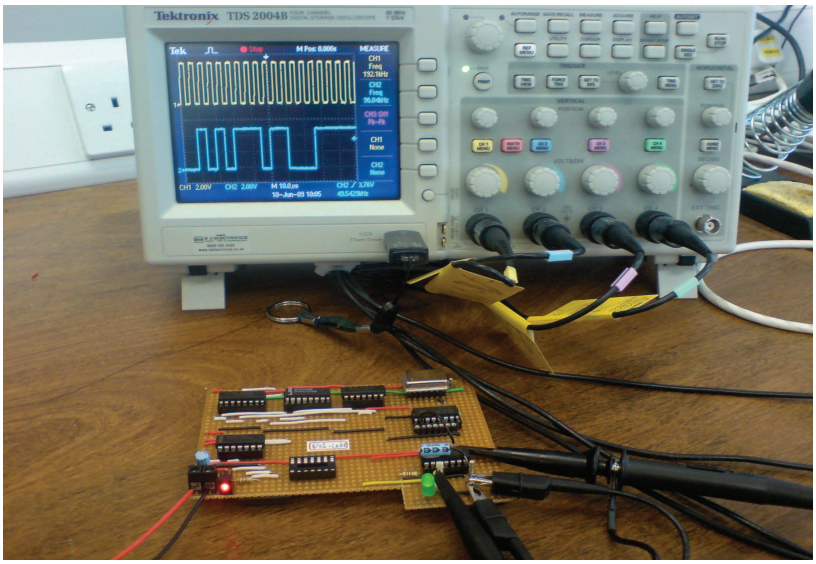


Figure (C1.0) shown the PN sequence generator circuit

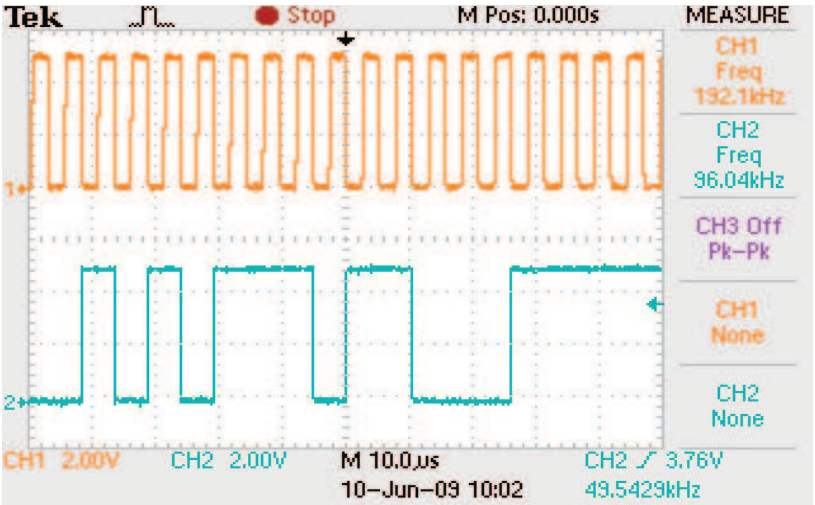


Figure (C1.1) the PN sequence waveform output (CH2)

3.1 The Proposed Implant Digital Modulators (TX/Rx)

The investigation was to improve the efficiency performance of the implant device, that for reduce the device size of the implant and the power consumption of the electronics circuits. The proposed full digital modulators are synthesized in programming code in VHDL the demodulator was redesigned by modified and replaced the ASK demodulator with a full digital demodulator that were synthesized in CPLD. Generally, the analogue RF received signal is converted into a digital form, and the output signal from the converter circuit is demodulated with the VHDL digital BPSK demodulator. The block diagram of our proposed VHDL digital modulators are demonstrated in Figure (C1.2), the second proposed RF design converter circuit as second solution for higher frequency.

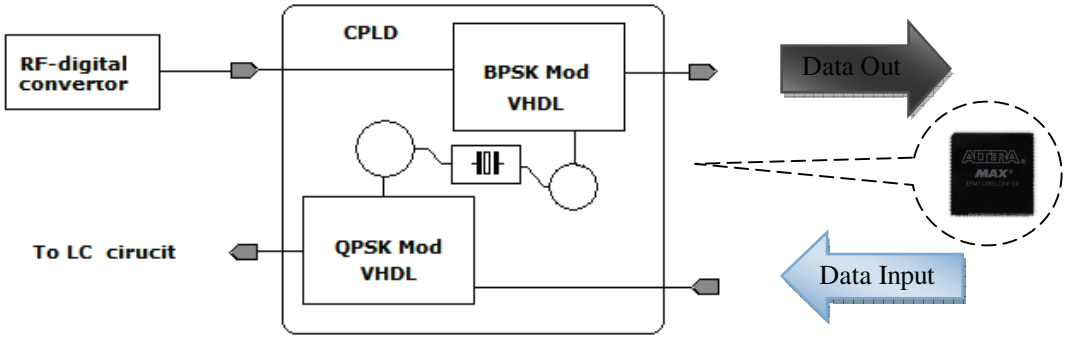


Figure (C1.2) the proposed full digital modulators at the implant device

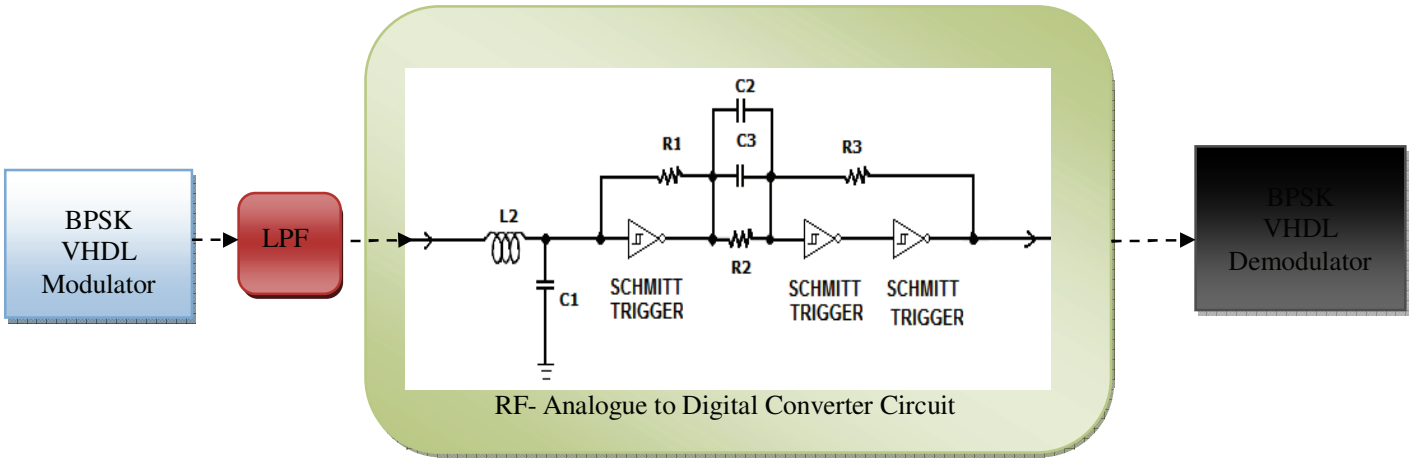


Figure (C1.3) illustrated the second proposed RF-digital circuit converter

The synthesized modulator and demodulator, which are generated by VHDL, code has shown in Figure (C1.4). However, the proposed BPSK demodulator and QPSK modulator are working as discussed in chapter four.

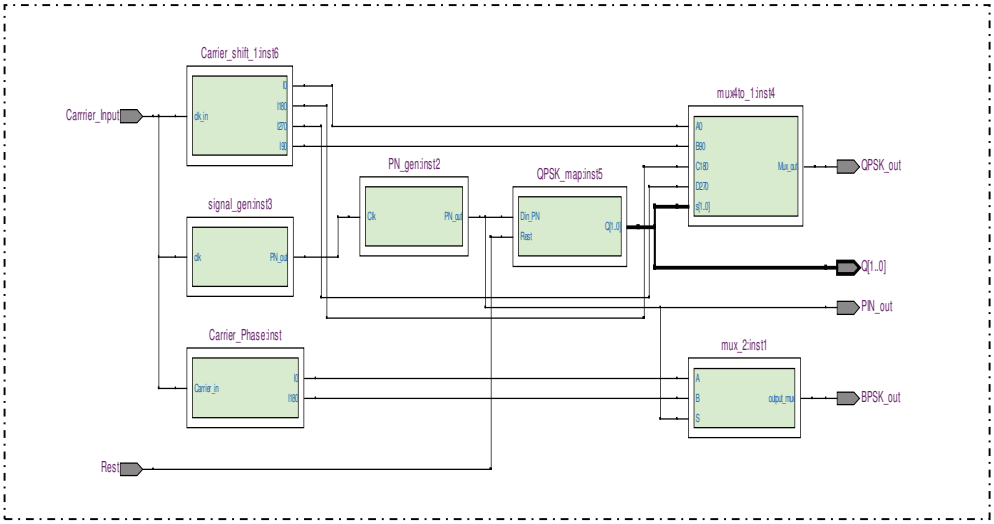


Figure (C1.4) the BPSK/ QPSK modulator/demodulator generated by VHDL

3.2 Wireless Transmission Investigation for High Data

3.2.1 Background

The transcutaneous wireless telemetry devices are rising to use higher frequencies up to the microwave region. That needs to design antennas to works in the implant device and matching the electronics device. Typically, the objective of any such antenna must be to maximize the transfer power from and out the body, this required careful design to match the antenna working in ISM band [138]. The frequency investigated in this research is 402 MHz; the consideration for design the antenna is the type of antenna: the size. Generally, the better type of antenna is a directional antenna as appropriate for biomedical applications, because they had advantage as a fewer disturbances to the radiation pattern and to the return loss. However, compared to omni-directional antenna it should be avoided to use in the implant device. Most of the new telemetry system is developed in order to be fitted with the common characteristic of future a higher performance radio powered implantable stimulators. These required transmitting higher data rate to control the large number of electrode arrays, and accurate definition enough power.

The prototype developed allows demodulating and decoding the information coming though the wireless transcutaneous link with data rates from 1.30 Mbps up to 4.46 Mbps. The proposed PCB antennas have the goal to provide UHF band as an alternative to accomplish a good compact RF system design, the PCB antenna is intended for 310 to 420MHz frequency of operation. Practically, the parameters for design UHF antenna (tracking loop antenna) are demonstrated in Figure (C1.5).

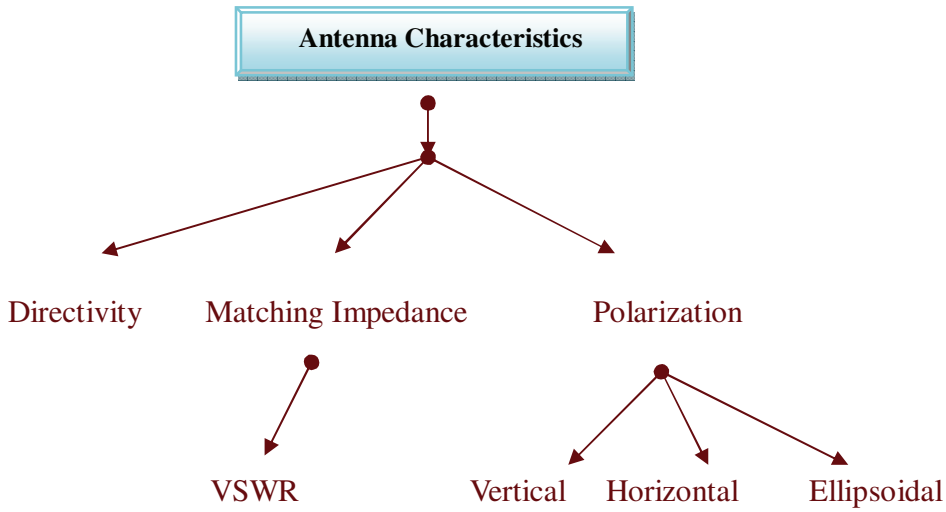


Figure (C1.5) demonstrate the parameters for coil antenna design at UHF

Conceptually, in biomedical purpose there are gaining acceptances for using 2.4GHz, originally developed for RFID applications [126] [58]. This band of frequencies needs practical antenna mostly designed as track or in printed board, which needs in design to consider the above parameters. Undeniably, the biodevices are still critical to design in UHF the band, as the power consumption is most important for implant devices. In addition, the modulator and PA are the hungry elements in implant device. However, we demonstrate in Figure (C1.6) below our UHF investigation solution over ISM band for short-range communication. In modern wireless technique using the direct modulation can reduce the transmitter size and power, in addition the local oscillator is a key element for efficient modulator design, and many investigations carry on for robust and appropriate design for implantable devices [59] [71]. The second modified solution using direct modulation technique, with VHDL modulator has shown in Figure (C1.7)

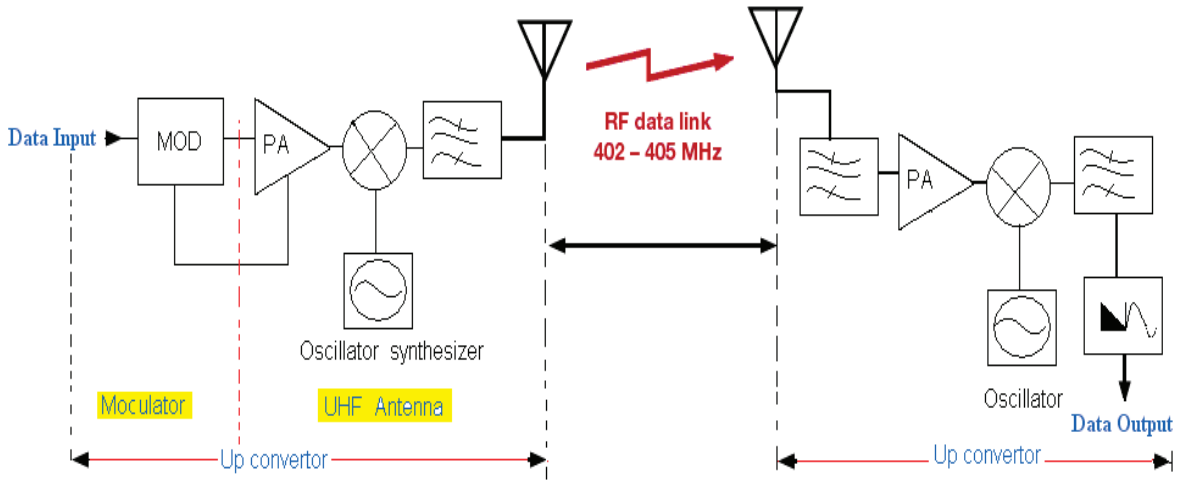


Figure (C1.6) the transceiver solution with UHF solution

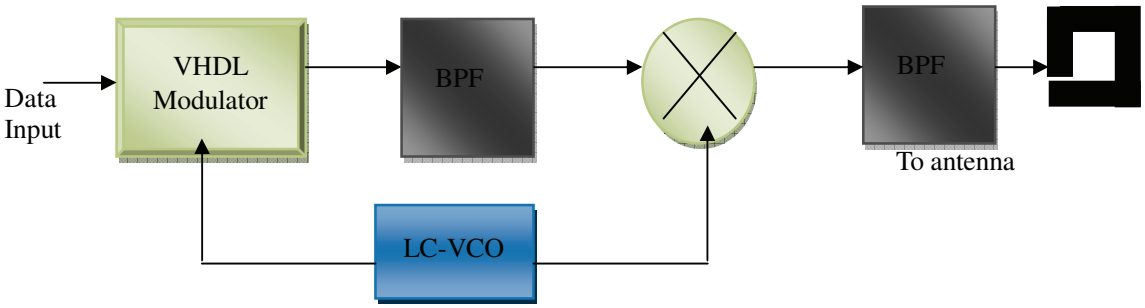


Figure (C1.7) Modified solution for a direct modulation with UHF at implant device

3.4.2 Design Of UHF antenna for biomedical purpose

3.4.2.1 RF-Spiral Inductor Design Methodology

The spiral square inductor is the most common applied in RFID, so the target in our project is to design a 150nH spiral square inductor with 10-quality factor **Q.** To achieve the quality factor of the spiral coil it is necessary to study the materials that form the substrate. Principally, the geometry of the spiral coil deign has been demonstrated in Figure (C1.8). However, to evaluate the inductance of the planar spiral square coil it can be calculated according to the Green's theorem [136] [103], that can be defined in the equation for self-coil for a straight conductor as:

$$L = 0.0021\left[\ln\left(\frac{21}{GMD}\right) - 1.25 + \frac{AMD}{l} + \left(\frac{\mu}{4}\right)T\right] \qquad (1.0)$$

Where **L** is the self-inductance in (μH), ***l*** is the coil length in cm; GMD and AMD represent the geometric and arithmetic mean distance, of the conductor cross section respectively. T is the frequency correction parameter. Generally, we used the top layer of metal of the spiral coil, it is a thin film inductor with rectangular cross section, and the equation (2.0) can be modified as;

$$L = 0.0021\left[\ln\left(\frac{21}{a+b}\right) + 0.50049 + \left(\frac{a+b}{3l}\right)\right] \tag{2.0}$$

In addition, there are many simplified formulas, which can be considered for design of spiral-integrated coils such as micro strip antennas. If we denotes the width and l the length of the coil, while b and h refer to the width and the height of its cross-section, C is equal to C = w + l + 2h in equation (3.0).

$$L = \frac{0.0276.(CN)^2}{1.908C + 9b + 10h}\ (\mu H) \tag{3.0}$$

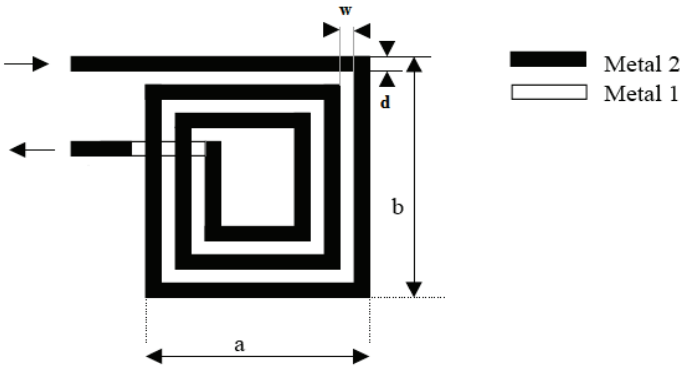


Figure (C1.8) the geometry of a typical rectangular spiral coil

3.4.2.2 Proposed Transmitter and Receiver coils Antenna design

The schematic of the miniature square spiral inductor antenna has shown Figure (C1.9). The strips and separation or the gap widths indicated as ***W*** and ***G***, respectively. The outer dimensions of the inductor are about 10×10 mm, the above dimensions typical appropriate for implantable devices. The frequency range is operating in the range 200 to 700 MHz to facilitate the characterization using signal-ground RF probe; a short length of coplanar strip line (CPS) excites the inductors [198]. In Figure (C1.10) is shown the loop trace of a typical inductor as antenna on PCB. It defended, as the loop track inductance and the quality factor are dependent on the strip and separation or gap dimensions.

In addition, elevation inductor by introducing an insulating layer such as spin-on glass (SOG) could improves the performance [205]. Hence, to carry out the parametric study several inductors with strip and gap dimensions in the range of 10 to 15µm. In this thesis, we synthesized different types of implant antennas for biomedical purpose, that are shown in Figures (C1.9) first, the second Figure (C1.10) and third Figure (C1.11) geometries of our proposed for UHF and power spiral coil design respectively.

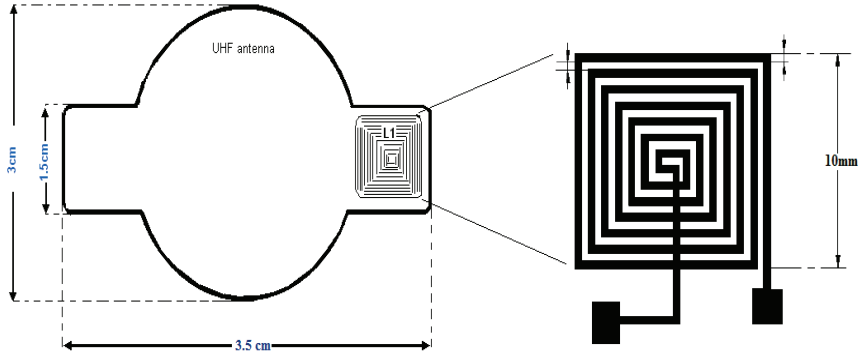


Figure (C1.9) geometry of the typical rectangular spiral coil for implant device [205]

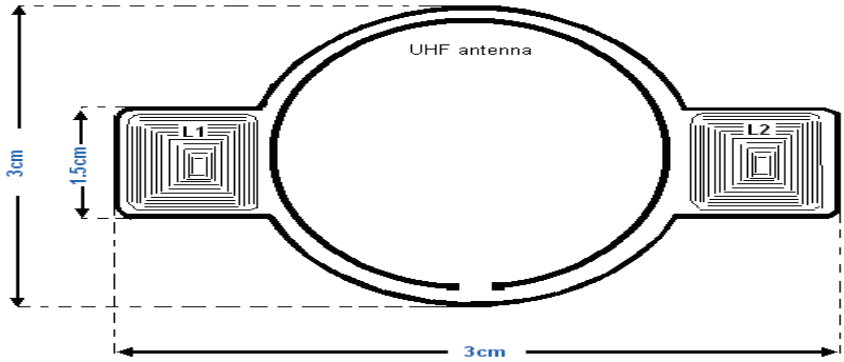


Figure (C1.10) our first proposed geometry design for UHF and power spiral coils

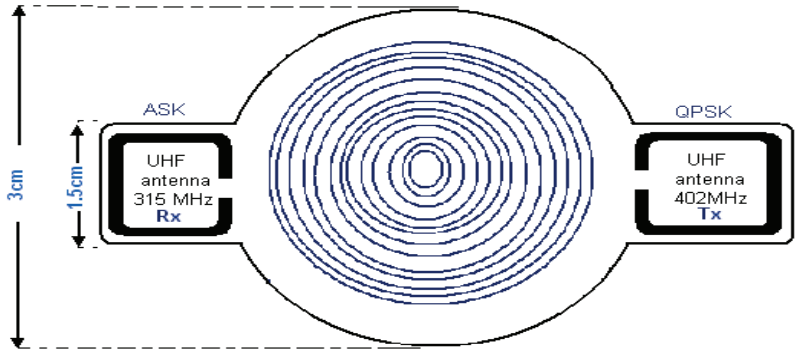


Figure (C1.11) the second proposed geometry of UHF antenna with power spiral coil

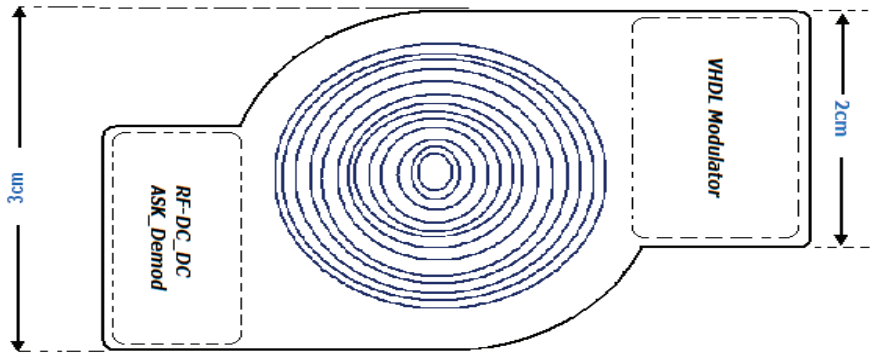


Figure (C1.12) the third proposed geometry of UHF antenna with power spiral coil

3.4.3.3 Reader Dipole Antenna Design

The dipole antenna is the appropriate design work in the reader part as a receiver for UHF frequency. As alternative, to accomplish a good compact RF system design the PCB antenna is intended for the band 310 to 420MHz. The proposed PCB antennas have the goal to provide UHF band operation; it resembles a dipole antenna characteristic behavior. That is similar to a real one and it can detune by proximity to conductive objects like metal, human body, etc. The fabricated performance of it may vary slightly due to process different from one PCB house to another (dielectric material). The dipole impedance is capacitive in nature with resonance frequency at approximately 650MHz. However, the Table (C1.0) illustrates the matching impedance of the most used frequencies from 300 to 450MHz. For matching the load impedance at 50Ω or other impedance value, a shunt inductor from the feeding point to ground and a series capacitor from the feed point to the RF circuit are needed as shown in Figure (C1.13) (the values needed for the 6th frequencies most used). The corrected or modified impedance after the antenna is matched as seen from RF circuit.

Frequency (MHz)	Z antenna(Ω)	Z matched(Ω)	C(pF)	L(nH)
303	10.5 - j235	41 - j27	1.2	82
315	11.2- j216.1	2.3 – j44.3	1.2	75
345	11 – j196.5	49.5 – j32	1.2	62
390	9.2 – j153.8	42 – j13.5	1.2	43
418	8.4 - j134.7	45 – j9.5	1.2	36

Table1 (C1.0) Dipole Antenna impedance and Retuned Impedance with LC circuit with matching values

Generally, the matching impedance is critical in order to get lowest ***VSWR*** and optimum transmitted power with less reflection to the source [212]. The ***VSWR*** is determining the amount

of energy, which is not converted by the antenna into radiated energy. The antenna can be either radiating the energy (desired), or turn it in heat is (undesired). This parameter can be calculated in the formula in equation (4.0).

$$SWR = \frac{(1+|\rho|}{(1-|\rho|} \tag{4.0}$$

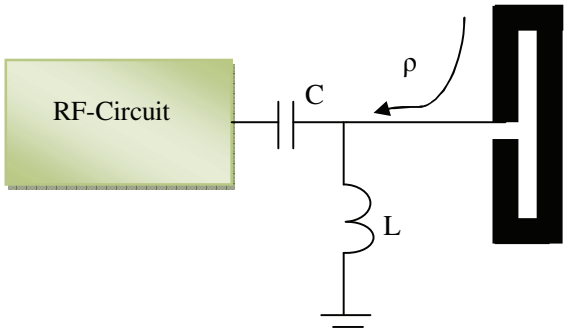


Figure (C1.13) Addition of Shunt capacitor for matching Antenna

The desired inductive loop or loop antennas in biomedical design need often to consider the quality factor and perform in minimum size. However, the disadvantages of these techniques are the unused area behind the antenna track 'ground plane area, which affects the PCB antenna performance and detuned the carrier frequency. Typically, this reduces the implant device efficiency when working in UHF and using the micro strip antenna to transmits the data from implant device into reader unit. In addition, the higher frequency used it increases the parasitic capacitance and the interference could disturb the transmitting of information if designed under the PCB antenna. Consequently, to use this work as a practical solution, it may be necessary to update our work in future for specific applications.

3.4.3.2 Convert the RF signal to digital signal

For working with digital circuits in high or low frequencies it essential to convert the analogue signal into digital form. In our situation, typically we use the CPLD for synthesized modulator and demodulator, which required the analogue RF signal to be converted into a digital signal for processing it in a CPLD chip. Obviously, the circuit size design and power consumption is critical inside the implant devices. Working with different circuits proposed designs for considering the carrier frequency and limited components for processing the analogue signal especially at implant part. The first proposed design is demonstrated in Figure (C1.14), in

the block diagram to illustrate the Simple process essential to convert the analogue modulated received signal, which uses single rectifiers for positive and negative transitions. The Schmitt triggers convert signals and combine them to provide digital signals. The second proposed design is shown in Figure (C1.15), which modifies the first design for higher frequency.

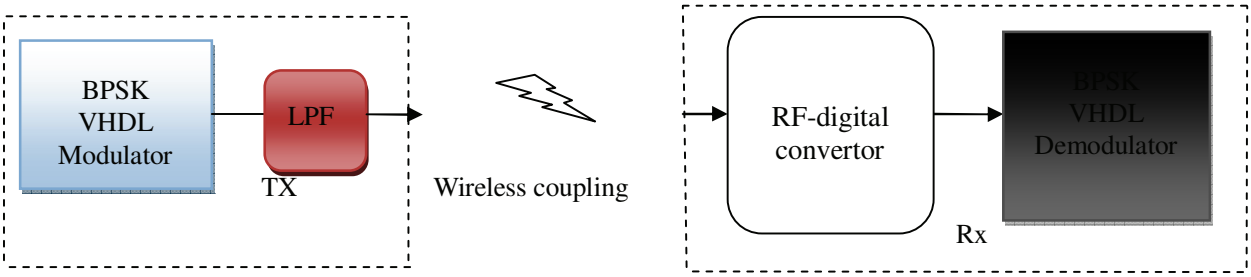


Figure (C1.14) the proposed block diagram of RF-digital convertor

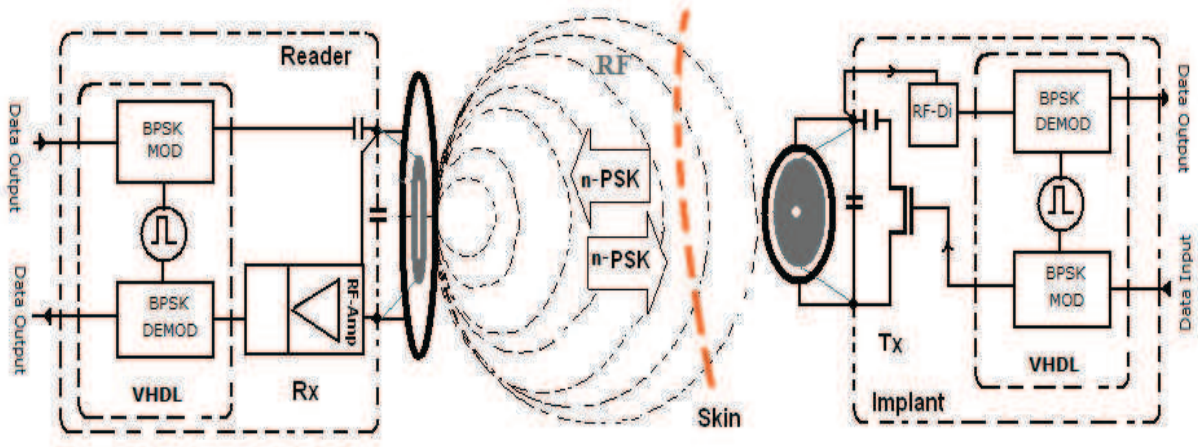


Figure (C1.15) the proposed completed block diagram of RF-digital convertor

5.3 New Methods for Automatic Control Frequency for the Class Power Amplifier

In practice, there are many methods for controlling and adjust the carrier frequency; our goal is to mentoring and controlling the transmitter carrier frequency by the power amplifier. The advantages of this technique which is offer a high transfer wireless power stability that maintains stability of DC voltages at implant device. We investigated another two methods, which can be implemented for monitoring the RF transmitter power, using the feedback control techniques. Obviously, we discussed in the chapter three two methods for this purposes. The first method

was used the VCO techniques we choose the PLL (HEF4046) as a simple implemented control circuit, with the auxiliary circuit for feedback signal. However, this method has been evaluated in hardware, which offers a good performance with class F comparing to class E power amplifier, especially where two coils are too closed. The transmit power and the frequency are affecting in this condition. Respectively, the second practical solution method was investigated with PWM techniques for generates the PWM signal using FPGA. Different methods has been studied for generates Pulse Width Modulation (PWM) in our case programmed by VHDL code. Generally, the proposed design has modified for correct the output PWM signal to perform the duty cycle at 50% at the tuned carrier frequency. This technique has offers a better performance for the suitability of the carrier frequency and the transmitter power amplifier. The main critical point for generates PWM it is the accurate generate frequency at certain value in our case is 135 kHz. We have investigated addition methods for more robust control design which discuses as:

A. Frequency Control System (Fuzzy logic controller -FPGA)

The third method we have proposed for the controller technique has based with fuzzy logic controller for generates a PWM with FPGA or CPLD as shown in Figure (C1.16). The central frequency has chosen in work is the common in all methods which is 135 kHz. This method has been simulated with MATLAB using Fuzzy controller tools for evaluate our work. However, this method has still under investigation for improvement and the implemented in hardware using the FPGA or CPLD.

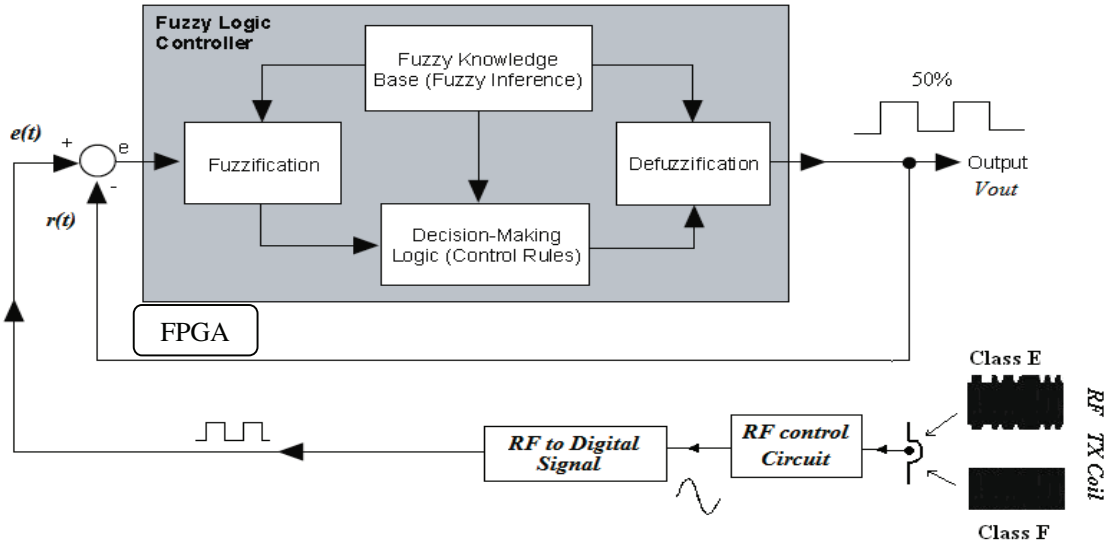


Figure (C1.16) third control method using Fuzzy logic controller

B. Frequency Control System (Microcontroller)

The fourth method to control the transmitter RF signal by using PWM techniques, which used microcontrollers as more flexible tools, whether the programming code use assembly or C languages. In this part, we investigated the PWM technique for controlling the fundamental carrier signal to increase the power efficiency of the system performance. Conversely, different techniques for generates the PWM signal using microcontroller, the application of this facilities in microcontroller for generates the PWM signal it is offers a flexibility for update the data and Auto-correction for the PWM signal. We described the feedback control method for the output pulse transmit signal and monitoring power amplifier Tx signal, modify the design for controller to Auto-correct the fundamental carrier signal that offer stability for Class- E/F power amplifiers. In Figure (C1.17) has shown our proposed feedback control system. The auto-control circuit was introduced for improving the transmitter power toward implant device. That offer stability of transfer the wireless power and provides minimum shifting for the carrier frequency, due to the un-stability of the temperature of the power amplifier. The microcontroller has generates PWM pulse signal at 135 kHz, this TX signal has captured by the loop coil circuit amplified than comparing to the filtered transmitted carrier signal. The microcontroller has converted them into digital to form that for the compactor, the error signal feed back into PWM generator for correct the output.

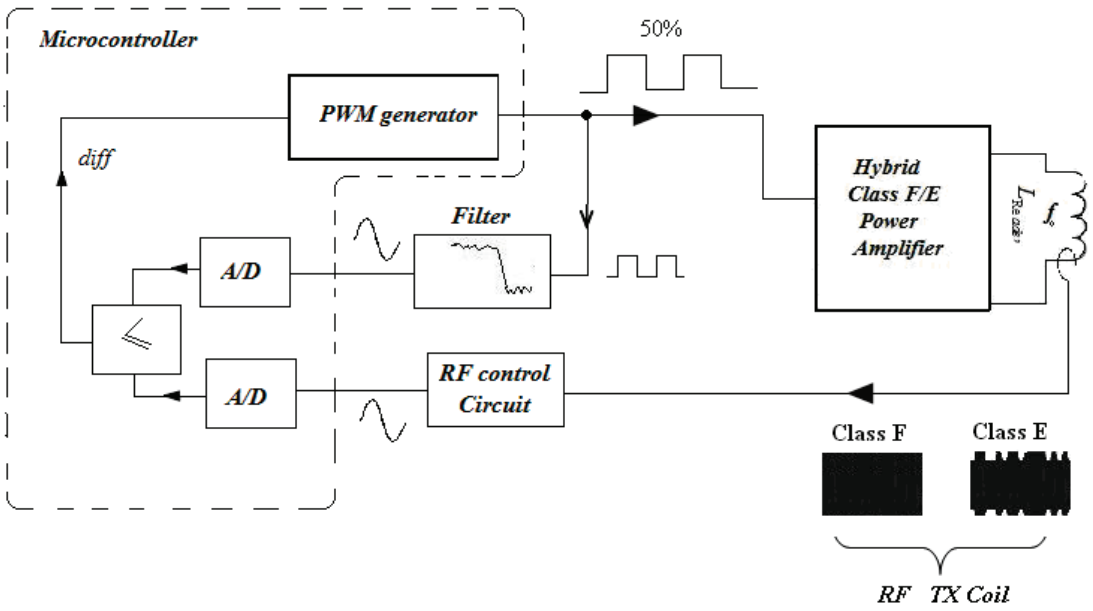


Figure (C1.17) Third method for frequency controller using microcontroller