Voltage and Capacitance Sensing Using Time Comparison

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Abstract

With the rapid advancement of electronic and mechanical system miniaturisation, new application types such as portable systems, internet of things (IoT) and wireless sensor networks (WSNs) have become promising areas of growth for industry. In these areas, the limits on battery life have opened opportunities for energy harvesting to become a commonplace choice as the system power source, which brings its own problems. One of these problems is that energy harvesting is in general a much more variable energy source than batteries and mains power supply, because of the unpredictable and intermittent nature of the external energy environment [1]. This implies that both energy harvesters and the loads they support require significantly more control, tuning and management than if the energy was supplied by traditional means. On the other hand, sensing is also an important aspect for such systems as many of these systems are sensors used to monitor physical parameters in the environment. Another reason is that the control, tuning and management of energy harvesting requires the support of energy/power sensing. It is therefore inevitable that sensing methods need to be developed targeting an environment where energy supply is volatile. However, sensing under a variable energy supply faces numerous problems. One such problem is the energy consumption of the sensing itself. In this regard, the capacitive sensor is widely used for sensing a physical parameter, such as pressure, position, and humidity, as it is suitable for low-power applications with limited energy budgets [2–4]. Another problem faced by sensing under energy supply variability is the difficulty of maintaining stable voltage and/or current references. This thesis is motivated by these issues.

In this thesis, a new sensing method is developed based on time domain techniques, which will be shown to be 1) suitable for capacitive sensing of environmental physical parameters, 2) suitable for sensing voltage, from which power and energy information can be derived, supporting energy harvesting management uses, and 3) robust to voltage and power volatility, making sensors derived from this method useful for miniaturised and energy autonomous systems.

At the centre of this work is a novel reference-free voltage level-crossing sensor, realised through time comparison techniques. By working in the time domain, it avoids the need for voltage or current references. Two more sophisticated sensors are then developed around this level-crossing sensing engine. The first is a voltage monitor which is capable of sensing the crossing of multiple predefined voltage boundaries within a range, targeting energy harvesting system management uses. The second is a capacitance-to-digital converter which senses and converts the value of a target capacitance to digital value. This could be used to support the monitoring of physical parameters in the environment including pressure, temperature, moisture, etc. as these might be made to directly affect the values of capacitances.

This thesis describes detailed design theory and reasoning, implementation, and validation of the presented sensors. Circuits are implemented in very-large-scale integration and investigated in the Cadence Analog Design Environment. In addition to analogue simulations, experiments were also conducted on a fabricated chip. Data collected from these simulation and physical experiments show that the time-domain method developed in this work has quantitative and qualitative advantages over existing designs.

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Chapter 1

Introduction

1.1 Motivation

As Moore's Law predicts, the development of integrated circuit technology has grown exponentially [34, 35]. Advances in these technologies have led to the development of sensor technology [36, 37]. Sensors have transformed from devices that convert simple physical signals to electrical signals into microsystems that incorporate intelligence and complexity, which is known as smart sensor system [5, 38]. Examples include wireless communications, analog-to-digital conversion and power supplies [5, 9, 39, 40]. Typically, a smart sensor system operates in a space of signals and timing. Fig. 1.1 organizes these along the lines of analogue and discrete representation. The first combination is analogue signal analogue time, which pertains to the fully analogue environment a smart sensor works in. The second combination is analogue time discrete signal, which is the sector investigated by this thesis. The third combination is discrete signal discrete time, which is the digital computer world to which a smart sensor interfaces to provide the sensed information. The final combination is analogue signal discrete time, which usually pertains to the output of digital to analogue converters and the intermediate signals in traditional analogue to digital converters.

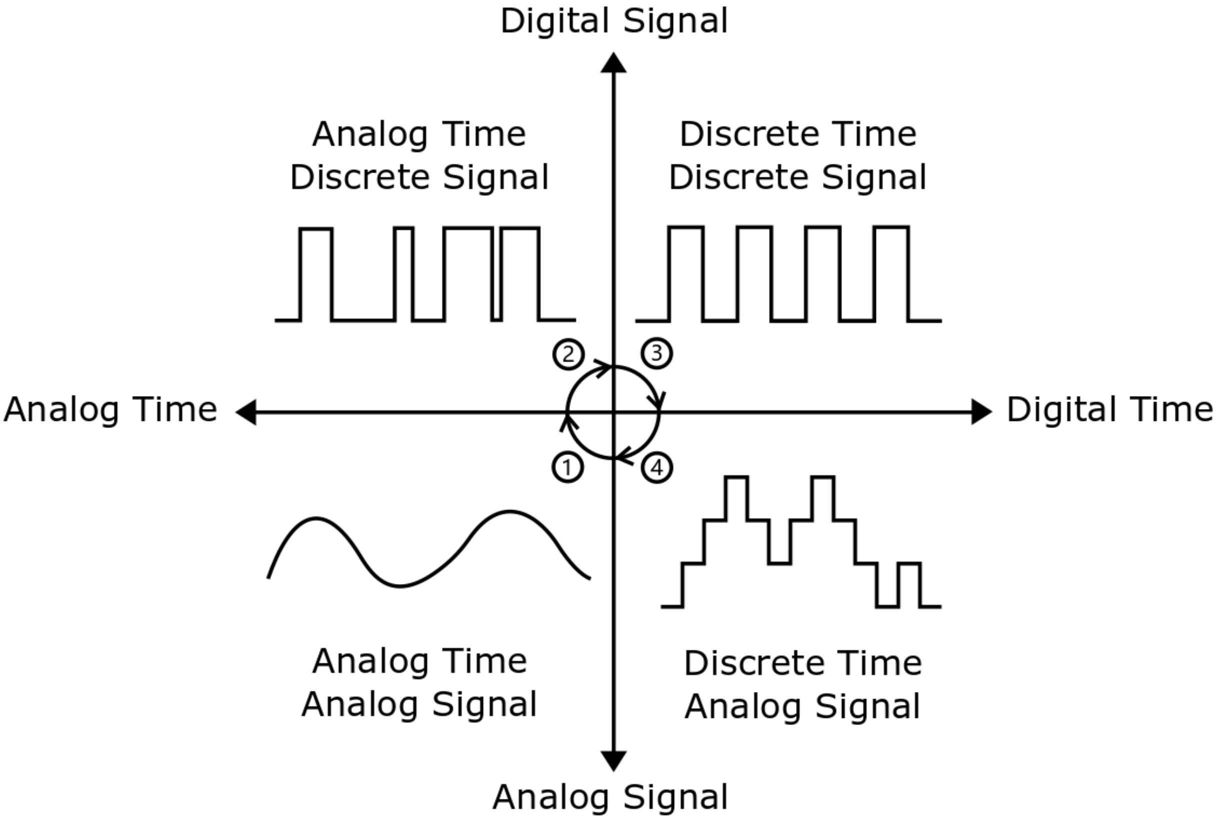


Fig. 1.1 Physical signal conversion from analog domain to digital domain adapted from [5, 6].

This thesis focuses on the domain of discrete signal analogue time, which corresponds with the output of a particular class of analogue to digital conversion. In this sector, the original signal in both analogue value and analogue time, is converted to a digital signal aiming to fit into the digital value digital time domain. In the middle of this conversion, it is possible to choose to move into digital time first and sample the analogue values at precisely spaced time intervals, which is the traditional approach [4, 41–43]. It is also possible to encode the original analogue signal in an analogue time value and produce digital pulses whose time distances represent the analogue value being sensed. This can be done through pulse width modulation, for which although the clock period remains constant, the converted value is encoded in variable (analogue) time (duty cycle length) [41, 44, 45]. Because of the maturity of the pulse width modulation technology, this method is easy to implement with high compatibility to subsequent digital stages [46]. On the other hand, pulse width modulation has poor energy efficiency because of the required constant switching which is not dependent on the input [41, 44, 45, 47]. Pulse frequency modulation encodes the sensed value in the frequency of its output signal, which is a discrete pulse trains of analogue variable pulse to pulse time. It has better energy efficiency in that pulses and switching are associated with the input and low input means low output power dissipation [45, 42, 48]. However, it has the disadvantage of high output ripples, leading to high output noise [48]. Pulse phase modulation makes use of a reference periodic signal and generates another periodic signal based on the value sensed and encode the sensed value by the phase difference (which is an analogue time) between the two periodic signals [49, 50]. The main problem is its need for a stable carrier clock and its energy requirements. The last method may be called signal time modulation or period modulation. It encodes the sensed value in a length (period) of time not associated with any clock. This length of time is compared with a reference delay which is only activated at the beginning of each sensing round [4, 28]. This method has two advantages. It does not require an external voltage of clock reference and it potentially saves energy by only activating the internal time reference when necessary [30, 51]. This thesis concentrates on this type of solution.

Each type of solution has its advantages and disadvantages. Sensing microsystem designers made design decisions based on the particular needs and requirements they face.

Such microsystems have become advanced enough to motivate the Internet of things (IoTs), wireless sensor networks (WSNs) and biomedical implants [51–54]. They have been widely used in many application areas, including environment monitoring [55], smart buildings [56] and healthcare monitoring [9, 57]. However, the insufficient energy resources available in the sensor node limit the large-scale deployment of sensing microsystems [58–61].

Most of these sensor nodes are battery-powered and operate on an extremely frugal energy budget to extend the limited battery lifetime. However, when sensor nodes are placed in inaccessible locations, replacing old batteries may be expensive and time-consuming or may not be feasible, which becomes a key bottleneck [9, 62–64]. Therefore, the energy consumption of the sensor node needs to be minimised to reduce the times of battery replacement or even avoid the replacement to keep the lifetime for several years [9]. In response to this, energy harvesting systems are beginning to be used extensively in wireless sensor networks to provide unlimited energy by converting the renewable and unlimited ambient energies [51, 65].

In addition, due to the small size of the sensor node, the capacity of the energy storage and the amount of power that can be harvested or transferred are limited. Thus, energy efficiency is the primary research focus for wireless sensor networks. Methods of improving efficiency include shortening the wireless transmission time [9, 60] and using an energy-efficient sensor [26]. As capacitive sensors are suitable for low-power applications with limited energy budgets [2–4], this makes them a preferable option for a wireless sensing microsystem from an energy efficiency perspective. Moreover, the capacitive sensing technique has been used widely for sensing physical environmental properties in various situations due to the small size and high sensitivity of a capacitive sensor, for instance, pressure, acceleration and humidity [66, 67] may be converted into digital values through capacitances.

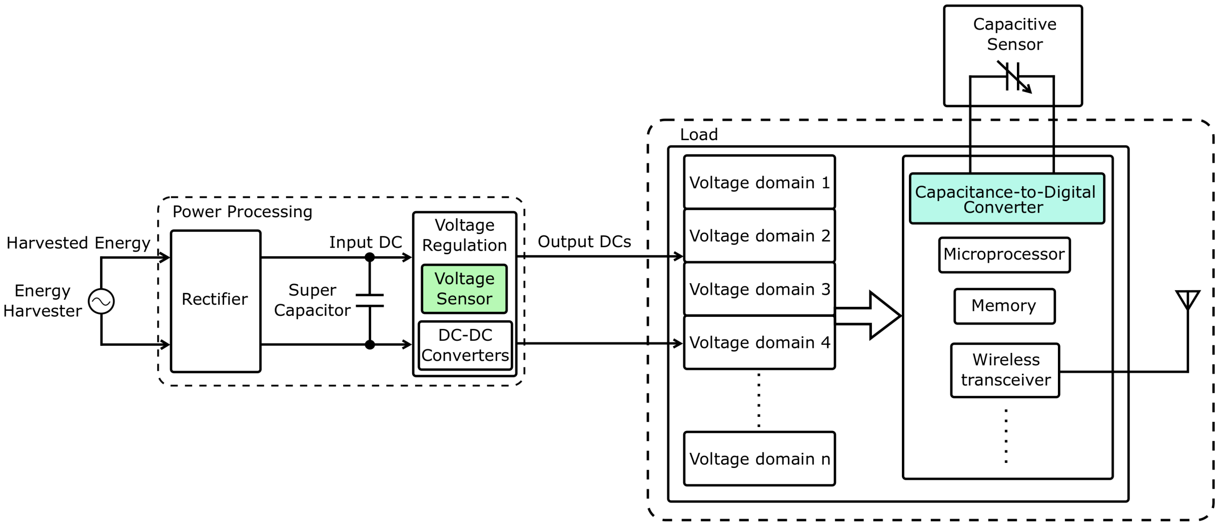


Fig. 1.2 System diagram of a wireless capacitive sensor node powered by energy harvesting system adapted from [7–9]. The harvested energy passes through the power processing part to obtain the regulated output DC voltages for the load element. Different voltage domains are created to power different blocks in the load. The capacitive sensor is interfaced with the capacitance-to-digital converter which is used to convert the capacitance to digital code.

Fig. 1.2 shows a simplified system diagram of a wireless capacitive sensor node powered by an energy harvesting system adapted from [7–9]. This system works in an environment with unpredictable energy availability, while the power supply may be non-deterministic during the working state [24, 68, 69]. A typical design has an energy harvester, a rectifier, a rechargeable super capacitor followed by a voltage regulation part. The regulated stable voltage powers the load which consists of capacitance-to-digital converter, microprocessor, memory, wireless transceiver, and antenna. Typically, the input DC is regulated to different voltage levels by using boost converter and buck converter. These converters can either be designed by using switched capacitors or inductors. The switched capacitor method has advantages of cheap and lightweight circuits, fast dynamic response and easy to be integrated. This method is commonly used in energy harvesting system. For the switched inductor is amenable in many converters with high boost ability, it is usually used in high gain DC-DC applications [70]. Generally, the required stable output DC voltage is regulated by DC-DC converter through a known voltage [71, 72] which is measured by special-purpose equipment such as voltage sensors. These sensors may be used to detect specific voltage levels and generate signals for event communication; this process referred to as voltage sensing [25, 29, 68] as shown in Fig. 1.2. A capacitive sensor converts the physical property being sensed into capacitance charge that can be measured. Thus, the sensor load has a capacitance-to-digital converter as the interface between the analog capacitive sensor and the microprocessor to convert the analog input into digital code for further processing in the digital world. These include the processing of measured data, data storage and data transmission.

Both the voltage sensor and the capacitance-to-digital converter focus on tracking physical analogue signals: input DC voltage or the change of the capacitance. Most existing design techniques work in the voltage domain for both voltage sensing and capacitance conversion. For instance, for voltage sensing, the general power-on reset circuit [8, 73, 74] is used to determine the crossing of a predefined voltage by directly monitoring the voltage; for capacitance-to-digital conversion, usually, the design needs to convert the capacitance into a voltage parameter, and then use an analog-to-digital converter to convert the voltage parameter into output digital code as presented in [66, 75, 76]. However, compared to the time domain technique used in [21] which has 0.9μs response time and 0.78mW power consumption, voltage domain techniques have certain drawbacks. Not only the complex circuit design for amplifier or analog-to-digital converter that may cause long response time (80ms in [77]) or high power consumption (4.4mW in [25]), but a stable reference voltage is also required during the sensing and conversion periods, respectively, which is difficult to obtain in an environment with insufficient and unstable energy [4, 21, 22, 28, 29, 72, 78, 79]. The authors from [80] state that "In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals". This includes that time-domain solutions being faster [81].

Due to these challenges, the focus of research starts shifting from voltage domain to time domain to remove either the complex op-amps [81, 82] or the stable reference voltage [21, 23]. There exist sensing techniques which involve charging/discharging a capacitor for sensing either the voltage or the capacitance in the time domain. For example, in the U.S patent No. 20130200727A1 presented in [22, 23], the authors employ an additional control unit to charge and discharge a constant capacitor. During the discharge process, an asynchronous counter is driven such that the energy inside the capacitor is completely depleted; the counter is read during this discharge period. The output code expresses the energy stored in the constant capacitor which is directly related to the initial voltage across the constant capacitor. Similar techniques are used to design a capacitance-to-digital converter presented in [4, 29]. The authors replace the constant capacitor with a capacitive sensor and then this capacitive sensor drives a digital circuit to achieve energy depletion, which is the same concept (charging/discharging the capacitor) as the U.S patent presented previously. In these design architectures, the authors used a ring oscillator for not only consuming energy stored in the sensed capacitor but also for directly converting the energy of the capacitor into a digital output code. As the charging voltage supplied at a time is constant, which is the supply voltage in [4, 29], the value of the output digital code depends on the value of the sensed capacitance. However, in these designs, the stable voltage still may be required for either storing the code [22, 23] or running the reference ring oscillator during the conversion period [4, 29].

The starting point of this thesis is to identify the limitations of traditional voltage and capacitance sensing techniques in the voltage domain presented previously, and subsequently explore alternative time domain solutions, similar to [4, 22, 23, 29], but aimed at removing the stable reference voltage and obtaining better performance.

1.2 Contributions

This research will develop a new type of threshold voltage detector using a time comparison technique to obtain the corresponding voltage information by determining the time delay. Two threshold voltage detectors are designed to create a time comparison-based voltage level-crossing sensor. This level-crossing sensor then forms the engine around which two more sophisticated sensing systems are designed, a voltage monitoring system and a capacitance-to-digital converter. The main contributions of this thesis are as follows:

1.2.1 Reference-free voltage monitoring system

- This voltage monitoring system does not require a stable V_{dd}, it can work under an extensive range of energy and voltage variations, for example, the operating supply voltage may be lower than 1.2V.
- An external stable current or voltage reference is not required, and replaced by an internal time reference.
- This voltage sensor can track both rising and falling voltage variations.
- Circuits are carefully designed and simulated over the range of voltage from 0.85V to 1.2V, the system was fabricated on-chip at the AMS 350nm technology node, and its operation correctness was validated through chip testing over the same voltage range.

1.2.2 Capacitance-to-digital converter based on time comparison technique

- A novel time comparison-based capacitance-to-digital converter with internal time reference is presented in this thesis.
- This time comparison-based capacitance-to-digital converter not only reduces the measurement time (76μs@7pF) but also improves the energy efficiency (10.17pJ/step) with high resolution (11.44bits) and high linearity (R^2=1).
- The voltage reference and comparison are not required during the digitalisation, which lowers the power consumption.
- According to the result of the test of the temperature dependence, a potential application, temperature sensor, is proposed as a future work.

1.3 Publications

The following papers have been published during this research work.

- Kaiyuan Gao, Yuqing Xu, Delong Shang, Fei Xia and Alex Yakovlev, " Wideband dynamic voltage sensing mechanism for EH systems, " 2015 IEEE 25th International Power and Timing Modeling, Optimization and Simulation (PATMOS), Salvador, 2015, pp. 185 - 192.

- Kaiyuan Gao, Delong Shang, Fei Xia and Alex Yakovlev, " Fast capacitance-to-digital converter with internal reference, " 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS), Shanghai, pp. 264 - 267.

- Delong Shang, Yuqing Xu, Kaiyuan Gao, Fei Xia and Alex Yakovlev, " Low power voltage sensing through capacitance to digital conversion, " 2016 IEEE 19th International Design and Diagnostics of Electronic Circuits and Systems (DDECS), Kosice, 2016, pp. 1 - 6.

1.4 Organisation of the thesis

This thesis is organised as follows:

- Chapter 2:
  This chapter discusses the general method of voltage sensing in the time domain, including the background of voltage-to-frequency converter and RC-based time reference.

- Chapter 3:
  This chapter is literature survey about some conventional voltage sensing techniques, including some existing reference-free voltage sensors either in the voltage or the time domain. At the end of this chapter, the capacitance-to-digital converter and some conventional conversion techniques are introduced.

- Chapter 4:
  The fundamentals of time comparison-based voltage level-crossing sensor are presented in this chapter. This chapter primarily presents the mechanisms and circuit design of two proposed reference-free threshold voltage detectors designed to work in the time domain.

- Chapter 5:
  This chapter focuses on the circuit design of the reference-free voltage monitoring system designed by combining the proposed reference-free threshold voltage detectors and the corresponding peripheral circuit. In addition, the chip fabrication was done in 350nm AMS technology node, was tested successfully during the voltage increases by performing measurements over the range from 0.85V up to 1.2V. In addition, the method (Focused ion beam) of chip repair are presented, and the temperature variation of the chip test is also discussed over the temperature range from 23°C to 100°C at the end.

- Chapter 6:
  This chapter aims to present the circuit implementation of the proposed energy-efficient

time comparison-based capacitance-to-digital converter. It describes circuit implementation, simulation results (tested from 1pF to 10pF) and temperature variation over a temperature range from -40°C to 120°C.

- Chapter 7:
  This chapter summarises the contributions of this work, and also discusses the future work based on the results of this study.

Chapter 2

Background

2.1 Introduction

This chapter provides the background information on voltage sensing in the time domain. Section 2.2.1 introduces the principle of the voltage-to-frequency converter and the three different implementations of voltage-controlled oscillator used to convert the voltage to frequency. In Section 2.2.2, the background of RC-based time reference is introduced.

2.2 Background of voltage sensing using time measurement

As discussed in Chapter 1, the research of voltage sensing in time domain has already shown a certain advantage compared to the design in the voltage domain, such as fast detection [81, 83]. Compared to the voltage domain approach, the time domain voltage sensing detects voltage in two steps; initially, the sensed voltage is converted into the time domain either as a time signal or frequency signal, which is then determined and converted to an event pulse signal or a digital code by a time detector or time-to-digital converter, respectively. Based on the theoretical study of the work in this thesis, this section introduces the background of the voltage-to-frequency converter and the background of the time constant of an RC circuit used to generate a constant time delay.

2.2.1 Voltage-to-frequency converter

The first challenge is converting the sensed voltage into the time domain. Generally, a voltage-to-time converter is used to generate a delayed pulse according to the sensed voltage [81]. Another way to convert the analog voltage into a time representation is to use a voltage-controlled oscillator. The voltage-controlled oscillator is one type of voltage-to-frequency converter used in many analog and digital circuits [11, 84] to generate a unique frequency or in other words unique period of clock at each voltage level by modulating its period according to the value of the analog voltage [85].

The ring oscillator-based voltage-controlled oscillator is a common structure which can be simply implemented due to the easy design and integrated into standard CMOS process [12, 86]. In addition, its frequency has better linearity with respect to the control voltage (or the supply voltage) and can be constructed with standard logic cells [12, 87]. As the voltage-to-time conversion engine is not within the scope of the contribution of this thesis, it should be as simple as possible. Therefore, the ring oscillator-based voltage-controlled oscillator was selected for converting the voltage to frequency.

The oscillation frequency of the voltage-controlled oscillator can be set to the desired value by tuning the input voltage. Equation 2.1 shows the output frequency for ideal voltage-controlled oscillator as follows[12, 84]:

$$f_{out} = f_0 + K_{VCO} \times V_{ctrl} \tag{2.1}$$

where f_0 is the free running frequency, V_{ctrl} is the input control voltage and K_{VCO} is the sensitivity or gain of the voltage-controlled oscillator [12]. In a basic inverter-based voltage-controlled oscillator (See Fig. 2.1), the V_{dd} is the V_{ctrl} in Equation 2.1. However, in an MOS capacitance-based voltage-controlled oscillator (See Fig. 2.3) and in a current starved inverter-based voltage-controlled oscillator (See Fig. 2.5), the V_{ctrl} is an extra variable voltage used to tune the frequency [10, 12, 32]. Equation 2.2 shows the proportional relationship between the output frequency and the control voltage [51, 84]:

$$f_{out} \propto V_{ctrl} \tag{2.2}$$

Thus,

$$V_{ctrl} \propto f_{out} \propto \frac{1}{T_{clk}} \tag{2.3}$$

where T_{clk} is the period of the voltage-controlled oscillator. Hence, V_{ctrl} is proportional to $1/T_{clk}$ at each V_{ctrl} level; a unique period is generated according to the corresponding voltage level [28]. Basically, the generated frequency of voltage-controlled oscillator increases with increase in input control voltage (V_{ctrl}) and decreases with decrease in input control voltage [11, 12, 51, 88].

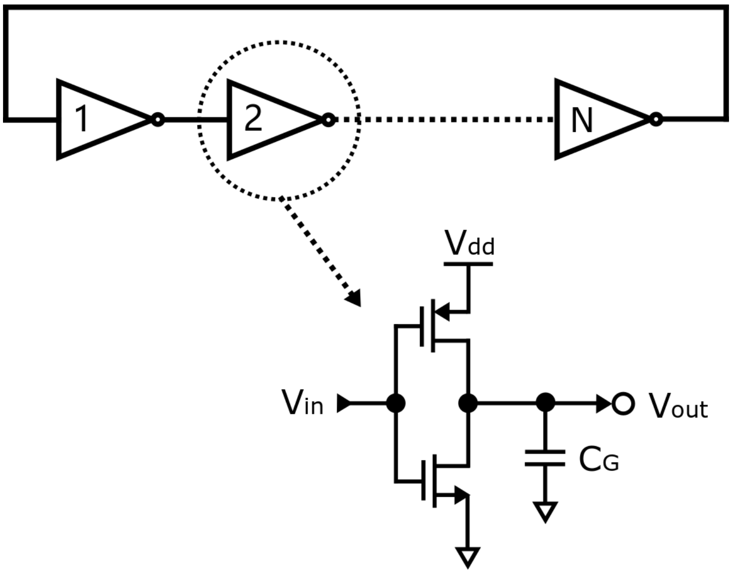


Fig. 2.1 Basic inverter-based voltage-controlled oscillator copied from [10]. C_G is the parasitic capacitance of the MOS transistor at each inverter stage.

Furthermore, the fundamental equation of the frequency is derived from the structure of the fundamental design of the voltage-controlled oscillator (See Fig. 2.1). Assume that there are N stages in a voltage-controlled oscillator and each inverter stage yields a delay time (t_D). The output frequency f_{out} can be expressed as follows [13, 15, 88]:

$$f_{out} = \frac{1}{2 \times N \times t_D} \tag{2.4}$$

During the oscillation, the operation at each inverter stage can be assumed as a process of charging or discharging the parasitic capacitance C_G through the MOS transistors treated as switches at each inverter stage. If it is assumed that transconductance G_m of NMOS transistor is equal to that of PMOS transistor, and the parasitic capacitor of NMOS transistor is equal to that of PMOS transistor, each inverter stage can be simplified to a simple RC circuit as shown in Fig. 2.2.

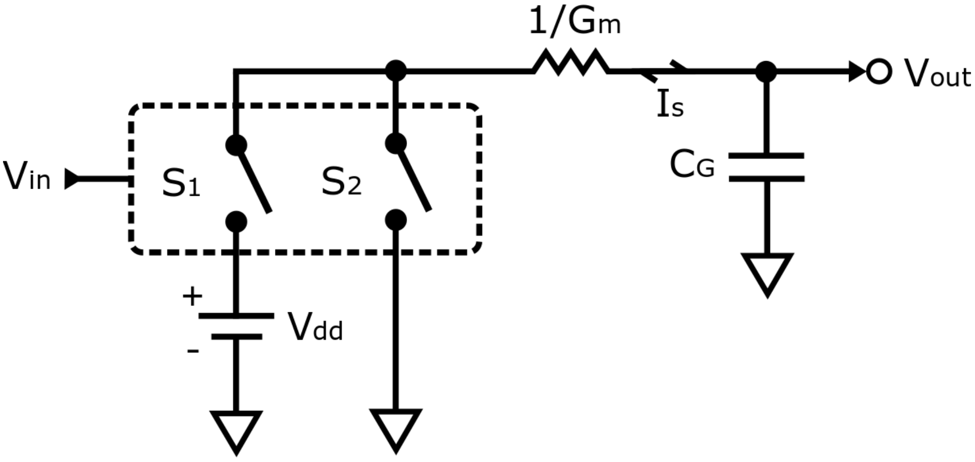


Fig. 2.2 Delay approximation of basic inverter-based voltage-controlled oscillator adapted from [11, 12]. Once the input V_{in} of one single inverter stage is low, S_2 is open and S_1 is closed to charge C_G through $1/G_m$. However, if the input is high, S_1 is open and S_2 is closed to discharge C_G through $1/G_m$. The current during the charge and discharge is the value of I_s.

The delay time t_D of each inverter stage can be approximately given by Equation 2.5 as [11, 12, 32, 88]:

$$t_D = \frac{C_G}{G_m} = \frac{C_G \times V_{dd}}{I_s} \tag{2.5}$$

Thus, the frequency of voltage-controlled oscillator can also be found as follows [11, 12, 32, 88]:

$$f_{out} = \frac{G_m}{2 \times N \times C_G} = \frac{I_s}{2 \times N \times V_{dd} \times C_G} \tag{2.6}$$

where N is number of the inverter stages in a voltage-controlled oscillator, C_G is the parasitic capacitor of each inverter stage, G_m is the transconductance of MOS transistors and I_s is the current flowing through the resistor in Fig. 2.2, V_{dd} is the power supply.

As illustrated in Equation 2.6, for a given number of stages, the oscillation frequency is controlled by the following parameters:

- The value of G_m or the value of I_s
- The capacitance of C_G
- And, the value of V_{dd}

As the change of the resistance of $1/G_m$ results in the change of current I_s, the common approach generally focuses on tuning one of them (generally $1/G_m$) to adjust the frequency [12, 84]. Based on these factors, three types of ring oscillator-based voltage-controlled oscillator will be introduced in this section. The first type is the basic inverter-based voltage-controlled oscillator as shown in Fig. 2.1, where the odd number (N) of basic inverter was connected in series, with the output of the last inverter fed back to the input of the first inverter. In this structure, the parameters of the NMOS and PMOS transistors of each inverter stage are constant, and thus the parasitic capacitor C_G is also constant. The frequency of this type is a function of the supplied voltage of V_{dd}. Therefore, it has the ability to generate a V_{dd}-dependent frequency.

The second type is MOS capacitance-based voltage-controlled oscillator as shown in Fig. 2.3, which tunes the load capacitance at the end of each inverter stage and the third type is current starved inverter-based voltage-controlled oscillator as shown in Fig. 2.5, which adjusts the current by tuning the G_m during the oscillation. The first structure (Fig. 2.1) only needs one power supply V_{dd} for both the powering and the controlling function ($V_{ctrl} = V_{dd}$, V_{ctrl} is from Equation 2.2), and the last two structures (Figs. 2.3 and 2.5) not only need V_{dd} for the powering function but also need an extra control voltage V_{ctrl} for the controlling function.

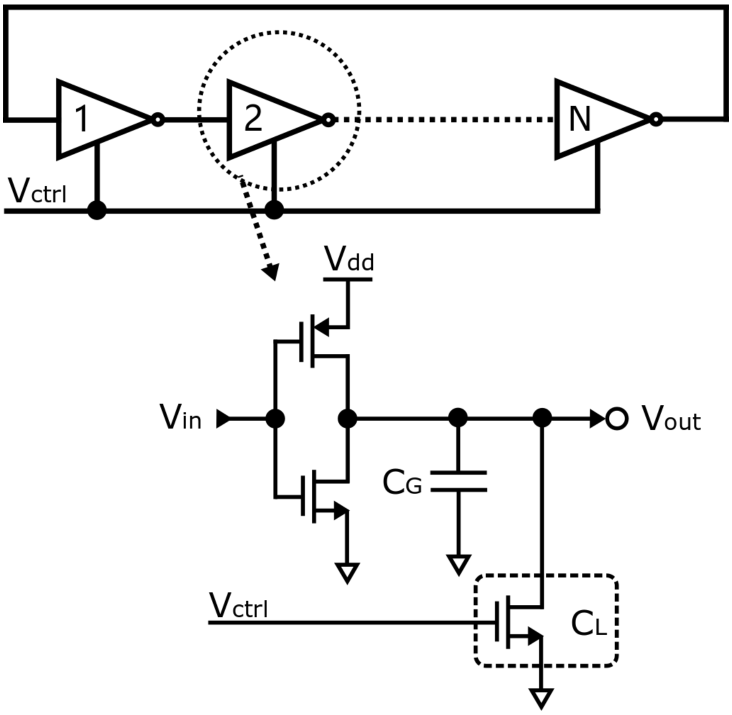


Fig. 2.3 MOS capacitance-based voltage-controlled oscillator adapted from [13]. A NMOS transistor-formed variable capacitor C_L is added to each inverter stage.

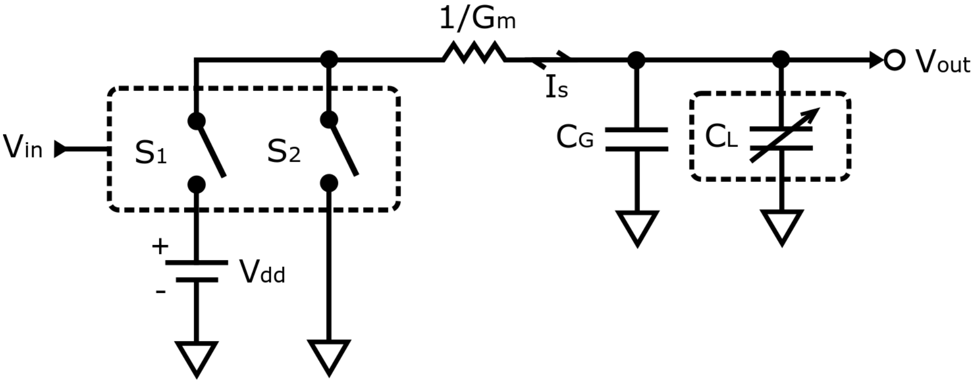


Fig. 2.4 Delay approximation of MOS capacitance-based voltage-controlled oscillator adapted from [13].

Similarly, a second type of voltage-controlled oscillator is also a single end oscillator which is same as a basic inverter-based voltage-controlled oscillator. Compared to the first type voltage-controlled oscillator, the MOS capacitance-based voltage-controlled oscillator adds one NMOS transistor at the output of each stage of the basic inverter-based voltage-controlled oscillator as shown in Fig. 2.3. The added NMOS transistor is a variable MOS capacitor obtained by applying the variable gate voltage V_{ctrl} at the gates, producing a variable MOS capacitance; thus, with a variable load capacitance at the output of each stage, the load capacitance at each stage will be $C_G + C_L$, resulting in a variable delay generated in the oscillator. The delay approximation is shown in Fig. 2.4. Hence, the oscillation frequency in terms of variable capacitor [10] is

$$f_{out} = \frac{G_m}{2 \times N \times (C_G + C_L)} \tag{2.7}$$

where C_L is equal to $\frac{C_{ox} \times C_S}{C_{ox} + C_S}$; C_S is defined as Semiconductor Capacitance. The derivation of Equation 2.7 can be found in [13]. According to Equation 2.7, the frequency of the oscillator is determined by three parameters in this type of voltage-controlled oscillator: transconductance G_m, parasitic capacitance C_G and variable MOS capacitance C_L. For a given voltage-controlled oscillator, G_m and C_G are device parameters and constant. The output frequency depends on the value of C_L [13] by regulating V_{ctrl} as shown in Fig. 2.3. As mentioned previously, this type of voltage-controlled oscillator also requires a extra voltage used as a stable V_{dd} for powering purpose.

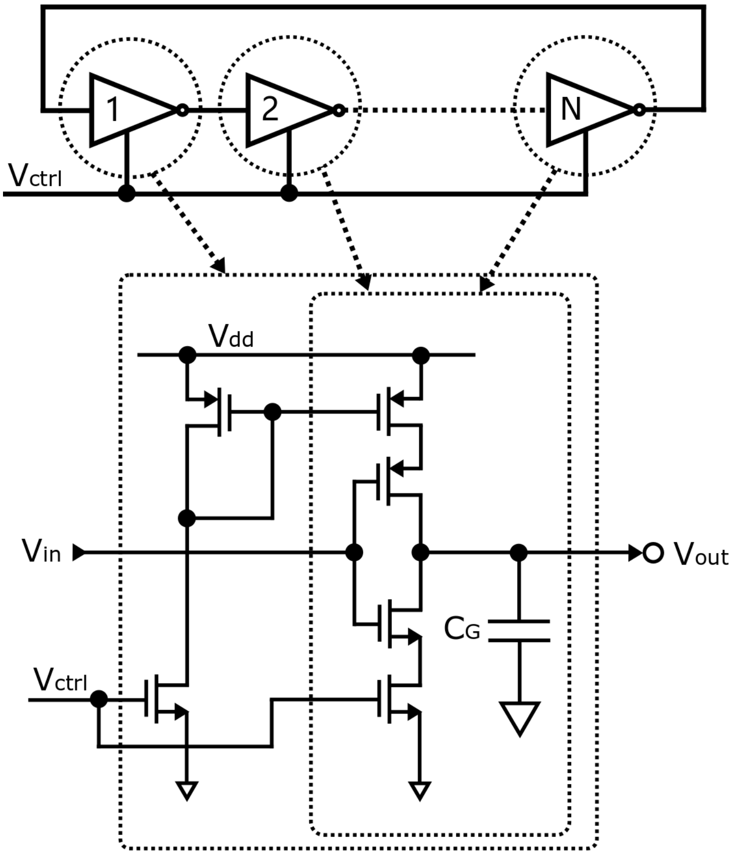


Fig. 2.5 Current-starved inverter-based voltage-controlled oscillator adapted from [14]. A current mirror is added to each inverter stage for copying the same current to each inverter stage.

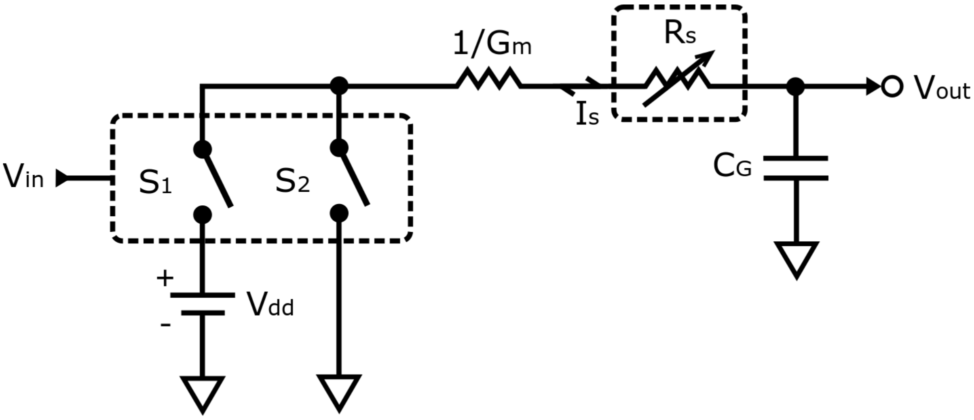


Fig. 2.6 Delay approximation of current inverter-based voltage-controlled oscillator adapted from [15].

The first two voltage-controlled oscillators have been described previously, according to tuning V_{dd} and load capacitance, respectively. Another way to control the frequency is to control the amount of current available to charge/discharge the load capacitance at each inverter stage in the oscillator which is named as a current starved inverter-based voltage-controlled oscillator as shown in Fig. 2.5. In this type of voltage-controlled oscillator, the control voltage V_{ctrl} is used to modulate the on-resistance of the pull-down/pull-up transistor through a current mirror, resulting in a tunable variable current. The delay approximation is shown in Fig. 2.6, and the variable resistor R_s is added to each inverter stage. In the current-starved inverter-based voltage-controlled oscillator, the current I_s is a variable parameter controlled by the variable resistor R_s. The current I_s used to charge/discharge the parasitic capacitance C_G with a function of the small value of V_{ctrl} allows a small current to flow, producing a large resistance and resulting in significant delay. Therefore, unlike MOS capacitance-based voltage-controlled oscillator, the current starved inverter-based voltage-controlled oscillator controls its frequency by tuning the variable bias current through changing the variable resistance [89] as illustrated in Equation 2.6 instead of adjusting the load capacitance at the output of each inverter stage.

Overall, the voltage-controlled oscillator can generate a unique frequency to correspond to any specific voltage value in these three types, basic inverter-based type, MOS capacitance-based type or current staved inverter-based type, with the corresponding voltages being either V_{dd} or V_{ctrl}. As this thesis primarily investigates the research of reference-free sensing technique in an unpredictable energy environment, unstable V_{dd} is applied in the system. Hence, the basic inverter-based voltage-controlled oscillator is the selected architecture for the voltage-to-frequency converter in this thesis.

2.2.2 RC-based time reference

As the unique frequency is generated at each V_{dd} level in the basic inverter-based voltage-controlled oscillator, the generated unique period can be used to represent each V_{dd} level. Therefore, the challenge is moved from how to convert the voltage to frequency to how to represent the period by a constant time delay according to the voltage level.

A constant time parameter can be implemented with a number of methods such as transistor- and capacitor-formed delay element in [90, 18] or inverter chain-formed delay element in [28, 4]. A simple method is using the time constant τ in an RC circuit [91] whose latency is independent of its supply voltage V_{dd} [16, Chapter 11, Equation 11-6]; Furthermore, it is fairly convenient to use a set of the predefined time constants with multiple values of τ. The value of τ in an RC circuit will affect the charge and discharge rate of the capacitor. The value depends on the product of the resistor R and the capacitor C [16, 92] can be expressed as follows:

$$\tau = R \times C \tag{2.8}$$

where R is in ohms, C is in farads, and τ has the units of second.

As shown in Fig. 2.7, during charging and discharging, the length of time (t) depends on the exponential function $e^{-t/\tau}$, and V_C (the voltage across capacitor) is exponential to t [16, Chapter 11, Equation 11-7 and Equation 11-13]. With the increase of t, $e^{-t/\tau}$ decreases and once $e^{-t/\tau}$ decreases to zero, the charging or discharging is complete. The Fig. 2.7 illustrates that changing the value of τ can adjust the time so that V_C reaches the 99.3% full voltage. As time constant is a voltage-independent value, the time delay based on the value of τ is possible to be a constant value in an undetermined energy environment.

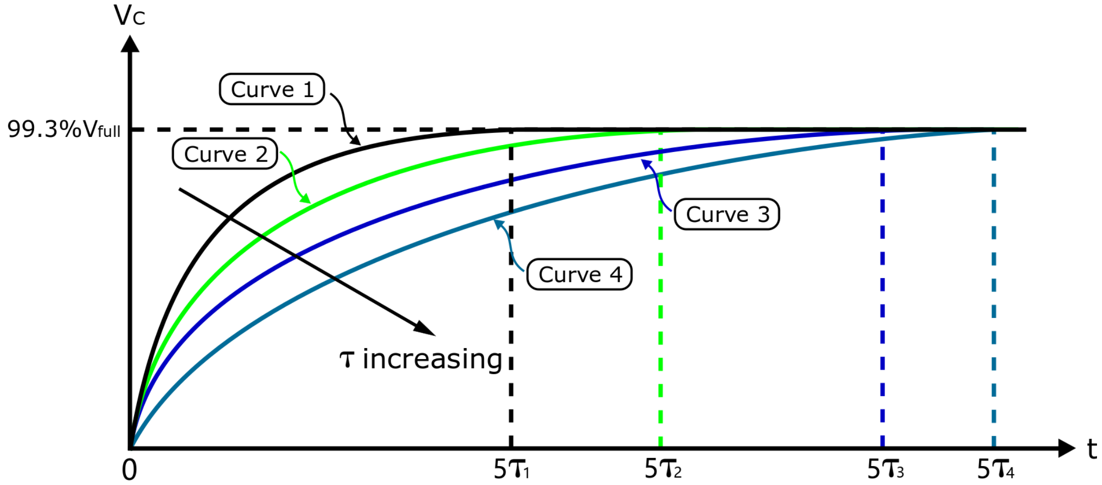


Fig. 2.7 The influence of time constant on the voltage in an RC circuit copied from [16]. The larger the value of τ, the longer the time needed to charge to 99.3% during the charge state. For the discharge state, the same influence; $\tau_1 < \tau_2 < \tau_3 < \tau_4$.

Therefore, the charging/discharging rate depends on τ in an RC circuit, and the value of τ which is voltage independent will be used to generate the different constant time delays corresponding to different voltage levels as illustrated in Equation 2.3. It will also be used in the proposed capacitance-to-digital converter which primarily focuses on determining the time interval of the capacitor discharging.

2.3 Summary

This chapter introduces the basics of voltage sensing in the time domain. This forms the foundation of the new voltage detection theory proposed in Chapter 4.

Chapter 3

Literature Survey

3.1 Introduction

In this chapter, the existing voltage sensing techniques is discussed in Section 3.2 and conventional design approaches of the capacitance-to-digital converter is introduced in Section 3.3. Due to the unstable energy environment in an energy harvesting system [24], the stable voltage cannot be easily provided in the system. The different types of reference-free voltage sensor are listed and introduced in this chapter to address the problem of needing a reference voltage. In addition, as discussed in Chapter 1, the capacitive sensor [30, 93, 94] is extensively used in physical sensor, which usually requires a digitalisation block to convert capacitance to digital code. Several conventional capacitance-to-digital converters have been introduced and discussed.

3.2 Voltage sensing techniques

Due to the extensive range of applications, the voltage sensing techniques have been developed in different designs to meet various specifications. This literature survey will primarily discuss two different types of voltage sensing techniques that directly compare with the method employed in this thesis. The first is the power-on-reset circuit that detects the intersection of the predefined threshold voltage. This thesis includes original research on voltage-crossing sensing techniques which accomplish a similar goal. The second is the reference-free voltage sensors. Design without reference voltage has significant advantage in an energy harvesting system as it is difficult to obtain a stable reference voltage in an energy harvesting system. The work in the thesis will contribute to the reference-free voltage sensing technique.

3.2.1 Power-on-reset circuit

Considering its features of low area and power consumption, the power-on-reset circuit is a type of conventional method used to detect the predetermined voltage level in mixed-signal integrated circuits [8, 73, 74]. In an energy harvesting system, the power-on-reset circuit is used in the power management unit to generate a flag signal to indicate the harvested energy level if the measured voltage surpasses the triggering threshold voltage [19, 95]. Generally, there are three typical designs of the power-on-reset circuit [96]:

1. The conventional design consists of a capacitor, a resistor and a pulse generator as shown in Fig. 3.1(a).
2. The common approach uses a reference voltage, a voltage comparator and a pulse generator as shown in Fig. 3.2.
3. The updated method uses a delay element and a voltage divider as shown in Fig. 3.1(b).

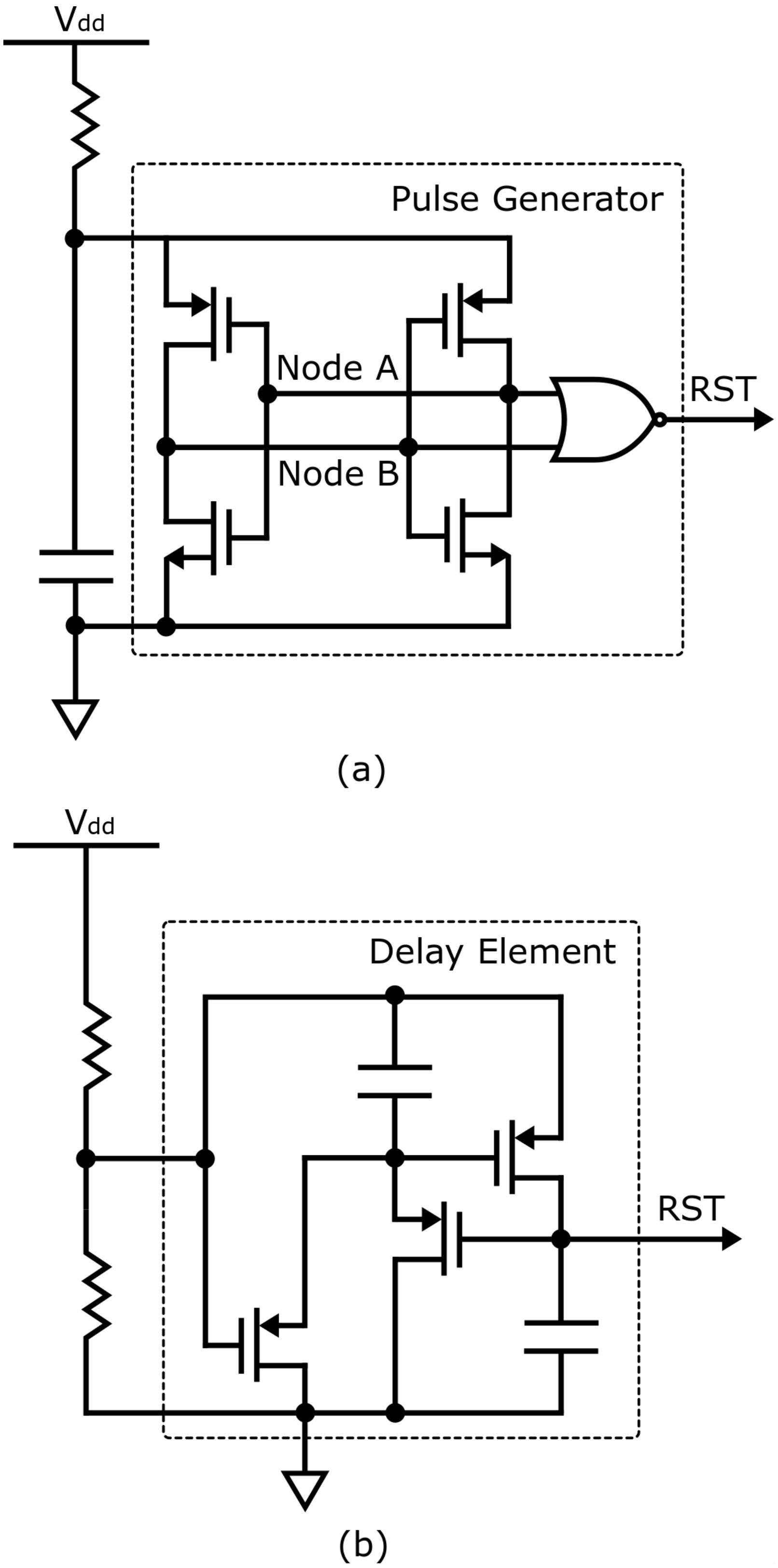


Fig. 3.1 Power-on-reset circuit. (a) RC-based power-on-reset circuit copied from [17]. (b) Delay-based power-on-reset circuit adapted from [18].

Fig. 3.1(a) shows a simple RC-based power-on-reset circuit. It is composed of a RC circuit and a pulse generator formed by a cross-coupled inverter pair and a NOR gate. The RC circuit is used to provide a sufficient ramp-up time of V_{dd} for the pulse generator to generate a reset signal RST.

The pulse generator is an unstable system due to the generated divergence of the two nodes of the cross-coupled inverter pair from the metastable point to the stable equilibrium point in the state space when the circuit powers up. The divergence is caused because of the various noise sources in the actual circuit. The two nodes of the cross-coupled inverter pair are connected to a NOR gate; once the difference voltage of them is greater than a predefined value, the *RST* is generated to represent the detection of the predefined voltage. A simple circuit based on an RC circuit for voltage detection is sufficient to be used as a power-on-reset circuit. However, due to the need for a long ramp-up time, the detection time of the predefined voltage becomes long, which is not efficient for an energy harvesting system in which energy is unstable [18, 97].

Multiple techniques have been explored to replace the RC-based power-on-reset circuit due to the long ramp-up time [19]. Fig. 3.1(b) and Fig. 3.2 show two common approaches used for research currently.

Fig. 3.1(b) shows a delay-based power-on-reset circuit. This power-on-reset circuit only consists of three transistors, two capacitors and a voltage divider. This power-on-reset circuit can tolerate an extensive variation of V_{dd} ramp-up times and an extensive range of final voltage values. The pulse of the generated reset signal *RST* has a desired width after a delay element. Moreover, [18] presented a new method to programme the pulse width by adding a reasonable number of delay elements for generating the required pulse width. Although the main contribution of this design is remove the RC circuit and save detection time, it still has another issue which is single threshold voltage detection. Multiple threshold voltage detection is required in the existing system-on-chip due to the multiple supply voltage domains in the system [19, 77, 98, 99]. It is a common issue in the conventional power-on-reset circuit to detect only one threshold voltage in the implementation. Therefore, a new approach based on the general signal voltage reference-based power-on-reset circuit was presented in [19, 20].

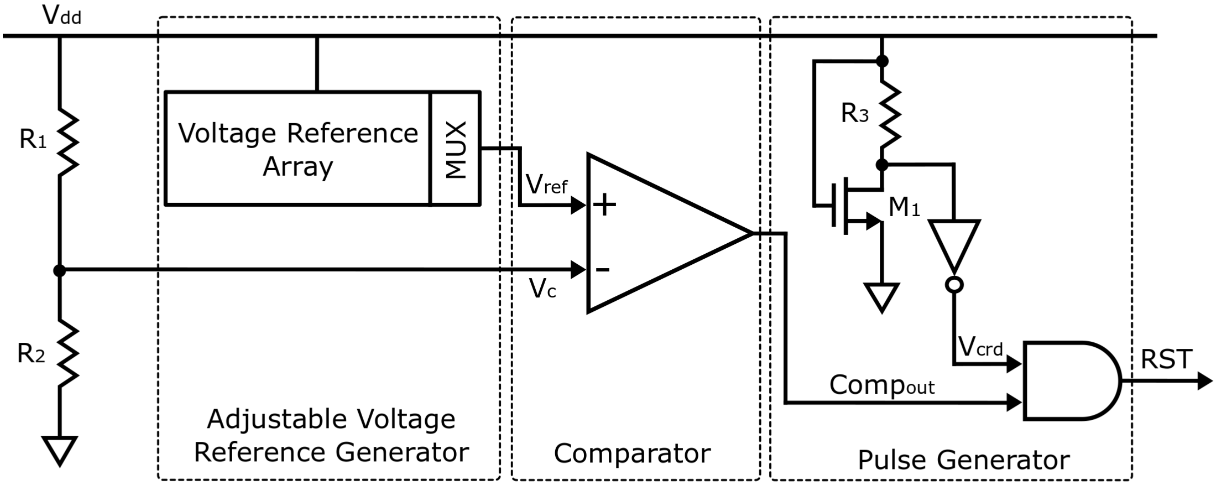


Fig. 3.2 Reference-based power-on-reset circuit adapted from [19, 20].

Fig. 3.2 shows the general reference-based power-on-reset circuit used to detect multiple voltage levels. In this design, MUX is used to select different reference voltage from the band gap voltage reference array to achieve the detection of the predefined threshold voltage in the different voltage domains required in the system [19]. Subsequently, the selected voltage reference V_{ref} is compared with the supply voltage V_{dd} to generate a compared output signal $Comp_{out}$ which can be used as a reset signal for the system. As V_{ref} also depends on V_{dd}, a range of V_{dd} may be formed for which the $V_c > V_{ref}$ when V_{dd} is smaller than the expected voltage of the trip point. In this situation, the $Comp_{out}$ is an inappropriate reset signal. Therefore, a transistor threshold-based level detector (formed by R_3 and M_1) may be used to mask the incorrect $Comp_{out}$. The V_{crd} range is guaranteed between $V_{in_{err}}$ (the voltage of V_{ref} that is just greater than V_d) and V_{L2H} (the voltage of V_d that is just greater than V_{ref} such that the power-on-reset circuit reset signal may be changed from logic low to high) and subsequently, $Comp_{out}$ and V_{crd} are passed through an AND gate to generate the reset signal RST as shown in Fig. 3.2. However, in low-power applications, the circuit operating at low voltages and the voltage reference generator should have the ability of working at a V_{dd} sufficiently lower than the required predefined threshold voltage to generate a stable V_{ref} and then achieve a precise predefined threshold voltage detection [97]. In an energy harvesting system, at such low and unstable operating voltages, generating a stable reference voltage is difficult as the reference voltage depends on the supply voltage [20, 22, 100]. Therefore, in order to address this issue in the generation of reference voltage, the reference-free techniques have become a new trend for voltage sensing.

[101] presents a new sensing method without the reference voltage in the power-on-reset circuit. This reference-free method is based on the threshold voltage of the transistor. The author uses a simple feedback circuit to trigger the power-on-reset circuit to generate a reset signal when the energy is sufficient to power this feedback circuit. Using this method, an extra reference voltage is eliminated because the reference voltage is essentially the threshold voltage of transistor. However, the limitation is obvious. First, the minimal detected voltage significantly relies on the structure of the feedback element, which is the SR latch in [101]. Second, this method can only detect voltage increases but not the voltage decreases. Finally, this approach has achieved a reference-free voltage detection but cannot detect multiple voltage levels. However, this ability is required to power different elements in a system as mentioned previously. To meet the requirements of multiple threshold voltage detection, the voltage sensor is alternative to sense or detect the predefined threshold voltage. In next subsection, the reference-free voltage sensors will be introduced and discussed.

3.2.2 Reference-free voltage sensors

In the previous subsection, a voltage sensing technique power-on-reset circuit that is often used in the system was introduced. In addition, analog-to-digital converter and voltage sensor are another two common voltage sensing techniques. The analog-to-digital converter is a conventional textbook voltage sensing technique used to accurately convert the voltage to a binary code indicating the sensed voltage level [21, 68, 102]. However, this solution requires a stable voltage for not only circuit power but also the reference signals, and the power consumption is quit high. Therefore, this solution is not suitable for most energy harvesting systems. As this paper focuses on the research of voltage detection technology in the field of energy harvesting system, the analog-to-digital converter will not be discussed in detail but only the research on the reference-free voltage sensing technique, which is a new direction of the voltage sensing, will be emphasised [101]. Fig. 3.3 and Fig. 3.4 present two time-domain reference-free sensors and two voltage-domain reference-free sensors.

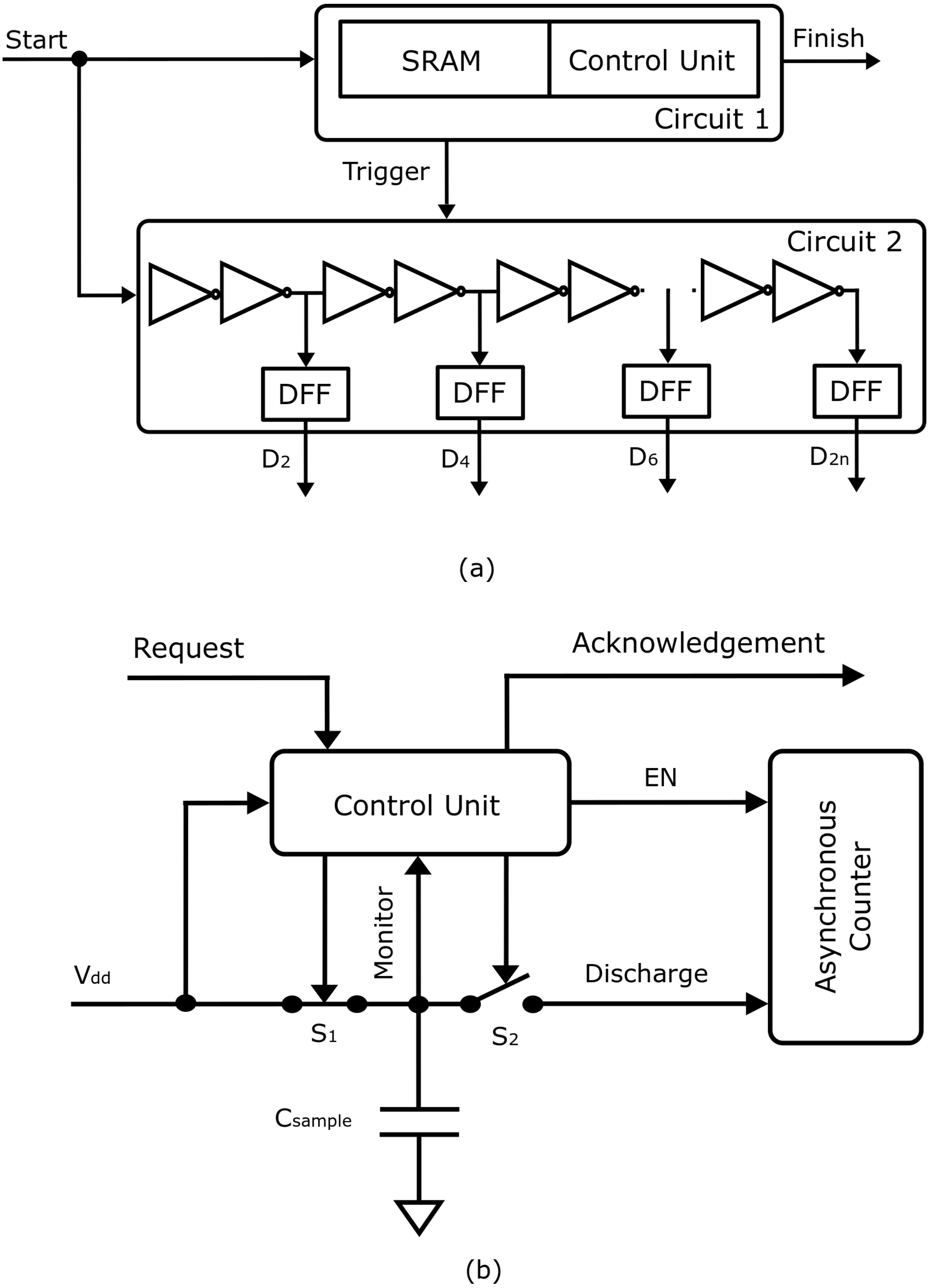


Fig. 3.3 Reference-free voltage sensors in time domain. (a) Adapted from [21]. (b) Copied from [22, 23].

As different circuits have different performance in the supply voltage environment, a new implementation of voltage sensing technique has accordingly been presented [21, 28, 29]. In [21], the authors present an approach to sense the voltage by using the different latencies in two different circuits under the same supply voltage environment as shown in Fig. 3.3(a). Circuit 1 consists of a speed-independent SRAM and a control unit. The SRAM's completion time is determined by the supply voltage, and the control unit is used to generate the finish signal and help the SRAM generate a trigger signal for latching Circuit 2 to output the thermometer code. Circuit 2 is a simple inverter chain with D Flip-Flop registers connected to every second node of the chain as shown in Fig. 3.3(a). This voltage sensor begins to sense the voltage when the *Start* signal is input into Circuit 1 and Circuit 2. The SRAM cell starts the read or write operation; in the meantime, the input value of the first inverter is flipped and flip in turn in the inverter chain until the operation of the SRAM is complete and the *Trigger* signal is generated and used to latch the circuit 2. The output of the D Flip-Flop is read to calculate the number of the flipped inverter. Therefore, the generated thermometer code from the D Flip-Flop is used to represent the sensed voltage. This method can achieve low voltage down to 0.2V and a fast response time up to 872ns in the 90nm technology node. However, the circuit area is comparatively large, resulting in higher consumption (0.78mW) compared to other three reference-free voltage sensors.

U.S Patent No. 20130200727A1 [22, 23] presents a novel reference-free voltage sensing technique: charging/discharging a sample capacitor to power an asynchronous counter as shown in Fig. 3.3(b). This approach uses a “run-to-death” method to sense the voltage. The measured energy is stored into a sample capacitor by charging. Once the capacitor is fully charged, it is disconnected from the energy source and connected to the asynchronous counter till stored energy is completely consumed by the counter, which means that the counter is "dead". Once this charging/discharging is complete, the generated code from the counter is used to present the measured voltage. As this stored energy is reused to power the counter, the energy in energy source is saved. Simultaneously, because "run-to-death" approach is used, the reference voltage is not required such that the reference voltage is approximately zero. However, the sensing time may be longer (98ms) as the sample capacitor has to be charged in the beginning which may need some time. Another issue is the preservation of the output code. After the counter is "dead", it can no longer keep the output code. An extra stable voltage powered memory is required to save the generated code during each code generation which may consume extra high energy.

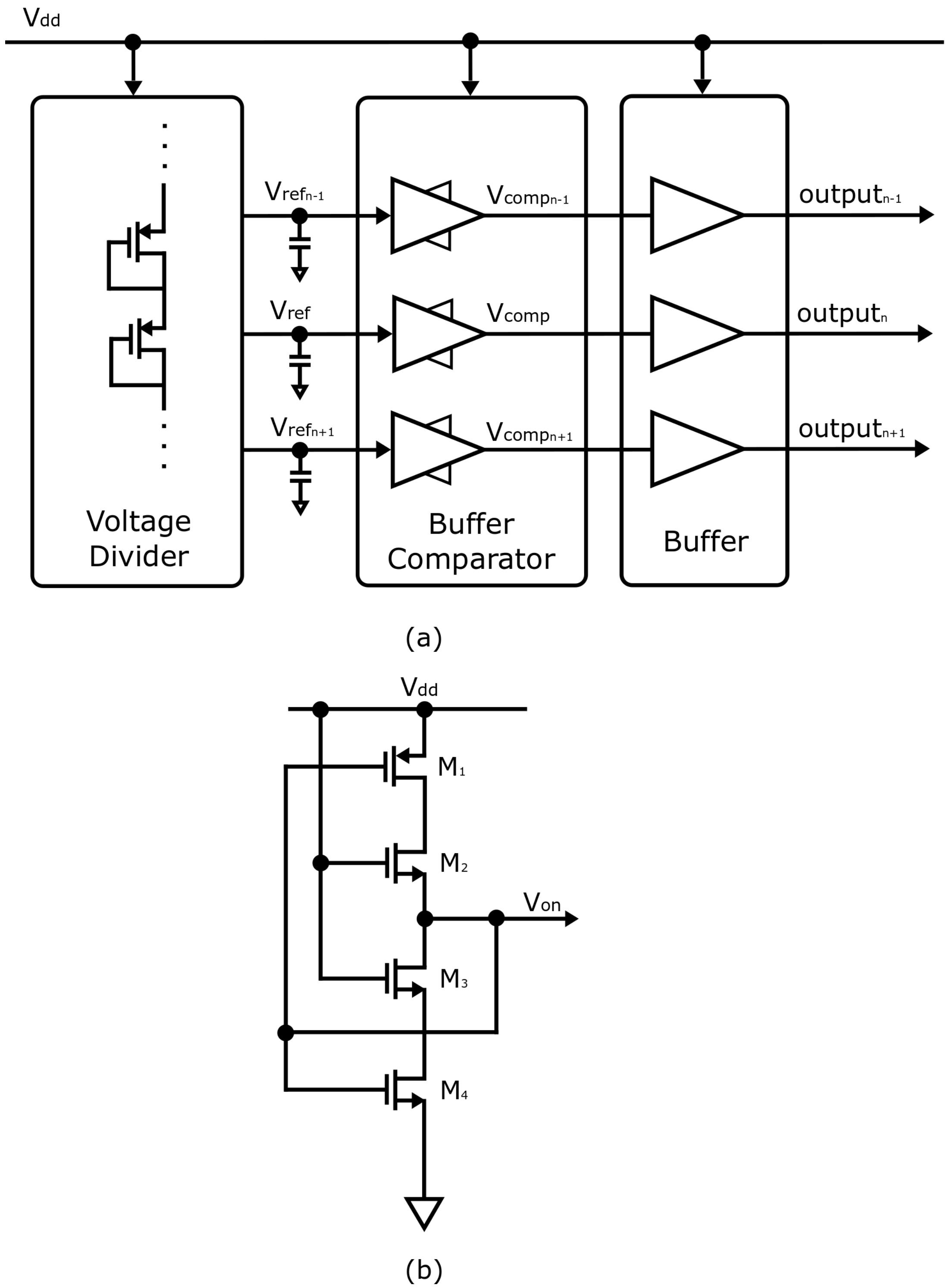


Fig. 3.4 Reference-free voltage sensors in voltage domain. (a) Copied from [24]. (b) Copied from [25].

In [24], the reference-free voltage sensor consists of a voltage divider, a buffer comparator and a buffer as shown in Fig. 3.4(a). The V_{dd} is split into different voltage values by the voltage divider, and each value is connected to the buffer comparator. Once the input value of the buffer comparator is over the inversion point of the cell, the output V_{comp} increases. Conversely, if the input value is under the inversion point of the cell, the output of of the comparator decreases, yielding a thermometer code corresponding to the measured V_{dd}. This approach removes the external reference voltage or clock by using the voltage divider to detect different predefined voltage, which is advantageous to determine the different voltage levels; other internal parameters can also be used to determine the voltage level, such as time delay [28, 29, 81]. However, this method causes other issue that the circuit area is possibly large, as the number of the resistor in voltage divider is increased with the increase of the number of the predefined voltage, and also the number of the comparator in buffer comparator is increased due to the same reason.

In 2015, another new simple reference-free voltage sensor was presented in [25]. This voltage sensor only consists of four transistors as shown in Fig. 3.4(b). These four transistors form a resistive divider which generates an output normal voltage V_{on} if the V_{dd} is stable. Once the V_{dd} is changed, the output generates a voltage difference from V_{on}. The author uses this feature to generate an event pulse to represent the voltage detection by using the negative feedback formed by connecting the gate of M_1, the gate of M_2 and the output. Due to the negative feedback, whenever the output differs from V_{on}, it will activate the corresponding transistor and drive more current in the opposite direction. Subsequently, the voltage difference in output will be eliminated until V_{on} is established. Through this process, a pulse is generated to inform the detection of the predefined threshold voltage. This reference-free voltage sensor is easy to implement and has a small circuit area. However, this voltage sensor is more similar to a power-on-reset circuit to detect one predefined threshold voltage without reference, as it can only detect one predefined threshold voltage instead of multiple voltage levels during voltage sensing.

Table 3.1 Overview of different voltage sensing techniques.

Type of voltage sensing	Advantage	Disadvantage	Reference Required
Power-on-reset circuit ([19])	Threshold adjustable (0.79V, 1.77V, 2.22V).	An array of stable reference voltages, complex circuit design (counter and comparator are needed).	Reference voltage
Power-on-reset circuit ([101])	No need reference, minimal area (21.3 μm^2), low voltage detection (400mV).	Single threshold voltage, the detected voltage is limited and fixed by the pulse generator (SR latch).	No
Time-domain voltage sensor ([23])	No need reference, low power consumption (0.36 mW), wide voltage range (0.8V - 1.8V).	only detects voltage drop.	No
Voltage-domain voltage sensor ([24])	No need reference, low power consumption (50μW), fast response (5ns).	only detects voltage drop, multiple complex voltage comparators.	No

Table 3.1 shows the overview of different voltage sensing techniques. As mentioned previously, the reference-free voltage sensing techniques has begun attracting researchers' attention. In the literatures discussed, the reference-free techniques can either be implemented in the time domain, such as in Fig. 3.3(a), using the characteristic of the different circuit and a smart solution in

Fig. 3.3(b), using the charge/discharge time to convert the voltage into readable code or can be implemented in the voltage domain, such as in Fig. 3.4(a), generating the internal reference voltage instead of external reference voltage and in Fig. 3.4(b), using the characteristic of the transistor. From the perspective of considering the complexity of the circuit design, in the literatures, the time-domain voltage sensor is the top option due to does not require complex analog circuits, such as amplifiers and analog-to-digital converters [23, 28, 29], which may lead to reduced design complexity and reduced power consumption.

3.3 Capacitance-to-digital converter

Capacitance-to-digital converter is the interface circuit used in the capacitive sensor for converting a unknown capacitor into a digital code. Generally, the sensed capacitance value (C_{sense}) is converted into a voltage parameter [75] or a time parameter. For example, period [103] and frequency [4]. According to the different output signals, the different conversion architectures are employed [9, 104] as shown in Fig. 3.5. In the flowing subsections, different capacitance-to-digital converter architectures are discussed with examples. Particularly, the architecture for converting to frequency will be highlighted, which is the same method used in the proposed capacitance-to-digital converter presented in Chapter 6.

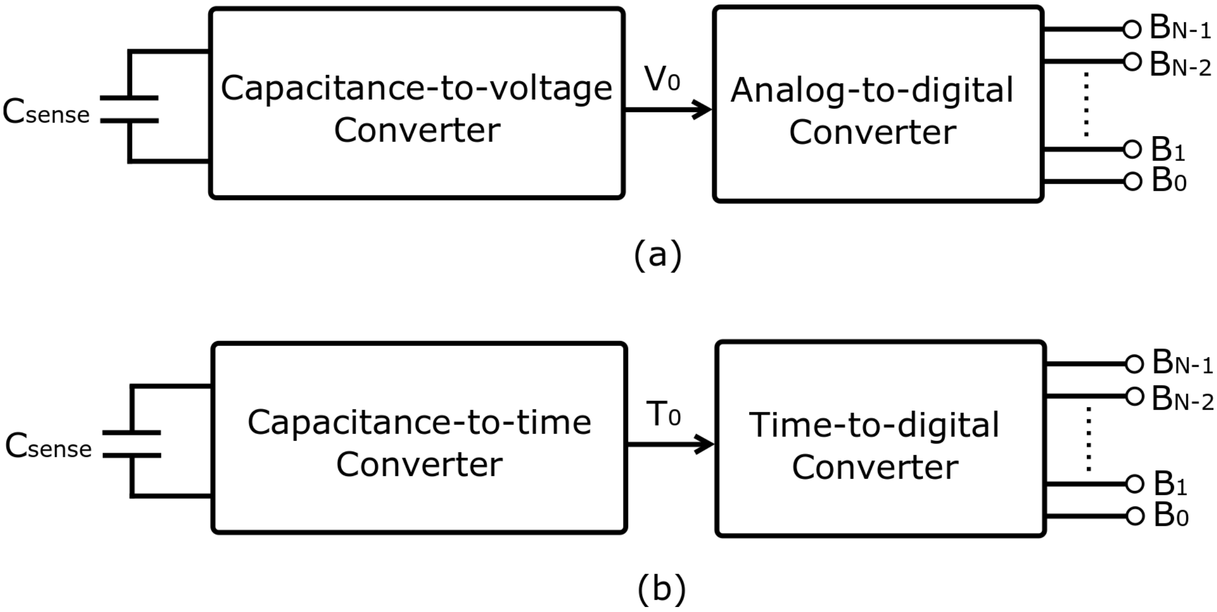


Fig. 3.5 Typical capacitance-to-digital converters architectures copied from [9]. (a) capacitance-to-voltage followed by an analog-to-digital converter; (b) capacitance-to-time followed by a time-to-digital converter.

3.3.1 Capacitance-to-voltage-to-digital

As the capacitance-to-digital converter can provide fine absolute resolution [76] and has good energy efficiency [105] in the voltage domain, the conventional design of such a converter is implemented by converting the capacitance to a voltage and then digitising the converted voltage via an analog-to-digital converter [4, 106, 107] as shown in Fig. 3.5(a). A dual-slope capacitance-to-digital converter is a common design integrating a dual-slop analog-to-digital converter [26]. Basically, the dual-slope technique converts the difference between the sensed capacitor (C_{sense}) and the base capacitor (C_{base}) [26, 108]. Fig. 3.6 shows the simplified circuit diagram of a dual-slope capacitance-to-digital converter; the charge difference between C_{sense} and C_{base} is fed to a C_{integ} when Φ_{s1} =0 and Φ_{s2} = 1 and then the charge difference is removed by iterative subtraction using C_{ref} until C_{integ} is depleted as presented below. The code is generated during the discharging time.

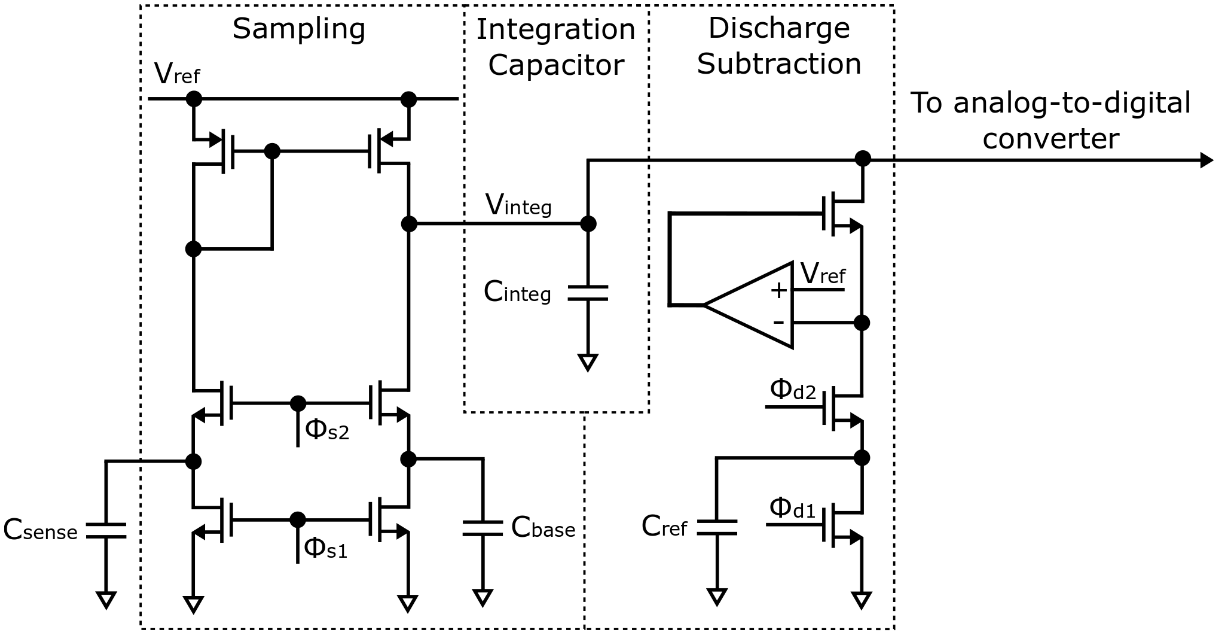


Fig. 3.6 Simplified circuit diagram of a dual slope capacitance-to-digital converter adapted from [26].

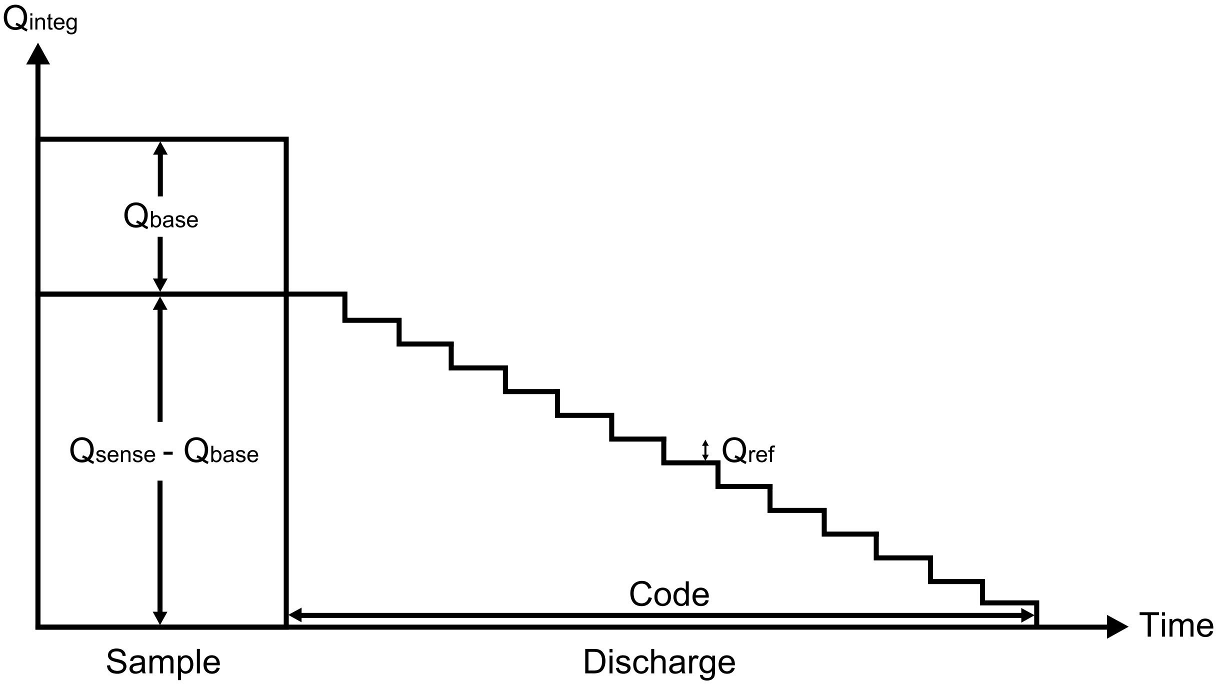


Fig. 3.7 Code generation copied from [26].

Fig. 3.7 shows the code generation with the depletion of charge. Before sampling, C_{sense} and C_{base} are fully discharged by setting Φ_{s1} =1 and Φ_{s2} = 0. During the sampling phase (Φ_{s1} =0 and Φ_{s2} = 1), the same current is generated in both sides of the current mirror, and within the same sampling period, the charge stored in C_{sense} is equal to the sum of charge stored in C_{base} and that in C_{integ}. Hence, the different charge between C_{sense} and C_{base} is the charge stored in C_{integ}, which is Q_{integ} = Q_{sense} - Q_{base}; Q_{sense}, Q_{base} and Q_{integ} are the charges on C_{sense}, C_{base} and C_{integ}, respectively. In the discharge subtraction phase, C_{integ}, starting with charge Q_{integ}, starts subtracting the constant charge Q_{ref} iteratively by switching on Φ_{d1}/Φ_{d2} alternately as shown in Fig. 3.7, and Q_{ref} is pre-stored into C_{ref} by V_{ref} through a comparator and an NMOS transistor before each subtraction cycle as shown in Fig. 3.6. Ultimately, the digital output code is the total number of discharging cycles counted by a ripple carry counter used as an analog-to-digital converter function. An example is given by [26]; the digital code is as follows:

$$Code = \frac{C_{sense}-C_{base}}{C_{ref}} \tag{3.1}$$

Thus,

$$C_{sense} = Code \times C_{ref} + C_{base} \tag{3.2}$$

where the C_{base} and the C_{ref} are known, and the code is recorded and readable.

Other dual slope capacitance-to-digital converter is reported in [109] to achieve a fast digital conversion with a high accuracy (0.05%). An energy-efficient dual slope capacitance-to-digital converter based on a dual slope analog-to-digital converter is presented in [107], which has 17-bit high resolution. Capacitance-to-voltage-digital-based capacitance-to-digital converter has various advantages such as high resolution (17 bits in [76]), energy-efficiency (1.8pJ/step in [110]), etc. However, in order to achieve the above advantages, a complicated circuit design and a larger circuit area (0.105mm^2 in [103]) may be required in the circuit design process which may result in a long conversion time (6.4ms in [26]). Therefore, the recent implementations designed in the time domain started using full digital conversion methodology for converting the capacitance to digital code as reported in [4, 27, 28, 30, 111]. This full digital capacitance-to-digital conversion approach can offer low complex circuitry, small area (0.05 mm^2 in [103]) and fast conversion time (0.945μs in [4]) [4, 30, 103]. In the following sections, the time-domain capacitance-to-digital converters related-works will be discussed.

3.3.2 Capacitance-to-period-to-digital

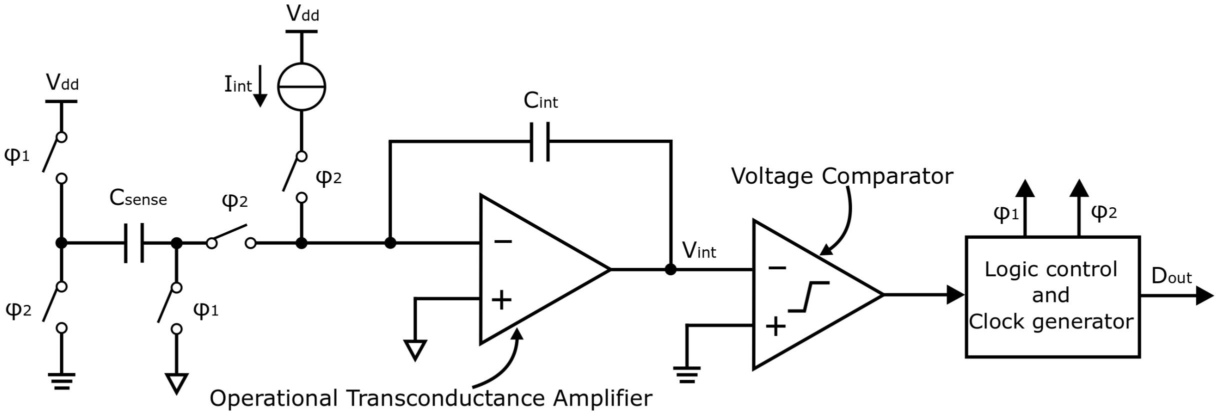


Fig. 3.8 Simplified block diagram of a capacitance-to-period-based capacitance-to-digital converter copied from [27].

One of the designs in the time domain is converting the capacitance to period, and then digitising the converted time into the digital code [27, 103, 112]. Fig. 3.8 shows a simplified block diagram of a capacitance-to-period-based capacitance-to-digital converter. It consists of a current source I_{int}, an operational transconductance amplifier used as an integrator, a voltage comparator and a logic control with the additional functionality of clock generation. During phase φ_1, the sensed capacitor (C_{sense}) is connected to the supply voltage (V_{dd}); the charge of $V_{dd} \times C_{sense}$ is charged into C_{sense}. In phase φ_2, C_{sense} is connected between the integrator and the V_{ss}, resulting in the charge of $C_{sense} \times V_{dd}$ being transferred to the integration capacitor C_{int}, as shown in Fig. 3.8, causing the output of the integrator to step up [27]. As a constant integration current source is applied, the charge stored in C_{int} is removed until the V_{int} is reduced to its original level. Fig. 3.9 shows the associated waveforms of a capacitance-to-period-based capacitance-to-digital converter [27].

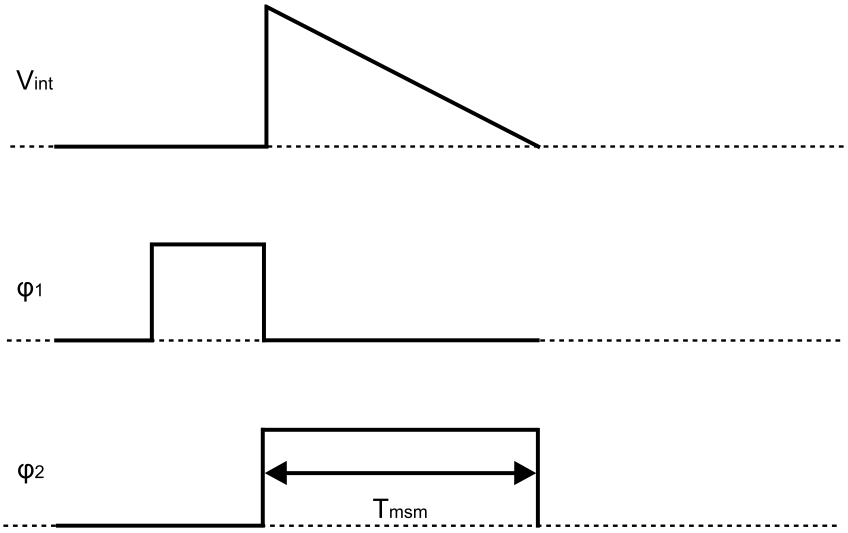


Fig. 3.9 Associated waveforms of a capacitance-to-period-based capacitance-to-digital converter copied from [27]. (Re-drawn version of Fig.1 in [27]).

A voltage comparator is used at the output of the integrator to track the operation of V_{int}, and subsequently the output of the comparator is fed to a logic control unit to generate the phases φ_1 and φ_2; in the meantime, this unit can generate the clock for digitisation, as shown in Fig. 3.9. The time interval T_{msm} is between the start of φ_2 and the point when V_{int} crosses the threshold of the comparator and is proportional to C_{sense}:

$$T_{msm} = \frac{V_{dd}}{I_{int}} \times C_{sense} \tag{3.3}$$

Thus, this time interval T_{msm} is measured and digitised by counting the number of clock cycles of the internal clock generator through the output data signal D_{out} as shown in Fig. 3.8. A digital counter can easily achieve this in a microprocessor [27]. The capacitance-to-period-based capacitance-to-digital converter is quite flexible in that the resolution can be easily tuned by applying a different clock generator during the digitalising process [43, 113]. In addition, this type can be used to converter a large input capacitance range (2000pF in [114], 300pF in [115]) with high resolution (16 bits in [114] and [115]). However, compared to the voltage conversion-based approach, the period conversion-based approach has less energy efficiency (139pJ/step in [27]) and long conversion time (100ms in [115]). The sensing completion time, or response time, is important. When sensing a changing signal, the sensing action must be fast enough in order to obtain the complete profile of the sensed signal, according to the Nyquist-Shannon sampling theorem [116]. Therefore, a fast conversion technique has been presented in [4, 28, 111] using inverter chain or oscillator to convert the capacitance to frequency for the digitising process.

3.3.3 Capacitance-to-frequency-to-digital

As mentioned in the previous section, converting capacitance to frequency is another recent method in the time domain. This section presents an example using a delay-chain discharge method; this type of capacitance-to-digital converter is a fully digital design based on monitoring the discharge process through a ring oscillator powered by a fully charged capacitor (C_{sense}). The number of discharging cycles, within the precharged voltage discharges to a known and fixed voltage (V_{ref}) is linear with the C_{sense}.

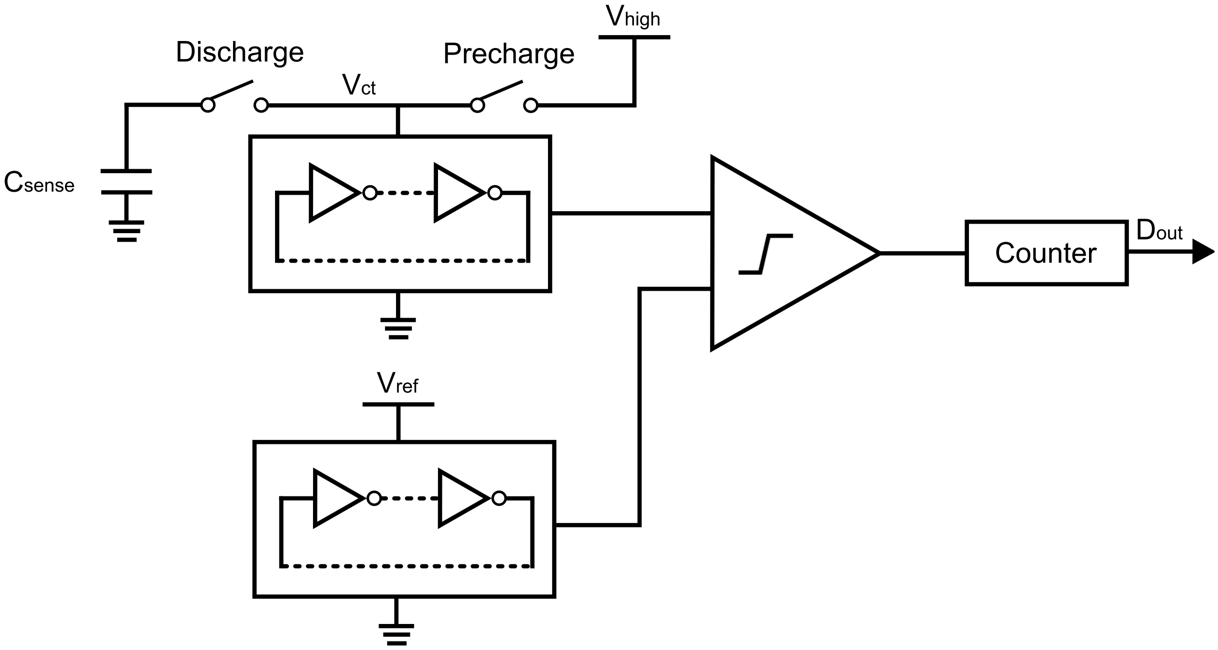


Fig. 3.10 General block diagram of a delay-chain discharge capacitance-to-digital converter adapted from [28, 29].

[28] presents an approach to detect the process of discharging from a high voltage (V_{high}) to a reference voltage (V_{ref}) as shown in Fig. 3.10. The sensed capacitor (C_{sense}) is directly connected to V_{high} by switching *Precharge* and *Discharge*, and C_{sense} is initially charged to V_{high} and discharges gradually as the oscillation of the ring oscillator by opening *Precharge*. The ring oscillator draws the charge from C_{sense}, gradually lowering the voltage on C_{sense} and resulting in the slowing down the oscillation of ring oscillator. In addition, there is another V_{ref} powered reference delay that generates a constant frequency as the applied stable V_{ref}, and then these two generated frequencies are fed to the delay comparator. A counter records the transitions of ring oscillator until the period of the V_{ct} powered ring oscillator is larger than (or equal to) the period of the V_{ref} powered ring oscillator and then outputs the code (D_{out}).

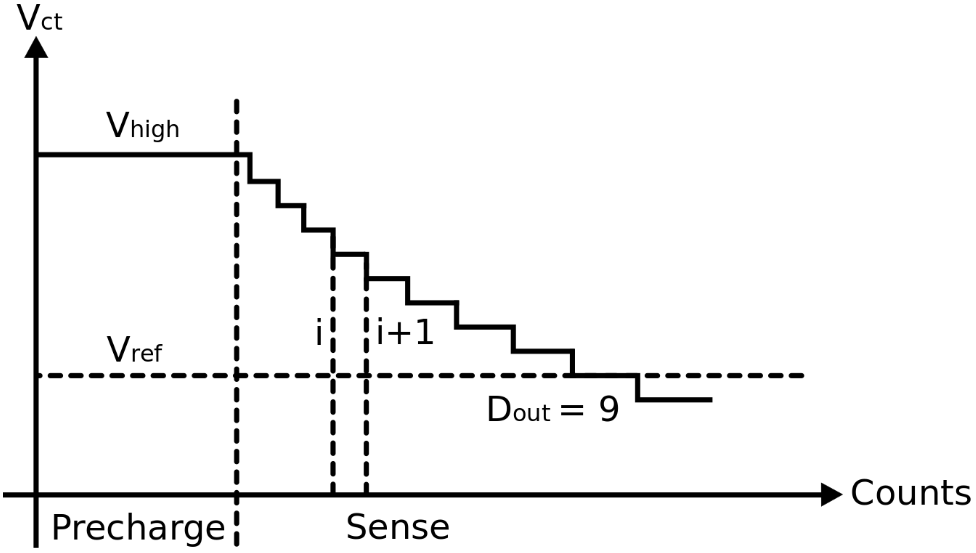


Fig. 3.11 Associated waveforms of a delay-chain discharge capacitance-to-digital converter copied from [29, 30].

D_{out} is equal to the number of transitions of ring oscillator while V_{ct} discharges from V_{high} to V_{ref}, as shown in Fig. 3.11. Q_i is equal to $V_i \times C_{sense}$ when processing to step i, and at step $i+1$, $Q_{i+1} = V_{i+1} \times C_{sense} + V_{i+1} \times C_p$ where C_p is the parasitic capacitor of the inverter chain [30]. As $Q_i = Q_{i+1}$, the following equation is determined as follows:

$$V_i \times C_{sense} = V_{i+1} \times C_{sense} + V_{i+1} \times C_p \tag{3.4}$$

Thus,

$$\frac{V_{i+1}}{V_i} = \frac{C_{sense}}{C_{sense}+C_p} \tag{3.5}$$

As $V_{i+1} = V_i \times (1-k)$, then,

$$k = \frac{C_p}{C_{sense}+C_p} \tag{3.6}$$

In addition, the discharge process is modelled by the following equation:

$$V_{low} = V_{high} \times (1-k)^n \tag{3.7}$$

where n is the number of steps taken to discharge from V_{high} to V_{ref}. Furthermore, the formula $(1-k)^n$ can be rewritten based on the Taylor series as follows:

$$(1-k)^n = (1-nk) + \frac{n\times(n-1)k^2}{2\times1} - \frac{n\times(n-1)\times(n-2)k^3}{3\times2\times1} + ... \tag{3.8}$$

If $nk << 1$, (3.8) can be shortened as $1-nk$. As V_{high} and V_{ref} are known and constant, the $(1-k)^n$ is a constant derived from (3.7). Assuming that $nk << 1$, then $1-nk$ is $constant$, and thereby $n\frac{C_p}{C_{sense}+Cp}$ is $constant$. As C_p is constant and small compared to C_{sense}, $\frac{n}{C_{sense}} = constant$, n is linearly proportional to C_{sense} [30].

This delay-chain discharge capacitance-to-digital converter technique may achieve low power consumption as it reuses the energy initially stored in the C_{sense} to power the ring oscillator. However, an additional ring oscillator delay-chain and a reference voltage are required to provide a constant reference delay time in this method, which may still increase the power consumption and complexity of the circuit.

Table 3.2 Overview of different capacitance-to-digital converters.

Type of capacitance-to-digital converter	Advantage	Disadvantage
Capacitance-to-voltage-to-digital	High accuracy (0.05% in [26]), energy-efficient (5.3pJ/step in [26], high resolution (17 bits in [76])	Long conversion time (6.4ms), large area (0.105mm^2) in [26]
Capacitance-to-period-to-digital	Large input capacitance range (2000pF in [114]), high resolution (16 bits in [115]).	Long conversion time (7.6ms), less energy-efficient (139pJ/step) in [27].
Capacitance-to-frequency-to-digital	Short conversion time (0.945 μs in [4]), energy-efficient (141fJ/step in [28])	Less resolution (11.44 bits in [30]), extra ring oscillator needed.

Table 3.2 shows the overview of different capacitance-to-digital converters. From the perspective of considering the conversion time and energy efficiency, the capacitance-to-frequency-to-digital technique is a better alternative. However, in the literature, this type of capacitance-to-digital

converter needs a stable reference voltage to power the ring oscillator. Consequently, they may be unable to operate in the energy harvesting system. In this thesis, the same concept, charging/discharging a sensed capacitor to operate a current-starved voltage-controlled oscillator, is used to design a fast energy-efficient capacitance-to-digital converter presented in Chapter 6.

3.4 Summary

This chapter reviews recently published work on voltage sensor and capacitance-to-digital converter. The limitations of each reviewed design are identified. Special emphasis is placed on the existing design of a reference-free voltage sensor without a stable V_{dd} reported in [21, 23–25] as reference points for comparison with the method presented in Chapters 4 and 5. In addition, the time domain technique can be extensively used in many areas such as capacitance-to-digital converter. Chapter 4 of this thesis presents a novel technique of this type. Some conventional designs have been presented in this chapter, and time domain capacitance-to-digital converter [4, 29, 30, 111] has been highlighted in the end, which will guide the proposed design of the capacitance-to-digital converter in Chapter 6. An expected design specifications summary of the proposed voltage sensor and the capacitance-to-digital converter is listed in 3.3.

Table 3.3 Expected design specifications of the proposed voltage sensor and capacitance-to-digital converter.

Voltage Sensor	
Fabrication technology	350nm AMS technology node
Unstable V_{dd}	0V$\sim$1.2V
Sensed voltage range	0.5V$\sim$1.2V
Frequency	Low frequency (<5kHz)
Resolution	25mV
Capacitance-to-digital Converter	
Fabrication technology	350nm AMS technology node
Operate voltage	1.8V
Predefined low voltage	1V
Sensed capacitance	7pF
FoM	Less than 100pJ/step comparted to [27]
Measurement time	Within magnitude of ms

Chapter 4

Time comparison-based voltage level-crossing sensor

4.1 Introduction

As discussed in the previous chapters, the reference-free voltage sensing technique has become a new interesting research area due to the advantages of low power, small area and no required stable voltage [21, 23, 24, 101]. This chapter proposes a new reference-free voltage level-crossing sensing technique based on time-comparison and investigates how the change of frequency in voltage-controlled oscillator as a function of V_{dd} can be used to determine the voltage level. This voltage sensing technique seeks to achieve voltage level-crossing sensing without a reference voltage in the time domain. This voltage level-crossing sensor not only detects the voltage increases but also voltage decreases using two separate threshold voltage detectors, and it can be used to detect multiple voltage levels with the support of related circuits as discussed in Chapter 5.

The proposed sensing method is based on two steps: (i) converting V_{dd} to frequency by the existing basic inverter-based voltage-controlled oscillator introduced in Chapter 2, and (ii) detecting the unique period generated by the corresponding predefined threshold voltage. In this chapter, the proposed voltage detector using a sensing technique for determining a predefined constant time delay which is equal to the period generated by the voltage-controlled oscillator when powered by the predefined voltage, which is different from the US patent [23] using a "run to death" method that depletes the restored energy on the constant capacitor and counts the depletion time using an asynchronous counter, and the counted code represents the voltage of the constant capacitor. This method cannot be directly used for detecting the crossing of arbitrary voltage levels as it essentially senses the crossing of approximately 0 volts. The proposed voltage detector in this chapter uses a constant predefined time delay applied as a time reference during the detection. Therefore, this voltage sensing technique uses a fixed time as an internal reference instead of a conventional voltage, so that the conventional reference voltage can be discarded. An arbitrary target voltage value for crossing detection can be set by setting the fixed time reference.

The remainder of this chapter is organised as follows. Section 4.2 contains the overview of the voltage level-crossing sensor and describes the function of each component in this sensor. In Section 4.3, the methodology of threshold voltage detection is presented and Section 4.4 describes the circuit implementation. Finally, conclusions complete the chapter.

4.2 Overview of time comparison-based voltage level-crossing sensor

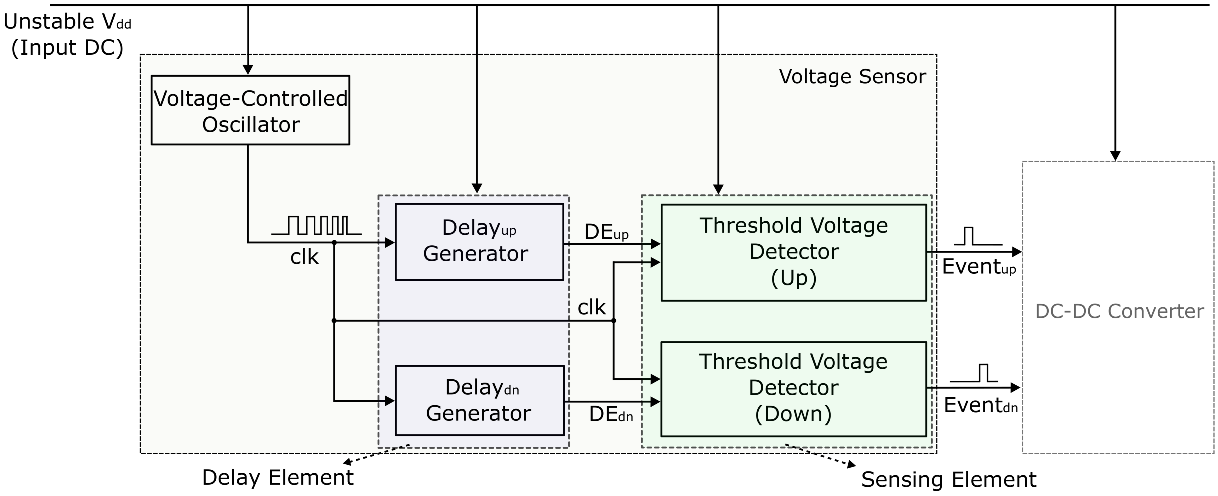


Fig. 4.1 Block diagram of the proposed time comparison-based voltage level-crossing sensor. The input is the unstable V_{dd} to be sensed known as the input DC in system, and the outputs are $Event_{up}$ and $Event_{dn}$ used to indicate the detected voltage for DC-DC converter for the voltage regulation as shown in Fig. 1.2. clk is a V_{dd}-dependent clock generated by voltage-controlled oscillator. DE_{up} and DE_{dn} are clk delayed edge by delay element used to determine the predefined threshold voltages. $Event_{up}$ and $Event_{dn}$ represent the predefined threshold voltage for voltage increases and voltage decreases, respectively, when V_{dd} crosses through the predefined threshold voltages. The predefined threshold voltages are named as V_{thup} and V_{thdn} in the example discussed below.

Fig. 4.1 shows the block diagram of the proposed time comparison-based voltage sensor. This proposed voltage sensor is powered by an unstable V_{dd}. It consists of one voltage-controlled oscillator, one delay element and one sensing element. The delay element includes one $Delay_{up}$ generator for V_{dd} increases and one $Delay_{dn}$ generator for V_{dd} decreases, respectively. Similarly, the sensing element consists of two threshold voltage detectors as well; one is used to detect V_{thup} during V_{dd} increases and other one is used to detect V_{thdn} during V_{dd} decreases. This proposed voltage level-crossing sensor will be the core element of the reference-free voltage monitoring system (in Chapter 5) to detect the crossing of multiple predefined threshold voltages, and the threshold voltage detector (down) will be the primary element of the time comparison-based capacitance-to-digital converter (in Chapter 6).

As discussed in Chapter 2, the voltage-controlled oscillator can generate a unique frequency at each powered voltage level and keep changing its frequency with the change of the V_{dd}, which means that the period of clk (T in Fig. 4.2 and Fig. 4.3) increases as the V_{dd} decreases and the increase of V_{dd} causes the decrease in the clk's period [11, 51]. The clk is the input of the delay element (See Fig. 4.1) that is an RC circuit. As the RC time constant is a voltage-independent value [16, Chapter 11, equation 11-6], the RC time constants will be used as constant time delays, $Delay_{up}$ and $Delay_{dn}$, generated from the delay element for detecting V_{thup} and V_{thdn}, respectively. These two time delays are applied to clk, when clk passes through the delay element. Two new signals are generated by the delay element, DE_{up} and DE_{dn} as shown in Fig. 4.1. These two new generated signals are the two inputs of the sensing element as shown in Fig. 4.1. In addition, clk is one input of the sensing element as well. In the sensing element, the threshold voltage detector (up) compares the DE_{up} with clk. If the rising edges of both overlap, the threshold voltage detector (up) generates an event pulse ($Event_{up}$) to represent that the predefined V_{thup} is detected (See Fig. 4.2). Similarly, the threshold voltage detector (down) generates a event pulse ($Event_{dn}$) when the rising edges of DE_{dn} and clk are overlapped. The $Event_{dn}$ pulse is used to represent the detection of V_{thdn} as shown in Fig. 4.3.

4.3 Threshold voltage detection

This section essentially introduces the theory and method of predefined threshold voltage detection. It includes two subsections; threshold voltage (V_{thup}) detection during V_{dd} rising, and threshold voltage (V_{thdn}) detection during V_{dd} falling.

4.3.1 Detect threshold voltage V_{thup} during voltage rising

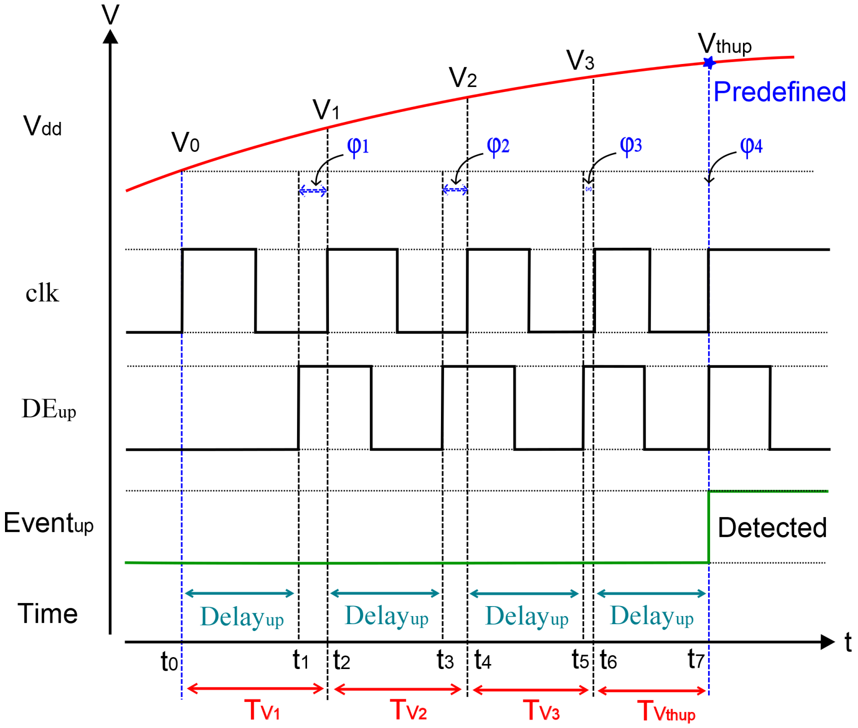


Fig. 4.2 Timing diagram of detecting V_{thup} during V_{dd} rising. $Delay_{up}$ is assumed as a constant delay between clk and DE_{up}, and it is generated by the $Delay_{up}$ generator in Fig. 4.1. V_{dd} increases from V_0 to V_{thup}.

Fig. 4.2 shows the timing diagram from the given points of the proposed threshold voltage detector (up) detailing its desired operation during V_{dd} increase. V_{thup} is a predefined threshold voltage which implies that the V_{thup} should be detected when V_{dd} increases to V_{thup} from a lower voltage, for example, from V_0 to V_{thup} in Fig. 4.2. clk and DE_{up} serve as the two inputs of the threshold voltage detector (up) (See Fig. 4.1), and the voltage crossing is detected by comparing the two time period inputs.

Assume that the system starts working at time t_0 and V_{dd} is V_0 at this moment as shown in Fig. 4.2. V_{dd} increases from V_0 to V_{thup} crossing through V_1, V_2 and V_3 in sequence. Note that the period of clk decreases as the V_{dd} increases as discussed in Section 2.2.1, Chapter 2. Therefore, in this example, as shown in Fig. 4.2, $T_{V_1} > T_{V_2} > T_{V_3} > T_{V_{thup}}$. The $Delay_{up}$ is applied to delay the generation of the rising edge of clk, resulting in generating the delayed edge DE_{up} (See Fig. 4.2). Before V_{dd} increases to V_{thup}, the predefined constant $Delay_{up}$ is less than the period of each clock of clk. For example, at time t_2, the period of clk is T_{V_1} (= t_2 - t_0), the $Delay_{up}$ is less than T_{V_1} as shown in Fig. 4.2. Similarly, when V_{dd} increases to V_2 at t_4 and to V_3 at t_6, the period of clk is T_{V_2} and T_{V_3}, and the $Delay_{up}$ is less than them. Once V_{dd} is increased to V_{thup}, the period of clk is $T_{V_{thup}}$ (= t_7 - t_6). At this moment, the predefined $Delay_{up}$ is same as $T_{V_{thup}}$, and thereby the rising edges of clk and DE_{up} overlap, resulting the $Detected$ signal to be generated in $Event_{up}$ to represent V_{thup}. This is the main principle of detecting the predefined V_{thup}.

With the increase of V_{dd}, the period of clk decreases, and thereby the phase difference φ (= $T - Delay_{up}$ in Fig. 4.2) between the rising edge of DE_{up} and the first rising edge of clk after the cycle of DE_{up} becomes shorter and shorter until it disappears. It is for this reason that the rising edges of clk and DE_{up} are likely to overlap. For example, $\varphi_1 = T_{V_1}$ - $Delay_{up}$, $\varphi_2 = T_{V_2}$ - $Delay_{up}$, $\varphi_3 = T_{V_3}$ - $Delay_{up}$ and $\varphi_4 = T_{V_{thup}}$ - $Delay_{up}$. As $T_{V_1} > T_{V_2} > T_{V_3} > T_{V_{thup}}$ and $Delay_{up}$ is a constant value, the relationship between the φs should be $\varphi_1 > \varphi_2 > \varphi_3 > \varphi_4$. Eventually, φ_4 approximately becomes zero as the T_{V_1} decreases to $T_{V_{thup}}$ and $Delay_{up}$ is predefined as $T_{V_{thup}}$. Therefore, at t_7, $T_{V_{thup}}$ and $Delay_{up}$ become same, and $T_{V_{thup}}$ is the period when V_{dd} increases to V_{thup}. In other words, when φ approximately decreases to '0', the predefined V_{thup} is approximately achieved as shown in Fig. 4.2. Therefore, the constant $Delay_{up}$ is a kind of reference time to determine the predefined V_{thup}. It is clear from this figure that the reference time should be set to $Delay_{up} = T_{V_{thup}}$ to detect V_{thup}. To summarise, to detect any predefined threshold voltage, the reference time is set to the clock period corresponding to that voltage.

4.3.2 Detect threshold voltage V_{thdn} during voltage falling

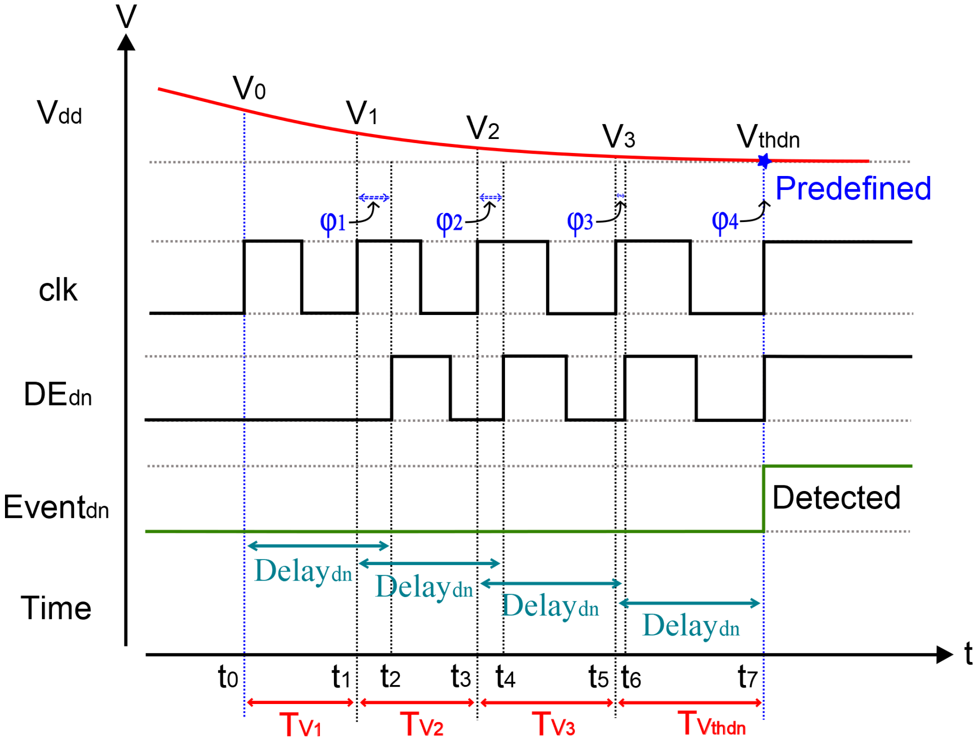


Fig. 4.3 Timing diagram of detecting V_{thdn} during V_{dd} decreases. $Delay_{dn}$ is a constant delay between clk and DE_{dn}, and it is generated by the $Delay_{dn}$ generator in Fig. 4.1. V_{dd} decreases from V_0 to V_{thdn}.

Fig. 4.3 shows the timing diagram of predefined V_{thdn} detection when V_{dd} falls. V_{thdn} is a predefined threshold voltage which means that the V_{thdn} should be detected when V_{dd} decreases to V_{thdn} from a higher voltage. For example, from V_0 to V_{thdn} in Fig. 4.3.

Similarly, the threshold voltage detector (down) (See Fig. 4.1) also compares the two inputs, clk and DE_{dn}, and there is a constant delay $Delay_{dn}$ between these two inputs which is a reference time (Explained in Section 4.3.1) to detect V_{thdn} in this example. As explained previously, a decrease in the V_{dd} will result in an increase in period of clk. Therefore, the period of clk, $T_{V_1} < T_{V_2} < T_{V_3} < T_{V_{thdn}}$ in Fig. 4.3 which is opposite to V_{thup} detection in Fig. 4.2. In addition, the reference time $Delay_{dn}$ is different to the reference time $Delay_{up}$ in V_{thup} detection. Here, the $Delay_{dn}$ is greater than one cycle of period of clk and less than two cycles of period of clk (See Fig. 4.3) as the period increases with the decrease in V_{dd} which is different from $Delay_{up}$ as shown in Fig. 4.2.

As can be seen in Fig. 4.3, V_{dd} is V_0 at t_0, and V_{dd} decreases from V_0 to V_{thdn} crossing through V_1, V_2 and V_3 in sequence. As the period of clk increases and $Delay_{dn}$ is constant, the phase difference φ (= $Delay_{dn} - T$ in Fig. 4.3) decreases. Once the V_{dd} crosses through V_{thdn}, the period ($T_{V_{thdn}}$) of clk at V_{thdn} overlaps with $Delay_{dn}$ and φ approximately equals to zero ($\varphi_4 \approx 0$ as shown in Fig. 4.3), which is same as V_{thup} detection such that $Dealy_{up} = T_{V_{thup}}$ at the stop event. In the meantime, the $Detected$ signal is generated in $Event_{dn}$ which implies that the predefined V_{thdn} is detected at t_7. Therefore, similarly, the reference time $Delay_{dn}$ should be set to the clock period corresponding to the predefined V_{thdn}.

For both rising and falling threshold detection, it is possible to have non-ideal cases where a clock edge does not coincide with φ=0. In such cases, up to one more period of clk is required to register the fact that the threshold voltage has been crossed.

4.4 Circuit implementation

This proposed reference-free time comparison-based voltage level-crossing sensor is implemented on AMS 350nm CMOS technology.

4.4.1 Basic inverter-based voltage-controlled oscillator

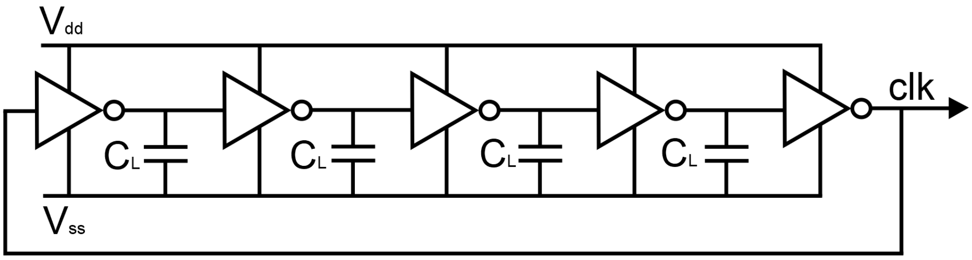


Fig. 4.4 Circuit diagram of the basic inverter-based voltage-controlled oscillator adapted from [11, 31]. The function of the proposed voltage-controlled oscillator is used to generate a V_{dd}-dependent clk.

This proposed voltage level-crossing sensor targets low frequency detection to verify the proposed sensing mechanism. The frequency range selected is below 5KHz in the experiment. Meanwhile, as this proposed voltage level-crossing sensor is designed to sense unstable V_{dd} as shown in Fig. 4.1. Therefore, the structure of basic type inverter-based ring oscillator whose generated output frequency (*clk* in Fig. 4.4) is related to V_{dd} [32, 84] is a suitable choice for my purpose.

The design of this voltage-controlled oscillator is adapted from [11, 31] as shown in Fig. 4.4. This voltage-controlled oscillator is a single-ended delay stages ring oscillator powered by sensed V_{dd}, and it consists of five basic inverters with the output of the fifth stage fed back to the input of the first one as shown in Fig. 4.4. C_L is added to limit the output frequency [88]; based on the simulation results, the value of C_L is 430pF.

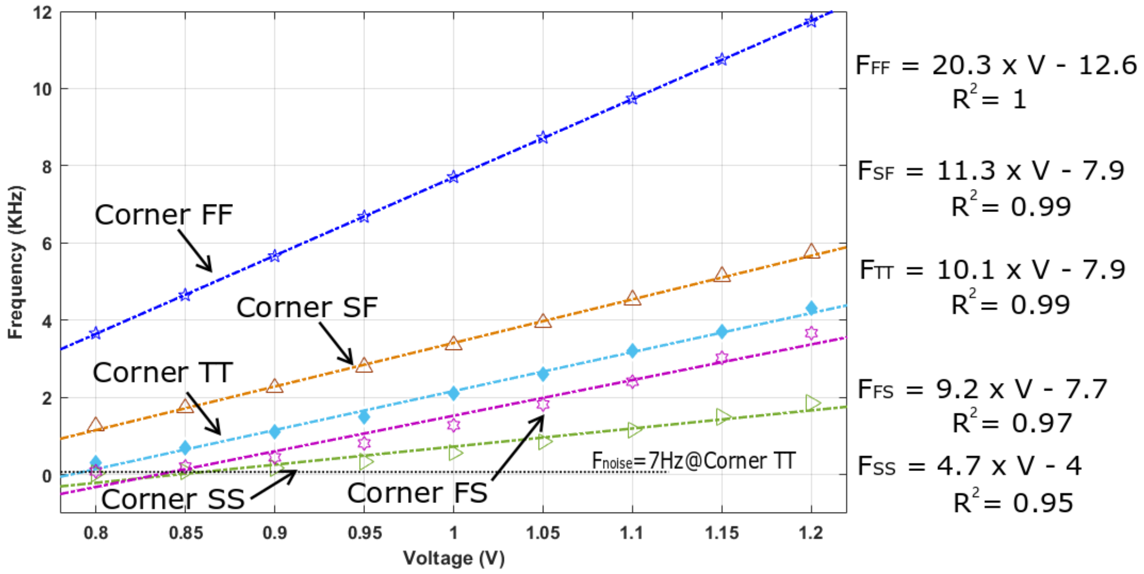


Fig. 4.5 Curve fitting of V_{dd}-dependent frequency in different corners. V_{dd} is increased from 0.8V to 1.2V. The generated frequency of TT corner is increased from 0.3KHz @0.8V to 4.3KHz @1.2V.

According to Fig. 4.5, going by the TT corner, the generated frequency equation in cadence can be used to determine the reference time *Delay* due to the good linearity. $R^2 = 0.99$ as shown in Fig. 4.5. The *Delay* can be easily determined by Equation 4.1.

$$F_{TT} = 10.1 \times V - 7.9 \tag{4.1}$$

where F_{TT} is the V_{dd}-dependent frequency (kHz) of TT corner. V is sensed V_{dd}(V).

According to 4.1, the calculated period can be determined as shown in Table 4.1. This calculated period is used to predefine the *Delay* during voltage sensing.

Table 4.1 Calculated period according to Equation 4.1.

V_{dd} (V)	Calculated Period (ms)
1.2	0.239
1.175	0.254
1.15	0.272
1.125	0.292
1.1	0.315
1.075	0.342
1.05	0.374
1.025	0.413
1	0.461
0.975	0.522
0.95	0.602
0.925	0.709
0.9	0.864
0.875	1.106
0.85	1.530

Because of the internalisation of reference, the quantitative behaviour of such a voltage-controlled oscillator is dependent on process variations. As shown in Fig. 4.5, different corners produce different versions of equation 4.1 with different coefficients. This indicates that sensors based on this type of internal time reference require calibration before or during use. The need for calibration is a necessary price to pay for not requiring stable V_{dd} and not requiring external references.

4.4.2 Single delay generator

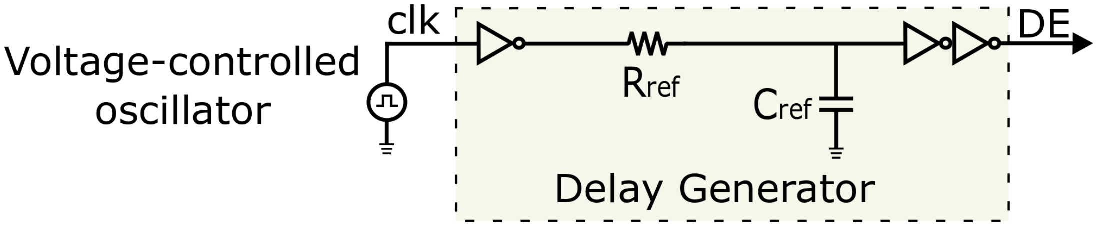


Fig. 4.6 Circuit diagram of delay generator. The function of the delay generator is to generate a RC time constant.

Since there is no stable V_{dd} during voltage sensing, the generated delay should be voltage-independent. The RC time constant generation is used to design the delay generator because of voltage-independence as introduced in Chapter 2 which will be confirmed through the experiments below. As shown in Fig. 4.6, the V_{dd}-dependent *clk* is fed to the delay generator via an inverter. The reason to invert *clk* is that there is no need to sense the entire period of *clk* when V_{dd} reaches the predefined threshold voltage; sensing the half period of *clk* can also determine the predefined threshold voltage because the half period is known due to the known entire period of *clk* when V_{dd} reaches the predefined threshold voltage. The equation of the constant delay time can be adapted from Equation 2.8 as illustrated below:

$$Delay \approx k \times R_{ref} \times C_{ref} + Delay_{inverter} \tag{4.2}$$

where $Delay$ is the delayed time (reference time); R_{ref} and C_{ref} are resistance and capacitance, respectively, used in the RC circuit to generate the required time constant. C_{ref} is equal to 1.4nF in this delay generator example, but can be tuned to other values given implementation considerations such as available silicon area, sensor response time, sensor resolution, etc. k is the coefficient of generating the delay at each voltage level in a given digital circuit. The value of k can be measured from the experiment. The $Delay_{inverter}$ is the delay time generated from those three inverters in Fig. 4.6.

In this design, the assumption is that the RC time constant is independent of the unstable V_{dd}. In other word, the delayed time ($Delay$) should be constant against the V_{dd}. In addition, due to the extra three inverters added, the final may be impacted by the V_{dd}. Therefore, a verification experiment was conducted to verify the generation of the constant delay time. The experiment involved testing the same sets of RC values under different V_{dd} and then checking the difference in time delay generated due to the voltage difference.

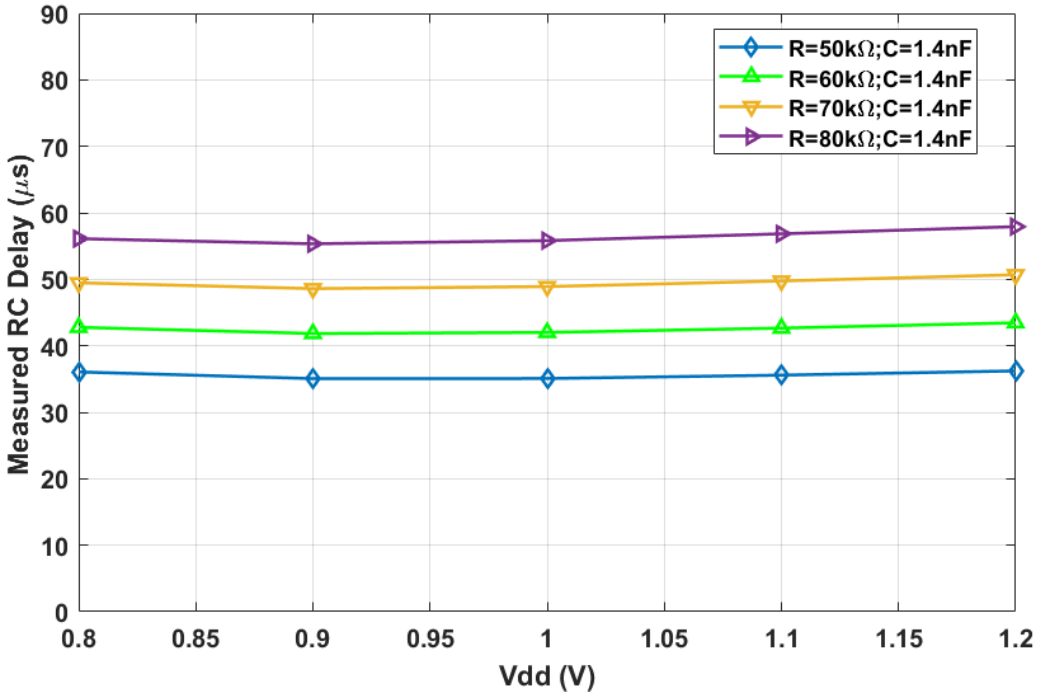


Fig. 4.7 Verification of RC delay time under different V_{dd}s. This figure presents simulated results to prove the stability of the constant delay time generated by the RC circuit under different V_{dd}s.

Fig. 4.7 shows the delay time against V_{dd} applying different values of resistor with the same value of capacitor (1.4nF). V_{dd} increases from 0.8V to 1.2V with 0.1V increment, and the resistances are 50kΩ, 60kΩ, 70kΩ and 80kΩ, respectively. The results show that the generated delay time remains almost constant with different RC values. Hence, the delay generated from the extra three inverters can be ignored during the generation of the constant delay time. According to Equation 2.8, the τs are equal to 70μs, 84μs, 98μs and 112μs, corresponding to the values of R as shown in Table 4.2. It has been shown that the value of k is approximately 0.5 regardless of the values of V_{dd} and R.

Table 4.2 Data for verification of constant delay time.

V_{dd} (V)	R ($k\Omega$)	C (nF)	τ (μs)	$Delay$ (μs)	$k = Delay / \tau$
1.2	50	1.4	70	36.22	0.52
1.2	60	1.4	84	43.46	0.52
1.2	70	1.4	98	50.68	0.52
1.2	80	1.4	112	57.92	0.52
1.1	50	1.4	70	35.58	0.51
1.1	60	1.4	84	42.67	0.51
1.1	70	1.4	98	49.75	0.51
1.1	80	1.4	112	56.85	0.51
1	50	1.4	70	35.08	0.51
1	60	1.4	84	42	0.5
1	70	1.4	98	48.91	0.5
1	80	1.4	112	55.82	0.5
0.9	50	1.4	70	35.06	0.5
0.9	60	1.4	84	41.84	0.5
0.9	70	1.4	98	48.6	0.5
0.9	80	1.4	112	55.34	0.49
0.8	50	1.4	70	36.07	0.52
0.8	60	1.4	84	42.78	0.51
0.8	70	1.4	98	49.47	0.5
0.8	80	1.4	112	56.11	0.5

Due to the constant value of k and small delay difference generated from inverters, the Equation 4.2 can be rearranged as follows:

$$Delay \approx k \times R_{ref} \times C_{ref} \tag{4.3}$$

where k is equal to 0.5. The estimated R_{ref} is shown in Table 4.3.

Table 4.3 Estimated R_{ref} according to Delays.

Predefined threshold voltage (V)	Estimated R_{ref} ($k\Omega$)	*Delay* (ms) = Period / 2 (calculated from Table 4.1)
1.2	170	0.119
1.175	182	0.127
1.15	194	0.136
1.125	208	0.146
1.1	226	0.158
1.075	244	0.171
1.05	268	0.187
1.025	296	0.207
1	330	0.231
0.975	372	0.261
0.95	430	0.301
0.925	508	0.355
0.9	618	0.432
0.875	790	0.553
0.85	1092	0.765

4.4.3 Threshold voltage detector (up)

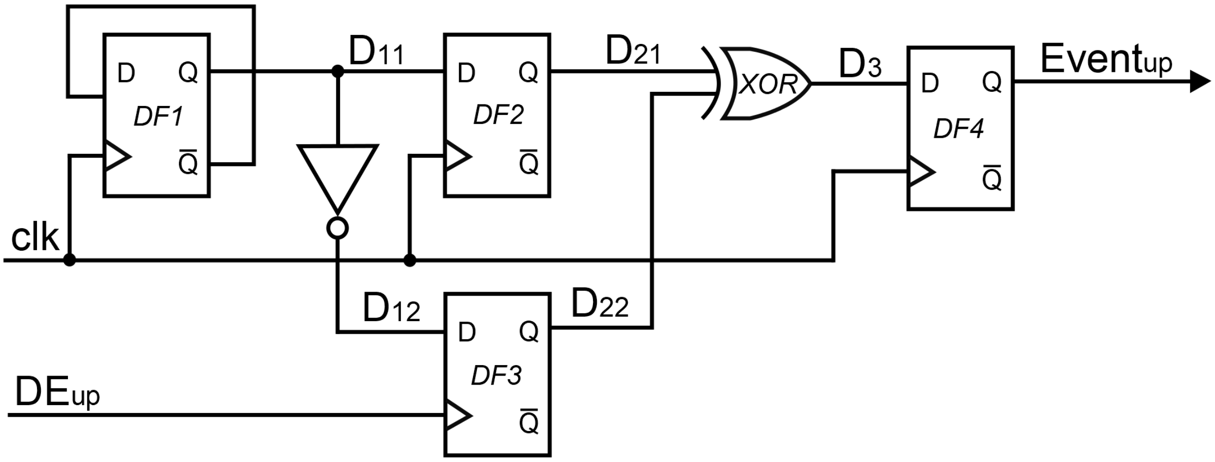


Fig. 4.8 Circuit diagram of the proposed threshold voltage detector (up). The function of this proposed voltage detector is to achieve the methodology of voltage detection shown in Fig. 4.2.

The proposed threshold voltage detector (up) for voltage increase detection is shown in Fig. 4.8. The design of this detector is based on the 'Shadow Register' approach, and is derived from the structure of the phase detector (PD) reported in [118]. This resulting threshold voltage detector (up) consists of four D Flip-Flops (*DF*s), one inverter and one XOR Gate. On the left is *DF*1 which is a data source. It is used to store and toggle the data along with *clk*. The second

*DF*2 immediately to the right of *DF*1 is used to store the value at the positive edge of *clk*. The *DF*3 is located at the bottom of *DF*2. This D flip-flop is designed as a shadow register and is used to capture the inverted data (D_{12}) at the positive edge of the reference time delayed edge (DE_{up}). Finally, these two outputs (D_{21} and D_{22}) are compared by passing through the XOR Gate, and the comparison result is captured by *DF*4; in the meantime, the event signal ($Event_{up}$) is generated. A detection example is illustrated in Fig. 4.9, which describes the detection of a threshold voltage based on the predefined $Delay_{up}$ during voltage increases. Meanwhile, the mechanism of detecting a threshold voltage during voltage decreases can be designed by the same principle. Here, the internal $Delay_{up}$ is related to the predefined threshold voltage (V_{thup}) as explained in Section 4.3.1.

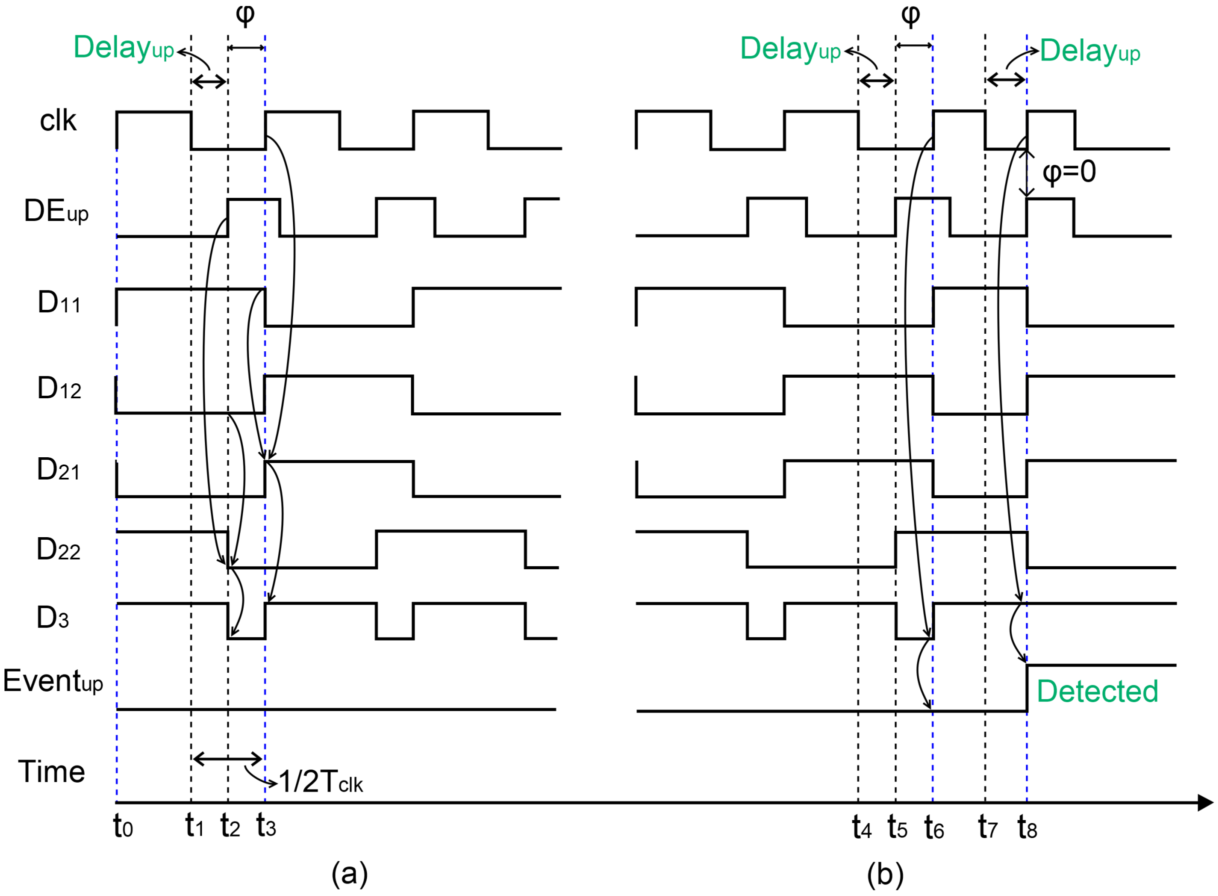


Fig. 4.9 Timing diagram of operation of the proposed threshold voltage detector (up). a. Non-detected waveforms during the threshold voltage detection; b. Detected waveforms during the threshold voltage detection.

As mentioned in Section 4.4.2, there is no need to detect the entire period of *clk*; detecting half the period of *clk* can also determine the predefined threshold voltage. Fig. 4.9a shows that the phase difference φ is generated because $Delay_{up}$ is less than $1/2T_{clk}$ of *clk* at t_3. For this φ, the formed window D_3 is pulled down and is captured by *clk*; thereby, the $Event_{up}$ signal is not generated. In other words, the frequency does not change beyond the predefined range, which means that *clk* remains the same (non-changed voltage), or the change is too small (kept in a certain range). The window D_3 is formed by D_{21} and D_{22} with logic low after passing through the XOR gate, in which *clk* will be sitting inside, without setup and hold violations.

Consequently, the event signal is low, which indicates that the targeted voltage is not detected. D_{21} is generated as the positive edge of clk captures D_{11} as shown in Fig. 4.9. At t_0, clk captures the previous state (logic '0') of D_{11}, resulting in D_{21} changing to low, and D_{11} at t_3 is logic '1' resulting in a logic '1' in D_{21}. D_{22} is generated by the positive edge of DE_{up} which captures D_{12} (inverted D_{11}) as shown in Fig. 4.9. For example, at t_2, DE_{up} captures the state of D_{12} resulting in the logic '0' in D_{22}.

Note that the positive edge of clk is getting closer to the DE_{up} with the increase in V_{dd} as the frequency increases. Fig. 4.9b shows the detected waveforms of the threshold voltage detection. $1/2T_{clk}$ changes and approaches the predefined value ($Delay_{up}$) and thereby the φ decreases. Eventually, clk and DE_{up} rise simultaneously, and φ reduces to zero. Once φ becomes zero, the window D_3 disappears, and clk can only capture the logic '1' from D_3. Subsequently, the $Event_{up}$ signal generates a logic '1' which indicates the detection of the predefined threshold voltage as shown in Fig. 4.9b at t_8.

4.4.3.1 Simulation results of V_{thup} detection

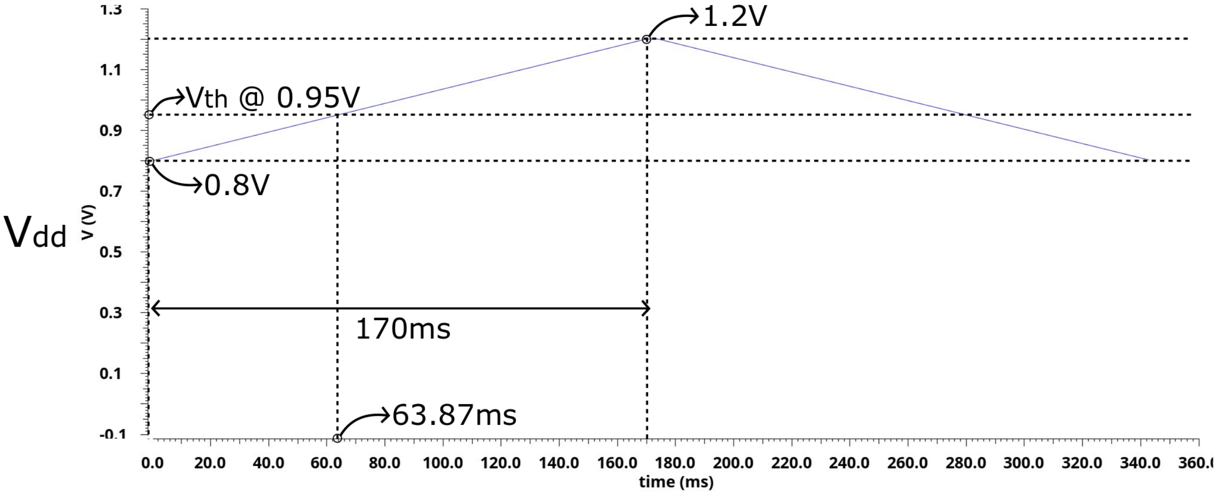


Fig. 4.10 V_{dd} waveform over time. In this experiment, V_{dd} increases from 0.8V to 1.2V in 170ms. The predefined threshold voltage is 0.95V, and the $Delay_{up}$ is equal to 0.301ms.

Having introduced the aforementioned design approaches, a simulation was conducted for illustrative purpose, and the results are depicted in Fig. 4.11. The predefined V_{thup} is 0.95V as a example in this simulation, the $Delay_{up}$ is 0.301ms as shown in Table. 4.3 and the calculated period of clk is 0.602ms when V_{dd} reaches 0.95V as shown in Table 4.1. Therefore, once 0.95V is detected, the period of clk should be approximately equal to 0.602ms.

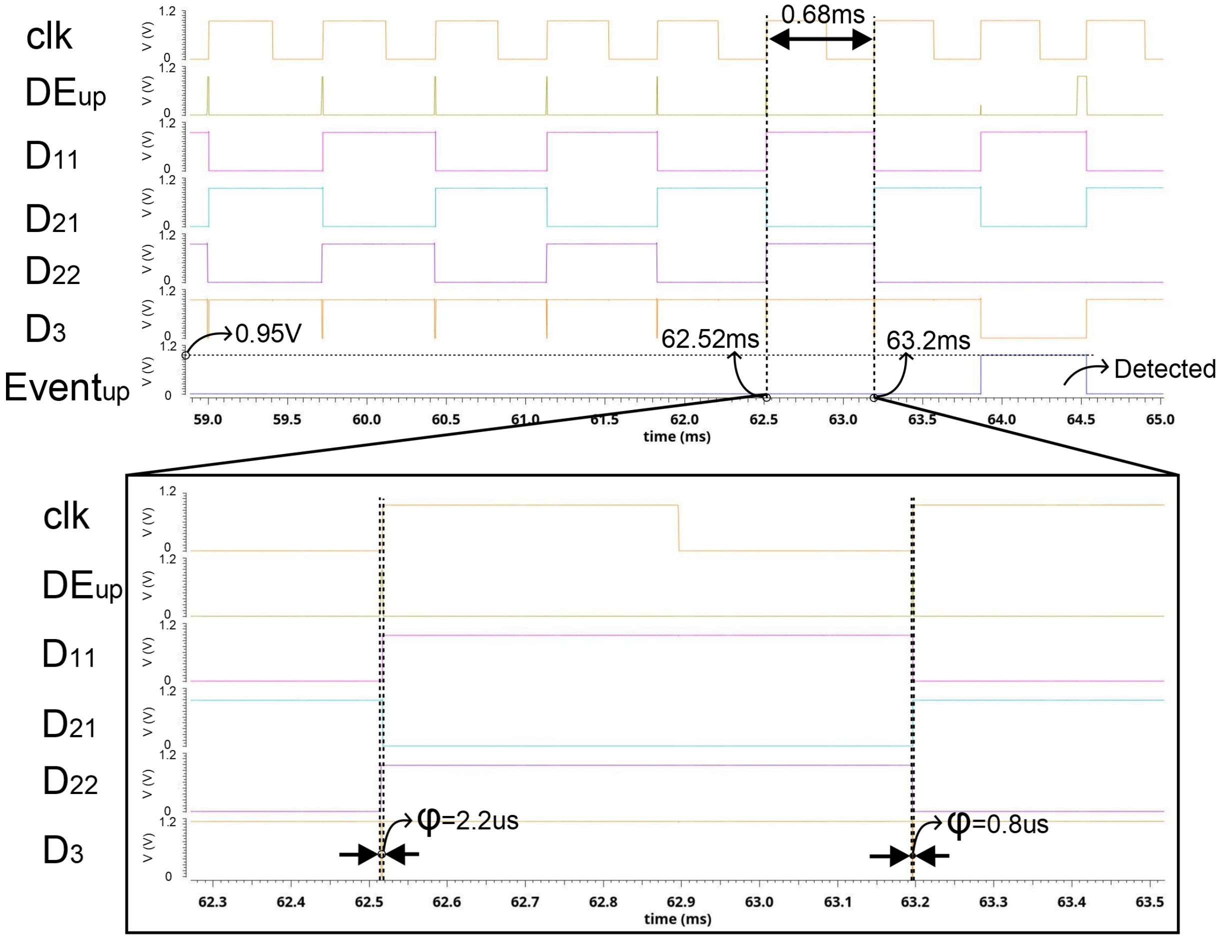


Fig. 4.11 Simulated operation of the threshold voltage detector (up). The zoomed-in figure shows the detected period. φ is decreased from 2.2μs to 0.8μs which becomes shorter and is detected as discussed in Section 4.3.1.

Fig. 4.11 shows that the detected signal is generated in $Event_{up}$ when V_{dd} almost reaches 0.95V. Due to the processing latency during the detection, the $Event_{up}$ pulse cannot be generated at the proper predefined $Delay_{up}$ as described in theory. The detected period in the schematic simulation is shown in Table 4.4. The comparison between the detected period in schematic simulation and the calculated period is shown in Fig. 5.22. This figure also shows the comparison between the detected period in post simulation and in chip test.

Table 4.4 Detected period in schematic simulation.

Predefined threshold voltage (V)	Detected Period (ms)
1.2	0.233
1.175	0.250
1.15	0.270
1.125	0.294
1.1	0.321
1.075	0.353
1.05	0.392
1.025	0.439
1	0.5
0.975	0.575
0.95	0.68
0.925	0.808
0.9	0.99
0.875	1.26
0.85	1.68

4.4.4 Threshold voltage detector (down)

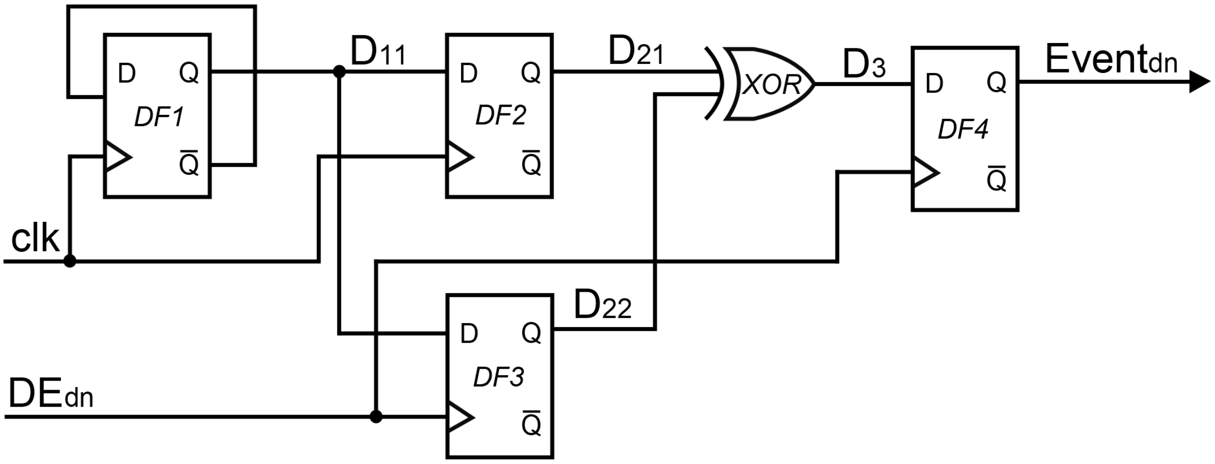


Fig. 4.12 Circuit diagram of proposed threshold voltage detector (down). The function of this proposed voltage detector is to achieve the methodology of voltage detection shown in Fig. 4.3.

Fig. 4.12 shows the circuit diagram of the proposed threshold voltage detector (down). The design of this detector is similar to the design of threshold voltage detector (up) as shown in Fig. 4.8. Comparing these two threshold voltage detectors, differences can be found in two aspects: first is the stored value for DF_3. In Fig. 4.8, the stored value of DF_3 is inverted D_{11}. However, here this value is D_{11} generated from DF_1 as shown in Fig. 4.12. The second is the trigger signal of DF_4, for the threshold voltage detector (down); DF_4 is triggered by DE_{dn} as shown in Fig. 4.12, but in threshold voltage detector (up), *clk* is used to trigger DF_4 (See Fig. 4.8). Other than these, the rest are unchanged.

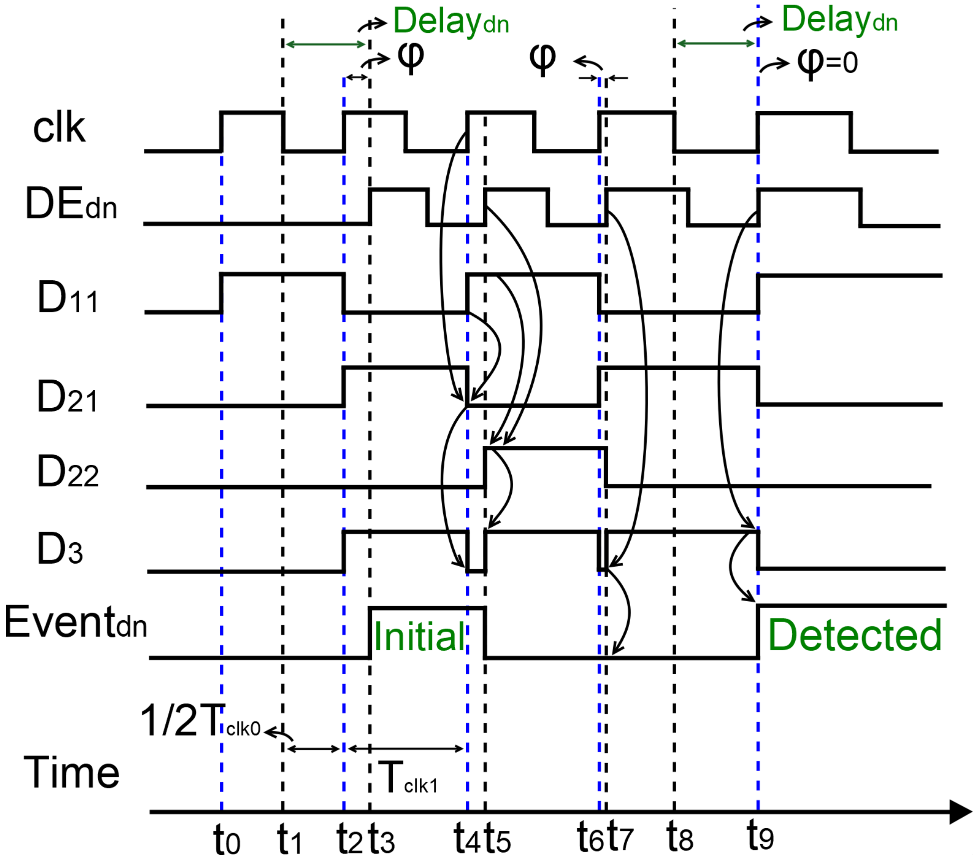


Fig. 4.13 Timing diagram of operation of the proposed threshold voltage detector (down). Detected waveform during the threshold voltage detection is shown here.

Fig. 4.13 provides an example operation of the threshold voltage detector (down). With decrease in V_{dd}, the period (T_{clk}) of *clk* increases, as shown in Fig. 4.13. The period of *clk* is T_{clk} with initial value T_{clk0} ($= t_2 - t_0$) and next period is T_{clk1} ($= t_4 - t_2$) as shown in Fig. 4.13. $Delay_{dn}$ is set according to $1/2T_{clk0} < Delay_{dn} < 1/2T_{clk0} + T_{clk1}$ due to the half period detection presented in Section 4.3 and Section 4.4.2. Initially, when the first pulse of DE_{dn} is generated at t_3, *clk* is already in the second period. At this point $D_{22} = \overline{D_{21}}$ and D_3 = '1', resulting in generating an initial pulse (*Initial*) in $Event_{dn}$. This only happens once when the threshold voltage detector (down) is initialising. Subsequently, in general, at the point of sampling by DE_{dn}, D_3 = '0' because $\varphi >$ '0', and D_{22} is delayed by φ after D_{21}, resulting in $D_{22} = D_{21}$. As T_{clk} increases, eventually $1/2T_{clk} = Delay_{dn}$, φ = '0' and the rising edge of DE_{dn} catches up with that of *clk* at t_9. At this point D_3 = '1', because $D_{22} = \overline{D_{21}}$. Therefore, the positive edge of DE_{dn} catches this '1' resulting in a *Detected* pulse generated in $Event_{dn}$ which indicates the detection of the predefined threshold voltage as shown in Fig. 4.13 at t_9.

4.4.4.1 Simulation results of V_{thdn} detection

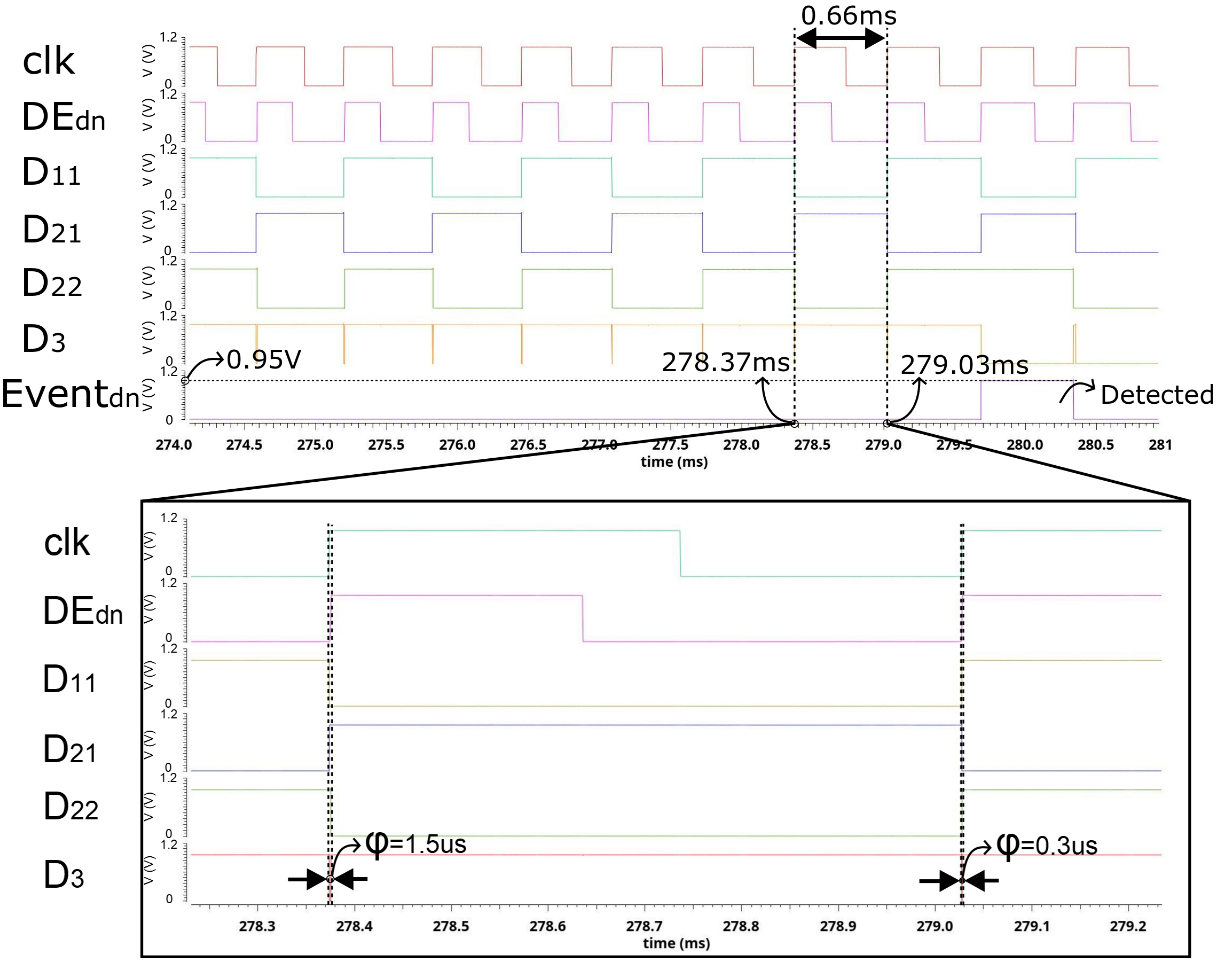


Fig. 4.14 Simulated operation of the threshold voltage detector (down). The zoomed-in figure shows the detected period. φ decreases from 1.5μs to 0.3μs becoming shorter and is detected as discussed in Section 4.3.2.

In the simulation results of V_{thdn} detection, the predefined threshold voltage is 0.95V as shown in Fig. 4.14 which is the same as V_{thup} detection in Section 4.4.3.1. The V_{dd} waveform is same as the V_{thup} detection. However, the V_{thdn} is detected when V_{dd} decreases. Fig. 4.14 shows the *Detected* signal which is generated to represent the V_{dd} which already reached the predefined 0.95V. Overall, the threshold voltage detection does not influence V_{thup} detection or V_{thdn} detection. The detected signal can be generated to represent the predefined threshold voltage within next cycle when the positive edges of *clk* and *DE* are overlapped. Fig. 4.15 shows the detection of 0.95V during V_{dd} increases and decreases.

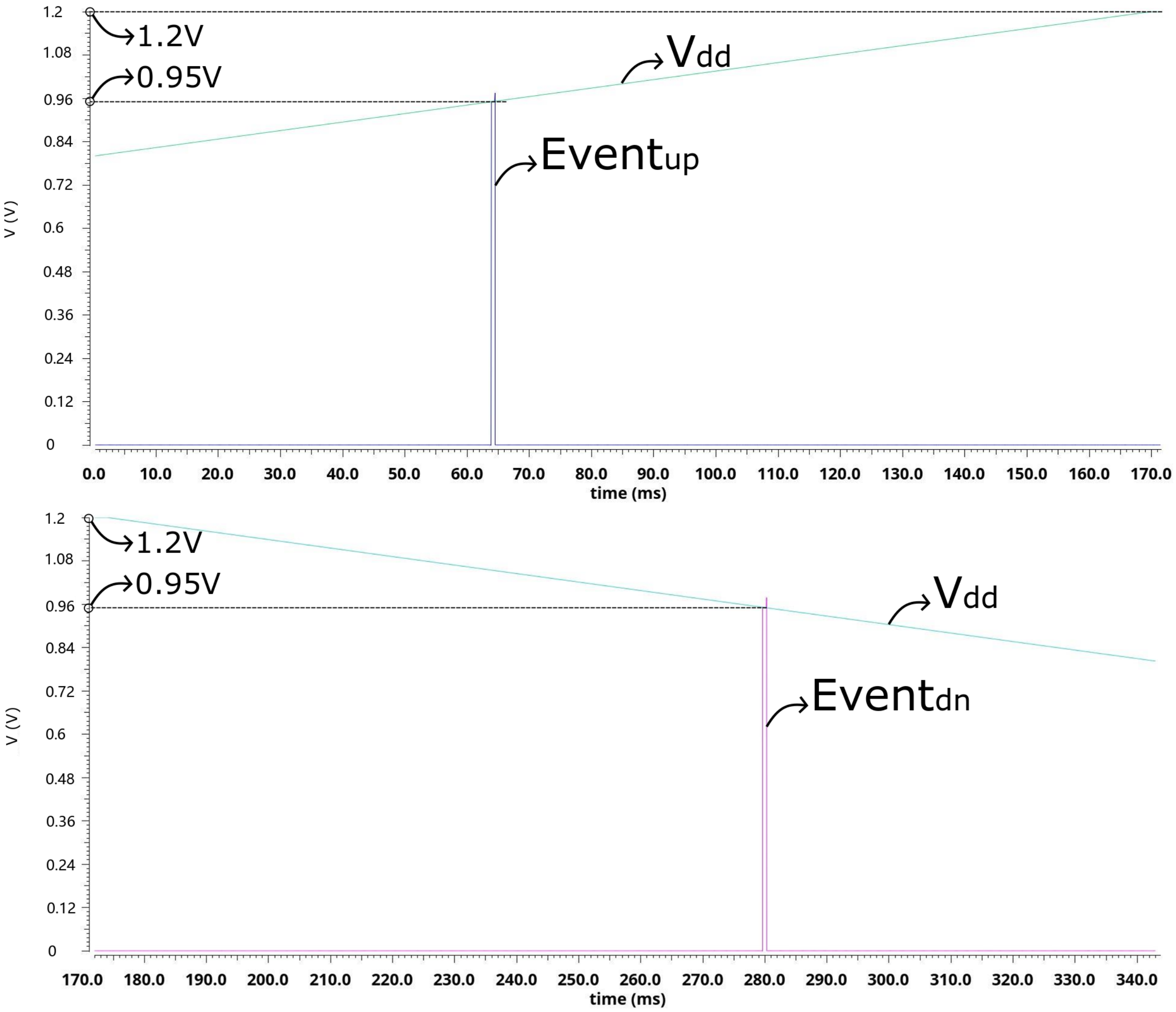
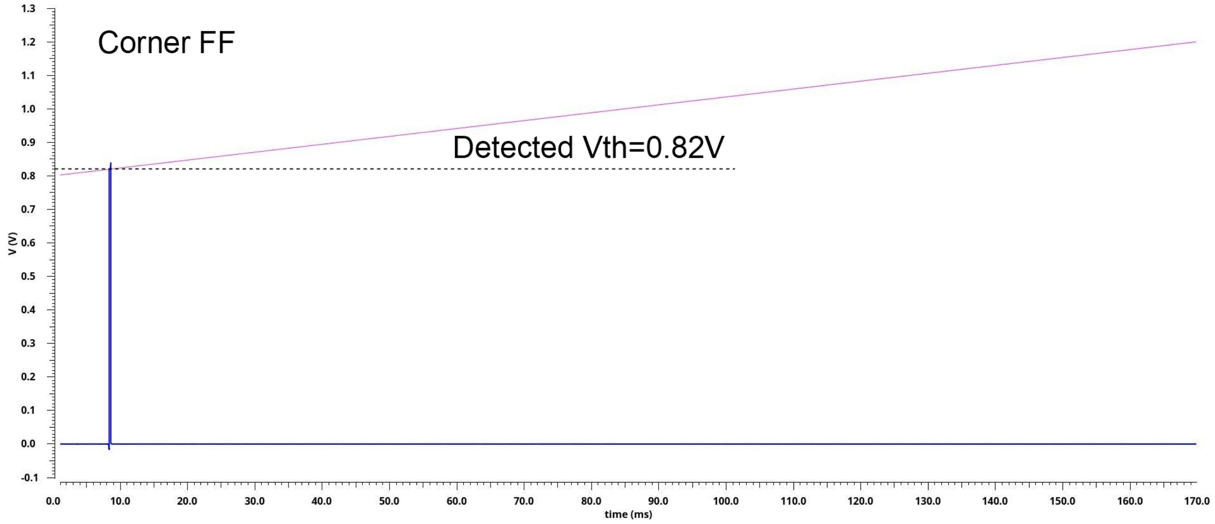


Fig. 4.15 Detection of 0.95V during V_{dd} increases and decreases.

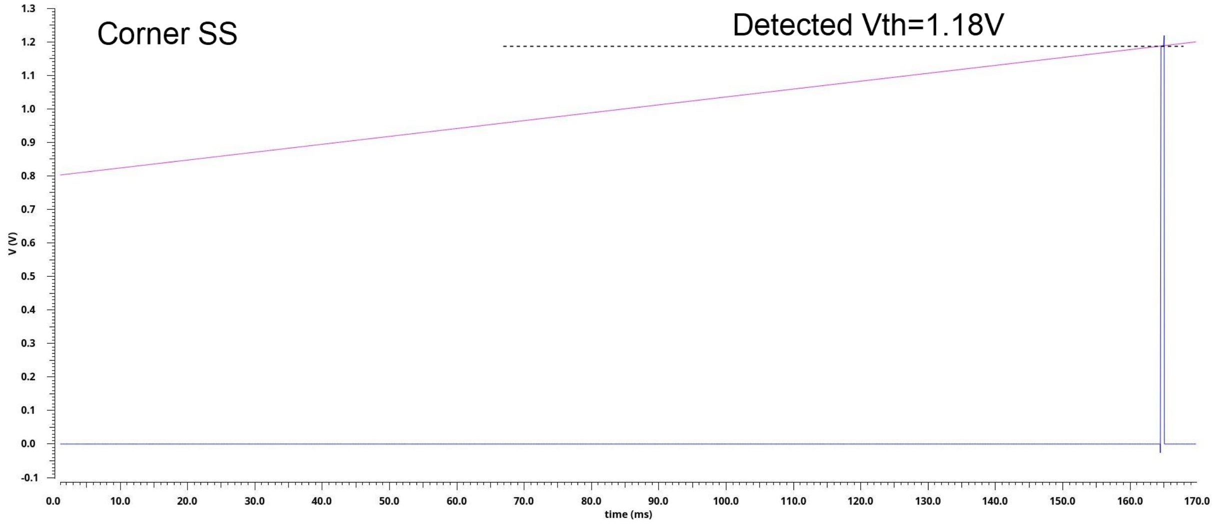
4.4.5 Process variations

The process variations may affect the final threshold detection in the proposed voltage level-crossing sensor. Therefore, the effect of the process on the proposed voltage level-crossing sensor are investigated with different process corners. The simulation showed the maximum variation at FF (Fast NMOS and Fast PMOS) and SS (Slow NMOS and Slow PMOS) corners when detecting 0.95V. Fig. 4.16 shows the corner simulations of proposed voltage level-crossing sensor for detecting 0.95V. The deviation from the detected level of 0.95V on the typical corner is 130mV less than 0.95V for the FF corner and 230mV more than 0.95V for the SS corner.

This further confirms that the internalisation of references causes them to be dependent on PVT variations. These types of sensors therefore require post-manufacture calibration [8].



(a) Detected V_{th} is 0.82V in corner FF.



(b) Detected V_{th} is 1.18V in corner SS.

Fig. 4.16 Corner simulations of proposed voltage level-crossing sensor for detecting predefined V_{th} = 0.95V at typical corner. (a) In FF corner simulation, the detected voltage level is 0.82V less than the predefined 0.95V. (b) In SS corner simulation, the detected voltage level is 1.18V larger than the predefined 0.95V.

4.5 Conclusion

In this chapter, a new voltage sensing technique based on the ability of the voltage-controlled oscillator to generate a unique period of clock under variable V_{dd} was developed. By detecting the unique period under the predefined threshold voltage, reference-free implementation of the proposed voltage level-crossing sensor frees it from the requirement for a reference voltage or any external stable power supply. This voltage level-crossing sensor consists of one voltage-controlled oscillator, two *Delay* generators and two threshold voltage detectors. This proposed reference-free voltage level-crossing sensor can detect single predefined threshold voltage. The key feature of this method is that the voltage sensor is entirely powered by the unstable sensed

V_{dd}, and the speed of oscillation reflects this voltage. The internalisation of references predictably causes a need for sensor calibration, essentially presenting the user with a choice of trading off requiring a stable V_{dd} and/or an external reference with sensor calibration. This proposed reference-free voltage level-crossing sensor will be used as the core element to design a multiple threshold voltage detector. It is the resolution of the difference between two neighbouring points presented in Chapter 5.

Chapter 5

Reference-free voltage monitoring system

5.1 Introduction

In Chapter 4, a new type of reference-free voltage level-crossing sensor was presented (See Fig.4.1) to determine the crossing of a predefined threshold voltage by using a constant time delay in the time domain. This proposed voltage level-crossing sensor can only sense the crossing of a single voltage level. However, continuous voltage sensors with the ability to sense multiple voltage levels may be needed in energy harvesting system [19, 21, 22]. To achieve multi-detection of threshold voltage level using this proposed voltage level-crossing sensor, the corresponding peripheral circuit has been designed and presented in this chapter.

The remainder of this chapter is organised as follows: Section 5.2 will present the overview of this reference-free voltage monitoring system and its methodology of voltage monitoring. In Section 5.3, the circuit implementation and the physical implementation are presented, and Section 5.4 shows the experimental results including the method of the chip repair. In the last two sections, 5.5 shows the temperature variation, and 5.6 summarises this chapter.

5.2 Reference-free voltage monitoring system

5.2.1 Overview of the reference-free voltage monitoring system

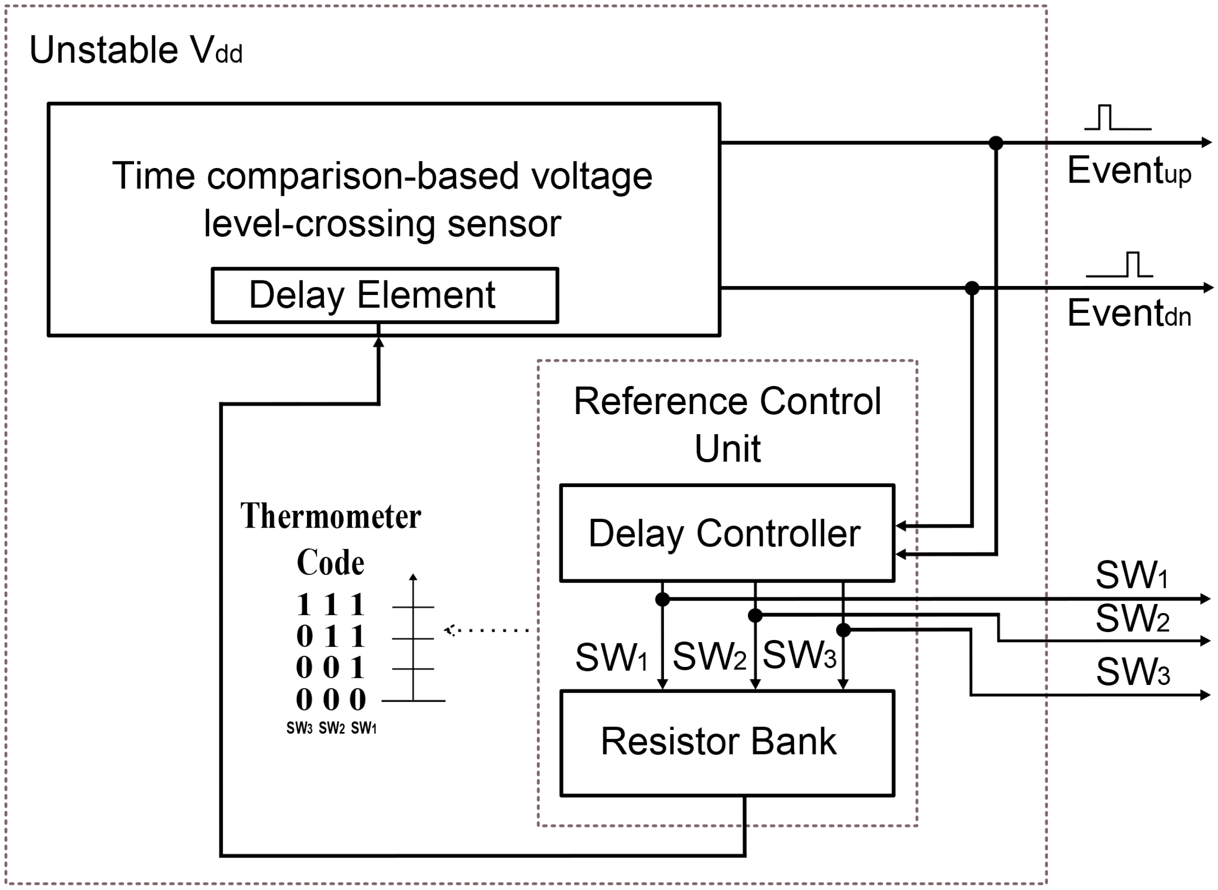


Fig. 5.1 Block diagram of the proposed reference-free voltage monitoring system. Time comparison-based voltage level-crossing sensor is used to sense the predefined threshold voltage presented in Chapter 4. The reference control unit updates the resistance value applied in the delay element of time comparison-based voltage level-crossing sensor to generate new delay corresponding to the next predefined threshold voltage; meanwhile, the thermometer code (SW_1, SW_2, SW_3) is generated as output to represent the detected voltage. Similarly, the input voltage is an unstable V_{dd} from the input DC as shown in system diagram Fig. 1.2. The output is the *Event* signals and the thermometer code. The DC-DC converter can either use *Event* signals or use thermometer code to regulate the V_{dd}.

Fig. 5.1 shows the block diagram of the proposed reference-free voltage monitoring system. It consists of the proposed time comparison-based voltage level-crossing sensor and reference control unit. The reference control unit updates the resistance value for the next sensing round. Once the redefined threshold voltage is detected, the *Event* signal is generated and fed to the delay controller in the reference control unit, and then the thermometer code is generated to represent the detected voltage; this thermometer code will be used to reconfigure the resistor bank to generate the new resistance value according to the next predefined threshold voltage. The new generated resistance value will be applied to the delay element located in the time comparison-based voltage level-crossing sensor as shown in Fig. 5.1. This new resistance value can generate a new reference time *Delay* with the capacitor in Equation 4.2 as shown in Fig. 4.6. Therefore, the *Delay* can be tuned following the different predefined threshold voltage.

5.2.2 Sensing mechanism

The voltage sensing algorithm using the time comparison methods given in previous sections is presented in Table 5.1:

Table 5.1 Algorithm of the sensing mechanism

```
Algorithm of the time comparison process
Loop forever
1. Generate two reference times ($Delay_{up}$ and $Delay_{dn}$), one for the next
   faster frequency $F_{up}$, and one for the next slower frequency $F_{dn}$ ;
2. Wait until either
   a. Rising half threshold voltage detector detects period overlapping with
      $Delay_{up}$; generates $Event_{up}$;
   b. Falling half threshold voltage detector detects period overlapping with
      $Delay_{dn}$; generates $Event_{dn}$;
3. Update to new reference time of next predefined threshold voltage point;
End loop
```

The working principle of reference-free voltage monitoring system is based on the algorithm as shown in Table 5.1. Each sensing round starts with the system having determined the current value of the period of *clk* and hence V_{dd}. Two subsequent *Delay*s are then generated corresponding to the subsequent predefined threshold voltages. $Delay_{up}$ pertains to V_{dd} rising by one precision voltage ΔV (See Fig. 5.2(a)) and $Delay_{dn}$ pertains to V_{dd} falling by one ΔV. When V_{dd} changes by one ΔV in either direction, the rising or falling threshold voltage detector generates the corresponding event based on the period of *clk* crossing either one of these reference times. The last step updates the reference time for sensing the next predefined threshold voltage and the process repeats. There is no obligation that the ΔVs for rising and falling detection are the same or constant across the range. They are programmable to the degree supported by the available programmable resistance values in the delay unit. This thesis investigates the same constant ΔV for both rising and falling V_{dd} situations without losing generality.

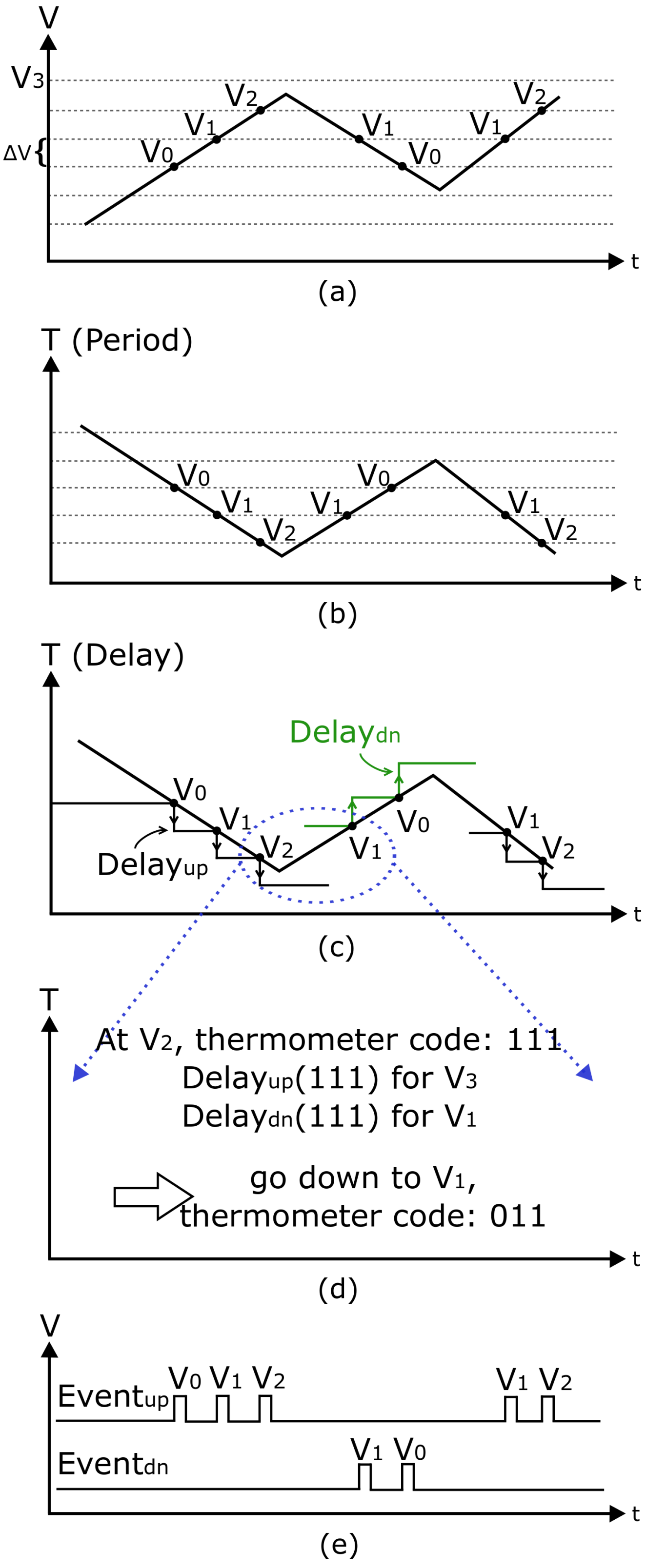


Fig. 5.2 Sensing mechanism operation analysis of the proposed reference-free voltage monitoring system. (a) An example of V_{dd}'s waveform over time, increasing from 0V to V_2, then down to V_1, and finally up to V_2. (b) Change of period of *clk* corresponding to V_{dd}. (c) Change of predefined *Delay* as a function of period of *clk*. (d) Functions of thermometer code: 1. indicating the detected voltage. 2. updating *Delay*. (e) Generation of *Event* signal according to detected predefined voltage.

Fig. 5.2 is an example of voltage sensing according to the algorithm in Table 5.1. The change of V_{dd} in (a) results in the period of *clk* changing from large (at low V_{dd}) to small (at high V_{dd}), then from small to large and back to small again as shown in (b).

Once the sensor starts sensing, the reference control unit generates two reference times, $Delay_{up}$ and $Delay_{dn}$ as discussed in Section 4.3. In (c), once the period of *clk* catches up $Delay_{up}$, $Event_{up}$ is generated to indicate V_{dd} increases to the first predefined voltage V_0, and the generated $Event_{up}$ signal triggers the delay controller in the reference control unit to move forward in the thermometer code from '000' to '001' as shown in Fig. 5.1. This thermometer code, on the one hand, represents V_0 and, on the other hand, helps the resistor bank generates new $Delay_{up}$ and $Delay_{dn}$ for the next sensing round as shown in Fig. 5.1. Subsequently, in the same manner, V_1 and V_2 are indicated.

The highest predefined threshold is V_2 in this example. After V_{dd} rises to V_2, the thermometer code is '111'with three '1's in the least significant bits. A smaller new $Delay_{up}$ and a larger new $Delay_{dn}$ are generated with relevant values for sensing either V_3 (V_{dd} increases) or V_1 (voltage decreases) as shown in (a) and (c). The figure (d) represents the zoom-in.

In (a), after V_2, although V_{dd} increases, it does not reach V_3, so the period of *clk* does not catch up V_3-related $Delay_{up}$. Consequently, $Event_{up}$ at V_3 is not generated (See in (e)). After slightly increasing, the voltage decreases as shown in Fig. 5.2(a), and eventually, the period of *clk* increases sufficiently to match $Delay_{dn}$. The $Event_{dn}$ signal is generated to indicate that V_{dd} decreases to V_1. Thereafter, as V_{dd} keeps decreasing, at each crossing point (V_0 in example), a new $Event_{dn}$ signal is generated to indicate a new voltage V_0. The subsequent changes in V_{dd} including further increasing will generate appropriate time comparisons on the same principles leading to the event pulses shown in (e) of Fig. 5.2.

The precision voltage $\mathit{\Delta}$V is defined as the difference in the voltage value between two detected threshold voltages, and therefore the first detected voltage V_0, as shown in Fig. 5.2(a) should be fixed and known. Once the $Event_{up}$ pulse is generated, it means that the predefined threshold voltage is detected and the preset $\mathit{\Delta}$V is determined; in the meantime, the thermometer code is updated. The updated thermometer code can be used to calculate the detected voltage. For example, if the first predefined voltage is V_0 and detected then the thermometer code is updated to '001' as shown in Fig. 5.2(d) and (e). Thereafter, the second $Event_{up}$ is generated and the code is changed to '011'. Similarly, the code is changed to '111' when the third $Event_{up}$ is generated. Each single generated code ('1') represents one ΔV during voltage detection as shown in Fig. 5.2(a) and (e). To sense V_{dd} decreases, the generated $Event_{dn}$ indicates V_{dd} drops one precision voltage from the pre-detected threshold voltage. The detected voltage can be determined as follows:

$$V_{detc} = \begin{cases} 0 & 0 \leqslant n < 1 \\ V_0 + (n-1) \times \Delta V & 1 \leqslant n \leqslant n_{max} \end{cases} \tag{5.1}$$

where V_{detc} is the n_{th} detected voltage. V_0 is the first detected voltage. ΔV is the precision voltage and n is the number of '1's in the thermometer code. n_{max} is the number associated with the predefined voltage (the upper end of the voltage monitoring range). As three voltages are predefined, n_{max} is equal to 3 in the proposed voltage-free voltage monitoring system.

5.3 Circuit implementation

The circuit implementation of the time comparison-based voltage level-crossing sensor has been presented in Chapter 4. This section will present the circuit implementation of the reference control unit. As shown in Fig. 5.1, the reference control unit consists of two elements. The first is the resistor bank presented in Subsection 5.3.1, and second is the delay controller presented in Subsection 5.3.2.

5.3.1 Resistor bank

The reference time *Delay* is a very significant factor in the proposed sensing mechanism. The higher its precision requirement, the more sophisticated the delay generator needs to be. There are many methods which can implement tunable delays. Because of the unstable V_{dd} in the proposed reference-free voltage monitoring system, the simple RC delay circuit is a good choice because its latency is independent of the supply voltage as discussed in Section 4.4.2

5.3.1.1 Multiple RC delay generator

In Chapter 4, the voltage level-crossing sensor is proposed to detect a single predefined threshold voltage; only one set of resistor and capacitor is needed for the predefined voltage as shown in Fig. 4.6. However, in this chapter the multiple voltage sensor is proposed; this means that multiple reference times are required to detect different predefined voltages. To provide more predefined voltage-related reference time, a multiple reference RC delay generator is proposed in this section.

Compared to the single reference time generator as shown in Fig. 4.6, this multiple reference RC delay generator uses a resistor bank rather than only one resistor, each resistor in the resistor bank corresponds to a predefined voltage-related reference time as shown in Fig. 5.3.

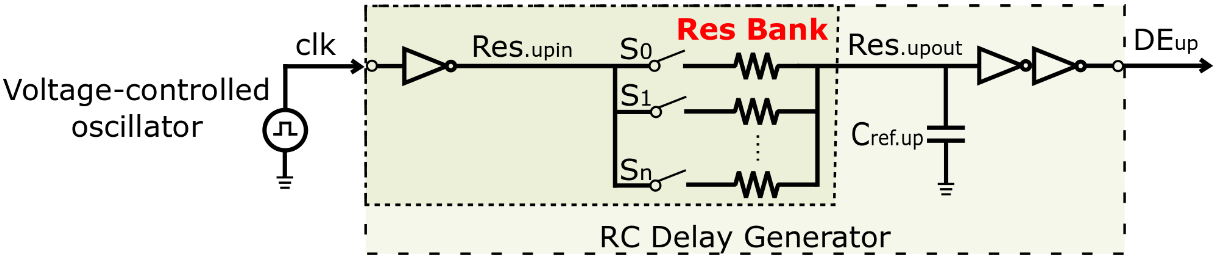


Fig. 5.3 Circuit diagram of multiple RC time reference ($Delay_{up}$) generator. This RC time reference generator (See Fig. 5.1) can be programmed to generate different delay times corresponding to the connected resistor. Basically, more resistors are connected in parallel, resulting in a smaller value of total resistance generated; thereby, the smaller delay is generated.

Fig. 5.3 shows the circuit diagram of the multiple reference times generator. It consists of one resistor bank and one fixed capacitor. As DE_{up} needs to be updated according to the predefined voltage during every new voltage detection round, the RC delay value needs to be tunable. RC programmability is achieved by having multiple resistors in the resistor bank which can be connected according to ΔV requirements. DE_{up} can be determined as follows:

$$R_{total.up} \approx \frac{DE_{up}}{C_{ref.up}} \tag{5.2}$$

where DE_{up} is the reference time according to the predefined voltage for the next detection round; $R_{total.up}$ is the total resistance which can be set to achieve DE_{up}. The estimated values of $R_{total.up}$ have been shown in Table 4.3, and here $C_{ref.up}$ is 1.4nF.

5.3.1.2 Programmable resistor bank

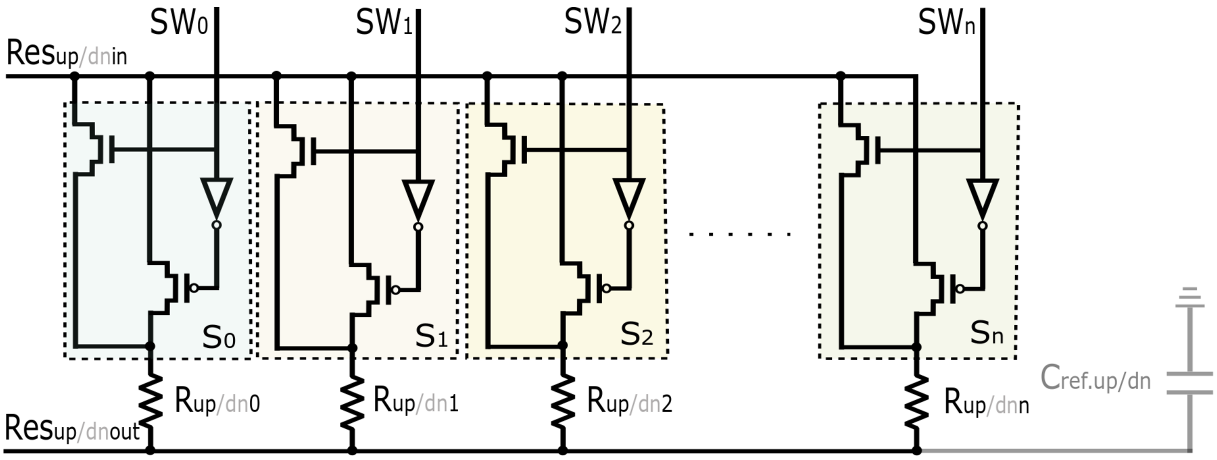


Fig. 5.4 Architecture of programmable resistor bank. The programmable resistor bank (See Fig. 5.1) consists of a set of switches connected to the resistor bank. The number of switches depends on the number of predefined voltages. In the explanation below, assume that n predefined voltages are present.

Fig. 5.4 shows the architecture of a programmable resistor bank, the required DE_{up} for each detection round is generated by triggering the switches S_0, S_1, S_2, etc. In order to derive the output terminal either to a low or high voltage equally well, these switches are composed of a transmission gate which combines an NMOS and PMOS transistor into a signal switch [119, 120]. The capacitance $C_{ref.up}$ is constant during the voltage detection, and we only need to change the resistance of the programmable resistor bank to assemble the required DE_{up}. The total resistance of this programmable resistor bank can be derived as follows:

$$R_{total.up} = \frac{1}{\frac{1}{R_{up0}} + \frac{1}{R_{up1}} + \ldots + \frac{1}{R_{upn}}} \tag{5.3}$$

Here, in (5.3), it is assumed that n resistors are connected during this detection round. The thermometer code (e.g. SW_0, SW_1, SW_2, SW_n) is used to control switches, as apparent from Fig. 5.4. Different combinations of these signals can generate different DE_{up} that is used to detect the different predefined voltages in the proposed reference-free voltage monitoring system.

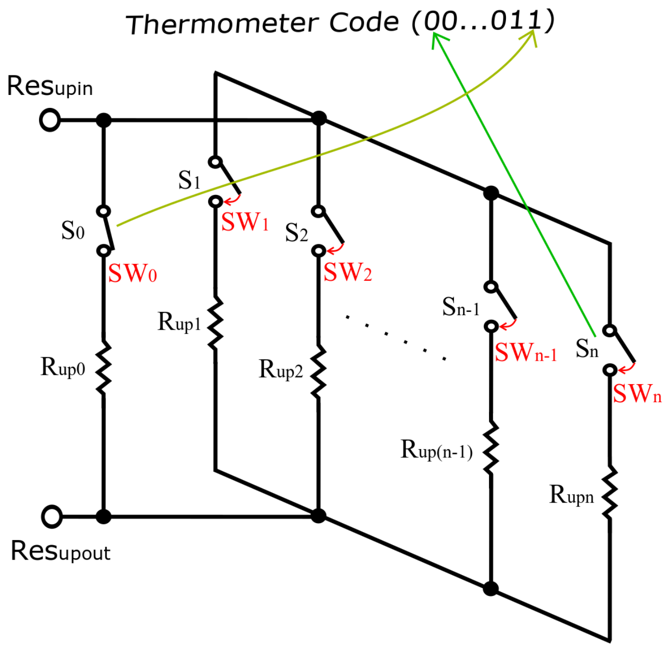


Fig. 5.5 Reconfiguration of reference time based on the updated thermometer code. When the sensor starts working, S_0 is switched on by SW_0 to detect the first predefined voltage. With the thermometer code moving forward, more and more resistors are connected corresponding to the predefined voltages. The generation of thermometer code will be presented in Section 5.3.2 as shown in Fig. 5.10.

In the beginning, S_0 is closed by triggering signal SW_0 and R_0 connected to the circuit for detecting the first predefined voltage V_0 (See Fig. 5.2). Hence, DE_{up} is $R_{up0} \times C_{ref.up}$ at this moment and V_0 is also set as an initial voltage $V_{init} = V_0$. The first detected voltage will be set as an initial voltage to be detected, which can be used to determine the further targeted voltages. As SW_0 needs to be pulled up to logic '1' when the reference-free voltage monitoring system starts working, SW_0 can be connected to the *start* signal of the entire system in the proposed reference-free voltage monitoring system. In other words, SW_0 is logic ‘1’ until the reference-free voltage monitoring system stops working. According to this, the thermometer code may exclude SW_0, and SW_1 is the first bit in the thermometer code. Once SW_1 is logic ‘1’ the output thermometer code is ‘00...01’ and the V_{init} is detected. The SW_1 connects the second resistor R_{up1} to the circuit. Then the new DE_{up} will be is 1 / (1 / R_{up0} + 1 / R_{up1}) × $C_{ref.up}$ updated for the next voltage detection round as explained in subsection 5.2.2, and the second detected voltage will be V_{init} + ΔV, and the thermometer code will be changed to ‘00...11’ once the second detected voltage is detected as shown in Fig. 5.2(d). Hence, with the increase of V_{dd}, the thermometer code accumulates further until all the predefined voltages are detected.

5.3.2 Delay controller

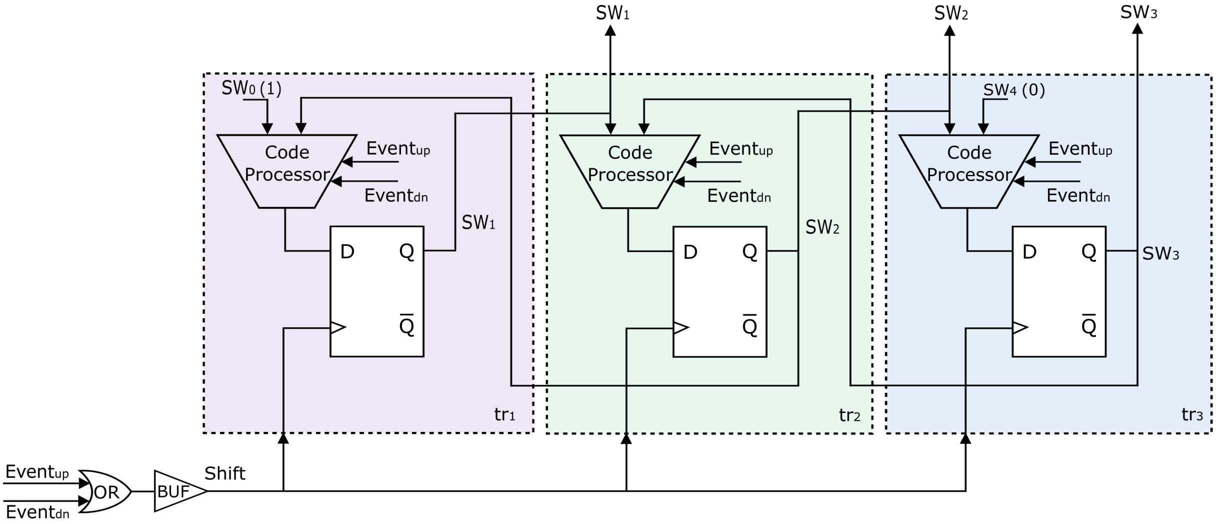


Fig. 5.6 Block diagram of delay controller, which has three trigger units (tr_1,tr_2 and tr_3). These trigger units are used to generate SW_1,SW_2 and SW_3 as shown in Fig. 5.1. Each trigger unit consists of one code processor and one D Flip-Flop. The code processor’s function is processing relevant data according to detected voltage for the D Flip-Flop which stores the data and generates the SWs. A shift signal is generated by $Event_{up}$ and $Event_{dn}$ passing through an OR gate and a buffer to advance or recede the thermometer code. A buffer is used to generate a delay for waiting till the code processor finishes data generation.

The delay controller (See Fig. 5.1) plays a significant role in the reference control unit. The function of this delay controller is used not only to advance or recede the thermometer code to represent the detected voltage but also to control the generation of reference time according to the next sensing round as illustrated in Fig. 5.2 (c) and (d).

As this proposed reference-free voltage monitoring system is designed to continuously sense three voltage values, the delay controller includes three trigger units with the function of generating each single code in the thermometer code. As introduced previously, all the trigger units are triggered by the $Shift$ signal generated by the $Event_{up}$ signal and $Event_{dn}$ signal. More $Event_{up}$ signals are generated, more trigger units are switched on, and on the other hand, more $Event_{dn}$

signals are generated, more trigger units are switched off. This feature of the delay controller will be used to tune the reference time in Subsection 5.3.1. The structure of the trigger unit is shown in Fig. 5.7.

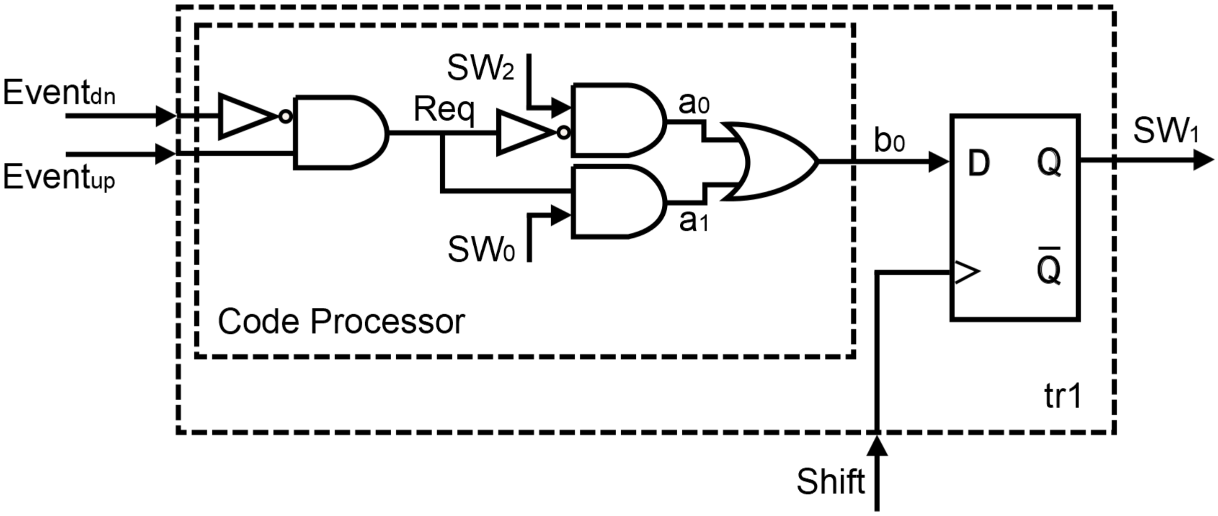


Fig. 5.7 Circuit diagram of the first trigger unit in Fig. 5.6. This code processor is used to generate a corresponding signal (b_0) to generate SW_1 once the D Flip-Flop is triggered by $Shift$ signal.

Fig. 5.7 shows the circuit diagram of the code processor in first tr_1, it consists of three AND Gates, two inverters and one OR Gate. This trigger unit has three inputs, $Event_{up}$, $Event_{dn}$ and $Shift$, and one output SW_1. The $Shift$ signal is generated irrespective of generating $Event_{up}$ or $Event_{dn}$ as shown in Fig. 5.6. Initially, before generating SW_1, b_0 is logic '0'. If $Event_{up}$ is generated, the signal b_0 pulls up to logic '1' by the code processor; in the meantime, $Shift$ is generated to trigger D Flip-Flop to catch b_0 thus generating logic '1' in SW_1. On the other hand, if $Event_{dn}$ is generated, the code processor pulls b_0 down to '0' and thus b_0 is passed to SW_1 by triggering D Flip-Flop. The operating details of the code processor will be shown in Fig. 5.8.

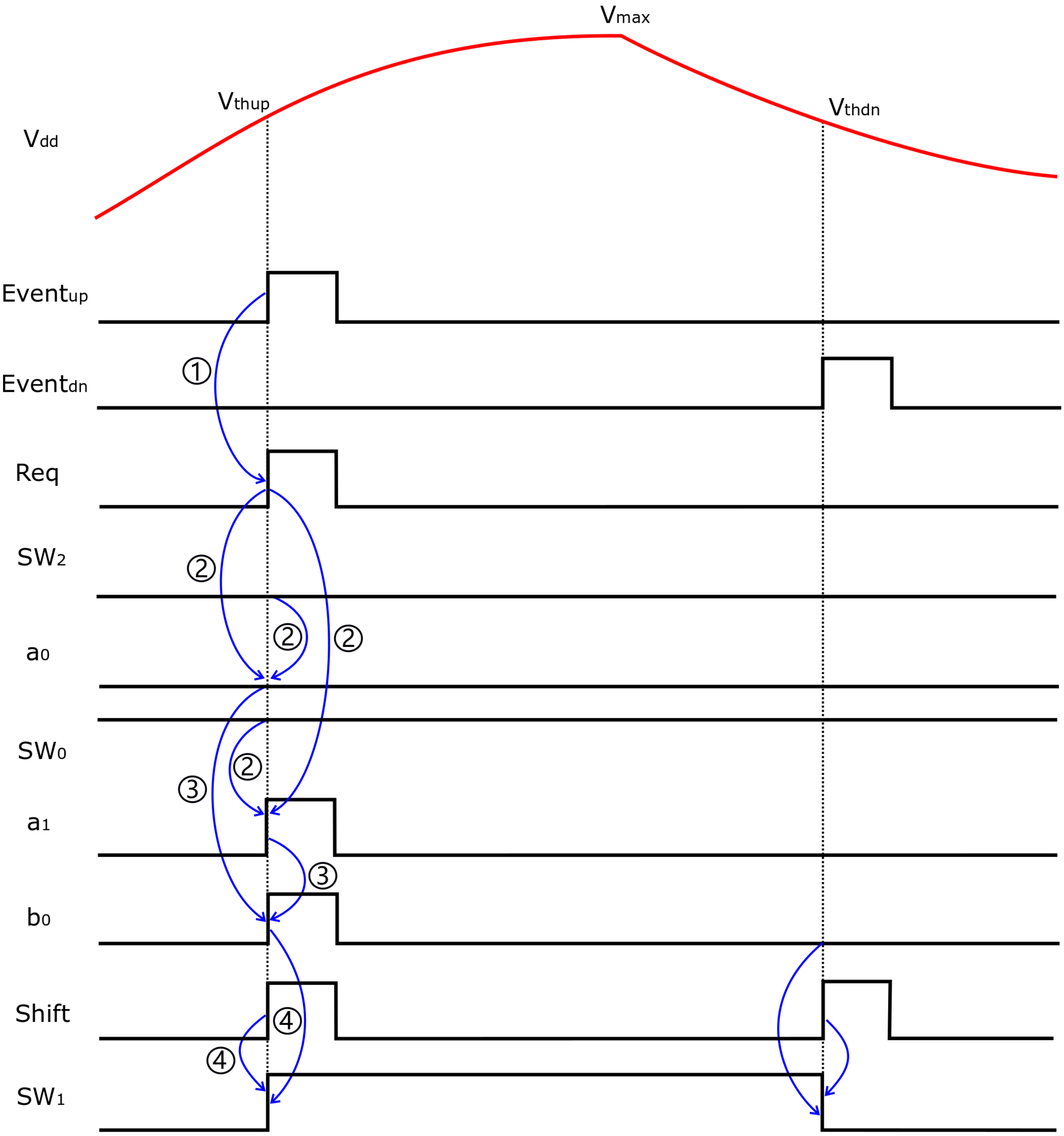


Fig. 5.8 Operating waveform of the first trigger unit used in Fig. 5.6. This figure shows the work process of the generation of SW_1.

As evident from the figure, the operating waveform of the trigger unit is shown for the example in Fig. 5.8. Initially, switch SW_0 is logic ‘1’, SW_1 and SW_2 are logic ‘0’. There is no action from $Event_{up}$ and $Event_{dn}$ to trigger the trigger unit. Once the V_{dd} starts increasing, SW_0 pulls up to logic ‘1’ automatically from the initial condition for detecting V_{init}. Generally, SW_0 is connected to a start signal which is treated as logic ‘1’. When V_{dd} increases to V_{thup}, the $Event_{up}$ signal is pulled up to logic ‘1’ to trigger the AND Gate on the left-hand side in Fig. 5.7 to generate Req as shown the step 1 in Fig. 5.8. Once Req is generated, a_0 remains the same, and the generated Req pulse pulls up a_1 (See step 2) to trigger the OR Gate to generate b_0 as shown in step 3 in Fig. 5.8. In the meantime, the $Shift$ signal is generated by the $Event_{up}$ signal, which triggers the D Flip-Flop to catch b_0 and pull up the signal SW_1 as shown in step 4. Similarly, the predefined voltage V_{thdn} is detected during V_{dd} decreases, the $Event_{dn}$ signal is pulled up, resulting in SW_1 being pulled down with the same work process as that when $Event_{up}$ generated as shown in Fig. 5.8.

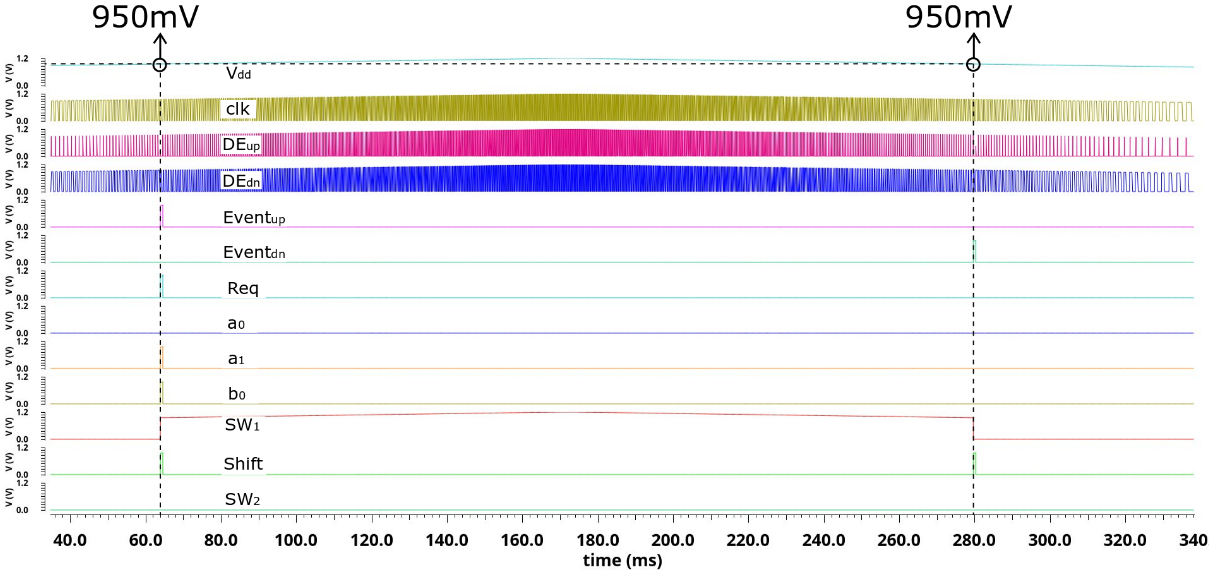
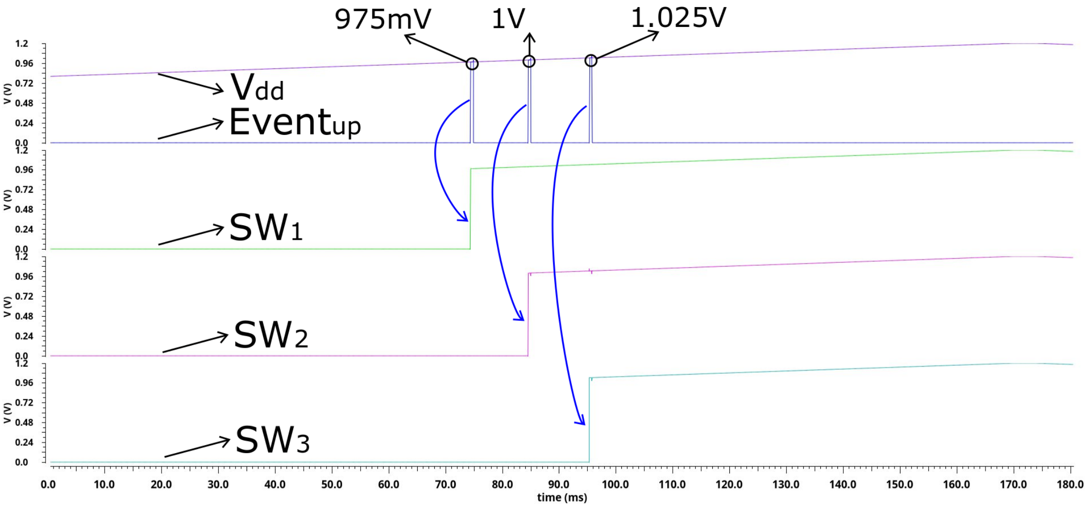


Fig. 5.9 The proposed trigger unit was simulated using 350nm AMS library. In this figure, the generation of SW_1 is shown when the predefined voltage (950mV) is detected.

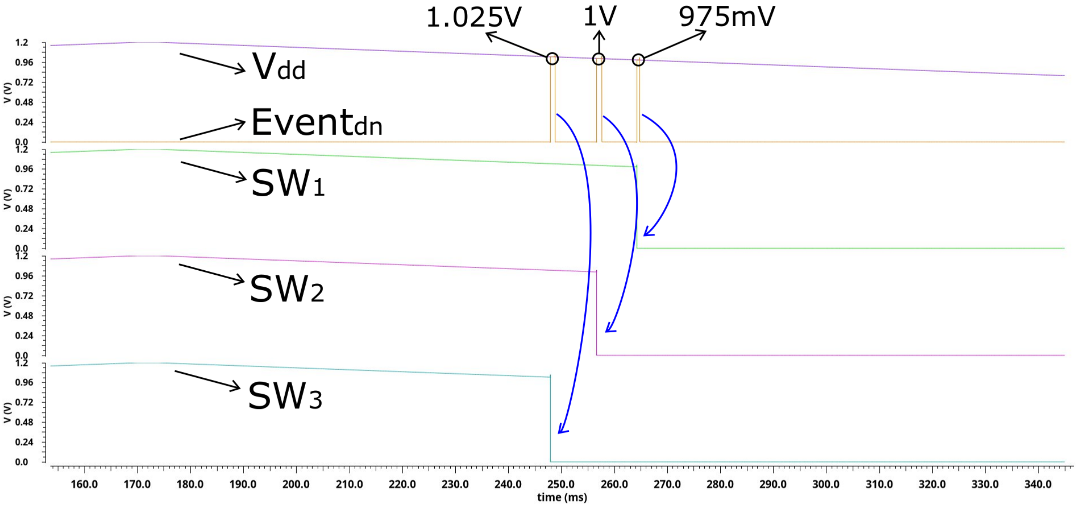
As this proposed reference-free voltage monitoring system is supposed to sense the voltage in energy harvesting system, the energy should be accumulated from zero in the super capacitor as shown in Fig. 1.2, and therefore the V_{dd} increases first and then may decrease or continue to increase or keep stable. Table 5.2 shows the truth table of the delay controller. This truth table indicates an example of switching on/off the control signal SW_1 and SW_2.

Table 5.2 Truth table of delay controller

$Event_{.up}$	$Event_{.dn}$	Req	a_0	a_1	b_0	SW_0	SW_1	SW_2	SW_3
0	0	0	0	0	0	1	0	0	0
1	0	1	0	1	1	1	1	0	0
0	0	0	0	0	0	1	1	0	0
1	0	1	0	1	1	1	1	1	0
0	0	0	0	0	0	1	1	1	0
0	1	0	0	0	0	1	1	0	0
0	0	0	0	0	0	1	1	0	0
0	1	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0



(a) Generation of SWs during V_{dd} increases.



(b) Generation of SWs during V_{dd} decreases.

Fig. 5.10 Delay controller operation. In this simulation, the ΔV is 25mV, and the estimated R_{ref} and $Delay$ are from Table 4.3. (a) SW_1, SW_2 and SW_3 are pulled up when three predefined voltages V_{thup}s are detected. (b) SW_1, SW_2 and SW_3 are pulled down when three predefined voltages V_{thdn}s are detected.

Fig. 5.10 shows the simulation results of the delay controller. As discussed, this proposed reference-free voltage monitoring system is designed to detect three predefined threshold voltages. In this figure, the three predefined voltages are 975mV, 1V and 1.025V with 25mV increment whenever the V_{dd} increases or decreases. The results show that the proposed reference-free voltage monitoring system has met our expectation: the SWs are switched on/off when the predefined voltages are detected. It can properly move forward/backward the thermometer code (See Fig. 5.1) to tune the reference time $Delay$ according to the predefined voltages as shown in Fig. 5.4. The adjustment of the reference time $Delay$ with the detection of the predefined voltage has been detailed in the chip measurement section as shown in Fig. 5.20 and 5.21.

For instance, in our chip test, V_{init} is 975mV, ΔV is 25mV, and the final targeted voltage is 1.025V, which is V_{init} + (3-1) × ΔV. Therefore n_{max} is 3, implying that the reference-free voltage monitoring system may detect three possible voltage crossings 975mV, 1V and 1.025V (See

Fig. 5.20). Before the first $Event_{up}$ is generated, the code is '000'. There are zero '1's in the code, and therefore V_{detc} is '0'. Once the first $Event_{up}$ pulse is generated, and updates the code to '001' there is one '1' in the code, and V_{detc} is changed to V_{init} that is 975mV. Similarly, when the second targeted voltage is detected, the second $Event_{up}$ is generated, resulting in two '1's in the code. V_{detc} equals to 1V which is 975mV + (2-1) × 25mV. Here, 25mV is ΔV and 2 is the number of detected voltages (n). If the voltage continues to increase, the third detection step will eventually detect the crossing of 1.025V in the same fashion before the voltage goes out of range for the monitoring system.

5.3.3 Physical implementation of the proposed reference-free voltage monitoring system

The reference-free voltage monitoring system designed in this chapter was fabricated at the 350nm AMS technology node. The layout of the entire system and the physical verifications were completed using the Cadence Virtuoso set of tools. The resulting layout of the reference-free voltage monitoring system as shown in Fig. 5.11 covers an active area of $0.0155\mu m^2$. As discussed, the proposed reference-free voltage monitoring system is supposed to function in a harsh environment with insufficient energy; the unstable V_{dd} is applied as shown in Fig. 5.11. The chip is designed such that the off-chip capacitors and resistors may be used for testing purposes as a back-up solution in case the on-chip RC circuits encounter malfunctions. The extra pins are added to connect the off-chip resistors and capacitors as shown in Fig. 5.11. The final step in the physical design flow is the physical verifications (Layout verse schematic (LVS) and Design Rule Check (DRC)).

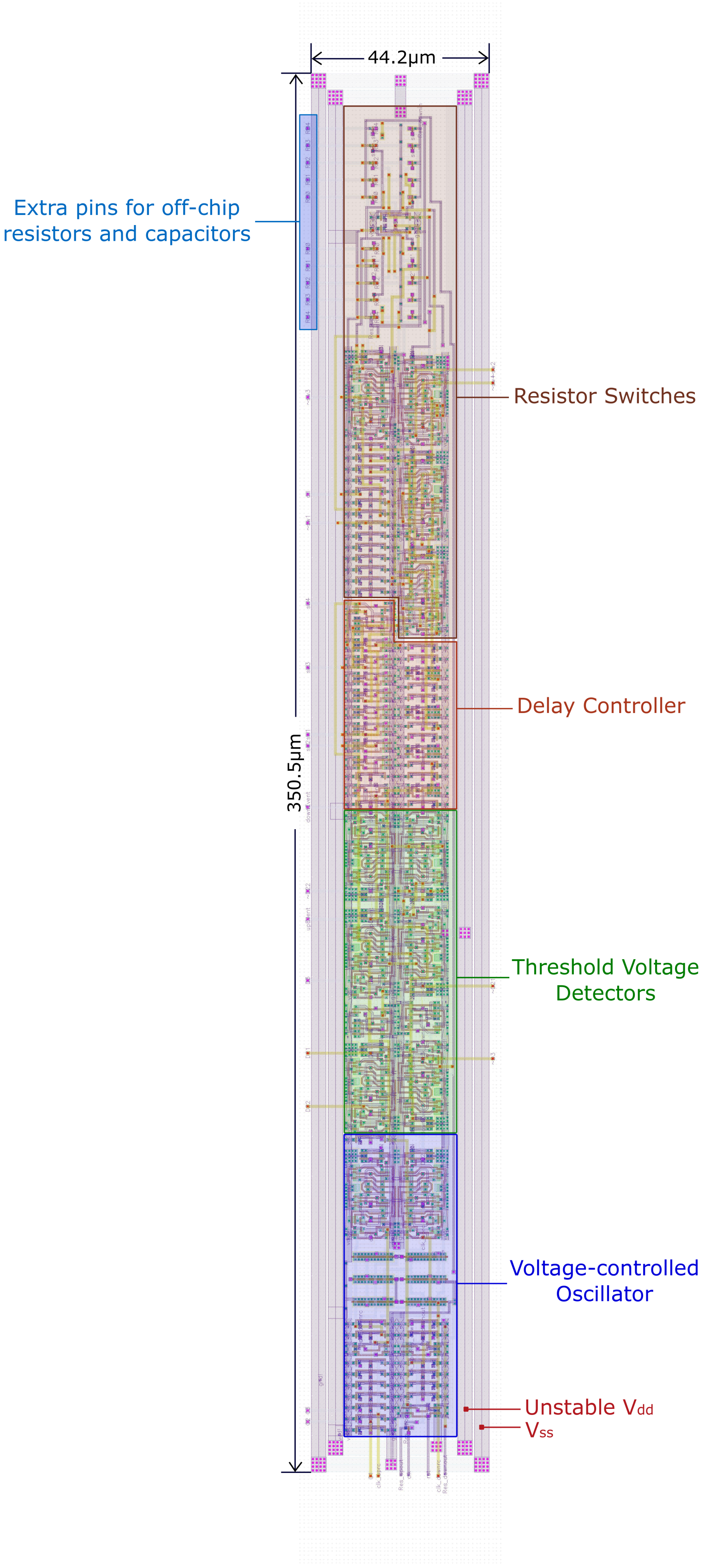


Fig. 5.11 Layout of the reference-free voltage monitoring system. The extra pins are used to connect the off-chip resistors and capacitors in case the on-chip resistors and capacitors cannot provide proper values. The design is implemented in the 350nm AMS technology node and covers an area of 350.5μm by 44.2μm.

5.4 Measurement results

This section discusses the chip test to validate the operation of the reference-free voltage monitoring system. Section 5.4.1 discusses the chip repair process, which can be a shared experience for other researchers who may need chip repair. Section 5.4.2 shows the micrograph of the fabricated chip and denotes its active area. Section 5.4.3 briefly discusses the printed circuit board (PCB) used to hold the chip during the testing. Section 5.4.4 presents the setup of the chip test including the equipment and test range of V_{dd}. Finally, Section 5.4.5 examines the operating performance, including logic oscillation, sensing operation, response time and power consumption, respectively.

5.4.1 Chip repair

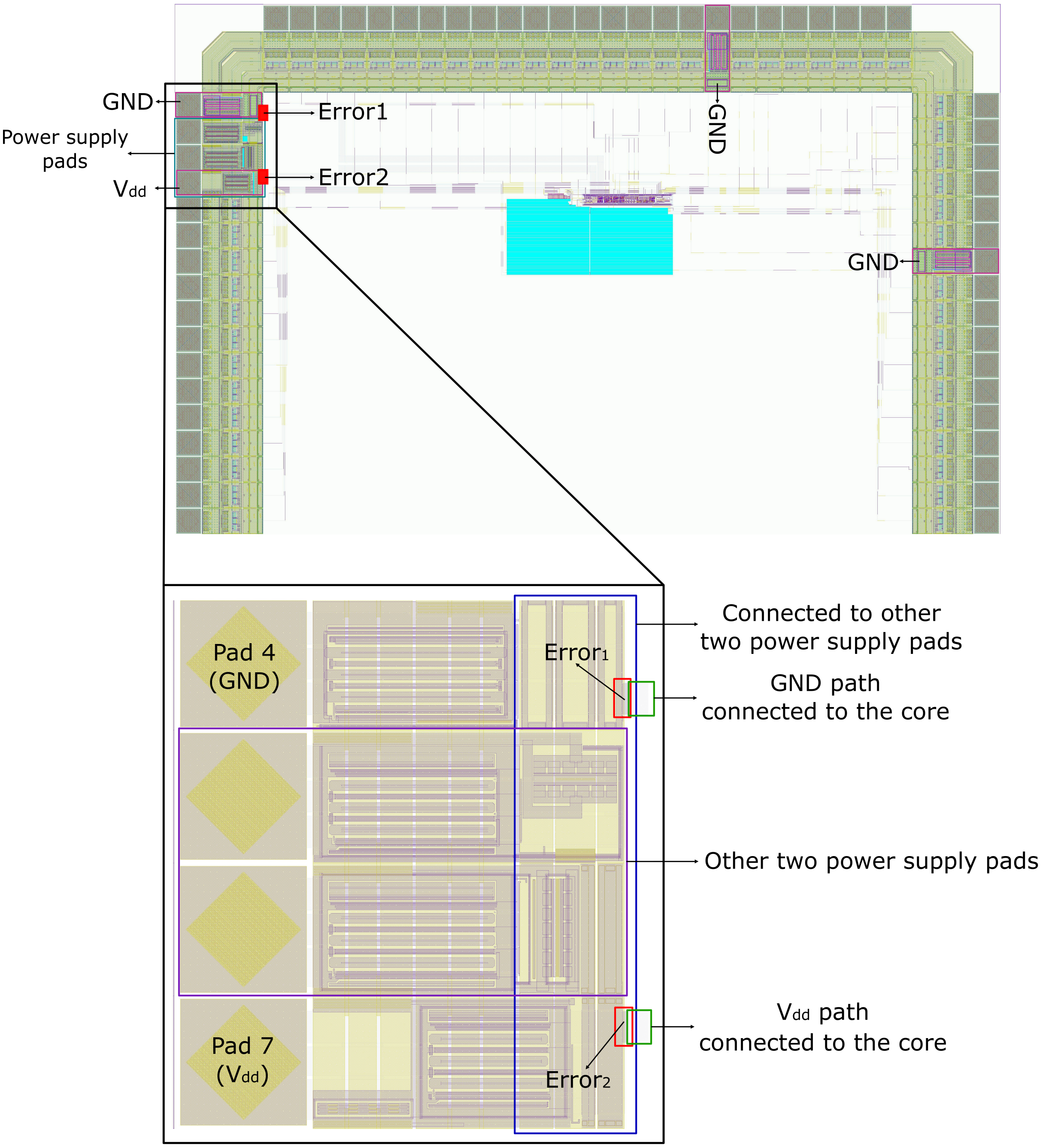


Fig. 5.12 Micrograph of the error's position. In the fabricated chip, three GND pads and three power supply pads are used. Two of the power supply pads are used to power all the pads in the chip, and the last one (Pad 7) is used to power the core design only. The errors are marked and zoomed-in in this figure.

Fig. 5.12 shows the errors during making the layout of the chip. Pad 4 and Pad 7 are connected to the core by GND path and V_{dd} path, respectively, for powering the system. Two extra vias ($Error_1$ and $Error_2$) were placed between $Metal_1$ and $Metal_2$ on these two pads connects to the core as shown in the zoomed-in figure in Fig. 5.12. $Error_1$ connects the ground to the $Metal_2$ in Pad 4, and $Error_2$ connects the V_{dd} to the $Metal_2$ in Pad 7. However, these two $Metal_2$s are connected by $Metal_3$ through via and also connected to other two power supply pads as shown in Fig. 5.12, resulting in the ground, V_{dd} and other power supply pads being shorted by $Metal_3$.

Focused ion beam (FIB) is a common method for via cutting. Two solutions can be used in this case. The first solution cuts both the errors and then reconnects the ground to Pad 4 and V_{dd} to Pad 7 by $Metal_1$. The second solution cuts $Error_1$ only and keeps $Error_2$, which means that Pad 4 is disconnected from the core. As there are three ground pads designed in the system as shown in Fig. 5.12, cutting $Error_1$ can still use the rest of the ground pads. However, both these solutions may give rise to unpredictable issues. For instance, the first solution has a high risk in the reconnection because the process of reconnection needs to be performed manually. However, on such a small chip, the operator can easily cause offset errors and damage the pads around Pad 4 and Pad 7. The second solution cannot measure the power consumption of the pads and core, respectively. However, in the fabricated design, there are three pads for power supply which is better for measuring the power consumption for pads and core, respectively. As an extra via ($Error_2$) added in Pad 7, these three power supply pads are connected as shown in Fig. 5.12. Therefore, to keep $Error_2$ in the second solution, three pads of the power supply are still connected through $Error_2$, and the measurement of power consumption will include both pads and core without differentiation. Finally, the second solution was selected in order to not risk total failure, and the fixed chip micrograph is shown in Fig. 5.13. The discrepancy between simulated and measured power shown in Fig. 5.25 may be related to this decision.

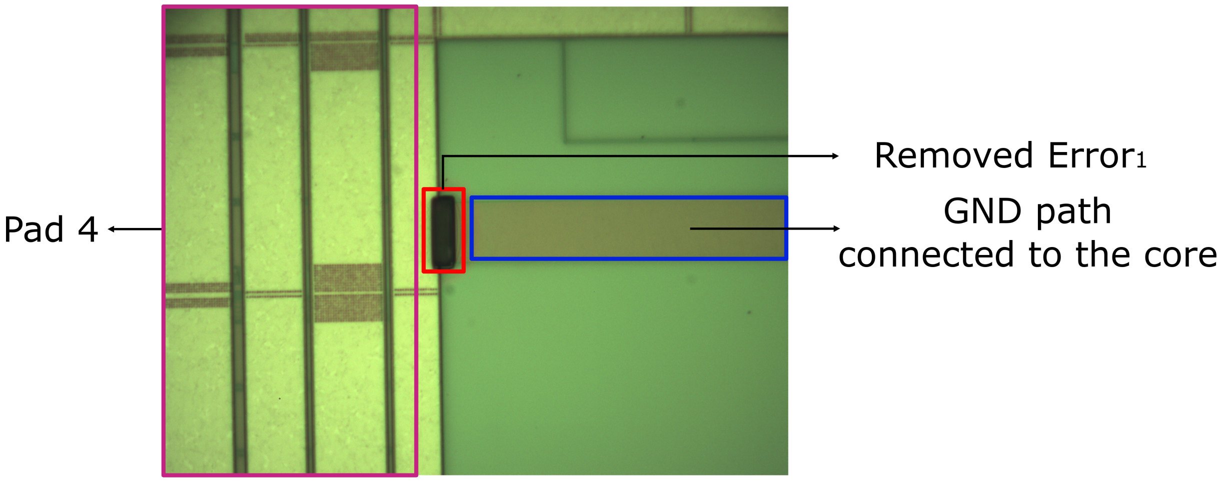


Fig. 5.13 Fixed chip micrograph. The $Error_1$ has been removed in Pad 4.

5.4.2 Fabricated chip

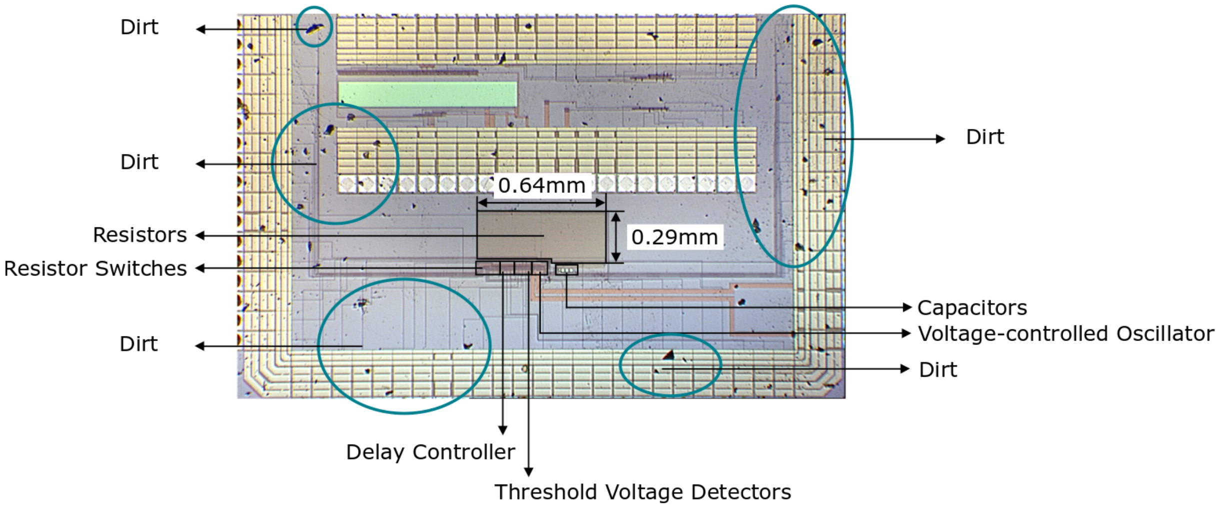


Fig. 5.14 Micrograph of the proposed reference-free voltage monitoring system with on-chip resistors and capacitors in 350nm AMS technology node. The dirt dropped due to the chip repair have been marked in this figure.

Fig. 5.14 shows the micrograph of the die. The chip contains voltage-controlled oscillator, two proposed threshold voltage detectors, a delay controller, resistor switches, resistors and capacitors as shown in Fig. 5.11. The occupied area of the voltage monitoring system is 0.016mm^2, 0.0022mm^2 of which is covered by the voltage-controlled oscillator, 0.0023mm^2 by the threshold voltage detectors, 0.0014mm^2 by the delay controller, 0.0038mm^2 by the resistor switches and 0.0063mm^2 by the V_{dd}/GND paths together. Independent of the reference-free voltage monitoring system, the on-chip resistors and capacitors occupied 0.177mm^2 together as shown in Fig. 5.14.

5.4.3 Printed circuit board

A two-layer printed circuit board (PCB) was designed and fabricated for the testing of the chip, covering an area of 165.99mm by 105.41mm. An array of female headers was used for the off-chip component connection as the off-chip resistor bank and capacitors are used as a backup solution as discussed in Section 5.3.3. Fig. 5.15 shows the PCB layout from the top and bottom views.

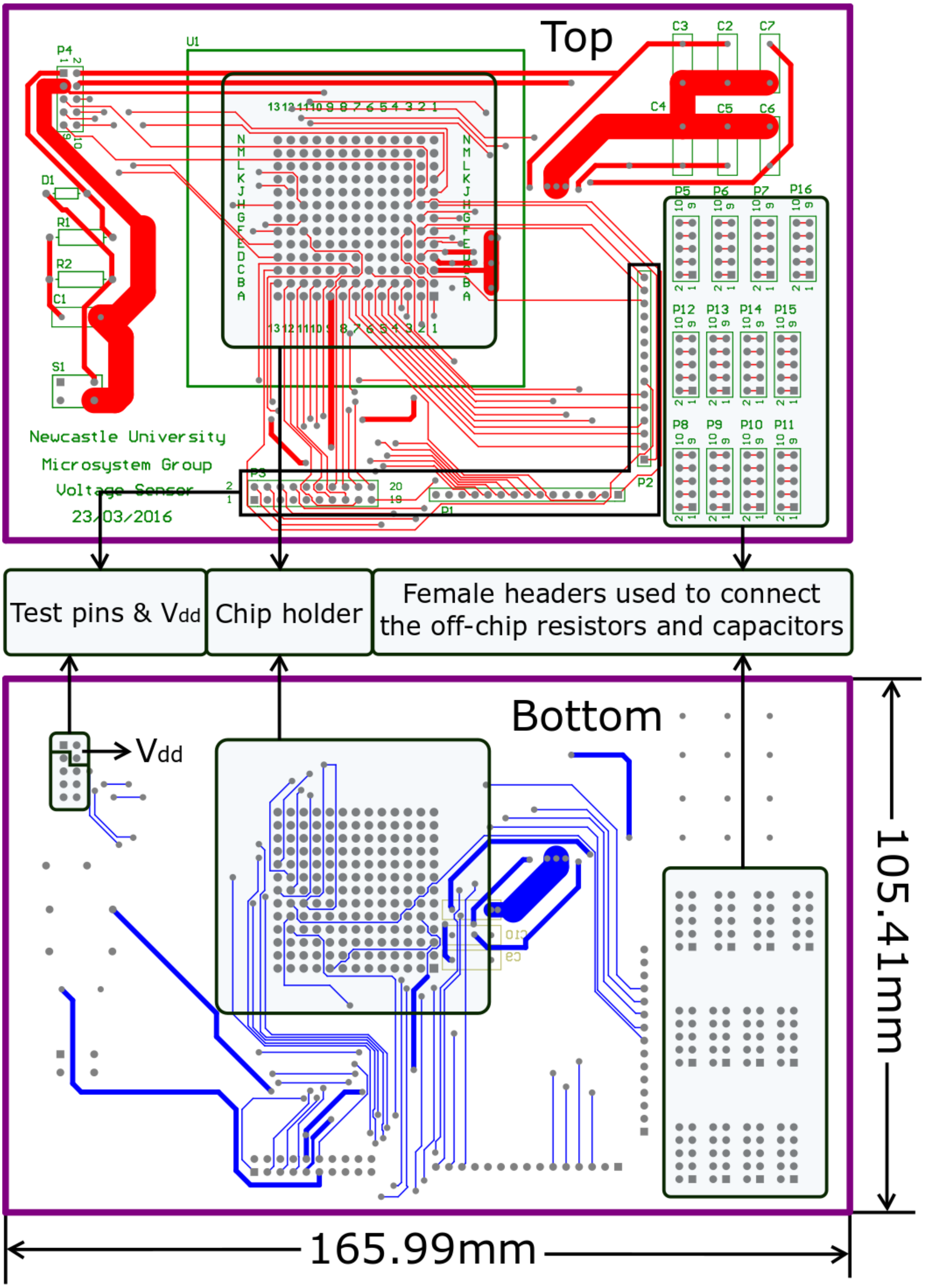


Fig. 5.15 PCB layout. The female headers, test pins, chip holder and V_{dd} have been marked.

5.4.4 Test setup

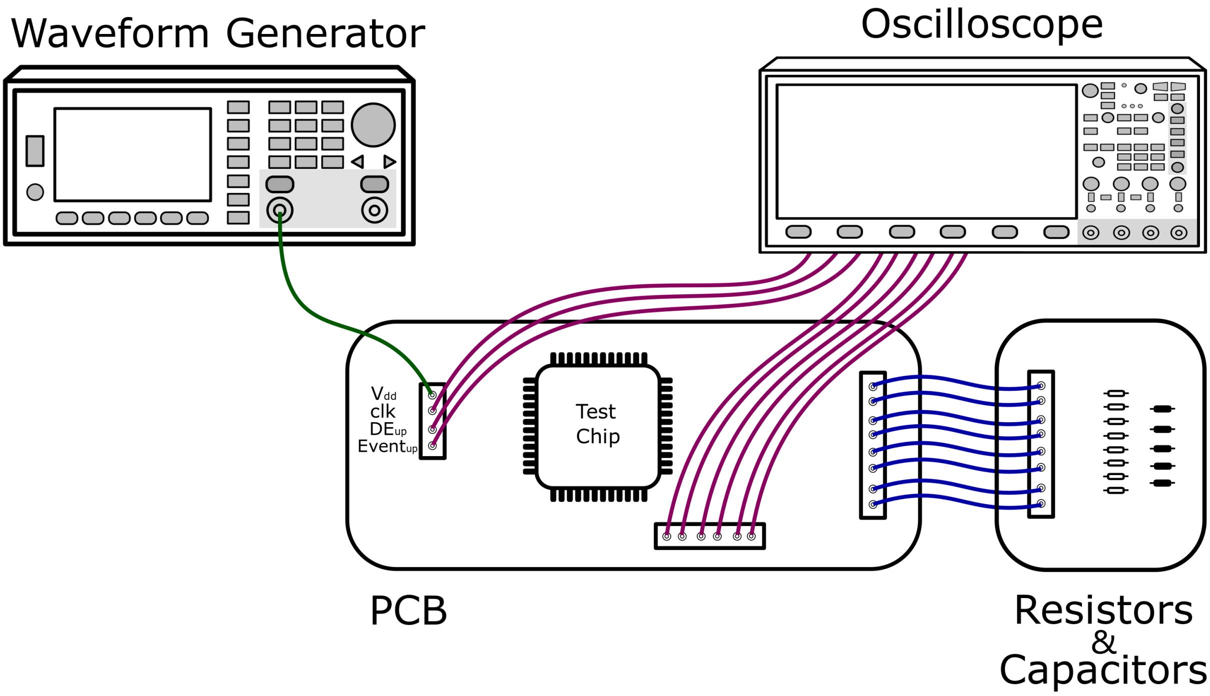


Fig. 5.16 Test Setup. The PCB is connected to a waveform generator (Keysight 33500B) that provides the unstable V_{dd} to simulate a harvested energy from the environment, an oscilloscope (Agilent DSO-X 2014A) and off-chip resistors and capacitors.

Fig. 5.16 shows the setup used in the experimental testing of the chip. The PCB is connected to a waveform generator (Keysight 33500B), an oscilloscope (Agilent DSO-X 2014A) and off-chip resistors and capacitors. This partially repaired test chip can only detect predefined voltages when the V_{dd} increases by using off-chip resistors and capacitors as its on-chip resistors and capacitors, and the falling voltage sensor does not work. The possible reason for this is that the lid of the die was opened for repairing the chip, and the top of the chip was broken and dirt fell on the top of the chip as shown in Fig. 5.14. The chip repair has a very low success rate. Five samples were sent for repair. Two of them were found completely damaged when the lid of the chip was opened. Two of them were damaged during the repair process. Only one of them was repaired to the point that it could be tested in the setup as shown in Fig. 5.14. The details of chip repair have been presented in Section 5.4.1. The oscilloscope was used to monitor the digital information generated by the test chip.

The Keysight 33500B waveform generator is used to generate the required V_{dd} used in the testing i.e a typical testing input is illustrated in Fig. 5.17, assuming that the V_{dd} is accumulated from 0V to 1.3V in 2s under a nominal temperature of 27°C in the energy harvesting system. In the chip test, the predefined voltages are set within the range of 0.85V to 1.2V with 25mV increment (the ΔV is set to be 25mV). For example, 0.85V, 0.875V, 0.9V, 0.925V and so on as shown in Fig. 5.18. To show the operation performance of the chip test, the predefined voltages of 975mV, 1V and 1.025V are used for discussion, respectively. Therefore, the estimated *Delay*s are 261μs, 231μs and 207μs for 975mV, 1V and 1.025V, respectively, as shown in Table 4.3.

These three predefined voltages will be used as an example to show the voltage detection of the reference-free voltage monitoring system in Section 5.4.5.2.

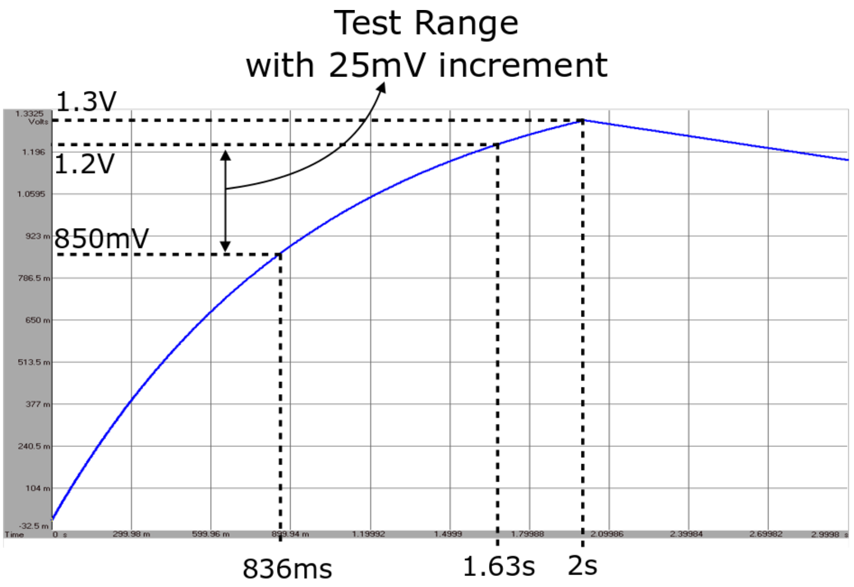


Fig. 5.17 Testing input (V_{dd}) generated by Keysight 33500B waveform generator. The test range of V_{dd} is from 0.85V to 1.2V with 25mV increment.

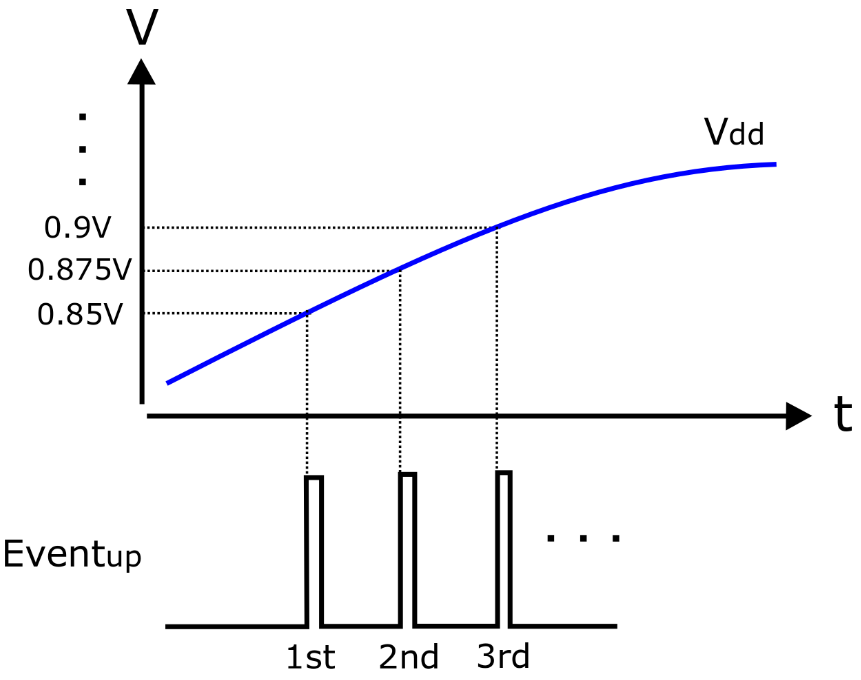


Fig. 5.18 The illustration of the predefined voltages in the chip test. The predefined voltage should be detected in order starting from 0.85V with 25mV increment till 1.2V. In the design of the fabricated chip, only three different predefined voltages can be detected after each manual setting of the reference time.

5.4.5 Operating performance

5.4.5.1 Logic oscillation

The performance of voltage-controlled oscillator is a crucial factor in the entire voltage monitoring process. This section compares the voltage-controlled oscillator in the Cadence tool and that in the tested chip. The voltage test range of V_{dd} varies from 0.85V to 1.2V with 50mV increment. Fig. 5.19 compares the frequency characteristics of chip measurement and Cadence simulations.

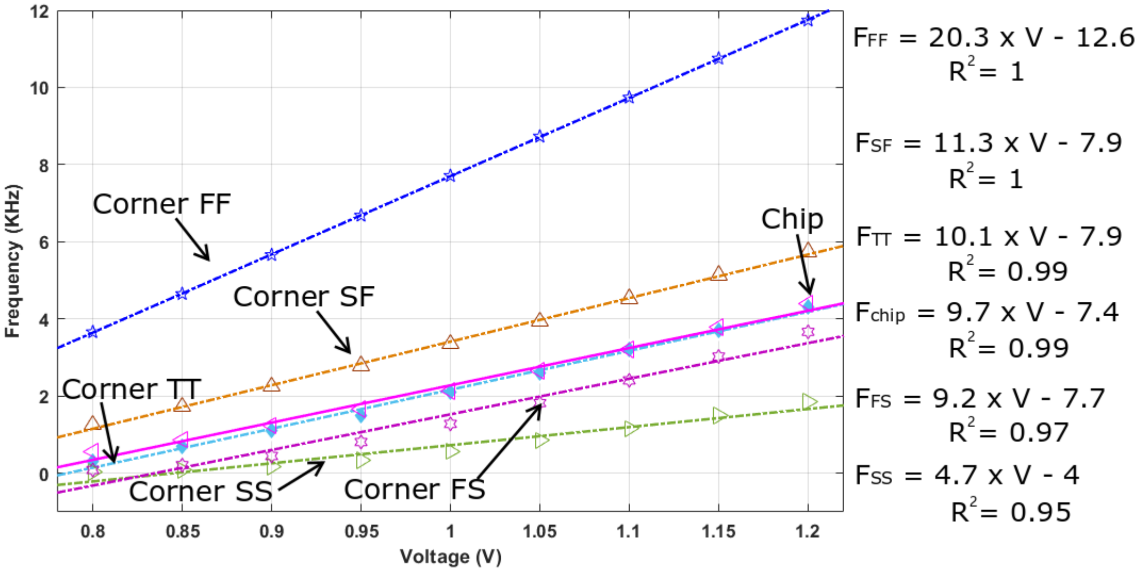


Fig. 5.19 Logic oscillation in simulation and measurement.

As evident from Fig. 4.19, the chip measurement results are very similar to the simulation results at the TT corner. The fitted equations have very close coefficients and the TT corner simulation equation can actually be used to estimate chip behaviour with high confidence. Because of the internalisation of references, sensors of this type are affected by process variations and require characterisation and calibration. However this example fabricated chip returned results much closer to the TT corner than the other corners. The following discussion compares the measured results with simulation results at the TT corner only. The comparison of the frequency variation between the measured result and the simulated result is shown in Table 5.3.

Table 5.3 Comparison of voltage-controlled oscillator between Cadence simulation (corner TT) and chip measurement.

	Simulated	Measured
Mean (KHz)	2.4	2.5
Standard Error (KHz)	0.45	0.44
Standard Deviation (KHz)	1.28	1.25

Comparing the simulated results to the measured results, all the main factors are slightly different. Table 5.3 shows small standard error in both simulated results and measured results, and the difference of the standard error between simulation and measurement is only 11Hz. The difference of standard deviation is approximately 30Hz, and the means of simulation and measurement are similar. Therefore, the designed specifics of the voltage-controlled oscillator are achieved, and it works correctly on the fabricated chip.

5.4.5.2 Sensing operation

As discussed in Section 5.16, the predefined voltages 975mV, 1V and 1.025V are used as examples to show the voltage detection of the reference-free voltage monitoring system in this section. Therefore, the first detected voltage (V_{init}) is 975mV, and the detection voltage precision (ΔV) is 25mV in the experiment as discussed in Section 5.16; this implies that the $Event_{up}$ should be pulled up three times when the V_{dd} crosses through 975mV, 1V and 1.025V, respectively.

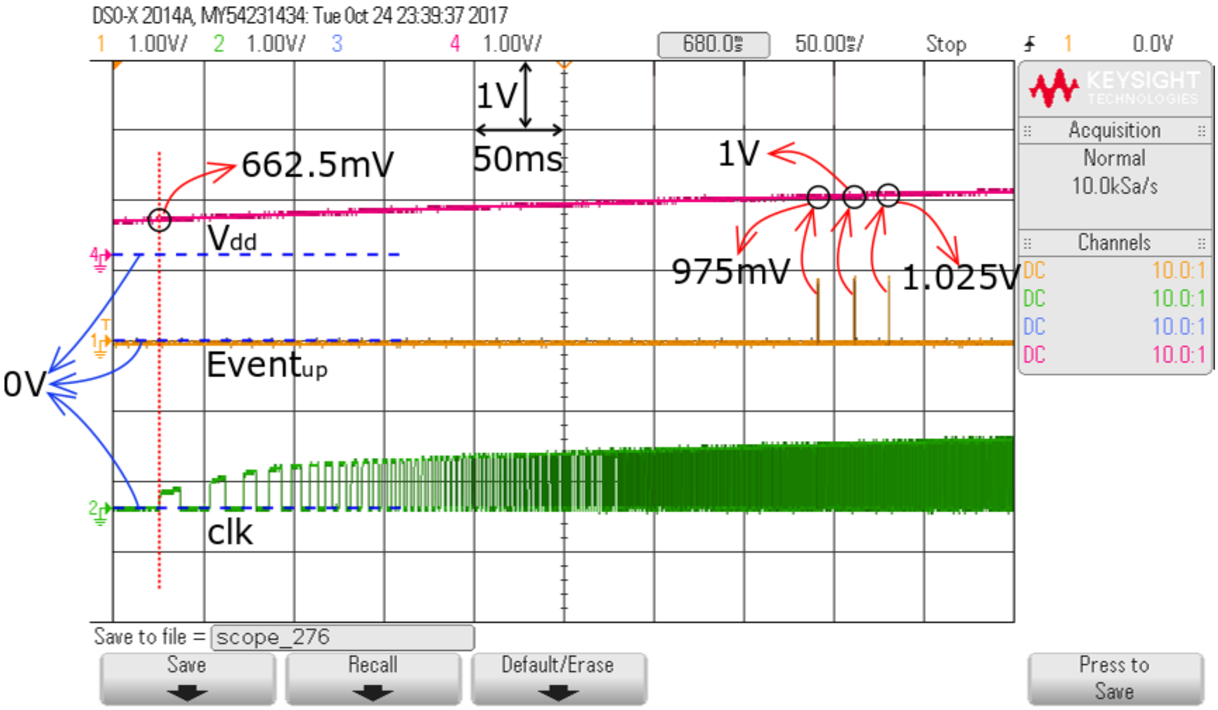


Fig. 5.20 Voltage detection over time. The voltage-controlled oscillator starts oscillation when V_{dd} increases to 662.5mV. The $Event_{up}$ has been pulled up three times to indicate three predefined voltages; 975mV, 1V and 1.025V have been detected.

Fig. 5.20 shows the captured waveform of the detection of these three predefined voltages. The voltage-controlled oscillator starts oscillating when V_{dd} crosses 662.5mV, which implies that for the system to start sensing voltage, V_{dd} should be at least 662.5mV and the lowest detectable voltage can be 662.5mV in theory. Based on the sensing methodology presented in Section 4.3.1, when the half period of *clk* crosses through the first predefined $Delay_{up}$ = 261μs (See Table 4.3 when predefined voltage is 975mV), the first $Event_{up}$ pulse is generated, which represents V_{dd} = 975mV. Subsequently, $Delay_{up}$ is updated to detect the next predefined voltage which is

1V (975mV + 25mV). Similarly, once the second $Event_{up}$ pulse is generated, the $Delay_{up}$ is updated 207μs, that is, half the period of clk when V_{dd} increases to 1.025V. The adjustment of the $Delay_{up}$ is presented in Fig. 5.21 using the detected 975mV as an example.

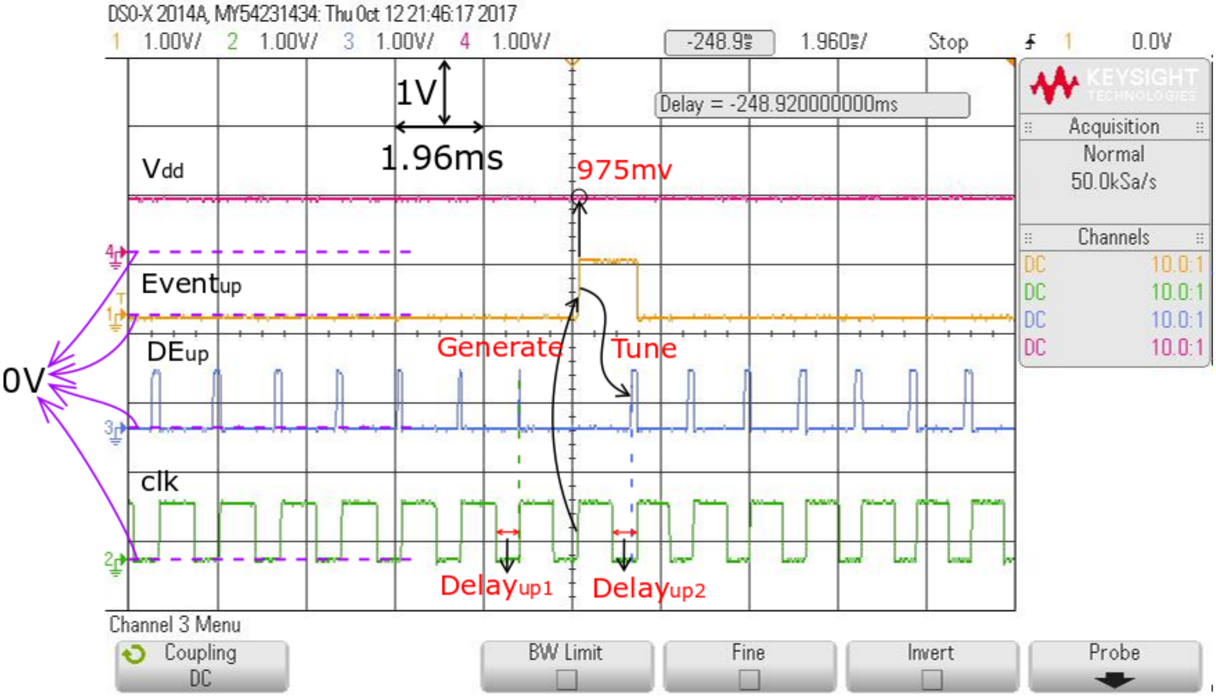


Fig. 5.21 Reference time ($Delay_{up}$) adjustment with voltage sensing. In this figure, the predefined voltage is 975mV used for illustration. $Delay_{up1}$ is the predefined reference time for 975mV and $Delay_{up2}$ is the predefined reference time for 1V. $Event_{up}$ is generated to tune the reference control unit as shown in Fig. 5.1, resulting in updating the reference time to $Delay_{up2}$. Compared to the theoretical waveforms earlier in Fig. 4.9, $Delay_{up}$ in Fig. 4.9 is $Delay_{up1}$ in this figure. The predefined voltage has been detected when the period of clk is overlapped with the calculated period (the calculated period = $t_8 - t_6$ in Fig. 4.9(b)).

Fig. 5.21 shows the adjustment of delay when the system is monitoring 1V from the detected 975mV. Here, the predefined voltage is 975mV whose $Delay_{up1}$ is supposed to be 261μs and the calculated period should be 522μs as shown in Table 4.1; however, because of the processing latency during the detection, the $Event_{up}$ pulse cannot be generated at the proper predefined $Delay_{up1}$ as described in theory. Generally, $Event_{up}$ is pulled up after one cycle as shown in Fig. 5.21. Once the $Event_{up}$ pulse is generated, $Delay_{up}$ will be tuned to a new value which is $Delay_{up2}$ = 231μs for detecting 1V in the new sensing round. It is apparent that the DE_{up} almost disappears before $Event_{up}$ is pulled up, however, it starts to re-oscillate after $Event_{up}$ pulse is generated based on the new $Delay_{up2}$ as shown in Fig. 5.21.

Table 5.4 Error between detected period (chip test) and calculated period.

Predefined threshold voltage (V)	Calculated period (ms)	Detected period (ms)	Error (ms)	Percentage (%)
1.2	0.239	0.235	0.004	1.7
1.175	0.254	0.245	0.009	3.5
1.15	0.272	0.258	0.014	5.1
1.125	0.292	0.280	0.012	4.1
1.1	0.315	0.301	0.014	4.4
1.075	0.342	0.330	0.012	3.5
1.05	0.374	0.360	0.014	3.7
1.025	0.413	0.412	0.001	0.2
1	0.461	0.438	0.023	5
0.975	0.522	0.512	0.010	1.9
0.950	0.602	0.567	0.035	5.8
0.925	0.709	0.696	0.013	18.3
0.9	0.864	0.778	0.086	10
0.875	1.106	0.960	0.146	13.2
0.85	1.530	1.13	0.4	26.1

Table 5.4 shows the comparison between the calculated period (See Table 4.1) and the detected period from chip test. For the predefined voltages, the maximum percentage of error is 26.1% at 0.85V, and the minimum percentage of error is 0.2% at 1.025V. The maximum percentage may cause a voltage sensing error of approximately 23mV under simulation. This is very close to ΔV (25mV) and further demonstrates the need for post-fabrication of sensors of this type.

To establish a more complete context, these results are further compared with those obtained through post layout simulation. This comparison is shown in Table 5.5.

Table 5.5 Detected period in post layout simulation.

Predefined threshold voltage (V)	Detected period (ms) in post layout
1.2	0.224
1.175	0.241
1.15	0.259
1.125	0.281
1.1	0.308
1.075	0.338
1.05	0.377
1.025	0.423
1	0.478
0.975	0.554
0.95	0.644
0.925	0.766
0.9	0.939
0.875	1.175
0.85	1.549

Compared to the detected period in schematic simulation (See Table 4.4), the detected periods in post layout simulation (See Table 5.5) are slightly less than the detected periods in schematic simulation. The biggest difference is 131μs at 0.85V and the smallest difference is 9μs at 1.2V as shown in Fig. 5.22. Therefore, the lower difference is produced at a higher predefined voltage within the tested voltage range from 0.85V to 1.2V.

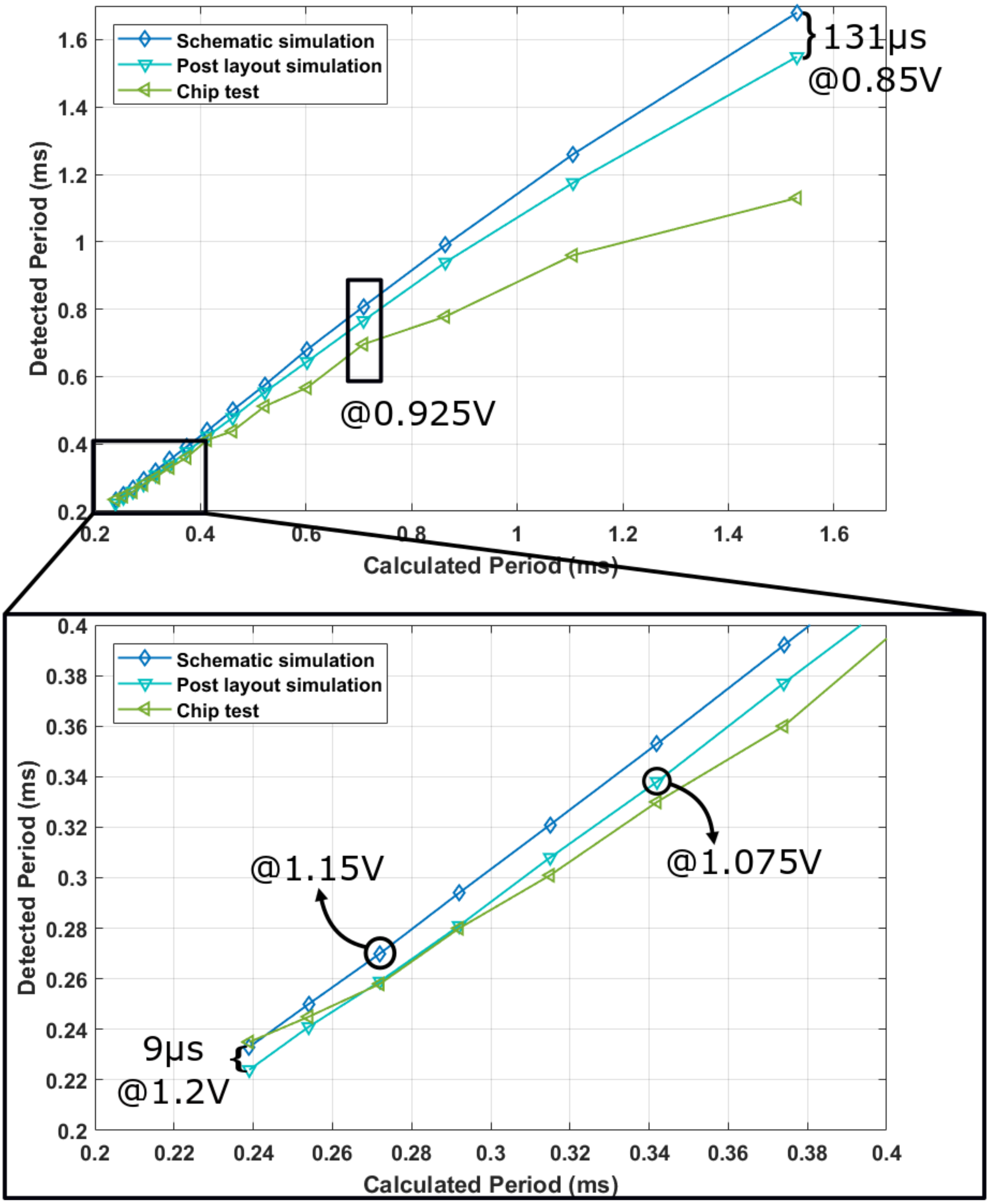


Fig. 5.22 Comparison of the detected period with the calculated period. Three different recorded detected periods: from the schematic simulation as shown in Table 4.4, from the post layout simulation as shown in Table 5.5 and from chip test as shown in Table 5.4, respectively. The top subfigure shows the detected period for detecting predefined voltage from 0.85V to 1.2V, and the predefined voltage in the zoomed-in figure is from 1.05V to 1.2V.

Fig. 5.22 shows the comparison of three detected periods (recorded from schematic simulation, from post layout simulation and from chip test) with the calculated period. Most of the detected periods in schematic simulation and post layout simulation are greater than the calculated period as shown in Fig. 5.22. In the schematic simulation, the detected period is less than the calculated period only when the predefined voltages are 1.15V, 1.175V and 1.2V, respectively. In post layout simulation, when the predefined voltages are 1.075V, 1.1V, 1.125V, 1.15, 1.175 and 1.2V, the detected periods are less than the calculated period as shown in the zoomed-in figure in Fig. 5.22. However, in chip test, all the detected periods are less than the calculated periods, and the difference between the detected period in post layout simulation and the calculated period increases significantly when sensing 0.85V, 0.875V, 0.9V and 0.925V as shown in Fig. 5.22. Based on the comparison in Fig 5.22, the detected period is significantly related to the characteristics of the circuit fabrication. Therefore, the calibration is necessary to achieve proper detection of the predefined voltages in the proposed reference-free voltage monitoring system.

5.4.5.3 Response time

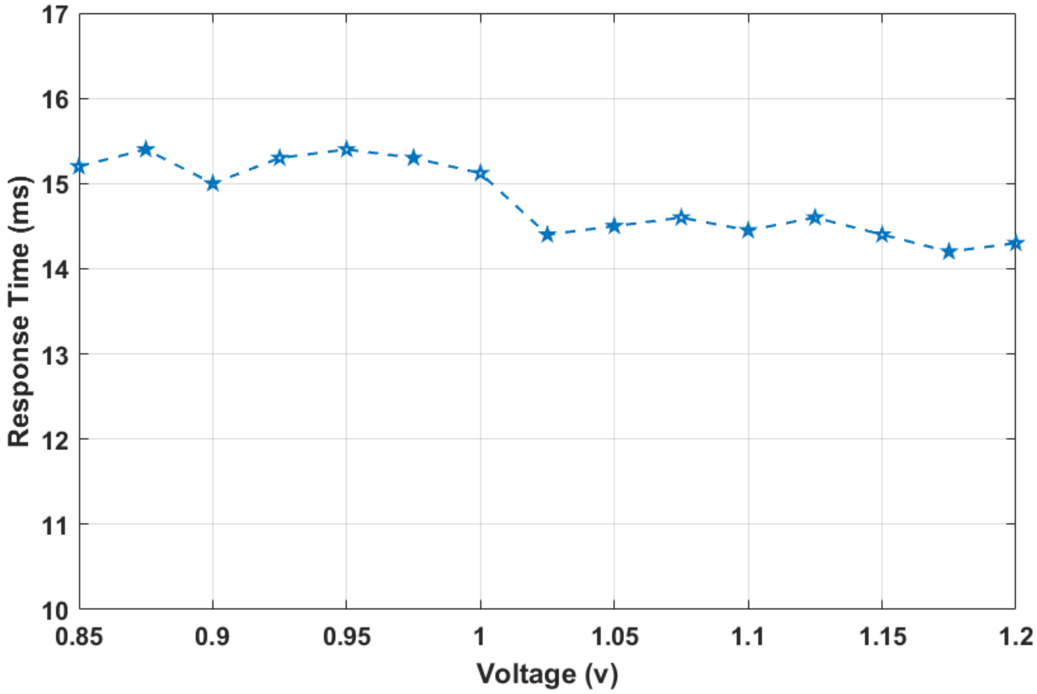


Fig. 5.23 Response time measured from the oscilloscope. The response time is the time between V_{dd} reaching the predefined voltage and $Event_{up}$ being generated as shown in Fig. 5.24. The time is measured by the oscilloscope Agilent DSO-X 2014A as shown in Fig. 5.16.

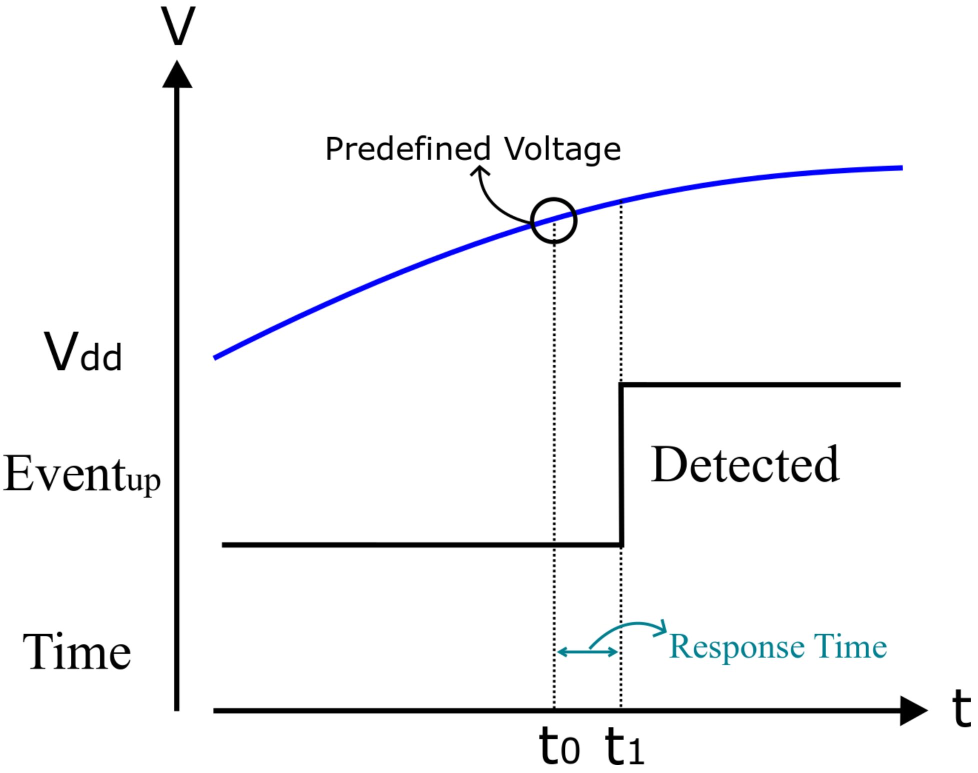


Fig. 5.24 Definition of response time in the chip test.

The response time as measured in the chip test illustrates that the detection can be completed between 14ms and 16ms within the tested range from 0.85V to 1.2V. Fig. 5.23 shows the variation trend of the response time. The maximum response time is about 15.4ms at 875mV, and the minimum is approximately 14.2ms at 1.175V, as shown in Fig. 5.23. As can be seen, the response time remains around 15.2ms before V_{dd} = 1V and then decreases to 14.4ms when V_{dd} is over 1V. Instead of falling monotonically with the rising V_{dd} as would be expected for CMOS components, the response time falls in general but with ups and downs. This is because the time comparison method is ultimately discrete in terms of the number of voltage-controlled oscillator cycles. The presented system shows significant improvements in terms of response time over existing solutions even when the existing solutions are measured at higher voltages, for instance, the power-on-reset-based voltage tracker. In [121], the response time is around 70ms at 3V and in [122], the response time is up to 200ms at 1.8V and 2.5V.

5.4.5.4 Power consumption

Table 5.6 Comparison of power consumption between measured results and simulated results.

Detected Voltage (V)	Simulated (mW)	Measured (mW)
1.2	0.39	0.42
1.15	0.33	0.36
1.1	0.27	0.3
1.05	0.22	0.26
1	0.17	0.21
0.95	0.14	0.17
0.9	0.09	0.13
0.85	0.06	0.09

Table 5.6 shows the power consumption of the reference-free voltage monitoring system under different voltage levels from 1.2V down to 850mV obtained from Cadence simulations and chip measurements. This measured power consumption includes the oscillator and all the sensing blocks. The worst case in this tested voltage range is 1.2V, the power consumption is about 0.42mW in measurement results and 0.39mW in simulation results which is about 30μW difference. As evident from Fig. 5.23, the response time is 14.3ms at 1.2V, and then the consumed energy is approximately 6μJ for detecting 1.2V. If compared to 180nJ for detecting 1.8V in [77], the consumed energy is large. However, external triggers are required in most conventional sensors [22, 29], which are not energy-free to generate.

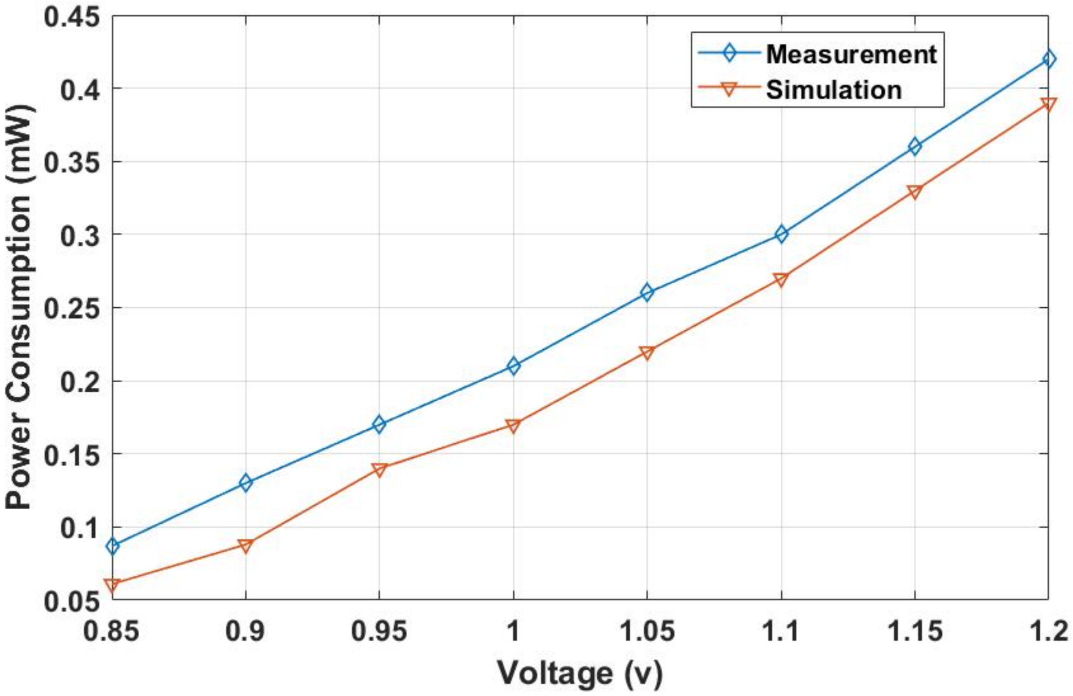


Fig. 5.25 Power consumption over voltage.

The power consumption of the simulated and the measured results are plotted in Fig. 5.25. It is shown that the difference between them is almost the same which is about 45μW regardless of V_{dd}. The difference (45μW) appears to be a constant overhead. The simulated power consumption is for the reference-free voltage monitoring system circuits only whilst the measurements were done off-chip. The distance between these two points of instrumentation may account for a relative power overhead.

The comparison with existing reference-free voltage sensors is listed in Table 5.7. An overview of the comparison table suggests that [22] has similar characteristics with this work. It has very close values of the power consumption and area, and the advantage of [22] is an extensive voltage range from 0.8V to 1.8V which is more than this work. However, the response time of [22] is significantly larger than this work. If compare the response time, [25] has the shortest time 0.6ns. However, [25] can only detect 1.1V with high power consumption 4.4mW.

Table 5.7 Comparison with prior ART.

Ref.	[22]	[77]	[122]	[21]	[25]	This Work
Tech. (nm)	180	180	250	90	40	350
Power (mW)	0.36	N/A	N/A	0.78	4.4	0.42
Area (μm^2)	13000	12000	40000	N/A	1400	16000
Response time	<98 (ms)	80 (ms)	<200 (ms)	<0.9 (μs)	<0.6 (ns)	<16 (ms)
Voltage range (V)	0.8-1.8	1.8	1.8&2.5	0.2-1	1.1	0.85-1.2
External reference	No	No	No	No	No	No
Voltage detection method	Voltage comparison	Voltage comparison	Time comparison	Time comparison	Voltage comparison	Time comparison

5.5 Temperature variation

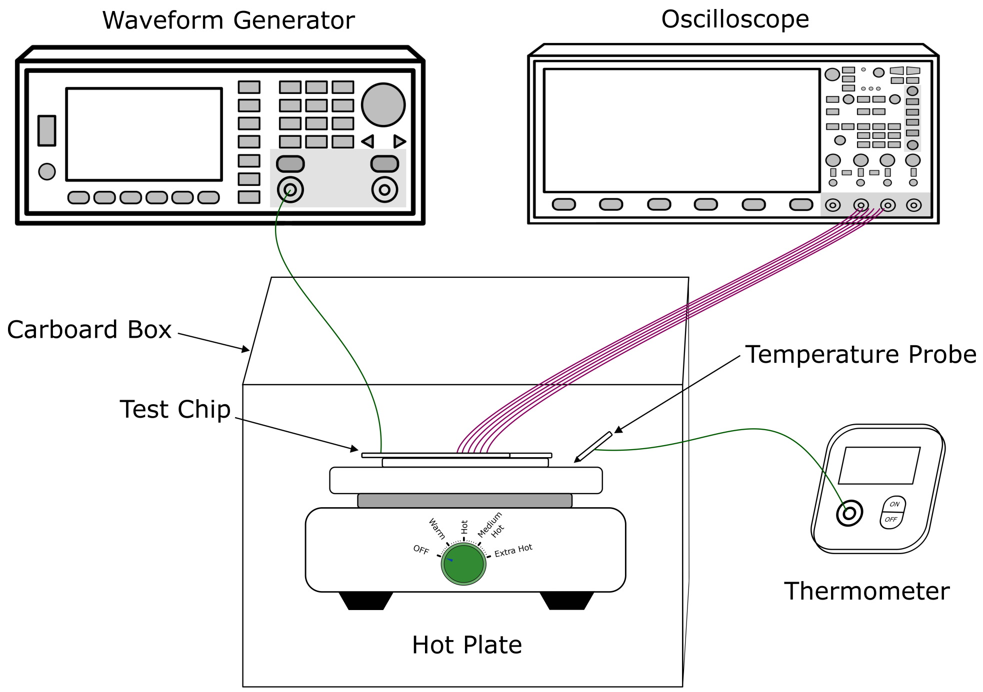


Fig. 5.26 Test setup of temperature variation. The waveform generator generates the same waveform for V_{dd} as shown in Fig. 5.17. Oscilloscope is used to monitor the $Event_{up}$ pulse during the heating period in the cardboard box. The thermometer is used to monitor the temperature in cardboard box.

Temperature variation is a significant factor for sensing in general. The temperature variation of the fabricated chip has been investigated experimentally. The experimental setup of temperature variation consists of an electric hot plate, a thermometer and a cardboard box as shown in Fig. 5.26. The connections between waveform/oscilloscope and test chip are the same as the setup shown in Fig. 5.4.4. In the test of temperature variation, the test chip was placed on the hot plate and both were placed in a cardboard box to maintain the temperature. The thermometer was used to monitor the temperature in the cardboard box which ranged between 23°C to 100°C, and the predefined voltages (975mV and 1V) are picked as an example to show the temperature variation. This experiment involved two steps. First, was the detection of 975mV at room temperature (26°C). Once 975mV was detected, $Event_{up}$ is pulled up and shown in the oscilloscope. Second, the temperature inside the cardboard box was gradually increased using a hot plate; in the meantime, the change of $Event_{up}$ was monitored in the oscilloscope. If any changes occur in $Event_{up}$, the temperature on the thermometer is recorded immediately. For example, the pulse of $Event_{up}$ is pulled up earlier or later compared to the pulse generated at room temperature in the first step. For testing the temperature variation of detecting 1V, the same test method is used.

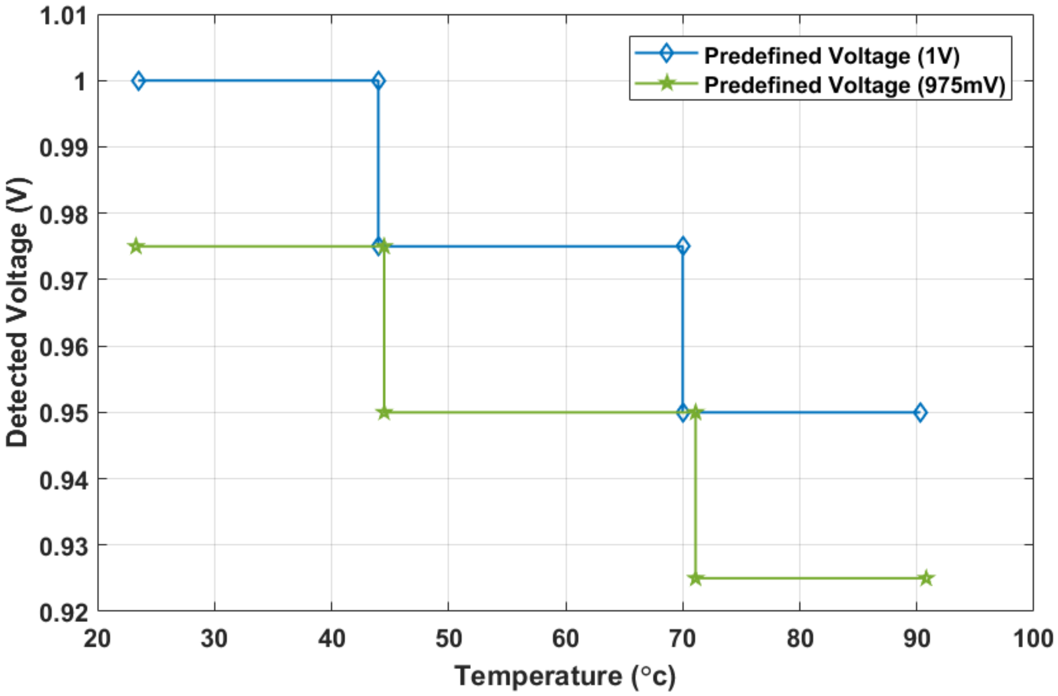


Fig. 5.27 Temperature variation of voltage detection.

Fig. 5.27 shows the different performances when the environment temperature has been changed within the preset temperature range. Two predefined voltages were tested which means that these two voltages are supposed to be detected at room temperature (26°C) with the predefined *Delay*s. It is apparent that the detected voltage is decreased with the increase of temperature. For both the predefined voltages, the reference-free voltage monitoring system maintained accurate detection until the temperature increased to around 45°C. When the temperature was over 45°C, the detected voltage decreases one ΔV which is 25mV in our test, for example, in Fig. 5.27 in which if the predefined voltage was 1V at room temperature, the actual detected voltage was the predefined voltage (1V). However, if the temperature increased to 45°C, the detected voltage was 975mV that is smaller than the predefined voltage (1V). Similarly, when the temperature increased to about 72°C, the detected voltage dropped two ΔVs which was 50mv in total compared to the predefined voltage. However, ΔV itself remained at 25mV regardless of the temperature. These results show that a resolution of ΔV = 25mV is realistic at three different temperature ranges, below 45°C, between 45°C and 72°C and above 72°C.

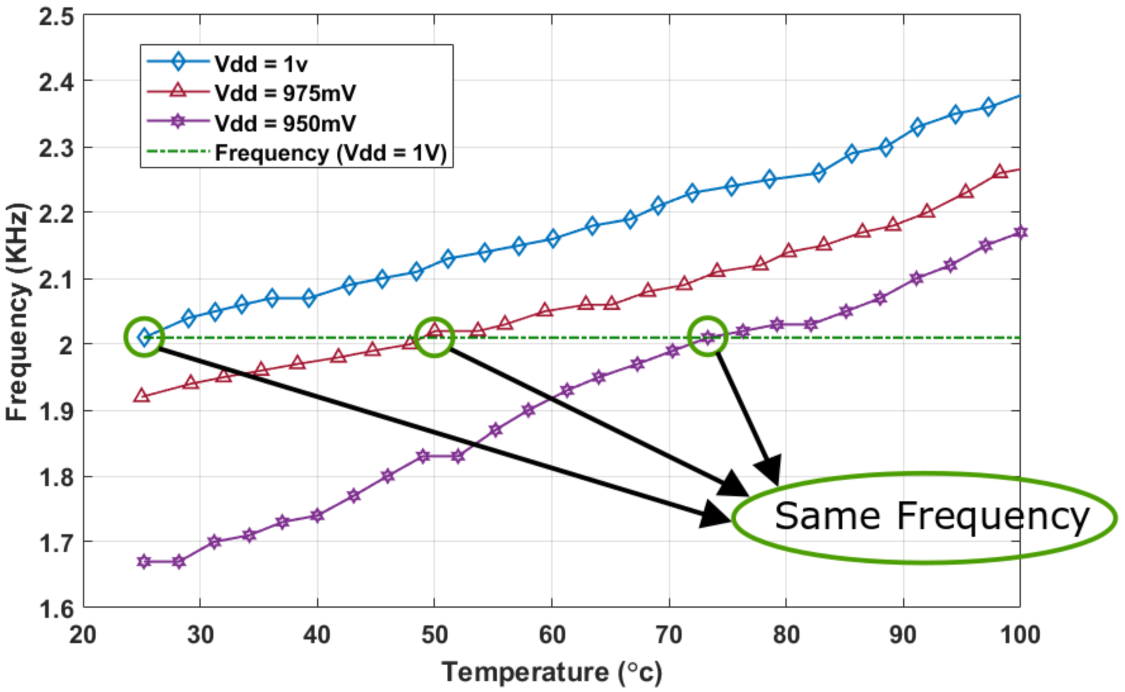


Fig. 5.28 Frequency variations over temperature. This figure explains the reason why the actual detected voltage decreases with the increase of temperature in Fig. 5.27. These two predefined voltages at room temperature can generate the frequency at specific temperatures. The method for this experiment involves randomly selecting three temperatures within every 10°C and recording the corresponding generated frequency.

According to [32], frequency increases with increase of temperature when V_{dd} is stable. Fig. 5.28 shows the temperature variation of the frequency. This figure illustrates the reason the actual detected voltage decreases with increase of temperature. The reason is that the same frequency is generated under the specific temperatures even if different V_{dd} is supplied in the reference-free voltage monitoring system.

As is evident, the temperature increases result in frequency increases within the temperature range of 23°C to 100°C. The performance of oscillation has been tested in different V_{dd}s 1V, 975mV and 950mV, respectively. These three different voltages achieved the same frequency at some specific temperatures. For instance, when the temperature was 23°C, the frequency was 2.01kHz at V_{dd} = 1V, however, if the temperature was changed to 49°C, the frequency increased to 2.11kHz. On the other hand, if the V_{dd} was changed to 975mV, the frequency was 1.92kHz at 23°C and increased to 2.01kHz at 49°C which is same as V_{dd} = 1V and temperature was 23°C. Similarly, when V_{dd} = 950mV, the voltage-controlled oscillator could also generate 2.01kHz frequency at around 72°C as shown in Fig. 5.28. As discussed in Section 4, this proposed reference-free voltage monitoring system determines the predefined voltage by detecting the period of *clk* generated from the voltage-controlled oscillator. Therefore, the detected voltage decreases with increase of temperature as the same frequency is generated under a higher temperature as shown in Fig. 5.27.

5.6 Summary

A novel reference-free voltage monitoring system was presented in this chapter. This design of the reference-free voltage monitoring system is based on the proposed time comparison-based voltage level-crossing sensor presented in Chapter 4. The design is implemented in 350nm AMS technology using the Cadence toolkit, simulated, and fabricated. The resulting chip is repaired to working condition and tested, using a specially designed testing rig. The simulation and measurement results were compared. These show that the achievement of the design goal and the method results in fully realising the desired reference-free voltage monitoring system functionalities. There are five contributions in this chapter: 1). A new voltage sensor with multiple-level detection was presented without external or internal voltage reference. 2). This sensor was tested by measuring the voltage range from 0.85V up to 1.2V with 25mV increment using the new time comparison technique with the internal reference time. 3). The voltage precision of this reference-free voltage monitoring system can reach 25mV when voltage increases. 4). The reference-free voltage monitoring system is shown to have short response times. 5). The method of preparing the chip was presented for the researcher who may need it.

It is apparent that the reference time error is another potential issue which could affect the detection result as shown in Table 5.4. The detection error rate may be reduced if the monitoring precision requirement is relaxed from 25mV. In addition, we tested the temperature effects of this reference-free voltage monitoring system. The temperature varied from 23°C to 100°C. During the variation of temperature, the system kept voltage precision stable which is 25mV. However, because of the discrete nature of the reference-free voltage monitoring system, at certain temperatures, errors of an entire resolution step (e.g. 25mV) may suddenly appear (e.g. at 45°C and 72°C in Fig. 5.27). Consequently, different ΔV selections will yield different working range boundaries. As is the norm with sensors, this may be dealt with through characterisation and calibration. Online calibration is also possible if the temperature can be measured at runtime. For instance, if it is known that the temperature has entered the range of 45°C -72°C, it would be trivial to offset the sensor by 25mV to compensate as in the example presented in this chapter.

With smaller technology nodes, it is expected that such a reference-free voltage monitoring system will start working from even lower voltages, bringing the voltage detection range down to even lower amounts of available energy from the energy harvesting. This conjecture remains untested and is one of the plausible next steps of potential future work.

Chapter 6

Time comparison-based capacitance-to-digital converter

6.1 Introduction

Existing capacitance-to-digital converters tend to require long measurement times such as 1s in [43], 100ms in [106] and 7.6ms in [27]. As shown in Table 6.2, the corresponding energy consumptions are also relatively high at 5mJ, 1020nJ and 1603.6nJ, respectively. Therefore, a new design that shortens the conversion time and, as a result, saves energy would be desirable. Further, an enhanced design would help avoid high-quality external energy sources for improving system robustness in variable energy environments during digital conversions. The proposed capacitance-to-digital converter in this chapter is based on the time comparison technology presented in Chapter 4. The proposed capacitance-to-digital converter described in this chapter is based on the time comparison technology presented in Chapter 4 and has been designed to shorten conversion time and reduce energy consumption. In addition, this chapter includes a follow-up design based on the temperature variation experiment results in Chapter 5. The basic inverter-based voltage-controlled oscillator is replaced by the current-starved voltage-controlled oscillator due to its low sensitivity of temperature. The design, implementation, and simulation validation of this converter are presented. The end of this chapter includes a temperature variation test.

6.2 Energy-efficient time comparison-based capacitance-to-digital converter

6.2.1 Overview of the time comparison-based capacitance-to-digital conversion system design

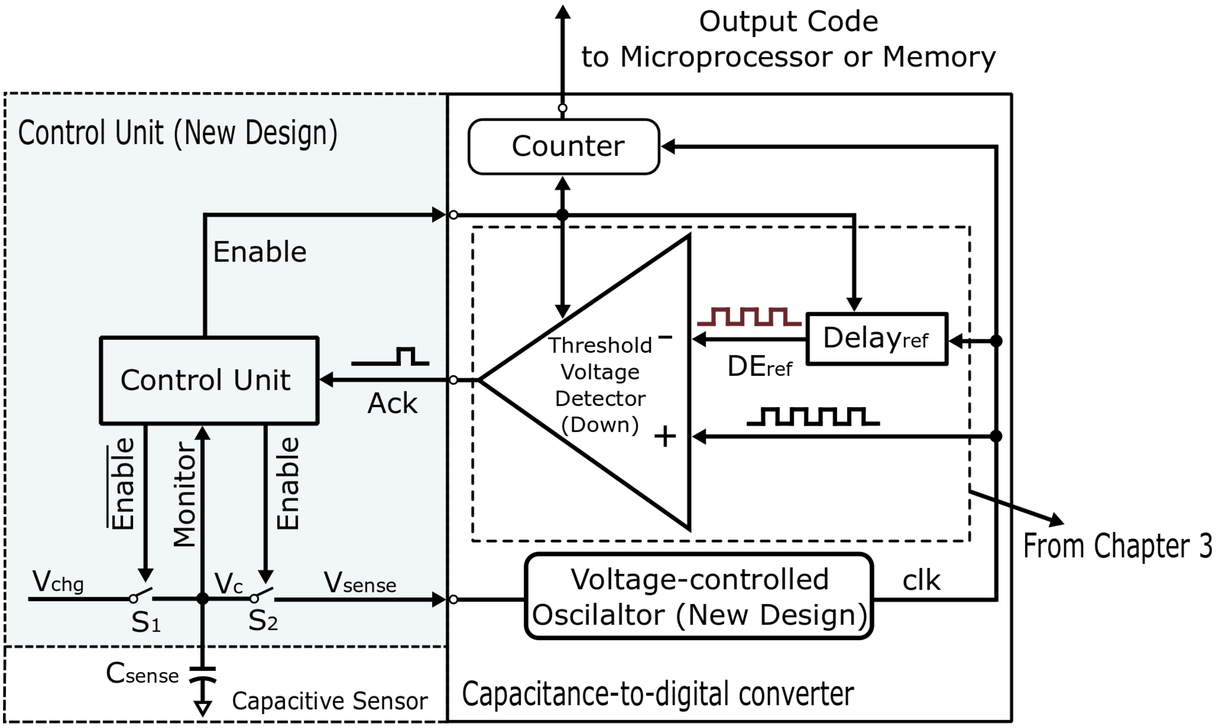


Fig. 6.1 Block diagram of the time comparison-based capacitance-to-digital converter with a control unit. The entire system is powered by a regulated output DC from the voltage regulation part, as shown in Fig. 1.2. Hence, V_{dd} is a stable parameter in this system. The control unit controls the switches S_1 and S_2 to charge/discharge the sensed capacitor (C_{sense}), which is the capacitive sensor shown in the system diagram in Fig. 1.2, and the output code is connected to the microprocessor or memory for future processes. The capacitance-to-digital converter consists of a counter for counting the number of generated *clk* pulses during the digital conversion period. The time comparison-based voltage level-crossing sensor (down) has three blocks: threshold voltage detector (down), voltage-controlled oscillator, and a $Delay_{ref}$ generator, as presented in Section 4.2. The counter can be placed either on a chip or off it.

Fig. 6.1 shows the block diagram of the energy-efficient time comparison-based capacitance-to-digital converter with a control unit. The capacitance-to-digital converter runs once per round of sensing (of the value of C_{sense}). Before a round of sensing starts, the sensed capacitor (C_{sense}) is charged by V_{chg} up to a known V_{ref} (= V_{dd} in the experiments presented in this chapter), V_c (the voltage across C_{sense}) = V_{chg} = V_{ref}. Once that happens, the control unit may disconnect C_{sense} to V_{chg} and start a round of conversion by issuing the *Enable* signal and connecting V_c to V_{sense}, which is discharged through an RC circuit integrated into the voltage-controlled oscillator, as shown in Fig. 6.7. The voltage-controlled oscillator then runs according to V_{sense}, which reduces with the depletion of the charge on C_{sense} according to the discharging of the RC circuit, as introduced in Section 2.2.2. It generates the V_{sense}-dependent clock (*clk*). The voltage level-crossing sensor compares *clk* with DE_{ref} (See Fig. 4.13). When the two clocks coincide, the voltage level-crossing sensor indicates the end of the conversion to the control unit by issuing the *Ack* signal. The counter records the number of oscillations (known as conversion steps) between the *Enable* and *Ack* signals, which is a function of the original charge on C_{sense} under $V_{ref}(=V_{dd})$, and, therefore, also a function of the value of C_{sense}.

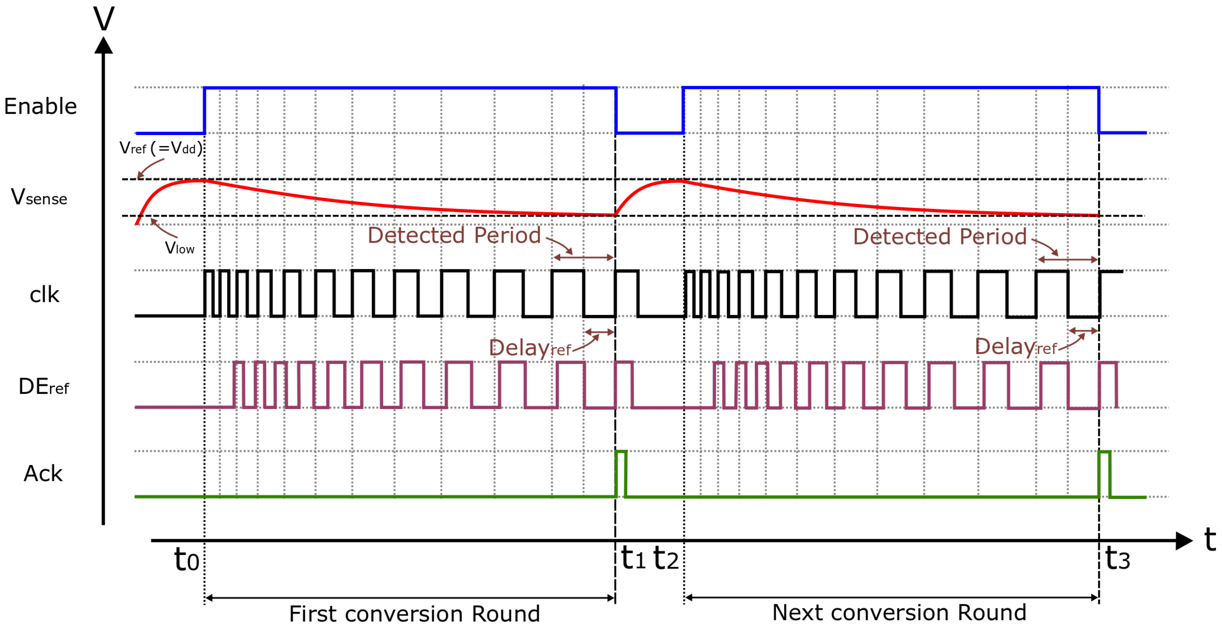


Fig. 6.2 Timing diagram of the proposed time comparison-based capacitance-to-digital converter. The digital conversion starts once the *Enable* signal is issued (at time t_0 and t_2) and stops when the *Ack* signal is issued (at time t_1 and t_3), thus during the time intervals between t_0 and t_1 or between t_2 and t_3, the number of *clk* pulses are counted by the counter as shown in Fig. 6.1.

$Delay_{ref}$ is a constant time delay determining the predefined period according to the final known V_{low}, which is implemented using an RC circuit that determines when the conversion should end, as explained in Chapter 4. After the *Ack* signal is issued, the control unit disconnects C_{sense} from the voltage-controlled oscillator and reconnects it to V_{chg}, in preparation for the next round of sensing. C_{sense} may be different for different sensing rounds. For instance, the value of C_{sense} may be related to a physical property such as pressure or temperature, which can be detected by using the capacitance-to-digital converter to measure C_{sense}. The starting point of V_{sense} for every conversion round is always the same, V_{ref}, but the energy depletion monitored by the voltage-controlled oscillator may be different, as C_{sense} may not be constant. This results in a varying number of conversion steps per conversion round, as recorded by the counter corresponding to different C_{sense} values [23, 28]. Fig. 6.2 shows the main waveforms recorded during two sensing rounds with the same C_{sense} value.

6.2.2 Mechanism of the digital conversion

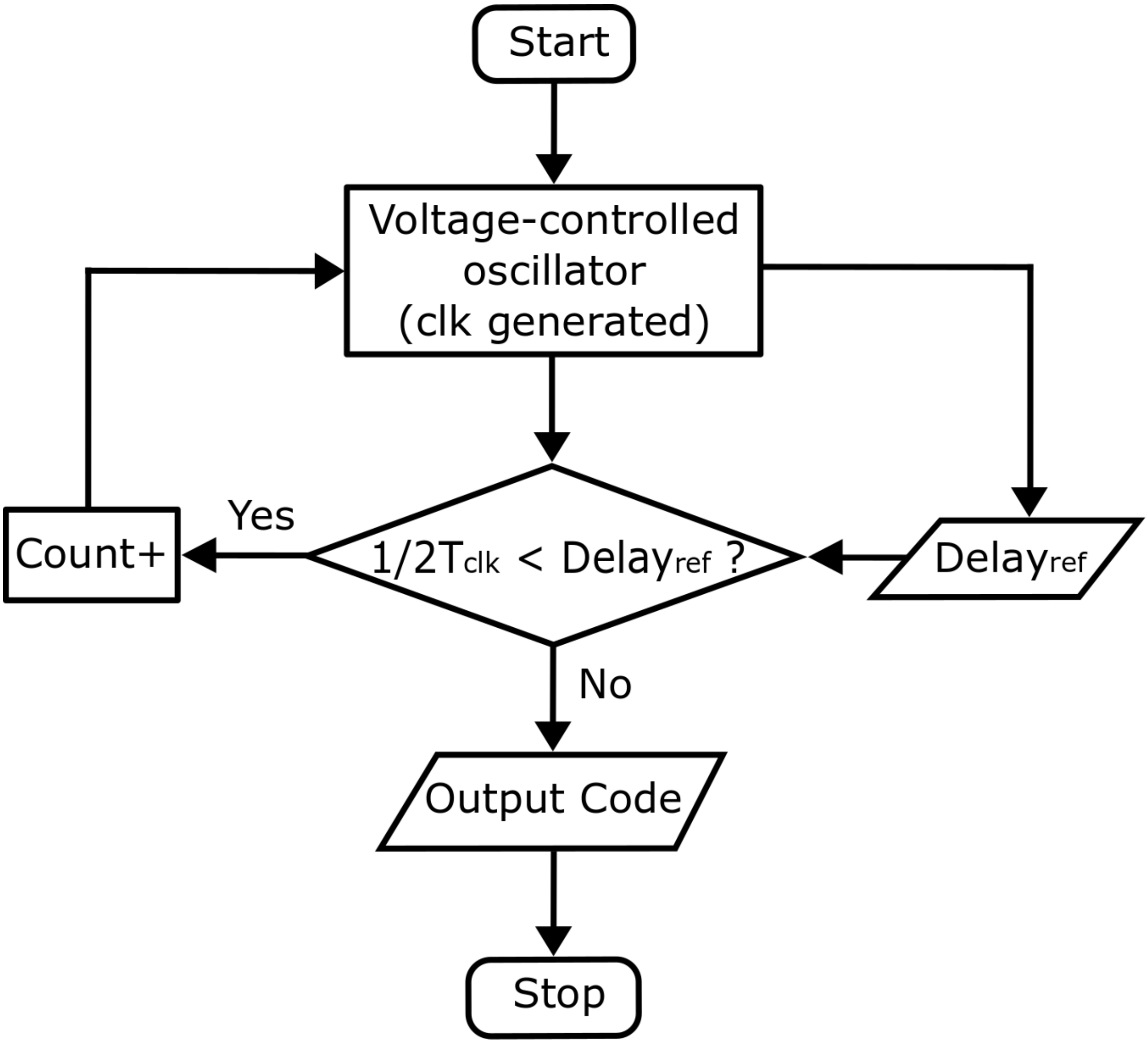


Fig. 6.3 Flowchart of the working mechanism of the proposed capacitance-to-digital converter. *clk* is the V_{sense}-dependent clock. T_{clk} is the period of *clk*. $Delay_{ref}$ is predefined delay time corresponding to V_{low} as shown in Fig. 6.2. In the implementation stage, the $Delay_{ref}$ is considered to be half of the predefined period according to the predefined threshold voltage as presented in Section 4.4.2.

Conventional methods require a reference voltage during the digitisation, and the reference voltage provided by the external voltage supply [4, 28, 111], which means that the system depends on an external voltage reference for its digitisation step. In comparison, the proposed approach uses the clock self-comparison method to determine the final discharged voltage using the method presented in Chapter 4. Fig.6.3 shows the counting operation of the counter illustrating that the basic algorithm of digital conversion. When the digital conversion starts to work, the voltage-controlled oscillator block generates the *clk* with T_{clk} period, which is sent to the threshold voltage detector (down) and internal time reference generator block, at which point the predefined time delay ($Delay_{ref}$) is applied into *clk* to generate DE_{ref} according to the final discharged low voltage as presented in Chapter 4. Then, T_{clk} and period of DE_{ref} ($T_{DE_{ref}}$)

are compared in threshold voltage detector to determine the smaller value between $1/2T_{clk}$ and $Delay_{ref}$. If $1/2T_{clk} < Delay_{ref}$, the counter increments by '1' and the conversion continues until $1/2T_{clk} \geq Delay_{ref}$, at which point the system outputs the number of stored counts to represent the capacitance of C_{sense} as shown in Fig. 6.1.

6.3 Circuit implementation

The circuit implementation process is presented in this section. As the threshold voltage detector (down) of the capacitance-to-digital converter and its circuit implementation are presented in Fig. 4.12 of Chapter 4, this section is focused on the circuit implementation of the control unit and the current-starved voltage-controlled oscillator used to replace the basic inverter-based voltage-controlled oscillator as shown in [32], to reduce the temperature dependency.

6.3.1 Control unit

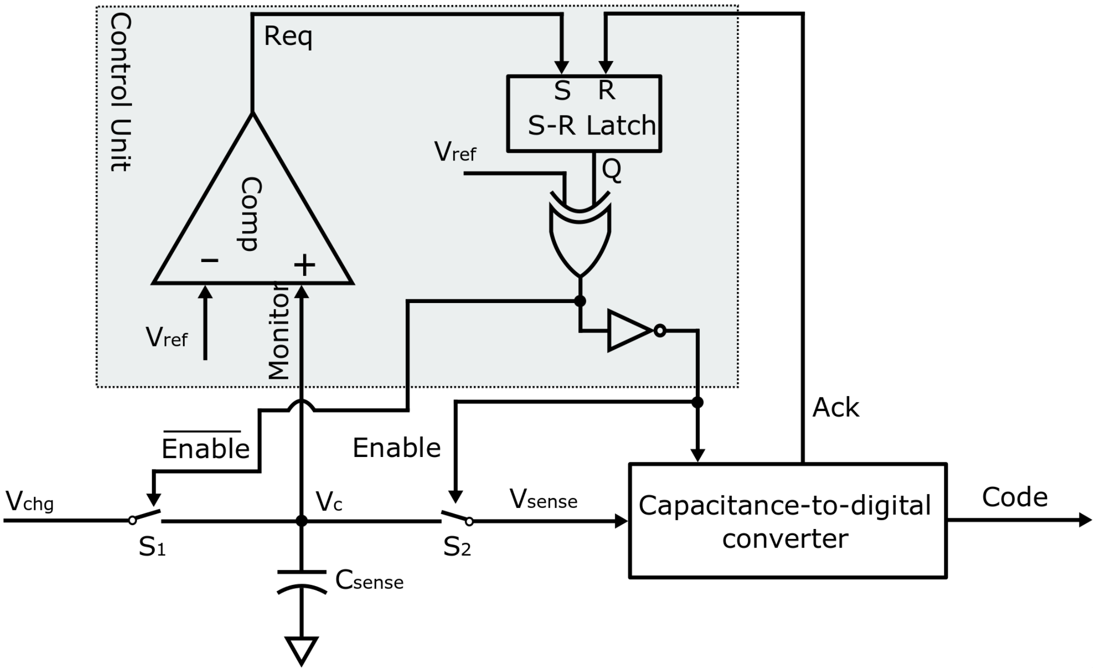


Fig. 6.4 Circuit diagram of the control unit. The control unit is used to monitor the voltage across C_{sense} to issue the *Enable* signal and receive *Ack* signal to finish the current conversion round and start the next round.

Fig. 6.4 shows the circuit diagram of the control unit. As discussed in the previous section, the control unit is only used to detect C_{sense} charging state. In other words, during the digital conversion, the control unit is turned off until the *Ack* signal is generated and fed to the control unit. The *Ack* signal is generated when the digital conversion is completed. Once the control unit receives the *Ack* signal, the control unit disables the digital conversion and starts monitoring the V_c until it is fully charged. The proposed control unit consists of a voltage comparator, a standard SR latch, an XOR gate and an inverter. When the entire system is working, the voltage comparator generates the *Req* signal if the V_c crosses V_{ref}. Here, the voltage comparator only works once per round of sensing to monitor whether the V_c is fully charged. The use of a control unit to monitor whether the charging has achieved V_{ref} takes the high-precision V_{ref} signal out of the energy path and makes it possible to charge the capacitor with a low-quality, low-precision V_{chg} as long as it has enough energy to charge C_{sense} up to V_{ref}. V_{dd} is the stable voltage regulated by the input DC (See Fig. 1.2). Meanwhile, both the *Req* signal and *Ack* generated from capacitance-to-digital converter are fed to the SR latch. Both of them work together to trigger two switches (S_1 and S_2) which turns the capacitance-to-digital converter on/off. Table 6.1 shows the truth table of the control unit.

Table 6.1 Truth table of control unit

Req	Ack	Q	V_{ref}	$\overline{Enable}$	Enable
0	0	0	1	1	0
1	0	1	1	0	1
0	0	1	1	0	1
0	1	0	1	1	0

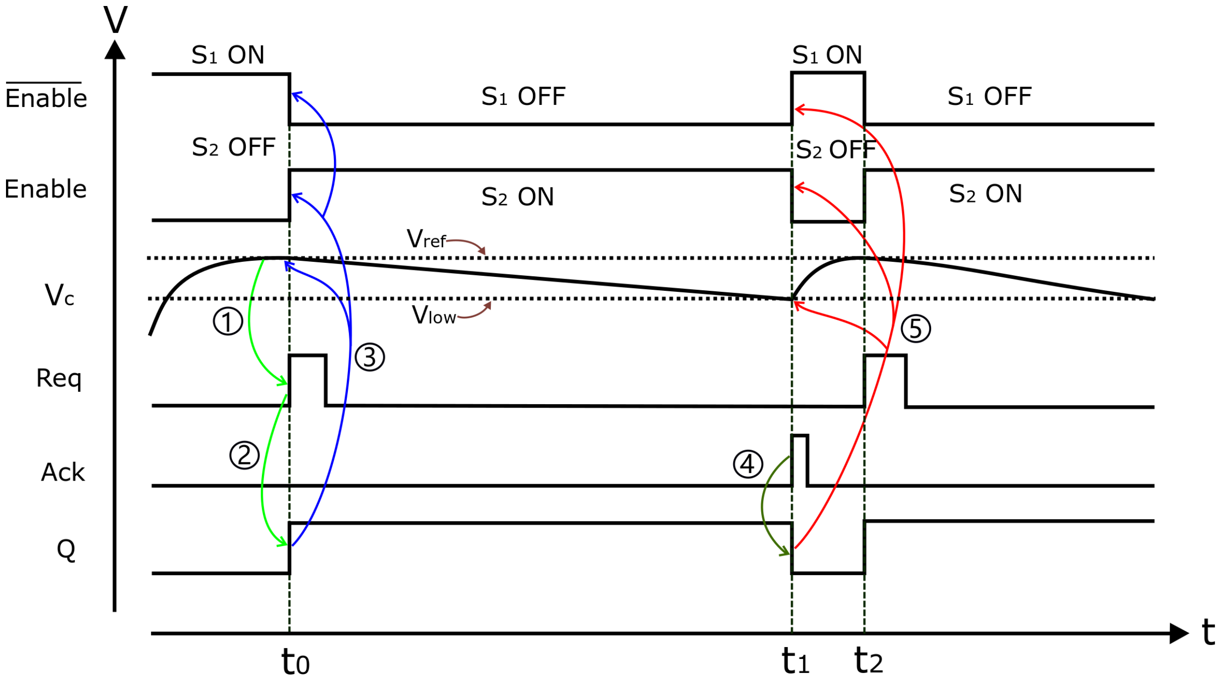


Fig. 6.5 Timing diagram of the operating in control unit. At t_0, V_c is fully charged to V_{ref}, the capacitance-to-digital converter starts digital conversion. At t_1, V_c discharges to V_{low}, the digital conversion ends.

Fig. 6.5 shows the timing diagram of the charging control unit's operation. The switch S_1 is initially in a closed state and S_2 is open. When the control unit starts working, the closed S_1

means that C_{sense} is charging as shown in Fig. 6.5. V_c increases over time until it reaches the reference voltage V_{ref} (at t_0), and then the *Req* signal is pulled down from logic ‘0’ to ‘1’ (step 1). Due to the function of the SR latch, the Q signal becomes logic ‘1’ (step 2). Consequently, $\overline{Enable}$, which is the output of XOR gate, is immediately forced to ‘0’ immediately (step 3), which means that S_1 gets switched off. In the meantime, the *Enable* signal is forced to ‘1’ (step 3). Once *Enable* is changed to ‘1’, S_2 immediately gets closed. Then, the V_c starts to gradually discharge and the capacitance-to-digital converter starts converting the value of C_{sense} to digital code until the digital conversion is completed (at t_1). As explained in Fig. 4.13, Chapter 4, the *Ack* signal is generated when the predefined $Delay_{ref}$ has been reached. Once the *Ack* signal is generated (step 4 at t_1), the switch S_1 gets closed and S_2 opens to allow C_{sense} to charge again (step 5). The control unit then restarts and begins a new V_c monitoring round until V_c reaches V_{ref} for the next conversion round at t_2 as shown in Fig. 6.5.

For the voltage comparator, a standard circuit design found in [[123], Fig. 3.13] is adopted within the design of the charging control unit. The design of this comparator is not critical for the sensor’s response time and power as it has negligible delay and energy consumption in the context of the entire sensor, and designing a sophisticated voltage comparator is outside the scope of this thesis.

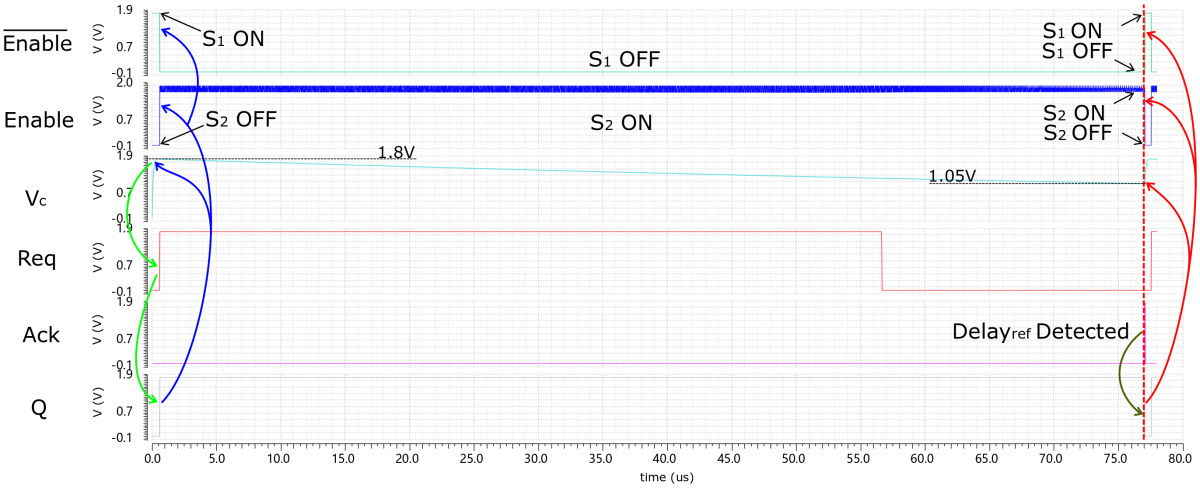


Fig. 6.6 The simulation result of the operation of the control unit. In this simulation, the C_{sense} is 7pF and initially charged to 1.8V, and then the capacitance-to-digital converter starts working to discharge C_{sense} until the V_c discharges to 1.05V (V_{low}).

The simulation result of the operation of the control unit is shown in Fig. 6.6. Compared to the mechanism shown Fig. 6.5, all of the functionalities of the control unit are achieved. When *Enable* is low, C_{sense} is charged and when *Enable* is high, C_{sense} is discharged. At the end of the C_{sense} discharge, *Ack* is generated to flip *Enable* again for the next round of charging.

6.3.2 Current-starved voltage-controlled oscillator

The proposed capacitance-to-digital converter uses a voltage-controlled oscillator to convert the energy stored on C_{sense} into the clock (*clk*) as presented in Chapter 2. The PVT variations play a vital role during the system operation, and the temperature variation, especially, can be a serious issue in the quantitative elements of the sensors [124]. Therefore, the voltage-controlled oscillator should have lower temperature sensitivity. Based on the temperature variation experiment results given in Chapter 5, the basic inverter-based voltage-controlled oscillator has high temperature sensitivity . G.Jovanovic in [32] suggested that current-starved inverters with output-switching could provide frequency stability even with temperature variations. Consequently, the five-stage current-starved voltage controlled oscillator adapt techniques from [32] for our voltage-controlled oscillator design rather than using the basic inverter-based voltage-controlled oscillator used in Chapter 5.

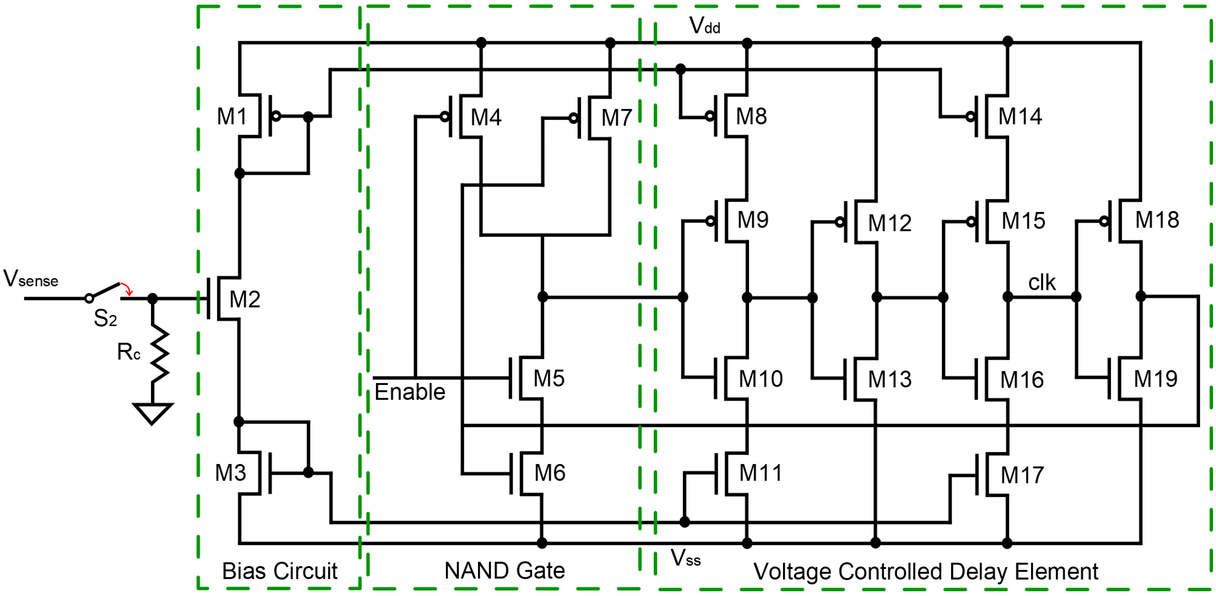


Fig. 6.7 Circuit diagram of the modified five-stage current-starved voltage-controlled oscillator adapted from [32]. R_c is equal to 20MΩ. For the all transistors, the width = 10μm and the length = 0.35μm.

Here, the current-starved voltage-controlled oscillator has been implemented by modifying the oscillator design from [32], which consists of one bias circuit, one NAND gate and one voltage controlled delay element as shown in Fig. 6.7. The voltage controlled delay element consists of two current-starved inverters and two basic inverters powered by a constant V_{dd}. Current-starved inverters are used in the delay element to improve the temperature independence [32]. The bias circuit includes transistors M1, M2 and M3, and provides the V_{sense}-dependent current to the following two current-starved inverters (formed by M8, M9, M10, M11 and M14, M15, M16, M17, respectively). The *Enable* signal controlled NAND gate is used to switch the oscillator on/off. M8 and M11 operate as the current sink and source, respectively, and receive the V_{sense}-dependent current from the bias circuit. M14 and M17 perform the same function. The current sink can limit the peak of current in an inverter and can vary the delay, which means that the inverter is starved for current. This combined voltage-controlled oscillator has good stability for both temperature variations and V_{dd} variations [32].

The concept of the proposed capacitance-to-digital converter is based on detecting a time delay,i.e. detecting the clock period changes rather than the voltage changes. The precharged C_{sense} is connected to R_c, when the switch S_2 is closed, causing it to discharge from a known voltage V_{ref} to a $Delay_{ref}$-dependent known voltage V_{low} as shown in Fig. 6.2. The most straightforward method is the one adopted in Section 3.3.3, where in the voltage across C_{sense} is directly discharged over a voltage-controlled oscillator, generating the clock periods for comparison with a reference delay time. However, such a voltage-controlled oscillator based on simple inverters may not provide good temperature independence. Here, we explore a different strategy by discharging through a constant R_c. This is coupled with a current-starved voltage-controlled oscillator, which has better temperature stability, to achieve the same functionality as the method found in Section 3.3.3. The inverters in this current-starved voltage-controlled oscillator are not powered by the discharge voltage but by the stable V_{dd}. As a result, the frequency of the oscillation tracks the discharge voltage, but the amplitude of the oscillation stays the same. This is conceptually shown in Fig. 6.8b.

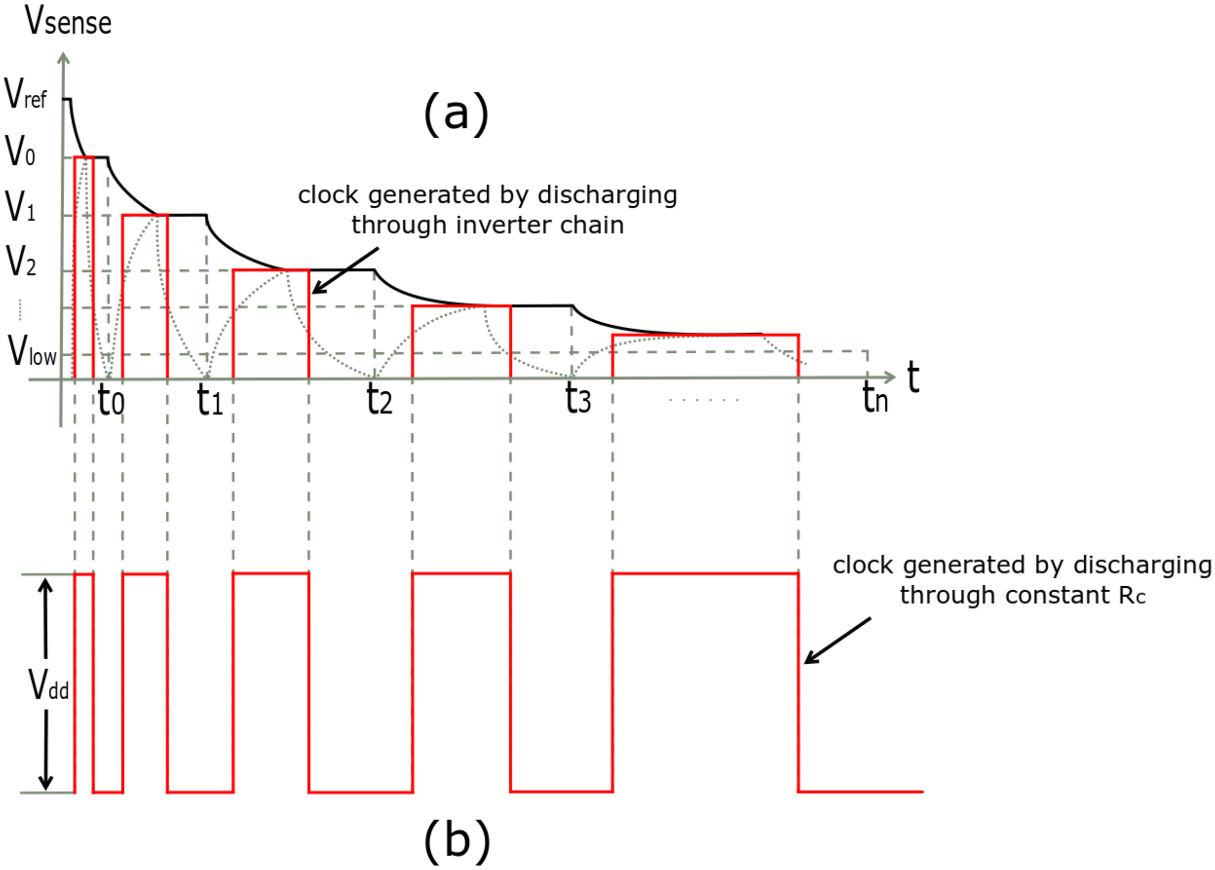


Fig. 6.8 The clock generation from: (a) C_{sense} is discharged by an inverter chain adapted from [8, 33]; and (b) C_{sense} is discharged by a constant R_c.

Fig. 6.8 shows the clock generation of the two different discharge processes. Fig. 6.8(a) shows the clock generation when C_{sense} discharges through an inverter chain presented in Section 3.3.3

and [8, 33]. Since the oscillator consumes the discharged energy, the amplitude of oscillation follows the drop of V_{sense} shown in Fig. 6.8(a). However, with the current-starved voltage-controlled oscillator proposed in this section, the energy is consumed by a constant R_c while the oscillator is powered by a constant V_{dd}. Hence, the amplitude of the clock is V_{dd}, but the clock period is related to V_{sense} (input voltage of the current-starved voltage-controlled oscillator as shown in Fig. 6.7). As V_{sense} reduces, the clock period increases. In this solution, the value and stability of V_{dd} are not important as the output clock signal of the current-starved voltage-controlled oscillator depends on V_{sense} and is not sensitive to V_{dd} changes. As a result, there is no requirement for a high-quality V_{dd}.

This capacitance-to-digital conversion system (see Fig. 6.1) is designed for use in an environment where a stable V_{ref} can be found. However, this high-quality constant voltage is only used as a pure reference voltage to help control the C_{sense} charging process, with negligible power contribution. The energy-supplying voltages, V_{chg} for charging C_{sense} and V_{dd} for powering the current-starved oscillator, do not have to be a high quality and can sustain variations. V_{chg} is only required to be able to charge C_{sense} to V_{ref}. In other words, V_{chg} should be higher than V_{ref} at the point where C_{sense} gets charged to V_{ref}. Other variations in the V_{chg} do not affect the sensor's operations. The variability tolerance is also high for V_{dd}, which powers the current-starved oscillator, as discussed in [32], and has an error of less than 2% over 18% V_{dd} variations. These design features makes it suitable for embedded applications where stable power supply voltages may be difficult to find but one single stable voltage that does not supply much energy can be made available.

6.4 Circuit design and simulation results

The proposed capacitance-to-digital converter is designed and implemented on 350nm CMOS AMS technology node, using the Cadence IC design tools. Fig. 6.9 shows the complete schematic of the energy-efficient time comparison-based capacitance-to-digital conversion system. The C_{sense} is varied from 0pF to 10pF with 1pF increment, and both V_{dd} and V_{ref} are 1.8V during the experiment.

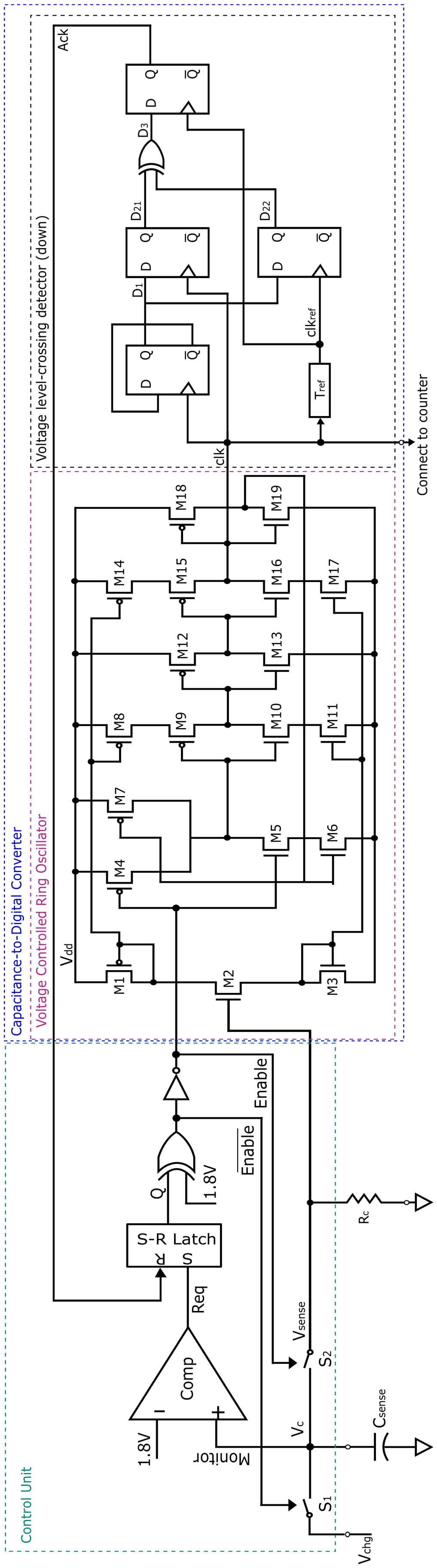


Fig. 6.9 Complete schematic of the time comparison-based capacitance-to-digital conversion system.

6.4.1 Performance of the current-starved voltage-controlled oscillator

Although the voltage-controlled oscillator has been partly adapted from others' work, the performance of the oscillator is a significant factor in the overall conversion process. In this section, we simulated the oscillation under a varied input control voltage (V_{sense} in this design as shown in Fig. 6.9) from 1V to 1.8V in increments of 50mV. Fig. 6.10 shows the relationship between the frequency and input control voltage.

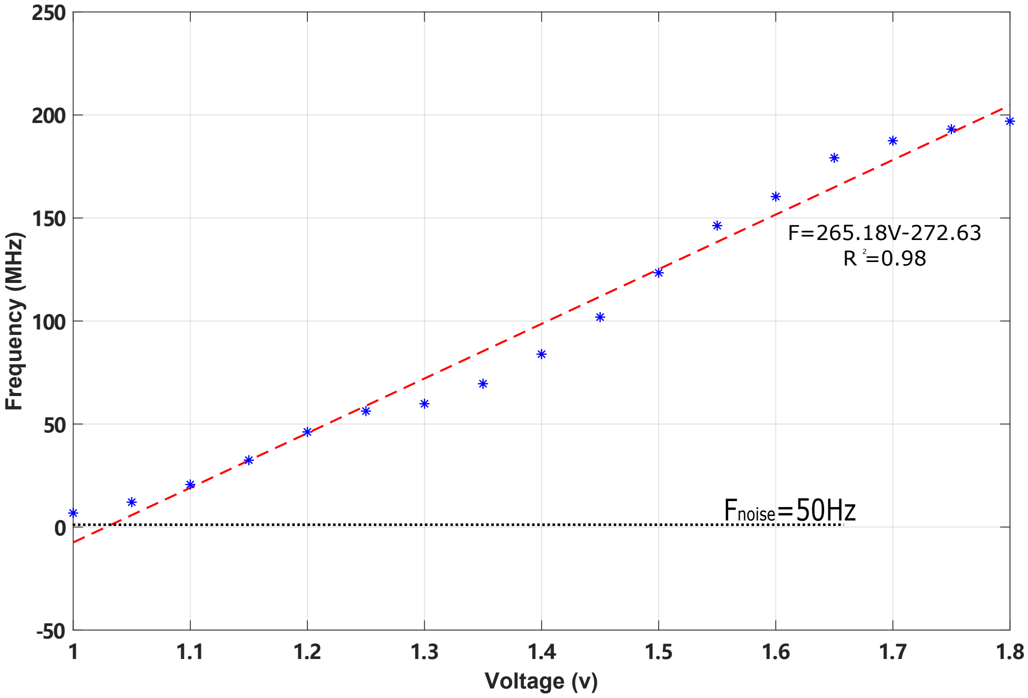


Fig. 6.10 Frequency characteristics. The input control voltage is increased from 1V to 1.8V with 50mV increment, and the highest frequency is 197MHz at 1.8V and lowest is 6.8MHz at 1V.

Curve fitting to a straight line resulted in an R-squared value of 0.98, close to '1'. This means that the proposed current-starved voltage-controlled oscillator has good linearity (See Fig. 6.10). Fig. 6.11 shows the linearity error of voltage-dependent frequency, which was calculated based on the difference (from the actual measured value and calculated value of the equation in Fig. 6.10) and the actual measure value as shown in the following equation:

$$L.Error = \frac{Actual\ Frequency - Calculated\ Frequency}{Actual\ Frequency} \times 100\% \tag{6.1}$$

where *L.Error* is the linearity error. *Calculated Frequency* is calculated by the equation as shown in Fig. 6.10. *Actual Requency* is the measured frequency of the circuit.

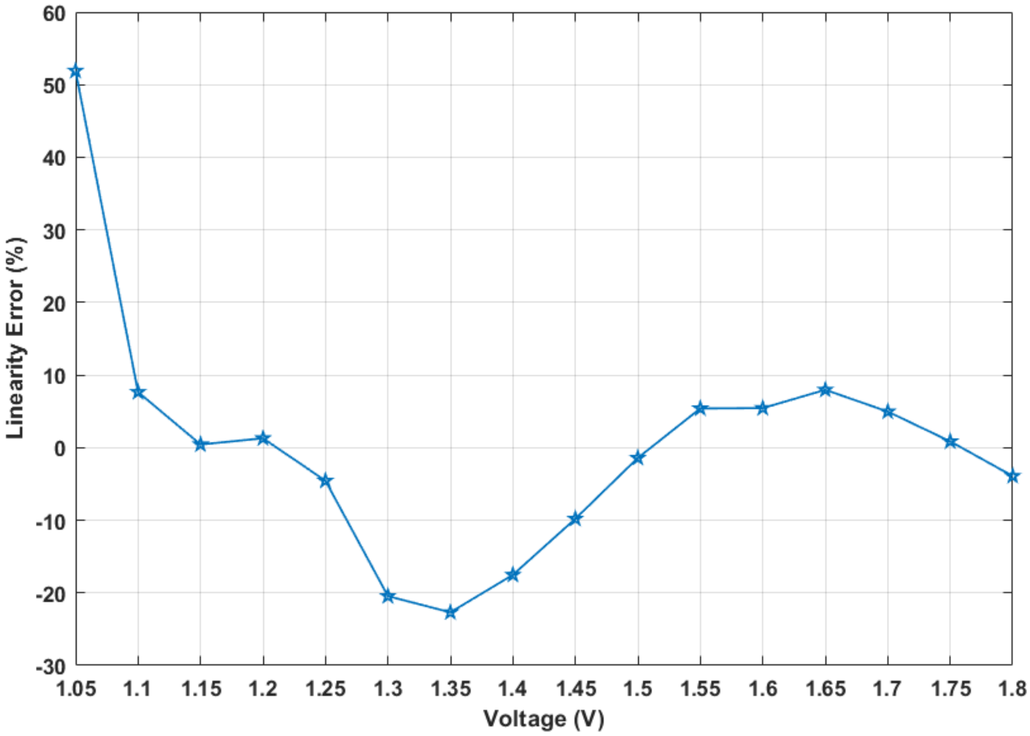


Fig. 6.11 Linearity error of voltage-dependent frequency. The linearity is better when the voltage is over 1.05V as shown in this figure. Hence, the V_{low} is set at 1.05V in the simulation. When the voltage is 1V, the linearity error at 1V is eliminated due to the negative frequency calculated according to the equation shown in Fig. 6.10.

The maximum error is 51.91% at 1.05V and the minimum error is 0.44% at 1.15V. In addition, as the capacitance-to-digital converter stops working at a constant V_{low}, the V_{low}-dependent $Delay_{ref}$ can be estimated from the actual measured frequency. According to the concept presented in Section 2.2.2 and the actual generated frequency at 1.05V in the simulation presented in Section 6.4.2, the estimated value of resistor (R_{ref} used in the delay generator presented in Section 4.4.2) is 8MΩ and the constant capacitance (C_{ref}) used is 10fF.

6.4.2 Performance of capacitance to digital conversion

As mentioned at the beginning of Chapter 6, the range of C_{sense} is from 0pF to 10pF with a 1pF increment, V_{dd} is 1.8V, the nominal operating temperature is 27°C, and the final detected voltage (V_{low}) is equal to 1.05V.

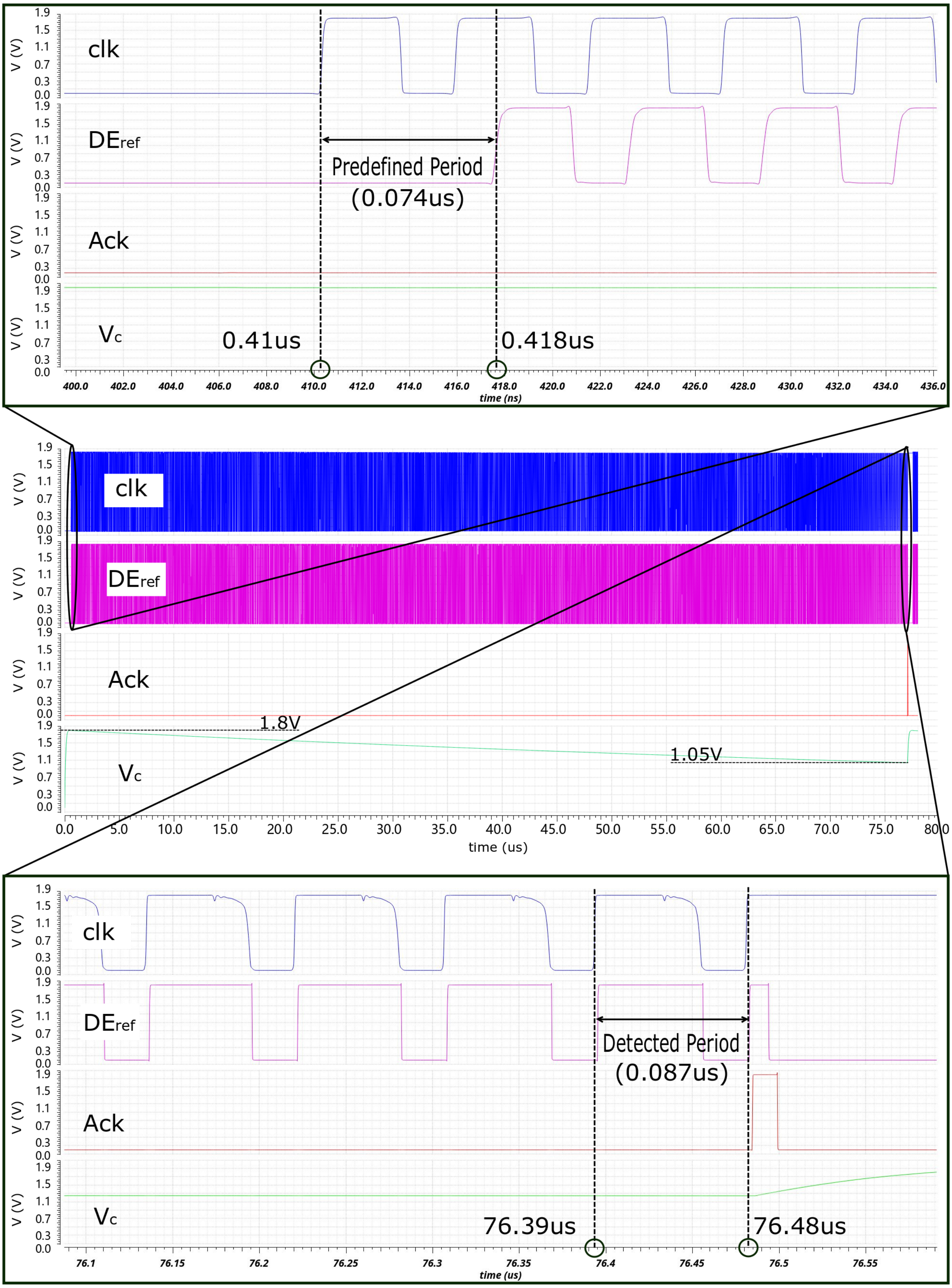


Fig. 6.12 Waveforms of one conversion round when C_{sense} is equal to 7pF. The clk was generated and fed to the counter when C_{sense} is charged to 1.8V at 0.41μs until V_c drops to V_{low} (= 1.05V) at 76.48μs. The counted number of clk's pulses is used to represent the value of C_{sense}. The top subfigure is the zoomed-in representation of the beginning of conversion, and the bottom subfigure is the zoomed-in representation of the end of the conversion.

Fig. 6.12 shows the waveforms of one conversion round when C_{sense} is equal to 7pF as an example. Once V_c is charged to 1.8V, C_{sense} is connected to V_c ($=V_{sense}$ as shown in Fig. 6.4) to start powering the RC discharge circuit discussed in Section 6.3.2. V_c drops, with the current-starved voltage-controlled oscillator's frequency tracking its drop, until it reaches a predefined period ($= 2\times Delay_{ref}$ as discussed in Section 4.4.3, Chapter 4) to generate the *Ack* signal as shown in Fig. 6.12. The predefined period is caught by the T_{clk} as explained in Section 4.4.4, Chapter 4, and Section 6.3, Chapter 6. As shown in Fig. 6.12, the finial detected period slightly changes from 0.074μs to 0.087μs because of the circuit latency. However, once the parameter of the circuit is set, the detected period and V_{low} are fixed for each conversion round. Therefore, this error between the predefined value and detected value can be ignored once the design is completed.

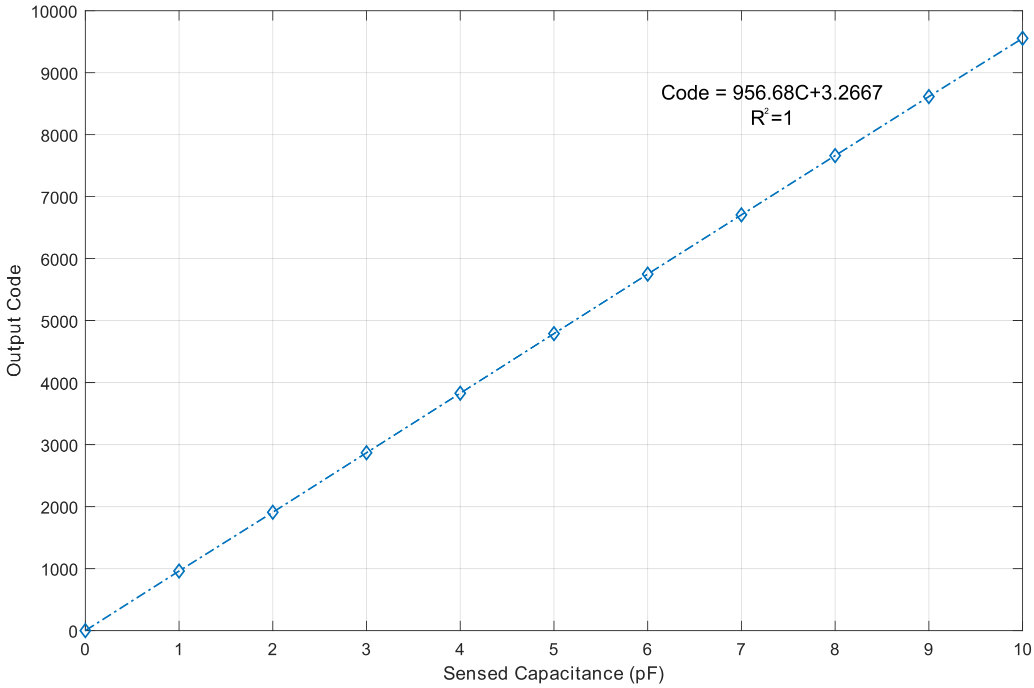


Fig. 6.13 Output code versus C_{sense}. This figure shows a good linearity between output code and C_{sense}, and the linearity error is shown in Fig. 6.15.

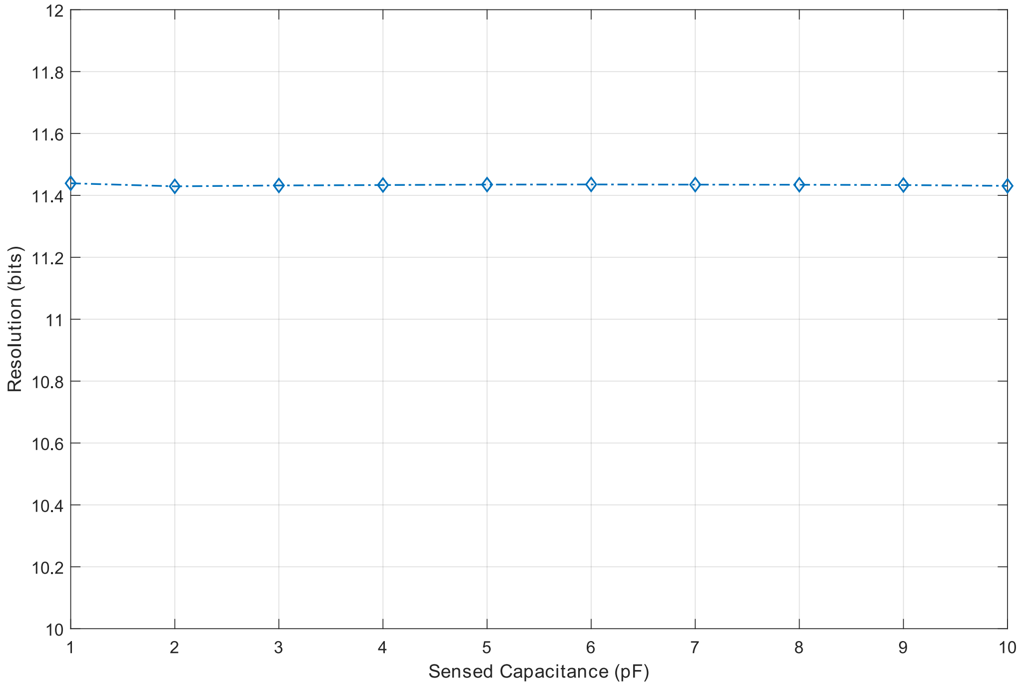


Fig. 6.14 Output resolution against C_{sense}. This figure shows quite a stable resolution around 11.4bits within a sensed capacitance range from 1pF to 10pF.

Fig. 6.13 shows the relationship between the output code and C_{sense}. It indicates that C_{sense} is linearly proportional to the output code with R-squared =1. Fig. 6.14 displays a plot of the simulated resolution against C_{sense}. The resolution is around 11.4bits within the range of C_{sense}. It has been found that this proposed time comparison-based capacitance-to-digital converter maintains a stable resolution, regardless of the capacitance of C_{sense}.

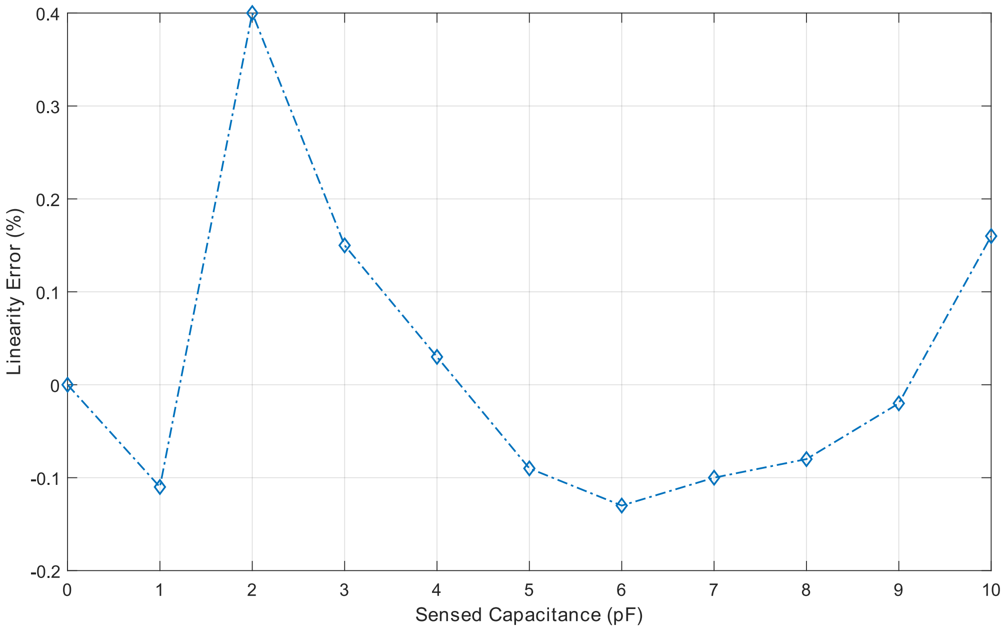


Fig. 6.15 Linearity error between the predicted code and the actual measured code. Within the tested range from 0 to 10pF, the proposed capacitance-to-digital converter had a small linearity error with a maximum value of 0.4%.

The error of linearity against C_{sense} between the predicted code (calculated code) and the actual measured code is plotted in Fig. 6.15. This linearity error is calculated by using Equation 6.1. The maximum error is 0.4% at a sensing value of 2pF, which can cause an about 8fF error, and 0.02% is generated as the minimum error, which has a maximum value of around 1.8fF at 9pF. These errors are negligible for engineering applications.

The overall simulated results are summarised in Table 6.2 and compared to the existing capacitance-to-digital converters. The compared figure-of-merit (F.o.M) normalises the consumed energy to the resolution [27] and was calculated using the following equation:

$$F.o.M = \frac{Conversion\ Energy}{2^{\text{Resolution}}} \tag{6.2}$$

Here, the resolution is determined as follows:

$$Resolution = (20 \times \log_{10} \frac{(Capacitance\ Range)/2\sqrt{2}}{Capacitance\ Resolution} - 1.76)/6.02 \tag{6.3}$$

where Capacitance Range is the designed range of input capacitance. Capacitance Resolution is the resolution measured in pF.

Table 6.2 Comparison with prior ART

	Type	Tech.	Power	Meas.time	Resolution	Input Capacitance	F.o.M
[43]	Capacitance-to-time	0.7μm	5mW	1s	20bits	5.8pF	4.7nJ/step
[27]	Capacitance-to-time	0.35μm	211μW	7.6ms	15bits	6.8pF	139pJ/step
[66]	Capacitance-to-time	0.18μm	18.4μW	17.5ms	N.A.	3.36pF	N.A.
[125]	Capacitance-to-time	0.35μm	15.84mW	N.A	8.8bits	0.8pF-1.2pF	1.78nJ/step
[106]	Capacitance-to-voltage	0.5μm	10.2μW	100ms	9bits	2.1pF-2.9pF	2nJ/step
[126]	Capacitance-to-voltage	0.25μm	20μW	40ms	12bits	1.5pF-2.5pF	195pJ/step
[127]	Capacitance-to-voltage	0.16μm	10.53μW	10ms	13bits	0.4pF-1.2pF	13pJ/step
This Work	Capacitance-to-time	0.35μm	371μW	0.076ms	11.44bits	0pF-10pF	10.17pJ/step

The comparison results in Table 6.2 pertain to sensing a 7pF capacitance. It can be seen that the proposed time comparison-based capacitance-to-digital converter has better F.o.M and high resolution compared to the prior ART. One of the advantages of this proposed capacitance-to-digital is the short measurement time, which is around 1315X lesser than [106], as shown in

Table 6.2. At the same technology node (350nm), this proposed capacitance-to-digital has 100X faster measurement with 13.7X less energy consumption per step compared to [27] when sensing a similar capacitance value.

6.5 Temperature and process variation

As mentioned earlier, PVT variations play an important role in CMOS systems. Experiments are carried out to test the temperature dependence and process dependence of the proposed capacitance-to-digital converter as well as the temperature dependence of the proposed current-starved voltage-controlled oscillator, respectively. In these experiments, the temperature range is limited between -40°C and 120°C, the C_{sense} is increased from 1pF to 4pF, V_{dd} is 1.8V and V_{low} is 1.05V.

6.5.1 Temperature variation on oscillator

Fig. 6.16 shows the frequency change rate depending on the temperature. In both cases, the current-starved voltage-controlled oscillator characteristics are compared with those of a five-stage voltage-controlled oscillator consisting of basic inverters. Here, the input voltage of the current-starved voltage-controlled is 1.8V to maintain the same voltage level applied in the two types of voltage-controlled oscillators.

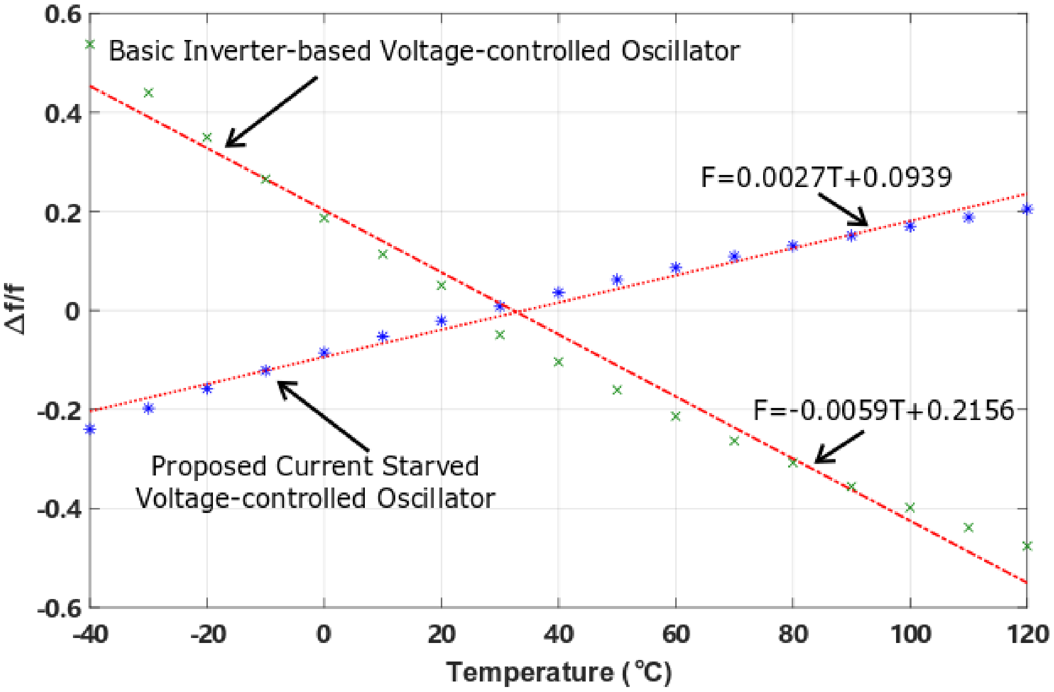


Fig. 6.16 Rate of change in terms of temperature variation on the proposed current-starved voltage-controlled oscillator. The rate of change in the basic inverter-based voltage-controlled oscillator is -0.0059 and that of the current-starved voltage-controlled oscillator is 0.0027.

Two observations can be drawn from Fig. 6.16. First, the temperature dependencies of these two types of oscillators have opposite trends. The frequency of our chosen five-stage current-starved voltage-controlled oscillator increases with temperature, while the frequency of the five-stage basic inverter-based voltage-controlled oscillator reduces when temperature increases. Second, the proposed current-starved voltage-controlled oscillator displays a smaller temperature variation on its frequency (0.0027), which is less than half of the basic inverter-based voltage-controlled oscillator's variation (0.0059).

6.5.2 Full converter temperature variation

The entire proposed capacitance-to-digital converter was also tested for its temperature variation. The temperature is changed within the range of -40°C to 120°C, and four C_{sense} values, from 1pF to 4pF, are chosen for the experiments.

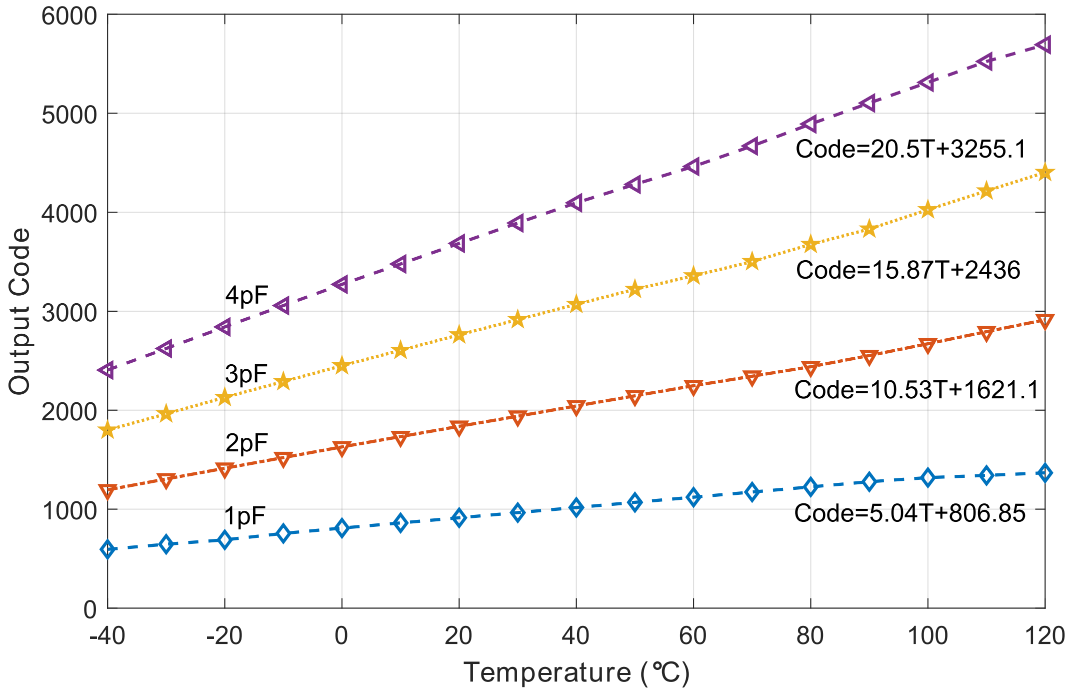


Fig. 6.17 Output code versus temperature. The larger the C_{sense}, the higher the change rate. The change rate is around 5 codes per °C of every 1pF difference.

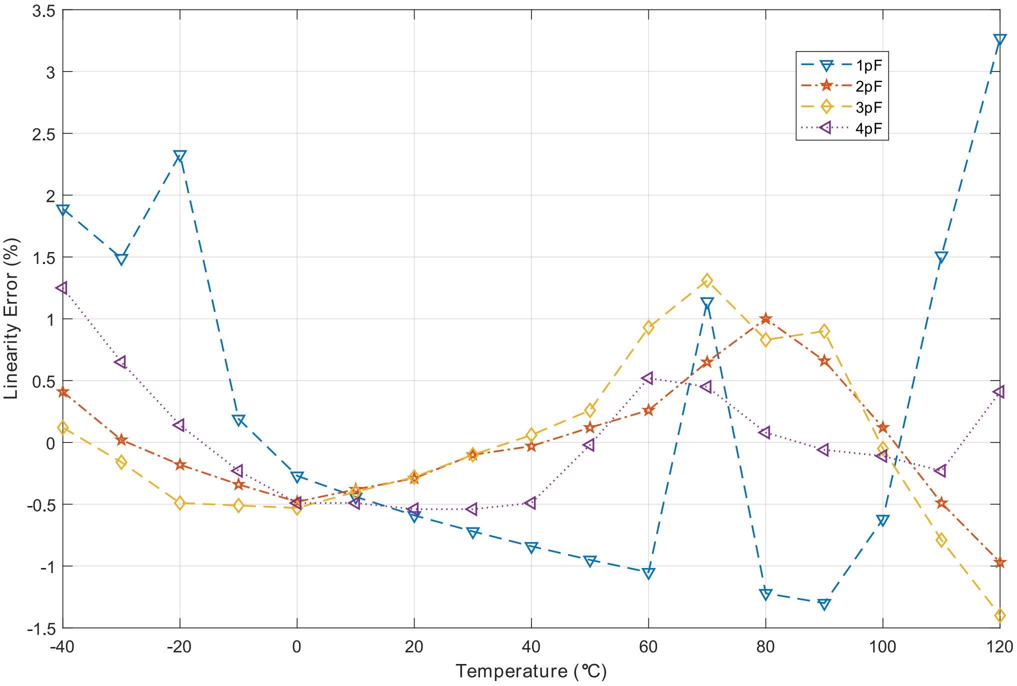


Fig. 6.18 Linearity error against temperature. This linearity error was calculated using the similar method given in Equation 6.1.

As can be seen from Fig. 6.17, the output code increases with an increase of temperature. The curve-fitting functions are given in the figure. As can be seen, the code to temperature relationship changes with the C_{sense} value. Therefore, for a given C_{sense}, the output code has a big difference with a change of temperature, which means that the entire capacitance-to-digital converter still has high temperature sensitivity. The maximum linearity error is around 3.3% at 120°C when C_{sense} is 1pF, and the minimum is about 0.02% at -20°C when C_{sense} is 2pF and at 90°C when C_{sense} is 4pF. In the temperature range of -12°C to 60°C, linearity is especially good for all the C_{sense} values with the maximum linearity error being 1%. Due to the inevitable temperature variations, this topic needs to be thoroughly revisited in future work. For instance, given the regular nature of the curves in Fig. 6.17, one promising method of compensating for temperature variations is to make use of a reference capacitor for online temperature calibration.

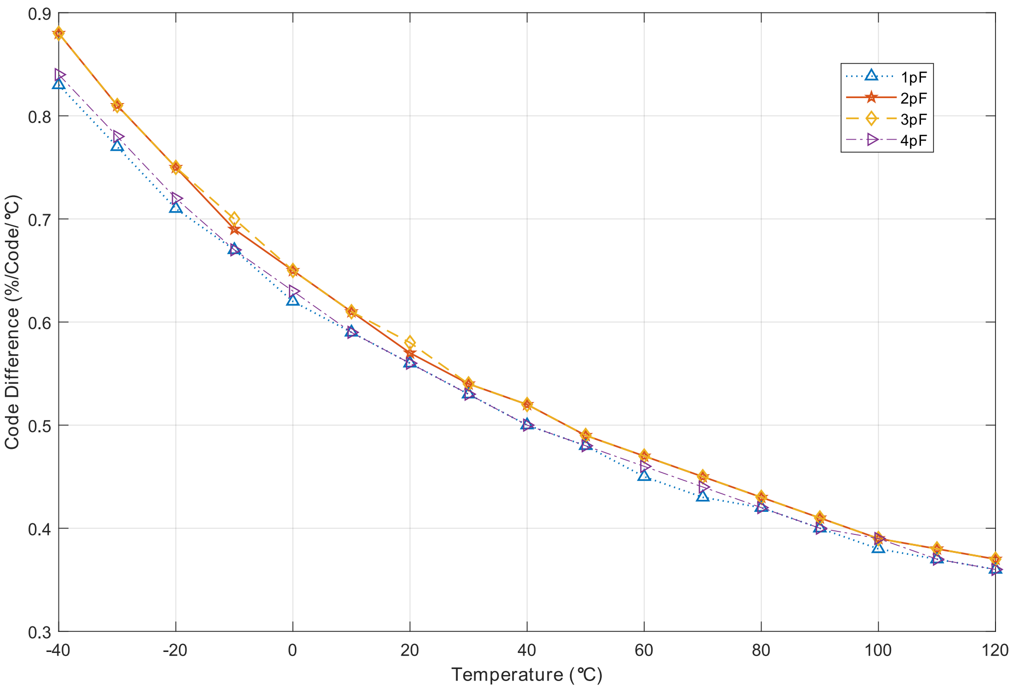


Fig. 6.19 Code difference (%/Code/°C) versus temperature.

Due to the temperature variation shown in Fig. 6.17, the percentage of code difference per code per °C may be determined by following (6.4):

$$C_oD_f = \frac{Code_{t+1^{\circ}C} - Code_t}{Code_t} \times 100\% \tag{6.4}$$

where C_oD_f is the code difference per code per °C; $Code_t$ is the code calculated for each C_{sense} by the equations in Fig. 6.17. Fig. 6.19 shows the code difference per code per °C. Comparing these four different C_{sense}s, the maximum code difference is 0.83% at -40°C when C_{sesne} = 3pF or 4pF. The minimum is 0.36% at 120°C when C_{sesne} = 1pF or 2pF. Based on the trend of those four capacitors, as the temperature increases, the output code error rate, calculated using the equations shown in Fig. 6.17, decreases. However, considering the full range of the temperature variation test, variations cause a small code difference per code per °C of less than 0.9%. The regularity of the curves in Fig. 6.17 and the well-behaved characteristics in Figs. 6.18 and Fig. 6.19 points to the potential of using this sensor for on-chip temperature monitoring. However, this requires in-depth investigations with real chip experiments and comparisons with current temperature sensing techniques. This is another potential topic for future work.

6.5.3 Full converter process variation

The variation of the output code against C_{sense} over various corners of analysis has been plotted in Fig. 6.20. Different output codes are generated at difference process corners. The analysis shows the maximum variation at the FF and SS corners.

A real chip tape-out is not done for this sensor. Given the results observed in Chapter 5 upon comparing the taped-out chip and corner analysis, it is reasonable to speculate that the corner analysis results at this technology node may be overly pessimistic. This is another future work requires. In any case, these corner-analysis results indicate that this type of sensor design, due to the internalisation of reference, is best used in systems where sensor calibration, offline or online, is possible.

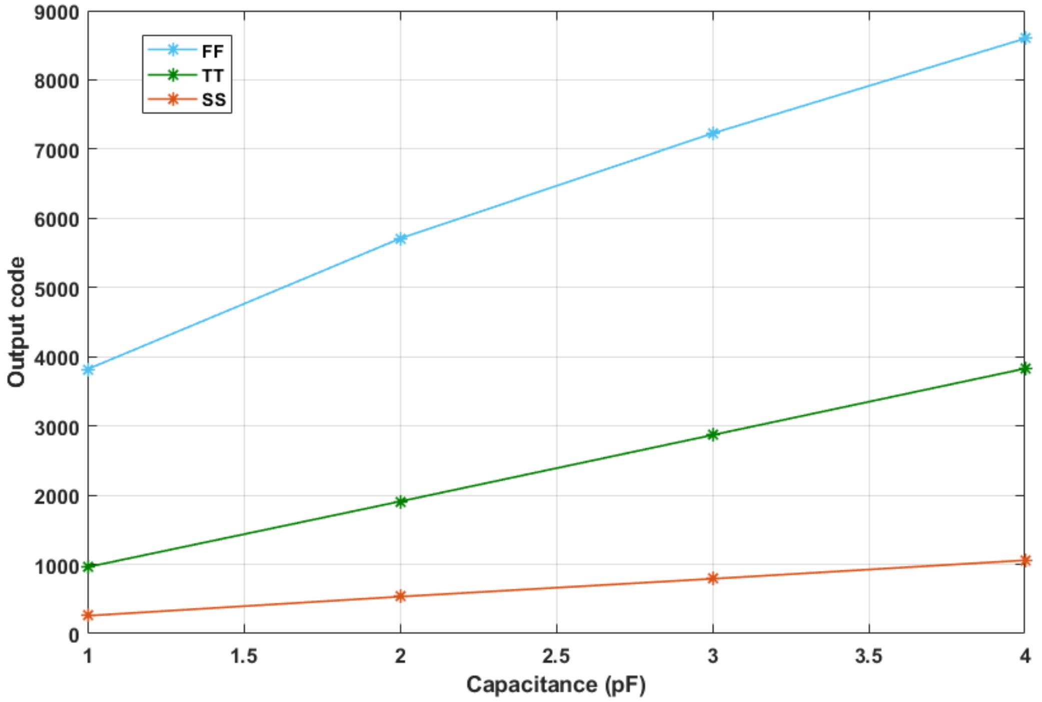


Fig. 6.20 Variation of the output code over process.

Fig. 6.20 shows good linearity level in the FF and SS corners, which can be used to calibrate the output code with a known reference capacitor to achieve a higher accuracy [28, 111]. This will be discussed in future works.

6.6 Summary

This chapter describes an energy-efficient time comparison-based capacitance-to-digital converter using the proposed voltage level-crossing (down) in Chapter 4 to achieve the V_{low} detection, and it is implemented and simulated in 350nm AMS technology node. The simulated results show that the proposed capacitance-to-digital converter has good linearity, which is an important factor for designing a capacitive sensor, and this proposed capacitance-to-digital converter can shorten the measurement time by 100 times as compared to [27] with the same technology (350nm technology). In addition, we tested the output code under temperature variations between -40°C and 120°C. The proposed current-starved voltage-controlled oscillator clearly reduces the temperature dependency, which is around two times smaller temperature variation compared to basic inverter-based voltage-controlled oscillator. However, the results of the temperature variation test for the entire proposed capacitance-to-digital converter resulted in significant sensitivity to temperature, which needs to be improved using other methods such as reference capacitor calibration [28]. The reference capacitor may be used for calibrations against both temperature and process variations [111]. Finally, the code difference in terms of temperature variation was discussed. The maximum code difference per code per °C is only 0.83%, which may not affect the output code within a small temperature range.

Chapter 7

Conclusions and future work

7.1 Conclusions

This work is based on the hypothesis that it is possible to design a sensing scheme without using external references. Such a scheme may be realised by exploiting the fact that it is possible to generate a voltage-dependent oscillating period or frequency by using a voltage-controlled oscillator. This scheme may be supported by the assumption that a constant time reference may be realised by using an RC circuit. Then, by combining such a constant time reference with the voltage-related oscillation period of a voltage-controlled oscillator, a voltage value may be determined. In Chapter 4, the methodology for detecting the constant delay time based on the proposed time comparison-based reference-free voltage level-crossing sensor was demonstrated. The design and circuit implementations of two proposed threshold voltage detectors based on this method are discussed in detail. The simulated results show the correct detection operation. These two up and down voltage threshold crossing detectors will form the foundation for the more sophisticated sensors subsequently described in Chapter 5 and 6.

Chapter 5 describes the detailed circuit implementation of the proposed reference-free voltage monitoring system targeting the detection of multiple predefined threshold voltages. It is fabricated using 350nm AMS technology and tested in a range of voltage from 0.85V to 1.2V with 25mV increments, and the temperature range is between 23°C and 100°C for the temperature variation test. The measurement results show that the response time, voltage range and power consumption are comparable to the previous voltage sensor based on reference-free techniques given in Table 5.7. The response time is around 15ms compared to 98ms generated by the US patent [22] using a similar theory to design the reference-free voltage sensing technique, and lower power consumption is about 0.4mW at 1.2V compared to 0.78mW in [21] which is a time-domain reference-free voltage sensor. However, the proposed voltage monitoring system needs to be tested with a wide voltage range, as a voltage range is only 0.35V so far. In addition, a chip fabrication error was discovered and recovery was carried out through a repair process using the focused ion beam technique.

Chapter 6 describes the design for a proposed capacitance-to-digital converter, which also makes use of the same time comparison method. For the operation of the capacitance-to-digital converter, the voltage always falls, which means that only the falling type of time comparison-based threshold voltage detector can be used. As one of the motivations for designing two different time comparison-based threshold voltage detectors for cases of rising and falling voltage is to reduce comparator complexity, this application requiring only one type strongly supports the design method. This proposed capacitance-to-digital converter has a good linearity with $R^2 = 1$ in the range of 0F to 10pF and high energy efficiency of 10.17pJ/step compared to 139pJ/step in [27] when sensing similar capacitance at the same technology node (350nm). It also reduces the measurement time down to 0.076ms. In addition, this capacitance-to-digital converter maintains a high precision/resolution of 11.44bits compared to the existing designs as shown in Table 6.2. This chapter also includes an exploration of the temperature dependency of the proposed capacitance-to-digital converter. Two possible types of voltage-controlled oscillator's design are investigated, with the current starved voltage-controlled oscillator showing less than half the temperature dependency of the basic inverter-based voltage-controlled oscillator.

7.2 Future work

The experiments conducted, including the simulations and chip measurements, generally support the conclusion that the method of converting voltage to time presented in Chapter 4 can be used in the design of more sophisticated sensors such as voltage monitors and capacitance-to-digital converters. However, these experiments also show up problems and challenges faced by these types of sensors.

- Firstly, it may be possible to reduce the silicon area of these types of sensors by employing better techniques than the typical sheet resistor for the RC circuit used in this work [117].
- Secondly, the process variation characteristics are not ideal, which may cause a few hundred mV of error, for instance, in the proposed time comparison-based voltage level-crossing sensor, the largest error is 230mV when detecting 950mV.
- Lastly, the results of the temperature variation experiments show a significant sensitivity to temperature in the experimented temperature range irrespective of whether the reference-free voltage monitoring system or energy-efficient capacitance-to-digital converter.

In response to the three issues above, corresponding solutions are given below for future work.

- The active resistor can replace the typical sheet resistor in the circuit due to the small area occupied in the entire chip. However, two potential issues need to be considered. 1). The active resistor is usually used to provide a resistance over a small resistance range [117], this small range has to be determined. 2). As the V_{dd} used in the proposed reference-free voltage monitoring system is unstable, the influence of this unstable energy on the resistance of the active resistor needs to be considered.

- To achieve PVT calibration in the reference-free voltage sensor, it is necessary to know the environmental conditions, such as the temperature and type of process, of the chip when it's functioning. Hence, the on-chip temperature/process sensor may be a good solution [124]. Once the environmental conditions are determined, the predefined voltage can be determined. However, this extra added circuit may increase the power consumption.
- For the PVT calibration of the capacitance-to-digital converter, the conventional method involves using a reference capacitor as presented in [28, 111]. A known capacitance $C_{PVT_{ref}}$ is applied to the system, and the ration of the $C_{PVT_{ref}}$ corresponding to the output code is obtained and stored. Therefore, in a normal digital conversion, the actual capacitance is calculated by multiplying the measured output code and the stored ratio.

In addition to the circuit improvements above, the experiments and research areas given below may also be explored.

- The proposed time comparison-based reference-free sensing technique is only experimentally verified as a separate subsystem. Therefore, another possible area of further development would be to incorporate these sensors in real systems. The first step for this would be to go beyond using signal generators to emulate energy harvesting waveforms and use real world energy source characteristics and harvesters instead.
- For the reference-free voltage monitoring system, the basic inverter-based voltage-controlled oscillator can be updated to reduce the temperature variations by using the current-starved voltage-controlled oscillator found in the proposed capacitance-to-digital converter. In the case of the capacitance-to-digital converter, there is scope for it to be investigated for reverse use, i.e. developing a temperature sensor by providing a known constant C_{sense}.

  For example, based on the results in Chapter 6, if the known constant C_{sense} is equal to 4pF based on Equation 7.1.

  $$Code = 20.5 \times T + 3255.1 \tag{7.1}$$

  Thus,

  $$T = \frac{Code - 3255.1}{20.5} \tag{7.2}$$

  where T is the measured temperature , and $Code$ is the measured output code. After cure fitting, the relationship between output code and temperature has a good linearity with R^2 = 0.9997. Therefore, Equation 7.2 can be used to measure the temperature, and then the proposed capacitance-to-digital converter can be used in reverse as an on-chip temperature sensor.

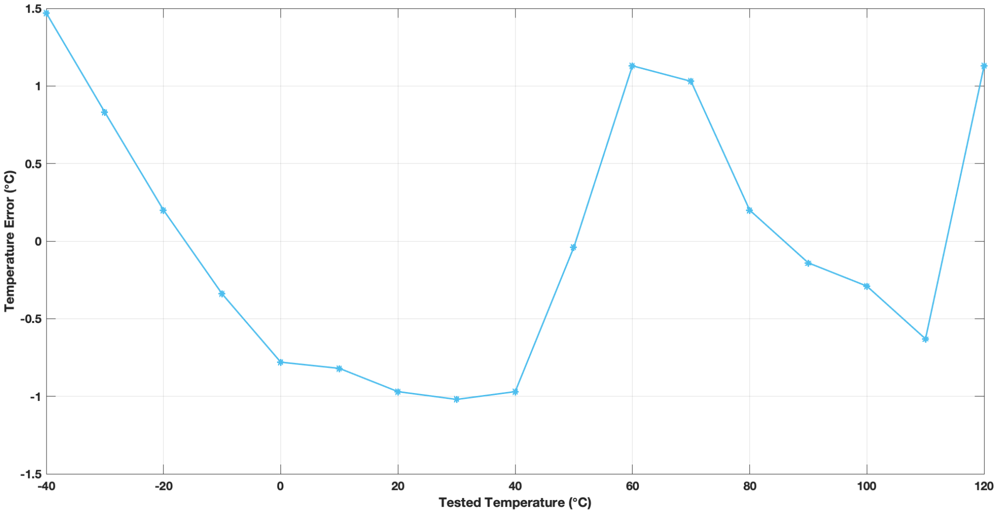


Fig. 7.1 Temperature error against tested temperature. The temperature errors is equal to the tested temperature minus the measured temperature.

Fig. 7.1 shows the difference between the tested temperature and the measured temperature. The biggest error is around 1.5 °C when the tested temperature is -40 °C, and the smallest error is -0.04 °C when the tested temperature is 50 °C. So far, the measured data can prove that the temperature sensor is a potential research direction. However, further verification of its performance is required. For example, the PVT variations, post layout simulation and actual experiments using the fabricated chip need to be considered. Table 7.1 provides a detailed comparison between the tested temperature and measured temperature, when C_{sense} is 4pF.

Table 7.1 Comparison of the tested and measured temperatures.

Tested temperature (°C)	Measured temperature (°C)
-40	-41.47
-30	-30.83
-20	-20.20
-10	-9.66
0	0.78
10	10.82
20	20.97
30	31.02
40	40.97
50	50.04
60	58.87
70	68.97
80	79.80
90	90.14
100	100.29
110	110.63
120	118.87

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