# Investigation of Switching Schemes for Three-phase Four-Leg Voltage Source Inverters

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To my uncle, Diansheng Cao

and my cousin, Peng Cao

# Abstract

Three-phase four-leg voltage source inverters (VSIs) are widely used in distributed power generation applications, three-phase UPS systems and fault-mode operation of a balanced three-phase system where the balanced three-phase voltage output is required when the loads are unbalanced. A three-dimensional space vector modulation (3-D SVM) switching scheme, which is proved to be compatible with modern DSP implementation for a four-leg VSI, has the advantage of higher DC link utilization, less harmonic contents and less switching losses compared with sinusoidal PWM. Therefore it is the first choice of switching schemes for a four-leg inverter.

Electromagnetic interference (EMI) which is associated with common-mode switching for a high voltage level power system can degrade the equipment performance and cause communication problems. The conventional 3-D SVM switching scheme exhibits high common-mode voltage (CMV) characteristics which may result in problems in high power applications.

The 3-D SVM has the drawback of being complex which could become a software burden in computationally intense real-time control applications. Attempts to reduce the complexity of the 3-D SVM have been made by many researchers and new switching schemes such as carrier-based PWM proved to have the same performance.

This thesis presents a switching scheme called near-state 3-D SVM that can reduce the CMV voltage level of a four-leg inverter by avoiding the use of the two zero switching states of the inverter. A laboratory test bench has been built to validate the proposed switching scheme. An in-depth analysis has been carried out for a four-leg inverter in terms of total harmonic distortion (THD) factor, current harmonic distortion factor, conduction losses and switching losses. The proposed switching scheme is analyzed and compared with the conventional 3-D SVM using the analysis method.

Additionally, a simplified switching scheme which is still based on space vector theory is proposed. This simplified switching scheme remains compatible with vector control. Experimental results show that the simplified switching scheme has the same performance as 3-D SVM, with reduced program execution time.

An output voltage control loop with current feed-forward term in *d-q-0* coordinate, which is designed in the discrete-time domain, proves to be most compatible with a DSP-based control system. Experimental results demonstrate the performance of the control loop in both steady state and transient operation.

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# Acronyms and symbols

## List of Symbols

| | |
|---|---|
| $C$ | Capacitance value |
| $d_x$ | Duration of the switching vector |
| $f_c$ | Cut off frequency of the digital RC filter |
| $f_{res}$ | Resonant frequency (in Hz) |
| $G$ | Matrix needed to calculate the vector duty ratios |
| $H_c$ | Computation delay |
| $I_L$ | Load current |
| $I_n$ | Neutral current which goes through the fourth leg |
| $j$ | Rotating operator (90°) |
| $K_i$ | Integral gain |
| $K_p$ | Proportional gain |
| $k_V$ | Voltage harmonic distortion factor |
| $L$ | Inductance value |
| $M$ | Fundamental per-phase modulation index value |
| $M_i$ | Modulation index value |
| $N$ | Number of calculation in 60° electrical angle |
| $P$ | Average switching losses during one power cycle |
| $P_{sw}$ | Power dissipated during one switching event |
| $q$ | Number of sampling time |
| $T$ | Park transformation matrix |
| $T_1$ | Period of fundamental frequency |
| $T_{PWM}$ | One PWM sampling time |
| $T_s$ | One switching period |
| $t_E$ | Effective turn-on time |
| $t_{1/2/3}$ | Duration time relating to $\vec{V}_{1/2/3}$ |
| $u_1$ | Fundamental phase voltage |

| | |
|---|---|
| $u_{1\text{six-step}}$ | Fundamental voltage of the six-step operation |
| $V_{\text{DC}}$ | DC link voltage |
| $V_{\text{h}}$ | Harmonic voltage |
| $V_1$ | Fundamental voltage |
| $\hat{V}_{ll}$ | Peak-to-peak value of the line-to-line voltage |
| $V_{\text{max/min}}$ | Instantaneous maximum/minimum voltage |
| $\vec{V}_{\text{ref}}$ | Reference voltage space vector |
| $\vec{V}_{\text{x}}$ | Voltage space vector |
| $V_{\text{ao/bo/co/fo}}$ | Phase-to-midpoint voltage |
| $V_{\text{an/bn/cn}}$ | Phase voltage (Phase-to-neutral voltage) |
| $V_{\text{eff}}$ | RMS voltage value |
| $V_{\text{no}}$ | Common-mode voltage |
| $X_{\text{A,B,C}}$ | Phase voltage or current |
| $X_{\text{p,n,0}}$ | Positive, negative, zero-sequence component |
| $Y$ | Star connection |
| $\alpha$ | Rotating operator (120°) |
| $\Delta$ | Delta connection |
| $\delta$ | Modulation angle |
| $\zeta$ | Zero-state partitioning function |
| $\theta$ | Rotating angle of the *d-q-o* coordinate |
| $\theta_{\text{a}}$ | Angle difference between the *D-Q-O* and *d-q-o* |
| $\theta_{\text{e}}$ | Rotating angle of the *D-Q-O* coordinate |
| $\rho$ | Gain value of the digital RC filter |
| $\psi$ | Modulator angle |
| $\varphi$ | Power factor angle |
| $\omega$ | Electrical velocity |
| $\omega_{\text{c}}$ | Cut-off frequency (in rad/s) |

## List of acronyms

| | |
|---|---|
| 2-D | Two dimensional |
| 3-D | Three dimensional |
| AC | Alternating current |
| ADC | Analogue to digital converter |
| C2D | Continuous to digital |
| CBPWM | Carrier-based PWM |
| CMV | Common-mode voltage |
| DAC | Digital to analogue converter |
| DC | Direct current |
| DSP | Digital signal processor |
| EMF | Electromagnetic force |
| EMI | Electromagnetic interference |
| FIR | Finite impulse response |
| FFT | Fast Fourier transformation |
| GDPWM | General discontinuous PWM |
| GPIO | General-purpose input/output |
| IGBT | Insulated gate bipolar transistor |
| ISR | Interrupt service routine |
| *L-C* | Inductor-capacitor |
| MLDPWM | Minimum loss DPWM |
| NSPWM | Near state pulse width modulation |
| PWM | Pulse width modulation |
| PCC | Point of common coupling |
| PF | Power factor |
| PI | Proportional integral |
| PLL | Phase locked loop |
| PR | Proportional resonant |
| PSU | Power supply unit |
| *RC* | Resister-capacitor |

| | |
|---|---|
| RSL | Relative switching loss |
| SHEPWM | Selective harmonic elimination PWM |
| SRAM | Static random-access memory |
| SVM | Space vector modulation |
| THD | Total harmonic distortion |
| UPS | Uninterruptible power supply |
| VSD | Variable speed drive |
| VSI | Voltage source inverter |
| ZOH | Zero-order hold |

# Chapter 1
# Introduction

Power generated from renewable resources is either connected to the grid or to the local loads through inverters. A three-phase four-leg voltage source inverter can guarantee a balanced three-phase output even when the load is unbalanced and nonlinear. A three-phase four-leg VSI therefore is mostly seen in applications such as standalone power generation system or a three-phase UPS system. The successful operation of the three-phase four-leg VSI requires the knowledge of power electronics, converter operation, switching scheme and most important of all control loop design. Both hardware design and software design have to cooperate well to meet the specifications of a power system.

The focus of this thesis is on the switching scheme that will address EMI issues that are related to the common-mode voltage of the three-phase four-leg VSI. The simplification of the available switching scheme and proposed common-mode voltage reduction switching scheme are also considered. A control loop is designed based on a real-time DSP system so that the whole system can meet the design specifications.

## 1.1 Motivations and Objectives

The concept of the three-phase four-leg VSI was introduced over 20 years ago. The past 20 years has witnessed great development in power electronics and their active role in energy generation, especially in the field of renewable energy. The higher ratings and better cooling of the power electronics mean that they can be used in medium or high voltage level application with improved efficiency. Together with the improvement in power electronics and its drive circuit, the digital signal processor works at faster operating speed, larger memory, faster A/D channels and more efficient communications between the subsystems. These altogether have made a three-phase four-leg VSI work at a high efficiency.

Severe EMI noise related to the common-mode voltage causes trouble for a high voltage level power system. According to [1], EMI is defined as ‘an unwanted electrical signal that produces undesirable effects in a control system. Sensors are affected by the EMI noise, nuisance trip of the driver circuit occurs if severe EMI noise persists, causing the failure of the communication of the drive system. The impact of the four-leg converter switching schemes on grounding and common-mode noise issues has rarely been investigated before and as the voltage level gets higher and switching frequency becomes higher, the EMI issue becomes severe.

The addition of an extra leg makes the switching schemes that are applied on the four-leg converter more complex compared with a three-leg inverter. Among the available switching schemes, a three-dimensional space vector modulation (3-D SVM) is considered the best switching scheme. However, the algorithm that is needed to compute the 3-D SVM is complicated. The disadvantages of this complexity include lengthy program code, high skill level needed by development engineers and longer program execution time, therefore the algorithm needs to be simplified.

Performance evaluation of a three-phase VSI from previous research work consists of analysis based on total harmonic diction (THD), crest factor, conduction switching loss. Analysis based on different switching schemes has been carried out and comparison has been made for a variable speed drive system. But there is no in-depth analysis has been made based on a four-leg inverter. Therefore there is a demand for a theoretical, vector-based analysis on a four-leg VSI.

The mathematical model of the four-leg system from a control point of view is a high order, coupled system. Methods to decouple the system and reduce the order of the system have been introduced in previous works. A control loop design based on discrete-time domain is appropriate with modern DSP system since it can take into account the delay caused by either PWM output or computational delay. Therefore this thesis presents a controller loop which is based on discrete-time domain.

More specifically, the objectives of the research are:

- To investigate the impact of three-dimensional SVM schemes on grounding and EMI issues related to the common-mode noise
- To design a common-mode voltage reduced space vector modulation method for a three-phase four-leg VSI

- To simplify the three-dimensional SVM algorithm
- To produce an in-depth performance analysis for a four-leg VSI
- To implement a control design in discrete-time domain
- To validate the results obtained using an accurate simulation model and a real-time laboratory test bench

## 1.2 Methodology

The introduction of the theory in this thesis makes use of a mathematical model in a three-dimensional space. The study of the mathematical model where matrix calculations are required was carried out with the help of Matlab. A simulation was modelled using the combination of Matlab/Simulink and Matlab/Simpower with the core controller programme written in Matlab/S-function block using the C programming language.

Later, the controller program code was slightly modified for use in the DSP based control unit for practical implementation. A Labview based user control panel is used to serve as a communication tool between the computer and the controller unit. The experimental data, e.g. sampled phase voltage and phase current values are captured and stored in the RAM memory of the DSP and can be downloaded to the host computer through an RS-232 channel. The panel is also used to allow the user to control the operation of the converter control system. Screenshots of the oscilloscope are also used to provide useful experimental results.

The in-depth evaluation requires math-intensive calculation and some of the most complicated calculations are done using the mathematical software Wolfram Mathematica[2, 3].

Control loop design of the system is based on discrete-time domain, and with the help of Matlab and Matlab/Sisotool[4], the delay caused by sampling and hold, computational delay can be simulated and used for controller design.

## 1.3 Contribution to knowledge

This section outlines areas of work that have not been published before or not covered in details in the current literature.

- Work done in this thesis has resulted in one conference paper publication:

***A zero-sequence component injected PWM method with reduced switching losses and suppressed common-mode voltage for a three-phase four-leg voltage source inverter***

*This paper appears in: IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*
*Date of Publication: 25-28 Oct. 2012*
*Author(s): Zhang, M.*
*School of Electrical & Electronic Engineering, Newcastle University, Newcastle upon Tyne, UK*
*Atkinson, D.J.; Armstrong, M*
*Page(s): 5068-5073*
*Product Type: Conference*

Also, a journal paper has been submitted to *IEEE Transactions on Power Electronics* and it was successfully accepted and the reviewers recommended publication with minor corrections. The title of this journal paper is

***A Near-State Three-Dimensional Space Vector Modulation for a Three-Phase Four-Leg Voltage Source Inverter***

This paper will appear in *IEEE transactions on Power Electronics*
*Author(s): Zhang, M.*
*School of Electrical & Electronic Engineering, Newcastle University, Newcastle upon Tyne, UK*
*Atkinson, D.J.; Ji, B; Armstrong, M; Ma, Mingyao*

- Development and application of a novel common-mode voltage suppression switching scheme for a three-phase four-leg voltage source inverter, by simulated and experimental verification.
- Performance analysis using graphic tools on switching schemes for a three-phase four-leg voltage source inverter.
- Simplification of available switching schemes for a three-phase four-leg voltage source inverter, by simulated and experimental verification.
- Simulated and experimental verification of a fast-dynamic control scheme for a three-phase four-leg voltage source inverter under unbalanced load conditions.

## 1.4 Thesis Overview

A brief description of each chapter is provided below:

Chapter 1 provides a general introduction covering recent developments in power electronics and digital signal processor technology and how they play an important role in terms of control of a four-leg VSI. The motivations and objectives of the research are introduced, methodology of the project is presented, and the thesis overview is also covered.

Chapter 2 is a literature review covering the converter topologies, switching schemes, control loop design and performance analysis based on the three-phase four-leg voltage source inverters.

Chapter 3 investigates the EMI issue that is related to the common-mode noise for a high voltage level three-phase four-leg VSI and introduces a near state 3-D SVM switching scheme that can reduce the common-mode voltage level. Both simulation and experimental results validate the proposed switching scheme.

Chapter 4 presents an in-depth performance analysis for different switching schemes on a four-leg VSI using the space vector method. Voltage harmonic factor, inductor current harmonic factor, conduction losses and switching losses of different switching schemes are compared.

Chapter 5 analyses the mathematical model of a four-leg inverter in an $\alpha$-$\beta$-$\gamma$ coordinate and decouples the system into a $\alpha$-$\beta$ plane plus $\gamma$ axis. By doing so a simplified switching scheme named zero-sequence injected PWM is then introduced. Simulation and experimental results show that the proposed switching scheme achieves the same performance as the 3-D SVM with a simplified algorithm.

Chapter 6 describes a design of the system control loop based on the model in discrete-time domain. Delays caused by a discrete control system have been taken into account. A voltage controller with current feed-forward guarantees the performance of the system under steady state and transient state conditions.

# Chapter 2
# Literature Review

The past decade has witnessed significant development in power conversion technology thanks to the continuous penetration of power electronics into power generation, transmission and consumption. With the performance improvement and cost reduction of the power electronics devices, new topologies of the power converters have become available, reducing the size, saving the energy, and improving the efficiency of the system.

In this chapter, the definitions of distributed power generation system and the three-phase uninterruptible power supply system are described. Both systems face the problem of supplying power to unbalanced loads. The effect of unbalanced loads is then studied and the converter topologies to deal with unbalanced loads are studied and compared.

A three-phase four-leg voltage source inverter is selected for this project because of its reduced size and greater controllability. The switching schemes that can be applied on a four-leg inverter are introduced and compared. Performance analysis on a three-phase three-leg voltage source inverter is then studied. Different control schemes for the four-leg inverters are reviewed at the end of this chapter.

## 2.1 Distributed power generation system

These days, the development of power generation systems using renewable energy such as wind, hydro power, and solar power has increased rapidly due to the rising demand for cleaner energy utilization[5, 6]. A distributed power generation system, also called small scale electricity generation system is often based on renewable energy resources. These systems are capable of supplying the power either to the grid or to the local load system[7] as it is shown in Figure 2.1. The definition, benefits and issues with the distributed power generation system are presented in details in [8]. Theoretical benefits

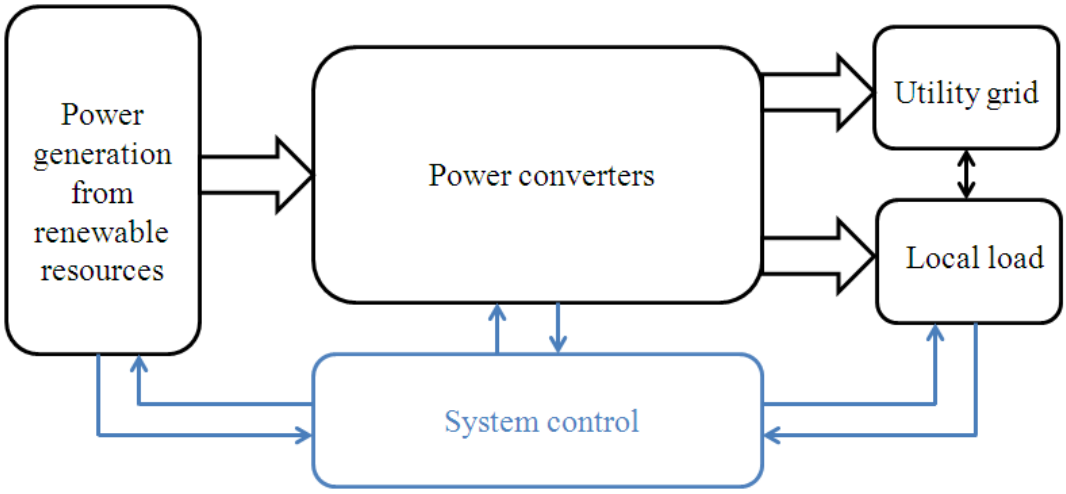



Figure 2.1 General structure for distributed power generation system

of the distributed power generation system include reliability and security benefits, economic benefits, emission benefits and power quality benefits.

There are different issues related to grid connection and load connection. Among all the issues, power quality should be considered mainly since it is strongly related to reliability of the power system. Abnormal switching operations in the power network and disturbances in the load network can cause a reduction in power quality of the system. Effects such as flicker (fast voltage variations), harmonic distortion and phase imbalance have a significant influence on the normal operation of the distributed power generation system [8] and therefore are main concerns in the power system design.

Another issue with a small scale power generation system is that most of the low voltage loads such as computers, lighting systems are single-phase. The layout of the three-phase power system has to be distributed to feed these single-phase loads, for instance, one phase per floor of a building. Generally a three-phase four wire power converter is utilized to distribute power, and transformers are used to deal with the zero and negative-sequence current caused by the unbalanced loads [9].

Other circumstances, such as islanding, in which a local generator keeps a disconnected power grid energized may lead to danger for the maintenance personnel. Therefore loss of mains detection is one of the topics in which research has been carried out intensively in recent years [10].

## 2.2 Uninterruptible power supply system

There has been an increasing demand for critical loads such as computer server systems, telecommunication systems, security systems and hospital equipment, etc [11]. These critical loads require clean and reliable AC power and the cost of power interruption would be unbearable. An uninterruptible power supply (UPS) system can provide secure and high quality power to such critical loads. Also, for distributed power generation systems, a distributed storage system combined with a UPS system can be used to add reliability and expandability to the system[12].

There are generally three types of UPS, namely offline UPS, line-interactive UPS and online UPS [13]. The steady-state performance characteristics of the UPS include THD, crest factor of the output while the dynamic response of the UPS is equally important that it becomes a measurement for the overall acceptance of a UPS.

Impact of sudden load change for a UPS should be taken into consideration since it is related to the dynamic response of the UPS[14]. Over-voltage (surge) or under-voltage (sag) would be observed during the load change, and the time taken for the output voltage to recover from either surge or sag determines the dynamic response of a UPS system [14, 15]. The sudden change of load can still be classified as unbalanced load condition since during the load change an unbalanced load current is always created.

## 2.3 Effects of unbalanced load condition

Most of three-phase inverters are designed to supply balanced three-phase voltage to the load side such as three-phase machine application in which cases the loads are always assumed to be balanced three-phase loads. However, unbalanced load conditions are common for UPS systems and distributed power generation applications where power is delivered to local loads. There is also an unbalance issue in fault-tolerant machine drives [16]. Unbalanced load condition creates unbalanced current circulating in the power system, causing overheat of the neutral wire for a four-wire system[17], and harmonic distortion on the output voltage[18]. Under circumstances in which the load is heavily unbalanced, the source could become unbalanced due to the impact of the unbalanced current [19]. In the following sections, the unbalanced load condition is reviewed and analyzed based on the symmetrical components theory. Later in this chapter, the impact of the unbalanced load current in *d-q-o* coordinate will also be reviewed.

### 2.3.1 Unbalanced load analysis based on symmetrical components

The symmetrical component theory was first introduced by C. L. Fortescue in 1918 and was soon widely used in power system fault analysis [20]. In this dissertation, this theory is used as an analysis tool for the unbalanced voltage and current, and is useful for the controller design.

According to the theory, a asymmetrical three-phase signal (either voltage or current) can be represented as a sum of positive, negative and zero-sequence components [21]. The transformation is expressed as

$$\begin{bmatrix} X_p \\ X_n \\ X_0 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} \tag{2.1}$$

And the inverse transformation is given by

$$\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{bmatrix}\begin{bmatrix} X_p \\ X_n \\ X_0 \end{bmatrix} \tag{2.2}$$

where $X$ could be $V$ (voltage) or $I$ (current) and $\alpha$ is an operator and has the value of $e^{j2\pi/3}$ and $\alpha^2=e^{j4\pi/3}$.

Since the neutral current in a three-phase four-wire system is defined as in Eq. (2.3), it is clear that the neutral current equals three times of the zero-sequence current.

$$I_n = -(I_A + I_B + I_C) \tag{2.3}$$

An arbitrary asymmetrical three-phase signal can then be represented as Eq. (2.4) and Figure 2.2 shows the decomposition of an unbalanced three-phase signal.

$$\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} = \begin{bmatrix} X_{A\_p} \\ X_{B\_p} \\ X_{C\_p} \end{bmatrix} + \begin{bmatrix} X_{A\_n} \\ X_{B\_n} \\ X_{C\_n} \end{bmatrix} + \begin{bmatrix} X_{A\_0} \\ X_{B\_0} \\ X_{C\_0} \end{bmatrix} \tag{2.4}$$

where

$$\begin{bmatrix} X_{A\_p} \\ X_{B\_p} \\ X_{C\_p} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} \tag{2.5}$$

$$\begin{bmatrix} X_{A\_n} \\ X_{B\_n} \\ X_{C\_n} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} \tag{2.6}$$

$$\begin{bmatrix} X_{A\_0} \\ X_{B\_0} \\ X_{C\_0} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} \tag{2.7}$$

According to [18], the IEC gives a definition of the degrees of the unbalance, the unbalance factor is described in terms of the negative-sequence unbalance factor and zero-sequence unbalance factor expressed in the following equations

$$Unbal\_N\% = \frac{\mathrm{X_n}}{\mathrm{X_p}} \times 100 \tag{2.8}$$

$$Unbal\_0\% = \frac{\mathrm{X_0}}{\mathrm{X_p}} \times 100 \tag{2.9}$$

where $X_{p,n,0}$ are positive, negative, zero-sequence component.

According to the definition given in Eq. (2.8) and Eq. (2.9), Table 2-1 shows some of the load conditions and their unbalance factors.

### 2.3.2 Effects of an unbalanced load

A short overview of the most common problems caused by an unbalanced load is given in this section. There are four types of connection between the load side and the source side of a power system.

In a Y/Y connection shown in Figure 2.3, a negative-sequence current will circulate at twice the fundamental frequency between the load side and source side through the three phase conductors. The zero-sequence current will travel at fundamental frequency between the neutral points of the source and load through the neutral conductor. Since the neutral conductor is generally designed for balanced conditions, the neutral current will cause excessive heat in the conductor, it is even worse when the load is nonlinear [17, 22].

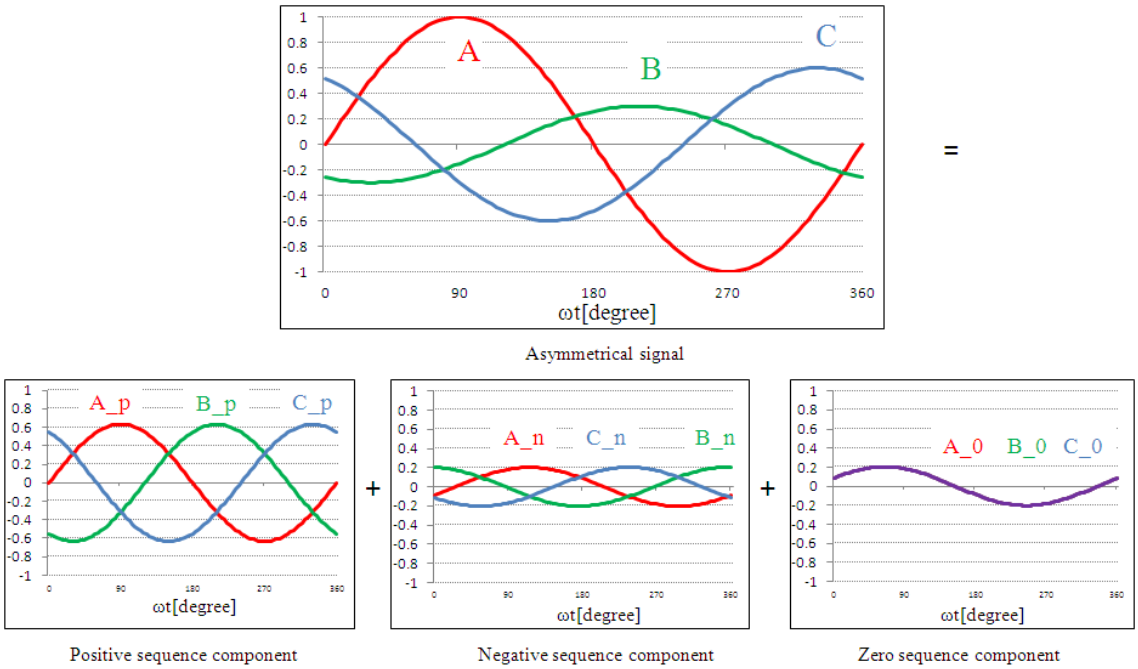



Figure 2.2 Symmetrical decomposition of an unbalanced three-phase signal

**Table 2-1Unbalanced load conditions and unbalance factors**

| Load Conditions | *Unbal_N*% | *Unbal_0*% |
|---|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $I_{LC}=0$, $PF_A=PF_B=PF_C=1$; | 50% | 50% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$ between 0.8 leading and 0.8 lagging | <=22.1% | <=22.1% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=1$, $PF_B=PF_C$ ranging between 0.8 leading and 0.8 lagging | <=22.1% | <=22.1% |

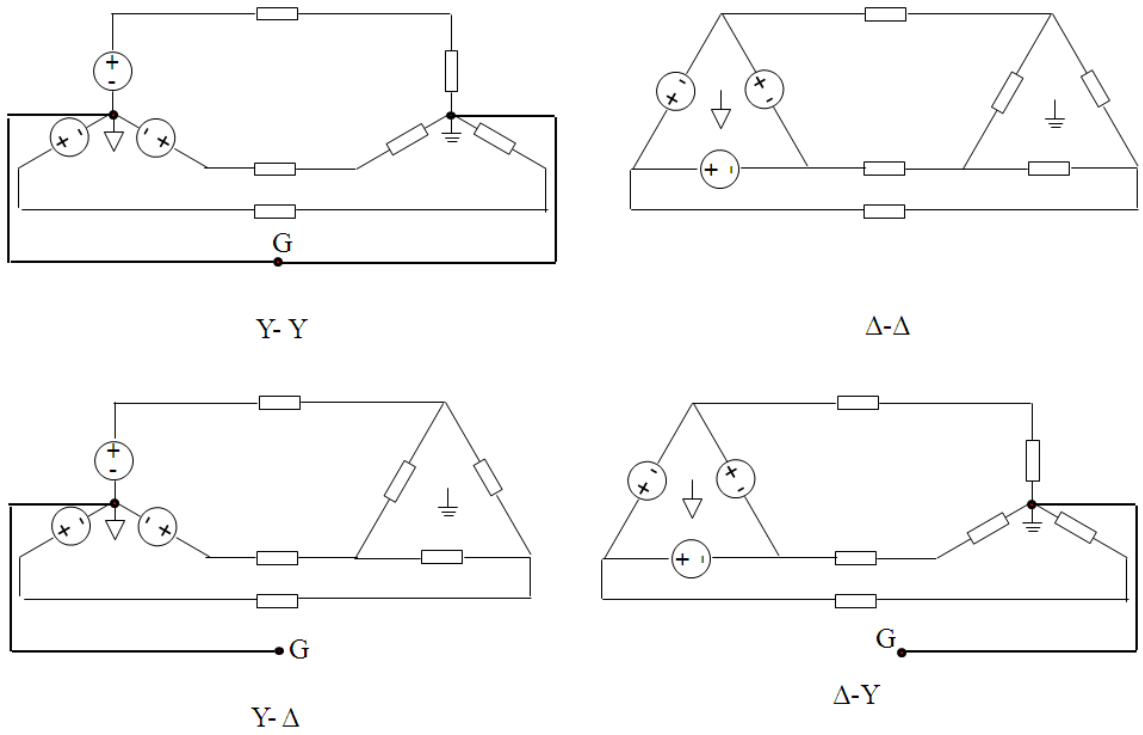



Figure 2.3 Possible connections between the source and load side of a power system

In a Δ/Δ connection, since there is no neutral point on both the source side and the load side (or there is floating neutral point of both sides), the effect of the zero-sequence current is eliminated because the zero-sequence current normally circulates in the Δ configuration of the load side. The negative-sequence current will circulate at twice of the fundamental frequency of both sides, causing voltage potential shifting all the time of both sides. The potential difference of both sides, through parasitic capacitance, could lead to common-mode current, therefore causing EMI issues.

For Y/ Δ and Δ/Y connection, apart from the fact that negative-sequence current will behave the same as it does in Δ/ Δ connection, there is zero-sequence current circulating in the Δ configuration side.

In induction machines that are connected to the load side, the unbalanced current introduces elliptical rotating magnetic field, thus influencing the torque-speed characteristics of the machine. Besides, the machine bearing could suffer damage because of the rippling torque caused by negative-sequence current. Also, the negative-sequence current creates inverse rotating magnetic field for the machine, causing excessive heat in the stator windings, therefore accelerate the process of thermal aging. For synchronous machines, the main issue with the unbalanced current is the excessive heat in the stator winding.

The capacity of transformers (if present), cables and transmission lines have to be chosen to have a higher rating if considering the unbalanced load condition [23]. This increases the cost size and the cost of the system.

## 2.4 Converter topologies for unbalanced loads

A neutral wire is required to cater for potentially unbalanced loads. Under balanced load conditions, the neutral current is zero. When the load is unbalanced, neutral current flows. There are many converter topologies available for three-phase four-wire systems. In the following sections, the main types and variations of power converters are described.

### 2.4.1 A three-phase four-wire VSI with split DC link capacitors

A very simple approach to connect the neutral conductor is to connect the star point of the loads to the mid-point of the DC link capacitors as it is shown in Figure 2.4. This connection arrangement is easy to install, however, it suffers two major drawbacks.

The first drawback is the low utilization of the DC link voltage [24, 25]. By connecting the start point and mid-point of the DC link capacitors together, the potential difference between the two points is then forced to be zero. Because the variation of the voltage between the mid-point of DC link and the ground is slow and small [26]. This means the star point of the load is not free to float regardless of the switching schemes that are used. In this case, the maximum phase voltage is $0.5V_{DC}$, which shows that DC link utilization is limited to be $\sqrt{3}/2$, this is 15% less than it would be achieved with a three-phase three-leg VSI using SVM or 60° PWM switching scheme [27].

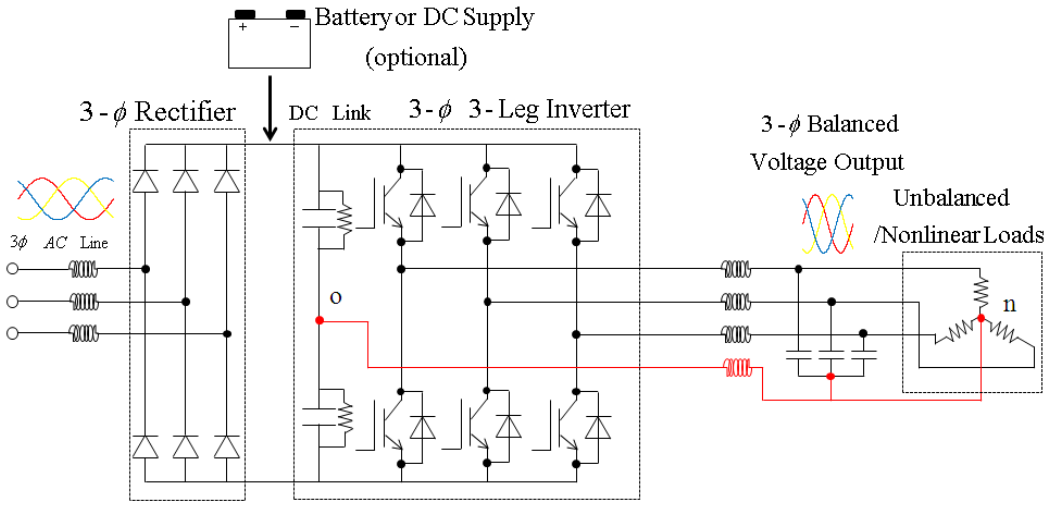



Figure 2.4 A three-phase four-wire VSI with split DC link capacitors

Another disadvantage of this topology is that two large capacitors are needed to deal with the current ripples caused by both negative-sequence current and zero-sequence current[24]. As it was explained in the previous section, negative-sequence current results in a $2\omega$ ripple while the zero-sequence current causes a ripple with the frequency of $\omega$. The choice of the DC link capacitors is a complex task [28] and the size of the capacitor depends on the ripple level[29]. As a result, this topology will increase the cost of the system dramatically, especially for high power applications.

### 2.4.2 A three-phase four-wire VSI with a Δ/Y transformer

An alternative approach to connect the neutral point is to connect the start point of the loads to the secondary side of a Δ/Y transformer. As it can be seen in Figure 2.5, due to the strong transformer coupling effect and by keeping the inductors on the primary side of the transformer, the zero-sequence current will only flow in the primary side windings [30]. This prevents the zero-sequence current from returning to the DC link and it is widely used in UPS applications[30]. However, this topology will not solve the unbalanced/nonlinear load conditions caused by the negative-sequence current. Another disadvantage is the size of the transformer which makes the whole system bulky and expensive.

A similar topology utilizes a zig-zag transformer instead of a Δ/Y transformer [31]. This is based on the idea that the zero-sequence current can be cancelled out using the phase shift of each phase of the transformer. The size and cost are still a disadvantage for this topology.

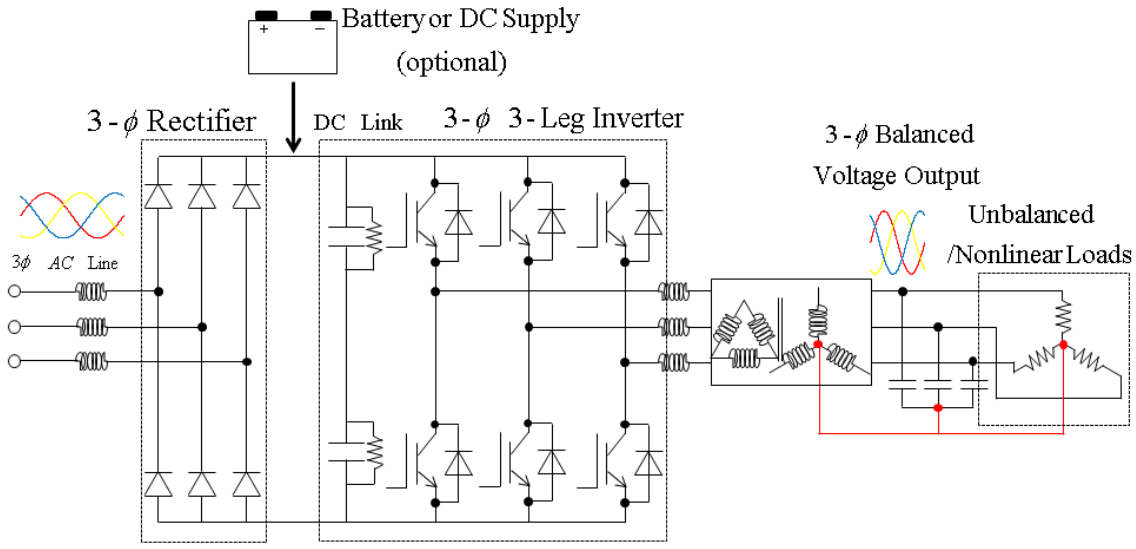



Figure 2.5 A three-phase four-wire VSI with a Δ/Y transformer

### 2.4.3 A three-phase four-leg VSI

A three-phase four-leg voltage source inverter was introduced to handle the neutral current caused by unbalanced and/or nonlinear load conditions [18]. As it is shown in Figure 2.6, the load star point is connected to the mid-point of a fourth leg of the converter, by doing so, the neutral point is now controllable through the fourth leg. The advantages of this topology are listed below:

- Full DC link utilization. Unlike the three-phase four-wire VSI with split DC link capacitors, the star point of the loads is now free to vary by controlling the fourth leg. Therefore maximum unity DC link utilization can be realized by adopting switching schemes such as 3-D SVM[32], carrier-based PWM[33] and other switching schemes. These will be presented in more detail in the following sections.

- The DC link capacitors can be smaller compared to the split DC link option. Since the star point of the loads is now tied to the mid-point of the fourth leg, there is no need to use two large capacitors for the DC link.

- A transformer-less converter. Compared to the converters which are either use Δ/Y transformer or zig-zag transformer, this topology does not have the considerable weight and size of a transformer. An extra pair of the IGBT/diode is comparatively small size/weight increase compared with a transformer. Of course, a more complicated switching scheme and control method are needed for this topology; however, with the availability of the modern digital signal processor, this should not present a problem.

- EMI and common-mode voltage reduction. In any fast switching power electric system, EMI is a potential problem which increases with the voltage levels[27]. For a three-phase system, common-mode voltage switching noise is a significant EMI source[24]. By controlling the fourth leg, the common-mode voltage can be reduced to a certain level[34].

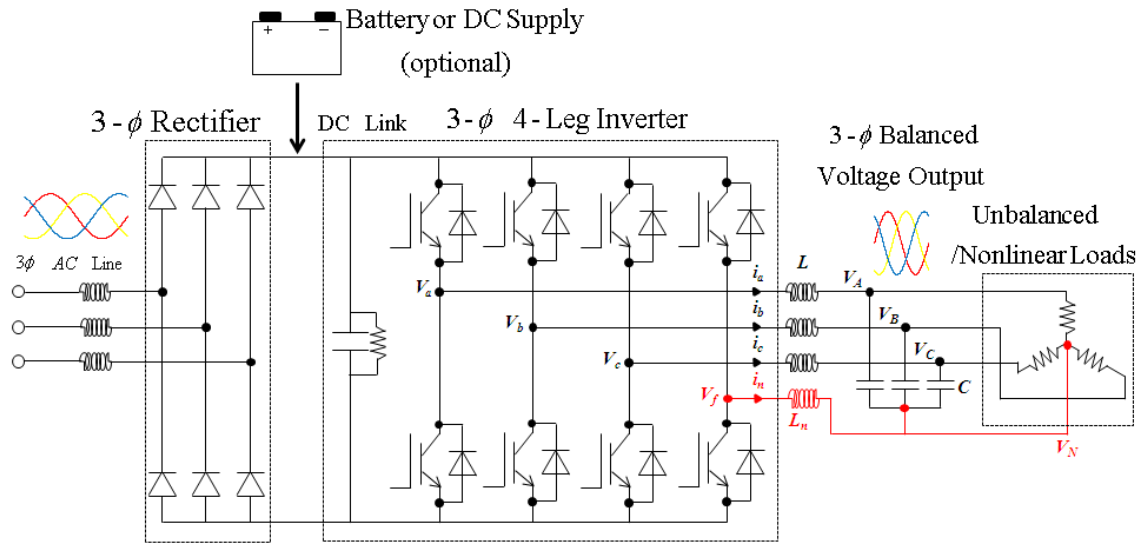



Figure 2.6 A three-phase four-leg VSI

## 2.5 Switching schemes for three-phase power systems

Power conversions include four different types, namely, DC to DC conversion, DC to AC conversion, AC to DC conversion and AC to AC conversion. All of these conversions are performed in a switching mode in which power electronics devices are switched on and off at a high repetition rate. The actual power flow in power converter is controlled by the on/off ratio, or the duty ratio of the respective switches[35]. The desired output of the power converters is achieved by varying the duty cycles either constant or sinusoidal with time, employing the technique of pulse width modulation (PWM)[35].

The following sections present a review of different types of PWM switching schemes. Starting from the switching schemes for three-phase three-leg VSI, the switching schemes that are implemented on a three-phase four-leg inverter are then introduced.

### 2.5.1 Switching schemes for three-phase three-leg VSI

For a three-phase voltage source inverter, a three-phase sinusoidal voltage or current is the control target. The first sinusoidal PWM switching scheme was based on the idea that three-phase sinusoidal reference signals are compared with a high frequency carrier-wave signal; the resulting signals are used for the gate drive signals to the switching devices. Because the output voltage and current distortions, switching loss of the power electronic devices and the EMI are closely related to the switching schemes [36], various derivations of sinusoidal PWM were developed [27]. There has been

intensive research on the topics of different switching schemes in terms of the output performance. The switching schemes might be classified into the following categories:

- Sinusoidal PWM and its derivations
- Space Vector Modulation
- Generalized discontinuous pulse width modulation
- Reduced common-mode voltage PWM
- Generalized carried-based PWM

Before the details are given on the different switching schemes, the definition of modulation index *Mi* must be given. According to [35], the modulation index value is defined as

$$Mi = \frac{u_1}{u_{1six-step}} \tag{2.10}$$

where $u_1$ is the fundamental phase voltage and $u_{1\text{six-step}}$ is the fundamental voltage of the six-step operation of the three-phase inverter. The maximum modulation index value, which is unity, can be only obtained if the converter is working under six-step mode, which in most of the power converter applications cannot be achieved.

Another definition, which is given by

$$Mi = \frac{\hat{V}_{ll}}{V_{DC}} \tag{2.11}$$

where $\hat{V}_{ll}$ is the peak-to-peak value of the line-to-line voltage of the converter output, $V_{\text{DC}}$ is the DC link voltage of the converter. By this definition, the unity modulation index is the limit of "linear" modulation range. After that, *Mi* can be increased through a further range before 6-step operation results. The maximum modulation index can be achieved as unity by adopting switching scheme such as space vector modulation and other PWM switching schemes. Therefore, this definition is chosen to represent the modulation index in this dissertation. Also, it is shown in [37, 38] that modulation index value is related to the quality of the output voltage and current under certain switching schemes. In [39], it is shown that some switching schemes have their limited linearity range. These will be given in details in the following sections.

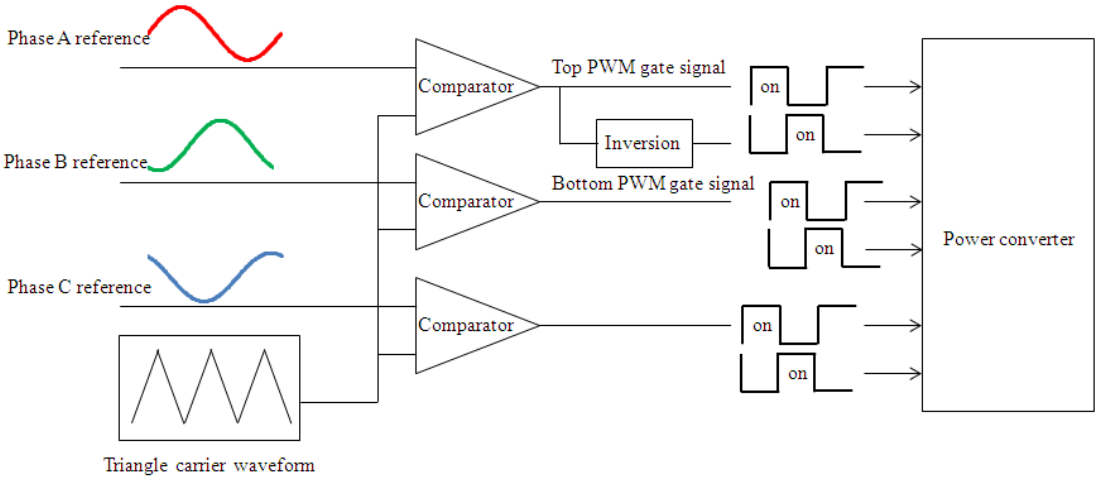



Figure 2.7 Sinusoidal PWM modulation

#### 2.5.1.1Sinusoidal PWM and its derivations

Sinusoidal PWM is the simplest PWM switching scheme which is easy to implement both in analogue circuit or digital circuit form[27]. It is also referred to as sine-triangle modulation because it is normally a triangular shape carrier waveform that is compared with three-phase sinusoidal reference as it is shown in Figure 2.7.

Simplicity and ease of implementation are the main advantages of this switching scheme. However, the drawbacks include insufficient DC link utilization since the maximum modulation index that can be reached is only $\sqrt{3}/2$ [27], that is 15% less compared to other switching schemes. The harmonic distortion of sinusoidal PWM is higher than other switching schemes, especially at high modulation index [35, 37, 40]. Since there're no zero switching states during the transient switching states, the switching loss is higher than some other switching schemes.

Because of the above disadvantages, there have been efforts to modify the sinusoidal PWM. The following switching schemes are some examples.

**A. Third-harmonic injection PWM**

Based on the sinusoidal PWM, a third-harmonic injection PWM adds a third harmonic component into the reference signal of each phase. By doing so, the neutral point of the system follows the third harmonic component around the $0.5V_{DC}$, where in sinusoidal PWM, the average neutral point is at $0.5V_{DC}$ [27]. Since the third harmonic component is exactly the same for each phase with no phase difference, the effective cancellation of the third harmonic component can be seen in the line-to-line voltage. As a result, a

higher fundamental phase voltage is obtained. The reference signal is given in Eq. (2.12) and the reference signal, which consists of a higher fundamental component and a third harmonic component, can be seen in Figure 2.8.

$$f(\omega t) = \frac{2}{\sqrt{3}}\sin(\omega t) + \frac{1}{3\sqrt{3}}\sin(3\omega t) \tag{2.12}$$

### B. 60° PWM

Third-harmonic injection PWM effectively increases the phase voltage by approximately 15% compared to sinusoidal PWM, realizing the full DC link utilization. In fact, the harmonic cancellation applies for all the tripling component such as $9^{th}$, $15^{th}$, etc because of the zero phase shifts of these components. 60° PWM utilizes the above tripling components as is shown in Eq. (2.13). As a result, not only the full DC link utilization has been achieved, a "flap-top" of the modulation index has been obtained from 60° to 120° and 240° to 300° as shown in Figure 2.9.

$$f(\omega t) = \frac{2}{\sqrt{3}}\sin(\omega t) + \frac{1}{2\pi}\sin(3\omega t) + \frac{1}{60\pi}\sin(9\omega t) + \frac{1}{280\pi}\sin(15\omega t) \tag{2.13}$$

During the time when the modulation index is clamped at the top or the bottom, the power electronics devices will not have any switching actions [35]. Therefore, any modulation index that has the "flap-top" characteristic will reduce switching loss in the power converter. In this case, since the total clamp time over one power cycle is 120°, a total 33% of the switching loss can be saved.

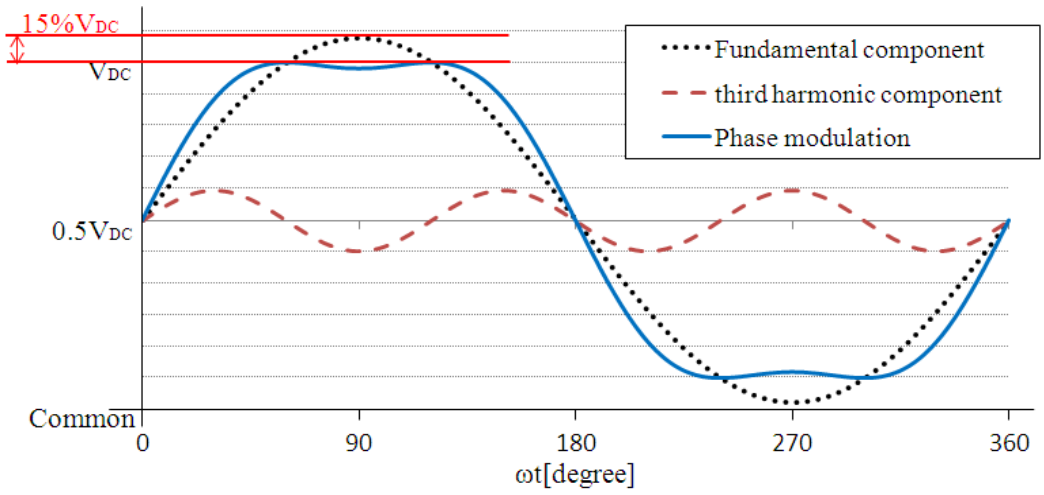



Figure 2.8 Third harmonic injected PWM

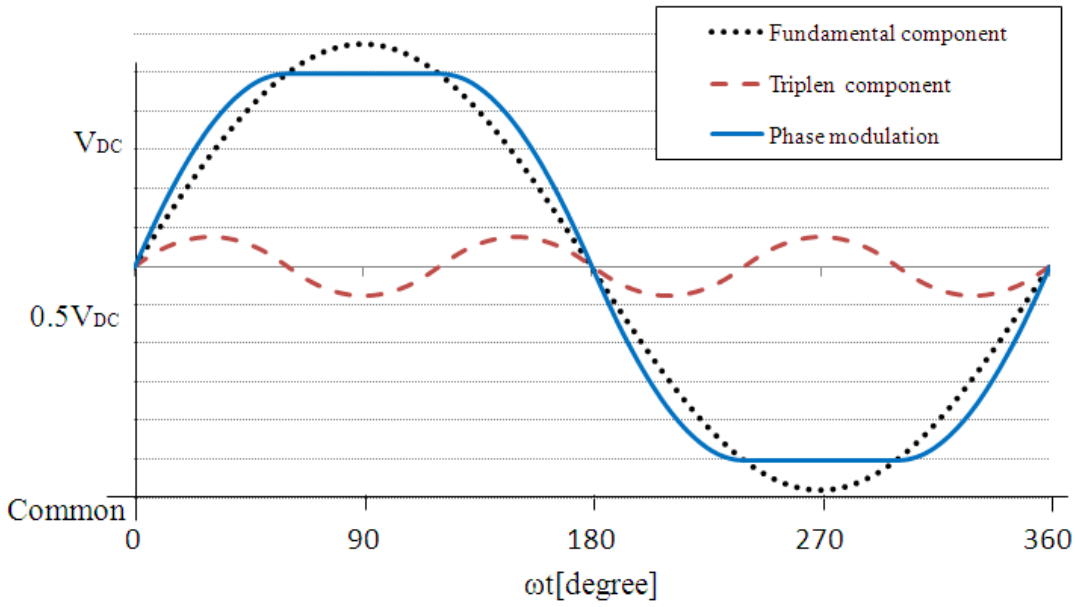



Figure 2.9 60° PWM

### 2.5.1.2 Space Vector Modulation (SVM)

Unlike the simple idea of comparing the carrier waveform with a reference signal to generate the switching signals, space vector modulation (SVM) is a quite different switching scheme [27, 35, 41, 42]. The switching scheme is based on the eight switching states of the three-phase VSI as shown in Figure 2.10; each switching state of the converter can be represented as a space vector. Transforming these switching states in the *A-B-C* coordinate into *α-β* coordinate is the most effective way to analyze the switching states. On the *α-β* plane, the six non-zero switching vectors $\vec{V}_1$-$\vec{V}_6$ form a hexagon while the two zero switching states $\vec{V}_z$ are in the middle of the hexagon as shown in Figure 2.11. Between two adjacent switching vectors, a transient switching vector can be obtained by applying the relevant switching vectors for certain time duration. Therefore, a rotating reference vector $\vec{V}_{ref}$ can be synthesized within each switching cycle. Without considering over-modulation, the trajectory of the reference vector is within the inner circle of the hexagon. The reference vector rotates at the electrical frequency of $\omega$. In each sector of the hexagon, the two adjacent switching vectors and one or two of the zero switching vectors are utilized to make the averaged switching vector equal to the reference switching vector. Finally the chosen switching vectors have to be sequenced in a way to generate the gate signals to the switching power converter. The whole process of the SVM can be seen in Figure 2.11.

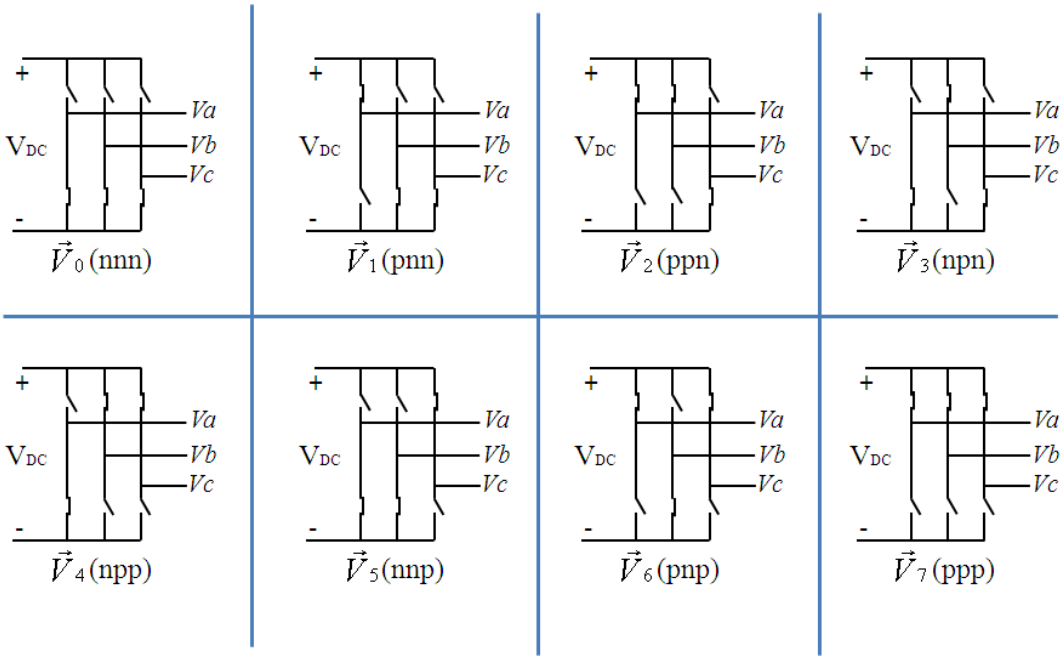



Figure 2.10 Switching states of the VSI and their switching vectors

**Choice of zero space vector $\vec{V}_z$ and sequencing of the selected switching vectors**

It is worth noticing that the choice of zero space vector $\vec{V}_z$ and the sequencing of the selected switching vectors play a vital role in forming the various modulation index waveforms. In most cases, the adjacent switching vectors are chosen, together with the zero space vectors to synthesize the reference vector. Only in some switching schemes which aim to reduce the common-mode voltage that different selections of the switching vectors are applied [43], as detailed in the next section. It has been shown in [32] that in terms of output voltage quality such as harmonic distortion, centre-aligned PWM achieves the lowest distortion compared to rising-edge, falling edge and alternative sequence. Therefore, centre-aligned switching is chosen in this dissertation to demonstrate all the SVM switching schemes.

There are different combinations in terms of choosing the zero space vector $\vec{V}_z$. The following options summarize nearly all the possible choices.

- Scheme 1: Choosing both $\vec{V}_7$ and $\vec{V}_0$ in each sector of the hexagon.
- Scheme 2: Choosing $\vec{V}_7$, $\vec{V}_0$ alternatively in each sector of the hexagon, in other words, $\vec{V}_7$ in Sector 1,3,5 and $\vec{V}_0$ in Sector 2,4,6 or $\vec{V}_0$ in Sector 1,3,5 and $\vec{V}_7$ in Sector 2,4,6.
- Scheme 3: Choosing either $\vec{V}_7$ or $\vec{V}_0$ in each sector of the hexagon.

- Scheme 4: Choosing $\vec{V}_7$, $\vec{V}_0$ alternatively by 60°, starts with $\vec{V}_Z$=$\vec{V}_7$ from region B1[26], namely, -30° from the α-axis.
- Scheme 5: Choosing $\vec{V}_0$, $\vec{V}_7$ alternatively by 60°, starts with $\vec{V}_Z$=$\vec{V}_0$ from region B1.
- Scheme 6: Choosing $\vec{V}_7$, $\vec{V}_0$ alternatively by 60°, but not strict to the sector.
- Scheme 7: Choosing neither of the zero space vectors.

The resulting modulation index waveforms of different schemes are shown in Figure 2.12. In Figure 2.12(a), scheme 1 is shown, which achieves the lowest harmonic distortion because of its symmetrically aligned characteristic [27, 32]. However, since there is no modulation index clamping, the switching loss of this scheme is high. Figure 2.12(b) and (c) show the two modulation index waveforms of scheme 2. Although these two waveforms are quite similar, the switching loss can be significant different depending on the load conditions. For inductive loads such as induction machine running in motoring mode, (b) will have lower switching loss because the modulation index clamping occurs during the time when the current is at its highest. For the same reason, (c) will have lower switching loss if the load is capacitive such as the induction machine running in a generating mode. Scheme 3 as shown in Figure 2.12(d) and (e) are not seen regularly in applications. $\vec{V}_z$=$\vec{V}_7$ may not work with the bootstrap circuits properly due to the failure of charge of the capacitor on top switches [27]. Scheme 4(shown in Figure 2.12(f)), often called DPWM1[35, 37], is generally considered the best discontinuous PWM switching scheme in terms of output voltage distortion, switching loss and linear operating range, especially for unity power factor load such as synchronous machine [32, 37, 38, 40, 43]. Scheme 5 is called DPWM3 and has rarely been seen in the literature, possible reasons include higher harmonic contents and small switching loss savings [37, 42, 44] compared to other schemes. Figure 2.12 (g) shows the waveform of DPWM3.

Scheme 6 is defined as generalized discontinuous SVM since the discontinuous part of the modulation index waveform varies according to the load condition. This scheme is more referred to as generalized discontinuous PWM depends on its scalar implementation. Scheme 7 can be referred to as common-mode voltage reduced SVM [39, 43]. Due to their unique characteristics, scheme 6 and 7 will be given in details in the next sections.

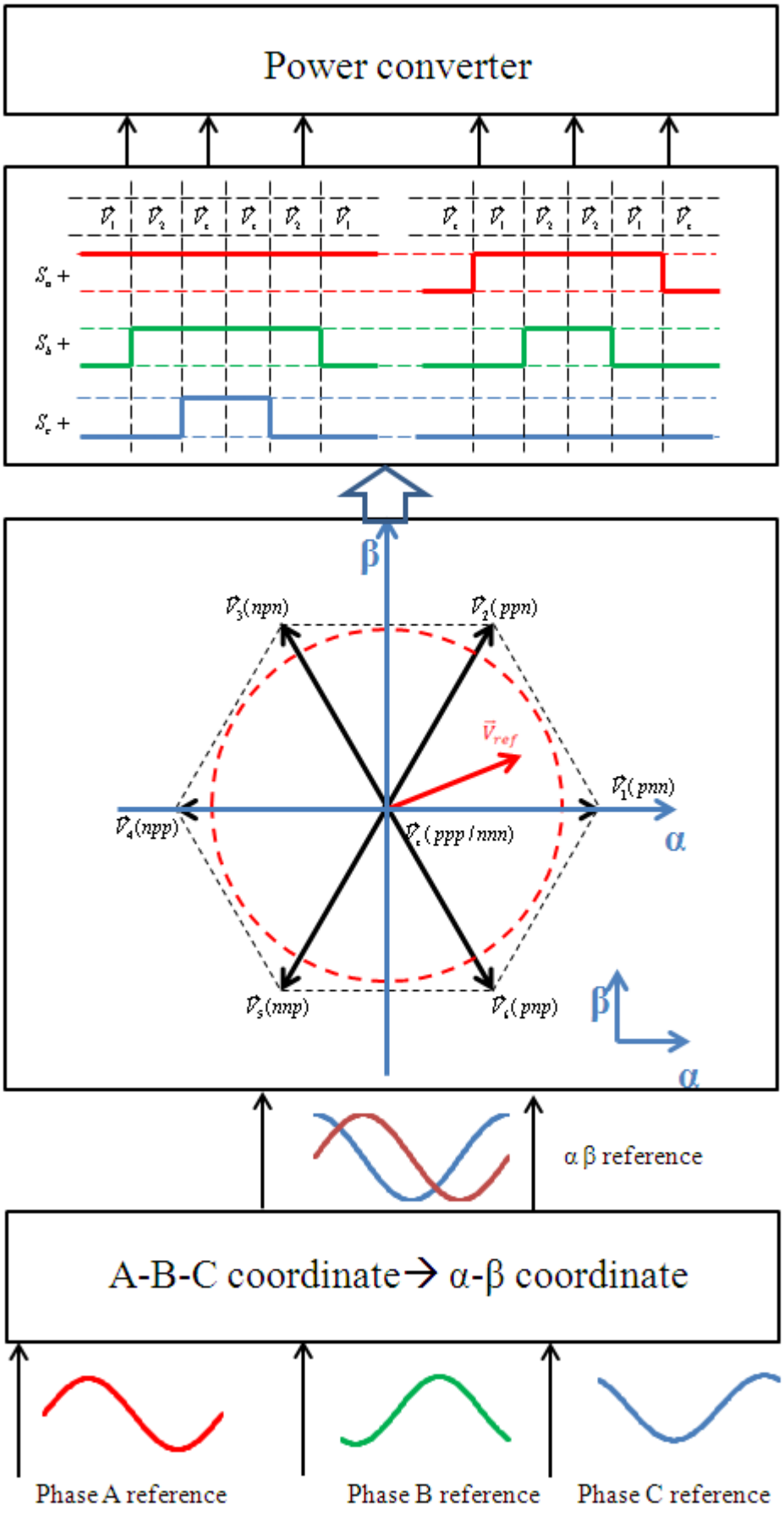



Figure 2.11 Block diagram of SVM

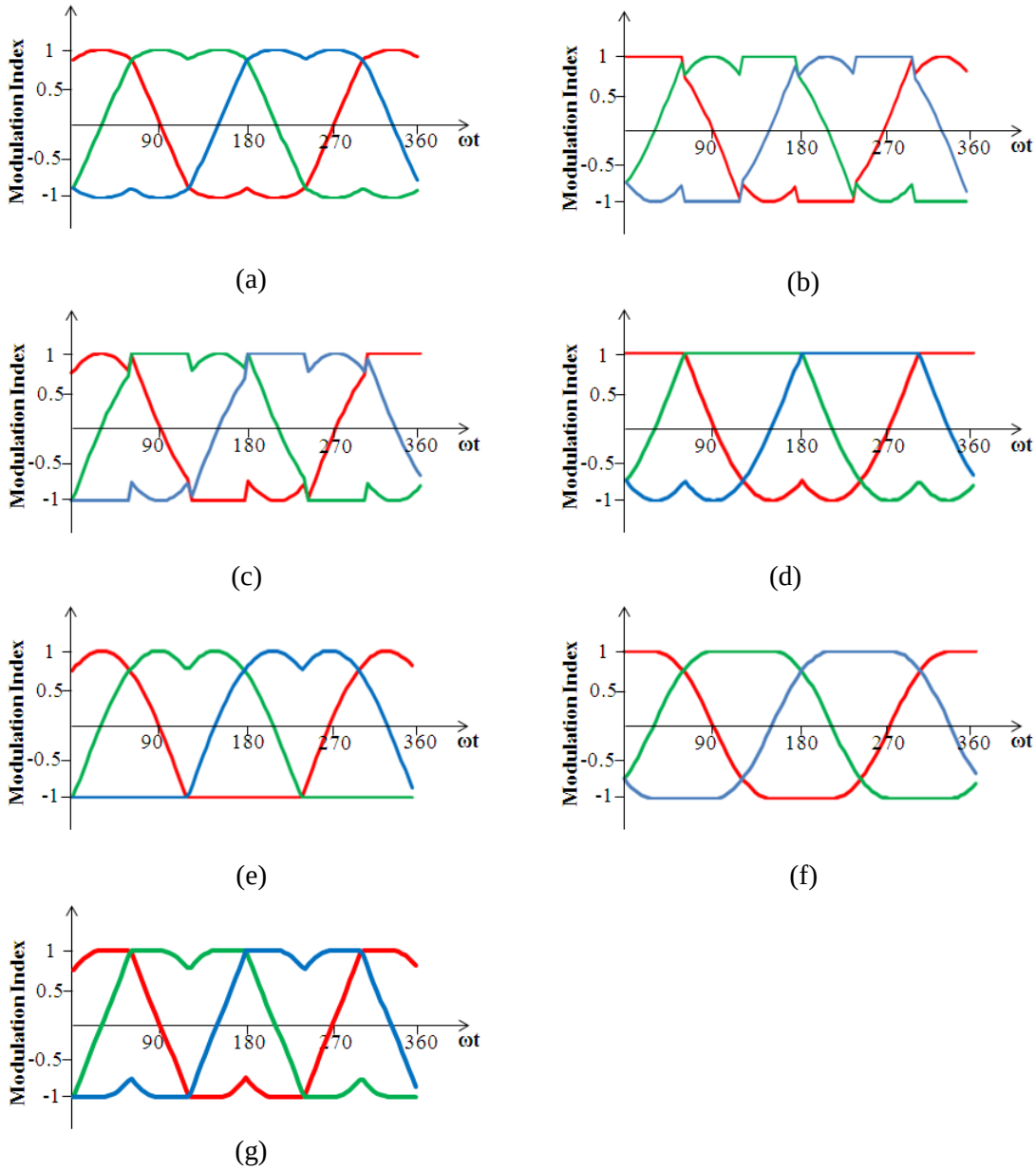



Figure 2.12 Switching schemes based on the selection of $\vec{V}_z$, $Mi$=1; (a) Scheme 1, $\vec{V}_z$=$\vec{V}_7$&$\vec{V}_0$ in each sector; (b) Scheme 2, $\vec{V}_z$=$\vec{V}_7$ in Sector 1,3,5 and $\vec{V}_z$=$\vec{V}_0$ in Sector 2,4,6; (c) Scheme 2, $\vec{V}_z$=$\vec{V}_0$ in Sector 1,3,5 and $\vec{V}_z$=$\vec{V}_7$ in Sector 2,4,6; (d) Scheme 3, $\vec{V}_z$=$\vec{V}_7$; (e) Scheme 3, $\vec{V}_z$=$\vec{V}_0$; (f) Scheme 4, DPWM1; (g) Scheme 5, DPWM3

### 2.5.1.3 Generalized discontinuous pulse width modulation (GDPWM)

In the previous section, variations of discontinuous PWM patterns are shown. However, each particular scheme is tailored for a particular load condition. In recent years, there is intensive research on what is called "generalized discontinuous PWM (GDPWM)" [38, 40, 42, 45]. The proposed switching scheme can change its switching pattern according to the varying load conditions. The implementations of the discontinuous PWM can be

divided into two types, namely scalar implementation and direct digital implementation. In [38, 40], a maximum magnitude test is used in the scalar implementation of the switching scheme. Scalar implementation is easy to implement, however, the drawback is the traditional controller design based on the rotating *d-q* axis cannot be achieved since the idea of the rotating switching vector is lost. Direct digital technique is used in [42, 45], although the calculation might be more complex compared to the scalar implementation, the rotating switching vector is obtained. Besides, for modern digital signal processor, the calculation will not become a software burden. The aim of the generalized discontinuous PWM is to achieve minimum switching loss over a wide modulation range under varying load conditions.

#### 2.5.1.4 Reduced common-mode voltage PWM

The common-mode voltage (CMV) of the three-phase system is defined as the voltage potential difference between the star point of the load network and the mid-point of the DC link capacitors [39]. Therefore, each switching state of the converter has its own related common-mode voltage level as shown in Table 2-2. It has been shown that the two zero switching states have the highest voltage level of $\pm V_{DC}/2$. The reduced common-mode voltage PWM method aims to reduce the common-mode voltage level by avoiding the two zero switching states ($\vec{V}_7$ and $\vec{V}_0$). Various switching schemes have been reported in the literature survey[46, 47], however, few are feasible[26]. In practice, limitations such as dead time delay and simultaneous switching of one phase pose problems.

**Table 2-2 Switching states and related common-mode voltage**

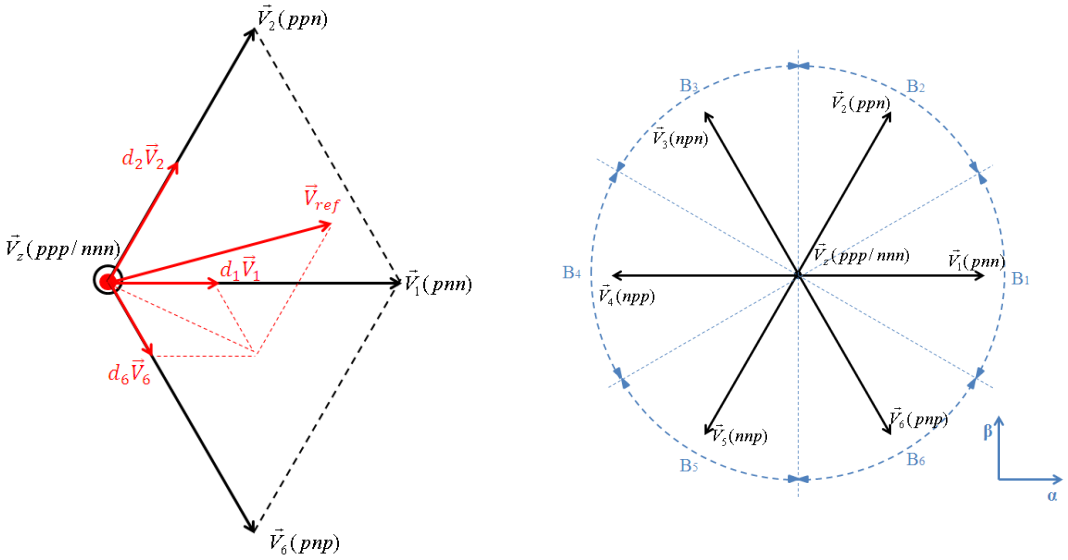
| Switching state | ppp | Pnn | ppn | npn |
|---|---|---|---|---|
| CMV | $V_{DC}/2$ | $-V_{DC}/6$ | $V_{DC}/6$ | $-V_{DC}/6$ |
| Switching state | npp | Nnp | pnp | ppp |
| CMV | $V_{DC}/6$ | $-V_{DC}/6$ | $V_{DC}/6$ | $-V_{DC}/2$ |

Among all these PWM methods that yield reduced CMV, active zero state PWM (AZSPWM) [46, 47] and near state PWM (NSPWM) [39, 43] deserve dedicated attention [26]. The ideas behind these switching schemes are almost the same. Instead of using two adjacent switching vectors and one or two of the zero switching vectors; three or four non-zero switching vectors are utilized to synthesize the reference switching vector. A near-state PWM is demonstrated here to illustrate how the switching scheme works.

As it is shown in Figure 2.13(a), synthesis of the reference vector in NSPWM utilizes three non-zero switching vectors $\vec{V}_1, \vec{V}_2$ and $\vec{V}_3$ for section $B_1$. The six sectors have to be redefined as $B_1$-$B_6$ for NSPWM as it is shown in Figure 2.13(b). As it can be seen, each new section has 30° phase shift with the conventional sector. Figure 2.14 shows the inverter switching states and the common-mode voltage patterns of the NSPWM in section $B_1$ and $B_2$. It shows clearly that there are only $\pm V_{DC}/6$ voltage levels in the CMV. The higher levels of $\pm V_{DC}/2$ have been reduced.

The big advantage of this switching scheme is that it reduces the common-mode voltage without sacrificing the DC link utilization and at the same time maintains the minimum switching loss since the actual modulation index waveform is exactly the same as DPWM1. However, there are two drawbacks of this switching scheme. First is the limitation of linear operating range. The effective operating range of the modulation index is limited to the range of 0.6667 to 1.0[39, 43]. However, this will not pose a serious problem for applications such as high power UPS system since most of the time, the system works under a high modulation index range. Another drawback is when implementing the scheme in a real-time system; six PWM channels will be used instead of three. The reason for this is that for a switching pattern as shown in Figure 2.14, two carrier waveforms are needed for each phase [39].

There are other reported PWM switching schemes that can reduce CMV[26], however, these methods require simultaneous switching between different phases. This cannot be realized due to the dead time effect and even if it is possible to do so, the sudden change of the line-to-line voltage leads to significant terminal overvoltage[26].




(a) NSPWM switching vectors for section $B_1$ (b) Redefined section area for NSPWM

Figure 2.13 A near state PWM method ;(a) NSPWM switching vectors for section $B_1$, (b) Redefined section area for NSPWM

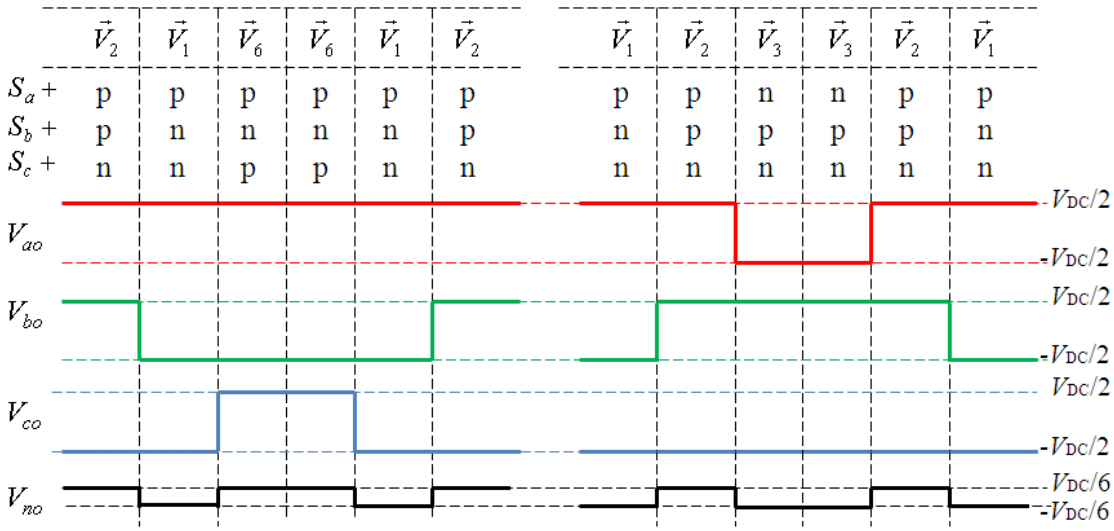



Figure 2.14 CMV pulse patterns of NSPWM in section $B_1$,$B_2$

### 2.5.1.5 Generalized carrier-based PWM (CBPWM)

As opposed to space vector modulation (SVM), a generalized carrier-based PWM (CBPWM) aims to have the same modulation index waveform as the SVM by implementing a scalar version of the switching scheme. In essence, it is based on the same idea as the sine-triangle modulation except in this case the reference signal is not sinusoidal. In [41], the relationship between the carrier based PWM and SVM has been fully analyzed, for each available SVM, there is an equivalent carrier-based PWM. The main advantage of the carrier based PWM is its simplicity in implementation, however, it also loses the concept of rotating reference vector. In [37, 40], a maximum magnitude

test is used to generate the reference signal. In [41], analysis and calculation on the pulses pattern were carried out so as to generate the reference signal.

### 2.5.2 Switching schemes for three-phase four-leg VSI

The previously discussed switching schemes for a conventional three-phase three-leg VSI, whether they're scalar or digitally implemented, are well established and their implementation is not difficult. For a three-phase four-leg VSI, the addition of a fourth leg makes the switching states become $2^4$=16. This means the switching schemes that can be applied on the four-leg inverter are more complex than the conventional switching schemes implemented on the three-leg inverter[48]. The following sections list the switching schemes that are implemented on the three-phase four-leg VSI.

#### 2.5.2.1 Three-dimensional space vector modulation (3-D SVM)

The concept of three-dimensional space vector modulation (3-D SVM) was invented by Richard Zhang and was first published in [18, 49]. Since the day of its invention, this scheme was regarded as the best switching scheme for a three-phase four-leg VSI under unbalanced/nonlinear load conditions[15, 19, 32, 50, 51]. There are sixteen switching states of the converter as shown in Figure 2.15. After transforming the switching vectors in *A-B-C* coordinate to the *α-β-γ* coordinate, they are located in a three-dimensional space as shown in Figure 2.16, that's where the name "3-D" comes from. The transformation between the *A-B-C* and *α-β-γ* are given by Eq. (2.14) and Eq. (2.15).

$$\begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2.14}$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} \tag{2.15}$$

where *X* could be *V* or *I* for the three-phase power system.

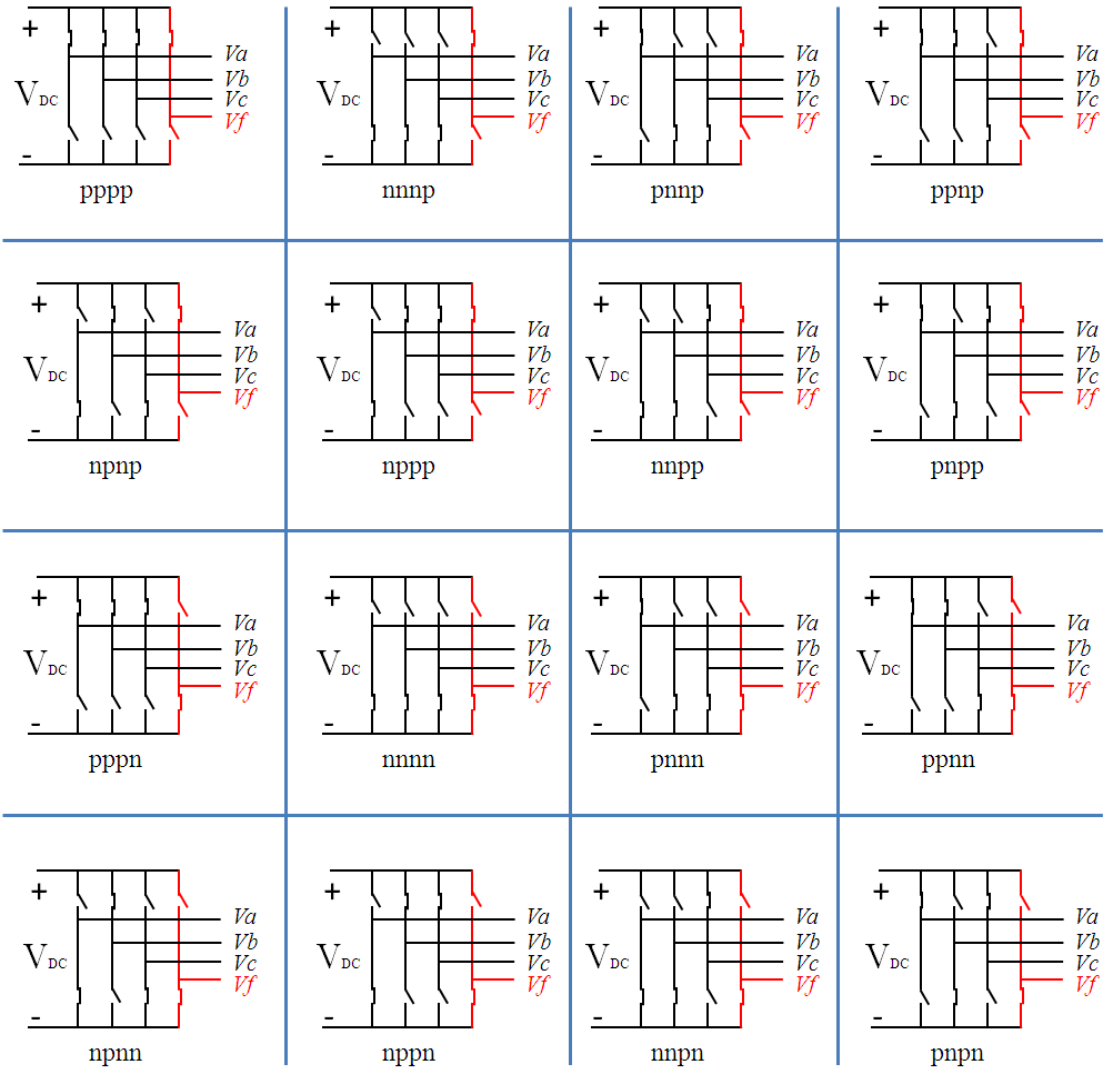



Figure 2.15 Sixteen switching states of the four-leg VSI

In Figure 2.16, it is shown that among all the sixteen switching vectors, there are two zero switching vectors (pppp, nnnn) which are located in the middle layer of the space. The other fourteen non-zero switching vectors are located in different layers according to the different voltage levels of $V_\gamma$. It should be noted that $V_\gamma$ is the zero-sequence component and related to the neutral current [18, 32]. There are altogether seven different voltage levels of $V_\gamma$ and therefore seven layers of the space. The projection of the switching vectors on $\alpha$-$\beta$ plane is also shown in Figure 2.16. As it can be seen, the projection of $V_\alpha$ and $V_\beta$ form the same circle as that of the conventional SVM.

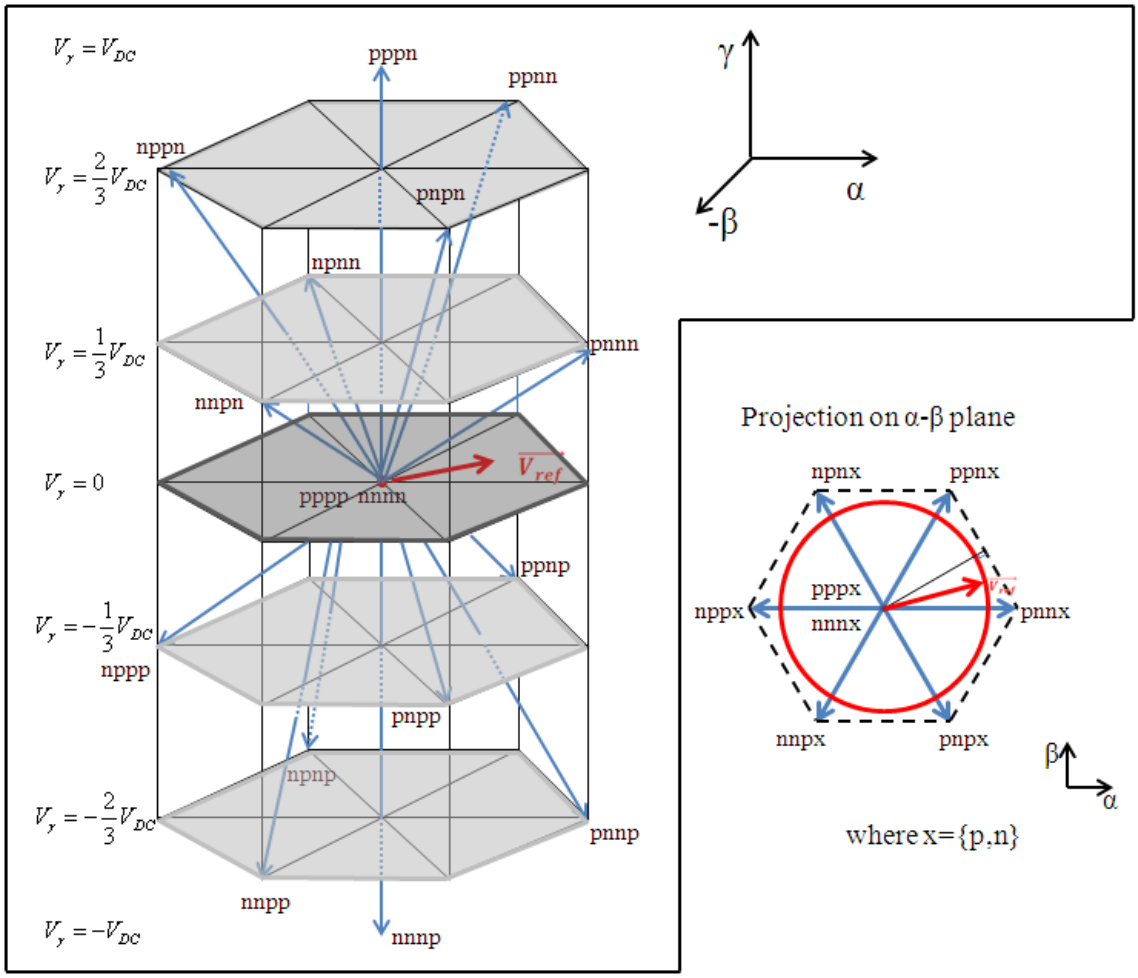



Figure 2.16 Sixteen switching vectors in *α-β-γ* coordinate and their projection

Synthesis of the rotating reference vector in the *α-β-γ* coordinate takes the following steps[32]:

- Prism and tetrahedron identification
- Projection of the reference vector
- Sequencing of the selected switching vectors
- Generation of modulation index

**Prism and tetrahedron identification**

For conventional SVM (2-D), the synthesis of the rotating reference vector is straightforward since the adjacent switching vectors are always chosen. For the same reason, adjacent switching vectors in the *α-β-γ* coordinate have to be selected. However, the adjacent switching vectors in the three-dimensional space are not easy to identify. It takes two steps to choose the adjacent switching vectors, namely, prism identification and tetrahedron identification [32]. As it can be seen in Figure 2.17, six prisms can be

identified in the space like the six sectors in the conventional SVM(It should be noted for demonstration purposes, each prism rotates by 60 degree from the previous prism). As it was discussed in the previous section, the knowledge of $V_\alpha$ and $V_\beta$ of the rotating reference vector will determine in which prism the reference vector locates. It is also noticed that in each prism, there're six non-zero switching vectors and two zero switching vectors that can be used. After the prism identification, four tetrahedrons are identified in each prism as shown in Figure 2.18. Each tetrahedron consists of three non-zero switching vectors and two zero switching vectors. These vectors are the adjacent switching vectors that are going to be used to synthesize the reference vector. To decide in which tetrahedron the rotating reference vector locates, the information of the phase voltages in *A-B-C* coordinate is needed, as it was stated in [50], the tetrahedron can be selected by directly comparing the relative sizes of the phase voltages and zero.

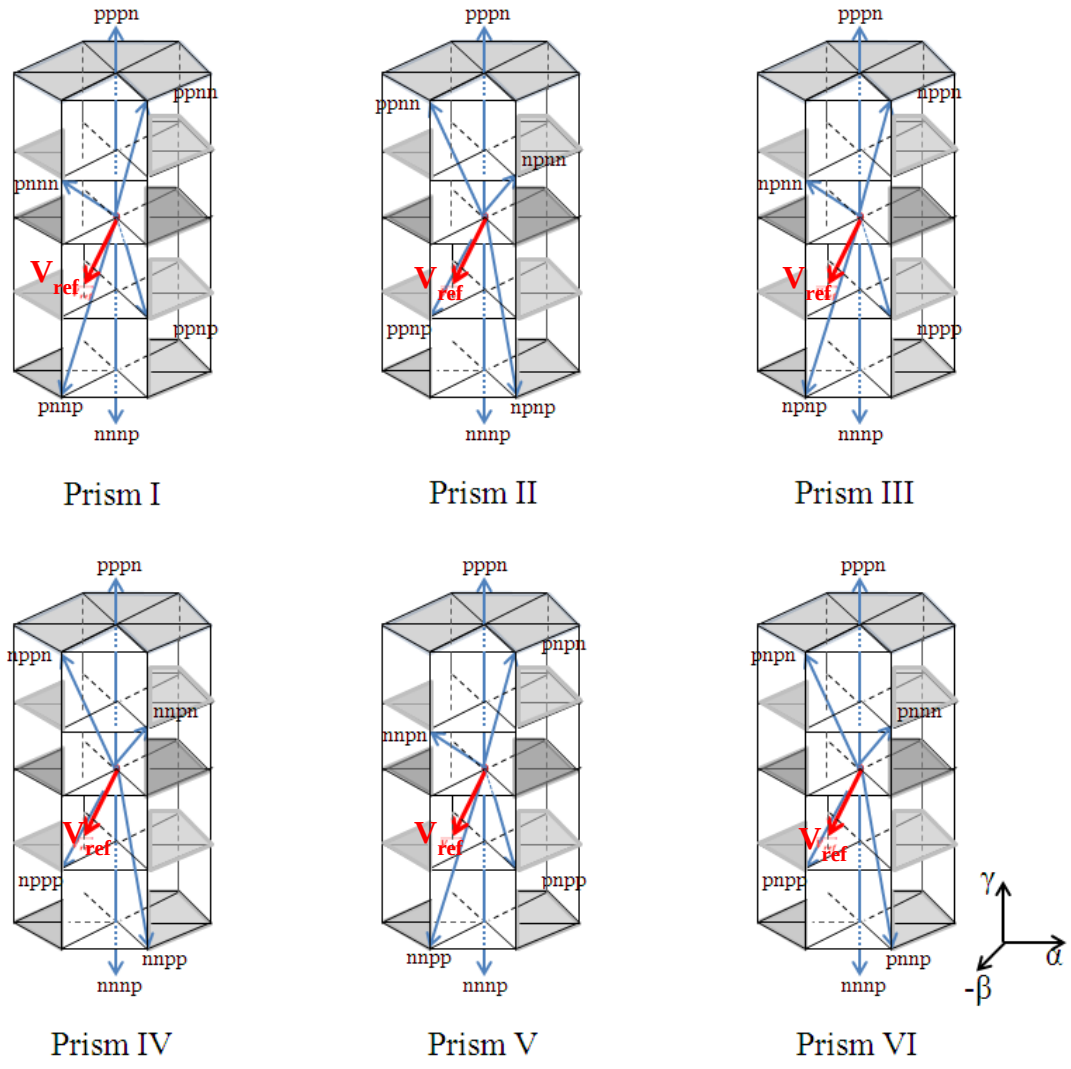



Figure 2.17 Prism Identification of the switching vectors

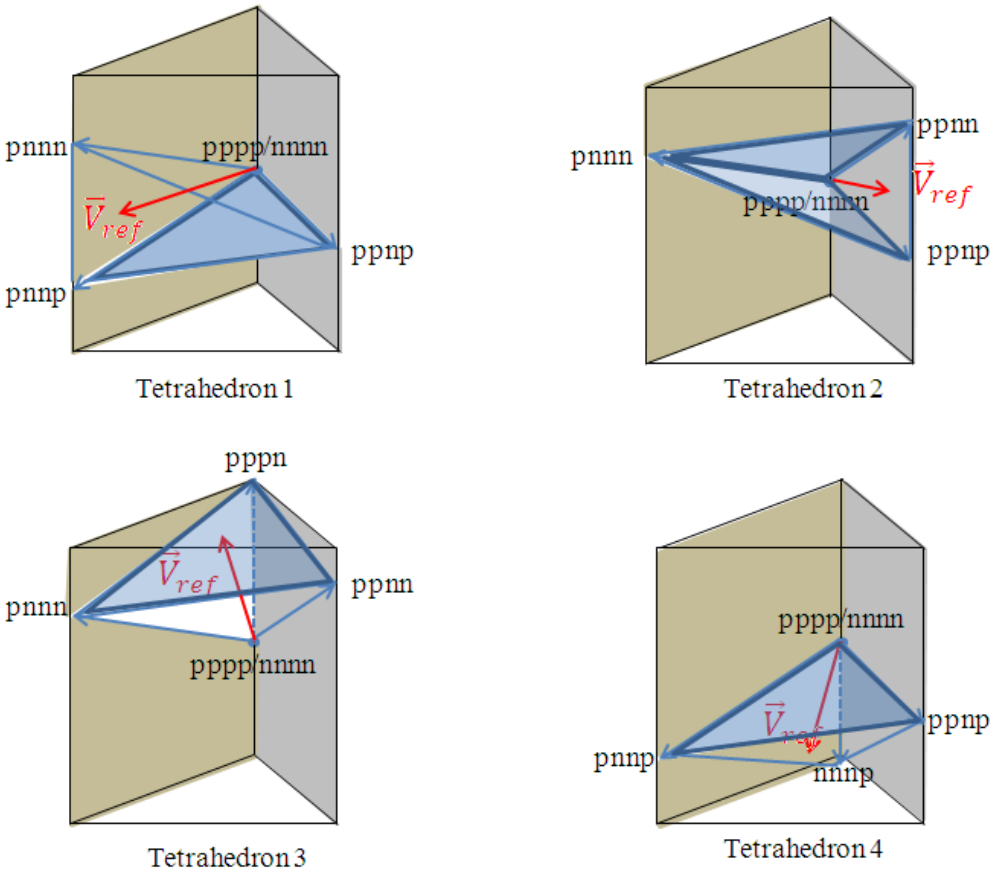



Figure 2.18 Tetrahedron identification in Prism 1

**Projection of the reference vector**

The duration of each selected switching vector can be calculated by projecting the reference vector on the switching vectors. The calculations are shown in Eq. (2.16), (2.17) and (2.18).

$$\vec{V}ref = d_1\vec{V}_1 + d_2\vec{V}_2 + d_3\vec{V}_3 \tag{2.16}$$

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_{DC}} G \begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} \tag{2.17}$$

$$d_z = 1 - d_1 - d_2 - d_3 \tag{2.18}$$

where $d$ is the duration of each selected switching vector, $G$ is the matrix needed to compute the duty ratios and can be found in [32].

**Sequencing of the selected switching vectors**

Sequencing of the selected switching vectors follows the same rule as the conventional SVM. In [32], two classes of the switching schemes are compared and analyzed. It is concluded in [32] that Class II centre-aligned is the best compromise between the switching loss and harmonic content and is normally adopted in real-time implementation.

**Generation of modulation index**

The waveform of modulation index can be derived from the duty ratios of the switching vectors $d_1$, $d_2$, $d_3$ and $d_z$ and sequencing scheme used[32]. For demonstration purposes, a balanced load condition is studied here. The modulation index waveform is obtained by supplying a balanced three-phase sinusoidal reference signal as in Eq. (2.19)

$$\begin{bmatrix} V_{ab\_ref} \\ V_{bc\_ref} \\ V_{ca\_ref} \end{bmatrix} = MiV_{DC} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 120°) \\ \sin(\omega t + 120°) \end{bmatrix} \tag{2.19}$$

Based on Eq. (2.14), the trajectory of the rotating reference vector is a circle only based on the layer of $V_\gamma$=0. The rotating reference vector in $\alpha$-$\beta$-$\gamma$ coordinate is then given by

$$\begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} = \frac{Mi}{\sqrt{3}} V_{DC} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \\ 0 \end{bmatrix} \tag{2.20}$$

The modulation index waveform is shown in Figure 2.19, with the continuous lines showing the modulation index for the first three phases, while the dashed line showing that for the fourth leg. The block diagram of 3-D SVM can be seen in Figure 2.20.

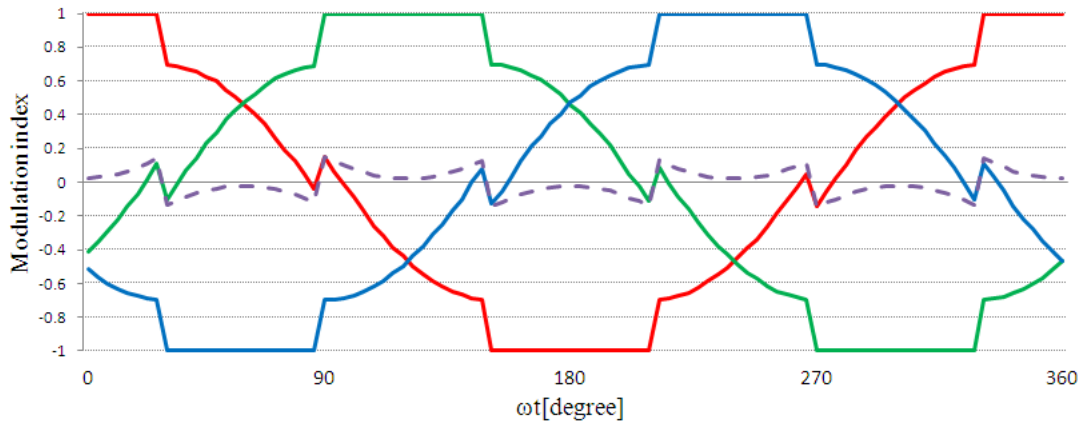



Figure 2.19 Modulation index waveform for 3-D SVM, Mi=0.85

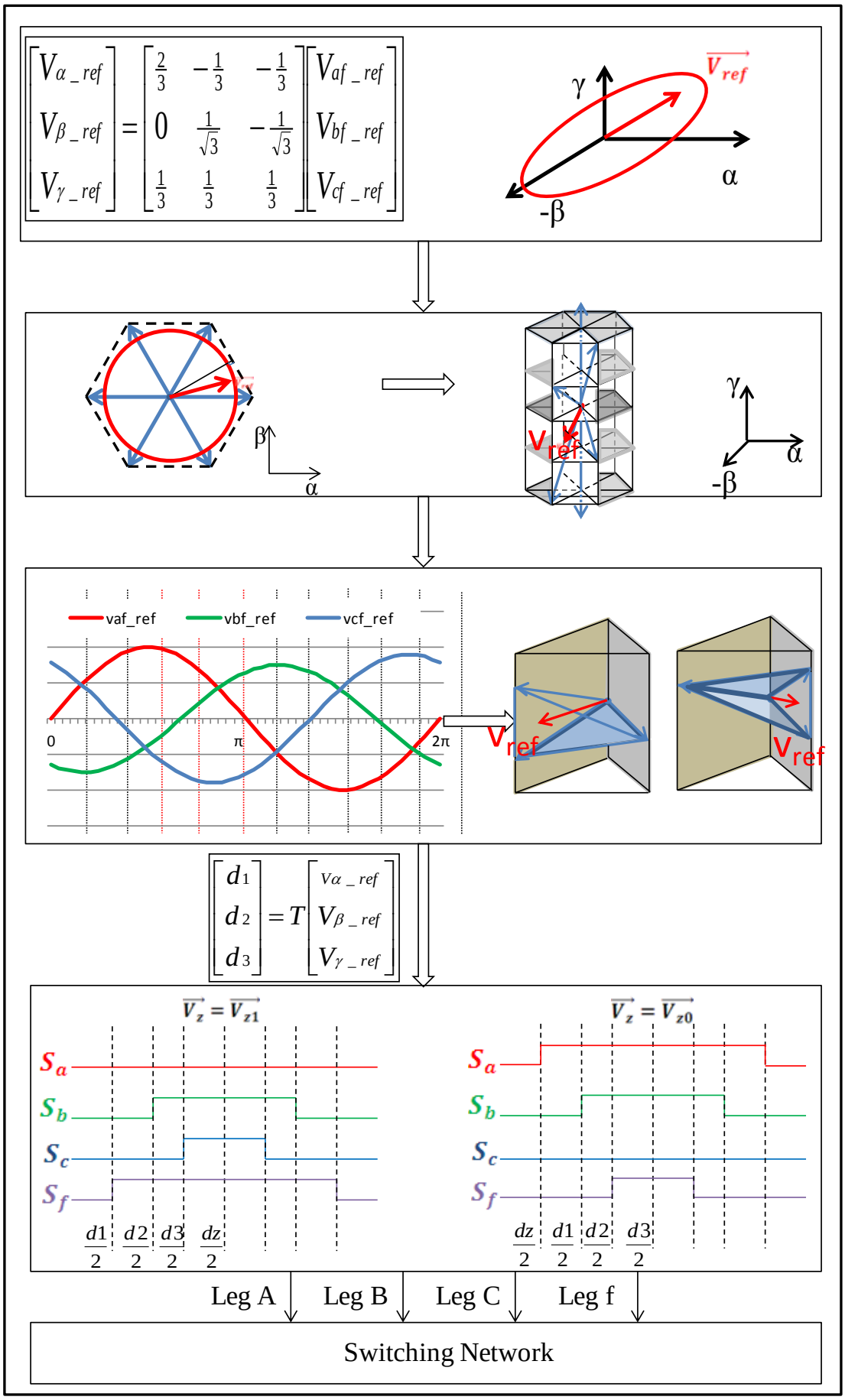



Figure 2.20 Block diagram of 3-D SVM

### 2.5.2.2Three-dimensional SVM in *A-B-C* coordinate

In spite of all the advantages that 3-D SVM enjoys, one of the drawbacks of the 3-D SVM is the complexity of the scheme. Prism and tetrahedron identification is not easy to understand, therefore, recent years have witnessed intensive research on simplification of the 3-D SVM. The transformation between the *A-B-C* and the *α-β-γ* coordinates can be removed if the *A-B-C* coordinate is used. It is argued in [15, 50, 51] that the algorithm is simplified by using the *A-B-C* coordinate. However, this scheme cannot avoid the location of the reference switching vector and the location of the reference vector, which takes almost the same steps as 3-D SVM in *α-β-γ* coordinate. The algorithm cannot be easily simplified because of the characteristics of the 3-D SVM.

### 2.5.2.3 Carrier-based PWM for four-leg VSI

Three-dimensional SVM is based on the concept of switching vectors corresponding to the switching states of the converter. Without using the concept of switching vectors, carrier-based PWM scheme can be used in scalar implementation for four-leg VSI [13, 33] and it is proved to be equivalent to 3-D SVM under open loop operation[33]. The modulation index waveforms for the first three phases follow the same rule as CBPWM for three-leg VSI. An offset voltage signal is then calculated for the fourth leg. The block diagram of the carrier-based PWM is shown in Figure 2.21. The variations of the modulation index waveforms depend on the offset modulation calculation. The fourth-leg modulation index should be within the envelope of the minimum and maximum function. In [35, 37], a similar idea was presented, the offset modulation index was called injected signal in this case. The calculation is different with that in [13, 33], therefore the boundary of the injected signal waveform is different.

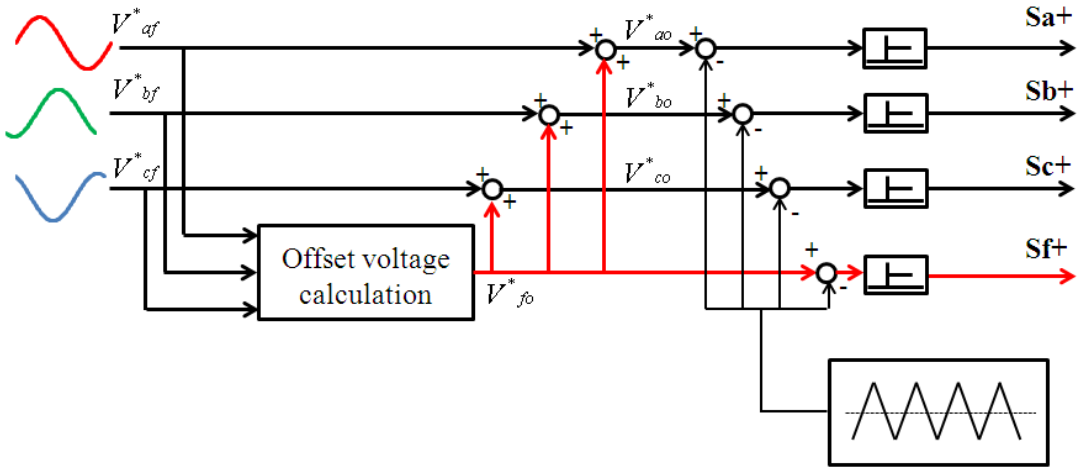



Figure 2.21 Block diagram of the carrier-based PWM for four-leg VSI

As it can be seen from Figure 2.21, the terminal phase reference voltages are given by

$$\begin{bmatrix} V^*_{ao} \\ V^*_{bo} \\ V^*_{co} \end{bmatrix} = \begin{bmatrix} V^*_{af} \\ V^*_{bf} \\ V^*_{cf} \end{bmatrix} + V^*_{fo} \tag{2.21}$$

The offset voltage calculation is then given by Eq. (2.22)[14]

$$V^*_{fo} = \begin{cases} (0.5-\xi)V_{DC} - \xi V^*_{\min}, V^*_{\max} < 0 \\ (0.5-\xi)V_{DC} + (\xi-1)V^*_{\max}, V^*_{\min} > 0 \\ (0.5-\xi)V_{DC} + (\xi-1)V^*_{\max} - \xi V^*_{\min}, elsewhere \end{cases} \tag{2.22}$$

where $V^*_{\max}$ =max($V^*_{af}$, $V^*_{bf}$, $V^*_{cf}$), $V^*_{\min}$ =min($V^*_{af}$, $V^*_{bf}$, $V^*_{cf}$) and $\zeta$ is called the zero-state partitioning function, and is defined as Eq. (2.23)[14]

$$\xi = \frac{t_{nnnn}}{t_{nnnn} + t_{pppp}} \tag{2.23}$$

where $t_{\text{nnnn}}$ is the time of the switching state where four bottom switches are on and $t_{\text{pppp}}$ is the time of the switching state where four top switches are on.

Thus the $\zeta$-based offset voltage calculation establishes the unification of the carrier-based PWM switching scheme for four-leg VSI.

The big advantage of CBPWM for four-leg VSI is its simplicity and therefore low cost of implementation. However, the performance under an unbalanced load condition is not clear. Another drawback of this switching scheme is a controller design based on *d-q-o* coordinate, or the synchronous reference frame is not possible since there is no rotating reference vector [52].

In [52], the authors stated that because of the ineffectiveness of the classical synchronous reference frame PI control, individual phase control should be used instead. Also in this paper, another modulation technique is adopted for the generation of CBPWM. The fourth-leg voltage is given by

$$V^*_{fo} = \frac{V_{DC}}{2}(1-2\zeta) - \zeta V_{\min} - (1-\zeta)V_{\max} \tag{2.24}$$

where $V_{\max}$ and $V_{\min}$ are the instantaneous maximum and minimum magnitudes of the three-phase reference phase voltages, $\zeta$ is the zero switching state partitioning parameter[52] and is given by

$$\zeta = 0.5 \times [1 - \text{sgn}(\cos(3\omega t + \delta))] \tag{2.25}$$

where $\delta$ is the modulation angle, variation of the modulation indexes is achieved by varying $\delta$. This method has the same drawbacks as any other CBPWM switching scheme.

**Over-modulated sinusoidal PWM**

Earlier work of Dr David, J Atkinson adopted another carrier based PWM switching scheme for a three-phase four-leg VSI. Aiming at the full DC link utilization, a three-phase over-modulated reference signal is given by

$$\begin{bmatrix} V^*_{af} \\ V^*_{bf} \\ V^*_{cf} \end{bmatrix} = Mi' \frac{V_{DC}}{2} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 120°) \\ \sin(\omega t + 120°) \end{bmatrix} \tag{2.26}$$

where $Mi'$ is the over-modulated modulation index, the maximum value of which is 1.15, meaning the full DC link utilization can be achieved.

Then the reference voltage signals for the first three phases can be obtained by

$$V^*_x = \begin{cases} \frac{V_{DC}}{2}, (V^*_{xf} > \frac{V_{DC}}{2}) \\ -\frac{V_{DC}}{2}, (V^*_{xf} < -\frac{V_{DC}}{2}) \\ V^*_{xf}, else \end{cases} \tag{2.27}$$

$$x = a, b, c$$

The fourth-leg reference voltage signal depends on the per-phase offset calculation given by

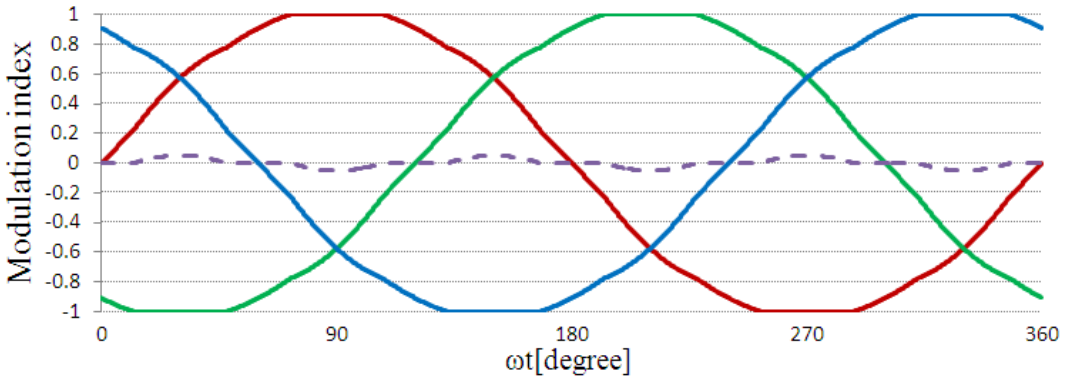
$$V^*_{fo\_x} = \begin{cases} \frac{V_{DC}}{2} - V^*_{xf}, (V^*_{xf} > \frac{V_{DC}}{2}) \\ -\frac{V_{DC}}{2} - V^*_{xf}, (V^*_{xf} < -\frac{V_{DC}}{2}) \\ 0, else \end{cases} \tag{2.28}$$

$$x = a, b, c$$

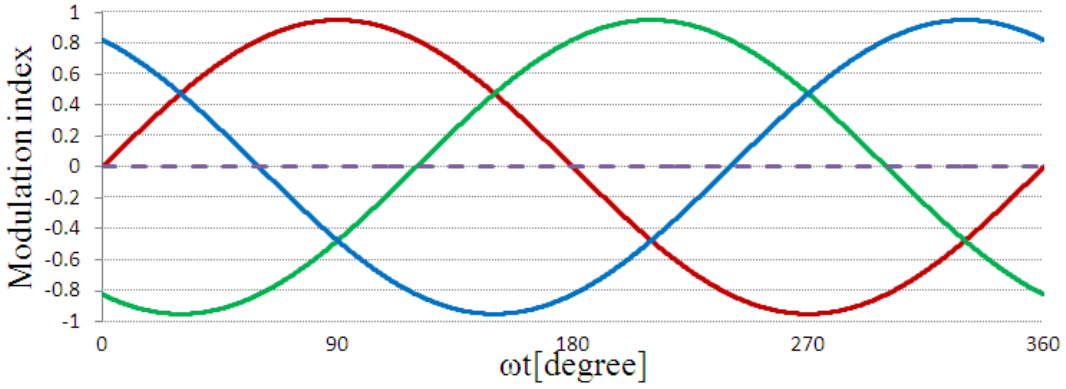
Therefore the fourth-leg reference voltage signal is obtained

$$V^*_{fo} = \sum V^*_{fo\_x} \tag{2.29}$$

This switching scheme, when supplied with full modulation index $Mi'$=1.15, happens to have the same waveform as standard 3-D SVM, or DPWM1 for the carrier-based PWM. Although the implementation is relatively easy, under a modulation index range below the full modulation index, the clamping part of the waveform decreases as shown in Figure 2.22 (a). This means the relative switching loss will increase as the modulation index decreases. Figure 2.22 (a) shows the switching scheme under $Mi'$=1.05 and (b) shows the switching scheme when $Mi'$=0.95. As it can be seen, when the modulation index is below unity, the waveform shown becomes the same as sinusoidal PWM with the fourth-leg voltage held at $0.5V_{DC}$. Although this switching scheme may be the simplest in terms of real-time implementation, the switching loss increases when the modulation index decreases.




(a) $Mi'$=1.05




(b) $Mi'$=0.95

Figure 2.22 Another carrier-based PWM modulation index waveform under (a) $Mi'$=1.05,(b) $Mi'$=0.95

### 2.5.2.4 Minimum loss DPWM (MLDPWM)

The minimum loss DPWM switching scheme aims to achieve the minimum switching loss at certain load conditions. This switching scheme is specially designed for UPS systems where single-phase load operating condition is quite frequent [14]. The basic idea is based on the carrier-based PWM switching scheme for four-leg inverter, with the zero state partitioning function $\zeta_{\text{MLDPWM}}$ given by

$$\xi_{MLDPWM} = \begin{cases} 0, |I_{V\max}| > |I_{V\min}| \\ 1, |I_{V\max}| < |I_{V\min}| \end{cases} \tag{2.30}$$

where $I_{V\text{max}}$ and $I_{V\text{min}}$ are the phase current magnitudes of $V^*_{\text{max}}$ and $V^*_{\text{min}}$, respectively [14].

Under normal operating conditions, e.g. a balanced load condition, the resulting waveform of the modulation index is the same as standard 3-D SVM or DPWM1. When under single-phase loading condition, the fourth-leg carries the same level of current as the phase current. In this case, the switching loss of standard 3-D SVM or DPWM1 becomes significant. With 240° modulation index clamp for the phase that carries the phase current (as shown in Figure 2.23, assuming phase A carries the largest current, current has been normalized in this case), The MLDPWM achieves around 25.2% less switching loss[14]. The modulation indexes for other phases are shown in Figure 2.24.

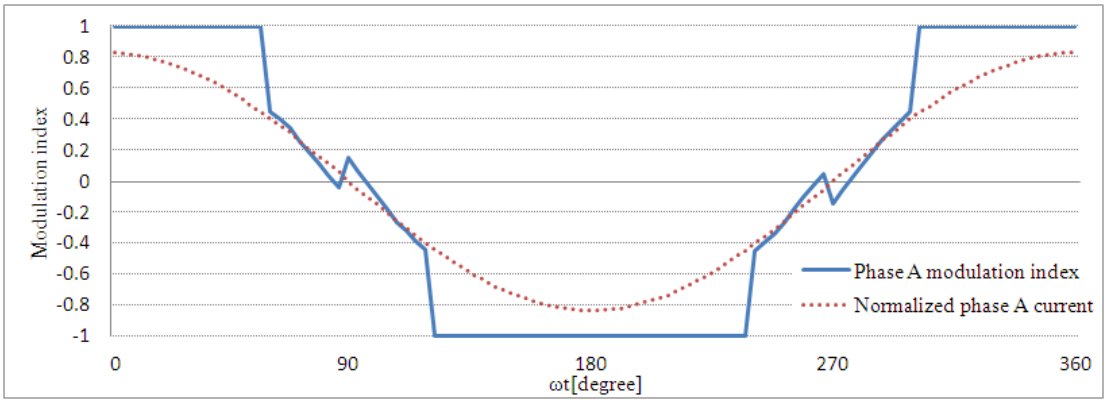



Figure 2.23 Phase A modulation index under MLDPWM, *Mi*=0.85

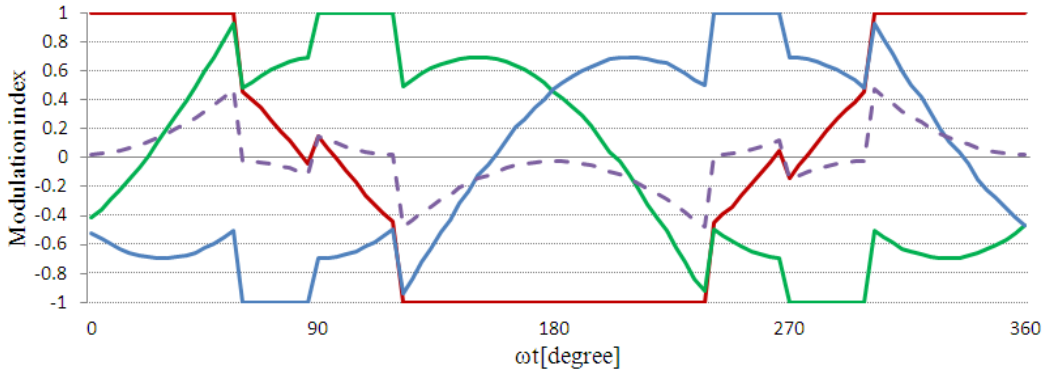



Figure 2.24 Modulation index waveform for MLDPWM, *Mi*=0.85

### 2.5.2.5 Selective harmonic elimination PWM (SHEPWM)

A selective harmonic elimination PWM (SHEPWM) switching scheme for a four-leg VSI was proposed in [53]. The SHEPWM for a three-leg inverter was described in [54], based on the idea of using Fourier-based equations, with the lower order non-triple harmonics eliminated. The SHEPWM for four-leg VSI aims to extend this technique in four-leg inverters, especially under unbalanced load condition. However, this technique is proposed for a low switching-to-fundamental frequency application, with switching-to-fundamental frequency ratio of 13 per unit[53]. When it comes to a high switching frequency application (5 kHz - 20 kHz), the calculation needed for the algorithm becomes too complicated, therefore limits its implementation.

So far, nearly all the switching schemes for a three-phase system have been studied. Switching schemes that are based on the space vectors rely on the information of the rotating reference vector and are generally compatible with the real-time DSP implementation. Carrier-based PWM switching schemes are relatively easier to implement compared to the SVM schemes and therefore are implemented using scalar implementation technique.

## 2.6 Analytical and graphical methods for PWM-VSI drives

Recent years have witnessed research on analytical and graphical methods for the study, performance evaluation of modern PWM switching schemes [26, 37]. The performance of a three-phase VSI depends on the output waveform quality, switching loss and sometimes over-modulation performance.

For VSI drives, the output waveform quality is mainly related to the output harmonics content [55]. For a three-phase four-leg VSI, total harmonics distortion is normally used to determine the quality of the output voltage[32]. Conduction and switching loss of the

power electronics devices not only depend on the switching frequency, turn-on time and turn-off time of the power switches, but also relate to the PWM switching schemes[56, 57]. Switching schemes that have discontinuous (or clamp on) waveforms have less switching loss compared to continuous PWM switching schemes[27]. Over-modulation operation is not often seen in applications where good quality outputs are expected, therefore the over-modulation operation is not presented in this dissertation.

### 2.6.1 Output voltage quality and THD

As was stated before, the output voltage quality is strongly related to the total harmonic distortion (THD). IEEE Std 519-1992 recommends the requirements for harmonic control in electrical power systems[58]. The total harmonic distortion, by definition, defines the effects of harmonics on power system voltage and could be used in low, medium and high voltage systems[58]. The THD is defined by

$$THD_V = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \tag{2.31}$$

where $h$ is the characteristic harmonic order, $V_{\mathrm{h}}$ is the harmonic voltage and $V_1$ is the fundamental voltage.

IEEE Std 519-1992 sets voltage limits at the point of common coupling (PCC) and asked the customers to be responsible for not causing excessive current harmonics[58]. For systems in which the bus voltage at the PCC is 69 kV and below, individual voltage distortion is limited to be below 3% and the THD is limited to be below 5%.

The Fast Fourier transformation (FFT) could be used to do spectral analysis of a given signal therefore could be used as a useful tool for THD calculations [59]. The algorithm requires a large amount of calculation, but with today's powerful computers and simulation software such as Matlab, the calculation can be done easily. The FFT could be implemented in a real-time DSP system providing a powerful DSP is selected[59].

### 2.6.2 Current harmonic distortion

For a variable speed drive application where the load is assumed to be balanced, current harmonic distortion is used as a factor to determine the output waveform quality [36, 55, 56, 60, 61]. In [37, 38, 40], harmonic distortion factor (HDF) was introduced. It has been found that the HDF is related to the modulation index value and the switching

scheme chosen. Therefore, it serves as a useful tool to compare the performance of different switching schemes.

### 2.6.3 Conduction and switching loss

A major source of loss and inefficiency in power converters is the conduction and switching loss[62]. Conduction loss is normally due to the forward voltage drops on the semiconductor device and switching loss is related to the large instantaneous power loss in the semiconductor devices during the turn-on and turn-off [62].

Conduction loss is normally estimated using an approximation based on the voltage characteristics of the semiconductors chosen, and it is linked to the switching scheme of the VSI and the phase angle of the load[57]. Switching loss is strongly related to the switching frequency of the VSI, the current in each device and the device's dynamic characteristics[27].

The conduction loss is found to be associated with the on-time of the power devices and the on-time is related to the switching scheme[57]. In [57], calculations for different switching schemes were used to analyze the conduction loss in the three-phase VSD.

The switching loss depends to some extent on the modulation techniques employed for a three-phase inverter. The calculation of the switching loss is fairly complex since it involves many factors such as anti-parallel diode loss, fundamental frequency, switching frequency and the switching scheme.

An analytical switching loss calculation based on different modulation techniques for a three-phase VSI is presented in [35, 37, 40, 42, 49]. For clarity, conduction loss, forward voltage drop and IGBT tail current are neglected. The power loss during the switch-off of an IGBT is shown in Figure 2.25. The waveform of the switch-on power loss is quite similar to that of switch-off, with only the time axis reversed. Here we assume the power dissipations of the turn-on and turn-off are the same, therefore the switching power loss during one full switch (switch-on and switch-off) is given by Eq. (2.32).

$$P_{sw} = \frac{1}{T_s}\int p(t)dt = V_{DC} \times I_L \times (t_{off} - t_{on}) \times f_{sw} \tag{2.32}$$

where $P_{sw}$ is the power dissipated during on switching event, $I_L$ is the inductor current, $T_s$ is one switching period, $t_{on}$ is the on-time of the device, $t_{off}$ is the off time of the device and $f_{sw}$ is the switching frequency.

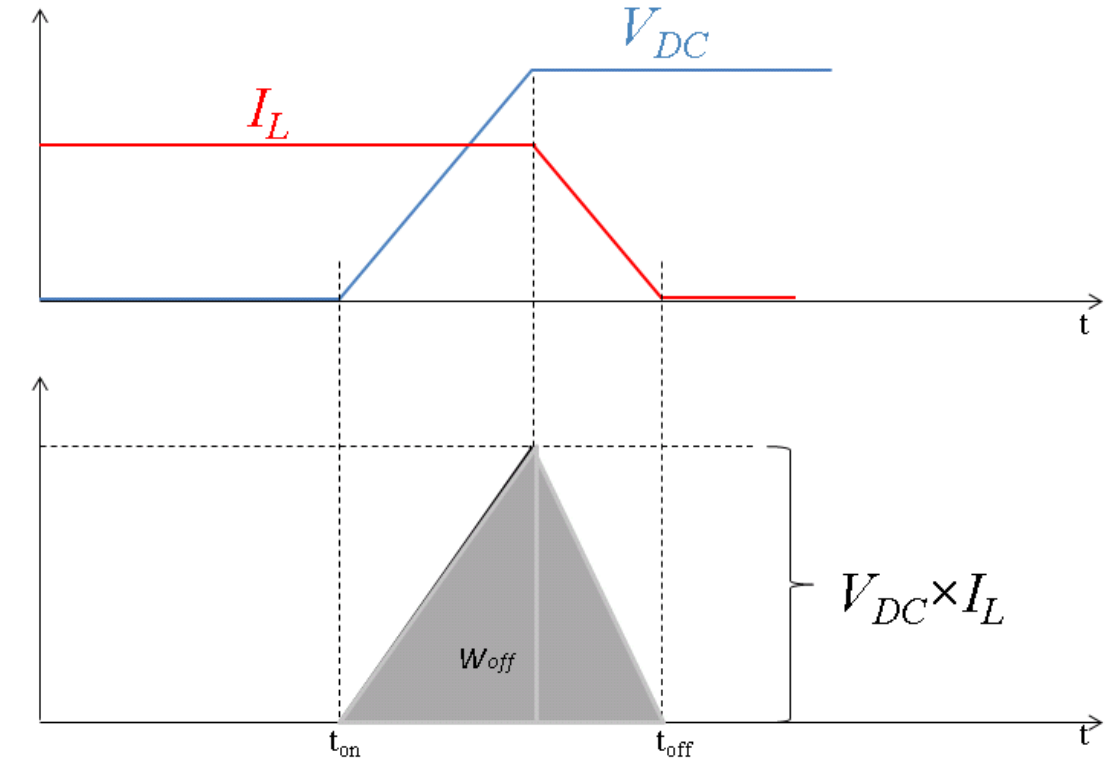



Figure 2.25 Switching loss of IGBT during turn-off transition

Therefore, the average switching loss over one power cycle can be obtained as

$$P = \frac{1}{2\pi}\frac{V_{DC}(t_{off}-t_{on})}{T_S}\int_0^{2\pi} f_i(\omega t)d\omega t \tag{2.33}$$

where $P$ is average switching loss over one power cycle, and the function $f_i(\omega t)$ is defined by Eq. (2.34) and its waveform is shown in Figure 2.26. As it can be seen, $f_i(\omega t)$ equals zero during the time when the modulation is clamped either at 1 or -1, and the absolute value of the current when $|Mi|<1$. Figure 2.26 also indicates that the function is related to the power factor angle $\varphi$.

$$f_i(\omega t) = \begin{cases} |I_L| & -1 < Mi < 1 \\ 0 & Mi = \pm 1 \end{cases} \tag{2.34}$$

It should be noted that the calculation is based on the steady state under balanced load condition. As a comparison, the switching loss under continuous PWM is defined in Eq. (2.35) and is $\varphi$ independent. The relative switching loss function RSL is then defined in Eq. (2.36).

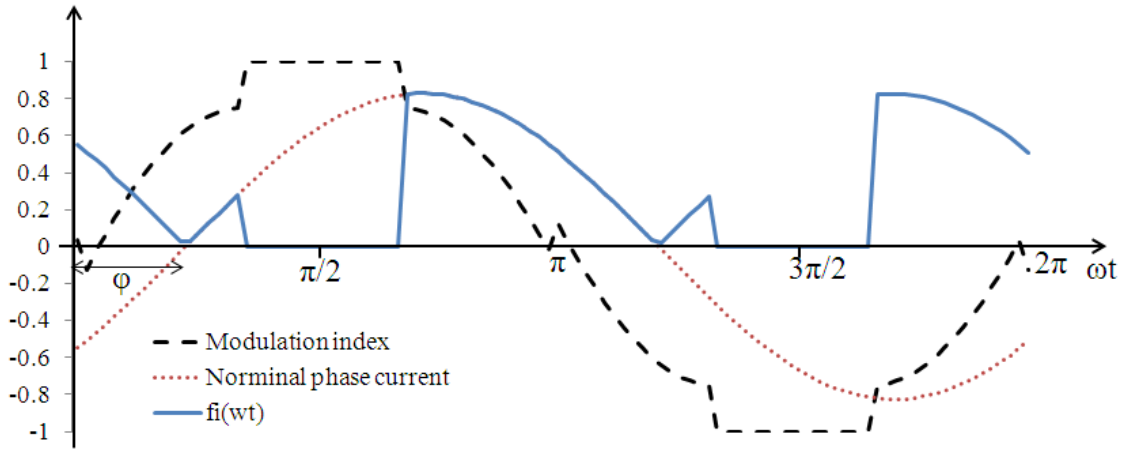



Figure 2.26 Waveform of $f_i(\omega t)$

$$P_0 = V_{DC} \times \hat{I}_L \times 2 \times (t_{off} - t_{on}) \times f_{sw} / \pi \tag{2.35}$$

$$RSL = P / P_0 \tag{2.36}$$

Based on the equations above, the relative switching loss of popular PWM switching schemes are compared and presented in [37, 40, 42]. It is concluded that the generalized discontinuous PWM switching scheme achieves the least switching loss over a wide range of power factor.

Switching loss analysis on a four-leg inverter is rarely seen in the literature. In [49], the authors present a comparison of relative switching loss between different schemes that are applied for a three-phase four-leg VSI. However, the details of calculation, especially when under unbalanced load condition is not given in the paper.

## 2.7 Output control of the three-phase four-leg VSI

Digital Signal Processor (DSP) has become more and more popular in power electronics, machine drive and control with powerful and fast calculation and other peripheral functions such as multi-channel PWM output with fault detection, A/D conversion, SCI and SPI communication, etc[59]. The size of the modern DSP is becoming smaller; therefore the cost is significantly reduced. It is insensitive towards parameter changes such as temperature. More complicated switching scheme and control algorithm can be implemented thanks to the fast computation speed of the DSP. The drawback of a DSP

is the time delay caused by sampling and sensing, which limits the control bandwidth[63].

Software such as Matlab provides some useful tools in terms of controller design. Close loop controller design in discrete time domain including the sampling and computation delay effect can be carried out using control and estimation tools in Matlab[63].

For high power converter systems, the switching frequency is limited (5 kHz-10 kHz) because of the conduction and switching loss of the power electronics devices [19]. The systems are often equipped with low-pass filter; the resonant frequency of the filter is normally designed below half of the switching frequency and higher than the fundamental frequency [28]. This limits the control bandwidth from the control point of view. In this case, feed forward control is normally introduced to compensate the slow dynamic behaviour of the voltage control loop.

Controller design varies based on different switching schemes. For space vector switching schemes, controller based on the synchronous reference frame is normally used while for carrier-based PWM, independent per-phase control based on natural reference frame is often seen in real-time system application. The following sections review the control strategies which are mostly seen for a high power three-phase four-leg voltage source inverter.

### 2.7.1 Output voltage control based on *d-q-o* rotating coordinate

Controller design in *d-q-o* rotating coordinate, which is also called synchronous reference frame control [7], is suitable for switching scheme such as 3-D SVM of a three-phase four-leg inverter. After the transformation from the *A-B-C* coordinate to *α-β-γ* coordinate, a rotating reference frame in *d-q-o* coordinate is obtained by

$$\begin{bmatrix} X_d \\ X_q \\ X_o \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} \tag{2.37}$$

By this means, controller design based on the DC operating point can be obtained [7]. The reason that the transformation is needed is because the steady state variables in *A-B-C* coordinate are sinusoidal; the absence of the DC operating point makes it difficult for the controller to track the reference signal due to the time varying characteristics of the reference signal. Figure 2.27 shows the average large signal model of the system in *A-B-C* coordinate and Figure 2.28 shows the average large signal model in *d-q-o*

coordinate[19]. It can be seen in Figure 2.28 that Channel d and q are coupled through terms of voltage source $\omega LI$ and current source $\omega CV$. This, when it comes to controller design based on each channel, presents a problem, especially when the load is not balanced [64]. The coupling voltage sources $\omega LI_d$ and $\omega LI_q$ can be easily decoupled in the controller design while the coupling current sources $\omega CV_d$ and $\omega CV_q$ presents a problem. It is suggested to use the concept of load conditioner to address the issue[19]. However, adding a load conditioner means adding the cost of the whole system, therefore it is used only under heavy nonlinear load condition.

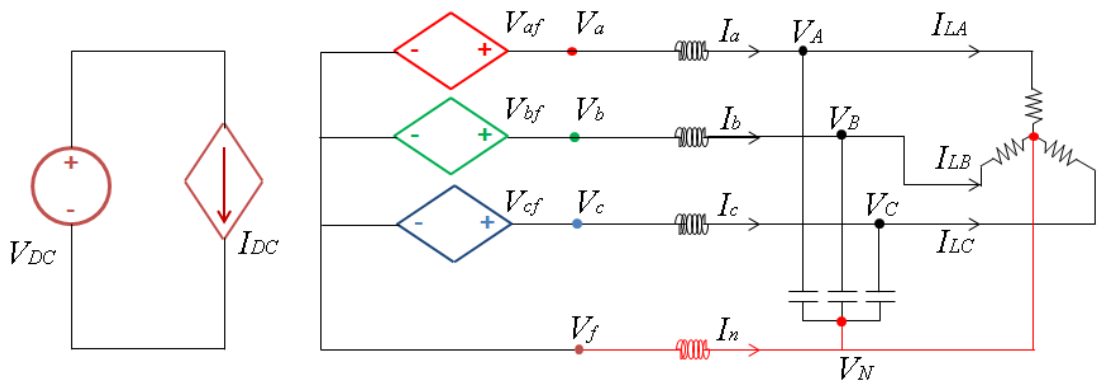



Figure 2.27 Average large signal model of a four-leg VSI in *A-B-C* coordinate

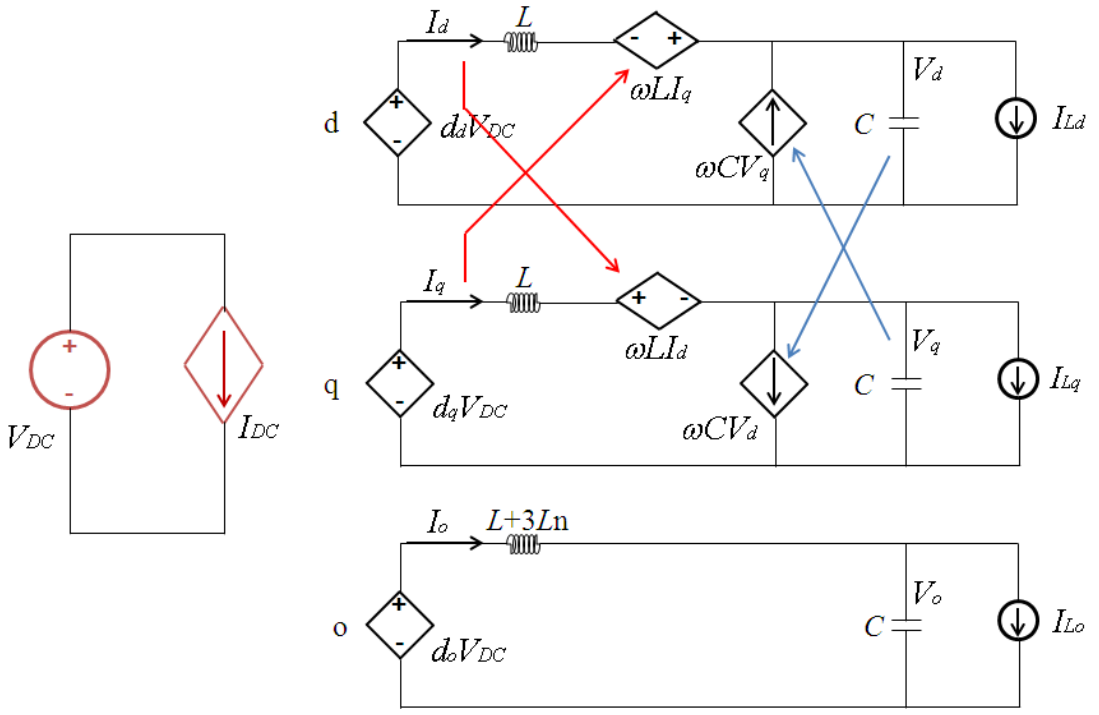



Figure 2.28 Average large signal model of a four-leg VSI in *d-q-o* coordinate

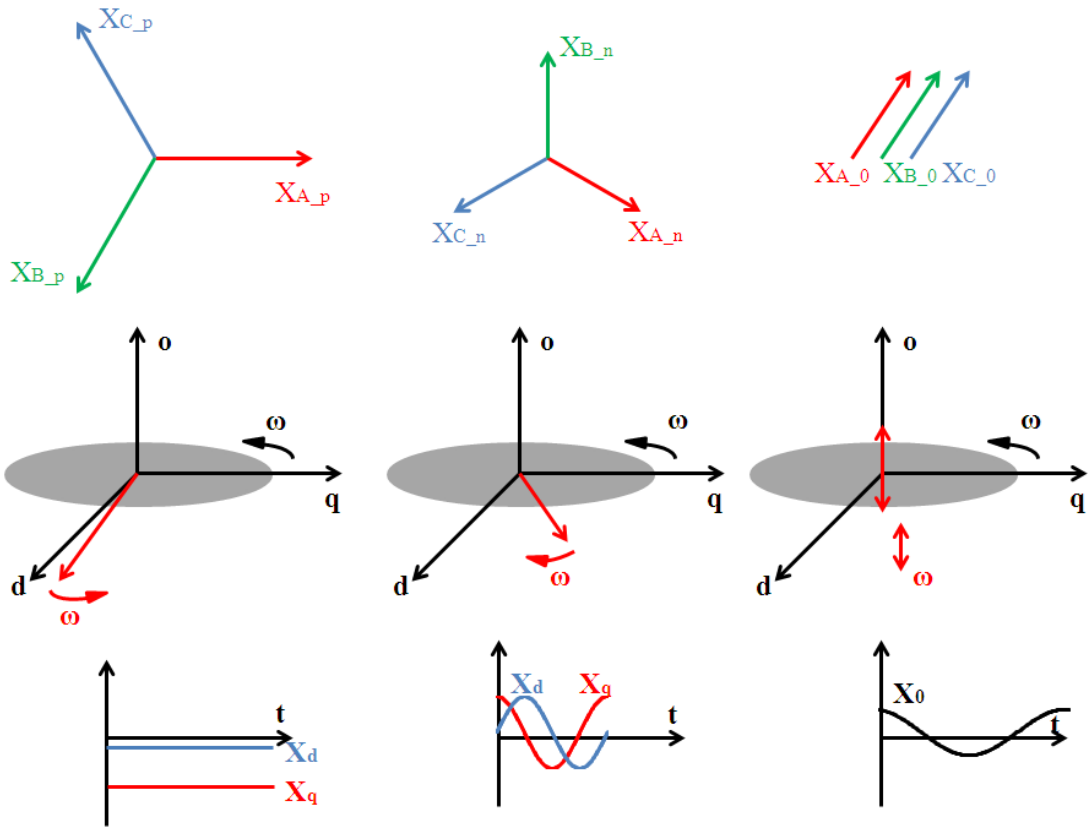



Figure 2.29 Decomposed sequence signals in *d-q-o* coordinate

The unbalanced voltage and current can be decoupled into positive, negative and zero-sequence as explained in the previous section. When it comes to *d-q-o* coordinate, the positive-sequence component shows constant DC values in channel *d* and *q*. The negative-sequence component travels in channel *d* and *q* at a frequency of $2\omega$ since the rotating direction of the sequence is opposite to the positive-sequence. The zero-sequence component circulates in channel o at the fundamental frequency. The decomposed signals in *d-q-o* coordinate are shown in Figure 2.29. Negative and zero-sequence disturbance signals are shown as disturbance signals and the controllers need to be designed fast enough to cope with the disturbances.

It also can be seen in Figure 2.28 that by neglecting the coupled terms in d and q channels, the system model in the *d-q-o* coordinate can be treated as three independent dc-dc buck converters. Therefore, the conventional controller design based on the DC operating point can be done in each channel. The designing process includes the following [19, 65]

- **Transfer function identification of each channel**, three independent control-to-output transfer functions can be obtained based on the model in *d-q-o* coordinate. The transfer functions in [19] are shown in continuous time domain with the consideration of the sampling time delay. Research in recent years show that when it comes to real-time DSP implementation, controller design in discrete time domain match better with the real-time system [66, 67].
- **Delay consideration**, with digital controller, the delay caused by sampling, sensing and computation can be modelled by zero-order hold and delay block. On the bode diagram of the control-to-output transfer function, delay causes the phase plot to drop at the high frequency range [63].
- **Controller design based on light load condition**, since the system could run in load conditions such as single phase loading. A worst scenario, which is light load condition, is considered for the close loop design. The bode diagram shows that there is a peak around the resonant frequency and the phase rolls down sharply below 180°. To ensure the system stability under light load condition, the controller bandwidth has to be designed to be very low[19].
- **Feed forward term if necessary**, the low controller bandwidth ensures the system stability, however, under heavily unbalanced load condition; the controller is not fast enough to compensate the ripples caused by negative and zero components due to the slow dynamic behaviour. Therefore, a current feed-forward term is normally introduced to address the issue[19, 65]

### 2.7.2 Sequence decomposed control based on *d-q-o* coordinate

In order to cope with the poor performance of the conventional controller design during the unbalanced loading, a control strategy based on the sequence decomposition of the unbalanced current/voltage is proposed in [15, 21]. The analyses of the unbalanced load and symmetrical component decomposition have been introduced in the previous sections. An algorithm is implemented before the PI controllers for each channel are designed so that the voltage and current signals are decomposed first.

The key of the decomposed method is to obtain the complex number $\alpha$ and it is shown in Figure 2.30. The complex number $\alpha=e^{j2\pi/3}$ can be developed using Euler's identity as $-1/2+j\sqrt{3}/2$ while $\alpha^2=-1/2-j\sqrt{3}/2$. The complex term $j$ can be thought of as an operator and multiplying a complex number by $j$ leaves the magnitude of the complex number unchanged and phase angle increase by 90°. In practice, it is $-j$ that is used because it

can be obtained by shifting the signal by the time of $T_1/4$, while $T_1$ is the period of the fundamental frequency. The shift is carried out by delaying the original signal by $T_1/4$ [15].

Once the signals are decomposed, the variables in positive-sequence will always show DC values in the *d-q-o* coordinate. The negative-sequence values in the *d-q-o* coordinate can be also shown in terms of DC quantities by rotating the *d-q-o* coordinate in the opposite direction and the transformation is obtained

$$\begin{bmatrix} X_{d-} \\ X_{q-} \\ X_{o-} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ \sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} \tag{2.38}$$

The zero-sequence component signals are in phase with the same amplitude. Therefore it is possible to apply a spatial rotation of -120° and -240° to the zero-sequence phases B and C [15] and the transformation matrix yields Eq. (2.39). Thus in a positive rotating reference frame, the DC operating point values can be obtained.

$$\begin{bmatrix} X_{A\_0} \\ X_{B\_0} \\ X_{C\_0} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha^2 & \alpha^2 \\ \alpha & \alpha & \alpha \end{bmatrix} \begin{bmatrix} X_A \\ X_B \\ X_C \end{bmatrix} \tag{2.39}$$

Therefore the DC operating point for each channel can be obtained without any disturbance. After the output of the controllers, sequence composition sum up all the sequence components and these are the input voltage reference signals $V_{af}$, $V_{bf}$ and $V_{cf}$ to the 3-D SVM. The block diagram of the control strategy is shown in Figure 2.31. Similar control structure was presented in [68].

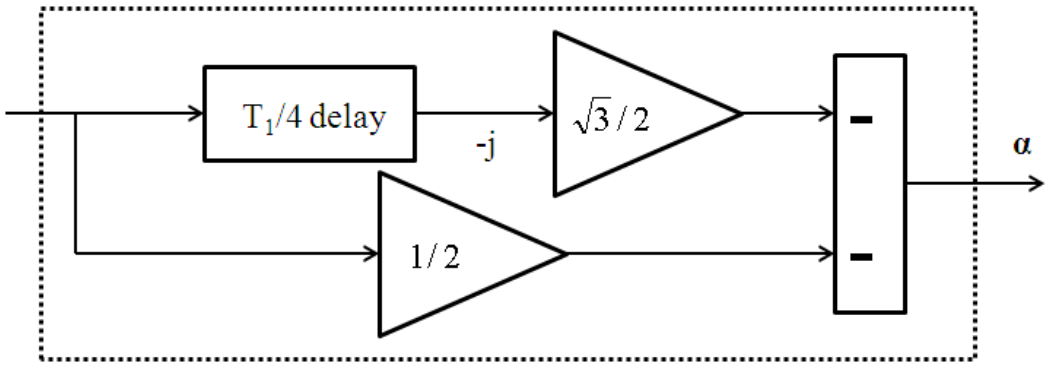



Figure 2.30 Block diagram of obtaining the complex number $\alpha$

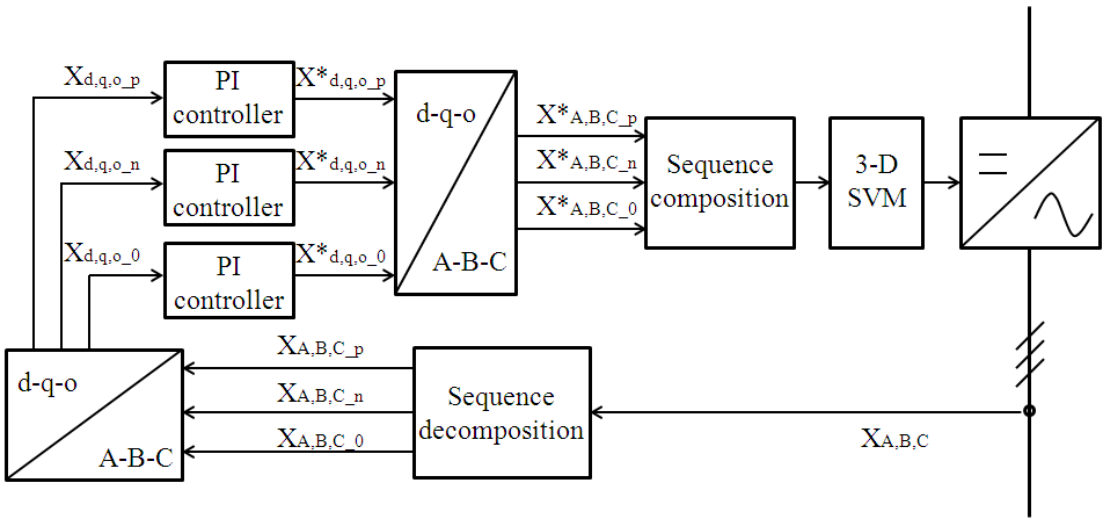



Figure 2.31 Block diagram of the sequence decomposed control strategy

The drawback of this strategy is that by shifting the signal by $T_1/4$, it introduces a delay, which is a quarter of a power cycle into the system, meaning the controller cannot respond to any changes in the system immediately due to a quarter of a cycle delay. Therefore the dynamic response of the controller has been affected, especially under light load condition.

### 2.7.3 Independent per-phase control

Independent per-phase control, also known as natural reference frame control, is introduced for a four-leg VSI in [52]. The authors stated that due to the unbalance and nonlinearity in the system, the best strategy is to use the actual AC voltage and current for controller design.

When it comes to natural reference frame, or stationary reference frame, PI controller struggles to remove the steady state error since the reference signals are sinusoidal waveforms[7]. In the cases of single-phase PV system application, a single-phase equivalent synchronous reference frame controller was introduced in [69, 70] and the block diagram is shown in Figure 2.32. According to spectrum analysis theory, after multiplying the reference sine and cosine waveforms, the harmonic content of the error signal at that reference frequency will be shifted to dc and double-frequency[69]. After the low-pass filter effect of the PI controller[66], only dc quantities are remained for the controller to deal with, hence the integral part of the controller will force the error amplitude to zero. The frequency of the reference sine and cosine waveforms are often obtained by using a grid synchronized phase-locked loop (PLL).

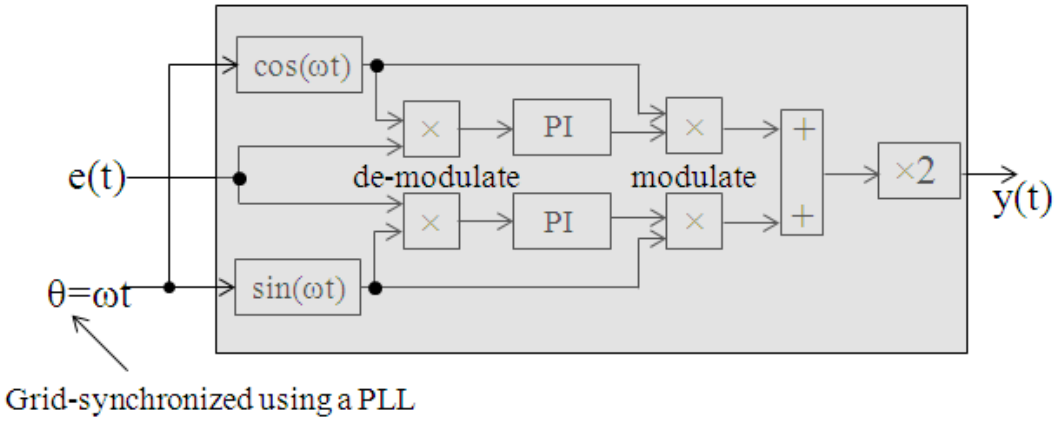



Figure 2.32 Block diagram of single-phase equivalent synchronous frame controller

Instead of using an equivalent synchronous frame controller, which is indirect and the control strategy includes both de-modulation and modulation block, a proportional resonant (PR) controller is introduced in [7, 69, 70]. The derived generalized PR controller is given by

$$H_{AC}(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{2.40}$$

where $K_p$ is the proportional gain term, $K_i$ is the integral gain term at the reference frequency ω and $\omega_c$ represents the cut-off frequency.

Because of the high integral gain at the reference frequency, an overall zero steady-state error can be obtained. Also, selective harmonic compensation can be achieved by adding PR controllers at the selected harmonics frequency[7]. PR controller can be used in either *α-β* coordinate or *A-B-C* coordinate. Details of digital implementation of the controller are fully presented in [70].

The idea of using PR controllers for a four-leg voltage source inverter was first seen in [14] and the control scheme was called scalar resonant-filter-bank-based output-voltage control. This control scheme is suitable for per-phase control and therefore it is implemented with a scalar implementation of the PWM switching scheme. The advantage of implementing this type of controller in a system includes simplicity and ease of implementation.

## 2.8 EMI in power converters

The fast switching actions of the power converter generate considerable electromagnetic interference (EMI) noise [71]. For a four-leg VSI application, the bus bar is normally

floating with reference to the ground[24]. With fast switching of the power electronic devices, the common-mode voltage (CMV) has become a big EMI source [1, 34, 72]. The parasitic capacitances between the DC link, packages, heat sinks and ground are significant, therefore cannot be neglected when designing the four-leg VSI system[24]. In [71], a metric for evaluating the EMI spectra of power converters has been introduced. The techniques of dealing with EMI issues include passive or active filtering [27, 73], soft switching[62], CMV mitigated controller[34], CMV reduced switching scheme[72, 74].

Recent years have witnessed intensive research on CMV reduced switching schemes in VSD system because of the fact that it is a good trade-off of cost and effectiveness [26, 39]. The work which focuses on the common-mode voltage noise for a four-leg inverter used in distributed generation was introduced in [24, 72].

## 2.9 Summary

In this chapter, the topology of a three-phase four-leg VSI has been reviewed and compared with other topologies. Typical application for a four-leg inverter includes distributed generated power system and three-phase uninterruptible power supply system where unbalanced loads are prevalent. Switching schemes that are seen for a three-leg inverter are reviewed first before the switching schemes for a four-leg inverter are introduced. Performance analysis tools for a three-leg VSI are also reviewed, these analytical methods serve as useful tools to compare the performance of different switching schemes in terms of THD, current harmonic distortion, switching and conduction loss. Control loop design for a four-leg inverter are normally based on either *d-q-o* coordinate or *A-B-C* coordinate, and often related to certain switching schemes. The EMI issues, which are associated with the common-mode voltage noise, are reviewed at the end of the chapter.

# Chapter 3
# Near-State 3-D SVM for Three-phase Four-Leg Inverters

This chapter introduces a modified 3-D SVM switching scheme which is called a near-state 3-D SVM (NS 3-D SVM) for three-phase four-leg VSIs. The impact of 3-D SVM scheme on grounding and common-mode noise issues has rarely been fully investigated before. This chapter firstly investigates the common-mode noise issues for a three-phase four-leg VSI, thus presenting a NS 3-D SVM which reduces the common-mode voltage (CMV) of a four-leg inverter. The proposed switching scheme reduces the CMV level of the inverter to be $V_{DC}/4$ while maintaining the merit of conventional 3-D SVM. The technique of implementation of the proposed switching scheme in a real-time DSP system is also introduced. Calculations of the duty ratios are given and the simulation and experimental results validate the effectiveness of the NS 3-D SVM. Frequency spectrum analysis based on NS 3-D SVM and conventional 3-D SVM have been carried out and compared. The experimental results also demonstrate that the proposed switching scheme can work both under balanced and unbalanced load conditions.

## 3.1 Common-mode noise and EMI issue

Common-mode noise is a type of EMI noise induced on signals with respect to a reference ground, it is a source of coupling noise by conduction or radiation[1]. The electrical equipments are susceptible to the magnitude, frequency and repetition rate of the common-mode noise. Common-mode noise is sometimes called common-mode voltage noise, implying that common-mode voltage characteristics are strongly linked with common-mode voltage noise. The EMI issue of power converters and how it is related to CMV has been reviewed in Chapter 2. In this section, the impact of CMV on a four-leg inverter is studied and presented.

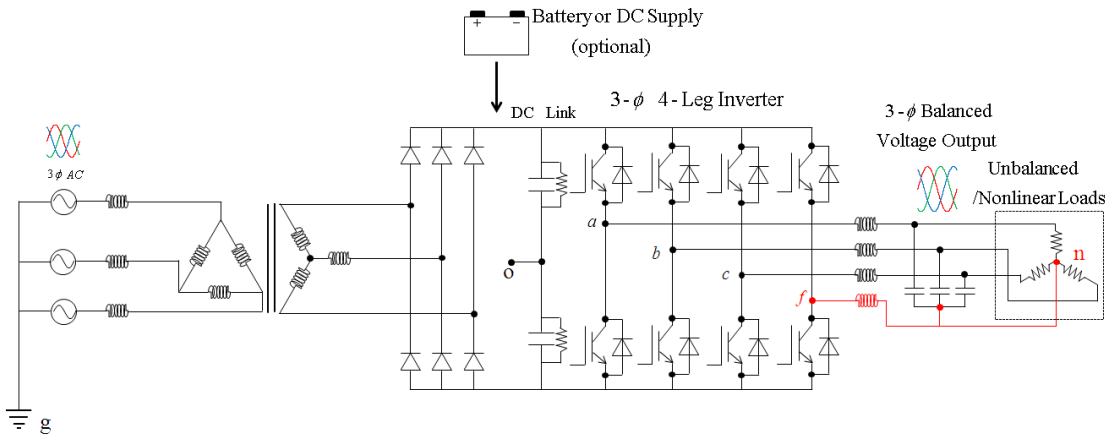



Figure 3.1A three-phase four-leg VSI power system

To start with, a definition of the common-mode voltage for a three-phase four-leg voltage source inverter must be given. Similar to a three-phase three-leg inverter, the common-mode voltage is defined as the potential difference between the star point of the loads and the power line ground ($V_{ng}$ shown in Figure 3.1). With $V_{ng}=V_{no}+V_{og}$ and $V_{og}$ being much smaller and slowly varying signal compared to $V_{no}$, the term of $V_{og}$ can be neglected [39]. Thus the CMV of a four-leg inverter is the potential of the star point with respect to the midpoint of the DC link capacitors ($V_{no}$ in Figure 3.1).

By the definition given above and neglecting the voltage drop across the neutral inductor, the CMV of a four leg inverter is

$$V_{no} = \frac{V_{ao} + V_{bo} + V_{co} + V_{fo}}{4} \tag{3.1}$$

where $V_{ao/bo/co/fo}$ are the phase-to-neutral voltage and $V_{no}$ is the CMV.

Depending on the switching states of the VSI, $V_{ao}$, $V_{bo}$, $V_{co}$ and $V_{fo}$ have $\pm V_{DC}/2$ voltage levels. Therefore for a four-leg VSI, the existing voltage levels of the common-mode voltage will show $\pm V_{DC}/2$, $\pm V_{DC}/4$ and 0 depending on the 16 switching states of the inverter. The details of the CMV according to different switching states are shown in Table 3-1.

During the transient between the switching states, the CMV changes by $\pm V_{DC}/4$. The switching schemes for the four-leg inverter, either 3-D SVM or carrier-based PWM, exhibit high CMV characteristics that pose problems in the high power application. With the increasing switching frequency of the modern power electronics and the high

DC link voltage level, excessive common-mode voltage with sharp edges can result in high common-mode current through the parasitic capacitors as shown in Figure 3.2. EMI has always been an issue together with the CMV. The power stage of the high switching inverter itself is a high EMI source while the control units of the system are very EMI sensitive. This is also shown in Figure 3.2.

**Table 3-1Common-mode voltage level with different switching states**

| | pppp | nnnp | pnnp | ppnp | npnp | nppp | nnpp | pnpp |
|---|---|---|---|---|---|---|---|---|
| $V_{ao}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ |
| $V_{bo}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ |
| $V_{co}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ |
| $V_{fo}$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ |
| $V_{no}$ | $V_{DC}/2$ | $-V_{DC}/4$ | 0 | $V_{DC}/4$ | 0 | $V_{DC}/4$ | 0 | $V_{DC}/4$ |
| | pppn | nnnn | pnnn | ppnn | npnn | nppn | nnpn | pnpn |
| $V_{ao}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ |
| $V_{bo}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ |
| $V_{co}$ | $V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ | $V_{DC}/2$ |
| $V_{fo}$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ | $-V_{DC}/2$ |
| $V_{no}$ | $V_{DC}/4$ | $-V_{DC}/2$ | $-V_{DC}/4$ | 0 | $-V_{DC}/4$ | 0 | $-V_{DC}/4$ | 0 |

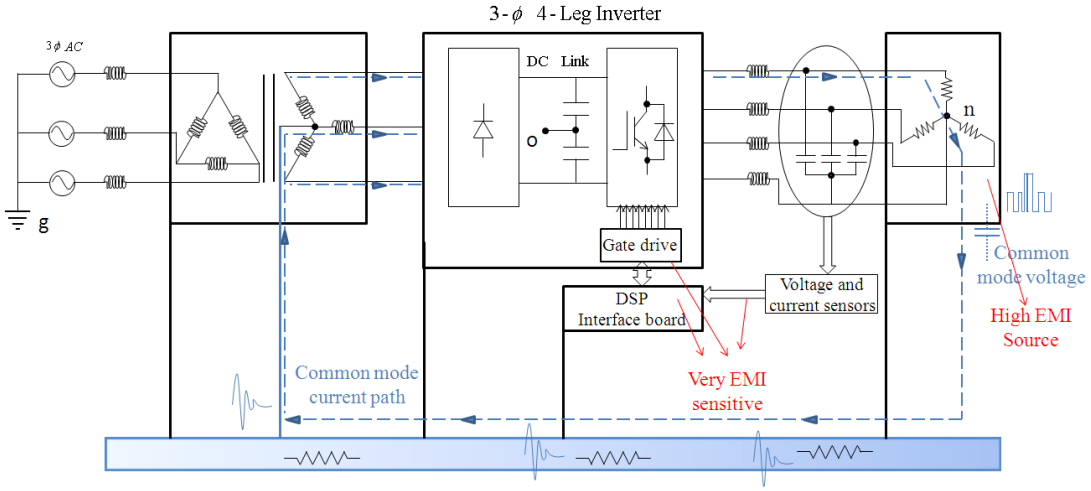



Figure 3.2 Common-mode current path and EMI issues in a four-leg inverter system

The cause of the EMI and the effect of it on the micro controllers and other sensitive semiconductor devices were reviewed in [1]. In some worst cases, EMI leads to nuisance trip of the inverter drive, or interference with other electronic equipment in the vicinity [26, 34, 39]. In Chapter 2, a near-state PWM(NSPWM) is reviewed and the method enjoys the reduced CMV characteristic without sacrificing the output voltage quality and the reduced switching loss[26].

The grounding and common-mode noise issues have rarely been investigated for a four-leg inverter. A four-leg inverter was proposed in [34] to eliminate the common-mode noise, however, this scheme cannot be used in an unbalanced/nonlinear load condition. In [72, 74], only six switching vectors are selected to synthesize the reference switching vector. According to Table 3-1, if the switching states pnnp, npnp, nnpp, ppnn, nppn, pnpn are chosen as shown in Figure 3.3, the CMV will end up with zero. This switching scheme could be named as CMV mitigation switching scheme since it aims to mitigate the common-mode voltage. On the $\alpha$-$\beta$ projection plane, the projection of the chosen vectors forms a hexagon as shown in Figure 3.3.

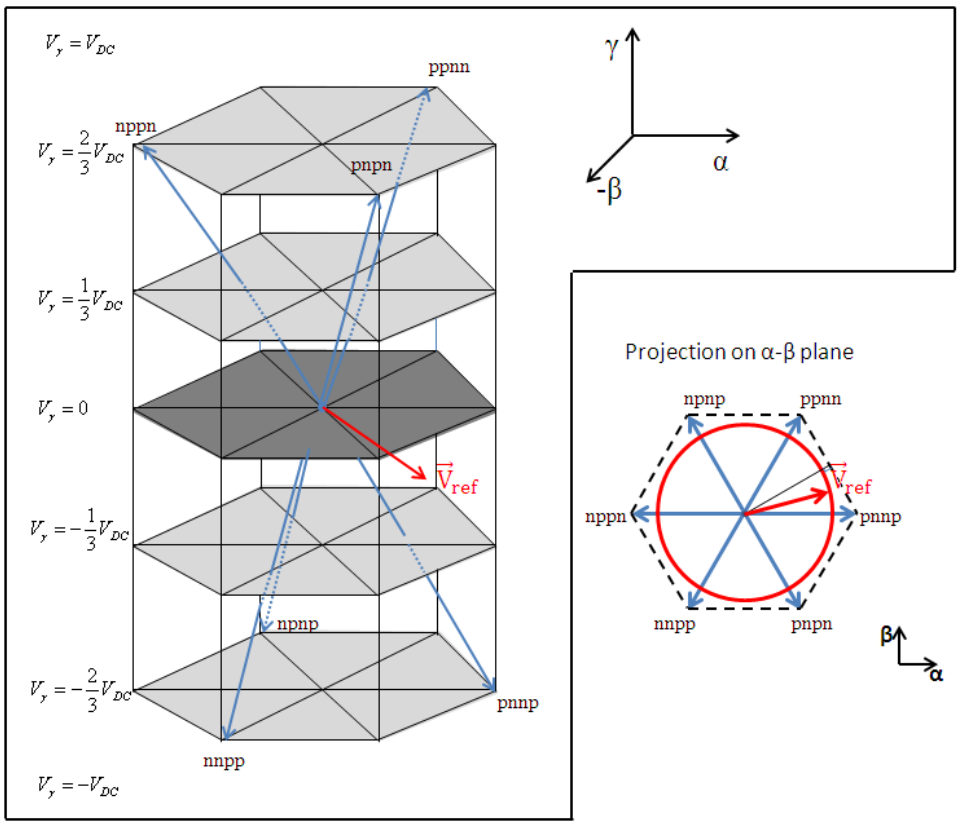



Figure 3.3 Selected six switching states to synthesize the reference switching vector

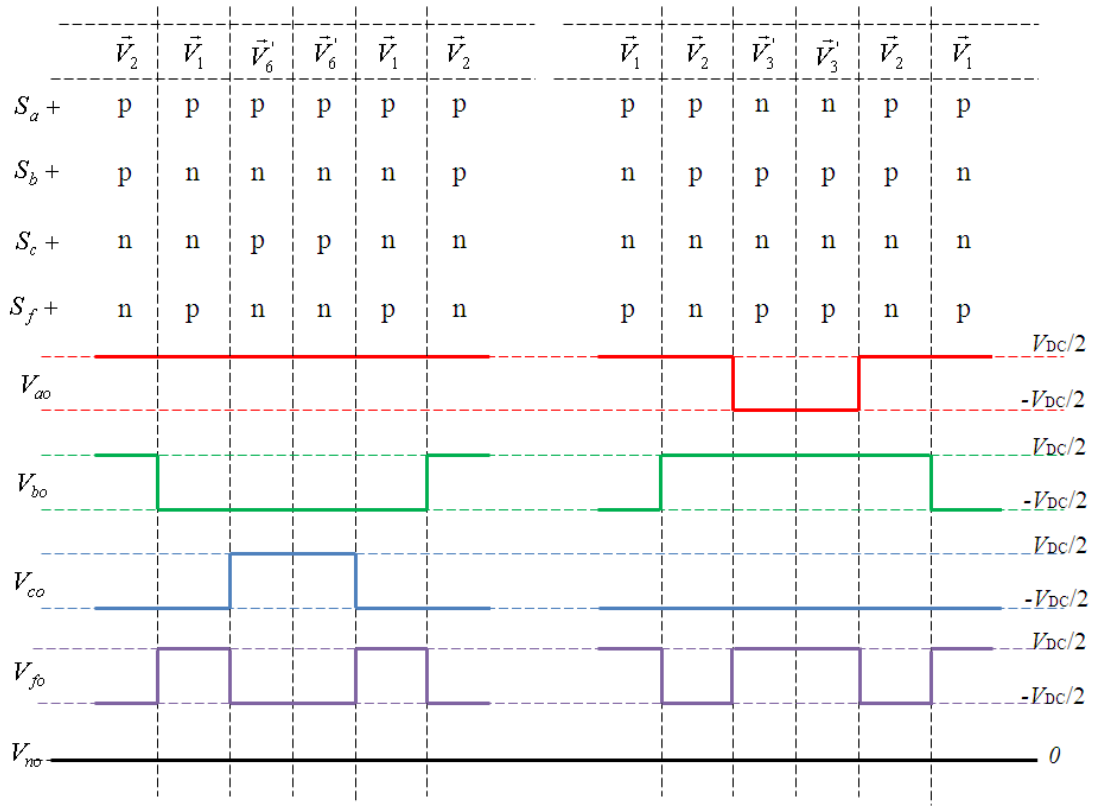



Figure 3.4 Switch pulse pattern and CMV, CMV mitigation switching scheme

The switching patterns of different legs covering [-60°, 60°] on the $\alpha$-$\beta$ plane are shown in Figure 3.4. As it can be seen, although the CMV achieves zero, there're simultaneous switching actions between different phases. This, as it was explained in the literature review, cannot be guaranteed in real-time implementation due to the dead time delay effect and the significant terminal overvoltage, in which case $2V_{DC}$, is created due to the simultaneous switching of different phases, this means the rated insulation will have to be doubled. Therefore, this scheme cannot be utilized in practical drives.

## 3.2 A near-state 3-D SVM

Adopting the method from CMV reduced PWM switching scheme for a three-phase three-leg VSI, a near-state 3-D SVM is presented here. In theory, by avoiding using the two zero switching states pppp and nnnn, the CMV level should be limited to $\pm V_{DC}/4$. Unlike the three-leg inverter which only has 8 switching states, the four-leg VSI has 16 switching states; this makes the selection of the non-zero switching vectors more difficult. Therefore the steps that are required to synthesize the rotating reference vector are different with the conventional 3-D SVM. The theory of the switching vectors in a

3-D $\alpha$-$\beta$-$\gamma$ coordinate has already been introduced in the review work of the 3-D SVM; therefore here the definition of the 3-D space vectors will be skipped.

### 3.2.1 Syntheses of the reference switching vector in $\alpha$-$\beta$-$\gamma$ coordinate

Instead of having prism and tetrahedron identification, unique section identification is required and therefore the selected adjacent switching vectors and the duration of each applied switching vectors are different with those of conventional 3-D SVM. Sequencing of the selected switching vectors follows different rules. Synthesis of the reference vector takes the following steps: (1) section identification; (2) selection of the near-state switching vectors; (3) projection of the reference vector; (4) sequencing of the selected switching vectors. The details are given in the following sections.

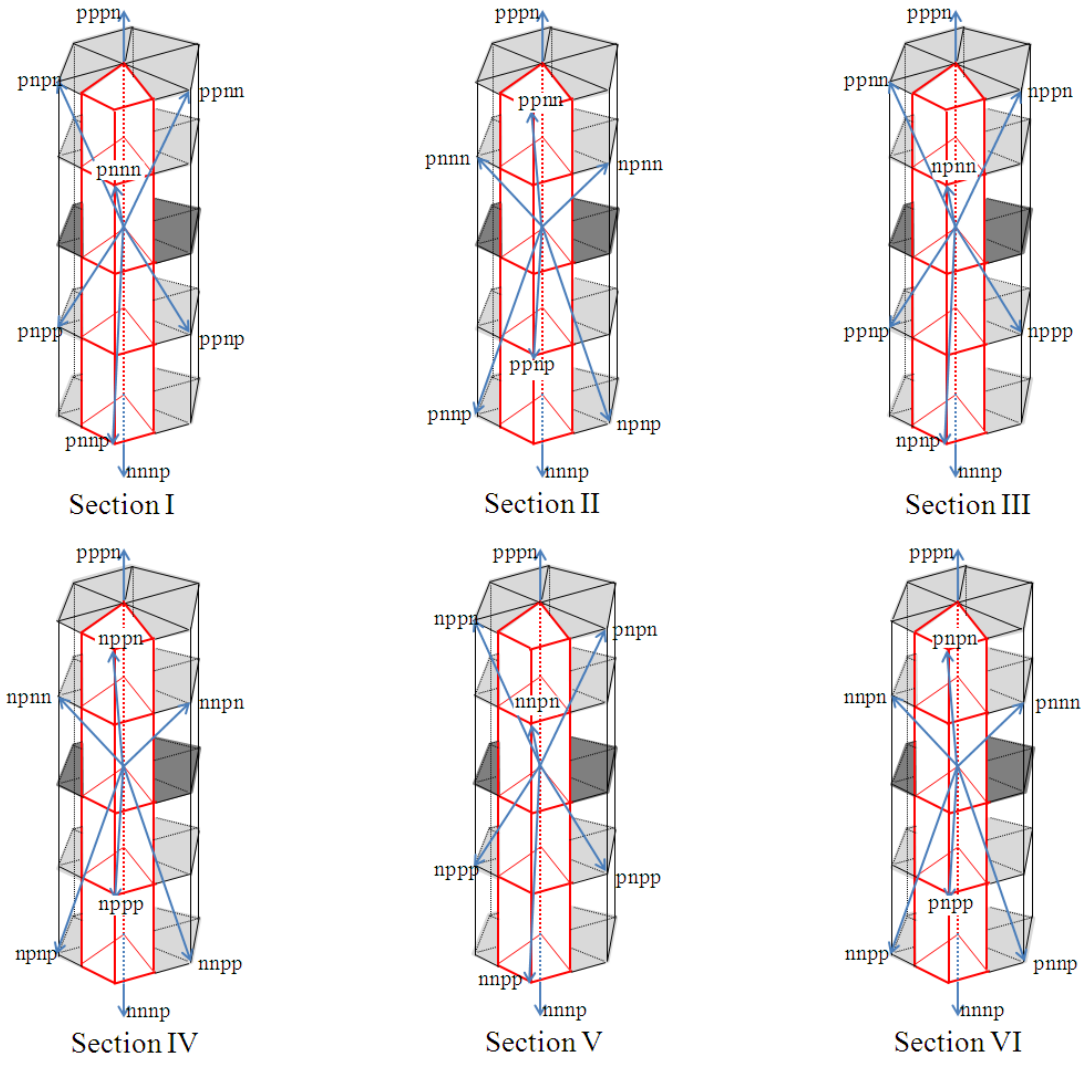



Figure 3.5 Definition of section identification of near state 3-D SVM

### 3.2.1.1 Section Identification

Just as the six prisms defined in the conventional 3-D SVM, six sections can be identified. They are numbered Section I through Section VI, as shown in Figure 3.5. For demonstration purposes, each section rotates by 60° compared to the previous one. Each section consists of half of the two adjacent prisms. For instance, Section I consists half of Prism VI and half of Prism I. Still based on the projection of the reference switching vector on the $\alpha$-$\beta$ coordinate, the projection of Section I lie in Sector $B_1$ which is between 330° and 30° on $\alpha$-$\beta$ plane as shown in Figure 3.6. Therefore, the criteria to determine in which section the reference vector lies relies on the projection of the reference vector in $\alpha$-$\beta$ coordinate.

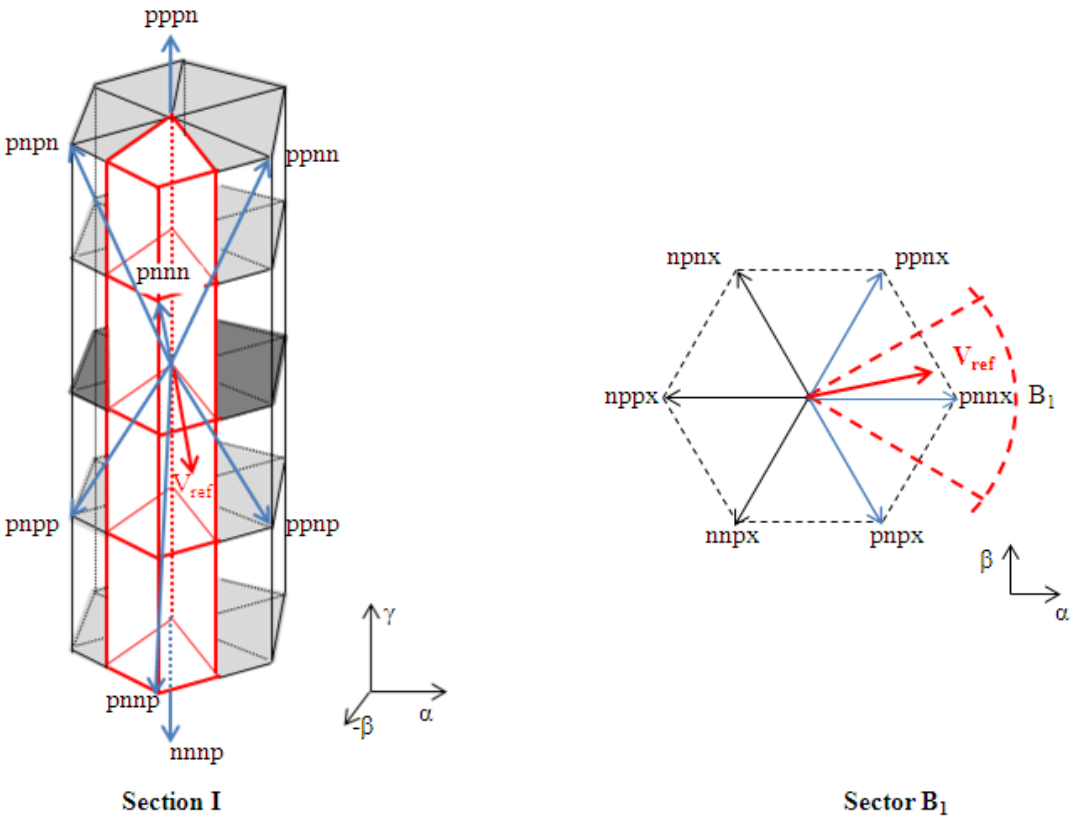



Figure 3.6 Definition of Section I in a 3-D space and its projection

### 3.2.1.2 Selection of the near-state switching vectors

When the reference switching vector is located in Section I, i.e. the projection of the reference vector is within sector $B_1$, four non-zero switching vectors are needed to synthesize the reference vector. In order to minimize the circulating energy, therefore reducing the current ripple and harmonic contents, switching vectors adjacent to the reference vector should be selected [32]. In this case, the adjacent switching vectors are called near-state switching vectors and there're altogether eight switching vectors are adjacent to the reference vector, four of which will be chosen. Selection of the switching vectors must follow the rules that as follows:

- Reduced common-mode voltage level
- Simultaneous switching between the phases must be avoided
- Minimum switching loss
- High DC link utilization
- Work under both balanced and unbalanced load conditions

Based on these rules, only two sets of four switching vectors can be selected to synthesize the reference vector in each section. Figure 3.7 shows the two sets of switching vectors in Section I and Section II. As it can be seen, each set consists of two tetrahedrons that rely in two prisms.

In Section I, for Set A, switching vectors of pnpp, pnnn, pnnp and ppnn are selected while for Set B, switching states of pnpn, pnnn, pnnp and ppnp are selected. It can be seen that the switching states pnnn and pnnp are selected in both cases since these two switching vectors are the closest to the reference vector. One of the two switching states of pnpp and pnpn is selected, and the fourth switching state will then be decided based on the third switching state that has been just selected.

The principle behind the selection is that simultaneous switching actions between phases should be avoided. Here we name the switching vector of pnpx (where x=p or n) as $\vec{V}_1$, the switching vector of pnnx as $\vec{V}_2$ and $\vec{V}_3$ and the switching vector of ppnx as $\vec{V}_4$. Hence the duration times of the applied switching vectors are named as $d_1$, $d_2$, $d_3$ and $d_4$. Therefore the reference switching vector can be represented as

$$\vec{V}_{ref} = d_1\vec{V}_1 + d_2\vec{V}_2 + d_3\vec{V}_3 + d_4\vec{V}_4 \tag{3.2}$$

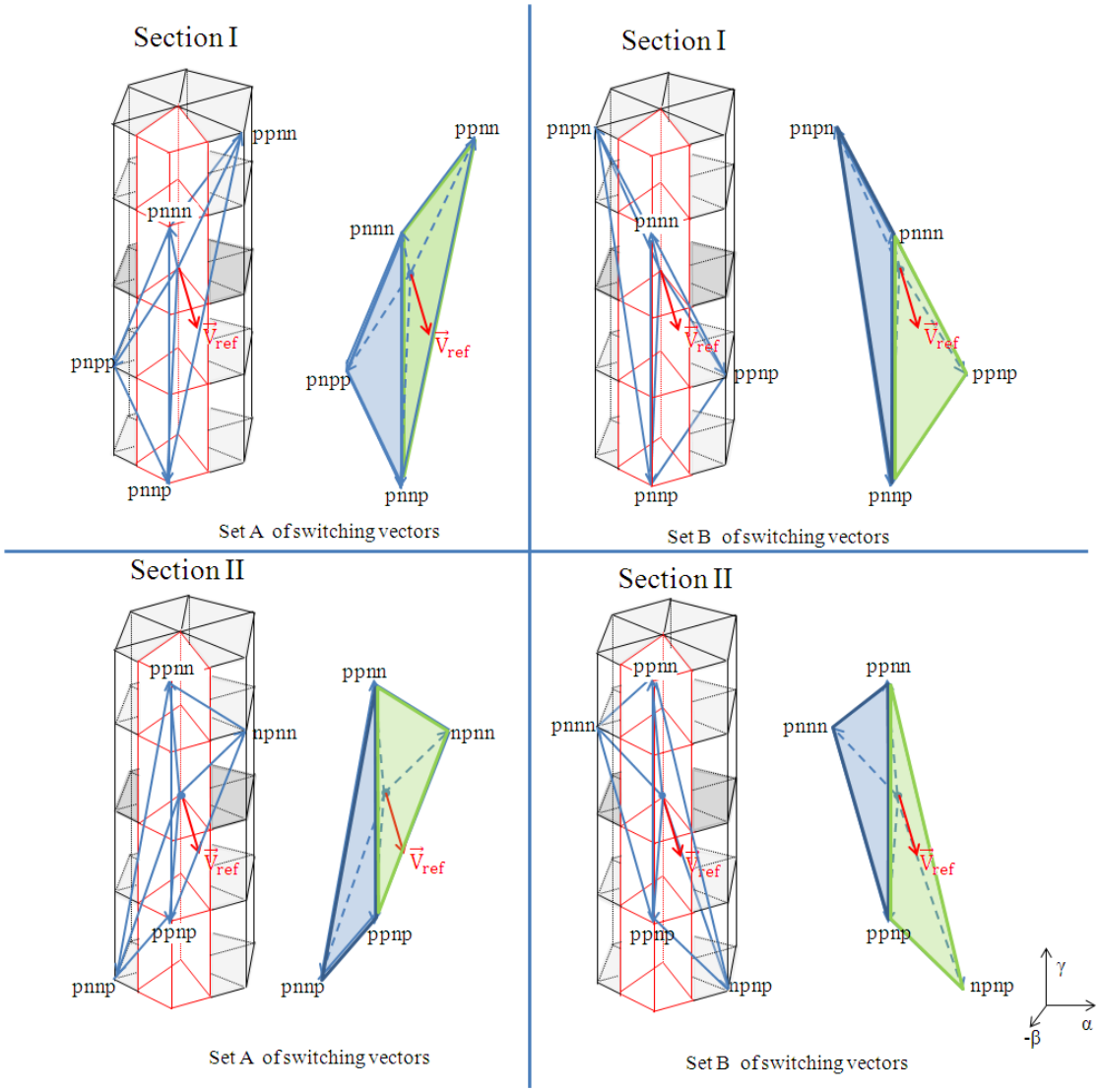



Figure 3.7 Selection of the adjacent switching vectors in Section I and Section II, Set A and Set B

When sequencing these two sets in Section I, it is interesting to find that the switching patterns for the first three phases are exactly the same while for the fourth leg, the switching patterns show opposite polarity as it can be seen in Figure 3.8. The effect of both sets therefore is the same. So for each section, one set of switching vectors will be used to synthesize the reference switching vector. The choice of sets in each section will lead to different levels of harmonic content and ripple in the output voltage and will be discussed later. It is also noted in Figure 3.8 that one of the phases is not switched during one PWM cycle, which indicates a third of the switching loss has been saved. There is no simultaneous switching action between the phases. Also it is shown clearly in Figure 3.8 that the CMV level has been reduced to $\pm V_{DC}/4$ as expected. In comparison, Figure 3.9 shows the CMV level of the conventional 3-D SVM. For demonstration purposes, Tetrahedron 2 in Prism VI and Tetrahedron 1 in Prism I are

used to synthesize the reference vector, since the projection of the reference vector in $\alpha$-$\beta$ coordinate covers the range of [-30° 30°]. It can be seen clearly that the $\pm V_{DC}/2$ level have been eliminated in the proposed switching scheme compared to the conventional 3-D SVM.

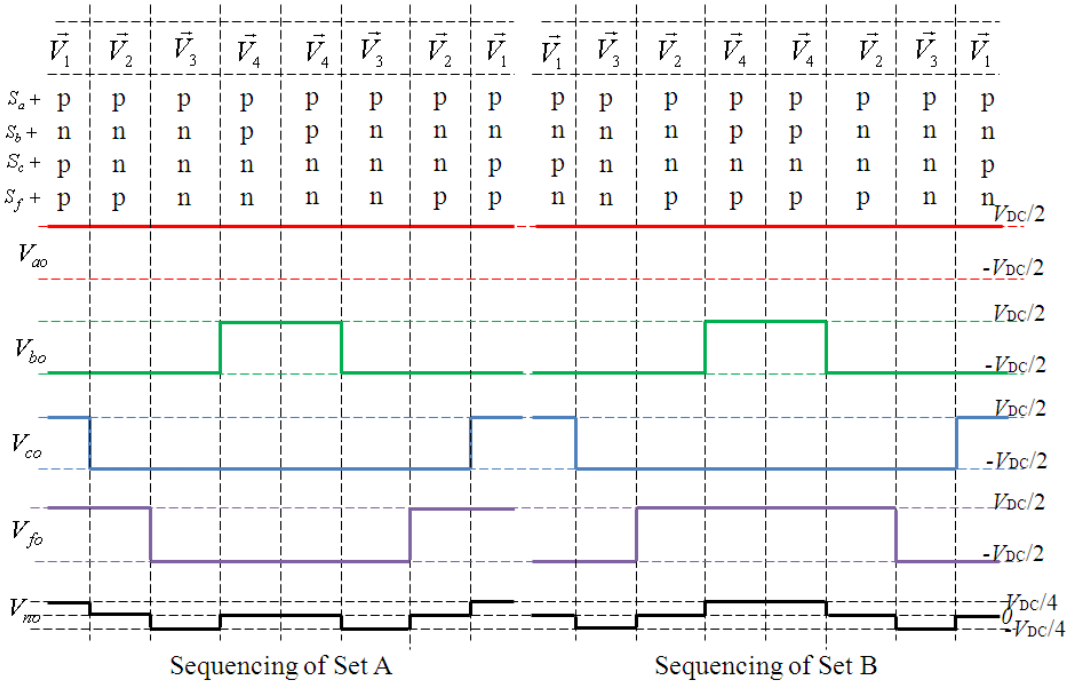



Figure 3.8 Switch pulse pattern and CMV, near state 3-D SVM

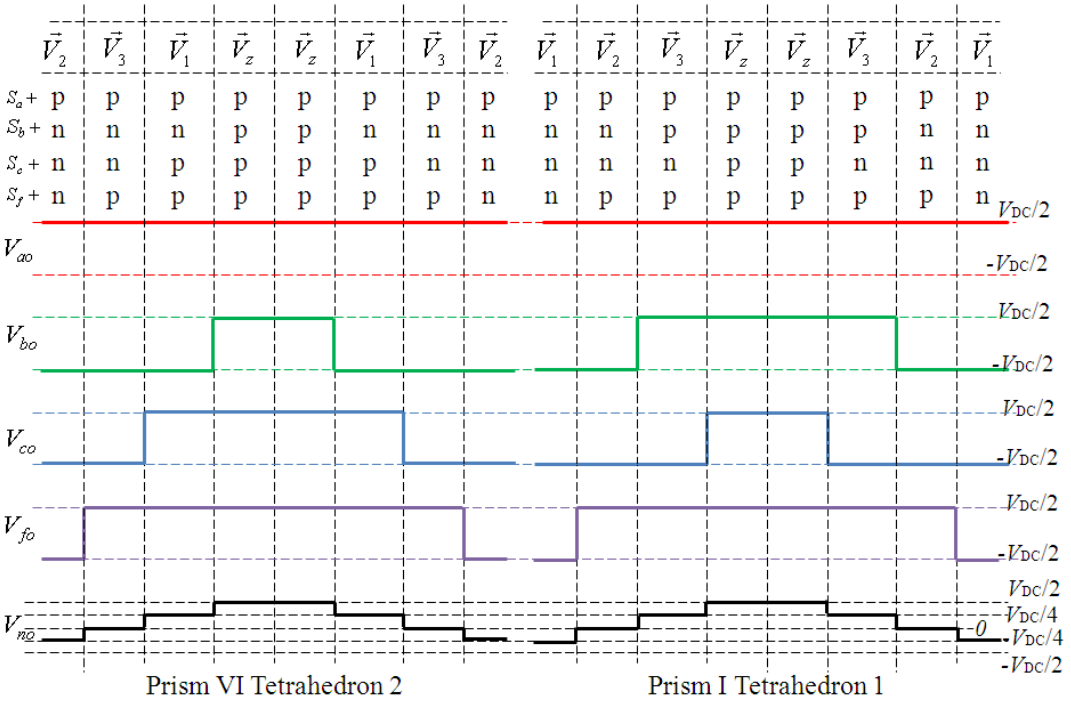



Figure 3.9 Switch pulse pattern and CMV, conventional 3-D SVM

There are four schemes in terms of set selection in each section and they are shown in Table 3-2. As explained before, in effect, Scheme 1 and 2 belong to the same class since they choose either Set A or B to sequence the selected switching vectors, hence they have the same output voltage waveform while Scheme 3and Scheme 4 chose Set A and B alternatively, so they have different output features compared to Scheme 1 and 2(see Figure 3.10). It has been found that the harmonic content and the voltage ripple of the output voltage of Scheme 1 or 2 are higher than that of Scheme 3 or 4 as it can be seen in the FFT analysis (Figure 3.11) based on the output voltages of both schemes. Therefore, Scheme 3 is selected in the real-time implementation as shown in Figure 3.12.

**Table 3-2 Set Selection Table**

| Section / Set selection | I | II | III | IV | V | VI |
|---|---|---|---|---|---|---|
| Scheme 1 | Set A | Set A | Set A | Set A | Set A | Set A |
| Scheme 2 | Set B | Set B | Set B | Set B | Set B | Set B |
| Scheme 3 | Set A | Set B | Set A | Set B | Set A | Set B |
| Scheme 4 | Set B | Set A | Set B | Set A | Set B | Set A |

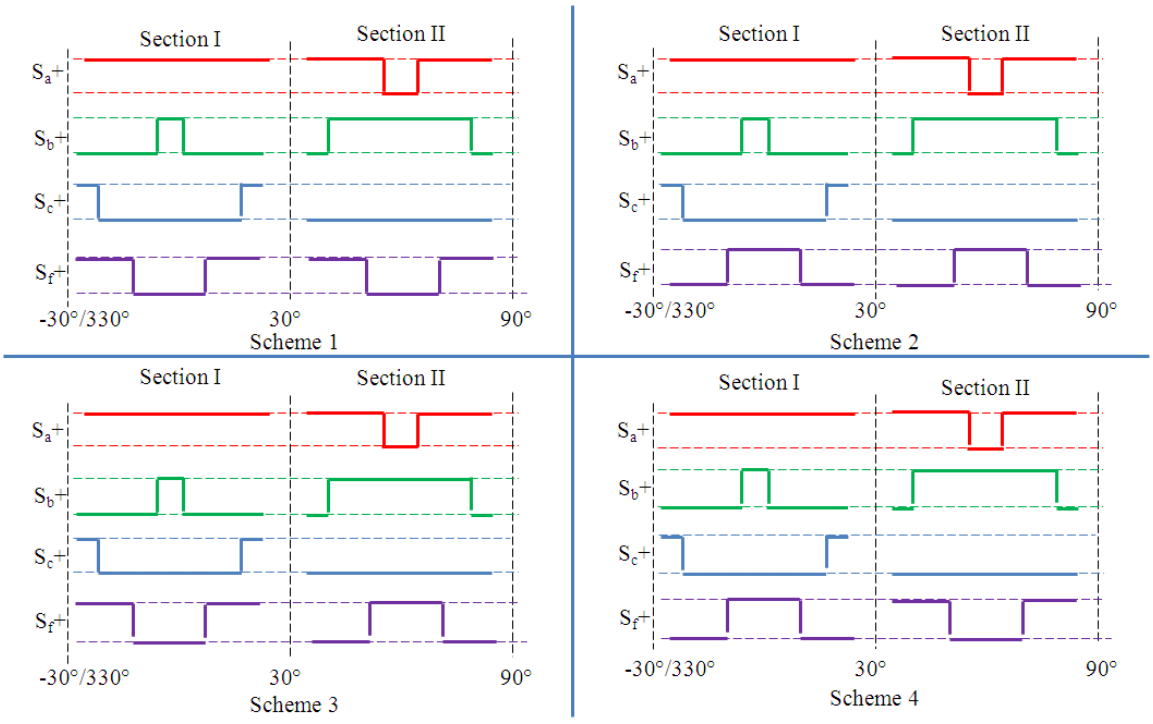



Figure 3.10 Switching patterns for different schemes, Section I and II are chosen for demonstration purposes

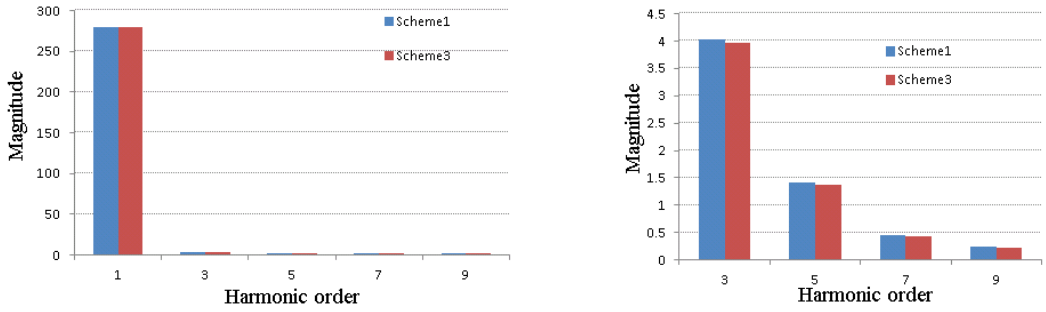



Figure 3.11 Comparison of harmonic contents based on the output voltages of Schem1 and 3; (a) FFT comparison between Scheme 1and 3; (b) zoomed in version showing harmonic contents at 3rd-9th

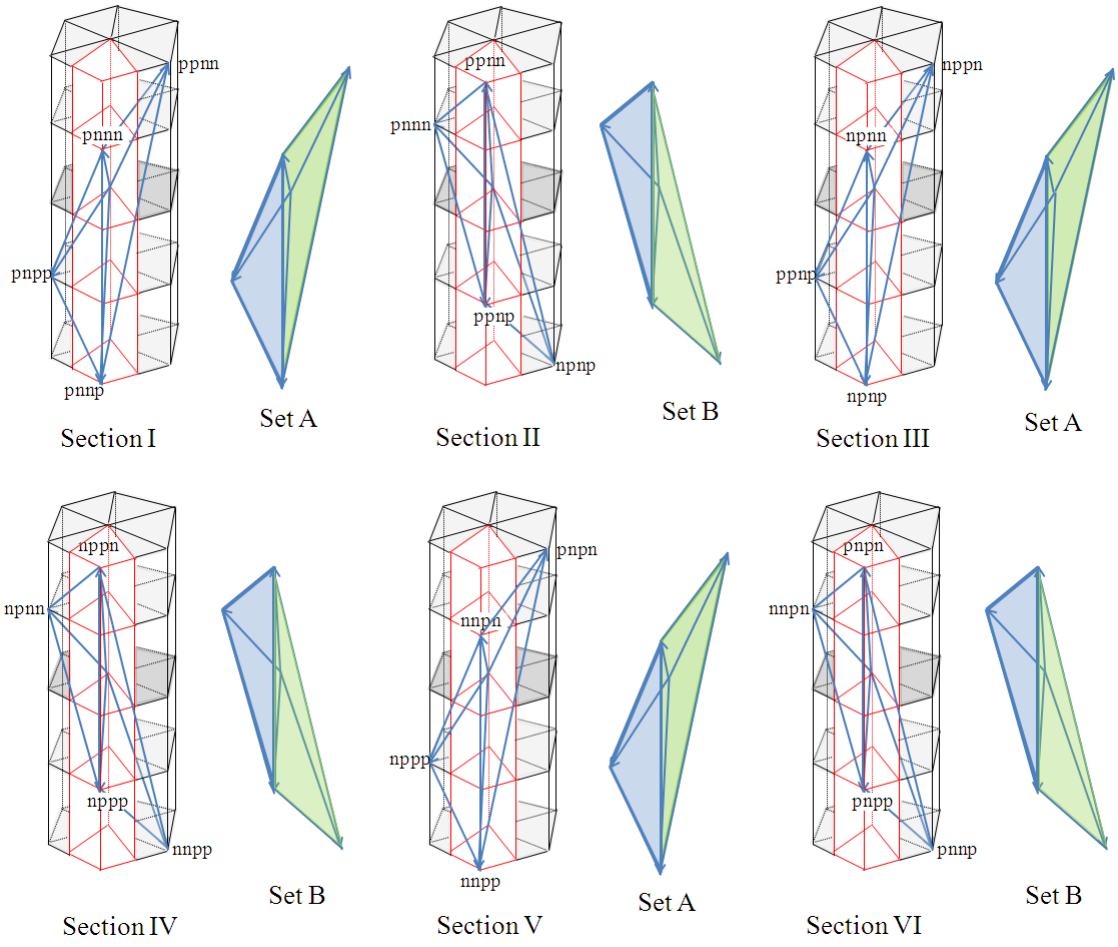



Figure 3.12 Scheme 3 is chosen to be implemented for the proposed switching scheme

### 3.2.1.3 Projection of the reference vector

The duration of each applied switching vector can be computed by projecting the reference rotating vector onto the switching vectors, which is similar to the conventional 3-D SVM. The difference in this case is that instead of utilizing the zero switching

vectors ($\vec{V}_Z$= pppp or nnnn or both), four non-zero switching vectors are utilized; therefore a 4×4 matrix is given as below (Assuming the reference vector lies in Set A of Section I) :

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 & 0 \\ \frac{5}{2} & -\frac{\sqrt{3}}{2} & 1 & -1 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \\ V_{DC} \end{bmatrix} \tag{3.3}$$

The details of calculating the 4×4 matrix can be seen in Appendix A. When the reference vector is located in other sets of other sections, the only thing that needs to be changed is the matrix in Eq. (3.3).

The corresponding near-state switching vectors for all the sets in different sections are shown in Table 3-3. Table 3-4 shows the matrices needed to compute the duty ratios.

#### 3.2.1.4 Sequencing of the selected switching vectors

The conventional 3-D SVM has many sequencing schemes with the option of choosing either one or two ZSVs. Unlike the conventional 3-D SVM, the sequencing of the near state 3-D SVM is straight forward with the constraints of minimum switching actions, no simultaneous switching actions between the phases, and reduced CMV. The symmetrical aligned scheme is chosen for the reason that it has less harmonic distortion compared with falling-edge or rising edge scheme [27, 32].Therefore there is only one sequence in terms of sequencing of the selected switching vectors, and it is $\vec{V}_1$-$\vec{V}_2$-$\vec{V}_3$-$\vec{V}_4$-$\vec{V}_3$-$\vec{V}_2$-$\vec{V}_1$. The switching states related to the switching vectors are shown in Table 3-4.

### 3.2.2 Linear operational range of near-state 3-D SVM

As with the NSPWM method for a three-phase three-leg VSI, the proposed near-state 3-D SVM has its linear operational range, according to the matrices shown in Table 3-4, it has been found that when $Mi$ <0.666, $d_2$ and $d_3$ both become negative, resulting even higher CMV level. Therefore the linear operational range of the proposed NS 3-D SVM is within [0.666 1]. In variable speed drives which must maintain a constant ratio of

voltage to frequency, it is therefore important that the PWM scheme can operate over its full modulation range of 0pu to 1pu. In distributed power generation applications however, the inverter frequency is always at line frequency and hence the output voltage range is restricted. Hence the modulation range of 0.666pu to 1pu does not present a problem in this application.

**Table 3-3 Corresponding switching vectors for near-state 3-D SVM**

| Section | I | | II | |
|---|---|---|---|---|
| Set | A | B | A | B |
| Set of switching vectors | $\vec{V}_1$:pnpp<br>$\vec{V}_2$:pnnp<br>$\vec{V}_3$:pnnn<br>$\vec{V}_4$:ppnn | $\vec{V}_1$:pnpn<br>$\vec{V}_2$:pnnn<br>$\vec{V}_3$:pnnp<br>$\vec{V}_4$:ppnp | $\vec{V}_1$:pnnp<br>$\vec{V}_2$:ppnp<br>$\vec{V}_3$:ppnn<br>$\vec{V}_4$:npnn | $\vec{V}_1$:pnnn<br>$\vec{V}_2$:ppnn<br>$\vec{V}_3$:ppnp<br>$\vec{V}_4$:npnp |
| Section | III | | IV | |
| Set | A | B | A | B |
| Set of switching vectors | $\vec{V}_1$:ppnp<br>$\vec{V}_2$:npnp<br>$\vec{V}_3$:npnn<br>$\vec{V}_4$:nppn | $\vec{V}_1$:ppnn<br>$\vec{V}_2$:npnn<br>$\vec{V}_3$:npnp<br>$\vec{V}_4$:nppp | $\vec{V}_1$:npnp<br>$\vec{V}_2$:nppp<br>$\vec{V}_3$:nppn<br>$\vec{V}_4$:nnpn | $\vec{V}_1$:npnn<br>$\vec{V}_2$:nppn<br>$\vec{V}_3$:nppp<br>$\vec{V}_4$:nnpp |
| Section | V | | VI | |
| Set | A | B | A | B |
| Set of switching vectors | $\vec{V}_1$:nppp<br>$\vec{V}_2$:nnpp<br>$\vec{V}_3$:nnpn<br>$\vec{V}_4$:pnpn | $\vec{V}_1$:nppn<br>$\vec{V}_2$:nnpn<br>$\vec{V}_3$:nnpp<br>$\vec{V}_4$:pnpp | $\vec{V}_1$:nnpp<br>$\vec{V}_2$:pnpp<br>$\vec{V}_3$:pnpn<br>$\vec{V}_4$:pnnn | $\vec{V}_1$:nnpn<br>$\vec{V}_2$:pnpn<br>$\vec{V}_3$:pnpp<br>$\vec{V}_4$:pnnp |

**Table 3-4 Matrix for switching vector duty ratio computation**

| Section | I | | II |
|---|---|---|---|
| Set | A | B | A |
| Matrix of duration of each switching vector | $\begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 & 0 \\ \frac{5}{2} & -\frac{\sqrt{3}}{2} & 1 & -1 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ \frac{5}{2} & \frac{\sqrt{3}}{2} & 1 & -1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 & 0 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} 0 & -\sqrt{3} & 0 & 1 \\ \frac{1}{2} & \frac{3\sqrt{3}}{2} & -1 & -1 \\ 1 & 0 & 1 & 0 \\ -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ |
| Section | II | III | |
| Set | B | A | B |
| Matrix of duration of each switching vector | $\begin{bmatrix} 0 & -\sqrt{3} & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 & 0 \\ 2 & \sqrt{3} & -1 & -1 \\ -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ -1 & 0 & -1 & 0 \\ -\frac{1}{2} & \frac{3\sqrt{3}}{2} & 1 & -1 \\ 0 & -\sqrt{3} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ -2 & \sqrt{3} & 1 & -1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 & 0 \\ 0 & -\sqrt{3} & 0 & 1 \end{bmatrix}$ |
| Section | IV | | V |
| Set | A | B | A |
| Matrix of duration of each switching vector | $\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \\ -\frac{5}{2} & -\frac{\sqrt{3}}{2} & -1 & -1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 & 0 \\ \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 & 0 \\ -\frac{5}{2} & \frac{\sqrt{3}}{2} & -1 & -1 \\ \frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} 0 & \sqrt{3} & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 & 0 \\ -2 & -\sqrt{3} & 1 & -1 \\ \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ |
| Section | V | VI | |
| Set | B | A | B |
| Matrix of duration of each switching vector | $\begin{bmatrix} 0 & \sqrt{3} & 0 & 1 \\ -\frac{1}{2} & -\frac{3\sqrt{3}}{2} & 1 & -1 \\ -1 & 0 & -1 & 0 \\ \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \\ 2 & -\sqrt{3} & -1 & -1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 & 0 \\ 0 & \sqrt{3} & 0 & 1 \end{bmatrix}$ | $\begin{bmatrix} -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \\ 1 & 0 & 1 & 0 \\ \frac{1}{2} & -\frac{3\sqrt{3}}{2} & -1 & -1 \\ 0 & \sqrt{3} & 0 & 1 \end{bmatrix}$ |

### 3.2.3 Duty ratios over one power cycle

A balanced linear load is used to show the duty ratio waveforms of each phase. In order to obtain a balanced three-phase output voltage, a rotating reference vector on the $\alpha$-$\beta$ coordinate has to be supplied. The following reference voltages represent the reference switching vector

$$\begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} = \frac{Mi}{\sqrt{3}} V_{DC} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \\ 0 \end{bmatrix} \tag{3.4}$$

The duty ratio waveform of the near-state 3-D SVM is then plotted in Matlab. It should be noted that the waveforms that are drawn in Figure 3.13 indicates that only one carrier waveform is utilized, which is the same case as real-time implementation. For demonstration purposes, it is easier and clearer to understand the duty ratio waveform if two carrier waveforms are utilized. Therefore the equivalent duty ratio waveform, which is plotted by using two carrier waveforms, is shown in Figure 3.14. Thus it is clear to see that the proposed switching scheme has inherited the merits of the conventional 3-D SVM such as higher DC link utilization, lower switching loss, and working under unbalanced load condition. However, the actual switching patterns of near-state 3-D SVM and conventional 3-D SVM are very different, and thus, the PWM ripple behaviour, output voltage quality, conduction loss, harmonic contents, etc are different. These will be analyzed and discussed in the following chapter.

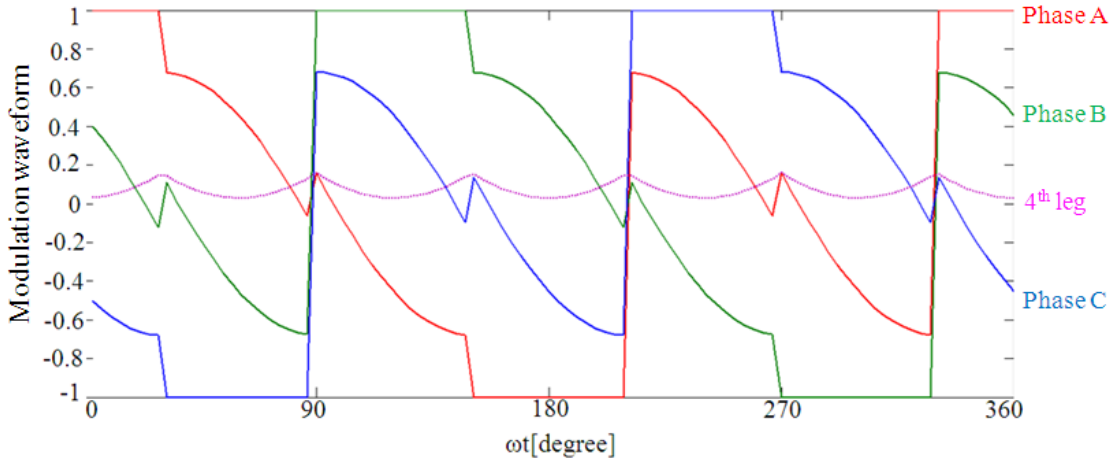



Figure 3.13 Simulated duty ratio waveform of the proposed near-state 3-D SVM with one carrier wave utilized (*Mi*=0.84)

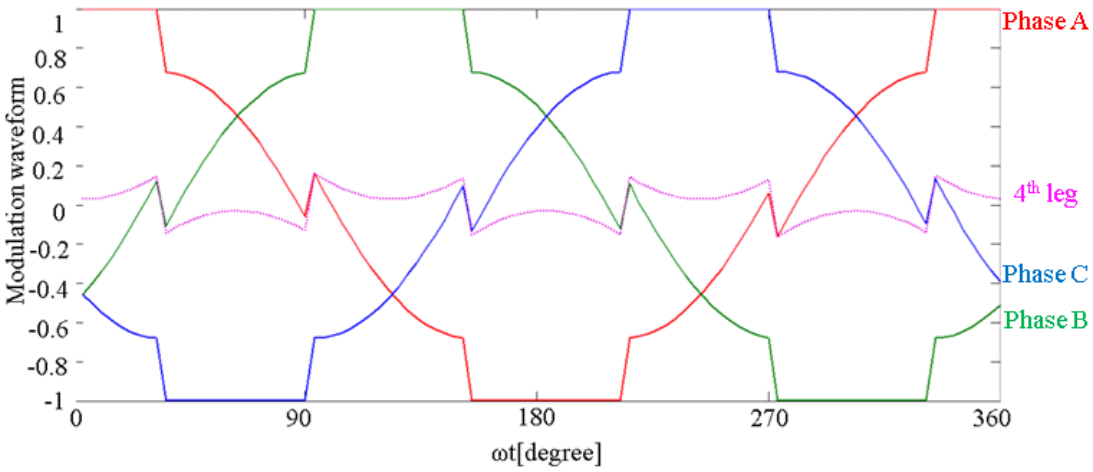



Figure 3.14 Simulated duty ratio waveform of the proposed near-state 3-D SVM with two carrier waves utilized (*Mi*=0.84)

### 3.2.4 Implementation of near-state 3-D SVM

Understanding how to solve complex math equations is part of the research, but knowing when and where to apply the math equations is more important[27]. This part discusses the techniques that are needed in terms of the experimental implementation of the proposed switching scheme. A low voltage level test bench was set up for this purpose where the DC link voltage is below 50V. The experimental results under high voltage level test are shown in the following sections.

#### 3.2.4.1 DSP implementation of the proposed switching scheme

Figure 3.15 shows the switching pulse patterns of four legs within six sections over one power cycle. As it can be seen, for each phase except the fourth leg, over one power cycle, there are two sections in which the pulse patterns show the opposite switching actions compared to the others. For instance, for phase A, it is clearly shown that Section II and Section III have opposite shapes with other sections. Here we assume that when modulation index value is larger than carrier wave value, the gate drive signal is active high, hence in this convention the gate drive signals in Section II and III are defined as the opposite. The switch pulse patterns of the fourth leg have to change polarity every section. This unique characteristic of the proposed switching scheme requires special techniques when it comes to real time implementation. A scalar implementation of NSPWM is proposed in [26, 39, 43], in which two carrier waveforms for each phase are utilized. The implementation is possible with DSPs that have two individual PWM comparator registers per-phase [39]. The drawback of this technique is that transient between sections causes distortion and it can be only optimized by

applying higher switching frequency, e.g. 20 kHz. For distributed power generation application where the switching frequency is low, a new technique is required.

Since 3-D SVM is perfectly compatible with digital implementation with modern DSPs, therefore, in this research the proposed near-state 3-D SVM is implemented using a Texas Instrument F28335 DSP. Four PWM output channels are needed to send gate signals to the gate drivers. Instead of using two carrier waveforms, here only one carrier waveform is utilized. The choice of the switching actions is section dependent and can be realized with the use of the flexible configurability provided by the action qualifier sub-module of the ePWM module in the DSP [75, 76]. The additional programming code for the proposed switching scheme is placed in the interrupt service routine (ISR) where the action qualifier control register changes the PWM switching pattern for the next PWM cycle. This is illustrated with phase A in Figure 3.16.

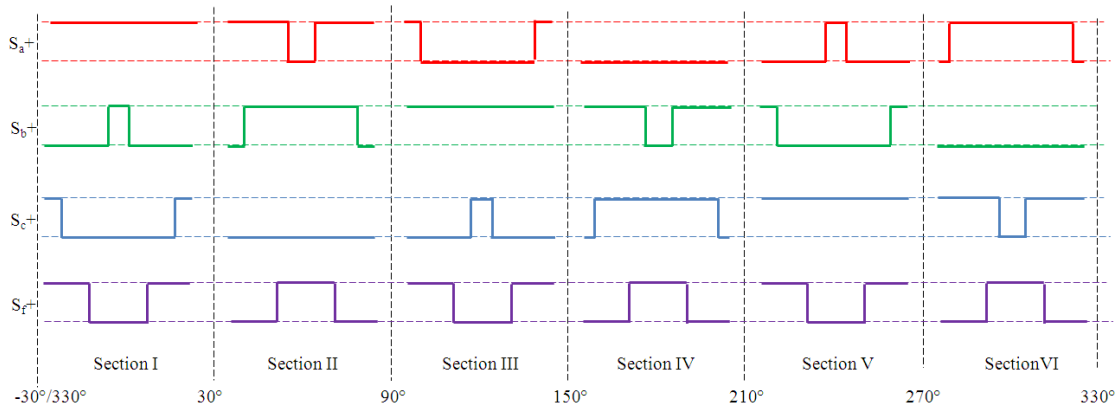



Figure 3.15 Switching pulse patterns of near-state 3-D SVM within six sections over one power cycle

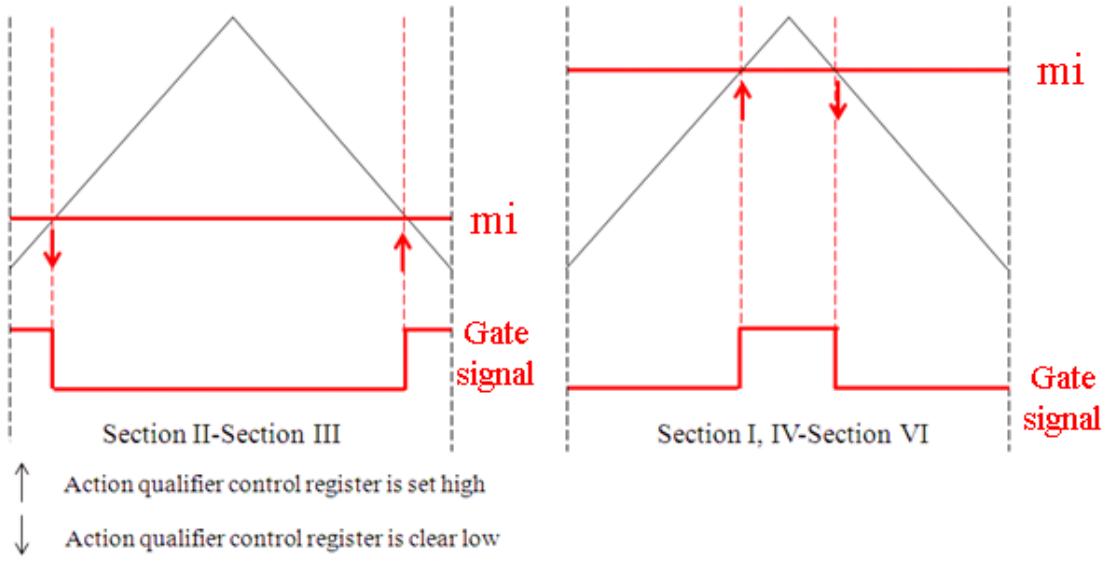



Figure 3.16 DSP implementation of near-state 3-D SVM (phase A)

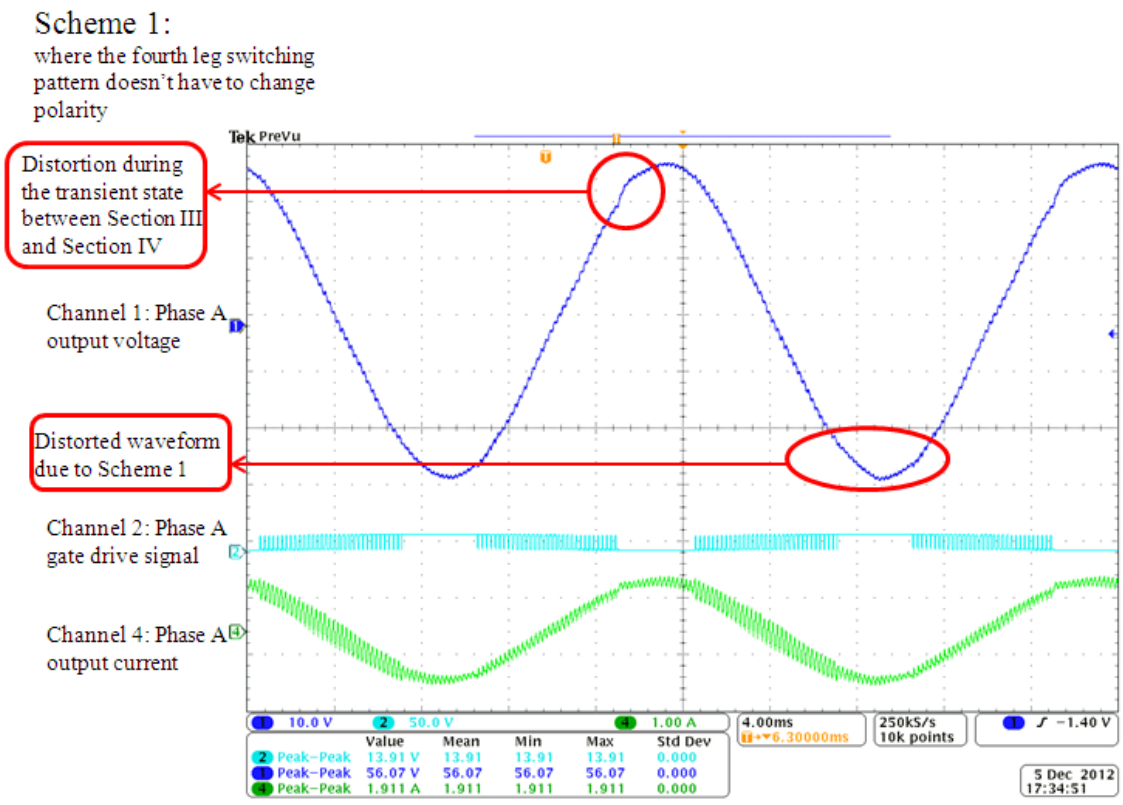
### 3.2.4.2 Instrumentation to solve the distortion during the transient between sections

One issue that is related to the implementation of the proposed switching scheme is the voltage distortion caused by unsmooth transient between the sections. For demonstration purposes, a low-voltage test bench was built to show the effect during the transient state of the sections. As explained in the previous part, the action qualifier control registers have to change switching actions during the transient between the sections of two opposite polarity of the switching patterns, a distorted voltage waveform is created due to this effect. The following part investigates the reason behind this effect, thus an instrumental solution is provided to solve the problem.

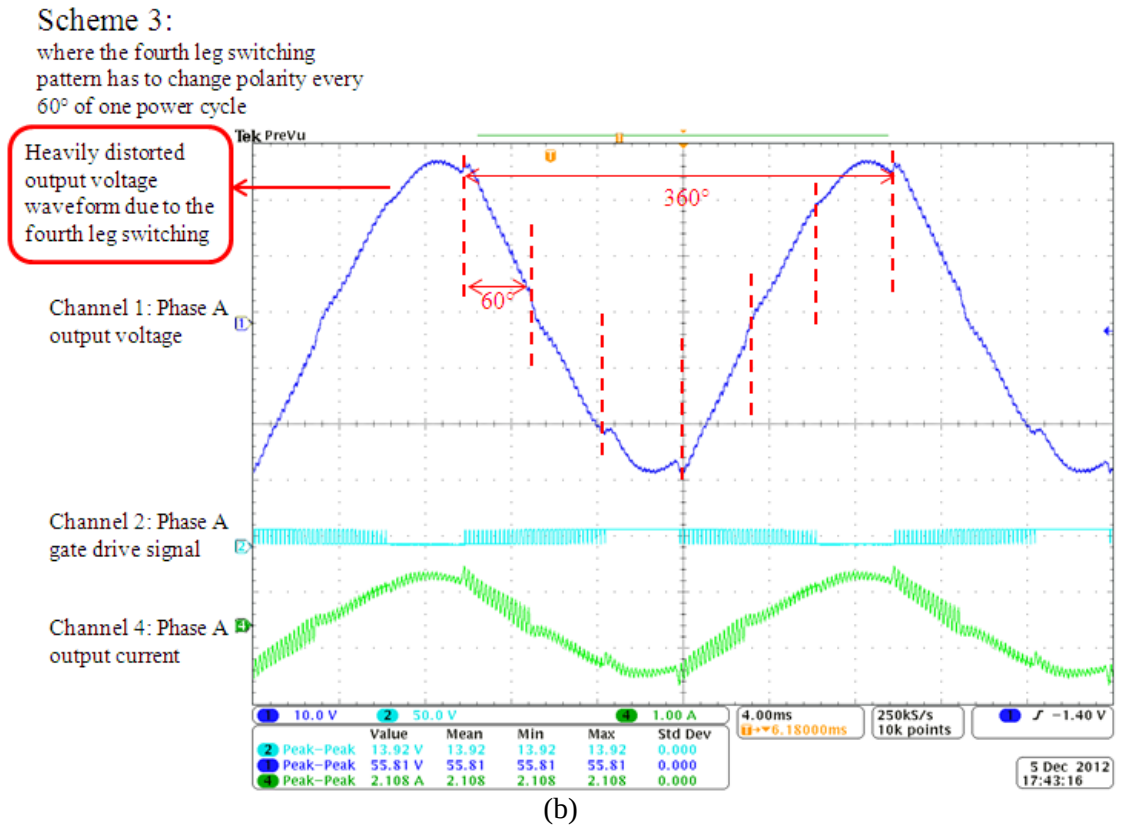
#### A. Distortion during the transient between sections

In Figure 3.17, both Scheme 1 and Scheme 3 are shown to demonstrate the unsmooth transient effect in the real-time implementation. Since the fourth leg switching patterns don't change polarity for Scheme 1, a distortion in the output voltage waveform is observed for Phase A (Figure 3.17 (a)). This is due to the transient state between Section III and Section IV. Also it is observed that the bottom of the sinusoidal waveform is slightly distorted, this is due to the higher harmonic content characteristics of Scheme 1 itself. Scheme 3 is supposed to provide a good quality output waveform with much less harmonic content than Scheme 1; however, as it is seen in Figure 3.17 (b), the output voltage is heavily distorted. This indicates the unsmooth transient between each section due to the fact that the fourth leg switching pattern has to change polarity every 60°.

A closer look at the transient state between Section III and IV for phase A is presented in Figure 3.18. It can be seen that in the last PWM cycle of Section III, the switching pattern is not the one which it is supposed to be. It is this one switching pattern that causes the distortion for Phase A.




(a)




(b)

Figure 3.17 Distortion during the transient state between the sections; (a) Scheme 1;(b) Scheme 3; Channel 1: Phase A output voltage; Channel 2: Phase A gate drive signal; Channel 3: Phase A output current

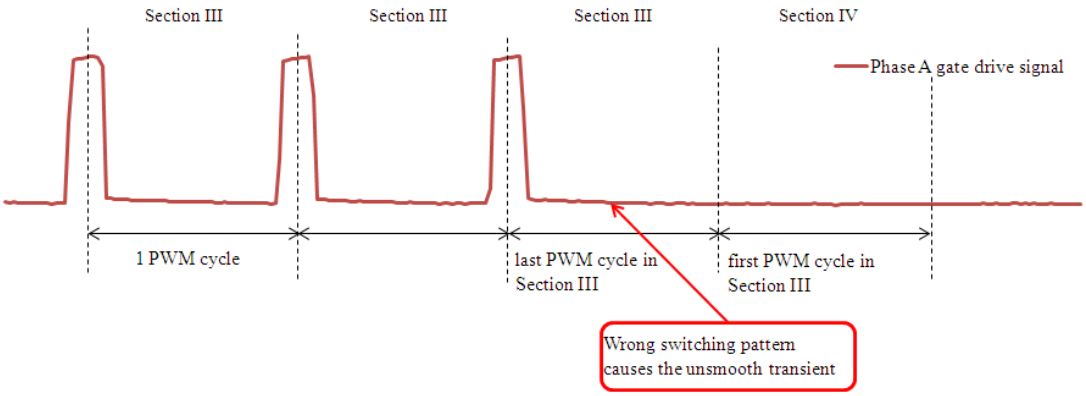



Figure 3.18 Gate drive signals for Phase A during the transient state between Section III and Section IV

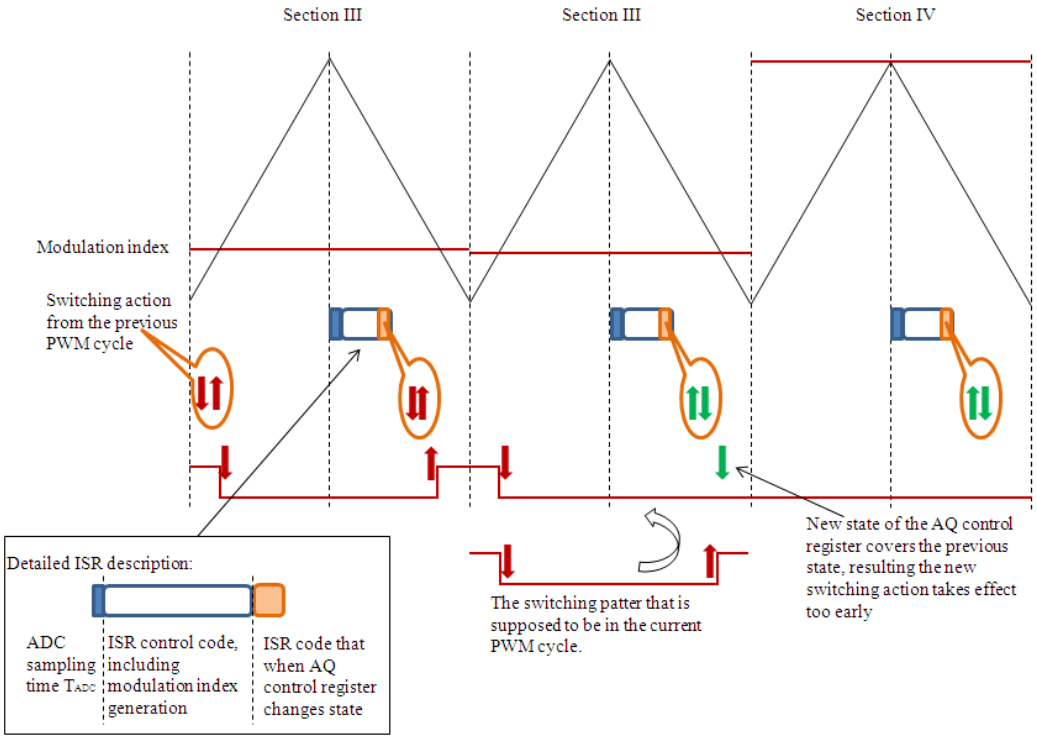



Figure 3.19 The way DSP updates the compare register value and action qualifier control register value caused the problem

Figure 3.19 shows how the wrong switching pattern is created. The programme for the change of the action qualifier control register in the DSP is placed in the ISR, and the ISR normally happens after the sampling of the output values of the inverter. The sampling scheme affects the digital controller design and needs appropriate attention[63, 75, 77]. In the ISR, the new modulation index value is generated and the new value is not updated until the next PWM cycle due to the shadow register inside the ePWM sub module [63, 78, 79]. However, the change of the action qualifier control register takes effect immediately, and this poses the problem during the transient since the new

control register value will cover the previous value which is the action that is supposed to be. Therefore the switching event that is supposed to take effect in the next PWM cycle appears in the current PWM cycle, resulting in the wrong switching pattern.

**B. Instrumentation solution**

As explained, the switching actions take effect immediately after the register is given a new value, and for the proposed switching scheme, this action is required when the new modulation index value takes effect. By deliberately putting a delay inside the ISR before the action qualifier control register takes effect, the problem can be solved. This delay time must be calculated precisely so that the switching action code will appear just after the current switching event finishes, but before the next PWM cycle comes. The technique required to calculate the ISR execution time is explained in details in Appendix B. Figure 3.20 shows the technique to insert the delay in the ISR for Phase A. This delay time has to be calculated for the full modulation range as well.

Apart from the delay that is put in the ISR, the starting state of the switching pattern has to be reset as well. This is because the output of the PWM pin from the previous PWM cycle will hold the value unless it is forced to pull up or down by setting the zero bit of the action qualifier control register. According to [78, 79], setting the zero bit of the register will not affect the rest of the switching actions for the current PWM cycle. Hence at the beginning of each PWM cycle, certain action qualifier registers have to be set to make sure that the actions from the previous PWM cycle has been cleared.

Therefore, combined with these two techniques as it can be seen in Figure 3.20, the distortion problem during the transient is fixed. The technique is also applied to the other phases during the transient state and the fourth leg for Scheme 3, so the heavily distorted output waveform that has been observed in Figure 3.17 is corrected. The modified Scheme 3 ensures a smooth transient state between each section; therefore a good quality output voltage waveform can be obtained as shown in Figure 3.21. The proposed near-state 3-D SVM switching scheme programming code can be found in Appendix C.

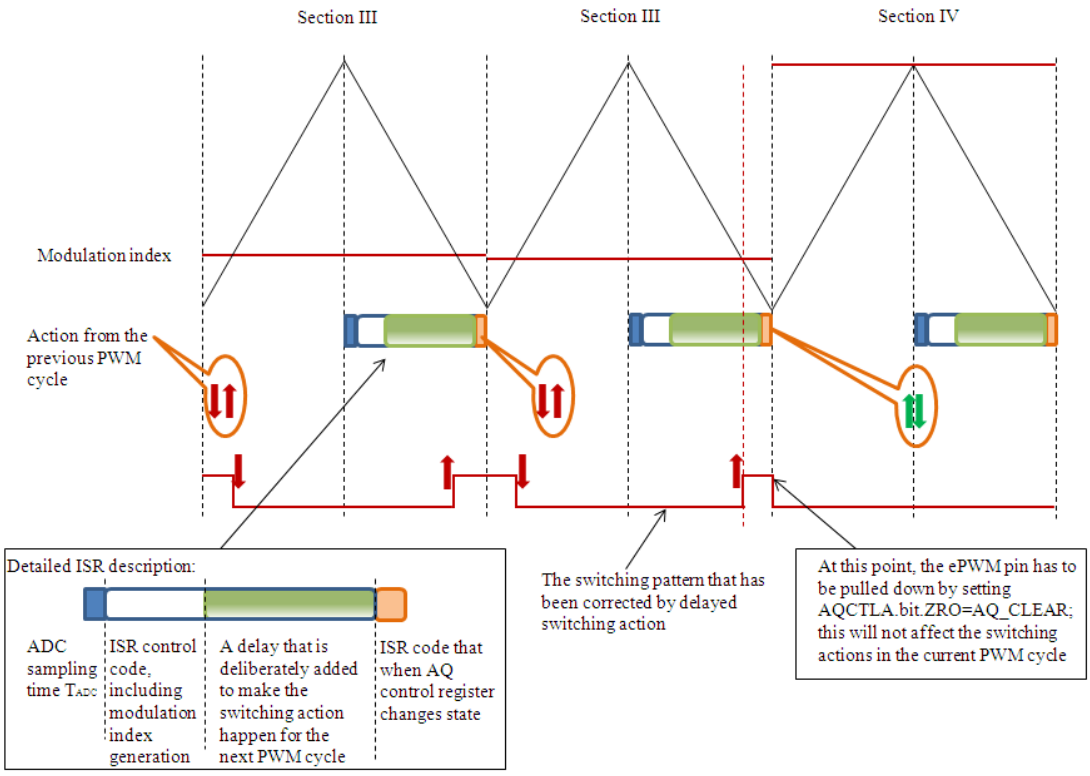



Figure 3.20 Adding a delay in the ISR before the action qualifier control register takes effect and pulling down the PWM output pin at the beginning of Section IV ensures a smooth transient state for Phase A

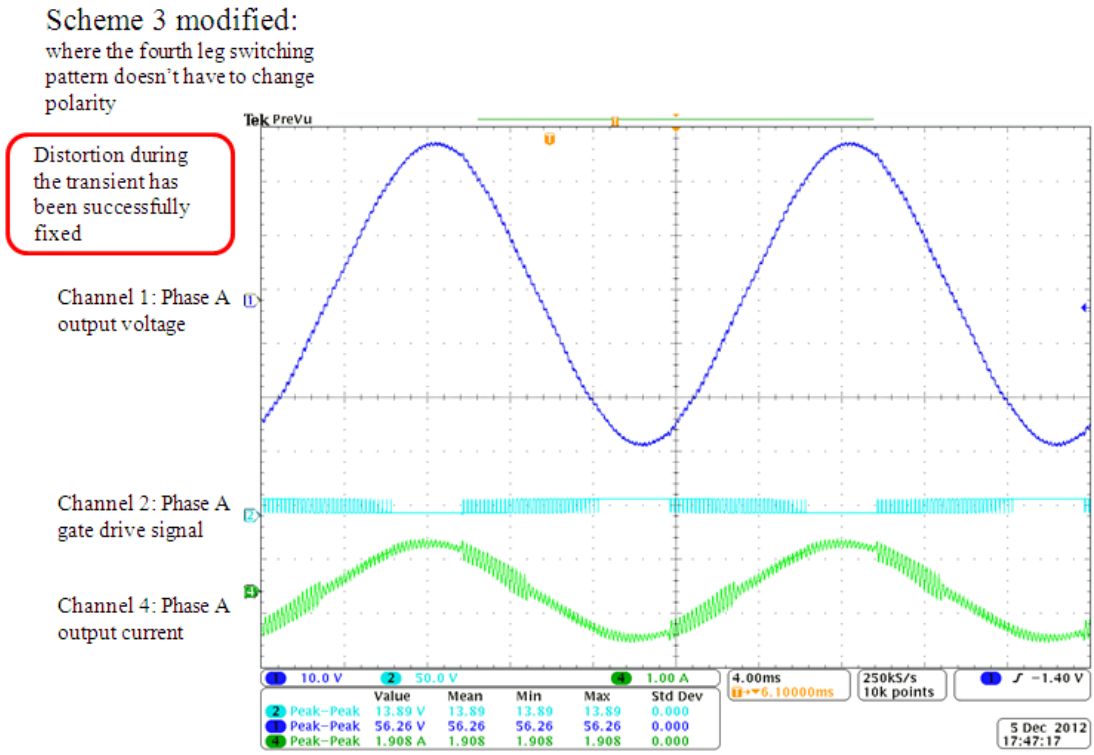



Figure 3.21 Output waveforms for Phase A when applying the techniques; Channel 1: Phase A output voltage; Channel 2: Phase A gate drive signal; Channel 3: Phase A output current

## 3.3 Laboratory test bench

### 3.3.1 Specifications

The design targets of the four-leg inverter are shown below:

- Output phase voltage: 200V
- Output frequency: 50Hz
- Output voltage THD:

  For balanced load condition: ≤ 3%

  For unbalanced load condition: ≤ 5%
- Maximum output power: 5 kW
- Load power factor range: 0.8Lagging to 0.8 Leading
- Load unbalance situation:

  $Unbal\_N\% \leq 100\%$

  $Unbal\_0\% \leq 33\%$

A laboratory test bench is set up to test the proposed switching scheme experimentally. The circuit layout for the laboratory test bench is shown in Figure 3.22. The individual hardware components are briefly introduced in the following sections.

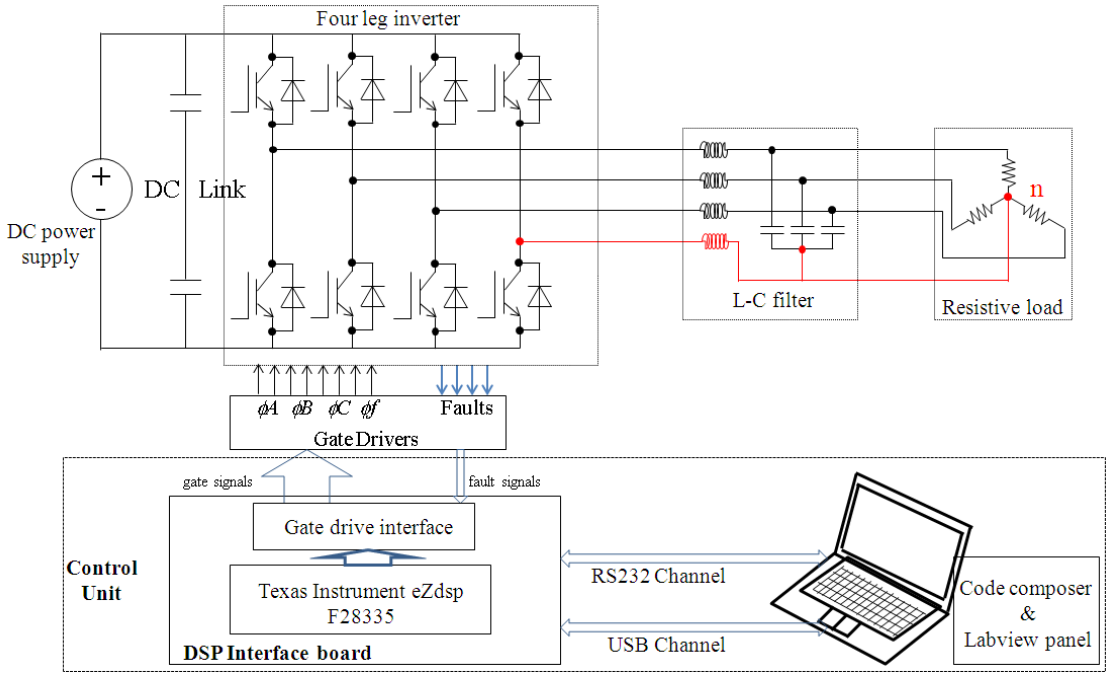



Figure 3.22 Laboratory test bench for testing the proposed switching scheme

## 3.3.2 Hardware components of the laboratory test bench

### 3.3.2.1 DC link

DC link side includes the DC power supply and DC link capacitors. Considering the phase voltage is 200V, the minimum DC link voltage required would be $200\times\sqrt{2}\times\sqrt{3}$=490V. During the transient state, the DC link voltage required will be even higher than this. Considering 10% more DC voltage is required for transient operation, a DC link of 539V is then needed. Also, under unbalanced load condition, the negative-sequence current will require a higher negative-sequence control voltage, this will, in effect, require a higher DC link voltage, therefore, 600V is used as the DC link voltage.

Although the zero-sequence current can be dealt with by the fourth leg, negative-sequence current still has a big effect on the ripples of the DC link. Two capacitors of 2200μF/400V are connected in series. It could be an argument in terms of choosing one capacitor or two split capacitors on the DC link side. Since the load neutral point is now connected to the fourth leg instead of the mi-point of the split DC link capacitors, one capacitor is preferable in terms of size and cost. However, in this experimental set-up, we choose two capacitors for the reason that by doing so the common-mode voltage can be easily observed. It should also be mentioned here that the author didn't choose the DC link capacitors, since the ripple on the DC link is considered small. The equivalent capacitor of the complete DC bus is then 1100μF/800V.

### 3.3.2.2 Switching cells

Switching cells include power electronics devices, snubber circuit and gate drivers. The switching frequency is selected to be 5 kHz. Each switch on-off means switching loss and conduction loss for the system and they should be kept as low as possible. Therefore 5 kHz is a compromise between the output voltage quality and system efficiency. Four IGBT modules SKM 50GB123D have been used to build the four legs of the inverter. To reduce the over voltage of the IGBT switching, capacitor snubber circuit is used for each IGBT module. Gate driver module SKHI 22 A with short circuit protection is compatible with the IGBT module that has been selected. The dead time for the gate driver module is set to be 3.3 μs to prevent shoot-through of the IGBT module.

#### 3.3.2.3 *L-C* filter

A second-order *L-C* filter is used to filter out the high switching frequency ripples on the output of the inverter. The designing process of the *L-C* filter starts with choosing the inductance value based on the current ripple of the phase current, then the resonant frequency is decided based on the switching frequency of the power electronics, the capacitance value is then calculated based on the inductance value and resonant frequency.

According to [62], the inductor design has to follow steps such as obtaining required inductance, avoiding saturation and low dc winding resistance. The maximum per-phase output current was set as 7A, a 10 mH inductor will have a less than 20% current ripple of the peak-to-peak current.

The resonant frequency $f_{res}$ is chosen to be 500Hz, the filter capacitance value can then be easily calculated according to Eq. (3.5), and three capacitors of 10μF were then chosen.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{3.5}$$

The choice of neutral inductor value is a trade-off between the size and the inductor's ability to reduce the neutral current ripple. Big-size inductor will reduce the neutral current ripple; however, big size means the size of the system increased. A neutral inductor of 10mH is selected as a compromise.

#### 3.3.2.4 Resistive Load

Three sliding resistors are used for open loop test under both balanced and unbalanced load condition. The resistance value for each phase can be changed to maximum 30Ω.

#### 3.3.2.5 Digital signal processor

A Texas Instrument eZdsp F28335 evaluation board is used for the project. This DSP is a high speed, floating point controller with hardware features such as high speed clock, off-chip SRAM memory, RS-232 interface, etc together with the software development environment; it can meet the application requirement.

#### 3.3.2.6 DSP interface board

A standard project DSP interface board which was designed at Newcastle University is used to provide an interface between the Texas Instrument F28335 eZdsp evaluation board and the power stage. The main features of the interface board include:

- Six gate drive interface allows the six pairs of PWM outputs of the DSP to interface to external gate driver modules. Fault reset signals are provided on the gate driver connectors for fault indication function.
- A flexible sensor interface is included to allow connection of a variety of current and voltage sensors to the DSP ADC inputs. There are ten identical sensor interfaces on the board.
- The board employs a voltage window detector to detect if a sensor goes out of normal range. Fast hardware over current protection and over voltage protection are provided. The upper and lower limits of the window detector are set so that the dual signal voltage comparator is connected to the trip zone signal on the DSP to enable the trip zone actions on the PWM outputs.
- A DAC is included to allow access to internal software signals in real-time when the micro controller is still operating. A TLV 5604 SPI DAC is included to provide 4 DAC channels.

There're also other features such as shaft encoder interface, general analogue interface, etc which are not used for this project, therefore the information of these features are not included here.

#### 3.3.2.7 Voltage and current sensors

Three isolated amplifiers and four current sensors are used to measure the three-phase output voltage and four inductor currents from the inverter output side. These values, through the sensor interface, will feed into the DSP to serve as feedback signals to the controller loop.

### 3.3.3 Software development environment

A code composer studio, which is a development environment supplied with the DSP is used to programme and debug the real time control code for the system. A Labview based user control panel is used to provide a safe way of communicating with the DSP during the real time operation. The test and control information are uploaded to the DSP

and the system parameter measurements are downloaded from the DSP during the operation. The communication is done through an RS-232 link.

### 3.3.4 Matlab simulation

A simulation model is built in Matlab/Simulink. The power stage is simulated using Simpower tool box so that the details of the power electronics such as forward voltage, current fall time can be emulated. The hardware parameters are set as the same as those of the laboratory test bench. Simulink is used to simulate PWM carrier waveform (one carrier is utilized in this implementation technique), dead time delay (3.3 μs), PWM outputs etc. The switching scheme and control scheme are all written in an embedded C environment block called S-function in Matlab, by setting the proper sampling time, in this case 200 μs relating to 5 kHz switching frequency, this can emulate the interrupt service routine in a real-time DSP system. It should be noted that the measurement blocks are not shown here for the purposes of a clear demonstration. Overall, it has been found a simulation model that is modelled using all these sub blocks gives a very close result to the real time system. The Matlab structure model is shown in Figure 3.23.

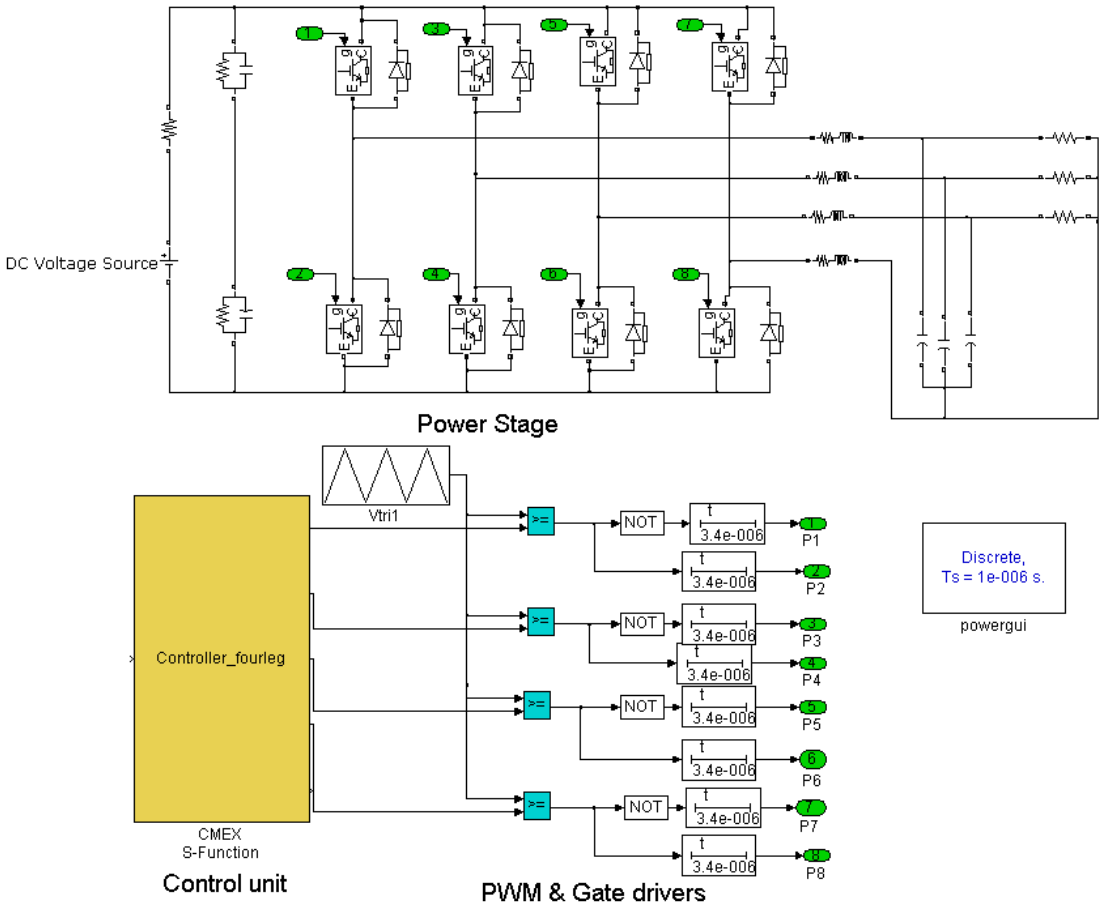



Figure 3.23 An open loop three-phase four-leg VSI implemented with near-state 3-D SVM, Simulation model in Matlab

## 3.4 Simulation and experiment result

### 3.4.1 Simulation and experimental results under balanced load

A balanced linear load is used for open loop simulation to test the near-state 3-D SVM switching scheme. Figure 3.24 shows the simulated three-phase AC terminal voltages. The three-phase output line to neutral voltages; load currents and the common-mode voltage are shown in Figure 3.25. As it can be seen, the common-mode voltage level has been successfully reduced to 150V, which is one fourth of the DC link voltage. The three-phase inductor currents and the neutral current are shown in Figure 3.26. In spite of the current ripple, the average neutral current under linear balanced load is shown as zero.

The experimental test rig has been tested open loop up to 4kW. The three-phase output voltage waveforms and the common-mode voltage waveform over two power cycles are shown in Figure 3.27. As it can be seen, the peak phase voltage reaches 282V; this demonstrates the 15% more dc link utilization compared to sinusoidal PWM. The common-mode voltage level shows the same feature as it was in the simulation.

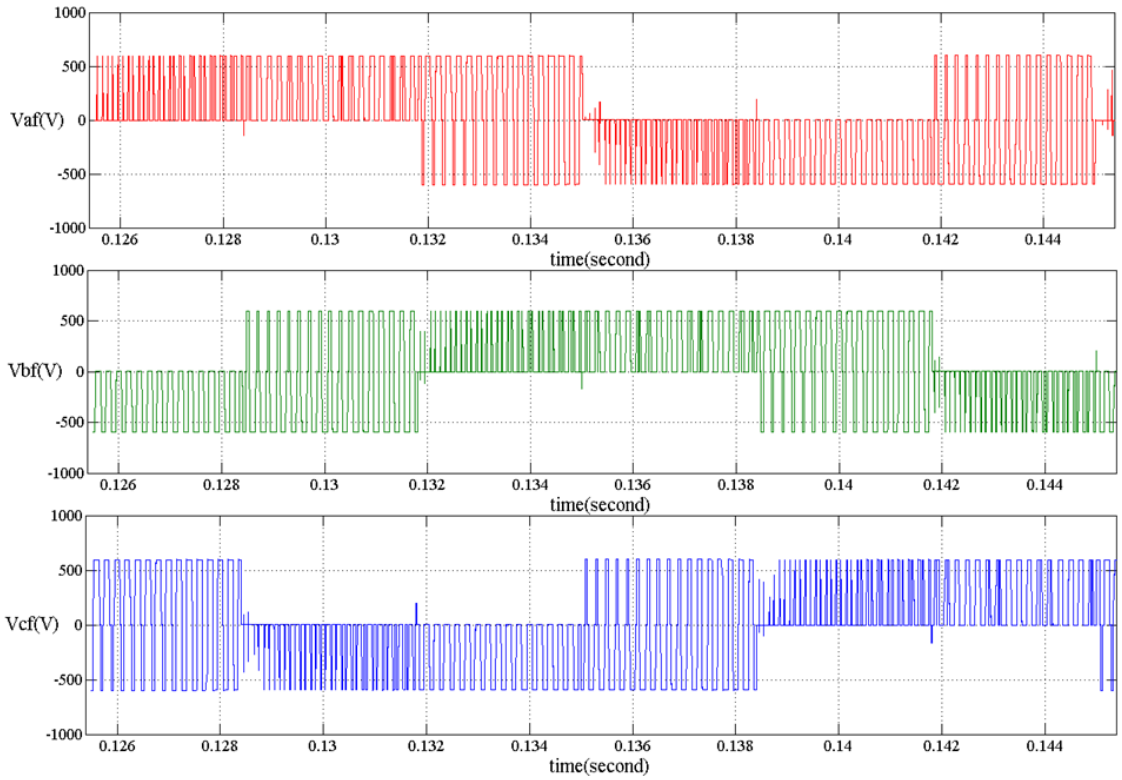



Figure 3.24 Simulated three-phase AC terminal voltages under balanced linear load

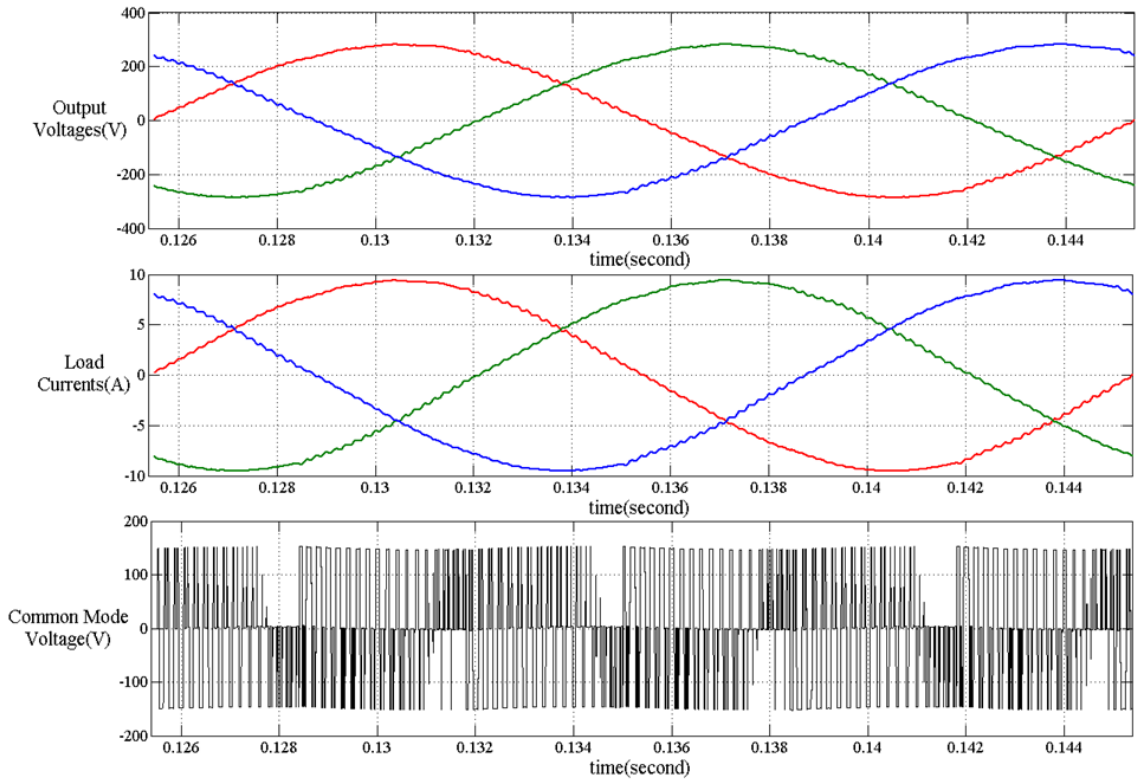



Figure 3.25 Simulated three-phase output voltages, load currents and the common-mode voltage under balanced linear load

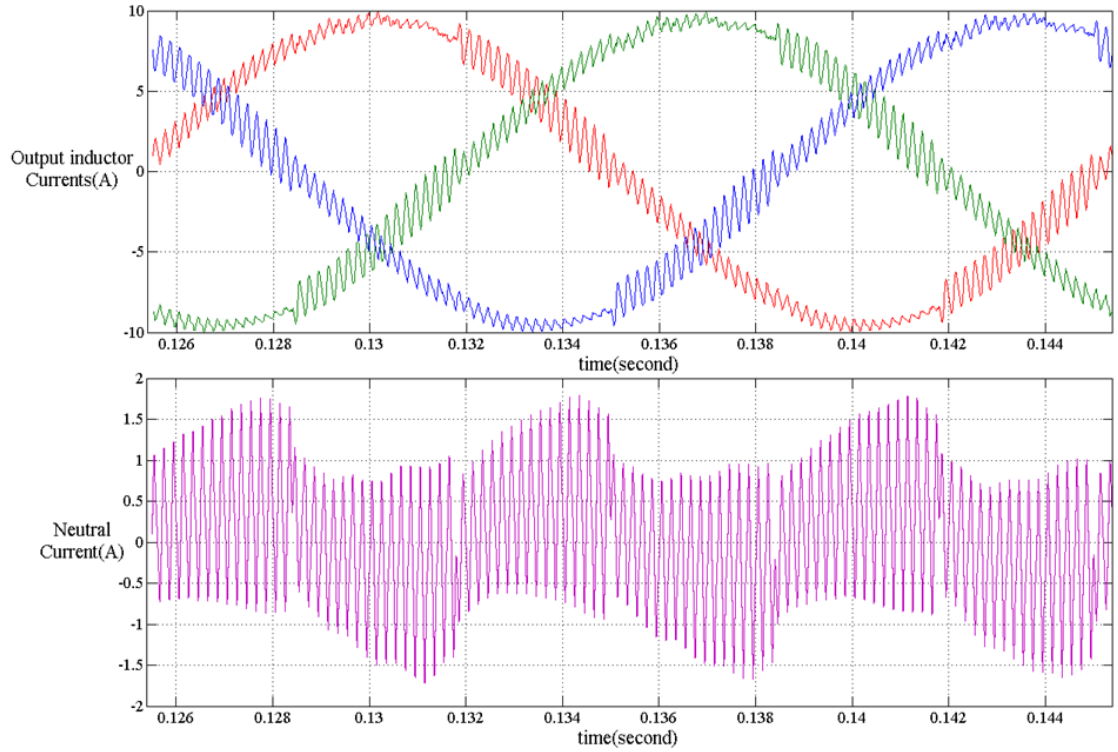



Figure 3.26 Simulated three-phase output inductor currents and the neutral current under balanced linear load

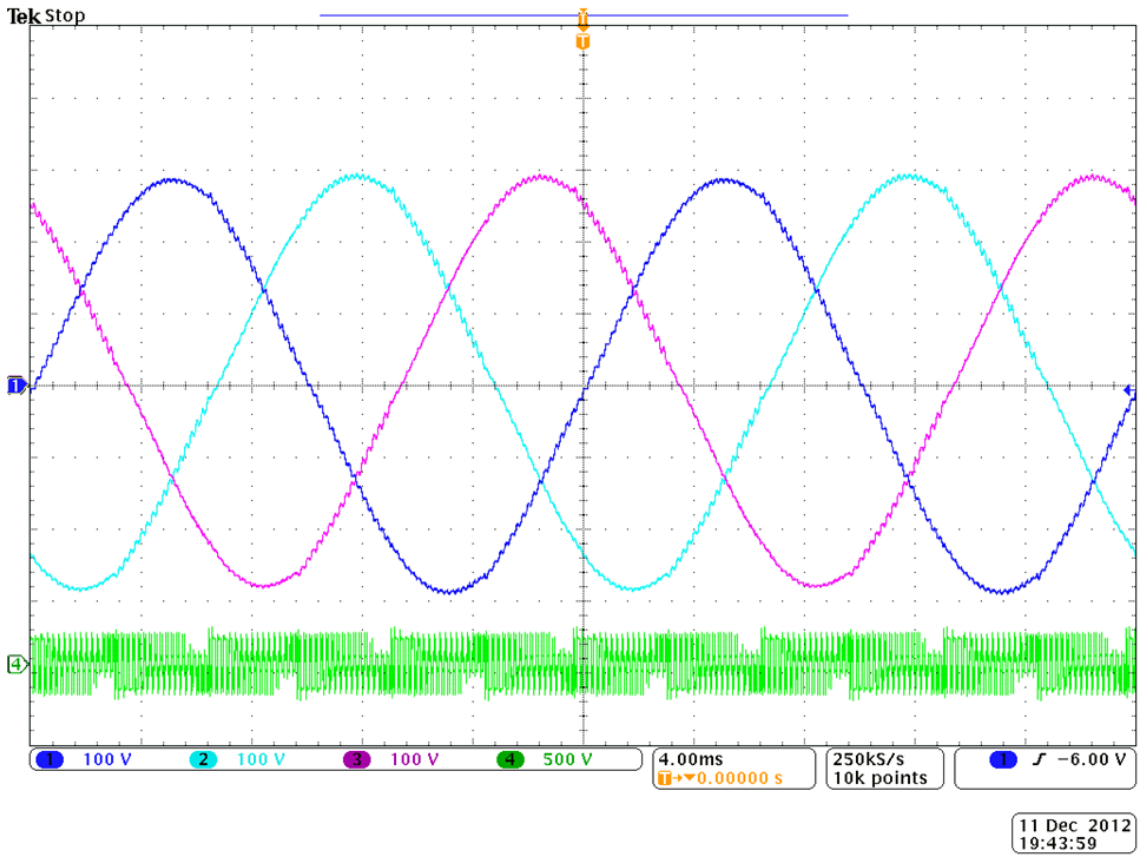



Figure 3.27 Experimental results showing three-phase output voltages (Channel 1-Channel 3), and the common-mode voltage (Channel 4)

The output voltage frequency spectrum is shown in Figure 3.28. From the frequency spectrum analysis, it can be seen that there are two distinct harmonic contents at the 3$^{rd}$ and 5$^{th}$ harmonics, and two harmonics contents around the switching frequency $f_{sw}$-$f$ and $f_{sw}$+$f$ as shown in the diagram. The output voltage THD therefore is calculated to be 3.01%, satisfying the design specification.

The frequency spectrum analysis based on the common-mode voltage under the proposed switching scheme is shown in Figure 3.29. As a comparison, the frequency spectrum of the common-mode voltage under the conventional 3-D SVM is shown in Figure 3.30. Comparing these two results, it has been shown clearly that at 5 kHz switching frequency, the harmonic content of the proposed switching scheme has been reduced to around a third of the conventional 3-D SVM. The near-state 3-D SVM brings higher harmonic contents around the sideband of the main switching frequency as it is shown in the frequency spectrum. In the higher frequency range, 10 kHz and 15 kHz, both switching scheme shows the similar harmonic content.

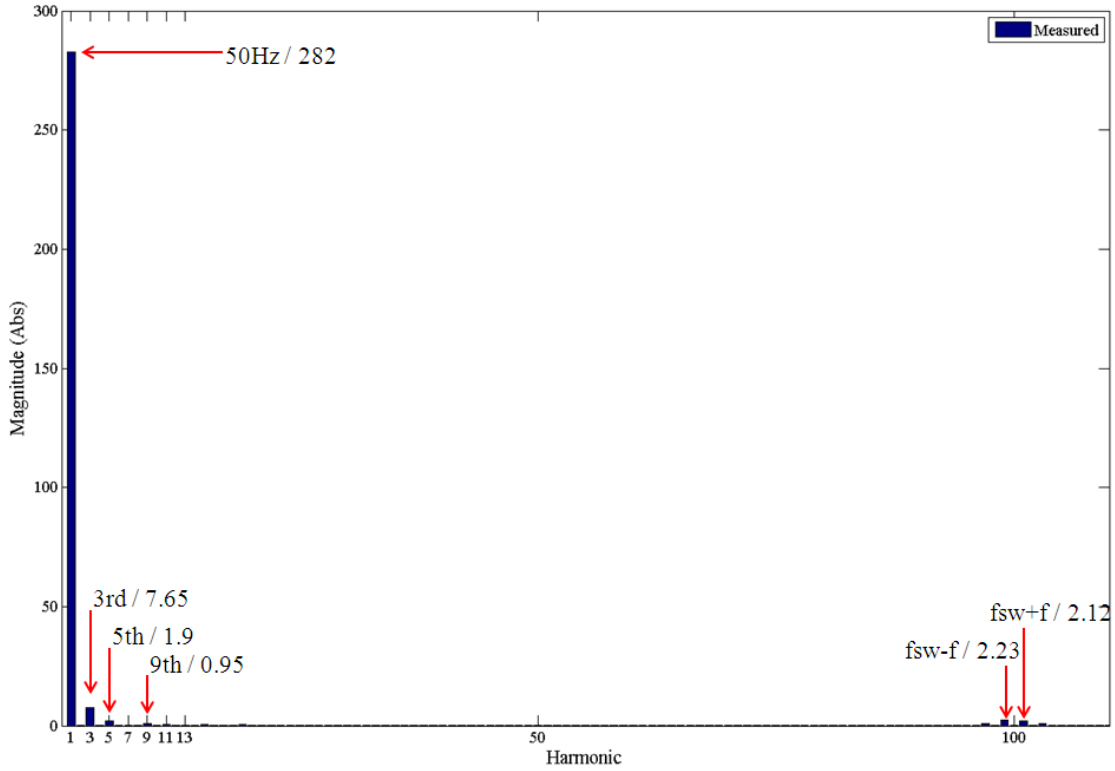



Figure 3.28 Frequency spectrum of Phase A voltage under the proposed switching scheme

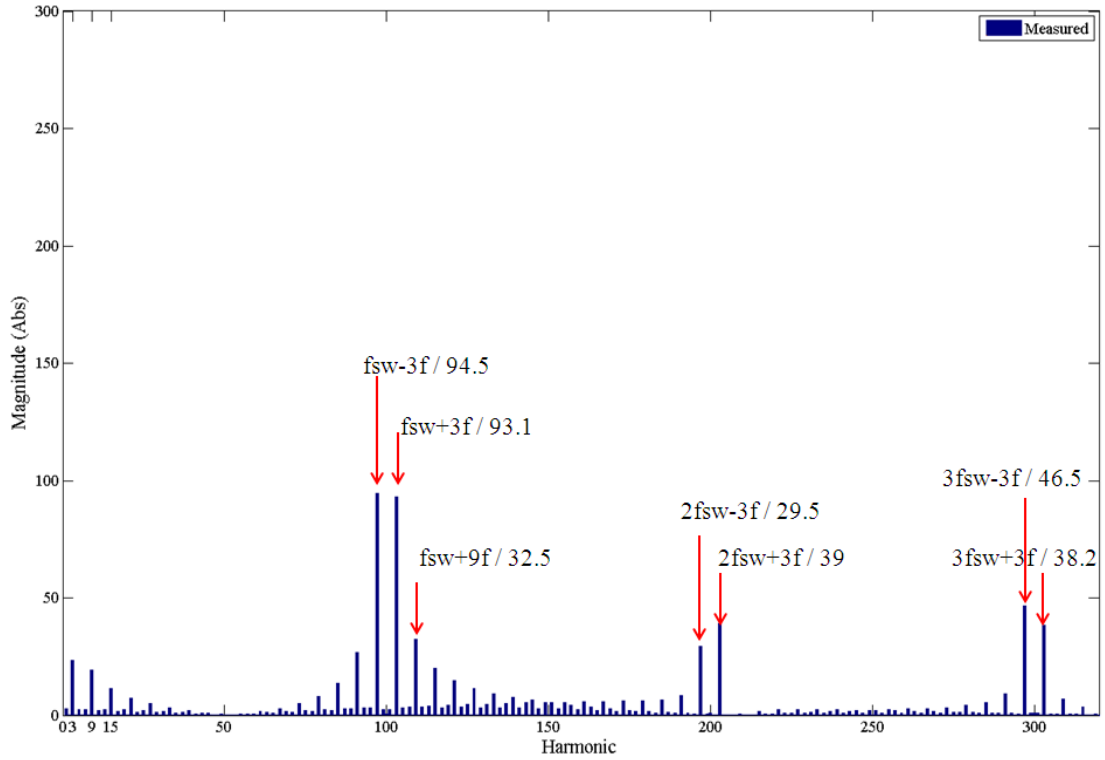



Figure 3.29 Frequency spectrum of common-mode voltage under the proposed switching scheme

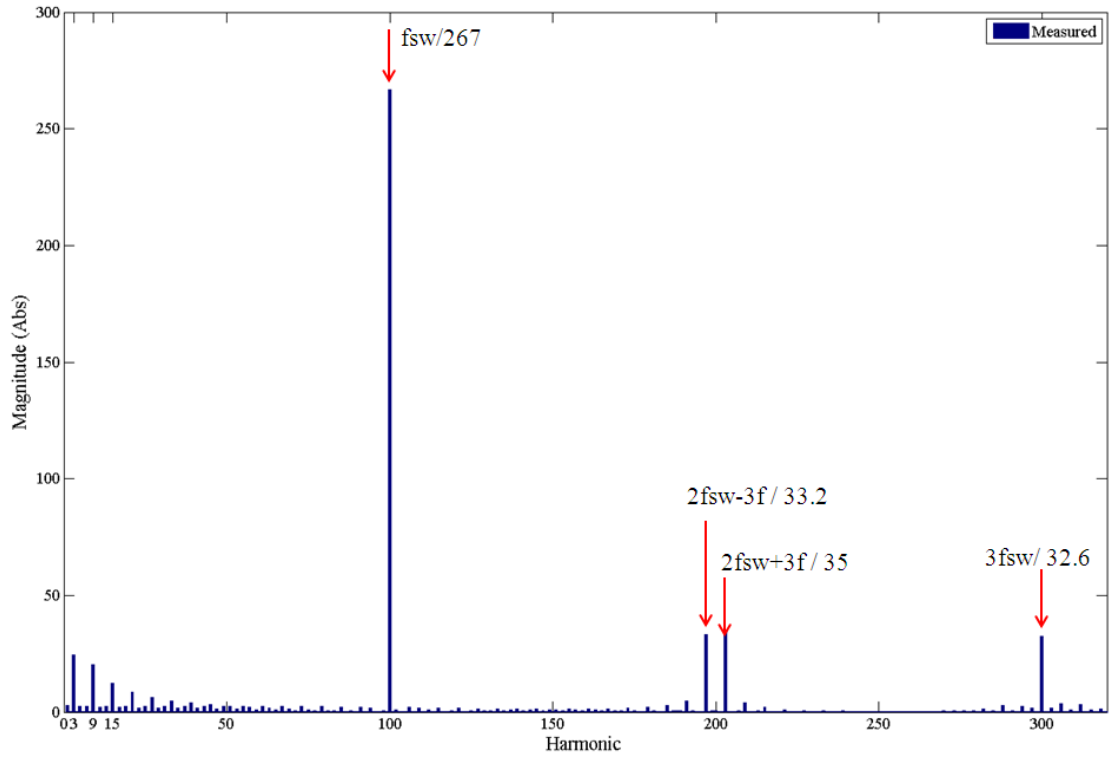



Figure 3.30 Frequency spectrum of common-mode voltage under conventional 3-D SVM

### 3.4.2 Simulation and experimental results under unbalanced load

The results shown in the previous part demonstrate that the proposed switching scheme is suitable for a three-phase four-leg VSI and it is effective in reducing the common-mode voltage to a certain level. The main purpose of using a three-phase four-leg VSI is its ability to control an unbalanced load, this part demonstrates that the near-state 3-D SVM also works under unbalanced load condition.

The unbalanced load condition varies from case to case in the power system. In this test, two unbalanced load conditions are created to test the performance of near-state 3-D SVM under unbalanced loading condition. The test is carried on based on open loop, so a reference switching vector based on the known load condition has to be pre-calculated. The calculation is based on the average large signal model of the four-leg inverter in *A-B-C* coordinate shown in Figure 2.27. The three-phase unbalanced current has to be decomposed into positive, negative and zero-sequence using symmetrical component theory before they are used to calculate the per-phase reference voltage.

#### 3.4.2.1 Unbalanced load condition 1

In this case, an open loop system simulation for an unbalanced load is created with three phase load as $R_A$=30Ω, $R_B$ =45Ω, and $R_C$=60Ω, this will result in an unbalanced three-

phase load current as $I_{LA}$=6.67∠0° A, $I_{LB}$=4.4∠-120° A, and $I_{LC}$=3.3∠-240°A. The neutral current $I_n$ in this case is 4.17A. The pre-calculated reference switching vector creates a skewed ellipse in the $\alpha$-$\beta$-$\gamma$ coordinate as shown in Figure 3.31. Also in Figure 3.31, the trajectory of the reference switching vector under balanced load condition is shown. The γ element of the reference switching vector under balanced load condition is zero; therefore the trajectory is located only on the two-dimensional $\alpha$-$\beta$ plane. For demonstration purposes, the trajectory of the unbalanced load current is shown as well. The details of the load current trajectory can be seen in Figure 3.32. The negative-sequence current causes the trajectory on the $\alpha$-$\beta$ plane to be an oval shape instead of a circle (Figure 3.32), and the zero-sequence current pulls the trajectory into $\alpha$-$\beta$-$\gamma$ coordinate.

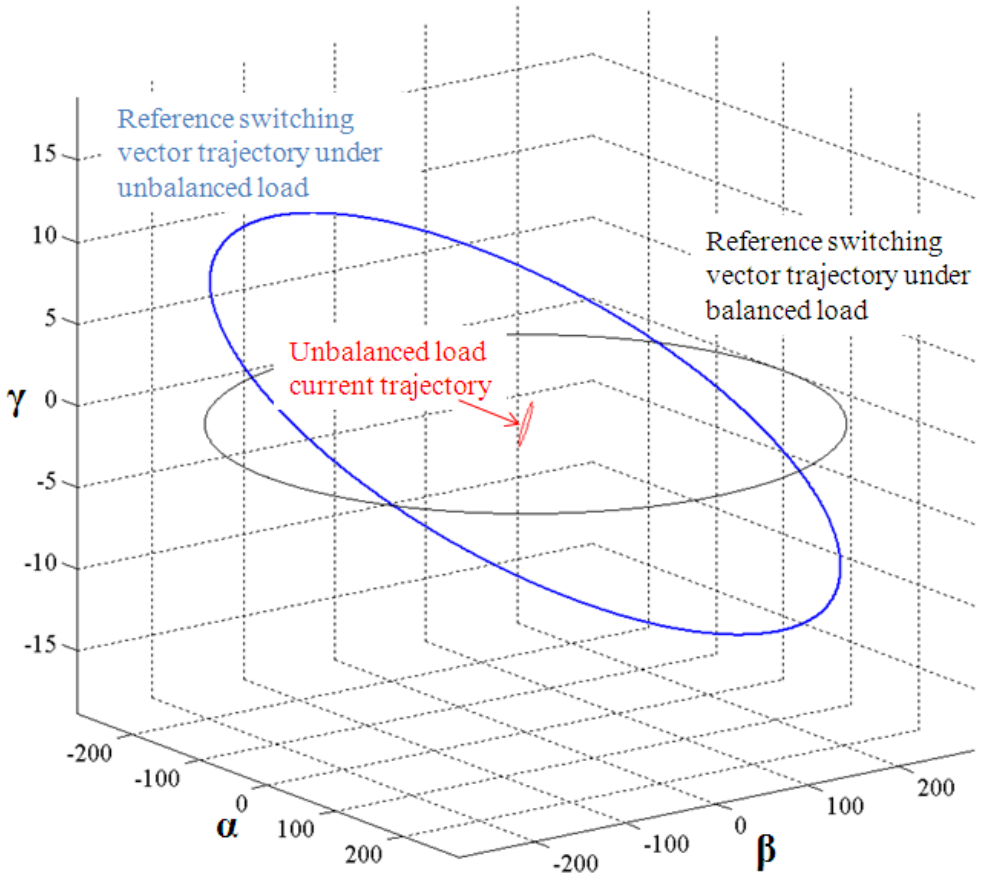



Figure 3.31 Trajectories of reference switching vector under balanced load, balanced load conditions and unbalanced load current trajectory ($I_{LA}$=6.67∠0° A, $I_{LB}$=4.4∠-120° A, $I_{LC}$=3.3∠-240°A)

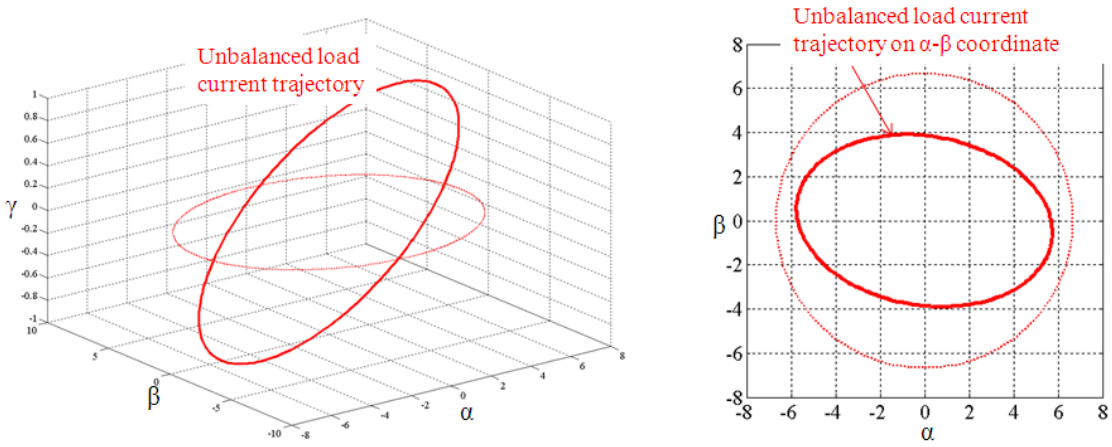



Figure 3.32 Trajectory of the unbalanced load current shown in $\alpha$-$\beta$-$\gamma$ coordinate and its projection on $\alpha$-$\beta$ plane ($I_{LA}$=6.67 $\angle$ 0° A, $I_{LB}$=4.4 $\angle$ -120° A, $I_{LC}$=3.3 $\angle$ -240°A)

The three-phase output line to neutral voltages; load currents and the common-mode voltage are shown in Figure 3.33. As it is shown, although the three phase load currents are unbalanced caused by unbalanced load condition, the three-phase output voltage maintain balanced. It is also important to notice that the common-mode voltage level is still reduced, proving that the proposed switching scheme works under unbalanced load condition as well. The simulated three-phase inductor currents and the neutral current are shown in Figure 3.34. Figure 3.35 and Figure 3.36 show the experimental results under the same unbalanced load condition. FFT analysis based on Phase A output voltage shows that the THD is 3.53%, which satisfies the specification.

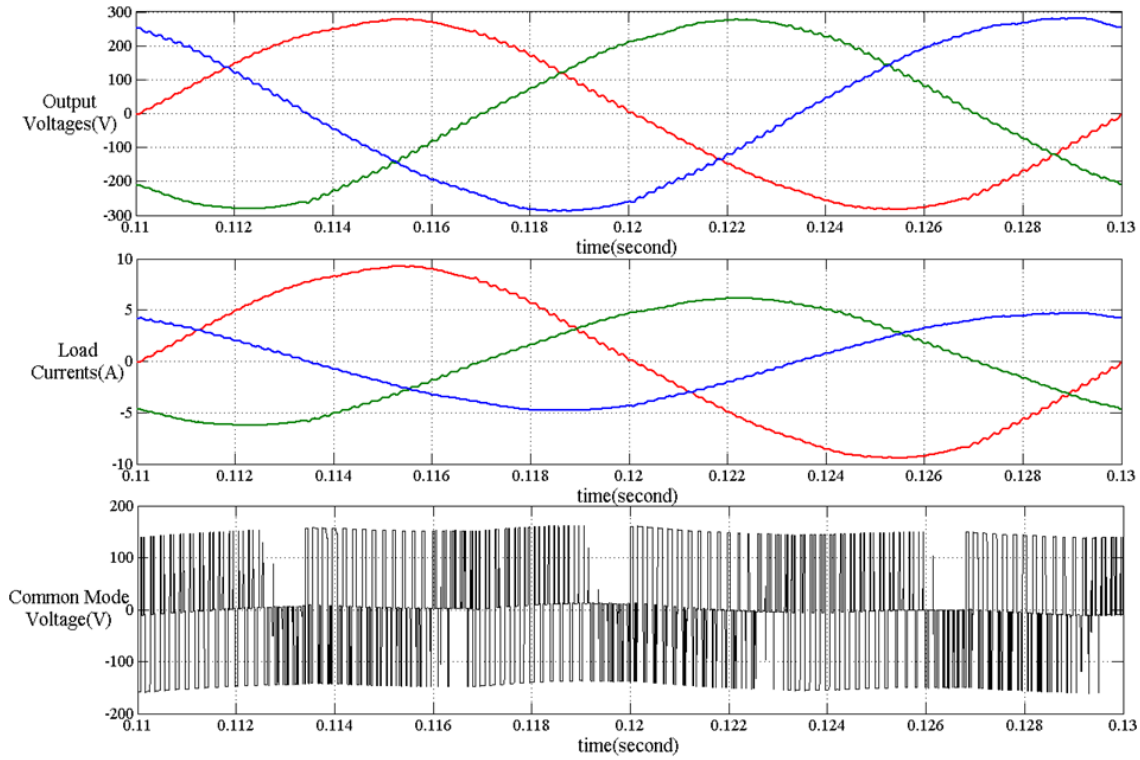



Figure 3.33 Simulated three-phase output voltages, load currents and the common-mode voltage under unbalanced load

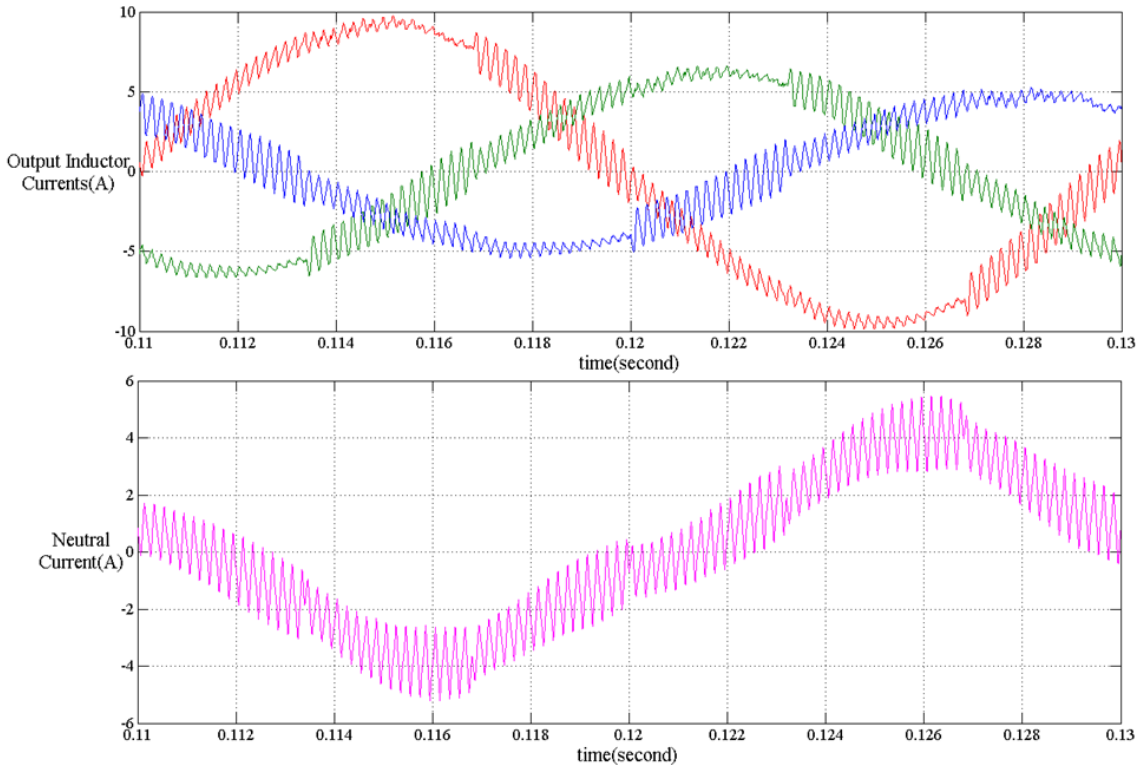



Figure 3.34 Simulated three-phase output inductor currents and the neutral current under unbalanced load

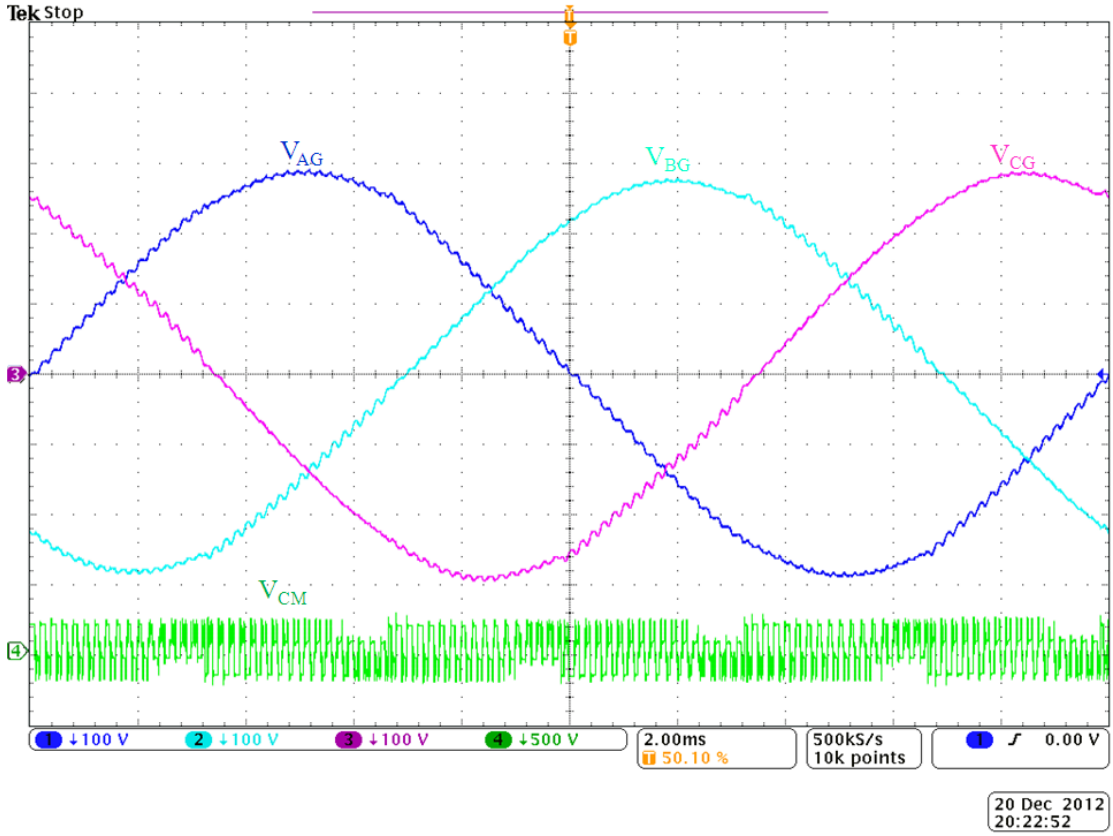



Figure 3.35 Experimental results showing three-phase output voltages under unbalanced load (Channel 1-Channel 3), and the common-mode voltage (Channel 4)

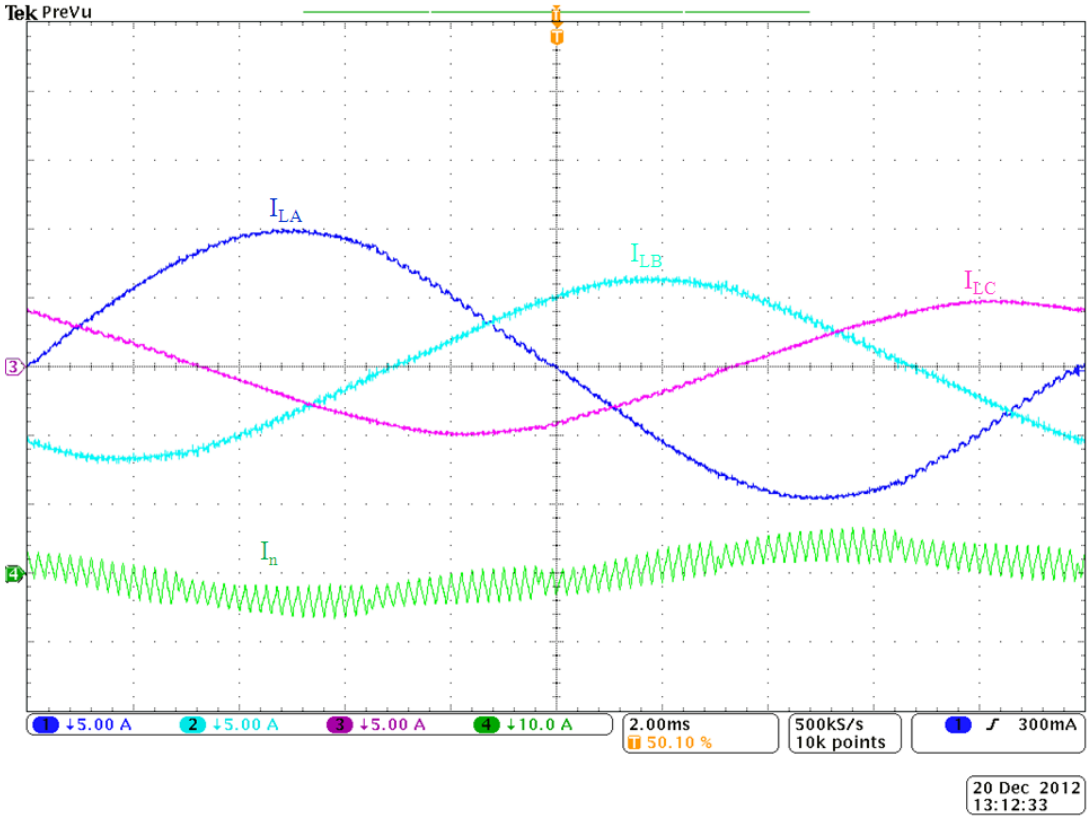



Figure 3.36 Experimental results showing three-phase load currents under unbalanced load (Channel 1-Channel 3), and the neutral current (Channel 4)

### 3.4.2.2 Unbalanced load condition 2

In this test, a heavily unbalanced linear load is tested. Phase A and B are connected to 30 Ω resistors and Phase C has no load. The DC link voltage is still 600V. The three-phase output voltages remain the rated value(one power cycle shown in Figure 3.37), which gives 6.67 A load currents for Phase A and B. Phase C current is zero since it is not loaded. It is shown in Figure 3.38 that the magnitude of the neutral current is equal to the value of phase A and B load current value, with switching ripples on the current waveform. With the proposed switching scheme, a balanced three-phase output voltage is obtained as it can be seen in Figure 3.37. The THD turns out to be 3.8%, considering the load unbalance percentage in this case, with *Unbal_N*%= *Unbal_0*%=50%, the quality of the output voltage maintain high.

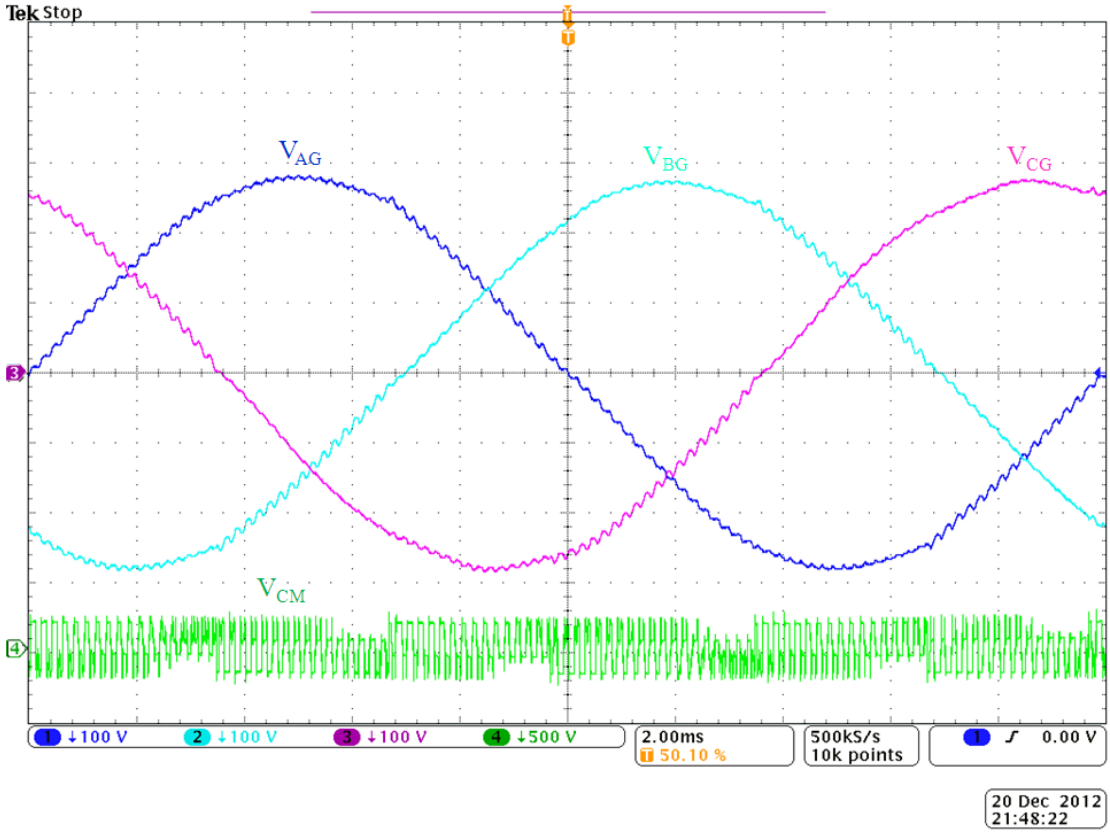



Figure 3.37 Experimental results showing three-phase output voltages when phase C is unloaded (Channel 1-Channel 3), and the common-mode voltage (Channel 4)

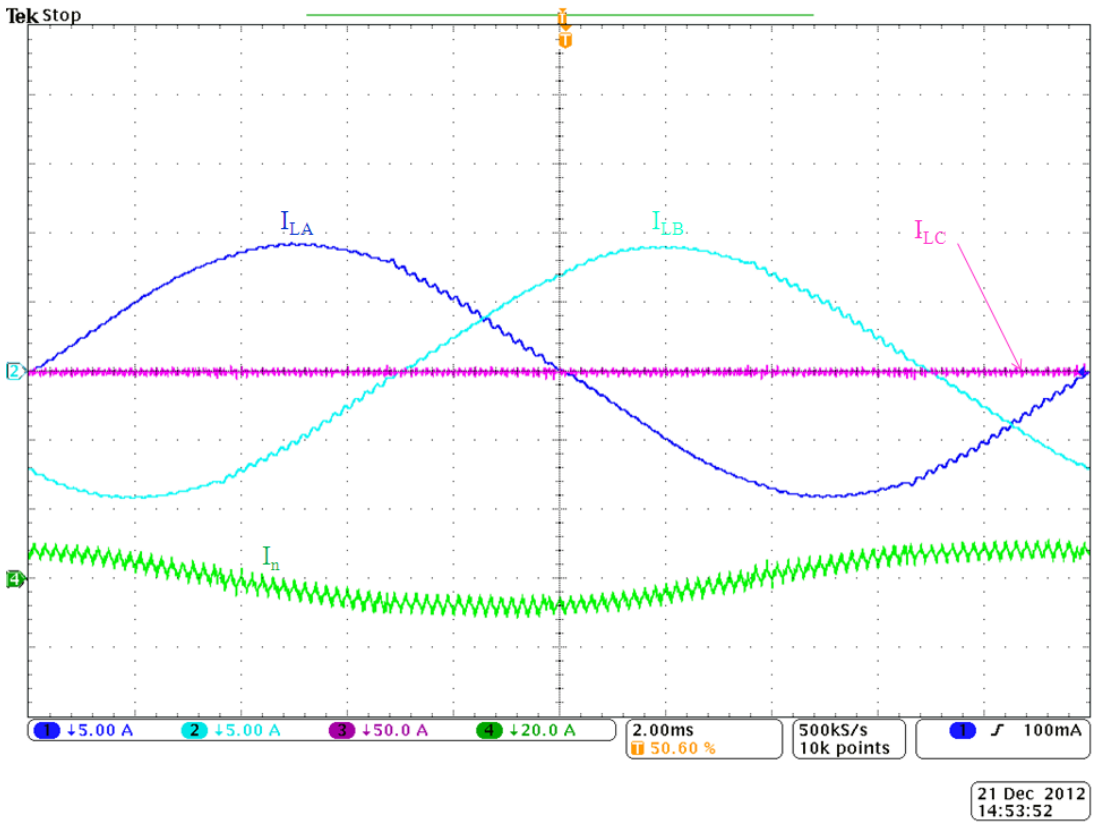



Figure 3.38 Experimental results showing three-phase load currents when Phase C is unloaded (Channel 1-Channel 3), and the neutral current (Channel 4)

## 3.5 Summary

In this chapter, a near-state 3-D space vector modulation scheme is proposed to implement in a three-phase four-leg voltage source inverter.

The proposed switching scheme avoids utilizing the two zero switching vectors, resulting a reduced common-mode voltage, and it inherits all the merits of the conventional 3-D SVM, such as high DC link utilization, lower switching loss and low harmonic distortion.

After introducing the EMI emission issues in a high power system and how it is related to the common-mode voltage, the definition of the common-mode voltage in a four-leg inverter is given. A near-state 3-D SVM switching scheme is therefore introduced to reduce the common-mode voltage. A comprehensive procedure to synthesize the reference switching vector is given, which consists of section identification, selection of the near-state switching vectors, projection of the reference vector and sequencing of

the selected switching vectors. Among all the schemes that can synthesize the reference switching vector, Scheme 3 is selected in the real time implementation.

The simulated and experimental results of the three-phase four-leg inverter demonstrate that the proposed near-state 3-D SVM works both under balanced and unbalanced load condition, and it is effective in reducing the common-mode voltage.

# Chapter 4
# Performance Analysis of the Modulation Schemes for a Four-Leg VSI

The fundamental voltage and current quality is usually based on the analysis of the phase current trajectory as generated by the power converter[80]. This quality is normally measured by the total harmonic distortion factor (THD), or current distortion factor [81]. However, for different modulation schemes that are applied on the three-phase VSIs, the difference sometimes is small and cannot be observed based on the THD analysis of the output waveform. Based on the fundamental per-phase circuit analysis of the inverter system, current harmonics can be calculated mathematically based on the pulse width modulation strategy [56, 61, 80, 82]. The current distortion factor can be calculated based on voltage and current space vector and much work has been dedicated to this subject [36, 55, 83-85]. The harmonic distortion determining factor can be also calculated in *d-q* coordinate, this eases the amount of calculation dramatically [56]. The influence of switching schemes on the conduction and switching loss of a PWM converter system has been fully investigated in [56, 57, 60], the calculation is based on the space vector as well.

Based on the space vector analytical method, this chapter introduces an in-depth performance analysis of the voltage and current quality for a four-leg VSI. As it was mentioned in the literature review, conventional 3-D SVM is dominant in a four-leg VSI implementation. Other switching schemes that are seen in a three-leg VSI implementation, which generates different modulation index waveforms, are not seen in a four-leg VSI application. The performance of a carrier-based PWM method is the same as 3-D SVM since it generates the same modulation index waveform as the 3-D SVM. Therefore, in this chapter, only the near-state 3-D SVM and conventional 3-D SVM are selected so their performance can be analyzed and compared. The voltage harmonic distortion factor and the inductor current harmonic distortion factor are

calculated; the conduction and switching loss based on different switching schemes are presented and compared.

## 4.1 Voltage harmonic distortion factor

For a three-phase four-leg VSI, since it is used for unbalanced or nonlinear load conditions most of the time, the output three-phase currents are unbalanced or distorted. In spite of this, the output voltage is always balanced; the voltage harmonic distortion factor can be calculated based on the voltage space vector.

The output voltage harmonic distortion factor of a three-phase three-leg VSI has been fully investigated in [36, 56, 61], and it has been found that the distortion factor is only related to the modulation index *M*[36]. It is worth noting that the modulation index *M* here is called the fundamental per-phase modulation index and it is different from the space vector modulation index *Mi* in Eq. (2.12), these two modulation indexes are related in

$$M = \frac{2}{\sqrt{3}} Mi \tag{4.1}$$

The same analysis method can be applied to a four-leg inverter. Before the analysis is applied, the following assumptions are made.

- The sampling frequency is the same as the switching frequency, and the new modulation index value for each phase is not updated until the next PWM cycle comes. This means within one PWM cycle the *Mi* value is piecewise constant.
- Symmetrical aligned PWM switching scheme is used, so the calculations will be simplified because of the symmetrical feature.
- The three-phase output voltages are balanced under all load conditions.

The following two sections introduce the analysis based on the conventional 3-D SVM and the near-state 3-D SVM, respectively.

### 4.1.1 Conventional 3-D SVM

The squared RMS value of the phase voltage can be defined as

$$V_{eff}^2 = \frac{1}{T_1}\sum_{k=1}^{2q} V_k^2 T_{PWM}/2 = \frac{1}{2q}\sum_{k=1}^{2q} V_k^2 \tag{4.2}$$

where $T_{\mathrm{PWM}}$ as one PWM sampling time, $T_1$ as one power cycle period time and $q=T_1/T_{\mathrm{PWM}}$ is the number of sampling times within one power cycle. It is also noted that because of the symmetrical feature of the sampling scheme, the calculation can be performed within half a PWM cycle.

The calculation can be carried out within the electrical angular range of [0, 60°], because the voltage and current waveforms in a balanced three-phase system repeat with alternating signs and changing allocation in the angular distance of π/3[60]. The phase voltage can be found by use of the definition

$$V_{an/bn/cn} = V_{ao/bo/co} - V_{no} \tag{4.3}$$

where $V_{\mathrm{ao/bo/co}}$ are phase to mid-point of DC link voltage and $V_{\mathrm{no}}$ is the common-mode voltage.

Figure 4.1 shows the phase voltage pulse patterns in Prism I under conventional 3-D SVM. The phase voltage levels of each phase are calculated based on Eq. (4.3). There are all together 7 voltage levels for each phase. Since the calculation takes the squared value, therefore the signs do not matter. The sum of the squared mean value of the three voltages is thus given by

$$(\Delta V_{a,eff}^2 + \Delta V_{b,eff}^2 + \Delta V_{c,eff}^2)T_{PWM}/2 = \int_0^{tE} V_a^2 dt + \int_0^{tE} V_b^2 dt + \int_0^{tE} V_c^2 dt \approx \frac{3}{4} t_E V_{DC}^2 \tag{4.4}$$

where $t_{\mathrm{E}}$ is the effective turn-on time. Eq. (4.4) shows that the sum of the squared mean value of the three phase voltages is proportional to the effective turn-on time of the converter. The distortion phase voltage should be kept as small as possible.

Over one power cycle, the average value of the effective phase voltage can be obtained by Eq. (4.5), notice $N$ is the number of calculation in one 60° section, and $N=2q/6$.

$$3V_{eff}^2 = V_{a,eff}^2 + V_{b,eff}^2 + V_{c,eff}^2 = \frac{3}{4}V_{DC}^2 \frac{1}{NT_{PWM}/2}\sum_N t_E = \frac{3}{4}V_{DC}^2 \frac{1}{N}\sum_N \frac{2t_E}{T_{PWM}} \tag{4.5}$$

Since the RMS per-phase values are the same, Eq. (4.6) gives the equation for RMS per-phase value:

$$V_{a/b/c,eff} = \sqrt{\frac{1}{3}\frac{3}{4}V_{DC}^2 \frac{1}{N}\sum_N \frac{2t_E}{T_{PWM}}} = \frac{1}{2}V_{DC}\sqrt{\frac{1}{N}\sum_N \frac{2t_E}{T_{PWM}}} \tag{4.6}$$

The effective turn-on time of the converter during half PWM cycle can be calculated based on Figure 4.1 and it is given by

$$t_E = t_1 + t_2 + t_3 = \frac{T_{PWM}}{2}\frac{V_{ao,ref} - V_{co,ref}}{V_{DC}} = \frac{\sqrt{3}}{2}M\frac{T_{PWM}}{2}\sin(\omega t + \frac{\pi}{3}) \tag{4.7}$$

where $t_{1/2/3}$ are duration time relating to the switching vectors of $\vec{V}_{1/2/3}$ and $V_{ao,ref}$ and $V_{co,ref}$ are the reference phase voltage signals. Also shown in the figure, $t_z$ is the duration time relating to the zero space vector $\vec{V}_z$.

Because the sampled PWM length is small, therefore the summation in Eq. (4.5) and (4.6) can be replaced by an integral and one can have

$$\frac{1}{N}\sum_N \frac{2t_E}{T_{PWM}} \approx \frac{\sqrt{3}}{2}M\left[\frac{1}{\pi/3}\int_0^{\pi/3}\sin(\omega t + \frac{\pi}{3})d\omega t\right] = \frac{3\sqrt{3}}{2\pi}M \tag{4.8}$$

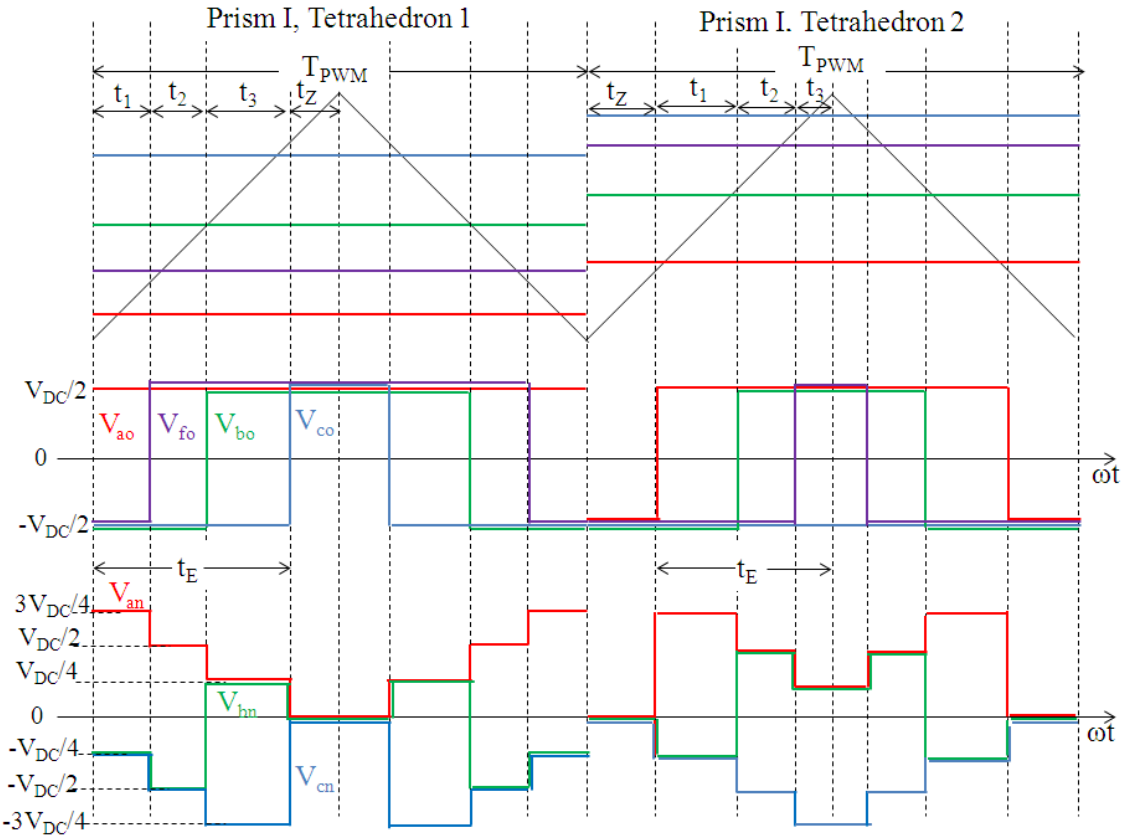



Figure 4.1 Switch pulse pattern of phase voltages( $V_{an}$, $V_{bn}$, $V_{cn}$) under conventional 3-D SVM while reference vector lies in [0,60°]

Combined Eq. (4.6) with Eq. (4.8) yields the per-phase RMS voltage

$$V_{a/b/c,eff} \approx V_{DC}\sqrt{\frac{3\sqrt{3}}{8\pi}M} \tag{4.9}$$

As explained before, the maximum per-phase modulation index value $M$ equals $2/\sqrt{3}$, so the maximum per-phase RMS voltage value is

$$V_{a/b/c,eff,Max} \approx V_{DC}\sqrt{\frac{3}{4\pi}} = 0.4886V_{DC} \tag{4.10}$$

The per-phase RMS voltage value is only related to the per-phase modulation index value as it can be seen from Eq. (4.9) with the maximum value of $0.4886V_{DC}$ (Eq. (4.10)).

The per-phase fundamental voltage value is given by

$$V_{ph,\ fundamental} = \frac{1}{\sqrt{2}}\frac{V_{DC}}{2}M \tag{4.11}$$

The voltage harmonic distortion factor $k_V$ can therefore be calculated as

$$k_V = \frac{\sqrt{V_{ph,eff}^2 - V_{ph,\ fundamental}^2}}{V_{ph,eff}} = \sqrt{1 - M\frac{\sqrt{3}\pi}{9}} \tag{4.12}$$

According to Eq. (4.12), the voltage harmonic distortion factor $k_V$ is in the range of [0.549 1], with the maximum value at $M$=0 and minimum value at $M$=$2/\sqrt{3}$.

### 4.1.2 Near-sate 3-D SVM

The calculation of the voltage harmonic distortion factor for the near-state 3-D SVM can be done based on the same analysis progress, except in the near-state 3-D SVM, the voltage level and effective turn-on time of the converter are different. This can be seen in Figure 4.2 which shows the phase voltage pulse patterns in Section I and II under near-state 3-D SVM switching scheme. There are all together 6 voltage levels for each phase (the zero voltage state is missing in this case). Because the phase voltage level within one PWM cycle is the same as 3-D SVM, Eq. (4.6) can be used to calculate the per-phase RMS voltage value. The difference here, as it can be seen from Figure 4.2, is for near-state 3-D SVM, the effective turn-on time is exactly half of the PWM cycle time. Therefore the RMS per-phase voltage value is calculated as

$$V_{a/b/c,eff} = \sqrt{\frac{1}{3}\frac{3}{4}V_{DC}^2\frac{1}{N}\sum_{N}\frac{2t_E}{T_{PWM}}} = \frac{1}{2}V_{DC} \tag{4.13}$$

As it can be seen from Eq. (4.13), instead of relating to the per-phase modulation index value, the RMS per-phase voltage value under the near-state 3-D SVM is fixed at $V_{DC}/2$.

The voltage harmonic distortion factor can therefore be calculated as

$$k_V = \frac{\sqrt{V_{ph,eff}^2 - V_{ph,fundamental}^2}}{V_{ph,eff}} = \sqrt{1-\frac{1}{2}M^2} \tag{4.14}$$

It should be noted that the per-phase modulation index value $M$ in this case is in the range of [0.77 1.155] due to the limiting operational range of the near-state 3-D SVM.

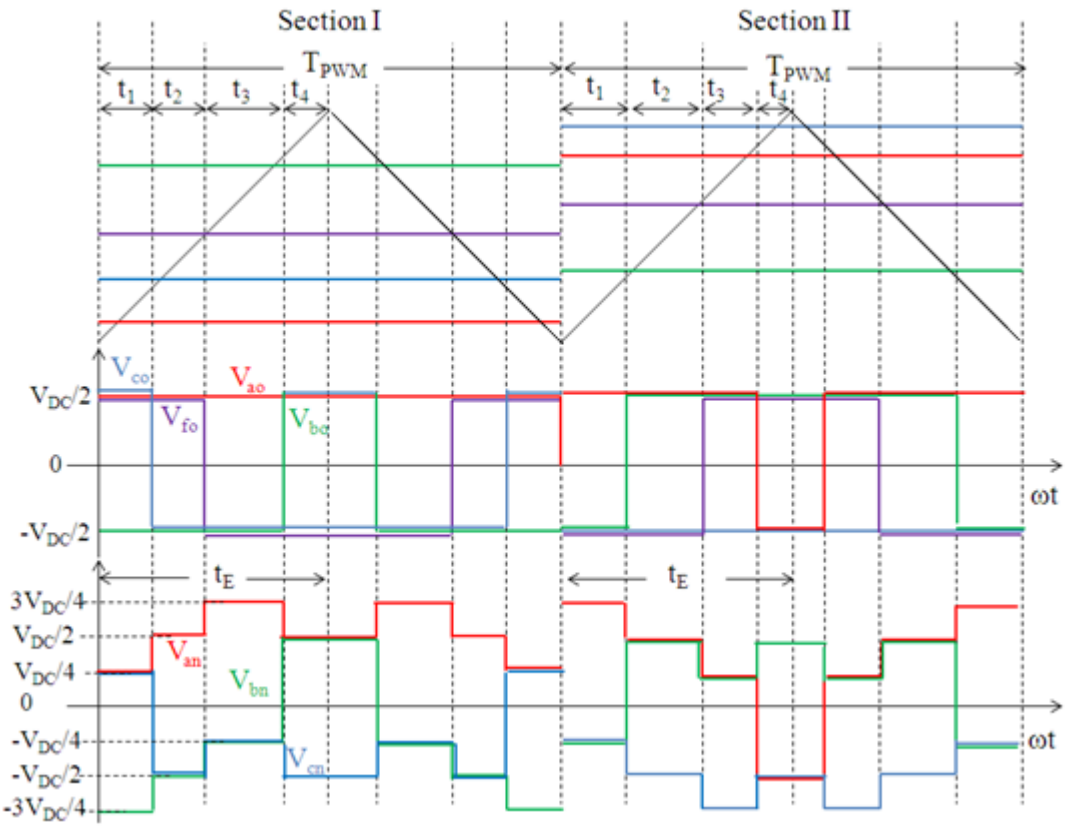



Figure 4.2 Switch pulse pattern of phase voltages( $V_{an}$, $V_{bn}$, $V_{cn}$) under the near-state 3-D SVM while reference vector lies in [0,60°]

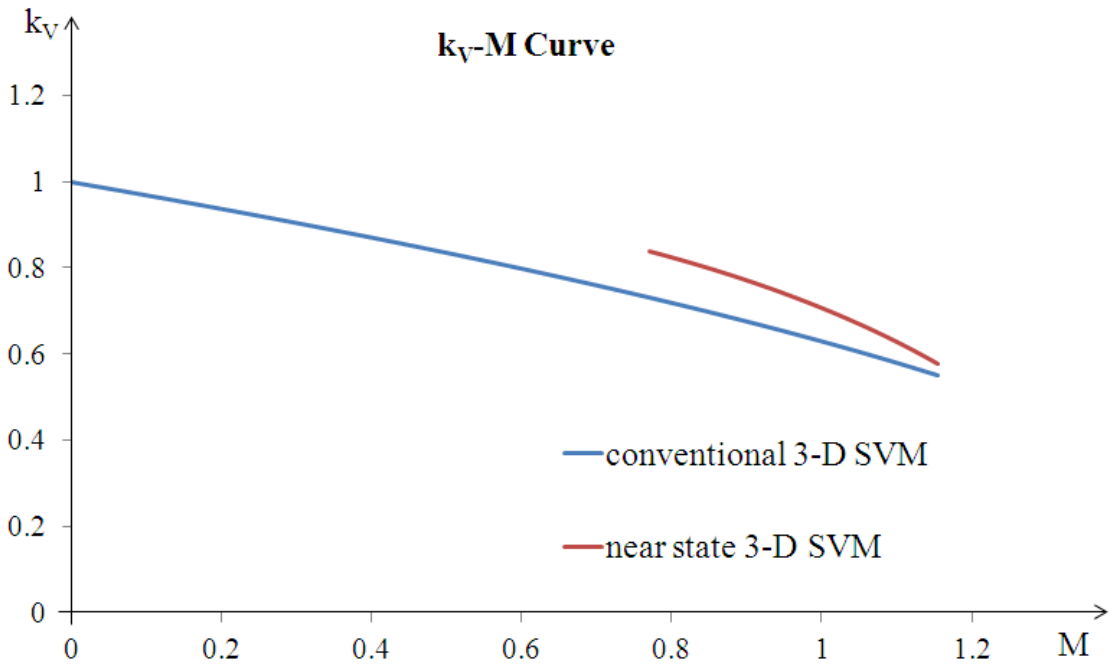



Figure 4.3 The voltage harmonic distortion factor under two different switching schemes

Figure 4.3 shows the voltage harmonic distortion factor under two different switching schemes, namely conventional 3-D SVM and near-state near-state 3-D SVM. This curve is named as $k_V$-$M$ curve. It could be seen that the near-state 3-D SVM has slightly higher voltage distortion factor than that of conventional 3-D SVM, which validates the experimental results when the two switching schemes are compared in Chapter 3. Also it can be seen that as the modulation index value increases, the voltage harmonic distortion factor of the two switching schemes are getting closer. When the per-phase modulation index $M$ exceeds unity, the difference of the voltage distortion factor for the two different switching schemes becomes relatively small; therefore this is the suggested operating range for the near-state 3-D SVM operation.

## 4.2 Inductor current harmonic distortion factor

To calculate the RMS value of the inductor harmonic current is not easy, even for a three-phase three-leg VSI [36, 80]. For a three-phase four-leg VSI, since it is used for unbalanced or nonlinear load condition most of the time, the output three-phase current are unbalanced or distorted. This makes the analysis on the current harmonic distortion factor even more difficult.

The calculation of the current harmonic distortion factor has been seen on a three-phase machine drive VSI [36, 55, 56, 60, 61, 80, 82], and the calculation always assumes that the inductor current is the current that goes through the machine winding. While in the case of a three-phase four-leg VSI, an *L*-*C* filter has been used to filter out much of the switching ripples on the inductor current, so the filtered output phase load current harmonic distortion shows the same trait as the $k_V$-*M* curve .

However, the inductor current harmonic distortion factor is a very important index for the power quality of the voltage source converter and the conduction loss and switching loss of the power electronics devices are strongly linked to the inductor current quality[60, 82]. Therefore it is of great interest to investigate the current harmonic distortion factor based on the inductor current instead of the load current for different switching schemes that are applied on a three-phase four-leg inverter.

The analysis is based on the following assumptions;

- The reference phase-to-neutral voltage $V_{ao,ref}$, $V_{bo,ref}$ and $V_{co,ref}$ are set at the beginning of each PWM sample and they remain piecewise constant during one PWM cycle.
- The sampled output voltages $V_{AG/BG/CG}$ are constant within one PWM sample, and they correspond to the phase voltage levels of $V_{an/bn/cn}$ without the fundamental current component.
- The analysis is based on three-phase balanced load condition; the situation in unbalanced load condition will also be briefly discussed at the end of this section.

With these assumptions, considering the large average signal model in Figure 2.27, the RMS value of the current distortion for each phase can be calculated as

$$\Delta I_{La/b/c} = \frac{1}{L}\int_0^{T_{PWM}/2}(V_{an/bn/cn} - V_{AG/BG/CG})dt \tag{4.15}$$

The output voltages are represented as in Eq. (4.16), where $\Delta\varphi$=0,-2π/3, +2π/3 for each phase respectively, and $V_{an/bn/cn}$ is the actual PWM phase voltage level and they depend on the switching scheme that has been chosen (see Figure 4.1 for conventional 3-D SVM and Figure 4.2 for near-state 3-D SVM),

$$V_{AG/BG/CG} = \frac{V_{DC}}{2} M\cos(\omega t + \Delta\varphi_{A/B/C}) \tag{4.16}$$

The squared RMS value of all three phase current distortion can thus be obtained

$$3\Delta I_{L\,a/b/c,distortion}^2 \frac{T_{PWM}}{2} = \int_0^{T_{PWM}/2} \Delta I_{La}^2 dt + \int_0^{T_{PWM}/2} \Delta I_{Lb}^2 dt + \int_0^{T_{PWM}/2} \Delta I_{Lc}^2 dt \tag{4.17}$$

Here, although the phase currents for each phase shown in (4.17) are approximated as linear, the integration of squared value of each phase current distortion in each switching state is very complicated. It is also noted that for different switching schemes, the on-time of each switching state are different, the on time $t_{1/2/3/Z}$ for conventional 3-D SVM and $t_{1/2/3/4}$ for near-state 3-D SVM will be given later.

So the calculation depends on the PWM phase voltage level and the duration time of each switching state within one PWM cycle. It was mentioned earlier that the calculation could be simplified by just calculating π/3 interval, since the three phase voltage waveform repeat every 60°, the calculation could be simplified as Eq. (4.18), with $\Delta\omega t=2\pi T_{PWM}/T_1=2\pi/(6N)$,

$$3\Delta I_{L\,a/b/c,distortion}^2 = \frac{1}{N}\sum_{k=1}^{N} 3\Delta I_{distortion}^2(k\Delta\omega t) \tag{4.18}$$

The squared per-phase current harmonic distortion can then be represented as

$$\Delta I_{L\,a/b/c,distortion}^2 = \frac{1}{N}\sum_{k=1}^{N} \Delta I_{distortion}^2(k\Delta\omega t) = \frac{3}{\pi}\sum_{k=1}^{N} \Delta I_{distortion}^2(\frac{k}{N}\frac{\pi}{3})(\Delta\omega t) \tag{4.19}$$

$\Delta\omega t$ can be viewed relatively small enough relative to the period of a fundamental power cycle, therefore Eq. (4.19) can be replaced by Eq. (4.20)

$$\Delta I_{L\,a/b/c,distortion}^2 = \frac{3}{\pi}\int_0^{\pi/3} \Delta I_{distortion}^2(\omega t)d(\omega t) \tag{4.20}$$

### 4.2.1 Conventional 3-D SVM

As it was mentioned before, for different switching schemes, the effective duration time of the switching states in one PWM cycle are different and also the per-phase PWM voltage levels are different as well. Therefore, the current harmonic distortion factor would be different. The angular range of [-π/6 π/6] is selected to make the calculation.

For conventional 3-D SVM, either Tetrahedron 2 in Prism VI or Tetrahedron 1 in Prism I can be selected in the calculation and they will lead to the same result. Here, Tetrahedron 1 in Prism I is selected. The per-phase PWM voltage level in Eq. (4.15) can

be read from Figure 4.1, and the duration time of each switching state can be found in Eq. (4.21), the detailed procedure to obtain the duration time can be found in Appendix D.

$$\begin{aligned} t_1 &= \frac{M}{2}\cos(\omega t)\times\frac{T_{PWM}}{2} \\ t_2 &= -\frac{M}{2}\cos(\omega t-2\pi/3)\times\frac{T_{PWM}}{2} \\ t_3 &= [\frac{M}{2}\cos(\omega t-2\pi/3)-\frac{M}{2}\cos(\omega t+2\pi/3)]\times\frac{T_{PWM}}{2} \\ t_Z &= [1-\frac{\sqrt{3}}{2}M\cos(\frac{\pi}{6}-\omega t)]\times\frac{T_{PWM}}{2} \end{aligned} \tag{4.21}$$

Therefore, the resultant RMS value of the per-phase current distortion can be obtained

$$\Delta I^2_{La/b/c,distortion} \approx \frac{V_{DC}}{L}T_{PWM}\sqrt{T_{PWM}}M\sqrt{0.0052-0.008M+0.0033M^2} \tag{4.22}$$

Here we define $I_B$ as the current harmonic distortion factor and its value for conventional 3-D SVM is expressed as

$$I_B = M\sqrt{0.0052-0.008M+0.0033M^2} \tag{4.23}$$

### 4.2.2 Near-state 3-D SVM

For near-state 3-D SVM, Section I is selected to do the analysis. The per-phase PWM voltage level could be seen in Figure 4.2, and the duration times of each switching state are given by

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} [1-\frac{\sqrt{3}}{2}M\cos(\frac{\pi}{6}-\omega t)]\frac{T_{PWM}}{2} \\ \frac{1}{2}M\sin(\frac{\pi}{6}+\omega t)\frac{T_{PWM}}{2} \\ [-1+\frac{3}{2}M\cos(\omega t)-\frac{1}{2}M\sin(\frac{\pi}{6}+\omega t)]\frac{T_{PWM}}{2} \\ [1-\frac{\sqrt{3}}{2}M\cos(\frac{\pi}{6}+\omega t)]\frac{T_{PWM}}{2} \end{bmatrix} \tag{4.24}$$

Again the detailed calculation could be found in Appendix E.

The per-phase RMS current distortion can be given by

$$\Delta I^2_{L\,a/b/c,distortion} \approx \frac{V_{DC}}{L}\sqrt{T^3_{PWM}}\sqrt{-0.0052+0.02176M-0.0179M^2-0.00085M^3+0.0033M^4} \tag{4.25}$$

The current harmonic distortion factor $I_B$ for near-state 3-D SVM can hence be obtained

$$I_B = \sqrt{-0.0052+0.02176M-0.0179M^2-0.00085M^3+0.0033M^4} \tag{4.26}$$

Figure 4.4 shows the inductor current harmonic distortion factor per-phase modulation index curve for the two different switching schemes. For the conventional 3-D SVM, the current harmonic maintains a certain level (around 0.02) when the per-phase modulation index exceeds 0.6, while the current harmonic content of the near-state 3-D SVM decreases as the per-phase modulation index $M$ increases. This shows quite similar characteristics as the $k_V$-$M$ curve, except the fact that the current harmonic content for near-state 3-D SVM at low modulation index range is high, suggesting that the recommended operational range of the near-state 3-D SVM is around unity.

Although the current harmonic distortion factor of the near-state 3-D SVM is higher than the conventional 3-D SVM, the analysis is based on the inductor current as it was mentioned earlier. The filtered phase load current quality will depend purely on the voltage harmonic factor, so the actual filtered current harmonics distortion factor would show similar feature as the $k_V$-$M$ curve.

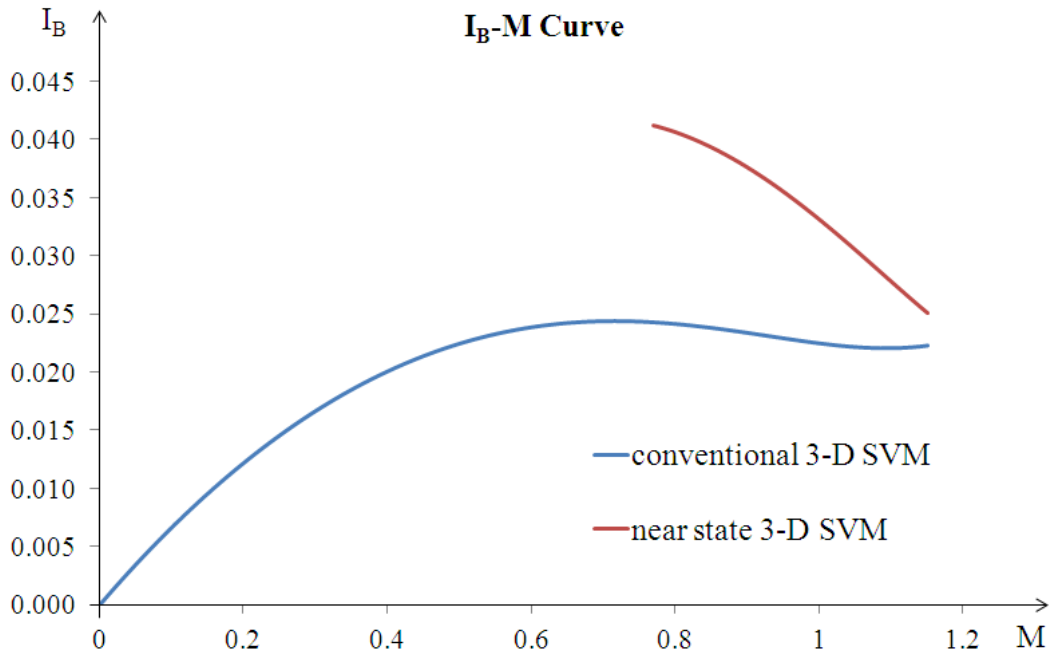



Figure 4.4 The inductor phase current harmonic distortion factor under two different switching schemes

The unbalanced current harmonic distortion factor is difficult to calculate for the simple reason that the currents are unbalanced. Although the output phase voltages are maintained as three-phase balanced output, the generated per-phase PWM voltage waveforms will depend on the varying unbalanced load condition. However, for the same unbalanced load condition, the inductor current waveforms, although unbalanced, still shows the similar trait as in the balanced load condition. Therefore, the $I_B$-$M$ curve can still be used as a useful guidance to estimate the inductor current harmonic distortion.

## 4.3 Conduction loss

The conduction loss and the switching loss of the power electronics devices are strongly linked to the modulation index waveform and the inductor current of the VSI [37, 60, 82]. The selection of the power electronics rating and especially the size of the heat sink also depend on the inductor current of the inverter. Higher current harmonic content can result in more loss dissipated on the heat sink; necessitating a larger or forced-cooled heat sink [86].

Since the analysis of the inductor current harmonic distortion factor for a four-leg VSI has already been introduced in the previous section. To distinguish the conduction loss between the two switching schemes would not be difficult. Here, we still assume that the load condition is balanced; hence the neutral current that goes through the fourth leg is almost zero with just switching ripples.

In [60], it is found that the calculation of the conduction loss can always be approximated with an accuracy. Analysis of conduction loss for different inverter topologies are shown in [57] and expressions of the calculation are given.

According to [57, 60], the expressions for conduction loss are related to the modulation index waveform, the phase angle between the fundamental phase voltage and the phase current. The calculation is based on the assumption that the load current is sinusoidal[57], therefore the modulation index waveform decides the conduction loss if the load has the same power factor for different switching schemes.

The calculation can be divided into two parts; first part is based on the modulation index waveform of the switching scheme and the fundamental per-phase current that is assuming that the phase current is purely sinusoidal without any harmonic content or

switching ripples. The second part of the calculation is associated with the harmonic content due to the switching ripples of the phase current. It has been found that the second part only marginally influenced the conduction loss of the inverter[60].

The modulation index or the reference phase voltage can be written as

$$V_{ao,\,ref} = \begin{cases} \frac{V_{DC}}{2}, & 0 \le \omega t < \frac{\pi}{6}, \frac{11\pi}{6} \le \omega t < 2\pi \\ V_{DC}\frac{\sqrt{3}}{2} M \cos(\omega t - \frac{\pi}{6}) - \frac{V_{DC}}{2}, & \frac{\pi}{6} \le \omega t < \frac{\pi}{2} \\ V_{DC}\frac{\sqrt{3}}{2} M \cos(\omega t + \frac{\pi}{6}) + \frac{V_{DC}}{2}, & \frac{\pi}{2} \le \omega t < \frac{5\pi}{6} \\ -\frac{V_{DC}}{2}, & \frac{5\pi}{6} \le \omega t < \frac{7\pi}{6} \\ V_{DC}\frac{\sqrt{3}}{2} M \cos(\omega t - \frac{\pi}{6}) + \frac{V_{DC}}{2}, & \frac{7\pi}{6} \le \omega t < \frac{3\pi}{2} \\ V_{DC}\frac{\sqrt{3}}{2} M \cos(\omega t + \frac{\pi}{6}) - \frac{V_{DC}}{2}, & \frac{3\pi}{2} \le \omega t < \frac{11\pi}{6} \end{cases} \quad (4.27)$$

The modulation index waveform of the near-state 3-D SVM is different from the conventional 3-D SVM in two sections where the switch patterns need to change. The effect of the on-time of each power electronics device for both switching schemes are found to be almost the same as shown in Figure 4.5. The only difference occurs during the transient state between the sections when the switch patterns need to change, where only 2 PWM cycles have been affected during the transient. Therefore the effect can be neglected. The gate drive signals for phase A under both switching schemes are shown in Figure 4.6.

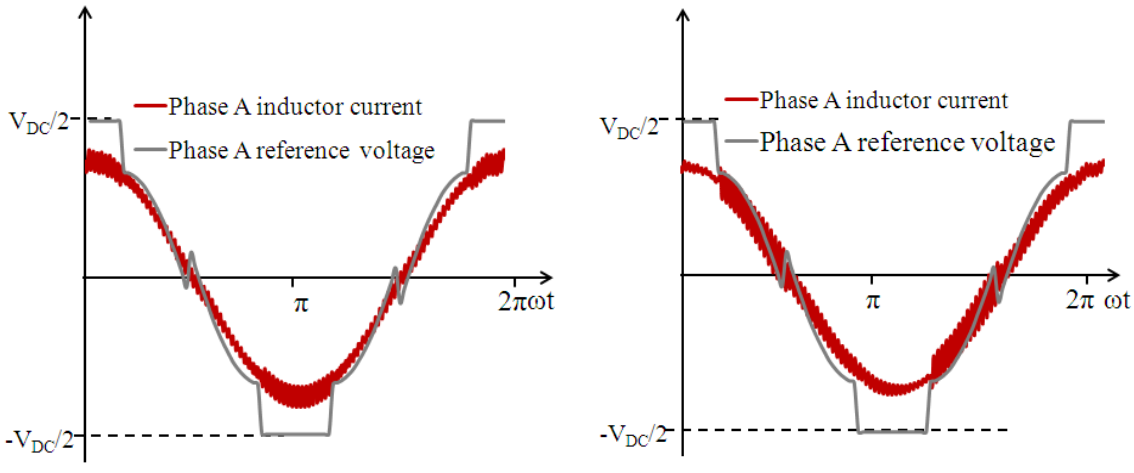



Figure 4.5 Phase A reference voltage waveform and the inductor current waveform, unity power factor, (a) conventional 3-D SVM, (b) near-state 3-D SVM

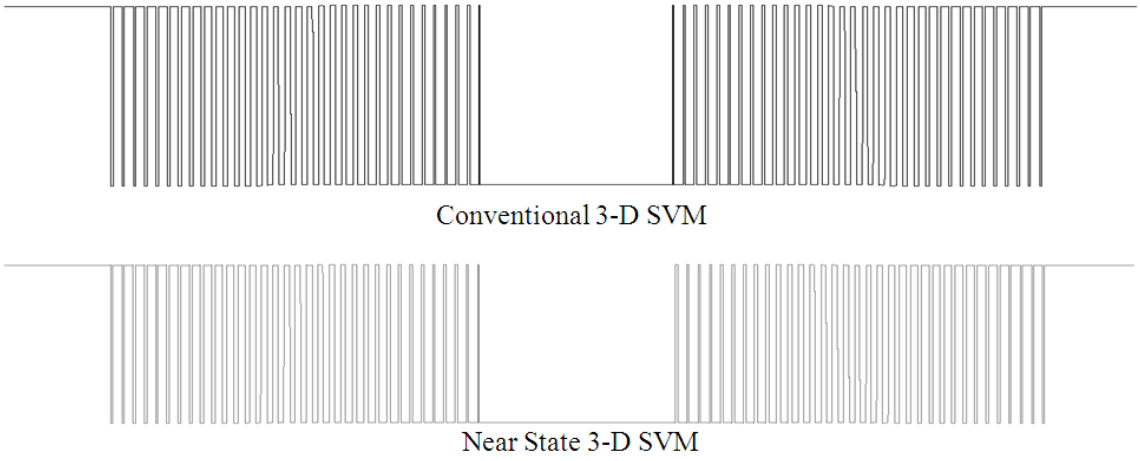



Figure 4.6 Phase A Gate drive signals over one power cycle; top, conventional 3-D SVM, bottom, near-state 3-D SVM

The calculation of the conduction loss based on the modulation waveform for both switching schemes are shown to be the same, here, only the result is shown, more details regarding the calculation can be found in Appendix F.

Assume that the phase angle $\varphi$ between the reference phase voltage and phase current is within the range of [0, π/6], which is the design specification of power factor. The power loss that is dissipated on transistor $T_1$ is given by Eq. (4.28) and the power loss on diode $D_2$ is given by Eq. (4.29)

$$P_{T_1} = \frac{V_T I_a}{2\pi}(1+\frac{\pi}{4}M\cos\varphi) + \frac{R_T I_a^2}{4\pi} \times[\frac{\pi}{3}+\varphi+(1-\frac{2M}{\sqrt{3}})\cos(\frac{\pi}{6}+2\varphi)+\frac{4M}{\sqrt{3}}\cos(\frac{\pi}{6}+\varphi)] \tag{4.28}$$

$$P_{D_2} = \frac{V_D I_a}{2\pi}(1-\frac{\pi}{4}M\cos\varphi) + \frac{R_D I_a^2}{4\pi} \times[\frac{2\pi}{3}-\varphi+(1-\frac{2M}{\sqrt{3}})\cos(\frac{\pi}{6}+2\varphi)-\frac{4M}{\sqrt{3}}\cos(\frac{\pi}{6}+\varphi)] \tag{4.29}$$

where $V_T$ and $V_D$ are the constant voltage over the transistor and diode, respectively, and $R_T$ and $R_D$ are the resistance across the transistor and diode, respectively.

The total conduction loss of the inverter under balanced load condition is

$$P_{conduction} = 6(P_{T1} + P_{D2}) \tag{4.30}$$

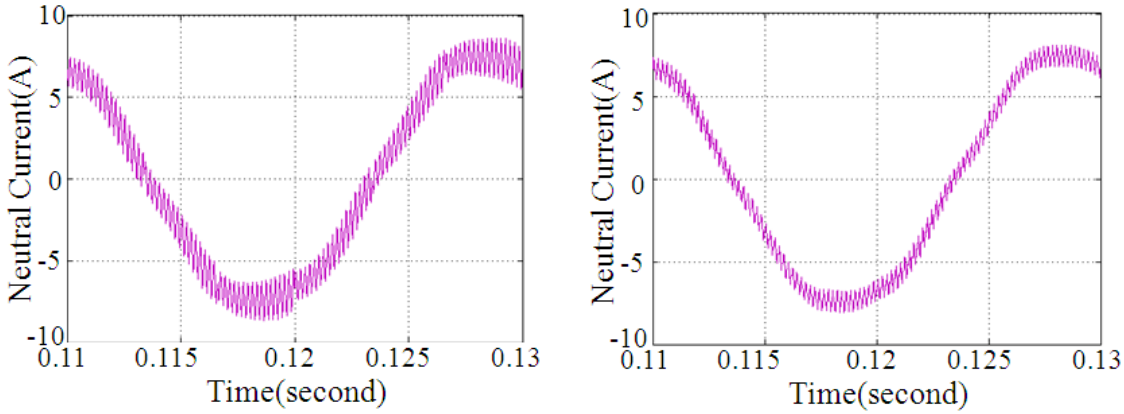
So the conduction loss analysis based on the modulation index waveforms, or more precisely, the on-time of the power electronics devices show that both switching schemes have the same conduction loss if the load current waveform is purely sinusoidal without the harmonic content or switching ripples.

However, the per-phase inductor currents show different harmonic content for both switching schemes which means the power loss due to the phase current harmonic content will be different. In this case, the $I_B$-$M$ curve can be used to analyze the power loss difference between the two switching schemes.

Therefore it can be concluded that the conduction loss of the near-state 3-D SVM is marginally higher than that of the conventional 3-D SVM due to the difference of the phase current harmonic content between the two different switching schemes.

Under unbalanced load condition, the neutral current will be flowing through the fourth leg, and depends on the unbalanced load condition, the amplitude and phase of the neutral current will be different.

Take the situation where one of the phases is unloaded, Figure 4.7 shows the neutral current under both switching schemes. It can be seen that the fundamental component of the neutral current under both schemes are exactly the same with amplitude and phase shift. However, the switching ripples of the near-state 3-D SVM is high than that of conventional 3-D SVM. Hence the difference of conduction loss of the fourth leg will also depend on the harmonic content of the neutral current; therefore $I_B$-$M$ curve can still be used to analyze the difference of the conduction loss between the two switching schemes under unbalanced load condition. It should also be noted that for this project, the neutral inductance and fourth-leg IGBTs are selected as the same rating as the other three phases, therefore the extra switching ripple of the proposed switching scheme brings is not an issue. More switching ripple potentially will create more heat in the fourth wire; therefore bigger inductance value may be needed to reduce the switching ripple and that is one of the drawbacks of the proposed switching scheme.




(a) (b)

Figure 4.7 Simulated neutral current in the fourth leg when one phase is unloaded, (a) conventional 3-D SVM, (b) near-state 3-D SVM

## 4.4 Switching loss

The calculation of the switching loss of the three-phase three-leg VSI has been covered in the literature review part. Since the effective on-time of the power electronics devices for each phase under different switching schemes has been found to be the same from the previous section, the calculation of the switching loss based on the fundamental phase voltage would be the same for both switching schemes. The relative switching loss function RSL has been introduced in Chapter 2 and the expressions are given by Eq. (2.33)-(2.36).

In the case of four-leg VSI, the total switching loss of the inverter under balanced load condition is

$$\begin{aligned} P_{switching} &= 3\times\frac{V_{DC}(t_{off}-t_{on})}{T_s}\times\frac{1}{\pi}\times\hat{I}_L\times[\int_0^{\frac{\pi}{3}-\varphi}\sin(\omega t)d\omega t+\int_{\frac{2\pi}{3}-\varphi}^{\pi}\sin(\omega t)d\omega t] \\ &= 3\times\frac{V_{DC}(t_{off}-t_{on})}{T_s}\times\frac{1}{\pi}\times\hat{I}_L\times[2-\cos(\frac{\pi}{3}-\varphi)+\cos(\frac{2\pi}{3}-\varphi)] \end{aligned} \tag{4.31}$$

So the relative switching loss *RSL* is

$$RSL = P_{switching}/\sum P_0 = \frac{1}{2}\times[2-\cos(\frac{\pi}{3}-\varphi)+\cos(\frac{2\pi}{3}-\varphi)] \tag{4.32}$$

Under balanced load condition, the RSL as a function of power factor angle $\varphi$ is plotted in Figure 4.8. It is worth noting that the power factor of the three-phase load has been taken into consideration for the calculation, the figure shows the *RSL* when the load power factor changes from 0.8 lagging to 0.8 leading, which is the design specification.

Unbalanced load conditions vary from load power unbalance to load power factor unbalance[49], and sometimes they are mixed. Also, under unbalanced situation, a neutral current is flowing through the fourth leg and this current varies depending on the different load conditions. It has been found that with 33% specified zero-sequence unbalance; the neutral current is the same as the rated per-phase current.

Figure 4.9 shows the *RSL* under two cases of unbalanced load condition. In the case of unbalanced power, phase C is loaded from full load to no load. For unbalanced power factor case, the power factor of phase C ranges from 0.8 lagging to 0.8 leading. The calculation involved is quite complicated, again, the detailed calculation will be found in the Appendix G.

As expected, the calculations based on the modulation index waveform for both the switching schemes are shown to be the same under balanced and unbalanced load condition. The difference of the switching loss due to the harmonic content of the phase current depends on $I_B$-M curve and its effect is neglected for the switching loss analysis.

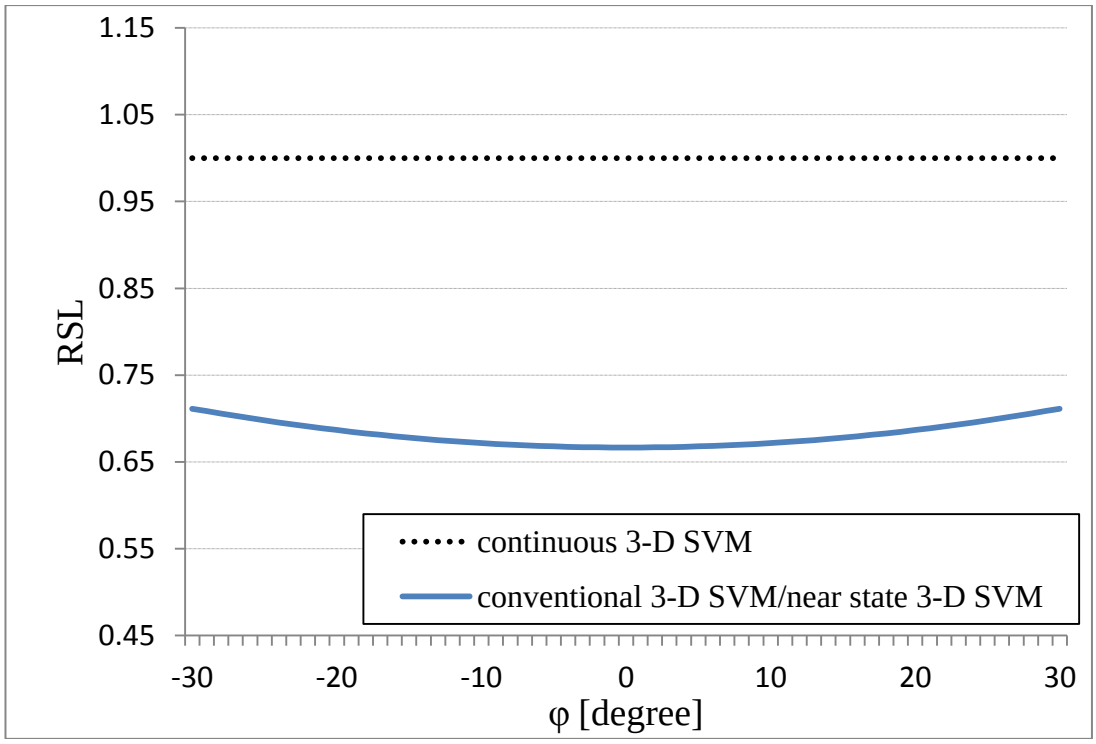



Figure 4.8 Relative switching loss *RSL* as a function of power factor angle $\varphi$

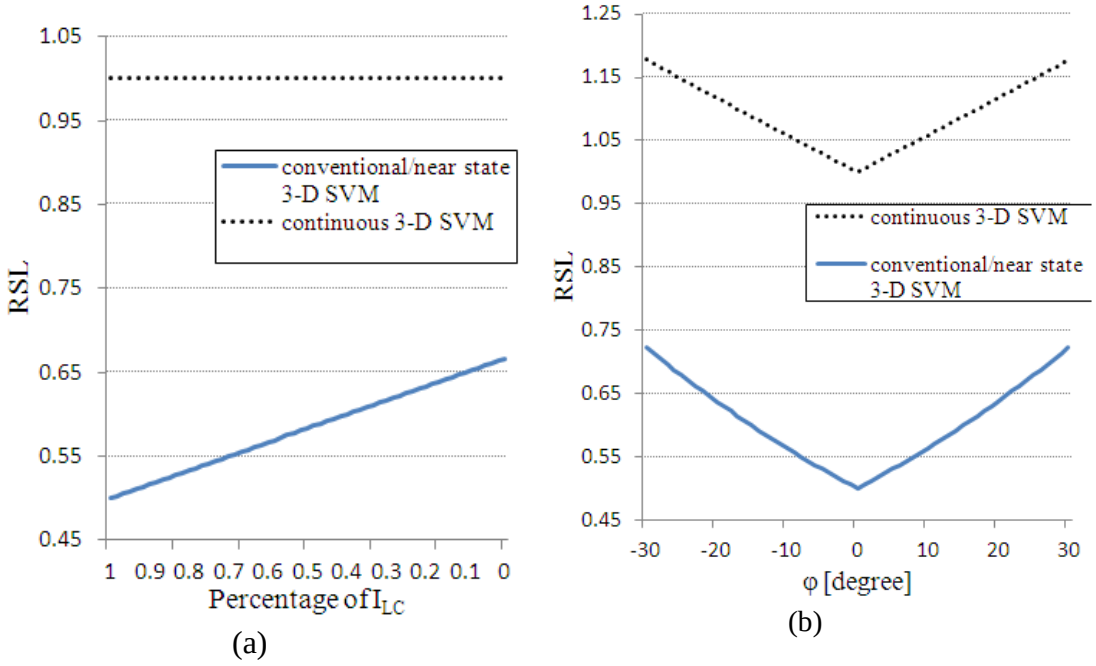



Figure 4.9 Relative switching loss *RSL* under unbalanced load condition; (a) case of unbalanced power, phase C from full load to no load (b) case of unbalanced power factor, power factor of phase C ranges from 0.8 lagging to 0.8 leading

## 4.5 Summary

In this chapter, an in-depth performance analysis is carried out for a three-phase four-leg VSI. A full comparison between the two switching schemes, namely near-state 3-D SVM and conventional 3-D SVM has been done based on the performance analysis.

The output voltage harmonic distortion factor without doubt is the most vital factor in terms of determining the output quality of the inverter. The output load current is also strongly related to the voltage harmonic distortion factor.

A $k_V$-$M$ curve is calculated and plotted to compare the harmonic distortion factor for the two different switching schemes. It is found that the near-state 3-D SVM has a higher voltage harmonic distortion than the conventional 3-D SVM. Also, as the modulation index increases, this difference is getting smaller, indicating a suitable operation modulation range for the near-state 3-D SVM.

Inductor current harmonic distortion factor is also very important for the performance analysis for the reason that the conduction loss and the switching loss of the inverter are related to the unfiltered phase current. An $I_B$-$M$ curve thus is plotted to show the difference between the two schemes. The $I_B$-$M$ curve shows quite similar feature as the

$k_V$-$M$ curve except at low modulation range, the difference of the harmonic content between the two schemes is much bigger at the low modulation range.

It has been found that for both the conduction loss and the switching loss, the analytical calculation equations have two parts, where the first part is related to the modulation index waveform of the switching scheme, and the second part is related to the harmonic current content only. The first part plays a major role in terms of the total loss, and it has been found for both the switching schemes, the loss calculations are the same. The second part of the calculation is associated with the inductor phase current harmonic content, which is hard to calculate.

So the conduction loss and switching loss between the two switching schemes are only marginally different due to the different current harmonic content, and this difference can be seen from the $I_B$-$M$ curve.

The performance analysis is based on three-phase linear balanced loads; the performance analysis under unbalanced load condition has been covered as well. The voltage harmonic distortion under unbalanced load condition shows the same characteristics as it is under balanced load condition. The difference of the conduction loss and switching loss between the two switching schemes under unbalanced load condition can still by analyzed and compared using the $I_B$-$M$ curve.

# Chapter 5
# Zero-sequence Component Injected PWM for Three-phase Four-Leg VSIs

Three-dimensional SVM has been proved to be most compatible with DSP implementation for a three-phase four-leg VSI [15, 18, 32, 51]. The carrier-based PWM switching schemes for four-leg inverters [13, 33], although easy to understand, generate the same modulation index waveforms as the 3-D SVM does. When it comes to control loop design, 3-D SVM has its advantage since the control model is based on the DC operating point in a *d-q-o* coordinate. However, the drawback of 3-D SVM is that the algorithm is difficult to understand and could also be a computational burden [33]. The relationship between the space vector modulation and the carrier based PWM has been fully studied in [35, 41] for a three-leg VSI. In [33], the authors have proved the carrier-based PWM is mathematically equivalent to the symmetrically aligned class I 3-D SVM. It seems from the literature survey, apart from these two available switching schemes, there has been little research done in finding another alternative switching scheme. A recent switching scheme which is called minimum-switching loss discontinuous PWM method achieves the minimum switching loss under different load conditions [14], it is also based on carrier-based PWM switching scheme.

In this chapter, a comprehensive analysis on the relationship between 3-D SVM and carrier-based PWM for a four-leg inverter is introduced. A zero-sequence component injected PWM switching scheme is thus introduced. The aim is to simplify the conventional 3-D SVM and near-state 3-D SVM algorithm, without abandoning the concept of a space vector, since most of the control designs are based on the space vector controls.

## 5.1 Decoupling the trajectory of reference voltage vector in *α-β-γ* coordinate

An unbalanced load current can be decomposed into positive, negative and zero-sequence current:

$$\begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \begin{bmatrix} I_{LA\_p} \\ I_{LB\_p} \\ I_{LC\_p} \end{bmatrix} + \begin{bmatrix} I_{LA\_n} \\ I_{LB\_n} \\ I_{LC\_n} \end{bmatrix} + \begin{bmatrix} I_0 \\ I_0 \\ I_0 \end{bmatrix} \tag{5.1}$$

The current in *A-B-C* coordinate can be transformed into *α-β-γ* coordinate by using:

$$\begin{bmatrix} I_{L\alpha} \\ I_{L\beta} \\ I_{L\gamma} \end{bmatrix} = T \begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = T \begin{bmatrix} I_{LA\_p} \\ I_{LB\_p} \\ I_{LC\_p} \end{bmatrix} + T \begin{bmatrix} I_{LA\_n} \\ I_{LB\_n} \\ I_{LC\_n} \end{bmatrix} + T \begin{bmatrix} I_0 \\ I_0 \\ I_0 \end{bmatrix} \tag{5.2}$$

where *T* is the Park transformation matrix in Eq. (2.14) and one has

$$\begin{bmatrix} I_{L\alpha} \\ I_{L\beta} \\ I_{L\gamma} \end{bmatrix} = \begin{bmatrix} I_{L\alpha\_p} \\ I_{L\beta\_p} \\ 0 \end{bmatrix} + \begin{bmatrix} I_{L\alpha\_n} \\ I_{L\beta\_n} \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ I_0 \end{bmatrix} \tag{5.3}$$

Hence the rotating reference vector on positive *α-β* coordinate, negative *α-β* coordinate and γ axis can be represented using:

$$\vec{I}_{L\_p} = I_{L\alpha\_p} + jI_{L\beta\_p} \tag{5.4}$$

$$\vec{I}_{L\_n} = I_{L\alpha\_n} - jI_{L\beta\_n} \tag{5.5}$$

$$\vec{I}_{L\_0} = I_0 = I_{L\gamma} \tag{5.6}$$

Comparing Eq. (5.4) and (5.5), it can be seen that the *β* element is lagging *α* element in the positive coordinate and leading *α* element in the negative *α-β* coordinate. It is shown in Eq. (5.6) that the zero-sequence component has no relationship with the *α-β* coordinate, it only affects γ element.

The same rule can apply for the reference rotating voltage vector, according to the large signal model of the system (Figure 2.27), the reference rotating voltage vector in *A-B-C* coordinate can be expressed in the following equations[18]:

$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} V_{af\_p} \\ V_{bf\_p} \\ V_{cf\_p} \end{bmatrix} + \begin{bmatrix} V_{af\_n} \\ V_{bf\_n} \\ V_{cf\_n} \end{bmatrix} + \begin{bmatrix} V_{af\_0} \\ V_{bf\_0} \\ V_{cf\_0} \end{bmatrix} \tag{5.7}$$

where $V_{xf\_p}$(x=a, b, c) is the positive-sequence reference voltage and it can be expressed [19]

$$\begin{bmatrix} V_{af\_p} \\ V_{bf\_p} \\ V_{cf\_p} \end{bmatrix} = \begin{bmatrix} L(d\frac{I_{LA\_p}}{dt} + Cd^2\frac{V_{AG}}{dt^2}) + V_{AG} \\ L(d\frac{I_{LB\_p}}{dt} + Cd^2\frac{V_{BG}}{dt^2}) + V_{BG} \\ L(d\frac{I_{LC\_p}}{dt} + Cd^2\frac{V_{CG}}{dt^2}) + V_{CG} \end{bmatrix} \tag{5.8}$$

The negative-sequence reference voltage is

$$\begin{bmatrix} V_{af\_n} \\ V_{bf\_n} \\ V_{cf\_n} \end{bmatrix} = L\begin{bmatrix} d\frac{I_{LA\_n}}{dt} \\ d\frac{I_{LB\_n}}{dt} \\ d\frac{I_{LC\_n}}{dt} \end{bmatrix} \tag{5.9}$$

The zero-sequence reference voltage is

$$\begin{bmatrix} V_{af\_0} \\ V_{bf\_0} \\ V_{cf\_0} \end{bmatrix} = (L + 3L_n)\begin{bmatrix} d\frac{I_0}{dt} \\ d\frac{I_0}{dt} \\ d\frac{I_0}{dt} \end{bmatrix} \tag{5.10}$$

Substitution of Eq. (5.2) and (5.3) into Eq. (5.8)-(5.10) yields the reference rotating voltage vector in $\alpha$-$\beta$-$\gamma$ coordinate

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \\ V_{\gamma} \end{bmatrix} = \begin{bmatrix} V_{\alpha\_p} \\ V_{\beta\_p} \\ V_{\gamma\_p} \end{bmatrix} + \begin{bmatrix} V_{\alpha\_n} \\ V_{\beta\_n} \\ V_{\gamma\_n} \end{bmatrix} + \begin{bmatrix} V_{\alpha\_0} \\ V_{\beta\_0} \\ V_{\gamma\_0} \end{bmatrix} \tag{5.11}$$

Where the positive-sequence reference voltage in $\alpha$-$\beta$-$\gamma$ coordinate is

$$\begin{bmatrix} V_{\alpha\_p} \\ V_{\beta\_p} \\ V_{\gamma\_p} \end{bmatrix} = \begin{bmatrix} L(d\dfrac{I_{L\alpha\_p}}{dt} + Cd^2\dfrac{V_\alpha}{dt^2}) + V_\alpha \\ L(d\dfrac{I_{L\beta\_p}}{dt} + Cd^2\dfrac{V_\beta}{dt^2}) + V_\beta \\ 0 \end{bmatrix} \tag{5.12}$$

The negative-sequence reference voltage in *α*-*β*-*γ* coordinate is

$$\begin{bmatrix} V_{\alpha\_n} \\ V_{\beta\_n} \\ V_{\gamma\_n} \end{bmatrix} = \begin{bmatrix} Ld\dfrac{I_{L\alpha\_n}}{dt} \\ Ld\dfrac{I_{L\beta\_n}}{dt} \\ 0 \end{bmatrix} \tag{5.13}$$

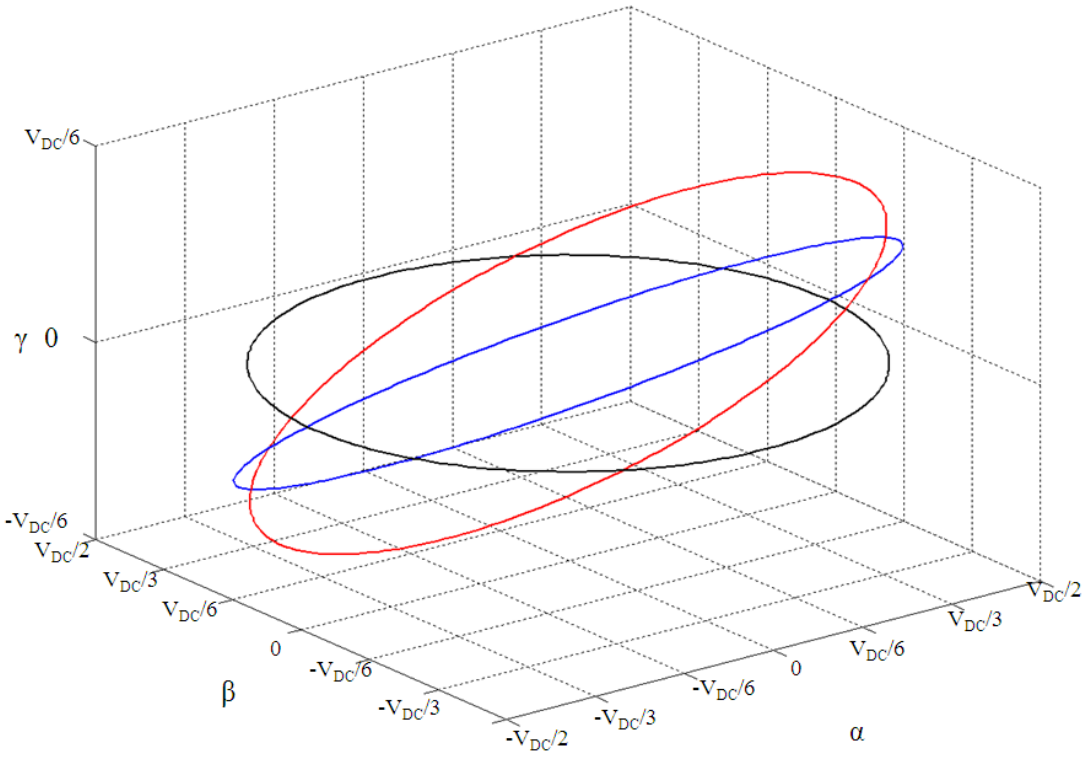
The zero-sequence reference voltage in *α*-*β*-*γ* coordinate is

$$\begin{bmatrix} V_{\alpha\_0} \\ V_{\beta\_0} \\ V_{\gamma\_0} \end{bmatrix} = (L + 3L_n)\begin{bmatrix} 0 \\ 0 \\ d\dfrac{I_0}{dt} \end{bmatrix} \tag{5.14}$$

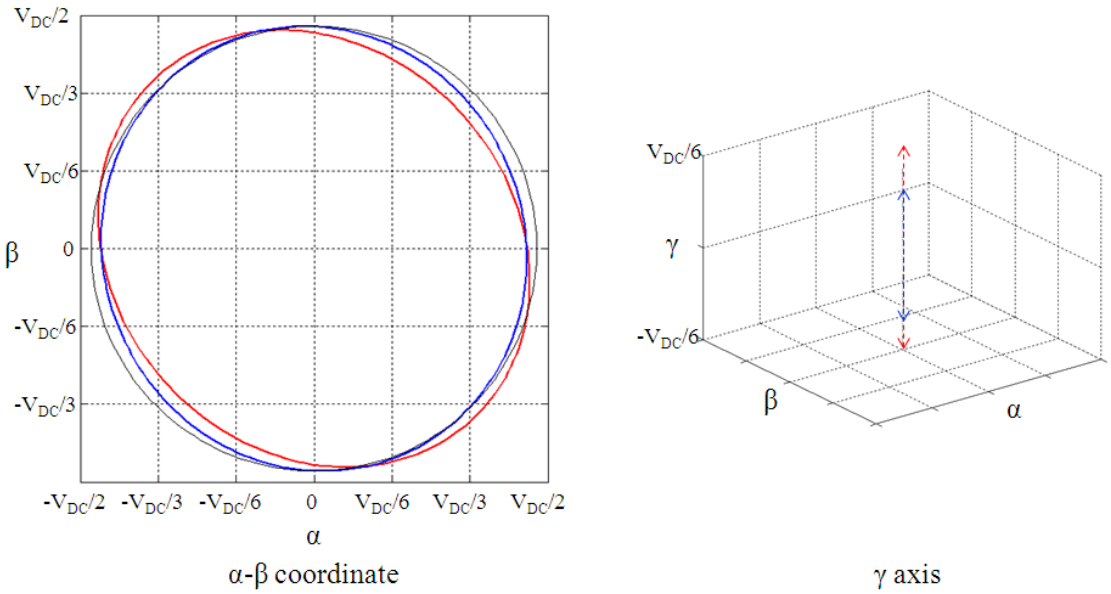
Therefore it can be seen that the positive and negative-sequence reference voltage only affect the trajectory of the reference vector on *α*-*β* plane. The zero-sequence reference voltage is only affected by the zero-sequence current and the trajectory of the reference vector only travels alongside the γ axis.

So a reference rotating vector in three-dimensional space can be decoupled into a reference vector rotates on the *α*-*β* plane and a vector which travels alongside the γ axis, this is shown in Figure 5.1.

In Figure 5.1 (a), the trajectories of reference voltage under different load condition are shown. The black trace is balanced load condition, while the blue and red traces are unbalanced. Figure 5.1 (b) shows that on *α*-*β* plane, the trajectories under unbalanced load condition show an oval shape, and the zero-sequence reference voltage travels alongside the γ axis.




(a)




(b)

Figure 5.1Trajectory of reference voltage under different load conditions, (a)in *α-β-γ* coordinate, (b)in decoupled *α-β* plane plus the γ axis; red trace unbalance percentage: *Unbal_N*%=*Unbal_0*%=100%;blue trace unbalance percentage: *Unbal_N*%=*Unbal_0*% =50%; black trace is balanced load condition

## 5.2 A zero-sequence component injected PWM scheme

Based on the decoupled model of the reference voltage vector, it is natural to assume that the modulation index for the first three phases, i.e. Phase A, B and C can be modulated based only on $\alpha$, $\beta$ element.

This can be proved mathematically by taking any one of the 24 tetrahedrons; in this case, Tetrahedron 1 in Prism I is chosen for demonstration purposes, the duty ratios can be written down below:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix} \begin{bmatrix} V_{\alpha\_ref} \\ V_{\beta\_ref} \\ V_{\gamma\_ref} \end{bmatrix} \tag{5.15}$$

$$d_z = 1 - d_1 - d_2 - d_3$$

Selecting $\vec{V}_z$= pppp as the zero switching vector, the modulation index for four legs are shown

$$\begin{bmatrix} Mi_A \\ Mi_B \\ Mi_C \\ Mi_f \end{bmatrix} = \begin{bmatrix} 0 \\ d_1 + d_2 \\ d_1 + d_2 + d_3 \\ d_1 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} 0 \\ \frac{3}{2} V_{\alpha\_ref} - \frac{\sqrt{3}}{2} V_{\beta\_ref} \\ \frac{3}{2} V_{\alpha\_ref} + \frac{\sqrt{3}}{2} V_{\beta\_ref} \\ V_{\alpha\_ref} + V_{\gamma\_ref} \end{bmatrix} \tag{5.16}$$

It can be seen clearly from Eq. (5.16) that the first three phase modulation indices are not related to the $\gamma$ element. Applying this calculation for the rest of the 24 tetrahedrons, notice that the matrix needed to compute the duty ratios and the sequencing of the selected switching vectors have to change in Eq. (5.15) and (5.16), the same conclusion can be obtained for each tetrahedron.

Therefore it can be concluded that the modulation index for the first three phases can be generated based on the information of $V_{\alpha\_ref}$ and $V_{\beta\_ref}$ only. This means that the two-dimensional SVM that is generally seen for three-phase three-leg VSI can be used to calculate the $\alpha$ and $\beta$ components so as to generate Phase A, B and C modulation index waveform. Now only one equation is needed to calculate the duty ratio of fourth leg and this will simplify the conventional 3-D SVM.

The relationship between the phase voltage modulation index and the fourth leg modulation index can be expressed below

$$\begin{bmatrix} Mi_{af} \\ Mi_{bf} \\ Mi_{cf} \end{bmatrix} = \begin{bmatrix} Mi_A \\ Mi_B \\ Mi_C \end{bmatrix} - Mi_f \tag{5.17}$$

where $Mi_{af}$, $Mi_{bf}$, $Mi_{cf}$ are the fundamental phase voltage references and are related to $V_{af}$, $V_{bf}$ and $V_{cf}$ in the large signal model of the four-leg inverter. These are the pre-calculated values for open loop operation; for closed loop system, these are the values from the controller outputs, so they are known values before being supplied as the modulation index for the switching scheme.

Now the simplification of the 3-D SVM switching scheme can be summarised as follows:

Based on the trajectory on the $\alpha$-$\beta$ coordinate, the modulation index for the first three phases can be obtained, this requires the same steps as space vector modulation, namely sector identification, selecting the switching vectors and sequencing the selected switching vectors, but since it is now in a 2-D plane, the process is much easier. Once the first three phase modulation indexes are obtained, using the fourth leg duty ratio calculation Eq. (5.17), the fourth leg modulation index can be easily generated. Compared with the 3-D SVM, this avoids the steps of tetrahedron identification, and the amount of calculation of the duty ratios for each switching vector has been reduced dramatically. The simplification of the switching scheme is shown in Figure 5.2.

Therefore, the algorithm of conventional 3-D SVM and the near-state 3-D SVM which is proposed in Chapter 3 can be simplified by using the proposed simplified method. The following sections show the simulation and experimental results under the zero-sequence injected PWM switching scheme.

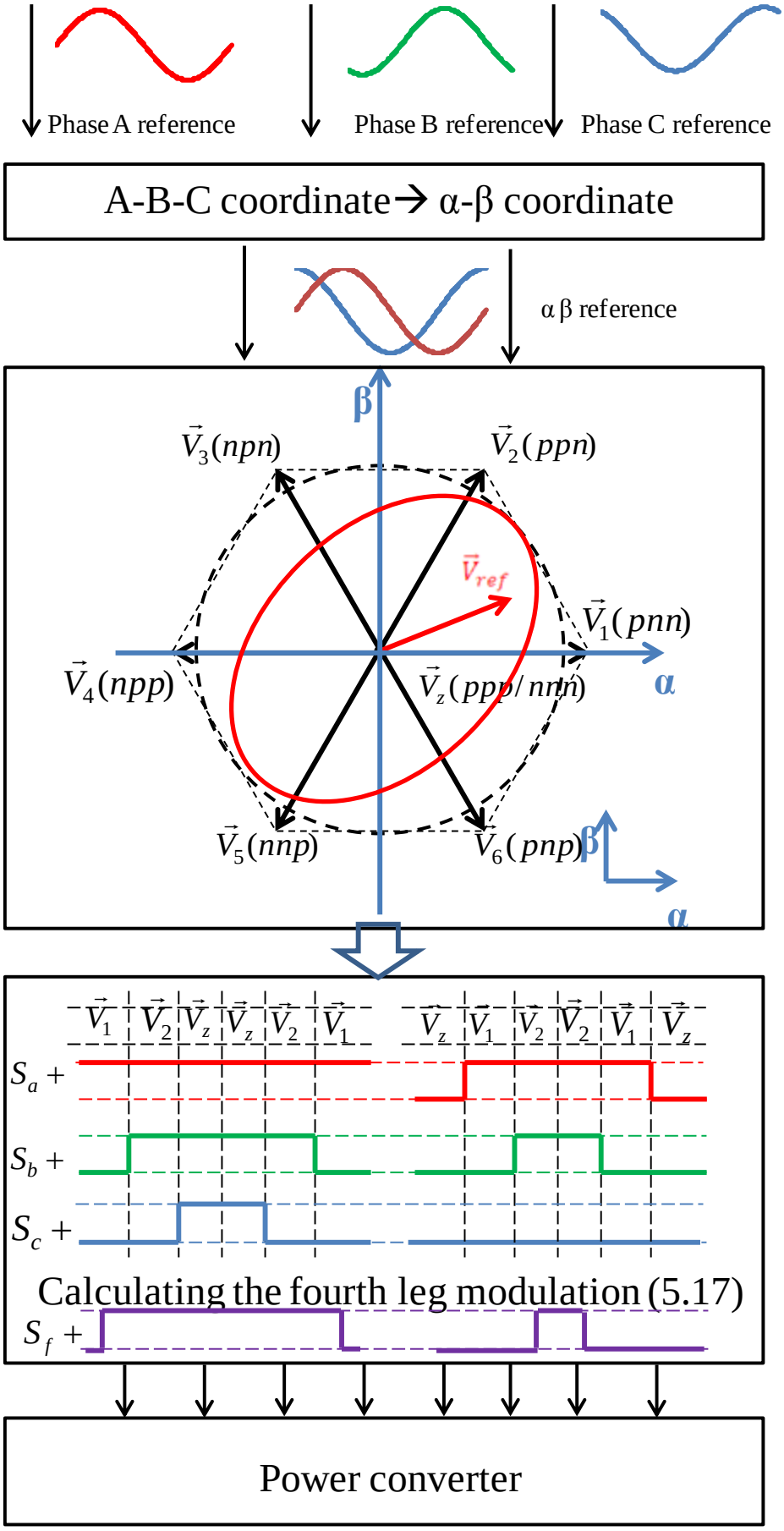



Figure 5.2 Block diagram of zero-sequence component injected PWM method

## 5.3 Simulation and Experimental Results

### 5.3.1 Conventional 3-D SVM

In [18], it is shown clearly that among all the possible schemes of the conventional 3-D SVM, symmetrical aligned Class II scheme is a good compromise between the switching loss and the harmonic content. The modulation index waveform of this scheme under balanced load condition shows the same feature as the DPWM1[37] for the three-phase three-leg inverter. The common-mode modulation index or zero-sequence signal for DPWM1 can be calculated according to Eq. (5.18)[36, 41], and it can be seen that the zero-sequence signal is the same as the fourth leg modulation of 3-D SVM under balanced load condition.

$$Mi_n = \frac{Mi_A + Mi_B + Mi_C}{3} \tag{5.18}$$

So the simplification of symmetrical aligned Class II 3-D SVM can be made as the combination of DPWM1 and fourth leg modulation calculation (shown in Figure 5.3). The sequencing of DPWM1 has been studied intensively; the simulation results are shown clearly that the resultant modulation index waveform and output voltage waveforms are exactly the same as that of 3-D SVM.

Figure 5.4 shows the experimental output voltage and current waveforms of the proposed switching method and the result shows the same waveform as the conventional 3-D SVM. The THD analysis also shows exactly the same result as that of 3-D SVM.

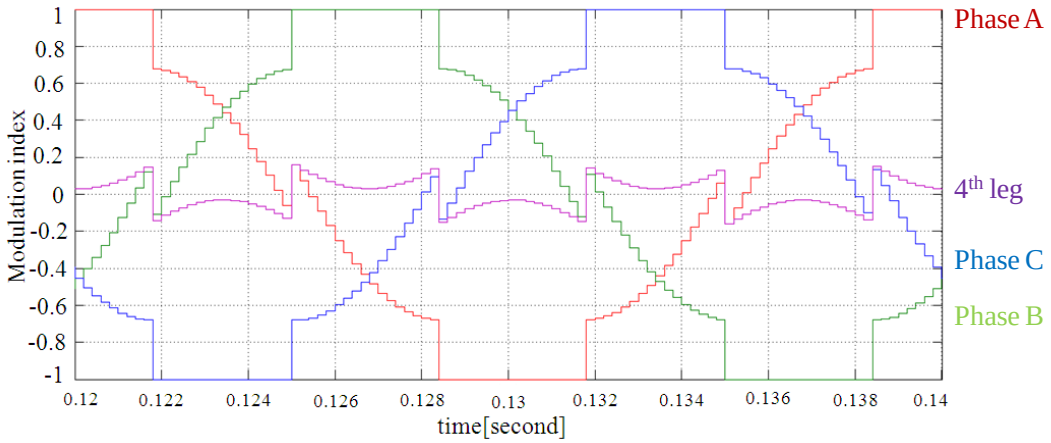



Figure 5.3 Simulated Modulation Index Waveform of the zero-sequence component injected PWM under balanced load condition

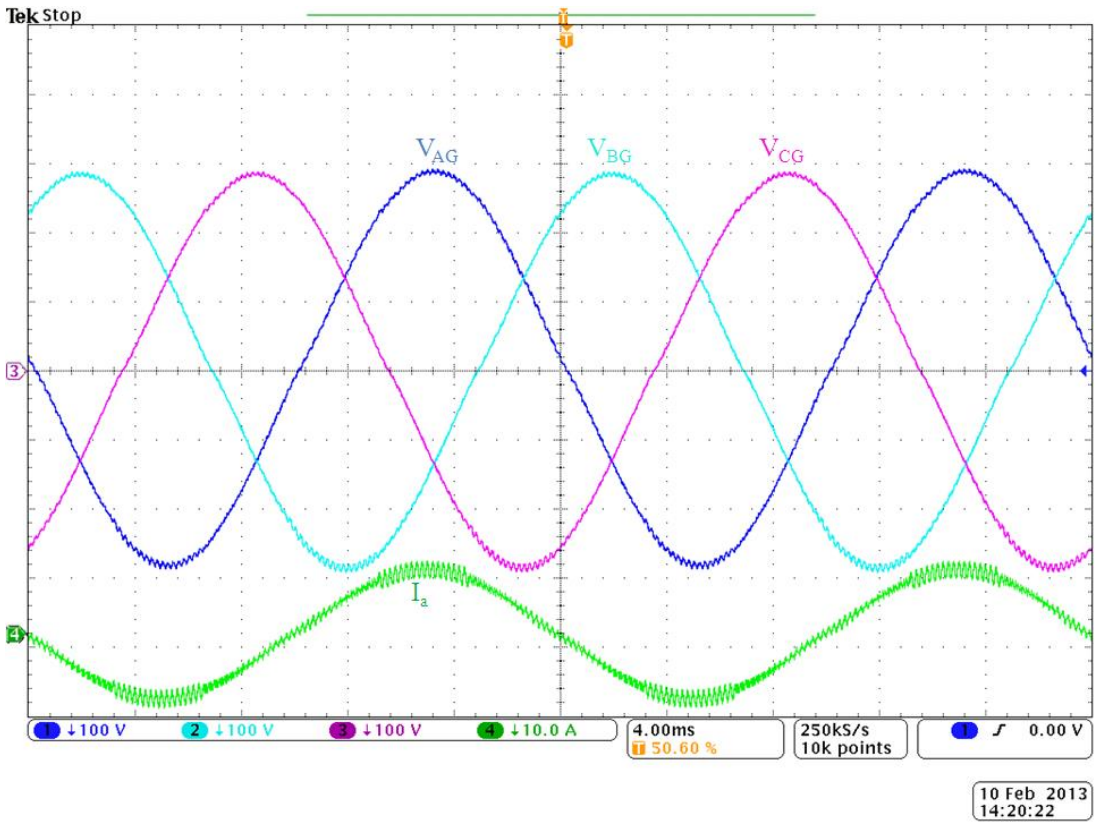



Figure 5.4 Experimental results show that the proposed zero-sequence component injected PWM scheme has the same result as the conventional 3-D SVM, channel 1-3: Output voltage; Channel 4: Phase A inductor current

In order to test whether the zero-sequence injected PWM method works well under unbalanced load condition, a heavily unbalanced load condition is chosen in which phase C is unloaded. Figure 5.5 and Figure 5.6 show the output voltage and load current under this load condition. The results prove that the proposed simplified switching method works exactly as the 3-D SVM under both balanced and unbalanced load conditions.

The simplified algorithm also leads to a reduction of the programme execution time and this can be seen in Figure 5.7. The technique required to monitor the programme execution time was explained in the previous chapters and the details can be found in Appendix B. In Figure 5.7, trace 1 shows the GPIO pin output and the width of the pulse is the execution time of the zero-sequence injected PWM algorithm. Trace 2 shows the pulse relates to the 3-D SVM execution time. It could be seen clearly that the simplified switching scheme reduces the code execution time by about 20%.

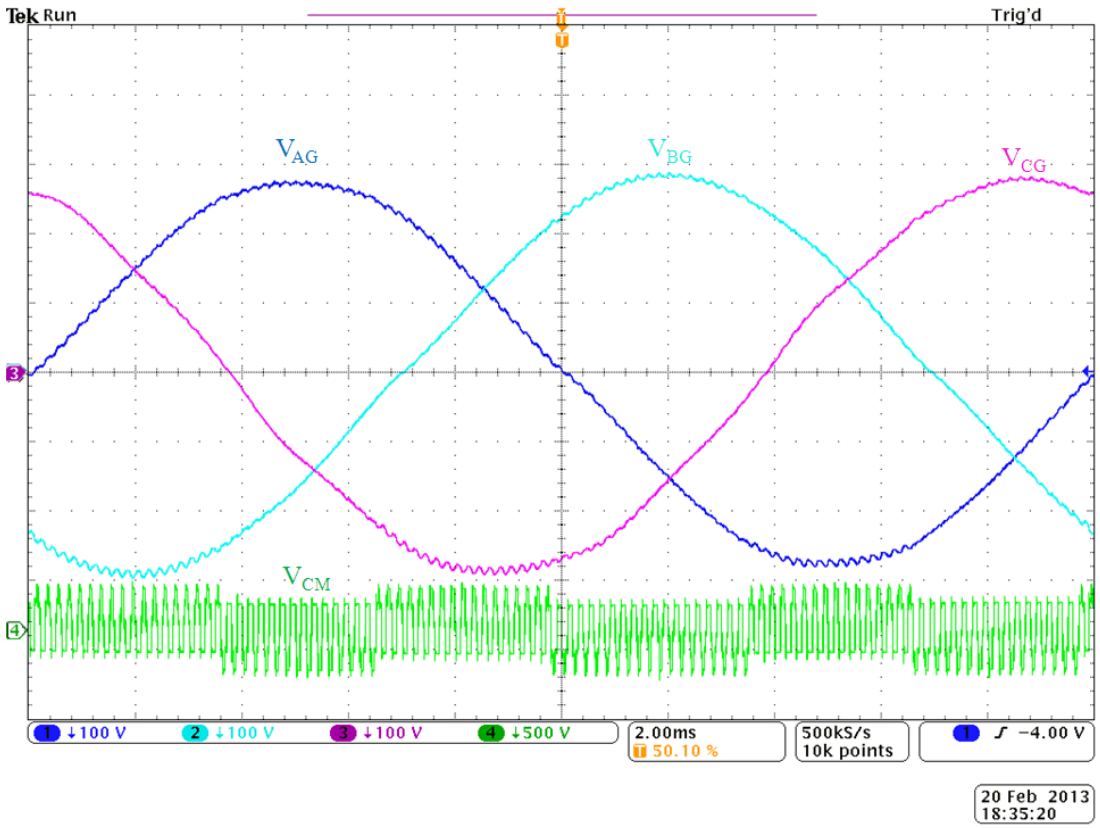



Figure 5.5 Voltage output under unbalanced load condition show the same result as the conventional 3-D SVM

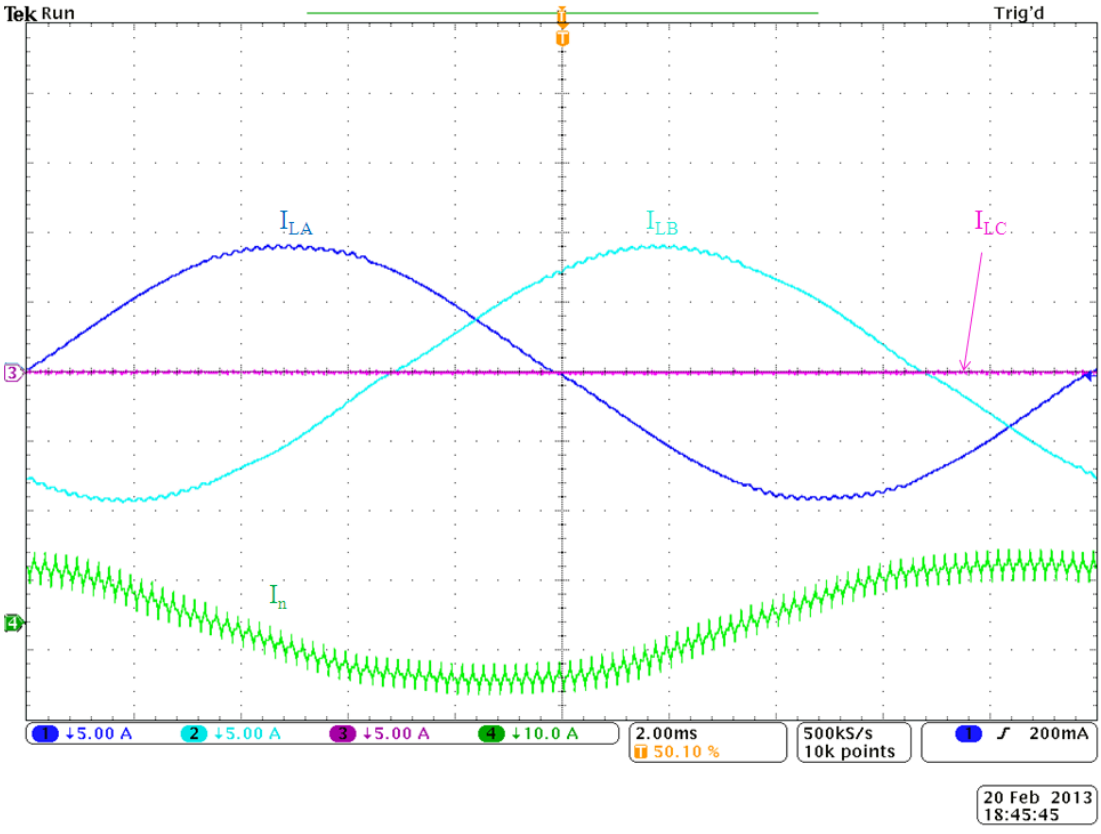



Figure 5.6 Load current and neutral current waveform under unbalanced load condition, showing the same result as the conventional 3-D SVM

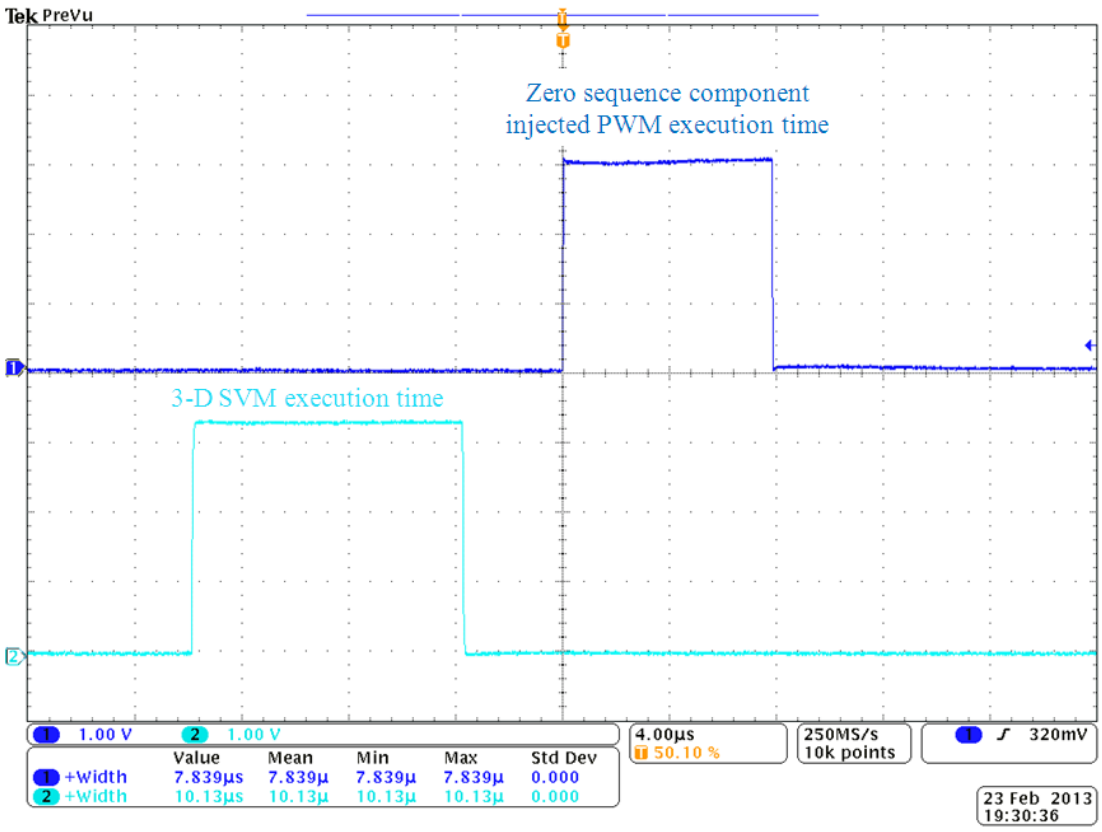



Figure 5.7 GPIO pulse test result shows that the proposed method reduces the programme execution time compared with the 3-D SVM

### 5.3.2 Near-state 3-D SVM

The simplification of the near-state 3-D SVM follows the same rule. The generation of the modulation index waveforms of the first three phases based on the near-state PWM method for three-phase three-leg VSI. The duty ratios of the required space vectors of NSPWM for region $B_i$ can be calculated as follows[39]:

$$
\begin{aligned}
d_{i-1} &= 1 - Mi \times \sin\left[\theta - \frac{(i-2)\pi}{3}\right] \\
d_i &= -1 + \frac{\sqrt{3}}{2} \times Mi \times \cos[\theta - \frac{(i-2)\pi}{3}] + \frac{3}{2} \times Mi \times \sin[\theta - \frac{(i-2)\pi}{3}] \\
d_{i+1} &= 1 - \frac{\sqrt{3}}{2} \times Mi \times \cos[\theta - \frac{(i-2)\pi}{3}] - \frac{1}{2} \times Mi \times \sin[\theta - \frac{(i-2)\pi}{3}]
\end{aligned}
\tag{5.19}
$$

The sequencing of the selected switching vectors is also a general form and is presented in [39], with the combination of Eq.(5.17), the near-state 3-D SVM can also be simplified. The simulated modulation index waveform shows exactly the same as in Figure 3.13.

The experimental results under both balanced load and unbalanced load conditions show exactly the same result as the near-state 3-D SVM. Since the results are the same as shown in Figure 3.35-Figure 3.38, they are not presented in this section.

## 5.4 Summary

In this chapter, a zero-sequence component injected PWM method is introduced. The algorithm of the 3-D SVM switching scheme, either conventional 3-D SVM or near-state 3-D SVM is very complex and difficult to understand. It requires a few steps to finally synthesize the reference vector. A decoupled reference voltage vector model in $\alpha$-$\beta$-$\gamma$ coordinate shows that the reference vector can be represented with $\alpha$-$\beta$ plane and independent axis of $\gamma$. By doing this, the algorithm required to synthesize the reference switching vector can be simplified. The modulation indexes for the first three phases depend on the trajectory of the reference vector on $\alpha$-$\beta$ plane and they can be generated using the steps to synthesize the reference vector for three-phase three-leg VSI. A fourth leg modulation index is then calculated based on the simple relationship to the reference voltage vector.

Both simulation and experimental results show that the proposed simplified switching scheme have the same results as the conventional 3-D SVM and near-state 3-D SVM under both balanced and unbalanced load condition. The simplified algorithm has the merit of easy understanding and reduced programme execution time. The reduction of the programme execution time has also been validated by experimental results.

# Chapter 6

# Control of Three-phase Four-Leg Inverters

A three-phase four-leg VSI is used for unbalanced loads and/or nonlinear loads [18, 32]. The controller design is therefore vital for a three-phase four-leg inverter system to secure a balanced three-phase voltage output under various load conditions. Stability is an important factor when it comes to a controller design; also equally important is the dynamic response of the controller since a fast controller will compensate the unbalanced voltage drop or correct the distorted voltage waveform in a short response time. Various controller designs have been investigated in the literature survey, and it has been found that the controller design in *d-q-o* coordinate is most compatible with the vector implemented switching scheme [18, 32]. In contrast the per-phase controller design is suitable for the scalar-based, or in other words, carrier-based PWM switching scheme[14]. Because the proposed switching scheme in Chapter 3 and simplified switching scheme in Chapter 5 are all vector based, a controller design based on *d-q-o* is presented in this chapter.

Modern DSPs with processor speed up to 150MHz and enhanced peripherals, real-time code debugging capability gives control engineers all the benefits of digital control[63]. It was shown clearly in the previous chapters that a simulation model based in Matlab/Simulink and Matlab/Simpower combined with programmable code in S-function gives a close simulation result to the experimental result. In this chapter, a controller design using Matlab/sisotool is shown as a very useful tool for the real-time controller design.

## 6.1 A four-leg inverter model in *d-q-o* coordinate

A four-leg VSI model in *d-q-o* coordinate has been intensively investigated in [18, 32] and its model was introduced in Figure 2.28 in the literature review. The *d-q-o* coordinate model is given by

$$\begin{bmatrix} X_d \\ X_q \\ X_o \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{6.1}$$

According to [19], the output to duty ratio transfer functions of *d* and *q* channel can be obtained based on the state space model below

$$\frac{d}{dt}\begin{bmatrix} V_d \\ I_d \\ V_q \\ I_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{CZ} & \frac{1}{C} & \omega & 0 \\ -\frac{1}{L} & 0 & 0 & \omega \\ -\omega & 0 & -\frac{1}{CZ} & \frac{1}{C} \\ 0 & -\omega & -\frac{1}{L} & 0 \end{bmatrix}\begin{bmatrix} V_d \\ I_d \\ V_q \\ I_q \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ \frac{V_{DC}}{L} & 0 \\ 0 & 0 \\ 0 & \frac{V_{DC}}{L} \end{bmatrix}\begin{bmatrix} d_d \\ d_q \end{bmatrix} \tag{6.2}$$

where $L$, $C$ and $V_{DC}$ are system hardware parameters and the values are the same as the experimental set up, $Z$ is the load impedance. Eq. (6.2) indicates the coupling term between the *d* channel and *q* channel. There is no coupling term in the *o* channel, and it is a typical second-order system, therefore the output to duty ratio transfer function of the *o* channel can be obtained

$$\frac{d}{dt}\begin{bmatrix} V_o \\ I_o \end{bmatrix} = \begin{bmatrix} -\frac{1}{CZ} & \frac{1}{C} \\ -\frac{1}{L'} & 0 \end{bmatrix}\begin{bmatrix} V_o \\ I_o \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_{DC}}{L'} \end{bmatrix} d_o \tag{6.3}$$

It should be noticed that in Eq. (6.3), $L' = L + 3L_n$[19], since here the neutral inductor has been selected the same value as per-phase inductor, therefore $L' = 4L$.

The state space model in Eq. (6.2) and (6.3) are based in continuous time domain; the model would be accurate if the system is controlled by analogue controller. However, since modern DSPs have been seen everywhere in a real-time implementation system these days, a system transfer function model based on discrete-time domain would be preferred.

Figure 6.1 shows a DSP controlled four-leg VSI. Isolation amplifiers and current sensors are used to sample the voltage and current outputs of the system. The controller design is based on the direct digital design[63] in discrete-time domain with the help of Matlab/sisotool.

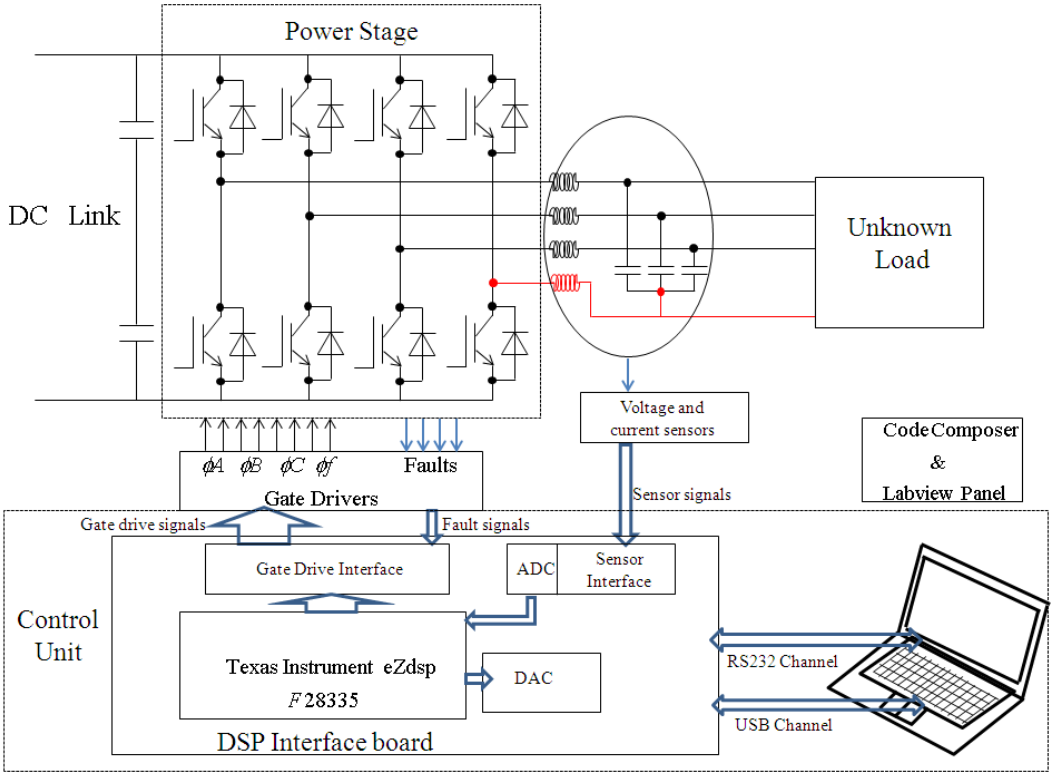



Figure 6.1 A DSP controlled four-leg VSI

The computation delay $H_c$ is defined as

$$H_c = e^{-T_d s} \tag{6.4}$$

where $T_d$ is the delay time. The sampling of the sensors and the PWM outputs altogether can be represented as a Zero-order hold[63] and therefore zero-order hold is selected as the discretization method

$$TF(z) = c2d(TF(s), T_{PWM}, \text{'zoh'}) \tag{6.5}$$

where *c2d* is a Matlab command in which continuous model is transformed into a discrete model, 'zoh' is the discretization method and $T_{PWM}$ is the sampling time and it is chosen as 200μs since the current and voltage sensors sample at the peak of every PWM cycle. Since the newly generated modulation index value only takes effect at the beginning of each PWM cycle, the delay that has been caused by the computational delay therefore is set as half of the sampling time with the value of $T_d = T_{PWM}/2$.

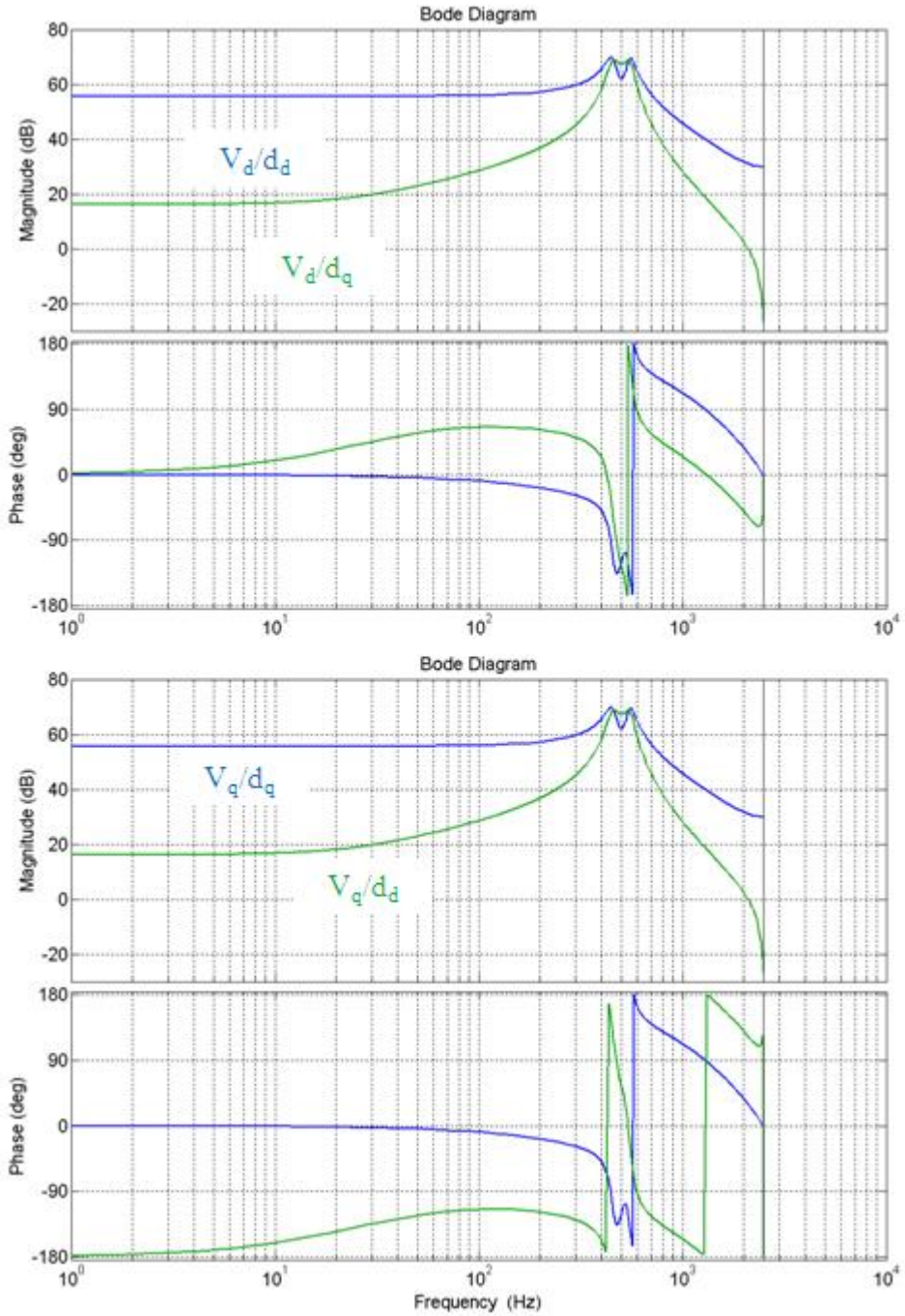



Figure 6.2 Simulated control-to-output transfer functions for *d* and *q* channel

The plant control-to-output transfer functions of channel *d*, *q* and *o* in discrete domain are therefore calculated and plotted using Matlab as shown in Figure 6.2 and Figure 6.3. A balanced three-phase light load with the per-phase impedance value of 300Ω has been selected as the worst load condition.

In Figure 6.2, the control-to-output transfer functions of *d* and *q* channels are shown. In the diagram, the following characteristics can be observed:

- As explained before, the *d* channel and *q* channel are coupled, therefore for each input, either $d_d$ or $d_q$, there are two outputs $V_d$ and $V_q$. The blue trace in Figure 6.2 shows the dominant transfer function while the green trace shows the coupled transfer function.
- The transfer functions, which are $V_d/d_d$, $V_q/d_q$, $V_d/d_q$ and $V_q/d_d$ are $4^{th}$ order systems, with four poles and two zeros around the resonant frequency. But since the four poles and two zeros are close to each other, the $4^{th}$ order systems show a very similar shape to a typical $2^{nd}$ order system.
- At the resonant frequency, a light load situation causes a peak in the magnitude plot, this poses a problem when it comes to controller design as it will be explained later. Also, on the phase plot, the phase drops sharply at the resonant frequency.
- The delays that are introduced, including the delay caused by zero-order hold and computational delay also causes the phase to roll down in the phase plot.

The bode diagram of the transfer function in o channel is shown in Figure 6.3. As explained, the *o* channel is a $2^{nd}$ order system. The impact of light load condition and the delay effect can be seen on the *o* channel as well.

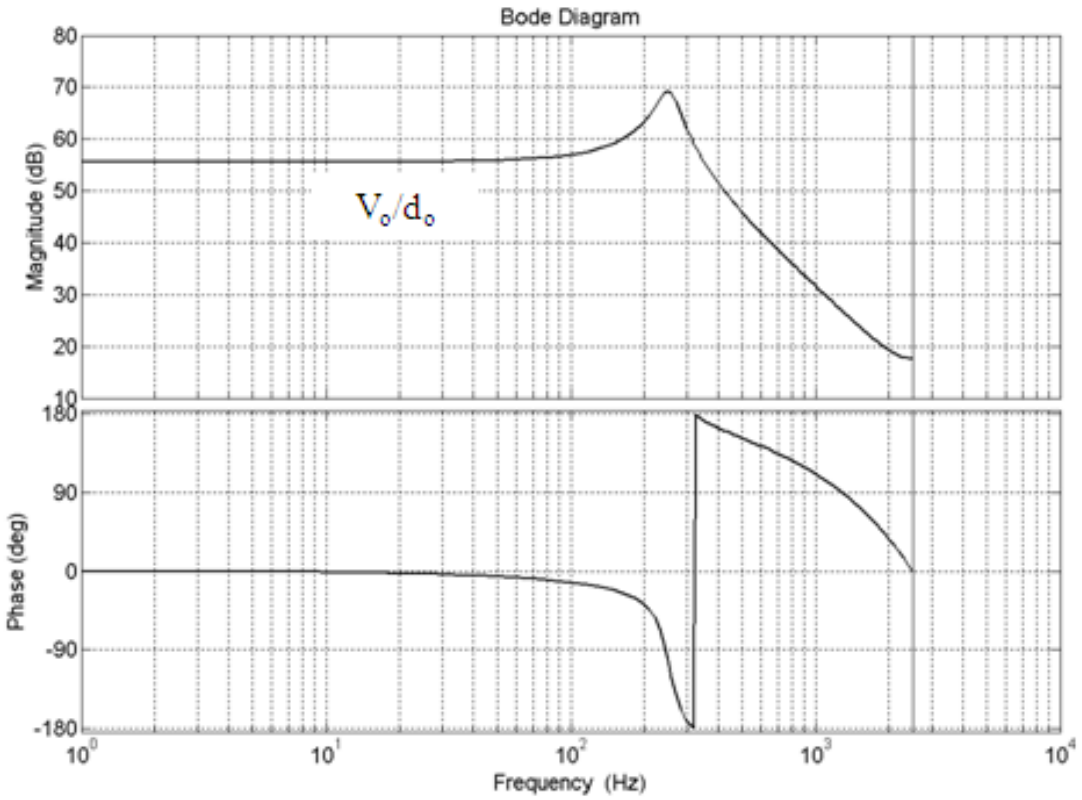



Figure 6.3 Simulated control-to-output transfer function for *o* channel

## 6.2 Controller design in *d-q-o* coordinate

### 6.2.1 Issue with low cut-off frequency

Now that the system transfer functions are identified, a feedback voltage control loop can be designed based on the control-to-output transfer functions. Since the transfer functions are $4^{th}$ order systems for *d* and *q* channel, a higher order controller with decoupling terms in the feed-forward loop is needed in theory [19]. However, as the four poles and two zeros are close to each other in the resonant frequency as explained before, the system can be simplified as a $2^{nd}$ order system. As for the coupling term, they are neglected at this stage since their gains are lower than those of the dominant transfer functions. Therefore PI controllers can be used as the voltage controller.

When designing the PI controller based on the control-to-output transfer functions under light load condition, the peak shown in the magnitude plot poses a stability problem. A PI controller which is optimized for the system stability is shown in Figure 6.4. For demonstration purposes, only *d* channel is shown here. A PI controller is designed so that the gain margin is over 10dB and the phase margin is 90°, this will ensure the system stability. As it can be seen, this design sacrifices the system dynamic behaviour due to the low cut-off frequency of the controller.

This control loop works well under balanced load condition and in cases where the loads are slightly unbalanced. However, under heavy unbalanced load condition, the low cut-off frequency makes the controller struggle to compensate for the unbalanced current that has been caused by unbalanced load. Normally, a faster inner current loop would help dampen the system resonance, provide over-current detection and protection and improve the dynamics performance of a cascaded loop control system [19]. However, in this case, unlike in the motor drive system where there is a variable back EMF due to the variable speed of the motor, the output voltage is related to the output current depending on the load type. This means the current loop control design will face the same low cut-off frequency issue as the voltage control loop design. Figure 6.4 also shows the current loop gain transfer function with controller in *d* channel. As it is shown clearly, both the voltage and current transfer functions have quite similar shape and the inner current loop only extends the bandwidth by tens of Hz. The details of the controllers design for voltage loop and current loop under channel *d* and *q* are shown in Table 6-1.

**Table 6-1 Designed voltage and current controller for d and q channel**

| | Controller | Cross-over frequency | Phase Margin | Gain Margin |
|---|---|---|---|---|
| Voltage loop | $9.23\times10^{-5}\,\frac{z-0.539}{(z-1)}$ | 20.6Hz | 90.7° | 11.1dB |
| Current loop | $0.0048\,\frac{z-0.543}{(z-1)(z-0.994)}$ | 39.3Hz | 89.5° | 4.4dB |

**Table 6-2 Designed voltage and current controller for o channel**

| | Controller | Cross-over frequency | Phase Margin | Gain Margin |
|---|---|---|---|---|
| Voltage loop | $9.92\times10^{-5}\,\frac{z-0.726}{(z-1)}$ | 13Hz | 91.4° | 11.1dB |
| Current loop | $0.003\,\frac{z-0.732}{(z-1)(z-0.935)}$ | 20.1Hz | 91.6° | 6.37dB |

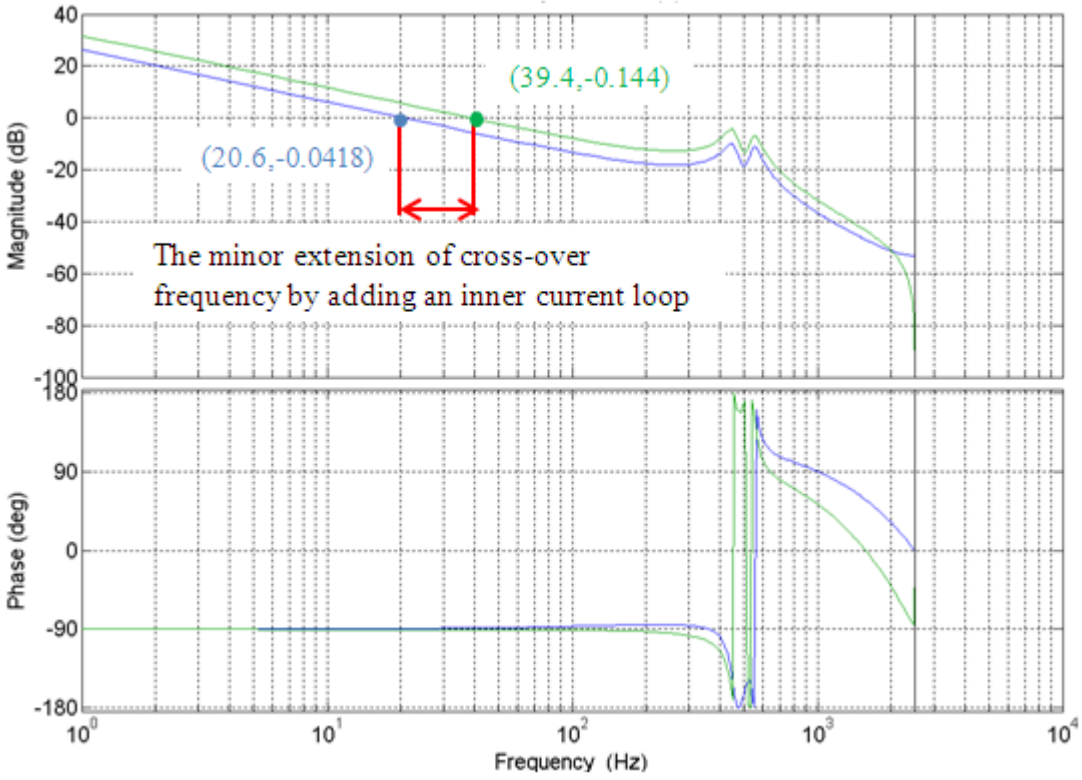



Figure 6.4 Voltage and current loop gain transfer functions with controllers

### 6.2.2 Controller output integration to 3-D SVM

Another issue which is worth noticing is that the integration between the controller output to the 3-D SVM switching scheme. The controller outputs from channel *d*, *q* and *o* are the control duty ratios $d_d$, $d_q$ and $d_o$. These values have to be supplied to the switching scheme. Similar to Eq. (6.1), $d_d$, $d_q$ and $d_o$ can be given by

$$\begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} \tag{6.6}$$

where $d_{af}$, $d_{bf}$ and $d_{cf}$ are the line to neutral duty ratios of the four-leg inverter and they are related to the reference line to neutral voltage signals $V_{af}$, $V_{bf}$ and $V_{cf}$ by

$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = V_{DC}\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} \tag{6.7}$$

Therefore, one obtains

$$\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} = M\frac{1}{2}\begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{6.8}$$

where *M* is the fundamental per-phase modulation index value and it is related to the modulation index value *Mi* for SVM by a factor of $2/\sqrt{3}$, so Eq. (6.8) can also be expressed as

$$\begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} = Mi\frac{V_{DC}}{\sqrt{3}}\begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2}{3}\pi) \\ \sin(\omega t + \frac{2}{3}\pi) \end{bmatrix} \tag{6.9}$$

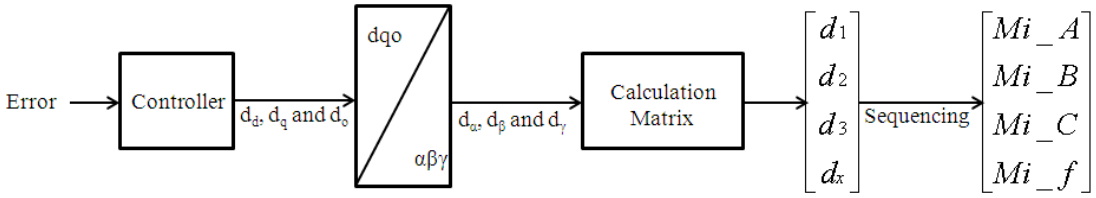



Figure 6.5 Controller output integrating to the 3-D SVM switching scheme

Based on Eq. (6.6) and (6.9), it is not difficult to calculate the maximum duty ratio value $d_{MAX}$ in *d*, *q* and *o* channel.

$$d_{MAX} = \frac{Mi_{MAX}}{\sqrt{3}} = 0.57735 \tag{6.10}$$

The duty ratio value in *d-q-o* coordinate and the modulation index value *Mi* in *A-B-C* coordinate have the same relationship as shown in Eq. (6.10). The value could be of great use in two aspects. Firstly, it could be used to estimate the amplitude of the three-phase output voltage. Secondly, it is very important to set up an anti-windup algorithm from the controller design point of view [87-89], and this value could be used as a reference to set up the upper limit of the anti-windup algorithm.

After $d_d$, $d_q$ and $d_o$ are obtained, it is better to transform these values into *α-β-γ* coordinate where the duty ratios for each phase can be calculated easily

$$\begin{bmatrix} d_\alpha \\ d_\beta \\ d_\gamma \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ \sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} \tag{6.11}$$

The final modulation index waveforms will then depend on the sequencing scheme that has been chosen. The process of the controller output integrating to the 3-D SVM scheme is shown in Figure 6.5.

### 6.2.3 Transformation between two *d-q-o* reference frames

When designing the voltage control loop, the sampled voltage values are the voltage values on the capacitors, $V_{AG}$, $V_{BG}$ and $V_{CG}$ shown in the average large signal model in Figure 2.27. While the 3-D SVM switching scheme depends on the information of the line-to-neutral reference voltage $V_{af}$, $V_{bf}$ and $V_{cf.}$ Between the line-to-neutral reference voltage and the phase voltage, there is a filter inductor which will cause a phase shift between. This will pose a problem when it comes to control in the *d-q-o* coordinate.

In [9], the author used the finite impulse response filter (FIR), so the specific knowledge of the output filter component values can be ignored for the control design. This thesis adopts another technique called phase angle compensation method. Aiming to compensate the phase delay by the *L-C* filter, an advanced angle is compensated, the details is given below.

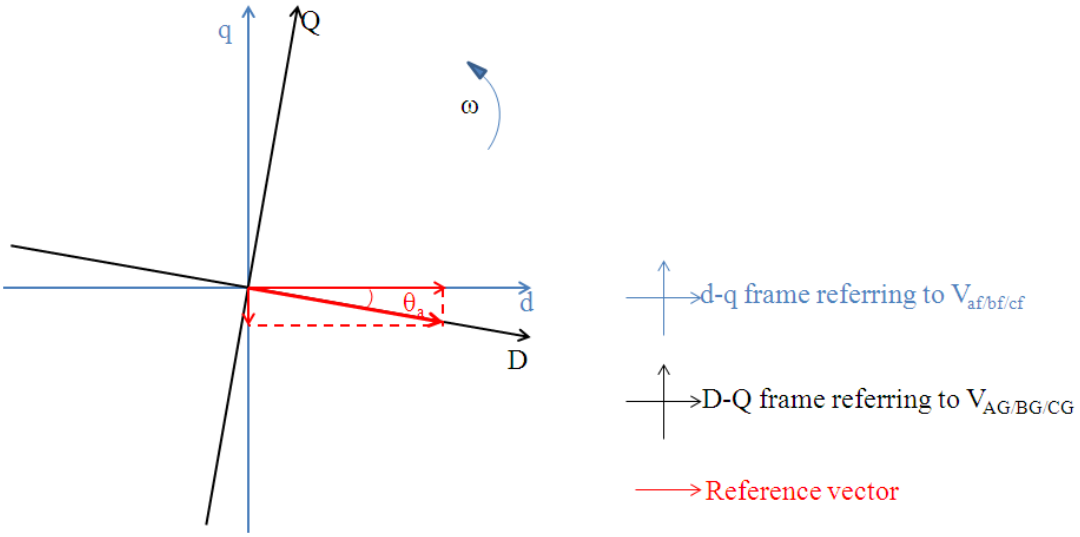
For demonstration purposes, the *d-q-o* reference frame which is related to the sampled phase voltage $V_{AG}$, $V_{BG}$ and $V_{CG}$ is defined as *D-Q-O* reference frame, with $V_D$, $V_Q$ and $V_O$ as the DC operating values. The *d-q-o* reference frame which is related to the line-to-neutral reference voltage $V_{af}$, $V_{bf}$ and $V_{cf}$ is then defined as *d-q-o* reference frame value with $V_d$, $V_q$ and $V_o$ as the DC operating values.

Under balanced load condition, both *d-q-o* and *D-Q-O* reference frames rotate at the same speed of $\omega$. Because of the filter component, the *D-Q-O* reference frame will be lagging the *d-q-o* reference frame by an angle of $\theta_a$. Here we define the rotating angle of the *D-Q-O* coordinate as $\theta_e$ and the rotating angle of the *d-q-o* coordinate as $\theta$. The value of $\theta_a$ depends on the inductance and capacitance value. This is shown in Figure 6.6 (a), without showing *o* channel since the o channel for both *D-Q-O* and *d-q-o* reference frames are the same. As it can be seen, if viewing from the *d-q* reference frame, *D-Q* reference is behind by $\theta_a$. A reference vector on *D* axis will have negative *q* value on the *q* axis of *d-q*. This can be demonstrated in simulation as well.

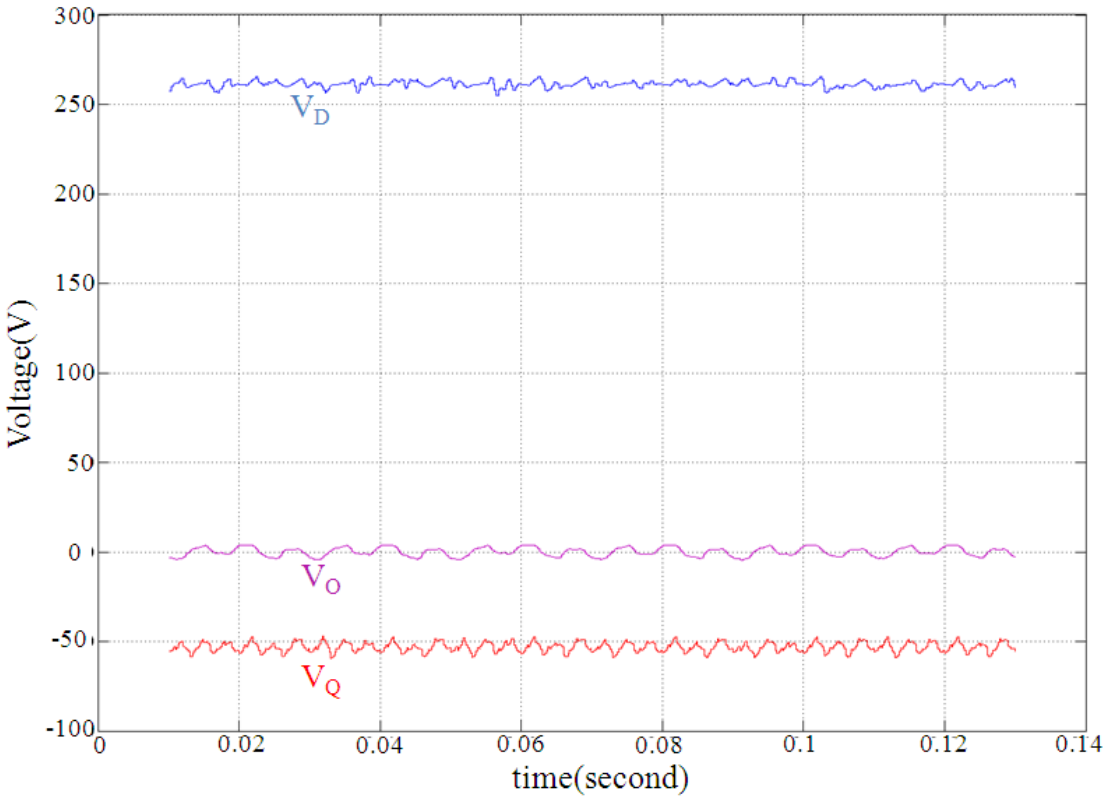
In Matlab simulation model, when setting up $V_d$=282V, $V_q$=$V_o$=0 to calculate the 3-D SVM algorithm in an open loop system, the three-phase voltages are sampled and then transformed into the values in a *D-Q-O* coordinate. It is shown in Figure 6.6 (b) that $V_Q$ has negative value and it can be calculated based on Eq. (6.12) that the angle $\theta_a \approx 10°$.

$$\theta_a = \theta - \theta_e = 0 - \arctan\frac{V_Q}{V_D} \tag{6.12}$$

The conventional 3-D SVM needs the information of the reference vector rotating angle, $V_{\alpha/\beta/\gamma}$ and $V_{af/bf/cf}$ to decide in which tetrahedron the reference vector locates, and the near-state 3-D SVM needs the information of reference vector to know in which section the reference vector is. Because the reference vector is strongly related to the reference vector in *d-q-o* coordinate, a transformation between *D-Q* reference frame and *d-q* reference frame is needed.




(a)




(b)

Figure 6.6 Relationship between *D-Q-O* reference frame and *d-q-o* reference frame; (a) The two rotating reference frames; (b) Sampled values of $V_D$, $V_Q$ and $V_O$

Once the angle of $\theta_a$ is known based on the *L-C* filter of the power stage, an angle advance technique can then be employed to compensate the phase lagging. The advanced angle is the same as $\theta_a$. Based on the information of $\theta_e$ and by using Eq. (6.12), the rotating angle $\theta$, which is used to implement 3-D SVM switching scheme, can be obtained. This technique, together with voltage control based on the *d-q-o* coordinate, is shown in Figure 6.7.

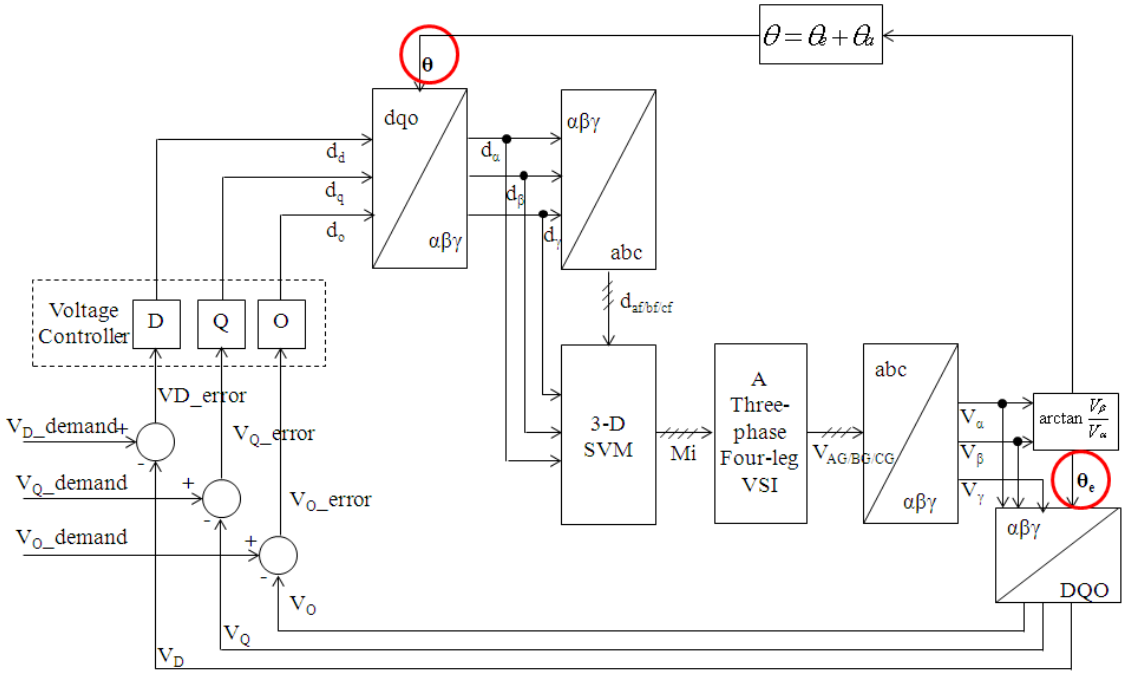



Figure 6.7 Phase advance technique together with voltage control loop based on *d-q-o* coordinate

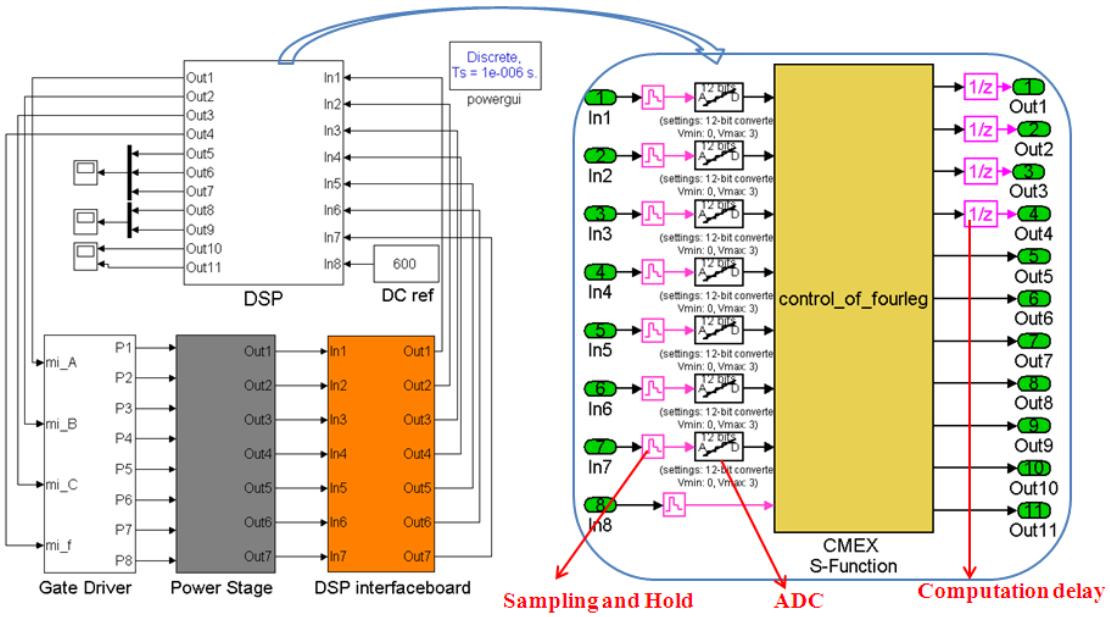



Figure 6.8 Simulation structure for a closed-loop four-leg VSI

## 6.2.4 Voltage ripples in *o* channel and current feed forward method

Figure 6.8 shows the Matlab simulation structure for a closed loop four-leg VSI. The gate driver block, Power stage block are the same as in the open-loop simulation structure (Figure 3.23), where the DSP block mimics the real-time DSP system with

sample and hold block and computation delay block. This simulation model takes all the delays caused by the digital processor; therefore it serves as a useful tool for the controller design in real-time implementation.

It has been stated in the previous sections that an inner current loop will not increase the dynamic behaviour of the controller. Therefore, three voltage controllers are designed according to the parameters in Table 6-1 and Table 6-2 for channel *d*, *q* and *o*. Under balanced load condition, results shown in Figure 6.9 indicate a balanced three-phase output. It can be seen that for a balanced voltage output, the errors in *d*, *q* and *o* channel are close to zero. The trajectory of the reference switching vector on the *α*-*β* plane draws a circle while the *o* channel signal has only small ripples close to zero. Figure 6.9 (d) shows the three-phase inductor currents and the neutral current under balanced load condition.

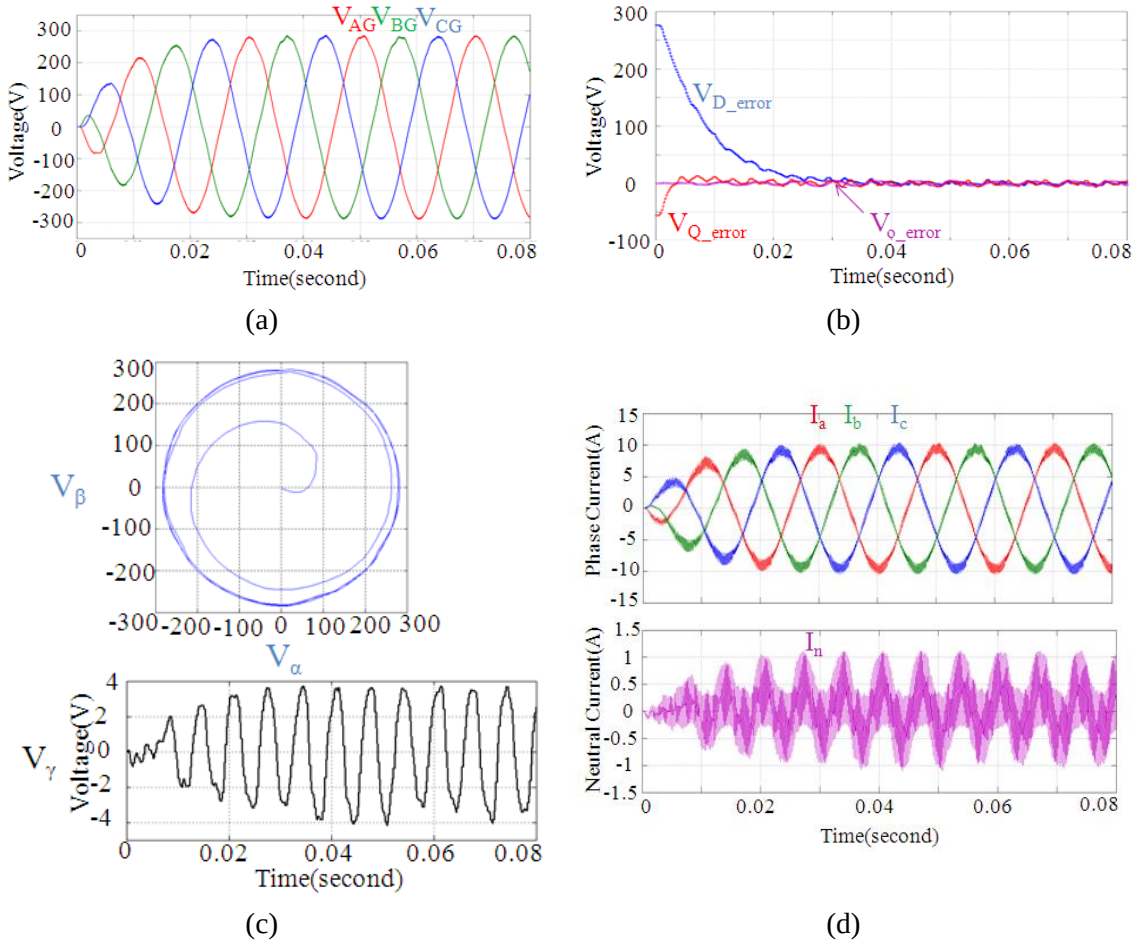



Figure 6.9 Simulated output of a four-leg VSI under voltage control under balanced load condition; (a)Output phase voltages; (b)Error signals in channel *d*, *q* and *o* (c)trajectory of *α*, *β* and *γ* components (d) Phase inductor currents and neutral current

Under unbalanced load condition, the voltage loops designed for *d*, *q* and *o* channel results in unbalanced output voltages as shown in Figure 6.10. For demonstration purposes, a single phase unloaded condition is chosen. It can be seen clearly in Figure 6.10 (b) that the voltage error signal in o channel has increased with a voltage ripple at the fundamental frequency. This is due to the zero-sequence current that has been created due to the single phase unloaded condition. Because of the slow dynamic response of the voltage controller alone, the voltage component shows a voltage ripple in $\gamma$ axis (Figure 6.10 (c)). The voltage ripples also appear in *d* and *q* channel at $2\omega$ rotating speed in conditions when the negative-sequence current is large. These ripples cause the phase voltages to be unbalanced and they need to be compensated for the controller design.

In [19], three current feed-forward terms were added in the voltage loop so as to improve the dynamics of the controller. The current feed-forward terms can be found in

$$\begin{cases} G_{iLd} = \dfrac{L}{V_{DC}}\left(\dfrac{d}{dt} I_{Ld} - \omega I_{Ld}\right) \\ G_{iLq} = \dfrac{L}{V_{DC}}\left(\dfrac{d}{dt} I_{Lq} + \omega I_{Ld}\right) \\ G_{iLo} = \dfrac{L^{'}}{V_{DC}} \dfrac{d}{dt} I_{Lo} \end{cases} \tag{6.13}$$

where $I_{Ld}$, $I_{Lq}$ and $I_{Lo}$ are the *d*, *q*, *o* components of the load current $I_{LA}$, $I_{LB}$ and $I_{LC}$.

The information of the load current can be obtained if the current sensors are allocated along the load side. However, since the current sensors are inductor current sensors, a technique is needed to use the inductor current as the feed-forward term.

There is a phase shift between the inductor current and the load current. The sampled inductor current, if phase shifted by certain angle, would be in phase with the load current. A digital filter can filter out the inductor current noise, and at the same time, delay the sampled signal. By selecting the digital filter parameters carefully, the filtered inductor current can then be used as the current feed-forward term. Figure 6.11 shows a digital *RC* filter that has been used in the control loop design. The gain value $\rho$ can be calculated based on

$$\rho = e^{-2\pi f_c T_s} \tag{6.14}$$

where $T_s$ is the sampling time and $f_c$ is the cut off frequency of the *RC* filter, here $f_c$ is chosen to be 300 Hz. This cut-off frequency is a good trade-off since at this frequency, the noise can be effectively filtered out while the phase delay is not big.

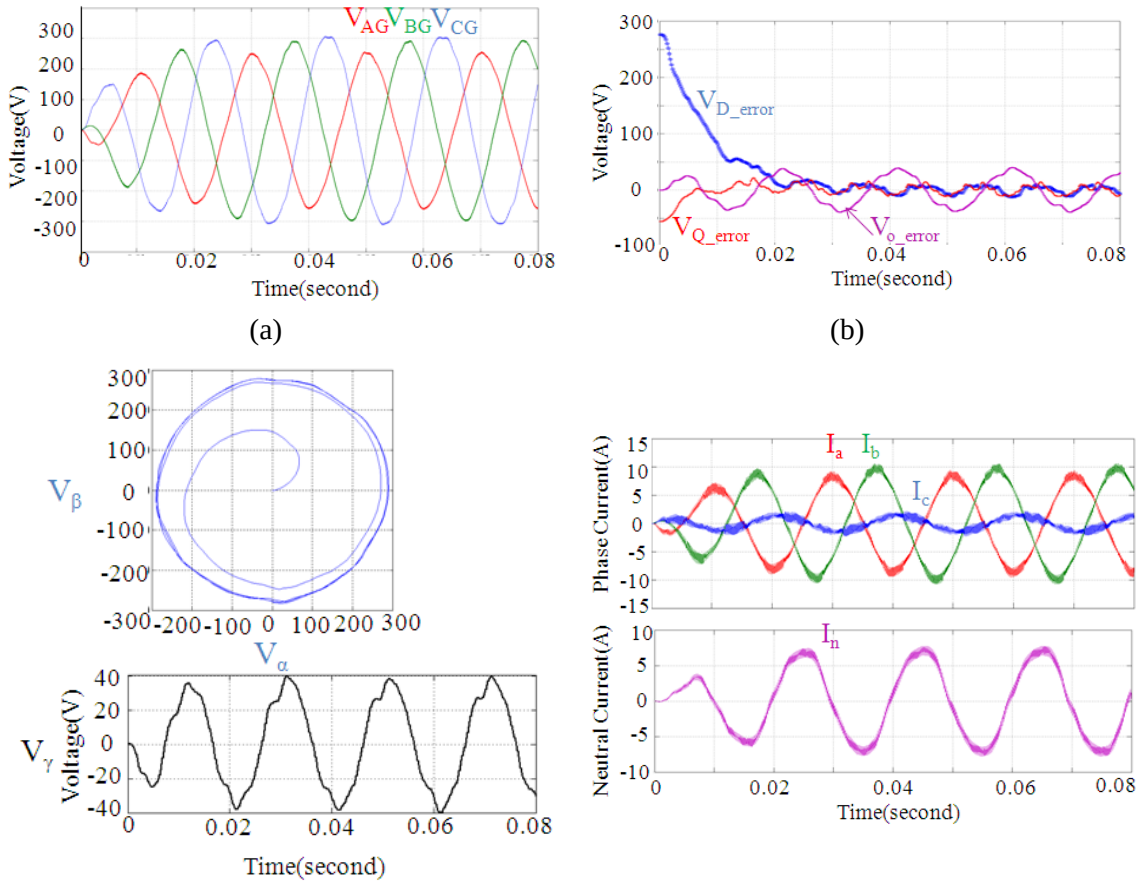



Figure 6.10 Simulated output of a four-leg VSI under voltage control under single phase unloaded condition; (a)Output phase voltages; (b)Error signals in channel *d*, *q* and *o* (c) trajectory of $\alpha$, $\beta$ and $\gamma$ components (d) Phase inductor currents and neutral current

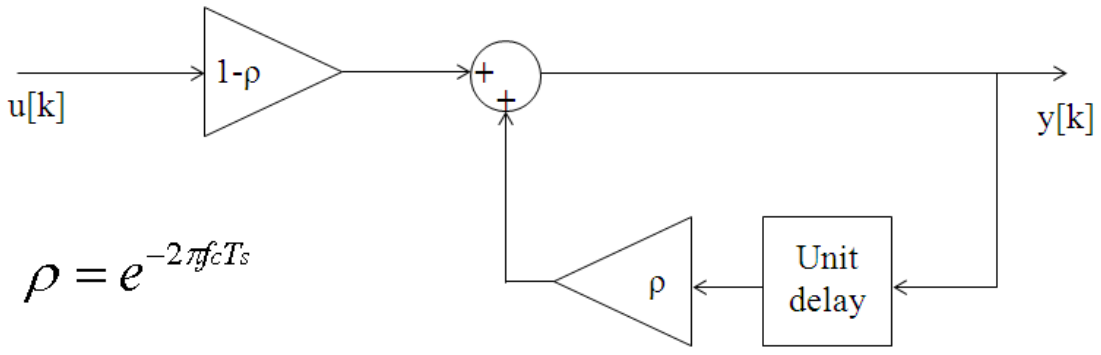



Figure 6.11Block diagram of a first order *RC* digital filter

### 6.2.5 Simulation results of the closed loop controller

So the current feed-forward term can be calculated based on the filtered inductor current, and they are added to the voltage control loop to compensate for the dynamic response of the system. The simulation result is shown in Figure 6.12. Compared to the results shown under voltage control alone, the controller design with the current feed-forward term has a better performance under single phase unloaded condition. The maximum output voltage difference is 10V, which is 3.5% of the rated output voltage. Without the current feed-forward term, the maximum output voltage is 45V, which is 15.9% of the rated output voltage. Also it can be seen from Figure 6.12(b) that the *o* channel error signal has been reduced dramatically, leading to a small voltage ripple on $V_\gamma$ (Figure 6.12(c)).

The control design has also been tested in another unbalanced load condition. In this case, an unbalanced load of $R_A$=30Ω, $R_B$ =45Ω, and $R_C$=45Ω has been selected, this will result in an unbalanced three-phase load current as $I_{LA}$=6.67 $\angle$ 0° A, $I_{LB}$=4.4 $\angle$ -120° A, and $I_{LC}$=4.4 $\angle$ -240°A.The simulated output voltage is shown in Figure 6.13(a). The phase current and neutral current are shown in Figure 6.13(d). The error signals in Figure 6.13(b) and the trajectory of the $\alpha$-$\beta$-$\gamma$ voltage components in Figure 6.13(c) show that the control loop can meet the design specification.

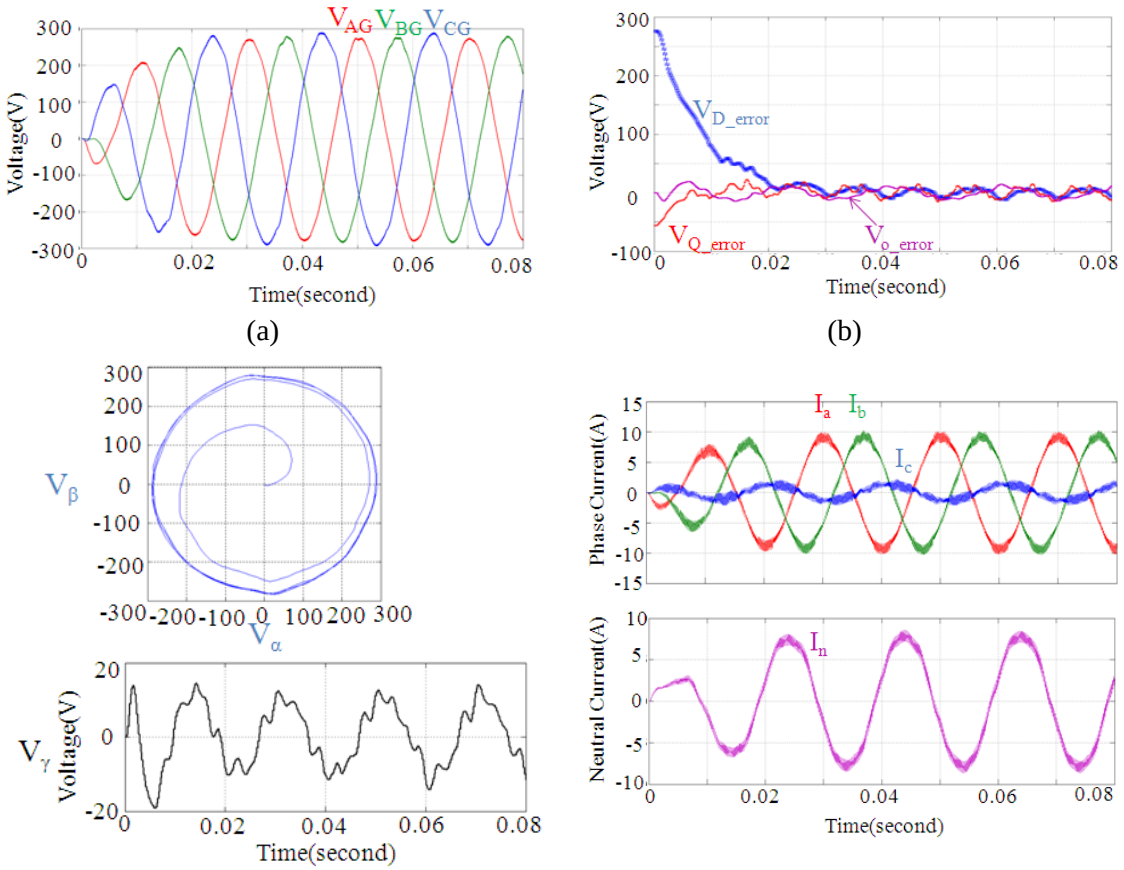



Figure 6.12 Simulated output of a four-leg VSI under voltage control with current feed forward term under single phase unloaded condition; (a)Output phase voltages; (b) Error signals in channel *d*, *q* and *o* (c) trajectory of *α*, *β* and *γ* components (d) Phase inductor currents and neutral current

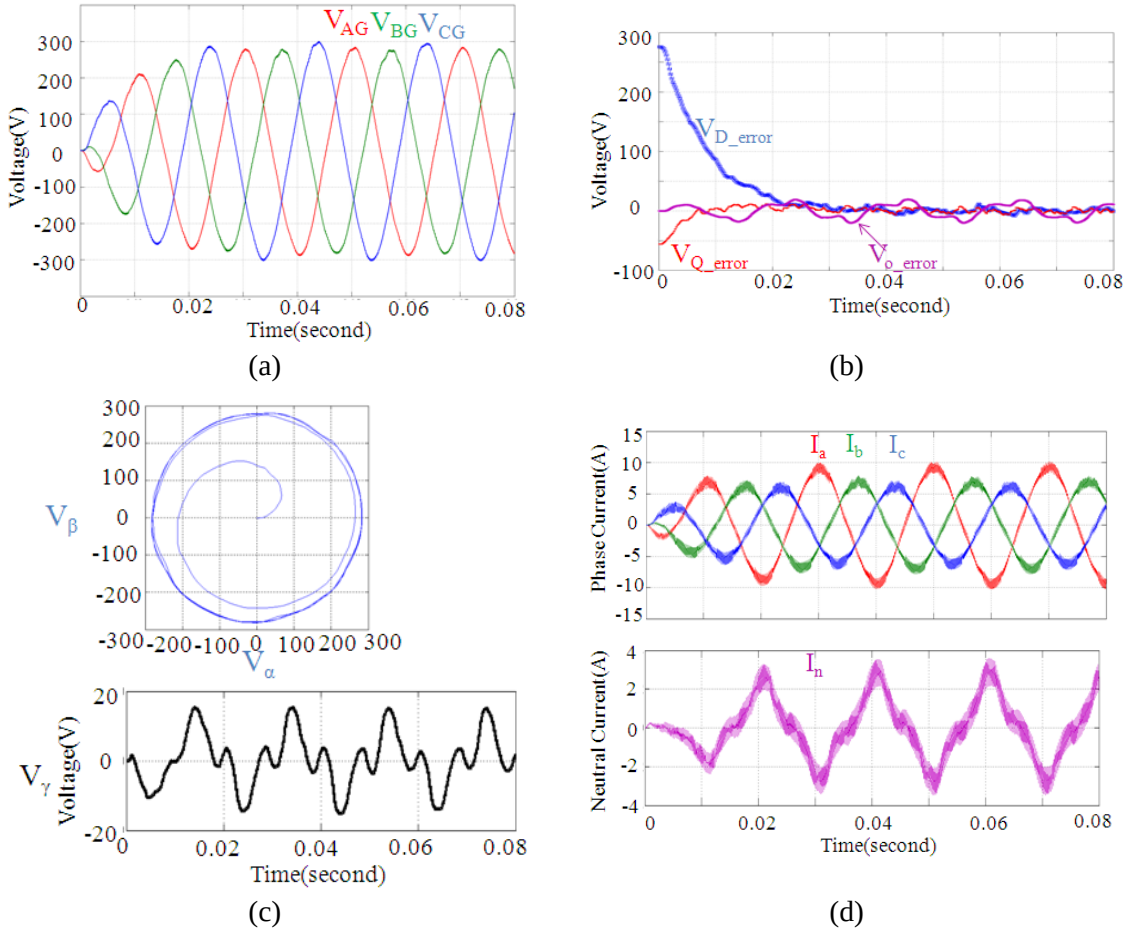



Figure 6.13 Simulated output of a four-leg VSI under voltage control under unbalanced load condition $R_A$=30Ω, $R_B$ =45Ω, and $R_C$=45Ω; (a) Output phase voltages;(b)Error signals in channel *d*, *q* and *o* (c) trajectory of *α*, *β* and *γ* components (d) Phase inductor currents and neutral current

## 6.3 Experimental results

A closed-loop laboratory test bench was set up as shown in Figure 6.14. Similar to the open-loop laboratory set-up, Code composer studio and a Labview based user control panel have been used to serve as a control panel. Three isolation amplifiers and three current sensors are used to sample the output voltage and current. The controller and digital filter algorithm are written in embedded C.

The controller parameters are tuned slightly based on the simulated controller parameters. The switching scheme for the control loop has been selected as zero-sequence component injected SVM since it obtains the merit of space vector and simple to implement as discussed in Chapter 5. Both conventional 3-D SVM and near-state 3-D SVM are implemented by using zero-sequence component injected method for demonstration purposes.

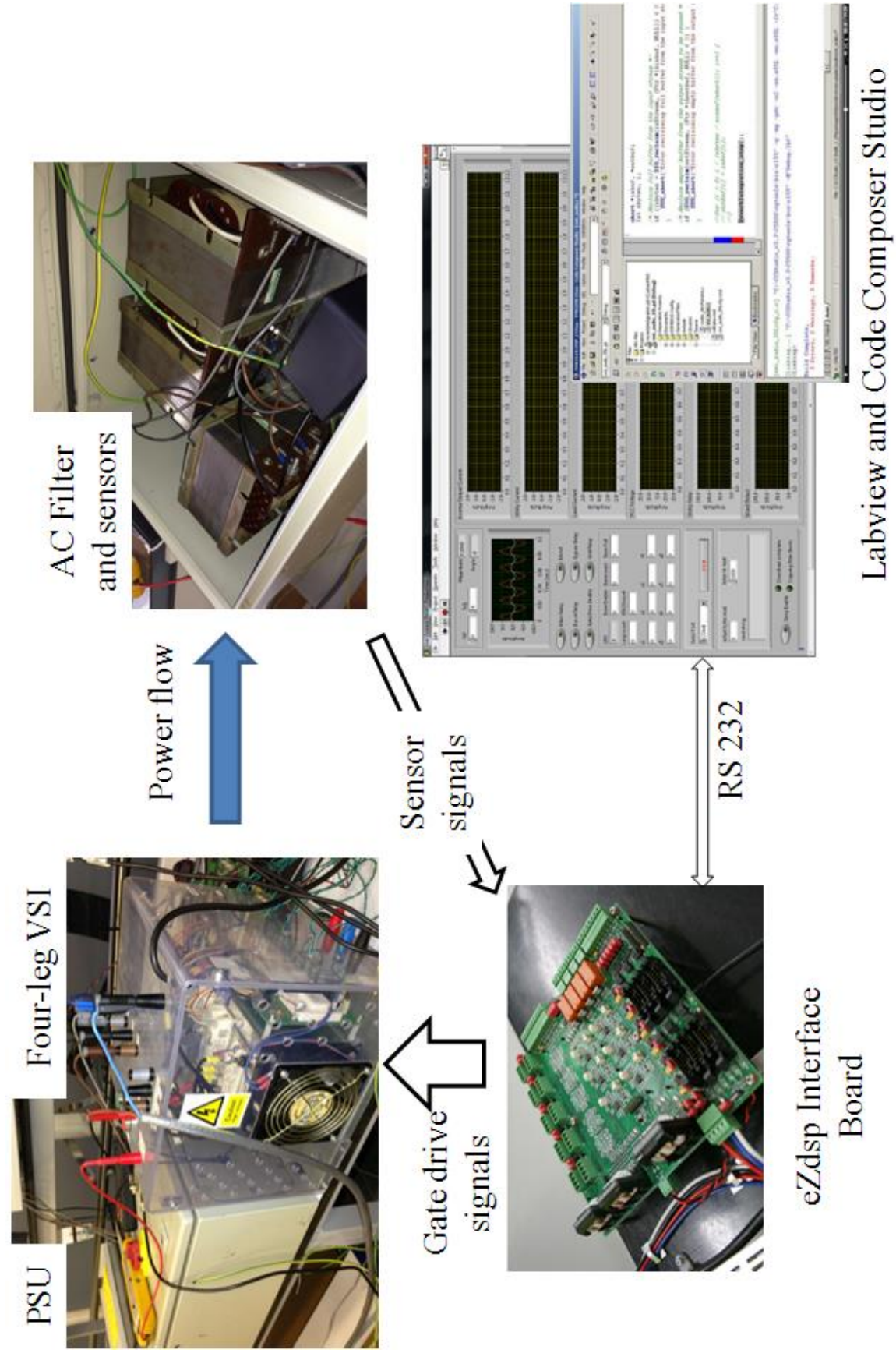


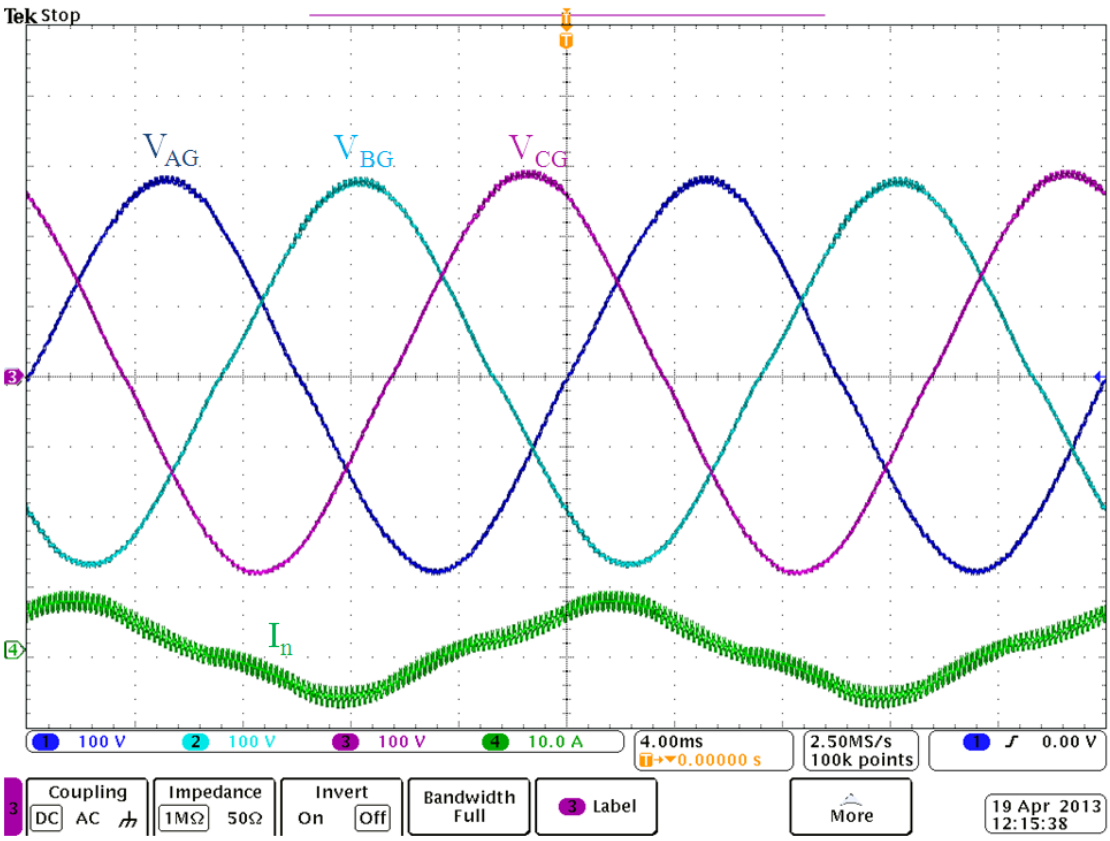

Figure 6.14 Laboratory test bench for a closed-loop four-leg VSI

### 6.3.1 Steady state performance under unbalanced load condition

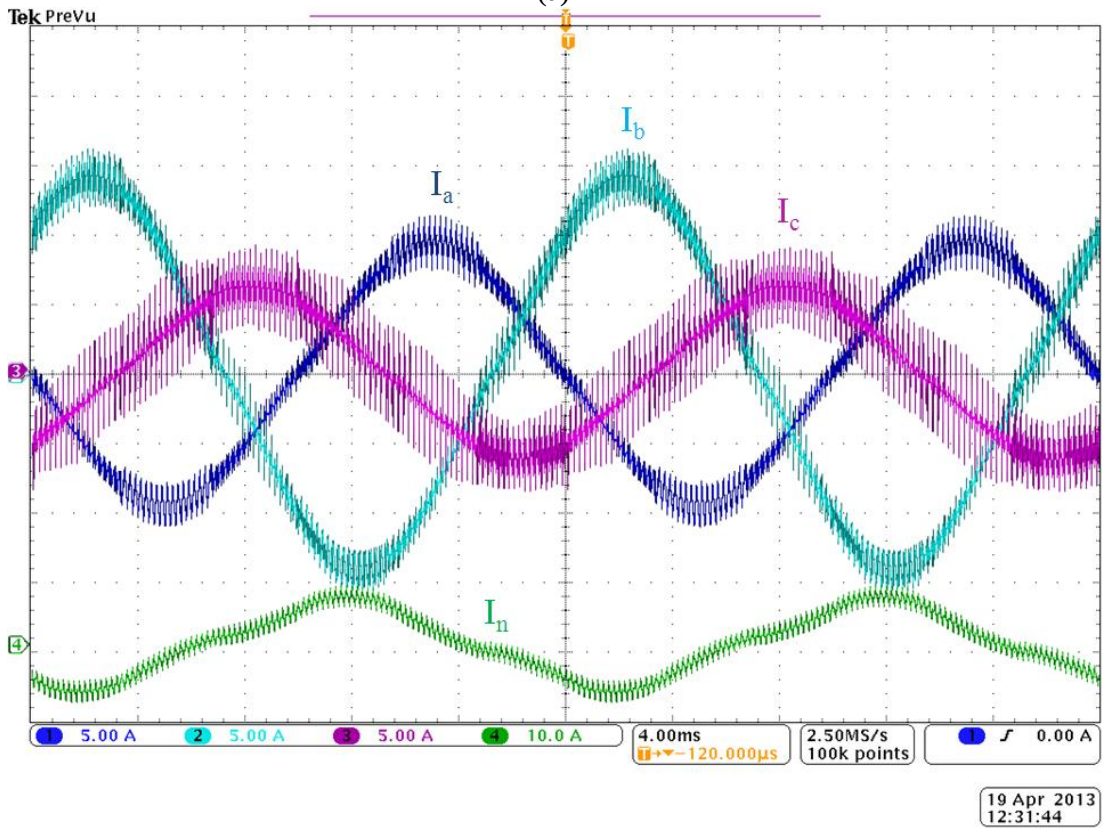
This section investigates the steady state performance of the designed controller under unbalanced load condition. An unbalanced load condition of $R_A$=30Ω, $R_B$ =20Ω, and $R_C$=45Ω has been selected, this will result in an unbalanced three-phase load current as $I_{LA}$=6.67 ∠ 0° A, $I_{LB}$=10 ∠ -120° A, and $I_{LC}$=4.4 ∠ -240°A.

Figure 6.15(a) shows the output voltage waveform under the unbalanced load condition while Figure 6.15(b) shows the three-phase inductor current and neutral current. A conventional 3-D SVM using zero-sequence injected SVM is selected as the switching scheme. As it can be seen, the steady state of the designed controller ensures a three-phase balanced output voltage.

Figure 6.16(a) and (b) show the output voltage waveform and inductor current waveform using zero-sequence injected near-state 3-D SVM.

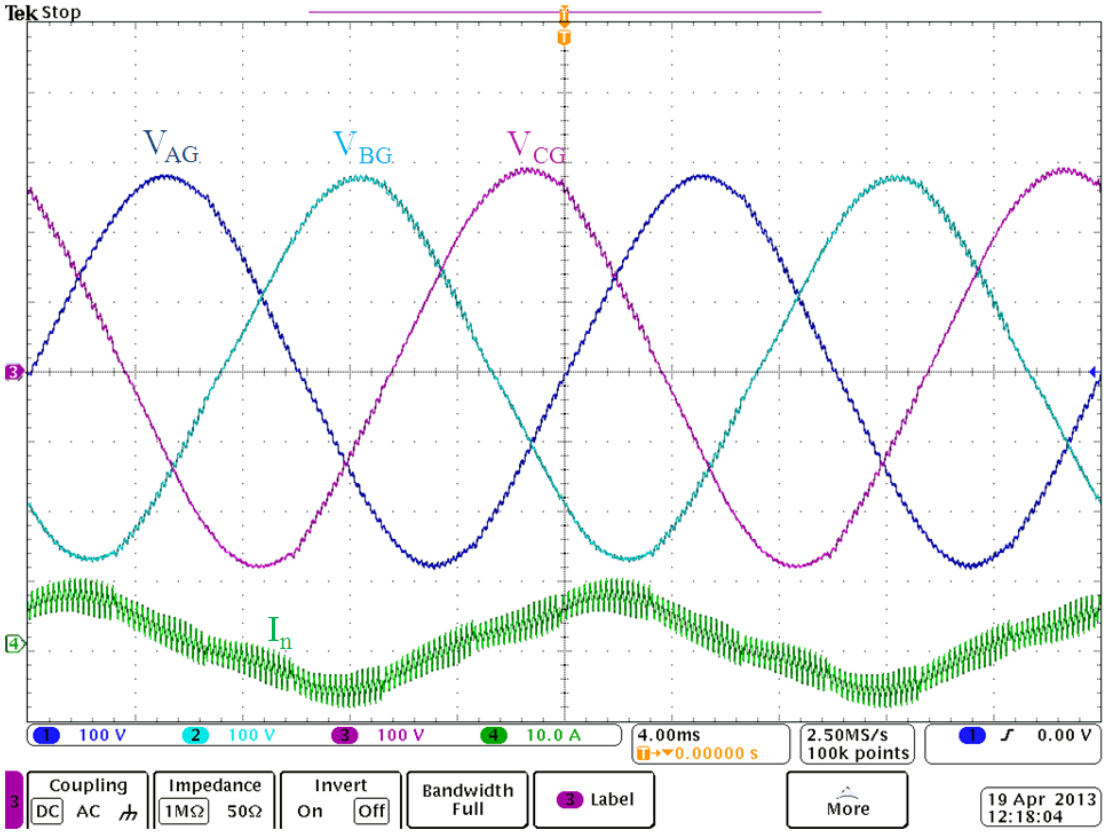



(a)

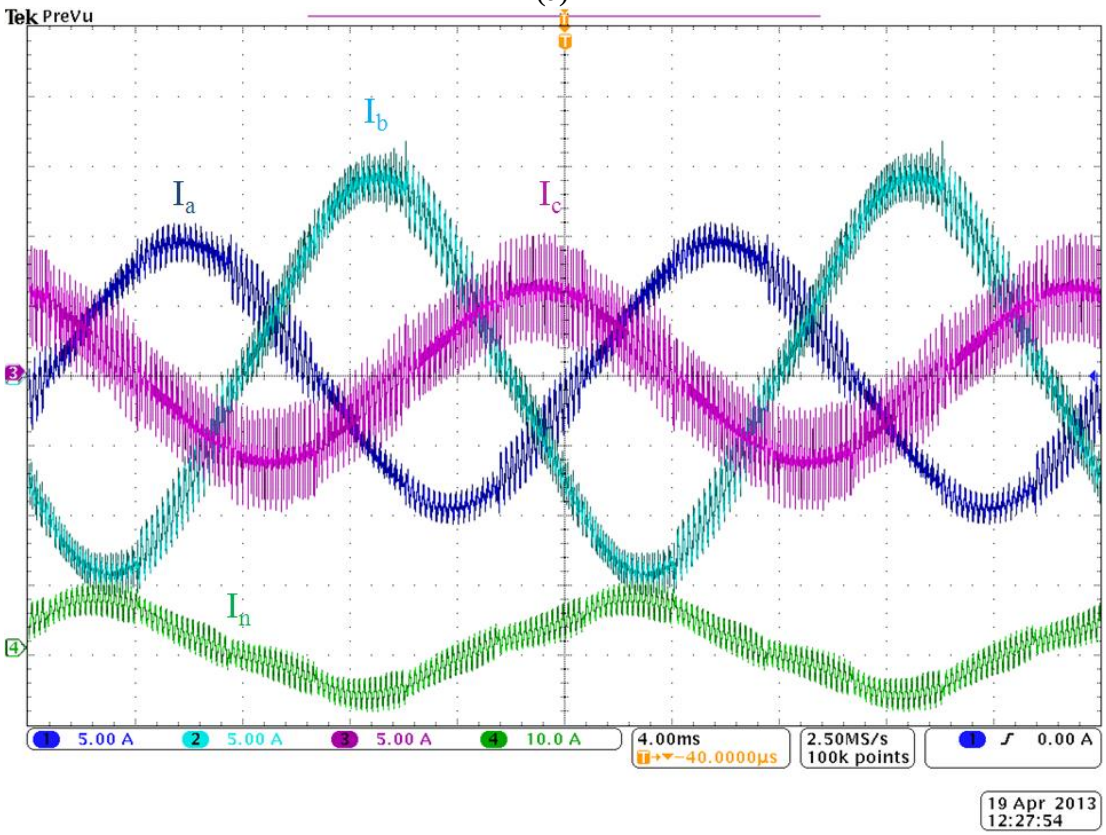



(b)

Figure 6.15 Experimental results under unbalanced load condition $R_A$=30Ω, $R_B$ =20Ω, and $R_C$=45Ω, zero-sequence injected 3-D SVM (a) Three-phase output voltage and neutral current (b) three-phase inductor current and neutral current




(a)




(b)

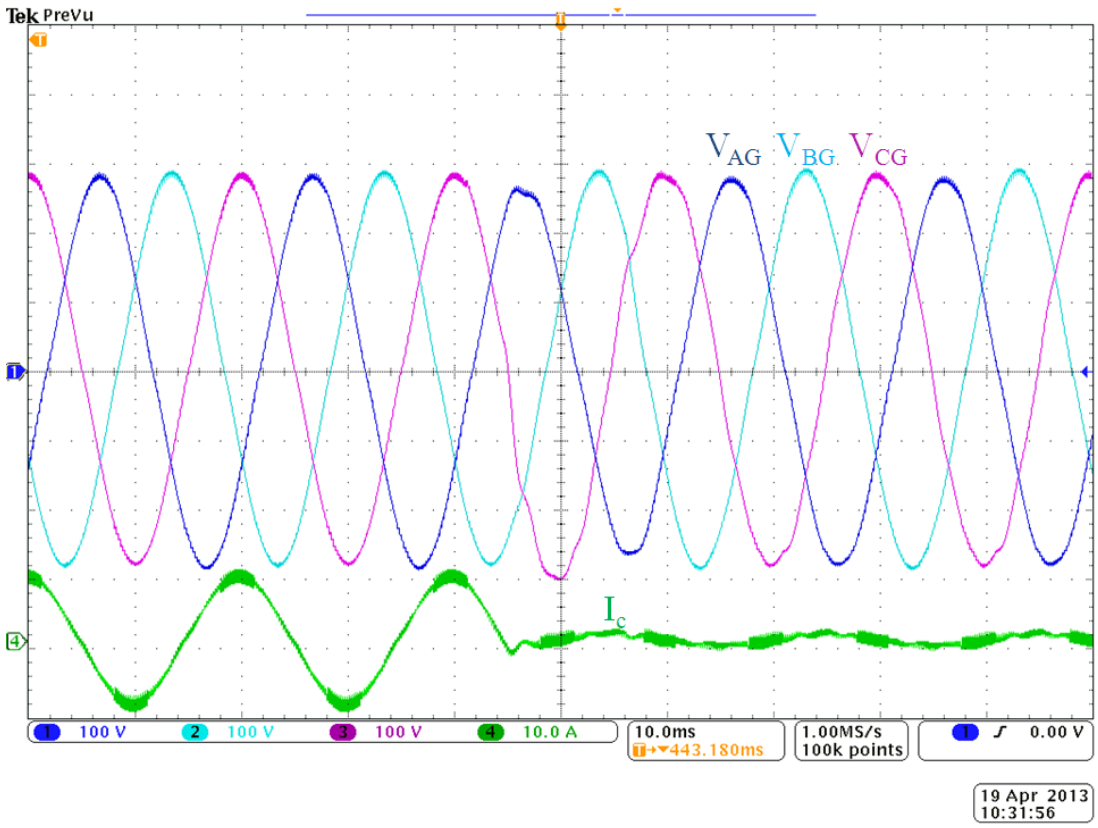
Figure 6.16 Experimental results under unbalanced load condition $R_A$=30Ω, $R_B$ =20Ω, and $R_C$=45Ω, zero-sequence injected near-state 3-D SVM (a) Three-phase output voltage and neutral current (b) three-phase inductor current and neutral current

### 6.3.2 Transient performance under unbalanced load condition

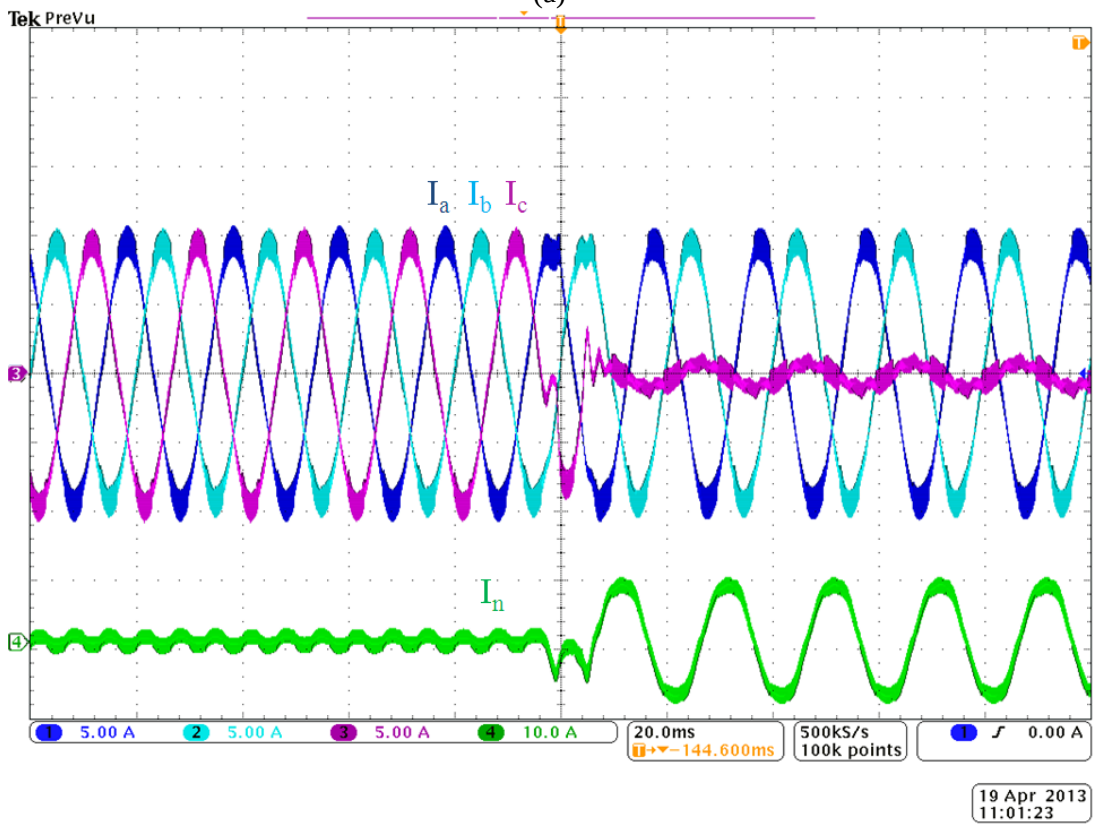
The transient performance under the designed control loop is investigated in this section. A transient situation has been created, during the time when the four-leg VSI was operating under a balanced load condition, phase C was then suddenly disconnected. Figure 6.17(a) shows the transient performance of the output voltage while (b) shows the transient of the phase current and neutral current. Zero-sequence injected 3-D SVM has been used as the switching scheme.

Figure 6.18(a) and (b) show the voltage and current transient under the zero-sequence injected near-state 3-D SVM.

The transient performance shown in Figure 6.17 and Figure 6.18 proves the effectiveness of the designed control loop. The maximum output voltage difference is very similar as the simulation result. A disturbance can be noted during the transient; however, it takes less than one power cycle for the disturbance to be corrected, which illustrates the fast dynamic behaviour by using the current feed-forward terms.

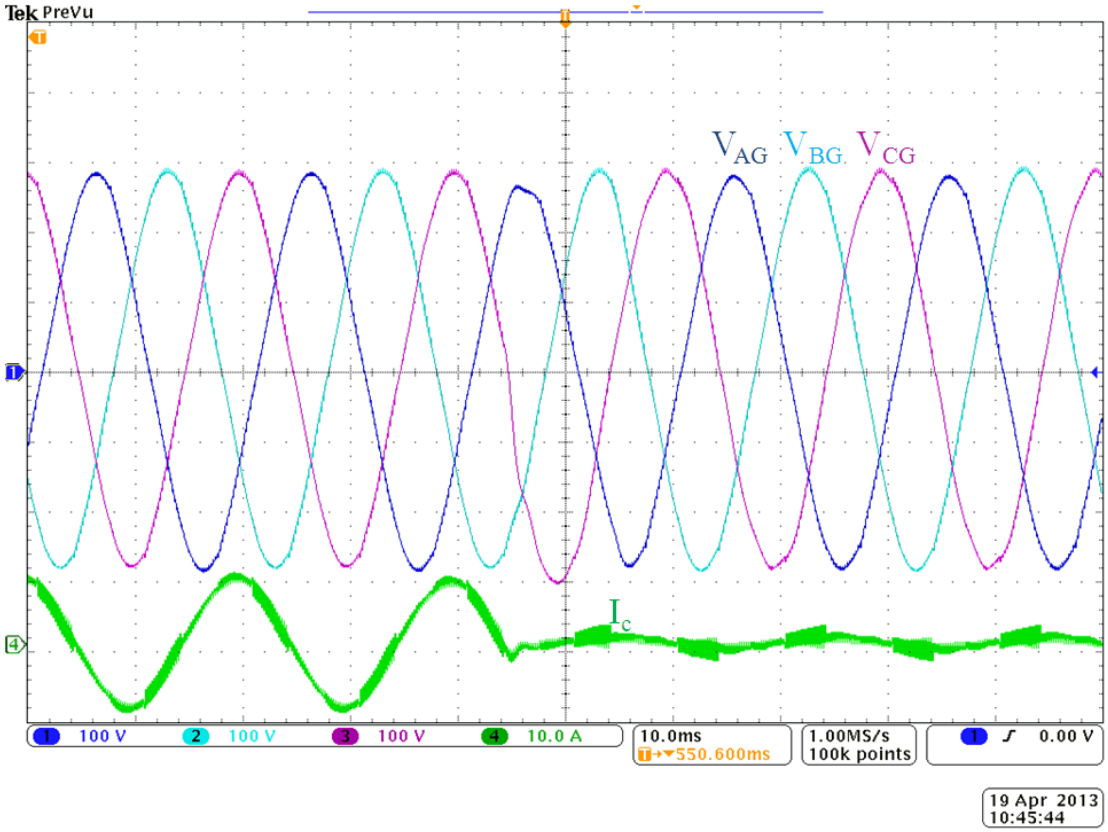



(a)

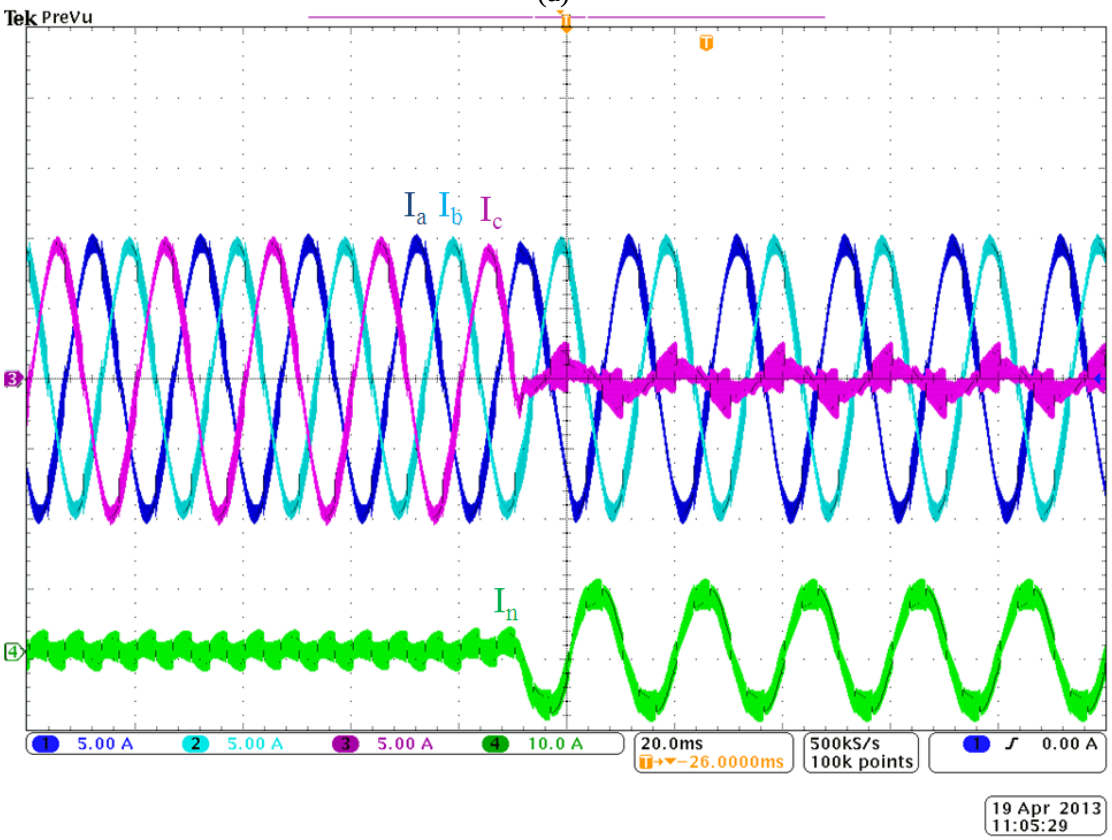



(b)

Figure 6.17 Transient operation of the four-leg VSI under single phase unloaded condition, zero-sequence injected 3-D SVM (a) Three-phase output voltage and phase C current (b) Three-phase inductor current and neutral current




(a)




(b)

Figure 6.18 Transient operation of the four-leg VSI under single phase unloaded condition, zero-sequence injected near-state 3-D SVM (a) Three-phase output voltage and phase C current (b) Three-phase inductor current and neutral current

## 6.4 Summary

In this chapter, a closed loop controller has been designed for a three-phase four-leg VSI. It has been found that the controller design based on the *d-q-o* coordinate is compatible with vector-based switching scheme; therefore a model of the four-leg inverter in a *d-q-o* coordinate has been studied first.

Based on the model in *d-q-o* coordinate, a voltage control loop has been designed in the discrete-time domain with the help of Matlab/Sisotool. The controller parameters are designed based on the light load condition to ensure the stability of the control loop. However, due to the low cut-off frequency of the closed loop transfer function, the dynamic performance has been suffered. The slow behaviour of the voltage controller struggled to cope with the voltage ripples caused by the unbalanced load current. Therefore, the filtered inductor currents are used as current feed forward terms. Simulation results show that under different unbalanced load conditions, the designed controller with current feed forward terms ensures a balanced output three-phase voltage.

Both steady state performance and transient performance of the designed control loop are tested in the laboratory test rig using the zero-sequence component injected method. The output voltage maintains balanced under unbalanced load condition. The transient behaviour of the inverter under the designed control loop shows a fast dynamic response to a sudden load change and quickly maintains the balanced output voltage.

# Chapter 7
# Conclusions

This chapter summarises the key points and important outcomes of the thesis. The available switching schemes for the four-leg VSIs are summarised and further improvements are suggested. The techniques, which are used in both simulation and experimental work, are presented to show how they are used to investigate different switching schemes. This chapter also includes suggestions for future work.

## 7.1 Three-phase four-leg VSIs

It has been found that three-phase four-leg voltage source inverters can supply balanced output voltages to the unbalanced loads. With the improvement of modern power electronics and the further cost reduction, it can be predicted that four-leg VSIs will be seen more often in a distributed power generation system. Compared to other power converter topologies, four-leg VSIs enjoy better control, reduced size and hence cost saving. The extra-leg gives the freedom for the control point of view, at the same time, increases the complexity of the switching schemes.

## 7.2 Switching schemes for four-leg VSIs

Compared to three-phase three-leg VSIs, the switching schemes for four-leg VSIs are limited for the reason that a four-leg inverter is used in a three-phase four-wire system in which the control targets are unbalanced load or nonlinear load.

Among the available switching schemes, the 3-D SVM is dominant. Other switching schemes, whether based on space vectors or based on scalar implementation, can only match the performance of the 3-D SVM. The proposed near-state 3-D SVM generates the same modulation index as the conventional 3-D SVM which means it inherits the merits of the 3-D SVM. Because the implementation requires switching pattern polarity change, the common-mode voltage level is reduced. The main advantage of the

proposed switching scheme is that it can reduce the common-mode voltage level, and at the same time maintain high DC link utilization. It also produces less switching loss and works under unbalanced load condition.

The drawbacks of the near-state 3-D SVM include limited operational range, increased harmonic contents in the inductor current. The limited operational range is not a significant issue in a distributed power generation system or high voltage level UPS system where most of the time the converter operates with a high modulation index value. The *L-C* filter of the four-leg VSI will filter out the switching noise caused by the near-state 3-D SVM; therefore the output voltage will not be degraded. However, the increased inductor current harmonics may result in increased losses.

This thesis also presents a simplified SVM switching scheme called zero-sequence injected PWM for a four-leg inverter. This switching scheme is based on the decoupled model of the four-leg inverter, and therefore represents the space vector on a *d-q* coordinate. Modulation for the fourth leg uses a zero-sequence injected method. This switching scheme simplifies the conventional 3-D SVM and the proposed near-state 3-D SVM. The experimental results show that the simplified switching scheme has the same performance as the 3-D SVM, and the control programme execution time has been reduced by almost 20%. Another advantage is that the simplified switching scheme is still based on space vectors; therefore control design can still be based on the DC operating point in a *d-q-o* coordinate.

## 7.3 Performance analysis for different switching schemes for four-leg VSIs

Performance analysis for a three-phase three-leg VSI has had much attention in the literature. Similar performance analysis is lacking for a four-leg inverter, especially for different switching schemes. Based on space vectors, the voltage harmonic distortion factor, inductor current harmonic distortion factor, conduction and switching loss of different switching schemes have been analyzed and compared.

Using the proposed analysis method, the performance of the two switching schemes, namely conventional 3-D SVM and near-state 3-D SVM were compared. A $k_v$-*M* curve shows the voltage harmonic content variation as the per-phase fundamental modulation index changes. An $I_B$-*M* curve shows the relationship between the inductor current

harmonic content and the modulation index value. Based on the $I_B$-$M$ curve, switching loss and conduction loss of the two switching schemes can be compared.

Under unbalanced load conditions, performance analysis becomes difficult and it depends on the various load conditions. It has been shown in this thesis that under unbalanced load conditions, since the output voltages are balanced, the $k_v$-$M$ curve can still be used for voltage harmonic content analysis. Also $I_B$-$M$ curve can be used to distinguish the current harmonic contents of different switching schemes.

Although it is difficult to calculate the exact switching power loss under unbalanced load conditions, in this thesis, several typical unbalanced load conditions are presented to show the relative switching loss.

## 7.4 Control loop design for four-leg VSIs

The control loop of the three-phase four-leg VSI is designed based on the mathematical model in a *d-q-o* coordinate. For a modern DSP-controlled system, the controller parameters are designed in a discrete time domain with the help of Matlab/Sisotool.

Under light load conditions, stability is the main concern when designing the controller. However, the low cut-off frequency of the closed-loop transfer function means the dynamic performance of the controller is not fast enough, therefore the inductor currents are used as the feed forward terms to compensate for the voltage controller.

Techniques such as controller output integration to the switching scheme, transformation between the two *d-q-o* coordinate, digital filter implementation, etc were used in the control loop design and real-time implementation.

Both simulation and experimental results show that the designed control loop ensures a balanced three-phase output voltage under balanced and unbalanced load conditions. Transient behaviour of the control loop is also tested with a sudden load change, and results show a good dynamic behaviour of the designed controller.

## 7.5 Future work

Areas for future work include:

- Investigate the impact on the DC link voltage ripple for different switching schemes.

- Design and develop a CMV reduced switching scheme in lower modulation index range. Combined with near-state 3-D SVM to achieve a full modulation range operation.
- Investigate the performance in over-modulation operation region.
- Dead time delay causes distortion on the top and zero crossing point of the voltage waveform. The larger the dead time delay is, the worse the distortion is. A dead time delay correction scheme for a four-leg VSI, especially with the near-state 3-D SVM switching scheme, is worthy of further research.
- For a severely unbalanced load, or nonlinear load, control schemes such as predictive control, or repetitive control are more compatible with the digital controller, therefore develop a model implementing these controllers may achieve good performance.
- A study of the relationship between the neutral current and load condition may produce a better controller design. The neutral current contains information on the load conditions[22], which may be used for better control design.
- Evaluate the performance of the scheme at a high voltage level more suitable for power system applications.

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# Appendix

## A. Projection of the reference vector

The calculation of the duration time or duty ratio relating to each switching vector is shown below. Taking Set A in Section I for instance, switching states $V_1$(pnpp), $V_2$(pnnp), $V_3$(pnnn) and $V_4$(ppnn) are selected. On the α axis, (A.1) can be written down

$$V_{\alpha\_ref} = d_1\frac{2}{3}V_{DC}\cos(\frac{\pi}{3}) + d_2\frac{2}{3}V_{DC} + d_3\frac{2}{3}V_{DC} + d_4\frac{2}{3}V_{DC}\cos(\frac{\pi}{3}) \quad \text{(A.1)}$$

Similarly, on the β coordinate,

$$V_{\beta\_ref} = -d_1\frac{2}{3}V_{DC}\sin(\frac{\pi}{3}) + d_4\frac{2}{3}V_{DC}\sin(\frac{\pi}{3}) \quad \text{(A.2)}$$

On the γ coordinate

$$V_{\gamma\_ref} = -d_1\frac{1}{3}V_{DC} - d_2\frac{2}{3}V_{DC} + d_3\frac{1}{3}V_{DC} + d_4\frac{2}{3}V_{DC} \quad \text{(A.3)}$$

Combined with (A.4)

$$d_1 + d_2 + d_3 + d_4 = 1 \quad \text{(A.4)}$$

A 4×4 matrix can then be calculated in Matlab as shown in (3.3)

## B. Techniques to obtain the execution time of controller code

There are two ways to detect the programme code execution time, software method and hardware method, and both methods should show the same result. The software method requires a DSP timer that will start counting the time when the programme starts and end counting when the programme ends. Using the information of the timer, the execution time can be obtained. For this project, a Labview block is used so as to monitor the real-time ISR running time.

Or alternatively, a GPIO pin could be initialized and used to be set high at the beginning of the execution code and set low at the end of the code, therefore a pulse could be observed using the oscilloscope. The GPIO 21 is used in this project.

**Initializing and using the timer**

A CPU timer0 is utilized to count the execution time, a period value is set up first and then the timer counts down if it starts working and stops at the stop value.

Put this code before the programme code

```
CpuTimer0Regs.TCR.bit.TRB = 1; // When write a 1 to TRB, the TIMH:TIM
is loaded with the value in the PRDH:PRD and the prescaler counter
(PSCH:PSC) is loaded with the value in the time divide-down register.
```

This code is at the end of the programme code

```
T0_count = CpuTimer0Regs.TIM.half.LSW; // since T0_count is defined as
Uint16, so only load the lower 16bits. T0_count value would be sent to
the Labview, where through some calculation; the execution time would
be calculated
```

The following code is used for initialization of the timer

```
void Timer0_init()
{
  // Set up CPU Timer 0
   CpuTimer0Regs.PRD.all = 0xFFFFFFFF;
   CpuTimer0Regs.TPRH.all = 0;
   CpuTimer0Regs.TPR.all = 0; // Cpu Timer Prescale and Divid-Down
   CpuTimer0Regs.TCR.bit.TIE = 0; // TIE= 0, the CPU-Timer interrupt
is disabled
   CpuTimer0Regs.TCR.bit.TSS = 0; // TSS = 0, Reads of 0 indicate the
cpu-timer is running
}
```

Once the value of T0_count is obtained, this value will then be passed to Labview, where through the following calculation, the execution time will be calculated.

Labview calculation

Execution time = (65536-T0_count) × 0.006666 μs

**Initializing and utilizing the GPIO**

A GPIO21 was initialized for monitoring the execution time

```
// Set up GPIO21 as a gpio output so as to monitor in the TP T5, this
pin is for estimating the execution time
   GpioCtrlRegs.GPAPUD.bit.GPIO21 = 0; // Enable pull up on GPIO21
   GpioDataRegs.GPACLEAR.bit.GPIO21 = 1; // Load output latch with 0
   GpioCtrlRegs.GPAMUX2.bit.GPIO21 = 0; // Used as a GPIO pin
   GpioCtrlRegs.GPADIR.bit.GPIO21 = 1; // As output signal
   EDIS;
```

At the beginning of the programme code

```
EALLOW;
   GpioDataRegs.GPASET.bit.GPIO21 = 1; // Load output latch with 1
EDIS;
```

At the end of the programme code

```
EALLOW;
   GpioDataRegs.GPACLEAR.bit.GPIO21 = 1; // Load output latch with 0
EDIS;
```

## C. Programming code for near-state 3-D SVM

Here presents part of the programming code for the near-state 3-D SVM. For demonstration purposes, programming code for [0° 90°] are shown here.

```
%%Ns 3-D SVM for four-leg inverter starts right from here

//Section BI, when the reference vector is in half of Section I

if(theta_e < 60)
   {
    // Calculating the duty ratios for each leg

   d1=(-3*v_alpha)/(2*v_dc) - (sqrt(3)*v_beta)/(2*v_dc) + v_dc/v_dc;
   d2=v_alpha/(2*v_dc) + (sqrt(3)*v_beta)/(2*v_dc)- v_gamma/v_dc;
   d3=(5*v_alpha)/(2*v_dc)-(sqrt(3)*v_beta)/(2*v_dc)+v_gamma/v_dc -
v_dc/v_dc;
   d4=(-3*v_alpha)/(2*v_dc) + (sqrt(3)*v_beta)/(2*v_dc) + v_dc/v_dc;


    // Sequencing the selected near-state switching vectors
   mi_A=1;
   mi_B=3750*(d1+d2+d3);
   mi_C=3750*d1;
   mi_f=3750*(d1+d2);

   // updating the modulation index value, sending values to the
//relevant registers, these won't be updated until the next PWM
   EPwm1Regs.CMPA.half.CMPA = mi_A;
   EPwm6Regs.CMPA.half.CMPA = mi_B;
   EPwm3Regs.CMPA.half.CMPA = mi_C;
   EPwm5Regs.CMPA.half.CMPA = mi_f;

// Setting the action qualifier registers properly
   EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
   EPwm1Regs.AQCTLA.bit.CAD = AQ_NO_ACTION;
   EPwm6Regs.AQCTLA.bit.CAU = AQ_SET;
   EPwm6Regs.AQCTLA.bit.CAD = AQ_CLEAR;
   EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;
   EPwm3Regs.AQCTLA.bit.CAD = AQ_SET;
   EPwm5Regs.AQCTLA.bit.ZRO = AQ_SET;
   EPwm5Regs.AQCTLA.bit.CAU = AQ_CLEAR;
   EPwm5Regs.AQCTLA.bit.CAD = AQ_SET;
 }


 //Section BII, when the reference vector lies in Section I and
Section II(30° to 90°)

if((theta_e<180)&&(theta_e>=60))
   {

DELAY_US(60); // This gives 60us delay

   d1=- (sqrt(3)*v_beta)/v_dc + v_dc/v_dc;
   d2=- v_alpha/(2*v_dc)+ (sqrt(3)*v_beta)/(2*v_dc) + v_gamma/v_dc;
   d3=(2*v_alpha)/v_dc + (sqrt(3)*v_beta)/v_dc - v_gamma/v_dc -
v_dc/v_dc;
   d4=- (3*v_alpha)/(2*v_dc)- (sqrt(3)*v_beta)/(2*v_dc) + v_dc/v_dc;

   mi_A=3750*(d1+d2+d3);
```

```
    mi_B=3750*d1;
    mi_C=3750;
    mi_f=3750*(d1+d2);

    EPwm1Regs.CMPA.half.CMPA = mi_A;
    EPwm6Regs.CMPA.half.CMPA = mi_B;
    EPwm3Regs.CMPA.half.CMPA = mi_C;
    EPwm5Regs.CMPA.half.CMPA = mi_f;

    EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
    EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
    EPwm6Regs.AQCTLA.bit.CAU = AQ_SET;
    EPwm6Regs.AQCTLA.bit.CAD = AQ_CLEAR;
    EPwm3Regs.AQCTLA.bit.ZRO = AQ_CLEAR;
    EPwm3Regs.AQCTLA.bit.CAD = AQ_NO_ACTION;
    EPwm5Regs.AQCTLA.bit.ZRO = AQ_CLEAR;
    EPwm5Regs.AQCTLA.bit.CAU = AQ_SET;
    EPwm5Regs.AQCTLA.bit.CAD = AQ_CLEAR;


    }
```

…….

Similar code would follow for the other sections.

## D. Calculation of the duration time for each switching state of a conventional 3-D SVM

The duration time of each switching state in a sampled PWM cycle can be obtained either by calculation based on Figure 4.1, or by the matrix that is for the specific tetrahedron. Take Tetrahedron 1 in Prism I for instance, $d_1$, $d_2$ and $d_3$ can be calculated as (D.1)

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} 1 & 0 & 1 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} \tag{D.1}$$

Since $V_{\alpha/\beta/\gamma}$ can be represented as (D.2)

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} \tag{D.2}$$

So $d_1$, $d_2$ and $d_3$ can be represented as (D.3)

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} \tag{D.3}$$

The three-phase output voltage can be represented as (D.4)

$$\begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \end{bmatrix} = \begin{bmatrix} M\frac{V_{DC}}{2}\cos(\omega t) \\ M\frac{V_{DC}}{2}\cos(\omega t - 2\pi/3) \\ M\frac{V_{DC}}{2}\cos(\omega t + 2\pi/3) \end{bmatrix} \tag{D.4}$$

Then the duration time can be calculated as (D.5)

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} \frac{M}{2}\cos(\omega t) \times \frac{T_{PWM}}{2} \\ -\frac{M}{2}\cos(\omega t - 2\pi/3) \times \frac{T_{PWM}}{2} \\ [\frac{M}{2}\cos(\omega t - 2\pi/3) - \frac{M}{2}\cos(\omega t + 2\pi/3)] \times \frac{T_{PWM}}{2} \end{bmatrix} \quad \text{(D.5)}$$

Then $t_Z$ can be calculated as

$$t_Z = \frac{T_{PWM}}{2} - t_1 - t_2 - t_3 = [1 - \frac{\sqrt{3}}{2} M \cos(\frac{\pi}{6} - \omega t)] \frac{T_{PWM}}{2} \quad \text{(D.6)}$$

## E. Calculation of the duration time for each switching state of a near-state 3-D SVM

Figure 4.2 shows the per-phase PWM output voltage levels of the 3-D SVM. Take Section I for instance, the duty ratio for each phase including the fourth leg can be obtained by (E.1)

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} -\frac{3}{2} & -\frac{\sqrt{3}}{2} & 0 & 1 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -1 & 0 \\ \frac{5}{2} & -\frac{\sqrt{3}}{2} & 1 & -1 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 & 1 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \\ V_{DC} \end{bmatrix} \tag{E.1}$$

Similar to conventional 3-D SVM, we have

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \\ V_{DC} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} & 0 \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \\ V_{DC} \end{bmatrix} \tag{E.2}$$

So $d_1$, $d_2$, $d_3$ and $d_4$ for Section I can be written as (E.3)

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} -1 & 0 & 1 & 1 \\ 0 & 0 & -1 & 0 \\ 2 & -1 & 0 & -1 \\ -1 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{AG} \\ V_{BG} \\ V_{CG} \\ V_{DC} \end{bmatrix} \tag{E.3}$$

The duration time for each switching state then can be calculated as (E.4)

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \frac{1}{V_{DC}} \begin{bmatrix} -V_{AG} + V_{CG} + V_{DC} \\ -V_{CG} \\ 2V_{AG} - V_{BG} - V_{DC} \\ -V_{AG} + V_{BG} + V_{DC} \end{bmatrix} \tag{E.4}$$

Simplified as (E.5)

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} [1 - \frac{\sqrt{3}}{2} M \cos(\frac{\pi}{6} - \omega t)] \frac{T_{PWM}}{2} \\ \frac{1}{2} M \sin(\frac{\pi}{6} + \omega t) \frac{T_{PWM}}{2} \\ [-1 + \frac{3}{2} M \cos(\omega t) - \frac{1}{2} M \sin(\frac{\pi}{6} + \omega t)] \frac{T_{PWM}}{2} \\ [1 - \frac{\sqrt{3}}{2} M \cos(\frac{\pi}{6} + \omega t)] \frac{T_{PWM}}{2} \end{bmatrix} \tag{E.5}$$

## F. Calculation of the conduction loss of the three-phase four-leg VSI

Assuming that the load condition is three-phase balanced linear loads, thus the neutral current that goes through the fourth leg is zero. The analysis is based on Phase A for demonstration purposes. Neglecting all the harmonic content of the phase current, which means the inductor current is assumed to be purely sinusoidal and it is given by (F.1)

$$i = I\cos(\omega t - \varphi) \tag{F.1}$$

where I is the peak phase current value and φ is the phase angle between the phase voltage and current, and according to the specification, φ is within the range of [0, π/3].

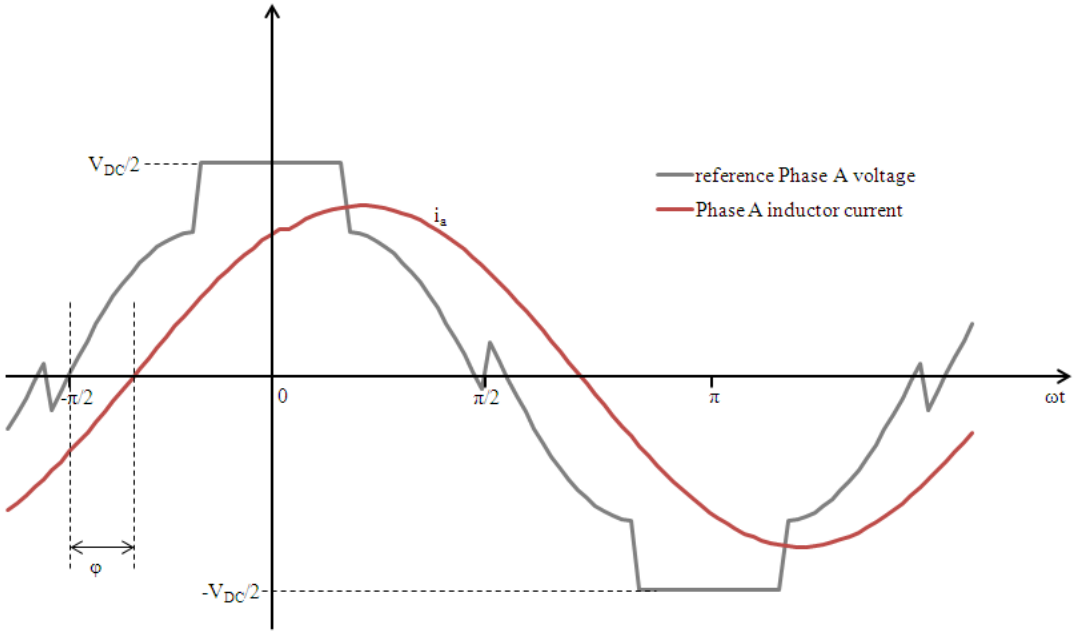


Figure F-1 Phase A reference voltage waveform and the phase A inductor current waveform

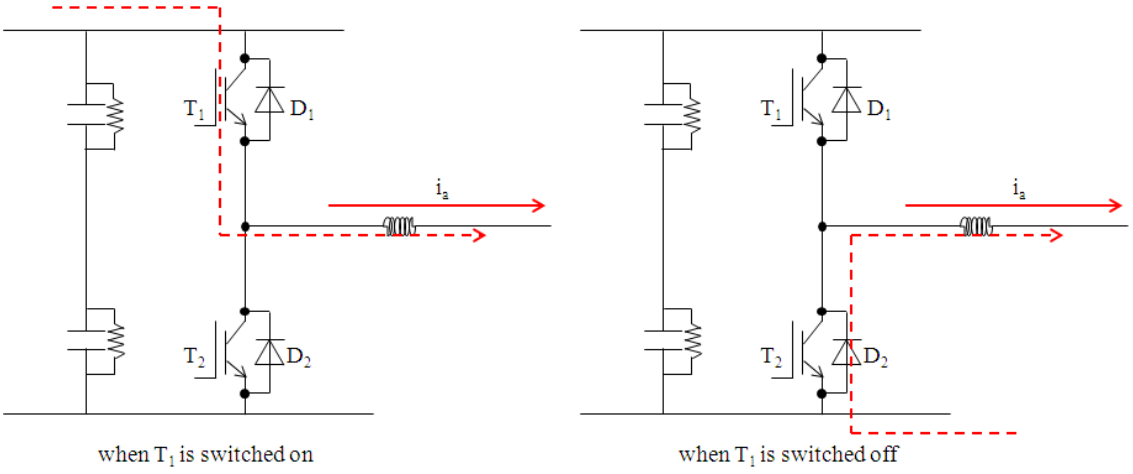


Figure F-2 Phase A current flow during the time when $T_1$ is on and off

According to Figure F-1 and Figure F-2, the on time of the top IGBT of phase A $T_1$ and bottom IGBT $T_2$ during phase current is positive can be calculated as

$$t_{T1on} = \frac{1}{2} + \frac{1}{2}\frac{v_{ao\_ref}}{V_{DC}/2} \tag{F.2}$$

$$t_{D2on} = \frac{1}{2} - \frac{1}{2}\frac{v_{ao\_ref}}{V_{DC}/2} \tag{F.3}$$

The voltage across the IGBT $T_1$ and free-wheeling diode $D_2$ can be expressed as

$$v_T = V_T + R_T i_T \tag{F.4}$$

$$v_D = V_D + R_D i_D \tag{F.5}$$

Therefore, during the time when Phase A current is positive, the conduction loss in IGBT $T_1$ can be obtained as

$$p_{T1} = t_{T1on}(V_T ia + R_T i_a^2) \tag{F.6}$$

The conduction loss in the free-wheeling diode $D_2$ can be obtained

$$p_{D2} = t_{D2on}(V_D ia + R_D i_a^2) \tag{F.7}$$

Therefore the average value of the conduction loss in T1 and D2 can be written as

$$P_{T1} = \frac{1}{2\pi}\int_{\varphi-\frac{\pi}{2}}^{\frac{\pi}{2}+\varphi} t_{T1on}(V_T ia + R_T i_a^2)\, d\omega t \tag{F.8}$$

$$P_{D2} = \frac{1}{2\pi}\int_{\varphi-\frac{\pi}{2}}^{\frac{\pi}{2}+\varphi} t_{D2on}(V_D ia + R_D i_a^2)\, d\omega t \tag{F.9}$$

Total conduction loss then

$$P_{conduction} = 6(P_{T_1} + P_{D_2}) \tag{F.10}$$

## G. Calculation of the switching loss of the three-phase four-leg VSI under unbalanced load condition

Two typical cases are investigated here as shown in the table below, Case (1) is the typical load power unbalance, while case (2) fills in the category of load power factor unbalance

**Table G-1 Two typical unbalanced load conditions**

| Load Conditions | *Unbal_N*% | Unbal_0% |
|---|---|---|
| (1) $\|I_{LA}\|=\|I_{LB}\|=I_m$, $I_{LC}=0$, $PF_A=PF_B=PF_C=1$; | 50% | 50% |
| (2) $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$ between 0.8 leading and 0.8 lagging | <=22.1% | <=22.1% |

Case 1:

**Table G-2 $|I_{LA}|=|I_{LB}|=I_m$, $PF_A=PF_B=PF_C=1$, $I_{LC}$ ranging from no load to full load**

| Load Conditions | *Unbal_N*% | Unbal_0% |
|---|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=PF_C=1$ | 0% | 0% |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.8I_m$, $PF_A=PF_B=PF_C=1$ | 7.15% | 7.15% |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.6I_m$, $PF_A=PF_B=PF_C=1$ | 15.4% | 15.4% |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.4I_m$, $PF_A=PF_B=PF_C=1$ | 25% | 25% |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.2I_m$, $PF_A=PF_B=PF_C=1$ | 36.4% | 36.4% |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0$, $PF_A=PF_B=PF_C=1$ | 50% | 50% |

**Table G-3 Neutral current under different load conditions**

| Load Conditions | Neutral Current |
|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=0$; |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.8I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=55/265=20.755\%\ I_m$ |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.6I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=112/265=42.26\%\ I_m$ |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.4I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=170/265=64.2\%\ I_m$ |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0.2I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=230/265=86.8\%\ I_m$ |
| $\|I_{LA}\|=\|I_{LB}\|=I_m$, $\|I_{LC}\|=0$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|=265/265=100\%\ I_m$ |

In order to analyze the switching loss, the phase currents and the neutral current under each load conditions have to be known and calculated.

The switching loss under the continuous PWM is calculated as:

$$\sum P_0 = 3 \times P_0 = 3 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times 2 \times \hat{I}_L \tag{G.1}$$

Since in this case, the generalized 3-D SVM generates the same modulation index as the standard 3-D SVM, the calculation is obtained as below:

$$\begin{aligned} \sum P &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{2\pi} \int_0^{2\pi} f_i(\omega t) d\omega t + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{2\pi} \int_0^{2\pi} f_i'(\omega t) d\omega t \\ &+ \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times 2 \times \hat{I}_n \end{aligned} \tag{G.2}$$

When $|I_{LC}|=0$,

$$\begin{aligned} \sum P &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \int_0^{2\pi} f_i(\omega t) d\omega t + 0 + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times 2 \times \hat{I}_L \\ &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times \hat{I}_L + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times 2 \times \hat{I}_L \\ &= 4 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times \hat{I}_L \end{aligned} \tag{G.3}$$

When $|I_{LC}|=0.5I_m$, $|I_n|=50\%\ I_m$

$$\begin{aligned} \sum P &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{2\pi} \int_0^{2\pi} f_i(\omega t) d\omega t + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{2\pi} \int_0^{2\pi} f_i'(\omega t) d\omega t \\ &+ \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times 2 \times \hat{I}_n \\ &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \hat{I}_L + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} 0.5 \times \hat{I}_L + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times 2 \times 0.5 \times \hat{I}_L \\ &= 3.5 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \times \frac{1}{\pi} \times \hat{I}_L \end{aligned} \tag{G.4}$$

When $|I_{LC}|=\rho I_m$, $|I_n|=(1-\rho)\ I_m$

$$\begin{aligned} \sum P &= 2 \times \frac{V_{DC} (t_{off} - t_{on})}{T_s} \frac{1}{2\pi} \int_0^{2\pi} f_i(\omega t) d\omega t + \frac{V_{DC} (t_{off} - t_{on})}{T_s} \frac{1}{2\pi} \int_0^{2\pi} f_i'(\omega t) d\omega t \\ &+ \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times 2 \times \hat{I}_n \\ &= 2 \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times \hat{I}_L + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times \rho \times \hat{I}_L + \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times 2 \times (1 - \rho) \times \hat{I}_L \\ &= (4 - \rho) \times \frac{V_{DC} \times (t_{off} - t_{on})}{T_s} \frac{1}{\pi} \times \hat{I}_L \end{aligned} \tag{G.5}$$

Case 2:

$|I_{LA}|=|I_{LB}|=|I_{LC}|=I_m$, $PF_A=PF_B=1$, $PF_C$ ranging from unity power factor to 0.8 Lagging.

**Table G-4 When $PF_C$=0.8 Lagging**

| Load Conditions | *Unbal_N*% | Unbal_0% |
|---|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=PF_C=1$ | 0% | 0% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.95 Lagging | 10.67% | 10.67% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.9 Lagging | 15.26% | 15.26% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.85 Lagging | 18.86% | 18.86% |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.8 Lagging | 22.1% | 22.1% |

**Table G-5 Neutral current under different load conditions**

| Load Conditions | Neutral Current |
|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|$=0; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.95 Lagging | $\|I_n\|$=84/265=31.7% $I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.9 Lagging | $\|I_n\|$=122/265=46.03% $I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.85 Lagging | $\|I_n\|$=142/265=53.585% $I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $PF_C$=0.8 Lagging | $\|I_n\|$=160/265=60.38% $I_m$; |

It can be seen that $|I_n| \approx 3 \times I_0$

**Table G-6 Neutral current under different $\varphi_C$ angle**

| Load Conditions | Neutral Current |
|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=PF_C=1$ | $\|I_n\|$=0; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C$=5° Lagging | $\|I_n\|$=22/270=8.15% $I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C$=10° Lagging | $\|I_n\|$=45/270=16.67% $I_m$; |

| | |
|---|---|
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C=15°$ Lagging | $\|I_n\|=72/270=26.67\%\ I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C=20°$ Lagging | $\|I_n\|=95/270=35.19\%\ I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C=25°$ Lagging | $\|I_n\|=116/270=42.96\%\ I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C=30°$ Lagging | $\|I_n\|=137/270=50.74\%\ I_m$; |
| $\|I_{LA}\|=\|I_{LB}\|=\|I_{LC}\|=I_m$, $PF_A=PF_B=1$, $\varphi_C=35°$ Lagging | $\|I_n\|=160/270=59.26\%\ I_m$; |

Therefore for continuous PWM:

$$\begin{aligned}\sum P_0 &= 3\times P_0 + P_0^{'} = 3\times \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times \hat{I}_L + \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times \hat{I}_n \\ &= 3\times \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times \hat{I}_L + \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times \sigma\times \hat{I}_L \\ &= (3+\sigma)\times \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times \hat{I}_L\end{aligned} \tag{G.6}$$

For 3-D SVM, conventional or near-state

$$\begin{aligned}&\sum P = 2\times \tfrac{V_{DC}(t_2-t_0)}{T_S}\tfrac{1}{2\pi}\int_0^{2\pi} f_i(\omega t)d\omega t + \tfrac{V_{DC}(t_2-t_0)}{T_S}\tfrac{1}{2\pi}\int_0^{2\pi} f_i^{'}(\omega t)d\omega t + \tfrac{V_{DC}(t_2-t_0)}{T_S}\tfrac{1}{\pi}\times 2\times \hat{I}_n \\ &= 2\times \tfrac{V_{DC}(t_2-t_0)}{T_S}\times\tfrac{1}{\pi}\times \hat{I}_L + \tfrac{V_{DC}(t_2-t_0)}{T_S}\times\tfrac{1}{\pi}\times \hat{I}_L \times[\int_0^{\frac{\pi}{3}-\varphi}\sin(\omega t)d\omega t \\ &+ \int_{\frac{2\pi}{3}-\varphi}^{\pi}\sin(\omega t)d\omega t] + \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times\sigma\times\hat{I}_L \\ &= 2\times \tfrac{V_{DC}(t_2-t_0)}{T_S}\times\tfrac{1}{\pi}\times \hat{I}_L + \tfrac{V_{DC}(t_2-t_0)}{T_S}\times\tfrac{1}{\pi}\times \hat{I}_L \times[2-\cos(\tfrac{\pi}{3}-\varphi)+\cos(\tfrac{2\pi}{3}-\varphi)] \\ &+ \tfrac{V_{DC}\times(t_2-t_0)}{T_s}\times\tfrac{1}{\pi}\times 2\times\sigma\times\hat{I}_L \\ &= \{1+0.5\times[2-\cos(\tfrac{\pi}{3}-\varphi)+\cos(\tfrac{2\pi}{3}-\varphi)]+\sigma\}\times\tfrac{V_{DC}(t_2-t_0)}{T_S}\times\tfrac{1}{\pi}\times 2\times\hat{I}_L\end{aligned} \tag{G.7}$$

There is relationship between $\varphi_C$ and σ.

For every $\varphi_C$, there is an σ.

It is worthwhile noticing that $|I_n|\approx 3\times I_0$

**Table G-7 Summary of zero-sequence unbalance and neutral current under different $\varphi_C$**

| Load Conditions | Unbal_0% | Neutral Current |
|---|---|---|
| $\varphi_C$=5° Lagging | 2.95% | 8.85% $I_m$ |
| $\varphi_C$=10° Lagging | 5.83% | 17.49% $I_m$ |
| $\varphi_C$=15° Lagging | 8.77% | 26.31% $I_m$ |
| $\varphi_C$=20° Lagging | 11.744% | 35.23% $I_m$ |
| $\varphi_C$=25° Lagging | 17.7546% | 44.264% $I_m$ |
| $_C$=30° Lagging | 17.77% | 53.32% $I_m$ |