

Complementary JFET Logic in Silicon Carbide

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Abstract

In the last decade or so, many prototype SiC devices and logic circuits have been demonstrated which have surpassed the performance of Si for the ability to function in extreme environments. The advance of silicon carbide technology has now reached a stage where commercialisation of high performance and energy efficient miniaturised devices and circuits is possible. These devices and circuits should be able to operate on the limited power resources available in harsh and hot hostile environments. These improvements require refining, experimenting and perhaps re-designing devices which can rightly claim their share in the current silicon dominant market. Consequently, there is a need for accurate simulation models for device engineers to understand device and circuit behaviour, examine performance trade-offs and verify the manufacturability of the design.

This work includes the first comprehensive study, to the author's knowledge, on the development and validation of 4H-SiC model parameters for high temperature, low power technology computer aided design (TCAD) finite element (FE) simulations. These model parameters are based on the physical and material properties of 4H-SiC and are derived from published data. The validation of these model parameters is performed using high temperature 4H-SiC lateral junction field effect transistor (JFET) data, fabricated and characterised by our group at Newcastle University.

TCAD tools and statistical techniques, such as design of experiment (DoE) and response surface modelling (RSM), play a key role in research to model and optimise semiconductor processes. These tools and statistical techniques also aid in studying the impact of process variability on device and circuit performance which ultimately affects the manufacturability and yield of the circuit. Based on TCAD tools and DoE and RSM statistical techniques, a

systematic methodology is devised to optimise high temperature, four terminal SiC JFETs. Using calibrated FE simulation model, enhancement mode 4H-SiC (normally off) n- and p-JFETs are optimised for operation in extreme environments. The normally-off nature of these devices is desirable for logic devices in terms of reduced gate drive complexity and power dissipation. Unlike previously reported devices, the optimised SiC JFETs are designed such that not only the gate length is reduced to 2 μm (in contrast to the 10 μm reported elsewhere), but are also able to operate over a temperature range of $-50\text{ }^{\circ}\text{C}$ to $600\text{ }^{\circ}\text{C}$ on a fixed voltage of 2 V, in contrast to the 20 V used in other work. Furthermore, the drain saturation current of the optimised JFETs increase with temperature which allows high on-to-off state current-ratio ($I_{\text{on}}/I_{\text{off}}$) at elevated temperatures. High $I_{\text{on}}/I_{\text{off}}$ is essential for low power logic circuitry with fast switching. At $500\text{ }^{\circ}\text{C}$, $I_{\text{on}}/I_{\text{off}} \sim 10^3$ for optimised (simulated) JFET as opposed to $< 10^2$ reported elsewhere. This is achieved by the choice of optimal gate bias, $|V_g| = 2\text{ V}$. The fourth, back-gate, terminal in the optimised JFET design provides an alternative route to tackle process variability. The effect of varying back-gate bias (V_{sub}) on the device performance parameters, such as threshold voltage (V_t), drain saturation current (I_{dss}) and channel leakage current (I_{off}) is also studied in detail.

Using enhancement mode n- and p-JFETs, logic circuitry based on 4H-SiC complementary JFET (CJFET) technology is described for the first time, to the author's knowledge. In order to assess the potential improvements in performance of digital logic functions as a result of using CJFET technology in their implementation, the static and dynamic characteristics of the most basic logic element, namely the inverter, are analysed using calibrated FE simulation model. The design and analysis of an inverter enables the design of more complex structures, such as NAND, NOR and XOR gates. These complex structures in turn form the building blocks for modules, such as adders, multipliers and microprocessors. The static and dynamic characteristics of CJFET logic inverters are analysed against operating frequency, temperature, supply voltage and fan-out. At $500\text{ }^{\circ}\text{C}$ and operating at a supply voltage of 2 V, the inverter has noise margin high = 0.36 V, noise margin low = 0.57 V, undefined

region = 0.51 V, propagation delay = 7ns, slew rate = 29.5 V/ μ s, maximum switching frequency = 10.6 MHz and static power = 353 nW. Apart from speed, these static and dynamic characteristics of the CJFET logic inverter, at 500 °C, are found to be comparable to those of silicon and strained silicon technology, at room temperature (RT). Currently, one of the biggest challenges faced by SiC technology in the development of complex ICs is high static power dissipation at 500 °C ($\sim 10^{-3}$ W). With the supply voltage scaled to 1 V, the static power of a CJFET inverter can further be reduced to 20.6 nW, but at an expense of degrading noise margin high to 0.15 V and noise margin low to 0.36 V.

Finally, in CJFET logic arrays, random variations in manufacturing process parameters can cause significant variations in neighbouring gates or transistors and, therefore, can largely be accountable for poor yield. Using DoE and RSM based statistical approach, the effect of ($\pm 10\%$) process variability on CJFET logic inverter's stability, in terms of noise margins, and efficiency, in terms of static power dissipation, are modelled and analysed at RT and 500 °C. It is found that the gate implant depth (t_g) and channel doping (N_D) have the most significant effect on the studied inverter *responses*. The fluctuation in these process parameters causes variations in threshold voltage (V_t) of the device which in turn affects the performance of the logic gate. However, these V_t variations can be tackled by the use of epitaxial gated devices which eliminate the issue of t_g variations and by the adjustment of back-gate biasing (V_{sub}). Furthermore, with the continuing advances in SiC wafer quality, with minimum tolerances, it is inevitable that soon SiC CJFET technology can be integrated with SiC gas sensors for monitoring extreme environments.

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Symbols and Abbreviations

ALU	Arithmetic Logic Unit
BJT	Bipolar Junction Transistor
CCD	Central Composite Design
CJFET	Complementary Junction Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
DoE	Design of Experiment
DTL	Diode-Transistor Logic
FCCC	Face Centred Central Composite design
FE	Finite Element
FF	Full Factorial design
IGBT	Insulated-Gate Bipolar Transistor
IIL	Integrated Injection Logic
JFET	Junction Field Effect Transistor
LED	Light Emitting Diode
MC	Monte Carlo
MESFET	Metal-Semiconductor Field Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
M-PRES	Multi-level Partitioned Response Surface
NM	Noise Margin
RS	Response Surface design
RSM	Response Surface Modelling
RT	Room Temperature
RTL	Resistor-Transistor Logic
SIMS	Secondary Ion Mass Spectrometry
TCAD	Technology Computer Aided Design
TTL	Transistor-Transistor Logic
VLSI	Very-Large-Scale Integration
VTC	Voltage Transfer Curve

N_A	Acceptor carrier concentration
V_{sub}	Back-gate bias
V_{subn}	Back-gate bias of n-JFET
V_{subp}	Back-gate bias of p-JFET
E_g	Bandgap
k	Boltzmann constant
V_{bi}	Built-in potential
I_{off}	Channel leakage current/Off-state current
E_c	Critical Breakdown Electric Field
N_c	Density of states in conduction band
N_v	Density of states in valence band
W_d	Depletion width
N_D	Donor carrier concentration
I_d	Drain current
I_{dss}	Drain saturation current
V_d	Drain voltage
μ_e	Electron mobility
n	Free electrons
p	Free holes
I_g	Gate current
V_g	Gate voltage
μ_h	Hole mobility
V_{IH}	Input Logic High Voltage
V_{IL}	Input Logic Low Voltage
n_i	Intrinsic carrier concentration
V_I	Inverter threshold voltage
f_{max}	Maximum switching frequency
NM_H	Noise Margin High
NM_L	Noise Margin Low
n_c	Number of centre runs
V_{OL}	Output Logic Low Voltage
V_{OH}	Output Logic High Voltage
ϵ_r	Relative dielectric constant

V_t	Threshold voltage
V_{tp}	Threshold voltage of p-JFET
V_{tn}	Threshold voltage of n-JFET

Chapter 1. Introduction

1.1 Silicon Carbide – A Brief History

Silicon carbide, a chemically bonded compound of silicon and carbon atoms, was first discovered in a laboratory experiment by Jöns Jacob Berzelius in 1824 [1]. More than half a century later, in 1885 Acheson carried out an experiment and mixed coke and silica in an electric smelting furnace which resulted in a product with great hardness, refractibility and infusibility [2]. He identified and named the Si and C compound “carborundum” and gave the chemical formula SiC. Since then SiC became well known for its robust properties and began to be used as an abrasive. Today, SiC is used for manufacturing various products requiring high endurance, including very hard ceramics used in applications such as car brakes/clutches/exhaust shield, domestic oven insulation, furnace and kiln back-up insulation, etc., see Figure 1.1.

Silicon carbide has been known as a semiconductor longer than silicon [3]. The first SiC light emitting diode (LED) was reported by Henry James Round in 1907 [4]. About half a century later, the interest in SiC as a semiconducting material was renewed in 1955 when J. A. Lely contributed in the development of SiC technology by presenting a new sublimation process of growing high quality SiC crystals [5]. However, soon after that, the difficulties in obtaining high purity SiC wafers shifted the interest towards silicon technology, with SiC research limited to former Soviet Union during the 60’s–70’s. During this period research mainly focused on the production of high quality, reliable SiC substrates. In 1978 there was a major breakthrough by Tairov and Tsvetkov who managed to produce high quality SiC substrates by seeded sublimation growth [6], followed by other notable growth contributions [7, 8].

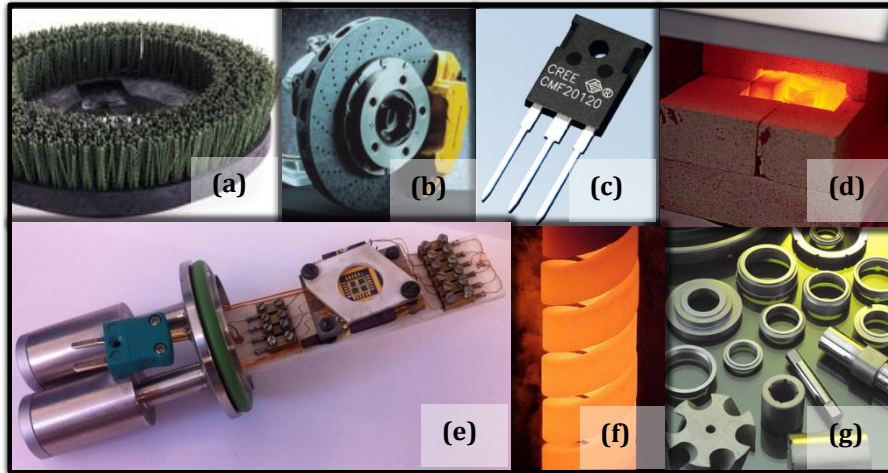


Figure 1.1. Various products made up of SiC: (a) abrasive, (b) brake disc and pads, (c) power metal-oxide-semiconductor field effect transistor, MOSFET, (d) furnace insulation, (e) gas sensor, (f) heating element; (g) seal faces [9-15].

In 1987, another major breakthrough was the first high quality off-axis epitaxy using “step controlled epitaxy” by the research group under R. F. Davis at North Carolina State University (NCSU) [16]. This discovery led to the formation of Cree Inc. [17], the current leader in SiC wafer fabrication and device manufacture, in 1989 by students from NCSU. During this time Cree manufactured the first commercial blue SiC LED from their high quality substrates and began to sell wafers. This marked a new era in SiC evolution. Since then extensive research has been conducted towards the advancement of SiC technology, in terms of improvements in wafer size and quality; along with fabrication of high temperature, radiation hard electronics for extreme environments. Currently, high temperature, SiC power devices [18, 19] are commercially available and are benefiting the power electronics sector, with the reduction in overall system size due to elimination of cooling requirements previously needed by Si based circuitry. A number of low power prototype devices and circuitry have also been reported over the past decade [20, 21]. These devices have operated successfully in high temperature, high-energy radiation and corrosive environments. However, with the current advance of SiC technology, the commercialisation of these devices demands optimisation of device dimensions and operating biases [21].

1.2 Logic Gates

Logic gates are the core of digital electronics. Every digital product, from computers and mobile phones to digital watches and calculators, contains logic gates. For example, logic gates are primarily used to carry out all the mathematical operations (arithmetic logic unit, ALU) and to store data (memory elements) in computing systems, to convert between analogue and digital signals for further signal processing in communication systems and as gate driver circuitry for controlling high power devices (e.g. MOSFETs, insulated-gate bipolar transistors, IGBTs, etc.) in power systems. Logic gates are usually designed by combining a number of transistors and/or resistors or diodes in a circuit, giving rise to different logic families. These logic families primarily differ from each other in terms of power consumption, speed, cost and size. There are several logic families, with further sub-variations in each one [22]. However, a few of the main types are briefly discussed in the following sub-sections:

Resistor-Transistor Logic (RTL)

The RTL family is the earliest class of transistorised digital logic and, as by name, is built using resistors and transistors (bipolar junction transistors, BJTs, MOSFETs, JFETs, etc.). The schematic of a simple two input RTL NAND gate is shown in Figure 1.2 (a). Here, R is the load resistor (pull-up device) and Q_1 and Q_2 are the enhancement mode n-MOSFETs (pull-down device). When both the inputs are high ($A = B = 1$), Q_1 and Q_2 are in conducting mode. Hence, most of the voltage ($\sim V_{dd}$) is dropped across R, giving a low logic level at the output ($O/P = 0$). Alternatively, when either of the two inputs are low ($A = B = 0$ or $A = 1, B = 0$ or $A = 0, B = 1$), Q_1 and/or Q_2 are in cut-off mode. Hence, most of the voltage ($\sim V_{dd}$) is dropped across the transistor(s), giving a high logic level at the output ($O/P = 1$). One of the advantages of RTL is its simplicity in logic design, requiring a minimum number of transistors for a logical function. However, the biggest disadvantage with RTL is high power dissipation in the pull-up resistor, making it unsuitable for complex logic functions.

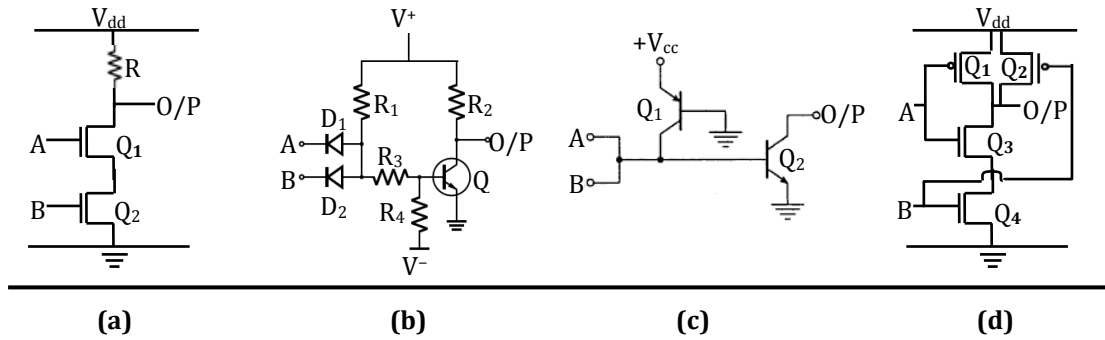


Figure 1.2. Schematics of two input NAND gate for different logic families, (a) resistor-transistor logic (RTL), (b) diode-transistor logic (DTL), (c) integrated injection logic (IIL) and (d) complementary metal-oxide-semiconductor (CMOS) logic.

Diode-Transistor Logic (DTL)

DTL is built from diodes, resistors and BJTs. The schematic of a two input DTL NAND gate is shown in Figure 1.2 (b). The circuit is divided into three stages: an input diode logic stage (R_1 , D_1 and D_2), a level shifter stage (R_3 , R_4 and V^-) and an amplification stage (R_2 , Q). When both the inputs are high ($A = B = 1$), the current due to V^+ is blocked through the reverse biased diodes and flows through R_3 , giving a high logic input to the transistor. Hence, with the transistor in conducting mode, the majority of the voltage ($\sim V^+$) is dropped across R_2 , giving a low logic level at the output ($O/P = 0$). Alternatively, when either of the two inputs are low ($A = B = 0$ or $A = 1, B = 0$ or $A = 0, B = 1$), the current due to V^+ flows through the forward biased diode(s) to ground. The current through R_3 is almost zero, giving a low logic input to the transistor. Hence, with the transistor in cut-off mode, most of the voltage ($\sim V^+$) is dropped across Q , giving a high logic level at the output ($O/P = 1$). DTL has a higher noise margin and greater fan-out capability than RTL. However, DTL suffers from low switching speed, especially when the transistor is being turned off.

Integrated Injection Logic (IIL)

IIL (or I^2L) consists of NPN and PNP BJTs. The schematic of a simple two input I^2L NAND gate is shown in Figure 1.2 (c). The inputs are connected to the base of NPN transistor (Q_2) and to the collector of PNP transistor (Q_1). Q_1 is called a current injector transistor because when its emitter is connected to an external

power source, it can supply current to the base of Q_2 . When both the inputs are high ($A = B = 1$), the current from the emitter of Q_1 is blocked from going towards the inputs and flows towards the base of Q_2 . This turns on Q_2 and allows all the current to sink to ground, giving a low logic level at the output ($O/P = 0$). Alternatively, when either of the two inputs are low ($A = B = 0$ or $A = 1, B = 0$ or $A = 0, B = 1$), the current from the emitter of Q_1 flows through the input(s). This transfers Q_2 to cut-off mode, giving a high, floating, logic level at the output ($O/P = 1$). I²L is suitable for very-large-scale integration (VLSI) as it has speed comparable to transistor-transistor logic (TTL) and dissipates power which is almost same as CMOS.

Complementary Metal-Oxide-Semiconductor (CMOS) Logic

CMOS logic is built using enhancement mode n- and p-type MOSFETs. The schematic of a simple two input CMOS NAND gate is shown in Figure 1.2 (d). The p-type MOSFETs, Q_1 and Q_2 , are connected in parallel; whereas the n-type MOSFETs, Q_3 and Q_4 , are connected in series. Each input is connected to the common gate of complementary pair. When both the inputs are high ($A = B = 1$), Q_1 and Q_2 are in cut-off mode ($V_{sg} \sim 0$ V), whereas Q_3 and Q_4 are in conducting mode ($V_{gs} \sim V_{dd}$). As a result, almost all of V_{dd} is dropped across Q_1 and Q_2 , giving a low logic level at the output ($O/P = 0$). Alternatively, when either of the two inputs are low ($A = B = 0$ or $A = 1, B = 0$ or $A = 0, B = 1$), Q_1 and/or Q_2 are in conducting mode ($V_{sg} \sim V_{dd}$), whereas Q_3 and/or Q_4 are in cut-off mode ($V_{gs} \sim 0$ V). Hence, most of the voltage ($\sim V_{dd}$) is dropped across Q_3 and Q_4 , giving a high logic level at the output ($O/P = 1$). In comparison to bipolar logic families, CMOS are simpler and inexpensive to fabricate, require much less power, have a better noise margin, a greater supply voltage range, higher fan-out capability and require much less chip area. However, they are slower in operating speed and are susceptible to static charge damage.

1.3 Scope of this Thesis

The objective of this study is to design and evaluate digital logic (based on enhancement mode SiC JFETs) for high temperature operation using TCAD FE

simulations. The current advances and challenges faced by SiC technology will be outlined in Chapter 2. A comparison of the superior material properties of SiC (allowing SiC electronics to function across a wide range of hostile environments) with leading semiconductor materials, such as Si and GaAs, will be presented. The need for sensor interface circuitry for monitoring hostile environments and the feasibility of using JFET device topology over MOSFET, metal-semiconductor field effect transistor (MESFET) and BJT device topologies will be discussed. The associated problem of high static power losses with current SiC logic families will be reviewed and the design and operation of CJFET logic for low power, sense interface electronics will be introduced. The advances in SiC wafer quality, along with the main types of process variations affecting device and circuit performance, will be reviewed. Finally, the role of TCAD FE computer simulations and the use of statistical techniques, such as DoE and RSM, for studying process variability and device optimisation will be discussed.

Chapter 3 will present the first comprehensive study, to the author's knowledge, on the development and validation of 4H-SiC model parameters for high temperature, low power TCAD FE simulations. A systematic methodology, based on TCAD simulations and DoE and RSM statistical techniques, will be utilised for optimising 4H-SiC enhancement mode JFETs for low power logic devices. The role of back-gate bias in the optimised JFET structure as a means to control process variability will be discussed. Finally, a comparison of some of the important performance parameters of the optimised n-JFET with comparable structures in literature will be presented.

In Chapter 4 the static and dynamic characteristics of 4H-SiC CJFET logic inverter will be studied, using calibrated FE simulations, to assess the potential improvements in performance over previously reported SiC logic families. The possibility of performance enhancements in 4H-SiC CJFET logic at high temperatures, in terms of reduced power dissipation with enhanced switching speed, will be analysed. Finally, the feasibility of SiC CJFET ICs to achieve high circuit complexities with low power consumption at 500 °C will be examined.

Chapter 5 will bind the work presented in previous two chapters. Using DoE and RSM statistical techniques under TCAD framework, the effect of manufacturing process variations on the performance of CJFET logic inverter, studied in Chapter 4, (as a result of subsequent variations in the geometric structure/doping profile and, hence, the electrical characteristics of the optimised JFET structure, studied in Chapter 3) will be modelled and analysed at RT and 500 °C. The model will be used to identify the key process parameters affecting the noise margins and static power dissipation of CJFET logic inverter. Finally, different approaches for tackling variability of these identified key parameters will be examined to improve the overall functional and parametric yield of CJFET ICs.

A summary of the work will be given in Chapter 6. The use of enhancement mode JFETs and CJFET logic for high temperature sensor interface digital electronics will be evaluated and the implications of further device scaling and process variations will be discussed. The thesis will conclude with suggestions for extending this work and predictions for future research.

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Chapter 2. State of the Art

This chapter presents a review on the current advances and challenges faced by SiC technology, with the main focus on SiC logic devices for hostile environments. The chapter is divided into six sections. Section 2.1 presents a brief introduction to the properties of SiC which enable electronics to function across a wide range of applications in high temperature, high radiation and corrosive environments, beyond the scope of narrow bandgap technologies. The feasibility of using JFET device topology for high temperature electronics and the issues with other device topologies is discussed in Section 2.2. Section 2.3 begins with a review of the current state of SiC logic devices. To tackle high power losses in current SiC logic families, the design and operation of CJFET logic is subsequently introduced in Section 2.3. Section 2.4 outlines: the advancement in SiC wafer quality, the main types of process variations affecting device structure; device and circuit performance and the role of TCAD for tackling process variability and device optimisation. The statistical techniques to model and analyse the effect of process variations on device and circuit performance are discussed in Section 2.5. Finally, the chapter is concluded with an overall summary and thesis motivation in Section 2.6.

2.1 SiC for High Temperature Electronics

Silicon carbide is actively being researched around the globe for the development of high temperature, radiation hard and corrosion resistant electronics [1]. The superior material properties of SiC, in comparison to other semiconducting materials (such as Si, GaAs, etc.), enables SiC electronics to function across a wide range of hostile environments. A comparison of some of the physical and electrical properties of SiC with other semiconductors is given in Table 2.1. Among all the material properties, the wide bandgap and, hence, the low intrinsic carrier concentration of SiC are the key feature to allow the

realisation of high temperature electronics. The relationship between intrinsic carrier concentration, temperature and bandgap is given by equation 3.2, in Chapter 3, which shows that intrinsic carrier concentration increases exponentially with temperature.

Property	Si	GaAs	4H-SiC	6H-SiC	3C-SiC
Bandgap, E_g (eV)	1.12	1.42	3.23	3.0	2.36
Relative Dielectric Constant, ϵ_r	11.9	13.1	9.66	9.66	9.72
Breakdown Electric Field, E_c (M V cm ⁻¹)	0.25	0.3	2.2	2.5	1.2
Thermal Conductivity (W cm ⁻¹ K ⁻¹)	1.5	0.5	3.7	4.9	3.6
Intrinsic Carrier Concentration, n_i (cm ⁻³)	10 ¹⁰	1.8×10 ⁶	5.0×10 ⁻⁹	2.3×10 ⁻⁶	1.5×10 ⁻¹
Electron Mobility, μ_e (cm ² V ⁻¹ s ⁻¹) @ $N_D = 10^{16}$ cm ⁻³	1200	6500	800	400	750
Hole Mobility, μ_h (cm ² V ⁻¹ s ⁻¹) @ $N_A = 10^{16}$ cm ⁻³	420	320	120	90	40
Saturated Electron velocity, (10 ⁷ cm s ⁻¹)	1.0	1.2	2.0	2.0	2.5
2012 Commercial Wafer Diameter (cm)	30	15	10	10	10

Table 2.1. Comparison of material properties of SiC polytypes with different semiconductors at 300 K [2-5].



Figure 2.1. Silicon carbide could have applications in high temperature, radiation hard electronics for spacecraft envisioned for both inner and outer solar system missions (right), predicting volcanic eruptions (centre) and monitoring exhaust gases (left) [6-8].

At RT, the bandgap of SiC is almost three times that of Si, whereas the intrinsic carrier concentration in SiC is nineteen orders of magnitude lower than that in Si. At high temperatures (around 125 °C) the intrinsic carrier concentration in Si increases beyond the doping concentration of low doped regions ($\sim 10^{12} \text{ cm}^{-3}$), resulting in uncontrolled device behaviour. In SiC, however, this matching of intrinsic carrier concentration with minimum doping density ($\sim 10^{14} \text{ cm}^{-3}$ [9]) happens at a much higher temperature (above 1000 °C), enabling SiC electronics to function at high temperatures.

There are many high and low power applications where silicon carbide electronics is useful [1, 10-12]. Among them one application where SiC is making a big impact is high temperature gas sensors for monitoring harsh and hot hostile environments [12, 13]. SiC gas sensors could be used in a number of systems, from monitoring pollutants released in car exhaust gases and jet engines to making measurements in planetary atmospheres and inside the vents of volcanoes, see Figure 2.1. A few examples are discussed below.

SiC sensors have the ability to distinguish different gases at high operating temperatures. Furthermore, a typical SiC gas sensor is around 100µm across and a fraction of a millimetre thick [14]. These features allow arrays of SiC gas sensors to be placed inside hot areas of aircraft and automobiles (where the temperature goes above 400 °C) for monitoring of pollutant gases released into the atmosphere. These gas sensors could also be used to check for un-burnt fuel and feed the information back to the aircraft/automobile engine-management system to control the flow of fuel in the cylinders, improving fuel economy and,

hence, reducing cost. In contrast, the use of silicon based microelectronic integrated circuits to monitor and/or control crucial hot sections of aircraft/automobiles either require the circuitry to be placed at cooler areas, or require active cooling through pumping cool air/liquid into the system. This reduces accuracy of the monitored data and introduces additional overhead to the system, in the form of longer wires, extra connectors, and/or cooling system plumbing, resulting in addition of undesired size and weight to the system. Consequently, the overall system becomes very complex with increased chances of potential failures.

There are almost 500 million people living in areas that are immediately at risk from volcanic activities [12]. Therefore, it is vital to be able to predict when an eruption is likely to happen. Corrosive gasses, such as SO₂, HCl, HF and H₂S, are found inside volcano vents at temperatures around 400 °C. The concentration of these emitted gases change dramatically before an eruption [15]. Scientists find this information useful for predicting eruptions. Currently, monitoring of these gas levels can be performed in two ways: (1) from manually extracted gas samples and analysing them in a laboratory by means of mass spectrometry (which present health risk and do not provide real time data), or (2) from optical absorption measurements [16] (which struggles to measure the low quantities of the relevant gases samples and require high power source at the volcanoes vents). SiC sensors, on the other hand, could be deployed into the vents itself to provide direct, real-time monitoring of the emissions [12]. The real-time monitoring of gasses, however, requires these sensor devices to be both sufficiently sensitive and selective for the gas species of interest.

The above examples demonstrate the importance of SiC gas sensors for monitoring hostile environments. However, for efficient operation of these sensors, the collected data must be relayed wirelessly to the host computer for monitoring [10]. This leads to the need for sensor interface circuitry, comprised of amplifier circuitry for amplification of the signal collected by the sensors, digital circuitry for digitisation of data and transmission circuitry for wireless transmission of digital data. The challenge now is to integrate the sensors with

electronics that can handle such extreme conditions. If the circuitry necessary to support these sensors can be developed, then SiC sensors may soon take their place in extreme environments from volcanoes to Venus. This work focuses on the digital aspect of the sensor interface circuitry.

2.2 Feasibility of SiC JFETs for High Temperature Electronics

As discussed previously in Section 2.1, there is a need for high temperature sensor interface electronics which can operate above 400 °C. This section outlines the current state and challenges faced by different SiC device topologies; along with the feasibility of using JFET device topology for high temperature sense interface electronics in the nearer term.

MOSFET

SiC MOSFET [17] is dominant in applications requiring fast switching speeds, as compared to other device topologies [10]. However, with the current state of dielectric processing, MOSFETs are not suitable for high temperature operation above 300 °C [18, 19]. The high quality thermal oxide required by MOSFETs is hard to achieve in SiC [13]. This oxide degrades with increase in temperature, leading to degradation in device threshold voltage (V_t), such as -14 mV/°C above 200 °C reported in [20]. Although experience from Si electronics dictates that complementary MOSFET (CMOS) technology is ideal for developing integrated circuits, the development of high quality thermal oxide in SiC, capable of long term operation at high temperatures, seems difficult to achieve in the nearer term [13].

MESFET

MESFETs [17], on the other hand, have also shown reliability issues for long term operation at high temperatures [13]. SiC MESFETs suffer from high gate leakage from Schottky diode, limiting usable operation to around 400 °C [21].

BJT

BJT [17] device topology is another candidate considered for high temperature electronics [10]. BJT does not require high quality thermal oxide or buried metal features, but utilises p-n junction for operation. However, SiC BJTs face difficulties in producing repeatable characteristics and undergo stability issues (due to the need of high quality metal contacts for both n- and p-type SiC) at temperatures above 300 °C [13].

Hence, MOSFET, MESFETs and BJT device topologies require further development, in terms of reliability and stability of various interfaces with SiC crystal, if they are to be used for high temperature sensor interface electronics.

JFET

JFETs [17] are controlled by p-n junction and do not require high quality thermal oxide or buried metal features, as by MOSFETs and MESFETs, respectively. Furthermore, unlike BJTs, SiC JFETs are tolerant to non-ideal (semi rectifying) contacts [13]. Hence, SiC JFETs have been accepted as the most promising candidate for long term reliable operation of SiC electronics at high temperatures [10, 13, 22, 23].

SiC JFETs can be fabricated in planar and non-planar configurations. The planar configuration utilises only ion implantation for selective doping of gate implant and source/drain regions. This is because the diffusion coefficient of impurities in SiC is negligible below 1800 °C; thereby making the conventional diffusion technique impractical [10]. In comparison to Si, ion implantation in SiC requires higher ion energy, thicker masking material and larger implantation dose, resulting in increased lattice damage. A post implantation annealing is therefore required to repair this ion-induced lattice damage and to electrically activate the dopants. The annealing temperature typically ranges from 1200–1800 °C, higher than that needed by Si. Consequently, such high temperatures cause surface roughness which can adversely affect the electrical characteristics of the doped regions, making them unsuitable for device fabrication [10]. To overcome this problem, ion implantation in SiC is generally carried out at elevated

temperatures (500–1000 °C) which assists in crystal restructuring during the implantation process and reduces lattice damage [24]. Conversely, in a non-planar configuration, SiC JFETs can be fabricated primarily from epitaxially grown layers with the exception of source/drain regions, eliminating the need for very high temperature annealing [24].

Another distinct feature in SiC JFETs is that they can be fabricated in vertical (VJFET) [25] or lateral (LJFET) [22] structures. VJFET structures are generally used for power devices. Recent developments have shown improvements in both normally-on [26] and normally-off [27] high power JFETs. Depending on the thickness of the n⁻ drift layer, such devices are capable of blocking voltages up to 14 kV [28].

LJFET structures, on the other hand, are generally used for low power operations. The lateral structure provides a flexibility of fabricating many devices on the same die, making SiC integrated circuits possible to achieve [29]. The research groups at NASA [30] and Case Western Reserve University (CWRU) [31] are the leading contributors for high temperature sensor interface electronics in SiC. They have demonstrated high temperature logic and amplification circuitry, based on depletion (normally-on) mode 6H-SiC JFETs [13, 22, 29]. These JFETs have a gate length of 10 μm and are fabricated in a non-planar configuration using 6H-SiC epitaxy. The schematic of a JFET by CWRU is shown in Figure 2.2.

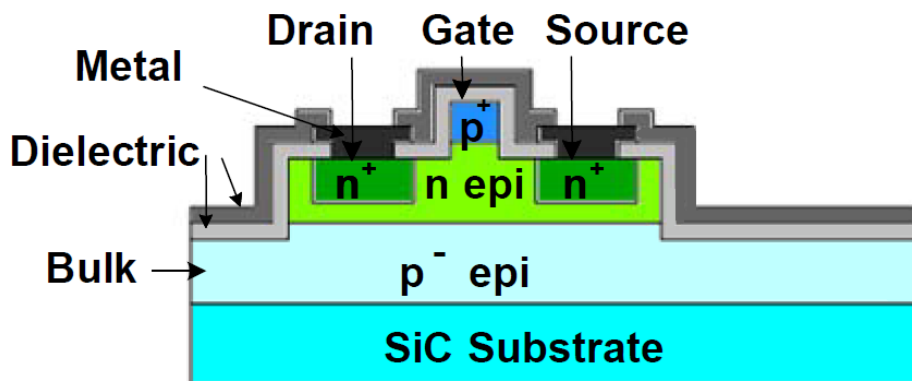


Figure 2.2. Schematic cross-section of n-channel SiC JFET (figure modified from [22]).

The high temperature SiC JFETs designed and characterised by CWRU [22] have a mean threshold voltage (V_t) value of around -8 V, with ~ 1 V standard deviation. Furthermore, the dependence of V_t on temperature is around -1.9 mV/ $^{\circ}$ C for temperatures up to 450 $^{\circ}$ C which is reasonable in comparison to -14 mV/ $^{\circ}$ C above 200 $^{\circ}$ C for the MOSFET structure reported in [20]. The exposure to high radiation is reported in [32] where the JFETs were tested to a radiation dose of 1 Mrad(Si) without significant degradation in device characteristics.

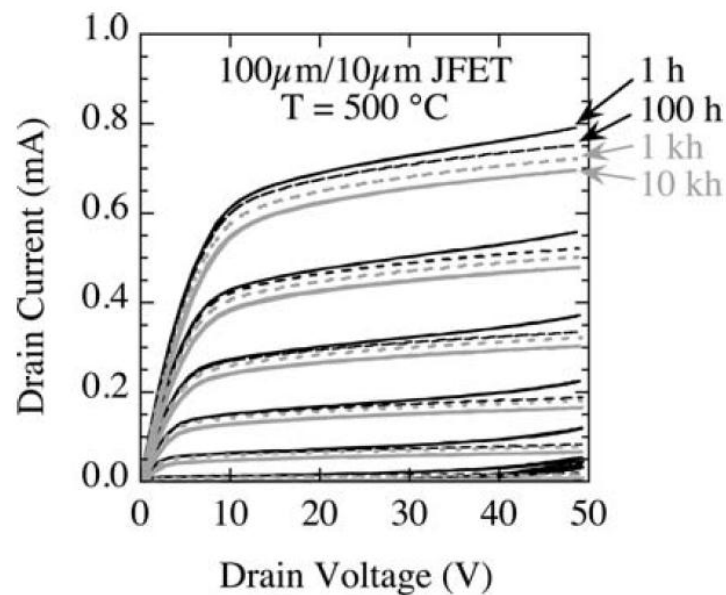


Figure 2.3. Drain I-V characteristics of packaged $100 \mu\text{m}/10 \mu\text{m}$ NASA 6H-SiC JFET measured during the 1st, 100th, 1,000th, and 10,000th hour of electrical operation at 500 $^{\circ}$ C. Gate voltage steps are -2 V starting from $V_g = 0$ V as the topmost sweep of each curve [13].

Recently NASA has demonstrated prolonged 500 $^{\circ}$ C operation of their (normally on) 6H-SiC n-JFETs for up to $10,000$ hours [13], as shown in Figure 2.3. These devices show a high degree of stability with less than 10% variation in transconductance (g_m) values and only 1% variation in device threshold voltage (V_t). NASA has also tested the stability of their packaged JFETs by sending them to the International Space Station (ISS) in November 2010. The successful operation of these JFETs and packaging for thousands of hours, without significant degradation, indicates robustness against high gravitational forces experienced during launch [33]. NASA has used a Ti/TiN/Pt contact structure

for both p- and n-type contacts with specific resistance of $1.5 \times 10^{-5} \Omega\text{cm}^2$ to $3.42 \times 10^{-4} \Omega\text{cm}^2$. These contacts have shown excellent resilience to high temperature degradation [34]. In other structures, the same group have used Ti/TiSi₂/Pt ohmic contacts which are semi-rectifying [35].

To conclude, MOSFET, MESFET and BJT device topologies have issues connected to reliability and stability of high quality interfaces (thermal oxide, buried metal or ohmic contacts) with SiC crystal at temperatures above 400 °C. JFETs, on the other hand, can operate acceptably with quite non-ideal (even semi-rectifying) contacts and, hence, promise to be the most feasible solution for high temperature sensor interface electronics in the nearer term. The stable device characteristics for thousands of hours at high temperatures, including robustness of wire bonding/packaging against high gravitational forces during launch to the ISS, have demonstrated stability of contacts in JFETs. However, these prototype JFET structures have a gate length of 10 µm and operate at high biasing voltages (> 20 V). Hence, miniaturisation of device dimensions and operating biases are the key for commercialisation of low power SiC electronics to monitor hostile environments. Furthermore, the normally on nature of these JFETs imposes extra complexity, with increased power losses, in the design of logic devices.

2.3 SiC Logic

This section presents a review on the current state of SiC logic gates. The main focus is on the high power losses in these designs, mainly due to lack of CMOS technology at high temperatures. Consequently, CJFET logic is introduced, as an alternate to CMOS, with low power losses and close to rail output swing at high temperature.

2.3.1 Current Advances

A summary of some of the major high temperature SiC logic gates in the

literature is presented in Table 2.2. These are discussed in the following sub-sections.

Device Type	Max. Temp. (°C)	Performance Summary	Ref.
6H-SiC, depletion mode n-JFET Logic	500	Operation of NOT, NOR, NAND gates for thousands of hours at 500 °C: $V_t = -7$ to -14 V, $V_{DD}/V_{SS} = 18$ to 30 V, $P_{stat} \sim$ mW, Propagation delay ~ 6 μ s, $f_{max} \sim$ kHz	[13, 36]
Monolithic NMOS Logic	300	Various logical functions (NOT, NOR, to RS flip-flops and half adders). At 300 °C: $V_t \sim 1$ V, $V_{DD} = 5$ V, $V_{GG} = 7$ V, NOT gate: $NM_L \sim 0.1$ V and $NM_H \sim 3.3$ V	[19]
6H-SiC CMOS Logic	300	Various logical functions (NOT, NOR, to flip-flops and half adders). At 300 °C: $V_t = 1.2$ V for n-MOS and -3.2 V for p-MOS, $V_{DD} = 5$ V, 11-stage ring oscillator: $f = 24.8$ kHz	[37]
n-MESFET	400	Simulation of NOT, NOR, NAND, XOR and T-Flip-Flops. High static power losses; requires level shifter circuitry.	[38]
4H-SiC, BJT Emitter Coupled Logic (ECL)	300	Two input OR-NOR gate: $V_{DD} = -15$ V, Noise margins ~ 1 V, $P_{stat} = 0.82$ W, Propagation delay ~ 280 – 320 ns. Three-stage ring oscillator: $f \sim 2$ MHz	[39]

Table 2.2. Summary of published logic gates in SiC.

JFET Logic

The SiC research group at NASA [30] is the leading contributor in the development of logic elements for high temperature operations. Using 6H-SiC depletion mode n-JFETs, NASA has successfully tested a variety of logic gates (NOT, NOR, NAND) for thousands of hours at 500 °C [13, 36]. These n-JFETs have a negative threshold voltage, ranging from -14 V to -7 V across the wafer. Hence, this prototype logic family operates at negative logic voltage levels and two power supplies, $+V_{DD}$ and V_{SS} , in the range of 18 to 30 V. This means that extra circuitry is required to produce correct logic levels for the input of

succeeding gates, imposing extra complexity upon logic design, with increased power dissipation. The schematics of a NOT gate is illustrated in Figure 2.4 (a), where it can be seen that the circuit is divided into two stages: a logic inverting amplifier stage (to perform the logic NOT operation to the input signal, V_{INA}) and a level shifter stage (to translate the output of inverting amplifier stage back to desired negative logic gate output voltages (V_{OH} or V_{OL}) that would successfully drive the input of a subsequent gate of this logic family). A more detailed explanation on operation of this logic family is given in [13, 36].

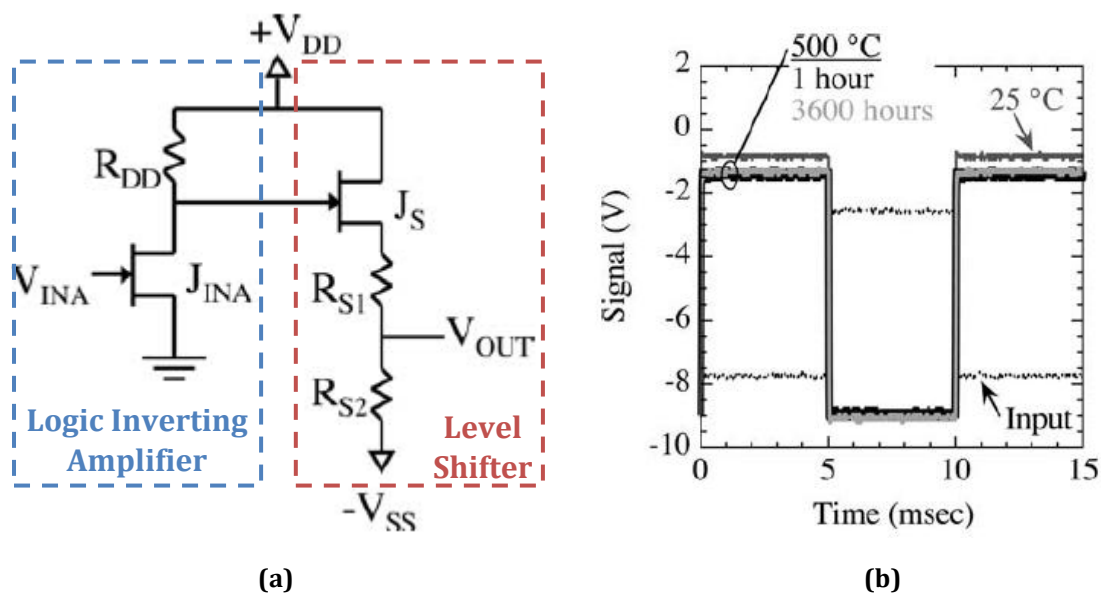


Figure 2.4. (a) Schematic diagram of prototype NOT logic gate integrated circuit test chip implemented at NASA using n-channel depletion-mode 6H-SiC JFETs and resistors. The circuit operates with two power supplies ($+V_{DD} = 24$ V and $-V_{SS} = V_{sub} = -20$ V) and negative logic signal voltages. (b) Experimentally measured NOT gate IC test waveforms showing that similar output is obtained at 25 °C and at the start (1 hour) and end (3600 hours) of prolonged 500 °C operational testing [13, 36].

The NOT gate IC was tested for thousands of hours at 500 °C ($f = 100$ Hz, $+V_{DD} = 24$ V and $-V_{SS} = V_{sub} = -20$ V) with slight degradation in output signal from the RT measurements, as shown in Figure 2.4 (b). The operating speed of this logic family decreases with temperature due to degradation in channel drift current at high temperatures. As a result, while driving the oscilloscope probe, the propagation time of the NOT gate increases from 1.7 μ s at 25 °C to about 6 μ s at 500 °C. Similar tests for NOR and NAND ICs for thousands of hours at 500 °C

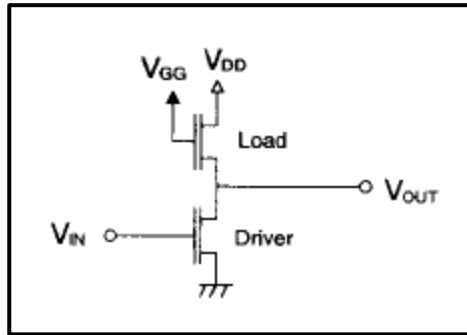
demonstrated stable output characteristics, i.e. without significant variation in output voltages (V_{OH} or V_{OL}).

For many applications, complex logic circuitries, far greater than a few-transistor ICs, are required. The major problem with this logic family to achieve such high circuit complexities is high static power dissipation ($P_{stat} \sim \text{mW}$ per gate) which is many orders of magnitude larger than that by logic gates implemented in Si CMOS technology. This is mainly because, unlike CMOS logic [40], there is always significant current flowing through one of the circuit branches. Hence, 6H-SiC depletion mode n-JFET logic family is not suitable for achieving complex logic functions.

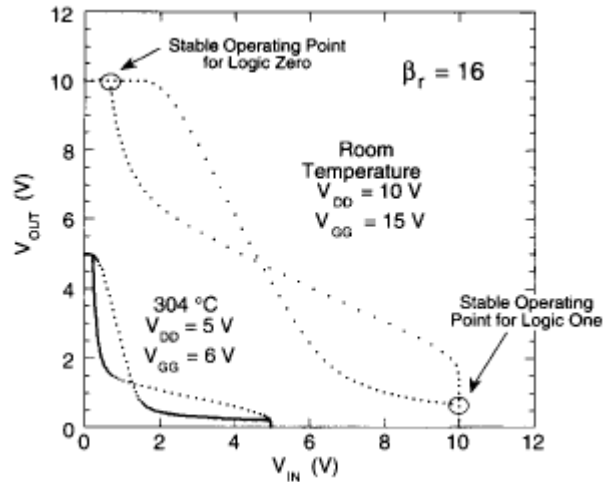
MOSFET Logic

The first monolithic NMOS digital IC in 6H-SiC to operate between RT and 300 °C was reported by [19]. Using enhancement mode NMOS ($V_t = 3 \text{ V}$ at RT and $V_t \sim 1 \text{ V}$ at 300 °C), various logic functions (such as NOT, NOR, NAND, XNOR, D-latches, RS flip-flops, binary counters and half adders) have been fabricated and characterised. Instead of a load resistor, the pull-up network in each gate is an n-channel enhancement mode MOSFET with separate gate (V_{GG}) and drain (V_{DD}), operated in the non-saturation mode. This is shown in the circuit diagram for NOT gate in Figure 2.5 (a). The inverter has noise margins of 1.4 V at RT (or $\sim 0.1 \text{ V}$ at 300 °C) for logic low and 3.7 V at RT (or $\sim 3.3 \text{ V}$ at 300 °C) for logic high, as shown in Figure 2.5 (b).

All circuits in this logic family are operated with $V_{DD} = 10 \text{ V}$ at RT (or 5 V at 300 °C) and $V_{GG} = 14 \text{ V}$ at RT (or 7 V at 300 °C). The devices continue to work successfully after a few hours operation at 300 °C. However, oxide degradation in enhancement mode NMOS is reported at higher temperatures. Hence, improvements in stability of high quality oxides are required before this logic family can be utilised in applications above 400 °C.



(a)



(b)

Figure 2.5. (a) Schematic diagram of SiC NMOS logic inverter. (b) Input-output characteristics at RT and at 304 °C. Stable operating points at each temperature are determined by the intersections of the normal and reversed transfer curves [19].

CMOS Logic

CMOS technology is ideal for digital logic because it offers full rail-to-rail output swing, enhanced noise margin and, most importantly, lower power consumption than any other logic family. The first CMOS digital IC in 6H-SiC to operate with a 5 V power supply between RT and 300 °C was reported in [37]. The enhancement mode n- and p-MOSFETs have threshold voltages of 3.3 V at RT (or 1.2 V at 300 °C) and -4.2 V at RT (or -3.2 V at 300 °C), respectively. The threshold voltage at 300 °C for both devices can be seen from the I-V characteristics shown in Figure 2.6.

Several digital circuits, such as NOT, NOR, NAND and 11-stage ring oscillator, were fabricated using these devices which exhibited stable operation up to 300 °C. Ring oscillator frequency of operation is 1.13 kHz at RT and 24.8 kHz at 300 °C, indicating that these circuits are suitable for low frequency applications and limited to 300 °C operation due to oxide degradation at higher temperatures.

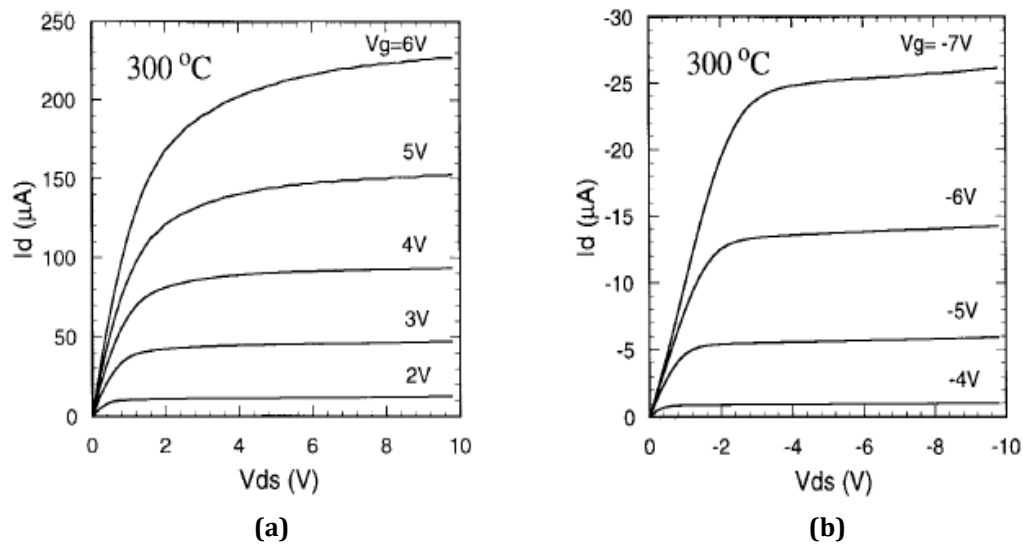


Figure 2.6. I-V characteristics of 40 $\mu\text{m}/5\mu\text{m}$ (a) n-MOSFET (b) p-MOSFET at 300 °C [37].

MESFET Logic

A demonstration of logic gates design with normally-on 4H-SiC n-MESFETs using calibrated high temperature Spice models is presented in [38]. Logic functions, such as NOT, NOR, NAND, XOR and T-Flip-Flops, are designed and simulated at 0, 200 and 400 °C. Similar to n-JFET logic demonstrated by NASA [13, 36], this logic family also works on negative logic voltage levels and, hence, requires a load resistor and an additional level shifter circuitry to produce correct input voltage levels for succeeding gates. This results in additional power consumption, making this logic family unsuitable for achieving complex logical operations.

BJT Logic

Recently, low voltage 4H-SiC n-p-n BJTs (capable of operating up to 300 °C) were used to demonstrate digital ICs (OR-NOR gate and three-stage Ring Oscillator) based on emitter-coupled logic (ECL) in [39]. The fabricated OR-NOR gate, schematics shown in Figure 2.7, consists of 10 n-p-n transistors (two of them are connected as diodes) and 11 integrated resistors, with a total area of 1.117 mm² (1000 $\mu\text{m} \times 1117 \mu\text{m}$). This shows the complexity of ECL design in comparison to complementary logic design, which would otherwise require only 4 transistors for a NOR gate.

Stable noise margins of about 1 V, with static power dissipation of 0.82 W/gate and propagation delay of 280–320 ns, are reported for a two-input OR-NOR gate, operated on $V_{DD} = -15$ V at 300 °C. Furthermore, the three-stage ring-oscillator is observed to have an oscillation frequency of ~ 2 MHz between RT and 300 °C. With such high power losses and complex design, this logic family is limited to achieving only rudimentary functions.

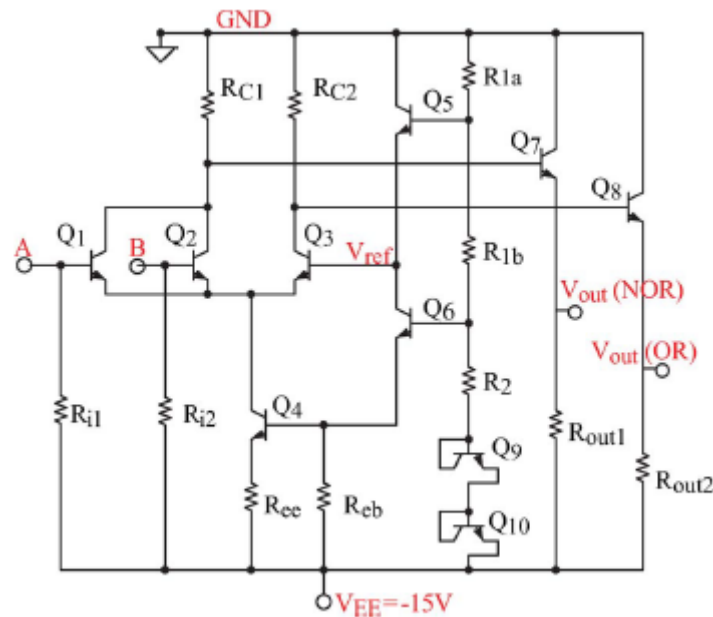


Figure 2.7. Schematic diagram of SiC ECL OR-NOR gate, featuring 10 n-p-n transistors (two of them are connected as diodes) and 11 integrated resistors [39].

To conclude, CMOS technology is ideal for digital logic, both in terms of design simplicity and power dissipation. However, oxide degradation at high temperatures has limited SiC CMOS operation to 300 °C; which seems to be a daunting challenge to achieve in the near future. In general, all SiC logic families published so far are based on the concept of RTL, which means there is always a non-negligible power loss in the load resistor. Furthermore, the use of depletion (normally-on) mode transistors in logic design means that the gate works on negative logic voltage levels. Hence, additional level shifter circuitry is needed to produce the correct input voltage levels for succeeding gates. This adds complexity to logic design and results in extra power dissipation in the level shifter circuitry.

In order to achieve complex logic functions in SiC at high temperatures, there is a need for an alternative technology to CMOS. The design and operation of CJFET logic, with low power losses and close to rail output swing, are discussed next.

2.3.2 Complementary JFET Logic

The wide bandgap of SiC (3.26 eV for 4H-SiC at RT) allows the fabrication of enhancement mode (normally-off) n- and p-JFET structures, requiring forward gate bias to switch the device on. Hence, by connecting the gate terminals of identical normally-off n- and p-JFETs, a complementary pair (CJFET) is formed. This simple inverter structure is identical to CMOS both in design and functionality, except that the n- and p-MOSFETs in a CMOS inverter (with oxide degradation issues above 300 °C) are replaced by much more stable high temperature n- and p-JFETs. The schematics of CJFET and CMOS logic inverters are shown in Figure 2.8.

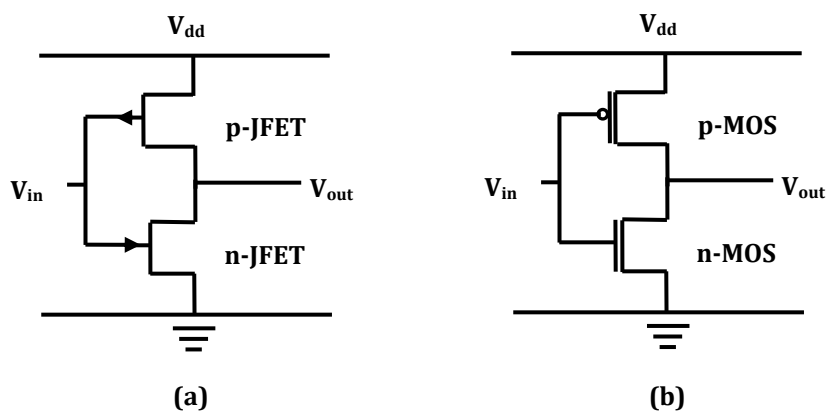


Figure 2.8. Comparison of (a) CJFET structure, formed by cascading normally-off n- and p-channel SiC JFETs, with (b) CMOS structure, formed by cascading normally-off n- and p-channel MOSFETs.

The CJFET logic family has the same basic operation as CMOS logic [40]. This is evident from the truth table for CJFET logic inverter, given in Table 2.3. For low input voltage (i.e. $V_{in} < V_t$ of n-JFET), the n-JFET is switched off, whereas the p-JFET (with $V_{dd} - V_{in} > V_t$ of p-JFET) is switched on. The circuit functions as a potential divider with the p-JFET operating as a small resistor and the n-JFET as

an open circuit. Thus, almost all of V_{dd} is dropped across n-JFET, giving a high logic voltage at the output. Similarly, for high input voltage, p-JFET is off and n-JFET is on, giving a low logic voltage at the output.

V_{in}	V_{out}
Low	High
High	Low

Table 2.3. Truth table of CJFET logic inverter.

One of the main advantages of CJFET logic is that it gives a full-rail output voltage swing which provides well-defined logic 0 and logic 1 voltages, and, hence, greater noise margin compared to TTL and other known logic types. This allows CJFET logic to operate at low supply voltages, with reduced gate drive complexity¹ and power dissipation, making it an ideal candidate for logic in extreme environments.

2.4 SiC Material – Defects and Variability

This section outlines the advancement in SiC wafer quality and discusses the main types of process variations affecting device structure and, hence, influencing device and circuit performance. The role of TCAD for tackling process variability and device optimisation also forms part of this section.

2.4.1 Current Advances in Wafer Quality

The quality of SiC commercial wafers has been improving since the first wafers were released for 6H-SiC in 1991 and 4H-SiC in 1994 [11]. However, the last decade has shown some exceptional improvements in SiC wafer quality. Currently, 4H-SiC substrates (n-type, p-type and semi-insulating) and SiC epitaxial wafers (n-type and p-type) are commercially available in 76.2 mm and

¹ The enhancement mode n- and p-JFETs ensures positive logic voltage levels and, hence, eliminates the need for extra level shifter circuitry common in most depletion mode logic designs discussed previously in Section 2.3.1.

100 mm sizes, with less than $\pm 10\%$ tolerance in epitaxial thickness and doping concentration [41] and micropipe density (MPD) $< 0.1 \text{ cm}^{-2}$ [9].



Figure 2.9. Micropipe reduction of 4H-SiC substrates by Cree [42].

Figure 2.9 shows the improvement in micropipe density of commercial SiC wafers by Cree Inc. [42] over the last decade. These micropipe defects [43] originate in the SiC substrate and appear in the device structure during epitaxial growth. The disadvantage of having a high defect density in the SiC wafer is smaller usable device area which results in low current and switching capabilities of these devices. The reduction in micropipe density along with increase in size of SiC wafers has supported the aggressive growth of SiC devices commercially.

For continual growth of SiC market, however, it is essential to continue reducing the overall unit area cost of SiC substrates and epitaxial wafers. This can be achieved by progressively increasing the diameter (size) of SiC wafers. In August 2010, Cree reported the first 150 mm SiC wafer prototype with an R&D best MPD of 8.8 cm^{-2} [42]. Furthermore, the 150 mm SiC epitaxy demonstrated excellent epitaxial layer uniformity: 2.1% standard deviation (σ)/mean doping uniformity (4mm edge exclusion) and 0.95% σ /mean thickness uniformity (5mm edge exclusion). With continued improvements in material and epitaxy capabilities,

Cree announced the 150 mm SiC n-type and epitaxial wafers to be commercially available by the second half of 2012.

To conclude, the increased popularity of SiC devices along with improvements in wafer quality and size have resulted in a significant downward price trend on a unit area basis. Today, Schottky-like 100 mm epitaxial wafers cost $\sim \$15/\text{cm}^{-2}$ in production volumes, as compared to $\sim \$25/\text{cm}^{-2}$ 3 years ago and $\sim \$40/\text{cm}^{-2}$ 8 years ago. This trend is expected to continue with 150 mm epitaxial wafers, forecasted at $< \$5/\text{cm}^{-2}$ in production volumes [42]. Hence, with the continued growth in wafer size and improvements in epitaxial layer uniformity, SiC based devices and circuits may soon be found beneficial in applications both within and beyond the reach of Si.

The next section looks in to the issue of process variability, effecting device structure and, hence, influencing device and circuit performance.

2.4.2 Process Variation

The term “variation” is defined as the deviation from intended or designed values for a structure or circuit parameter of concern [44]. Digital circuits are designed such that the fabricated circuits should meet the performance specifications, such as noise margin, speed and power dissipation, under all operating conditions. However, random fluctuations in the semiconductor fabrication processes, which are essentially permanent, cause an undesirable spread in the circuit performance. Furthermore, random variations in the environmental factors, such as temperature, power supply, and switching activity, during the operation of the circuit result in temporary variations in the circuit performance. The excessive spread of circuit performance can lead to a significant yield loss and hence can increase the unit cost of the product. The term yield used here refers to functional yield, the fraction of the total number of manufactured circuits which are free from logical faults, and parametric yield,

the fraction of the total number of manufactured circuits which pass the acceptability criteria² [45].

With the shrinkage of device dimensions to improve performance, variability of process parameters is becoming a serious concern. This is because as device dimensions become smaller, the number of atoms in the semiconductor material that produce many of the transistor properties become fewer, thereby amplifying the dependence of device characteristics with process parameters. Hence, it is important to consider the impact of these statistical variations, arising due to process and environmental factors, early on during the design of the circuit. It is always a goal to make the circuit performance less sensitive to these variations and should have enough margins such that a large fraction of the manufactured circuits pass the acceptability criteria [45-47].

The impact of process and environmental factors on device, circuit and system performance is shown in Figure 2.10 [45]. The figure illustrates the underlying relationship of device and circuit parameters to process variations. The fluctuations in manufacturing process parameters, such as variations in epitaxial layer (thickness and doping concentration) and implantation (dose and energy), result in the variation in device profile and its structural parameters. These variations, in addition to the variations in environmental factors, cause deviations in the device characteristics, resulting in circuit parameter variation. The variation in various transistors, circuits and components of the system on chip (SoC) has a negative impact on its overall performance.

For the purpose of circuit design, the variability in process parameters can be divided into two main categories [44, 47, 48]: inter-die variations and intra-die variations. These are briefly discussed next.

² The acceptability criteria require a circuit to satisfy each of its performances by the specified specifications. A circuit with parametric faults may be logically functional but may fail to meet some performance specifications.

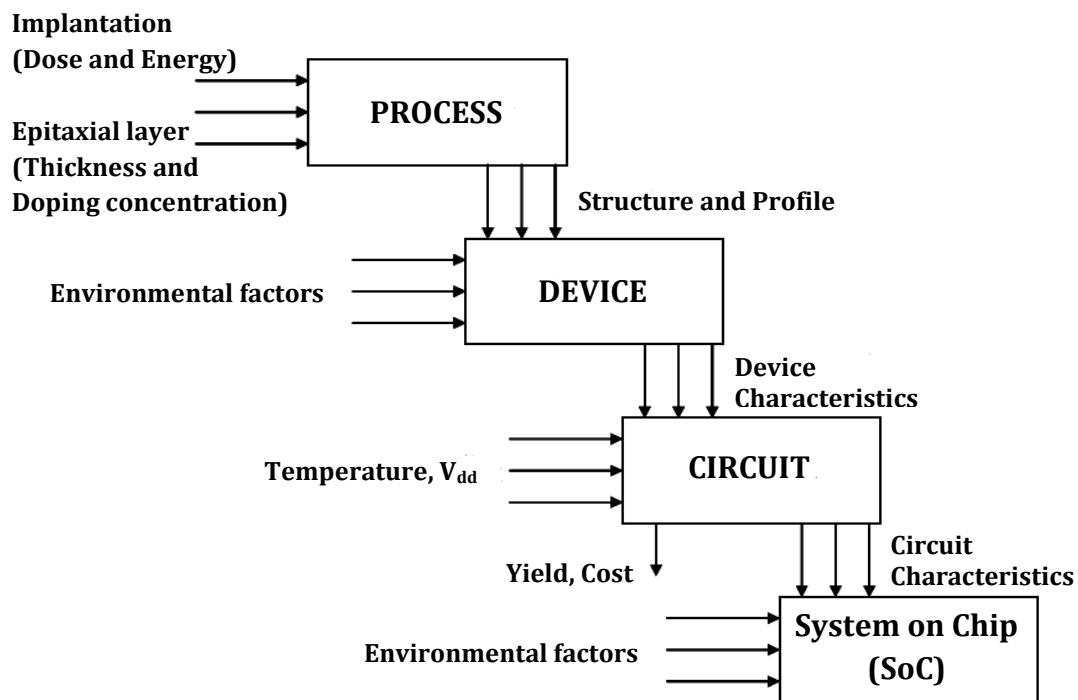


Figure 2.10. Effect of variations in process parameters and environmental factors on device, circuit and system on chip (SoC) performance (figure modified from [45]).

Inter-die variations

Inter-die (or die-to-die) variations are fluctuations in the process parameters of nominally identical dies, fabricated on the same wafer, on different wafers, or in different lots, as shown in Figure 2.11 [47]. In a given die, inter-die variations affect all structures or devices equally. For the purpose of circuit design, it is usually assumed that each component or contribution in inter-die variation is due to different physical and independent sources [44, 47]. Hence, the variation component can be represented by a uniform shift in the parameter mean across all devices in the circuit. For example, inter-die variation in a parameter, such as threshold voltage (V_t), would change its value in the same direction (increase or decrease) for all transistors in a die, causing variation in circuit noise margin, delay and power dissipation. This inter-die variation, however, does not cause a mismatch between different transistors in a die.

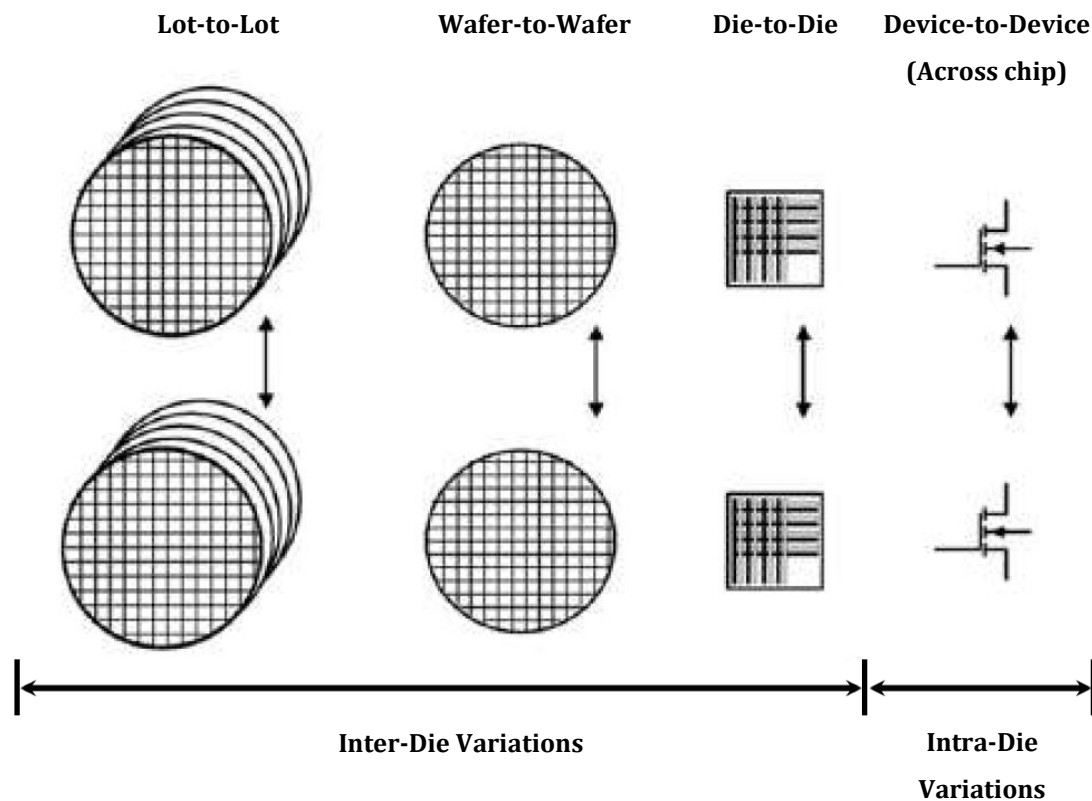


Figure 2.11. Process variability at different levels of manufacturing (figure modified from [47]).

Intra-die variations

Intra-die (or within-die) variations are fluctuations in the process parameters occurring spatially within a die, as shown in Figure 2.11 [47]. These variations may have a variety of sources depending on the physics of the manufacturing steps [44, 49, 50]. Unlike inter-die variations (affecting all structures on any single die equally), intra-die variations contributes to the loss of matched behaviour between structures on the same die. For example, intra-die variation in the threshold voltage (V_t) would change its value in different directions for transistors in a die (i.e. for some transistors V_t will increase, while for others V_t will decrease) [51]. This mismatch in V_t between transistors could seriously affect noise margin, speed and static power losses in digital circuits, such as logic elements. The effect of intra-die variations gets even worse when high temperature operations are involved, so much so that the output from one stage

may not be sufficient to drive the next stage in the logic array, impairing basic circuit functionality [52].

To conclude, inter-die and the intra-die variations in manufacturing process parameters result in variations in device structural parameters, causing variations in device and circuit performance parameters and, hence, affect the overall functional/parametric yield, as shown in Figure 2.10. The only concern with inter-die variations is how the unidirectional (increase or decrease) variation across a chip may impact performance or parametric yield. Whereas, intra-die variations concern circuit designers with an entire set of elements (such elements may be individual transistors, signal lines or segments of signal lines, or any other geometric or electrical parameter of the circuit) and how such elements vary differently from the designed or nominal values, or how such elements differ from each other [44].

Next, the process variations typically of concern in evaluating device structure, device characteristics and circuit performance are briefly discussed in Sections 2.4.3 to 2.4.5.

2.4.3 The Effect of Process Variation on Device Structure

The set of process variations directly affecting the structural or geometric characteristics of the JFET device are discussed below.

Variations in gate profile

The gate in a JFET, which control the flow of current through the channel, can be of two different types: implanted gate (planar structure) or epitaxial gate (non-planar structure), as discussed previously in Section 2.2. In the case of implanted gate (where the gate is implanted in the channel layer), the variations in implant dose, energy, and angle may affect the gate doping profile and gate implant depth (t_g). These variations in-turn affect the depletion width of the gate-channel junction and the channel thickness and, hence, affect the electrical parameters of the device.

In the case of epitaxial gated JFETs, the gate is formed from the epitaxial layer on top of the channel epitaxy; thus there is no major issues of gate implant depth variations. However, the fluctuations in the doping profile due to inter-die and intra-die variations affect the gate doping profile and, hence, influence the depletion width of the gate-channel junction. Furthermore, the fluctuations in photolithographic and etching processes may result in effective gate length variations, affecting the electrical parameters of the device.

Variations in channel profile

The channel carrier concentration is responsible for most of the electrical characteristics in JFETs. The variations in channel thickness and channel doping concentration (due to inter-die and intra-die variations) affect the flow of current through the channel by affecting (increasing/decreasing) the channel opening and the number of free carriers in the channel, thereby influencing performance at both device and circuit level.

The variations in device doping profile and geometric parameters (such as channel thickness/gate implant depth and channel doping) significantly affect the electrical characteristics of JFETs, especially enhancement mode JFETs and when high temperature operations are involved [13, 52].

2.4.4 The Effect of Process Variation on Device Characteristics

Variability of process parameters causes fluctuations in structural or geometrical parameters, resulting in variations in device characteristics such as threshold voltage (V_t), drain saturation current (I_{dss}), and leakage or off-state current (I_{off}).

Threshold voltage (V_t) variation

The threshold voltage is the key parameter for high temperature JFETs. This is because, like CMOS [40], CJFET based logic gates require enhancement-mode (normally off) n- and p-JFETs for operation. The threshold voltage of SiC JFETs is found to be most sensitive to the channel doping fluctuations and variations in channel thickness [52, 53]. The variations in these parameters cause V_t to

deviate from the nominal value, thereby degrading circuit performance. Furthermore, under extreme conditions, variations in these process parameters can shift the switching voltage of these JFETs, turning them into depletion-mode (or normally-on) devices, hence, impairing the basic functionality of the logic element.

Drain saturation current (I_{dss}) variation

Variations in device geometry/profile can significantly affect the drain saturation current in JFETs. The fluctuations in channel thickness and channel doping concentration (due to inter-die and intra-die variations) directly influence the flow of current through the channel. Subsequently, these variations in I_{dss} have a direct impact on the speed of CJFET digital circuits.

Leakage current (I_{off}) variation

The I_{off} variations, resulting mainly from channel and gate doping fluctuations and variations in channel thickness, can be a significant concern for circuit designers. I_{off} is directly connected to the static power losses in CJFET logic devices. At high temperatures, process variations can have adverse effect on I_{off} , which may lead to high static power losses, overheating the IC.

2.4.5 The Effect of Process Variation on Circuit Performance

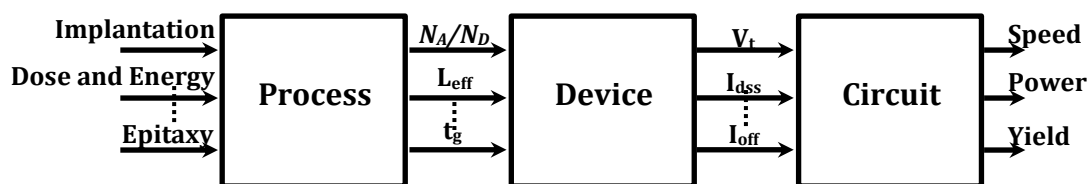


Figure 2.12. Impact of process variation on device and circuit performance.

Process variation has a direct influence on circuit performance. Figure 2.12 shows the impact of manufacturing process variations at both device and circuit level. As illustrated in this figure, variations in process parameters alters device geometrical parameters (such as gate implant depth (t_g) or channel thickness,

gate (N_A) and channel (N_D) doping concentrations and effective gate length (L_{eff}), leading to variations in device electrical parameters (V_t , I_{dss} , I_{off} , etc.). These fluctuations in device electrical parameter eventually affect circuit performance metrics, such as speed, power and, most importantly, integrity of proper logical operation in logic gates which affects chip functional and parametric yield.

To conclude, the inter-die and the intra-die variations in manufacturing process parameters, such as channel length, channel thickness, threshold voltage, gate and channel doping concentrations, result in significant variations in the delay, noise margin and leakage power consumption of digital circuits [52, 54-57]. Furthermore, the impact of random intra-die variations on the yield of digital circuits, such as memory cells and logic devices, is a serious issue in scaled CMOS technologies [46]. Similarly, the scaling of SiC devices, to improve performance, and with an addition of high temperature operations have both lead process variations to become a more dominant concern for circuit designers. However, with the continued advancement in SiC wafer quality (particularly, with improvements in uniformity of epitaxial layer thickness and doping concentration across a die), the effect of such variations on high temperature SiC CJFET circuits may be significantly reduced.

2.4.6 The Role of TCAD

TCAD computer simulations are being widely used by leading IC manufacturing industries to develop and optimise semiconductor processing technologies and devices [58, 59]. TCAD tools are based on the underlying physical principles of the semiconductor material under consideration. The structural properties and electrical behaviour of semiconductor devices are modelled by solving fundamental, physical partial differential equations, such as diffusion and transport equations. This deep physical approach gives TCAD simulations predictive accuracy for a broad range of technologies [58]. Hence, all leading semiconductor companies use TCAD tools as a mean to reduce costly and time-consuming test wafer runs when developing, optimising and characterising new semiconductor devices or technologies [59].

The demand for high performance and energy efficient miniaturised devices in silicon carbide [60, 61] has made TCAD tools a vital part of the development cycle. Using calibrated model parameters (based on the physical and material properties of SiC), TCAD simulations allow circuit designers to understand device operation and to accurately predict electrical characteristics of complex structures at high temperatures. Furthermore, TCAD tools and statistical techniques, such as DoE and RSM³, allow circuit designers to efficiently optimise high temperature SiC devices. This is achieved by determining the optimised device geometry and doping profiles before the fabrication stage, resulting in substantial reduction in cost and time. TCAD tools and statistical techniques also aid in studying the impact of process variability on device and circuit performance which ultimately affects the manufacturability and yield (functional and parametric) of the circuit.

2.5 Statistical Techniques for Modelling Process Variations and Device Optimisation

This section presents a detailed review on DoE and RSM methodology for modelling process variations and device optimisation.

2.5.1 Design of Experiments

DoE is an established branch of statistics which has been successfully used since the 1920s in multidisciplinary fields to model variability and optimise manufacturing processes [45, 62-68]. Statistical DoE is also widely used in manufacturing industry for improving product quality and productivity. Design of experiments involves the investigation of the effect of inputs (*factors*) on some measured output (*response*). Purposeful changes are made to the inputs of a process in a series of tests and changes in the *response* are observed and analysed. In other words, DoE refers to the methodology of planning an experiment so that the effect on the process *response*, as a result of variations in the process inputs, can be observed and analysed using statistical methods. The

³ Design of Experiment (DoE) and Response Surface Modelling (RSM) are discussed in detail in Section 2.5.

statistical DoE precisely relates the *factors-response* variation relationship by building a model, in the form of an equation, which may then be used to predict new observations. The advantage of DoE over other techniques, such as Monte Carlo (MC) [69], is that DoE is much more efficient to run, easier to integrate and generate a model which can be a surrogate to simulations or experiments for predicting variability [62]. A detailed comparison between DoE and MC is given in [70]. Two of the main DoE categories, namely full factorial (FF) and response surface (RS) designs [67, 68], are discussed in the following sub-sections.

Full Factorial Design

Full Factorial design (also known as factorial design) is the most basic experimental design category [71]. Factorial experiments are performed by selecting a fixed number of *levels* (N) for each of the inputs/*factors* (k) and then running experiments at all possible combinations (N^k) of the *levels*. The *response* for each of these experimental runs is then collected to determine the effect of any single *factor* on the *response* (called the *main effect*) and the effect of two or more *factors* on the *response* (called the *interaction effect*). In statistical terms, the *main effect* is defined as the change in *response* produced by the change in *level* of a particular *factor*. On the other hand, when the *effect* of one *factor* on the *response* differs according to the *level* of another *factor*, an interaction between the *factors* exists and is termed as *interaction effect*. Two of the most important considerations in factorial design is the choice of *factors* to be varied in an experiment and the ranges over which each *factor* will be varied. The ranges of the process variables (*factors*) can be categorised into minimum (-1), maximum ($+1$) and centre (0) *levels*. The choice of the number of *factors* (k), along with the number of *levels* (N) for *factors*, directly affects the number of experimental runs and, hence, the cost of performing the experiment.

Two-level factorial designs are by far the most commonly used designs for modelling the *main* and *interaction effects*, as they require fewer samples or simulations. In two-level designs, each *factor* has two levels, minimum (-1) and maximum ($+1$). The two-level factorial design incorporates all the possible combinations of (-1) and ($+1$) *levels*. Hence, for k *factors*, a total of 2^k number of

experiments or simulations will be required. A geometrical representation of three factor ($k = 3$) two-level factorial design is shown in Figure 2.13. In this case 2^3 or 8 experimental or simulation runs are required. Here x, y and z are the *main effects*, xy, yz and xz are the two-factor *interactions* and xyz is the three-factor *interaction*. Table 2.4 shows the design matrix for the 2^3 factorial design.

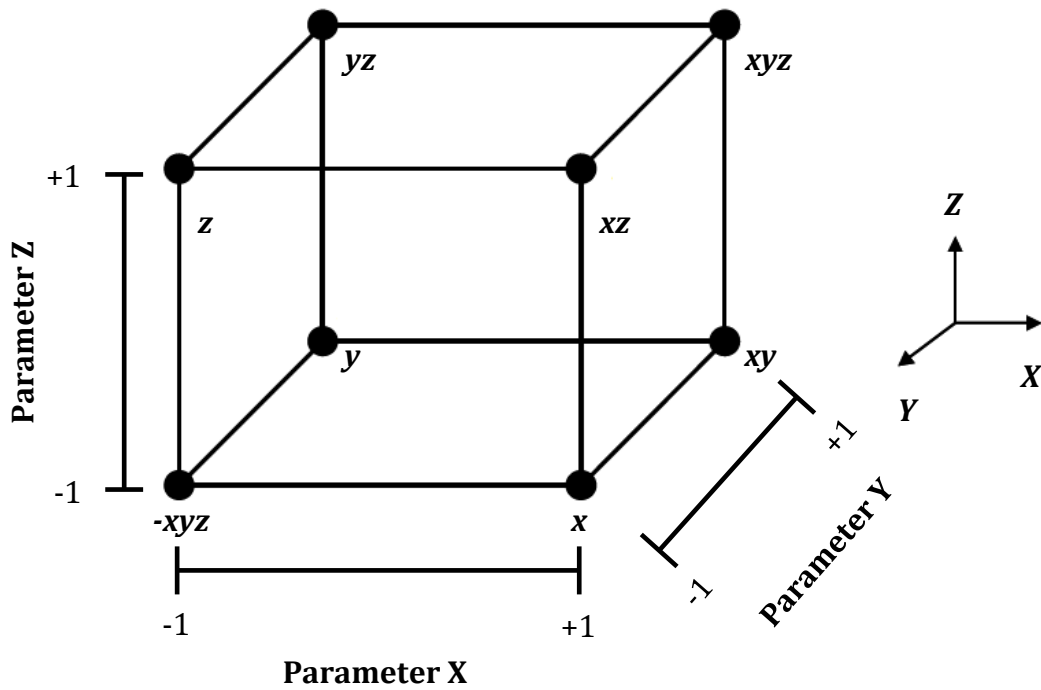


Figure 2.13. Factor level combinations of a two-level factorial design represented as the vertices of a cube.

Run	Parameter			Labels
	X	Y	Z	
1	-1	-1	-1	$-xyz$
2	1	-1	-1	x
3	-1	1	-1	y
4	1	1	-1	xy
5	-1	-1	1	z
6	1	-1	1	xz
7	-1	1	1	yz
8	1	1	1	xyz

Table 2.4. Design matrix for 2^3 factorial design.

The two-level factorial design assumes that the *effects (main and interaction)* are linear. If a quadratic *effect* is expected for a *factor*, a more comprehensive design should be used.

The three-level ($N = 3$) factorial design can be used to model curved surfaces, i.e. quadratic *effects* in the *response*. In addition to the minimum (-1) and maximum ($+1$) *levels*, the three-level design has a third central (0) *level* which can be used to estimate experimental errors and to tackle non-linearity issues. In this case, for k *factors*, a total of 3^k number of experimental runs will be required. For example, at $k = 8$, a total of 6561 experimental runs will be required by three-level factorial design. This design contains all combinations of the *factor* settings, which is more than what is necessary to model quadratic *effects* in the *response*. Furthermore, three-level full factorial designs are not computationally efficient as the sample size increases exponentially with the number of factors, proving them expensive to undertake. Hence, RS designs are mostly used to model quadratic *effects* in the *response*.

Response surface design

The response surface design provides an efficient, cost effective, way to model quadratic *effects* for continuous *factors*, as compared to three-level factorial design. RS design is actually a two-level factorial design augmented with centre and axial points. One of the most commonly used and popular types of RS designs [67, 68] is the central composite design (CCD) [45, 47, 72].

A CCD combines a two-level full factorial or fractional-factorial [71] design with centre points (where all parameters/*factors* have values at their midrange) and axial or star points (at a distance α from the design centre) which allow estimation of the curvature. The augmentation of “first order” two-level factorial design with centre and axial points makes CCD a “second-order” design. The two parameters that need to be specified in CCD are: the distance (α) of the axial points from the design centre and the number of centre runs (n_c). Figure 2.14 shows a geometrical representation of CCD for $k = 2$ *factors*, with 2^k i.e. 4 factorial points and $2k$ i.e. 4 axial points and one centre point.

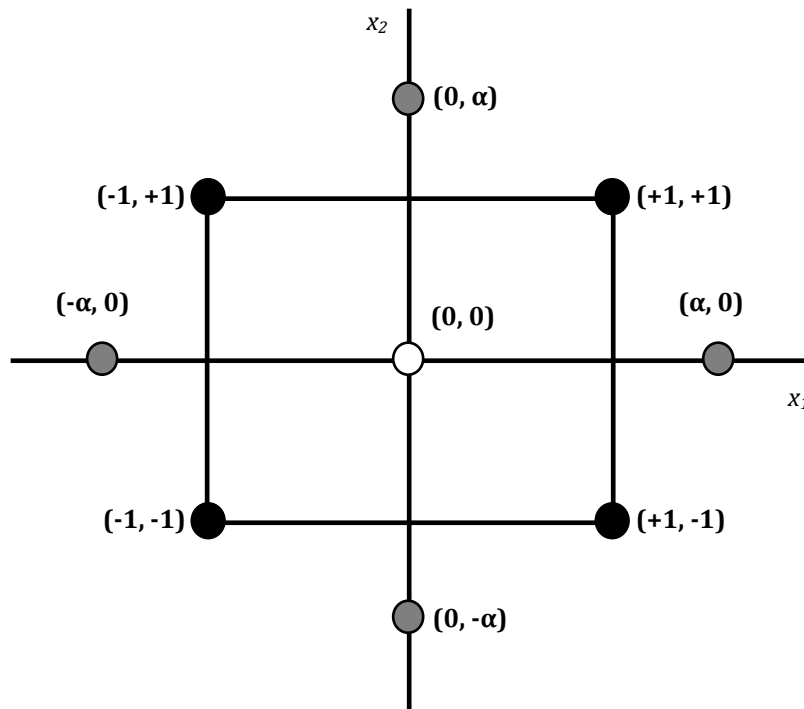


Figure 2.14. A CCD for $k=2$ factors.

Setting $\alpha = 1$, positions the axial points on the centres of the faces of the square, giving a face centred central composite design (FCCC). A FCCC design for $k = 3$ factors, with 2^k i.e. 8 factorial points, $2k$ i.e. 6 axial points and one centre point is shown in Figure 2.15.

In comparison to the three-level factorial design to model quadratic effects of factors, the CCD for 8 factors ($k = 8$) would only require a total of (2^8 factorial points, 2×8 axial points and 1 centre point) 273 experimental runs as opposed to 6561 runs by 3^k design. Hence, CCD provides a cost and time effective solution for process optimisation and modelling variability.

After selecting an appropriate design (based on the value of α , i.e. $\alpha \neq 1$ for CCD or $\alpha = 1$ for FCCC), the next step in RS modelling approach involves approximating or modelling the *response* parameter as a function of the input parameters/*factors*.

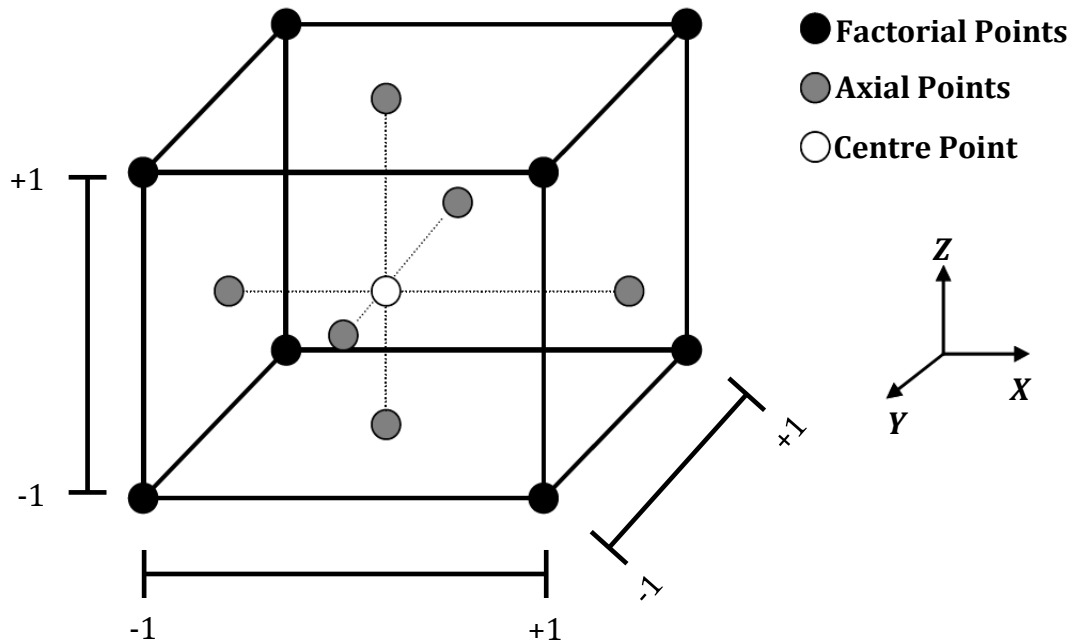


Figure 2.15. A FCCC design for $k=3$ factors.

2.5.2 Response Surface Modelling

Response surface modelling or methodology is a collection of mathematical and statistical techniques useful for modelling and analysing problems where a *response* or an output parameter under investigation is influenced by several input design parameters (*factors*) [67]. For the *response* of interest (y) and the vector of independent variables (x) included in the experimental design which influence y , the relationship between x and y is given by:

$$y(x) = f(x) + \varepsilon \quad (2.1)$$

where ε is a random error, assumed to be normally distributed with a mean of zero and a standard deviation σ . Since the actual RS function $f(x)$ is unknown, an approximate or predictive function, $g(x)$, is built using equation (2.2).

$$\hat{y} = g(x) \quad (2.2)$$

An RSM postulates a model in the form of a polynomial function, typically a low order polynomial assumed to be a linear equation given by (2.3) and obtained by designing a two-level fractional factorial experiment.

$$\hat{y} = \beta_0 + \sum_{i=1}^k \beta_i x_i \quad (2.3)$$

The second order polynomial in equation (2.4), including all two-parameter interactions, is commonly used for modelling larger variations.

$$\hat{y} = \beta_0 + \sum_{i=1}^k \beta_i x_i + \sum_{i=1}^k \beta_{ii} x_i^2 + \sum_{i=1}^k \sum_{j=1(i < j)}^k \beta_{ij} x_i x_j \quad (2.4)$$

In equations (2.3) and (2.4), k is the number of input variables/*factors*, x_i is the i^{th} input variable and β , given by equation (2.5), is the RSM coefficient calculated using least squares regression analysis to fit the response approximation \hat{y} .

$$\beta = [X'X]^{-1} X'y \quad (2.5)$$

In equation (2.5), X is the design matrix of sample data points (where the rows represent the experimental runs and the columns represent the particular setting of the *factor* or parameter for each run), X' is its transpose and y is the column vector representing the response value at each sample point.

RSM, also referred to as performance modelling, approximates the performance (*response*) of interest (e.g., noise margin, power, etc.) as a function of the parameters (*factors*) of interest (e.g., t_g , V_t , L , N_D , temperature, etc.) [73]. The linear approximation given by equation (2.3) is efficient and accurate when process variations are small. However for larger process variations, the non-linear second order response surface model given by equation (2.4) is necessary to capture these variations.

To conclude, the DoE and RSM techniques have been widely used within the TCAD environment, for the design and optimisation of process and device parameters, to reduce costly and time-consuming test wafer runs when developing new semiconductor devices or technologies [47, 59, 62, 63, 72, 74-82]. Furthermore, TCAD tools and statistical techniques, such as DoE and RSM, also aid in studying the impact of process variability on device and circuit performance which ultimately affects the functional and parametric yield of the circuit. Moreover, these techniques provide a reasonable balance between accuracy and computational efficiency, as compared to Monte Carlo simulations, by limiting the number and, hence, the complexity of simulations and modelling.

2.6 Chapter Summary and Thesis Motivation

In this chapter an overview of current advances and challenges faced by SiC technology, in particular logic devices for hostile environments, was presented. The wide bandgap and strong inter-atomic interactions in SiC allows SiC electronics to function in high temperature, high radiation and corrosive environments, beyond the scope of narrow bandgap technologies, such as Si and GaAs. The literature demonstrates the importance of SiC gas sensors for monitoring hostile environments, such as volcano vents and automotive/aircraft engines, without the need for cooling systems for the support electronics. Consequently, there is a need for high temperature sensor interface electronics for sensor signal conditioning, digitising and, finally, transmitting the data wirelessly to the base for monitoring. These sensor interface circuitries should demonstrate reliability and stability in operation across different extreme environments.

The issues with reliability and stability of high quality interfaces with SiC crystal limit the functionality of MOSFET, MESFET and BJT device topologies to 400 °C. JFET device topology, on the other hand, has shown to operate reliably for thousands of hours at 500 °C, without significant variations in electrical characteristics. However, these prototype low power JFETs are normally-on devices, require high operating bias and have large size; hence, need

improvements. With the current advance of SiC technology, commercialisation of high performance and energy efficient miniaturised devices and circuits is possible. These improvements require refining, experimenting and perhaps re-designing devices. The DoE and RSM statistical techniques have been widely used within the TCAD framework for the design and optimisation of process and device parameters; to reduce costly and time-consuming test wafer runs when developing new semiconductor devices or technologies. Consequently, there is a need for accurate simulation model for device engineers to understand device behaviour, examine performance trade-offs and verify the manufacturability of the design.

CMOS technology is ideal for digital logic, both in terms of design simplicity and power dissipation. However, oxide degradation at high temperatures has limited SiC CMOS operation to 300 °C; which seems to be a daunting challenge to achieve in near future. Generally, all the remaining SiC logic families published so far are based on RTL which means there is always certain power loss in the load resistor. Furthermore, the use of depletion (normally-on) mode transistors in logic design means that the gate works on negative logic voltage levels. Hence, an additional level shifter circuitry is needed to produce correct input voltage levels for succeeding gates. This adds complexity to logic design and results in extra power dissipation in the level shifter circuitry, limiting current SiC logic families to rudimentary functions only. Hence, for high temperature complex logic functions in SiC there is a need for an alternate technology to CMOS, with low power losses and close to rail output swing.

The current advancements in SiC wafer quality have shown improvements in wafer size, with reduction in defects and tolerance values. However, the inter-die and intra-die variations in manufacturing process parameters result in variations in device structural parameters, causing variations in device and circuit performance. Furthermore, the impact of random intra-die variations on the yield (functional and parametric) of digital circuits, such as memory cells and logic devices, is a serious issue in scaled CMOS technologies. Similarly, the scaling of SiC devices, to improve performance and functionality per unit area,

and with an addition of high temperature operations have both lead process variations to become a more dominant concern for circuit designers. Hence, with the increased sensitivity of SiC enhancement mode JFETs, and subsequent logic circuits, to process variations, failure and performance analysis is of paramount importance to enhance the yield of high temperature logic for sensor interface circuitry.

2.7 References

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Chapter 3. Modelling and Optimisation of 4H-SiC JFETs for High Temperature Operation

3.1 Introduction

A review on the advancement of SiC technology and the role of TCAD FE simulations in the development of improved, commercial, SiC devices and circuits has been presented in Chapter 2. Accurate simulation models are required by design engineers in order to understand device operation and to be able to accurately predict electrical characteristics of complex structures. These models should be based on the physical and material properties of SiC, so that the advantages provided by the superior material properties of SiC can be utilised by SiC based devices and circuits for operation in extreme environments.

This chapter presents the first comprehensive study, to the author's knowledge, on the development and validation of 4H-SiC model parameters for high temperature, low power TCAD FE simulations. Subsequently, a systematic methodology, based on TCAD simulations and statistical techniques, is devised for optimising enhancement mode 4H-SiC JFETs for low power logic devices. The optimised devices can then be fabricated and used for commercialisation of high temperature logic circuitry. The contents of this chapter are divided into five main sections. Section 3.2 discusses the 4H-SiC models and parameters used in TCAD simulations. The validation of these model parameters, using data from fabricated 4H-SiC lateral JFETs, is presented in Section 3.3. Section 3.4 begins with the discussion of proposed methodology for optimising device process parameters which is undertaken in sub-section 3.4.2. The section continues with the optimisation of n-JFET process parameters in sub-section 3.4.3. The results of optimised n- and p-JFETs, along with the discussion on the role of back-gate

bias as a means to control process variability, are presented in sub-sections 3.4.4 and 3.4.5, respectively. A comparative study on some of the important device parameters of the optimised n-JFET with comparable structures in literature is given in sub-section 3.4.6. Finally, the chapter is summarised in Section 3.5.

3.2 SiC Models and Parameters

Bandgap Energy, E_g (eV) [1]	$E_g(0) = 3.26$ $\alpha = 6.5 \times 10^{-4}$ $\beta = 1300$	
Effective Density of States in Conduction Band, N_c (cm ⁻³) [1]	1.7×10^{19}	
Effective Density of States in Valence Band, N_v (cm ⁻³) [1]	2.5×10^{19}	
Intrinsic Carrier Concentration, n_i (cm ⁻³) [1]	1.7×10^{-8}	
Relative Dielectric Constant, ϵ_r [2]	9.66	
Low Field, Doping Dependent Mobility (cm ² V ⁻¹ s ⁻¹) [3-6]	Electrons	Holes
Mobility (\perp to c-axis)	$\mu_{max} = 947$	$\mu_{max} = 124$
Anisotropic Mobility (\parallel to c-axis)	$\mu_{max} = 700$	$\mu_{max} = 114$
Minority Carrier Lifetime (s) [1]	2.6×10^{-7}	0.5×10^{-7}
Auger Recombination (cm ⁶ s ⁻¹) [7]	$C_n = 5 \times 10^{-31}$	$C_p = 2 \times 10^{-31}$

Table 3.1. Simulation parameters for 4H-SiC at 300 K.

In this section a detailed overview of the models and parameters used in TCAD simulations and theoretical calculations of this thesis has been discussed. These model parameters are based on the physical and material properties of 4H-SiC and are derived from published data. Table 3.1 summarises the model parameters for 4H-SiC used in this study. The following sub-sections discuss in detail the models for bandgap, bandgap narrowing, low field mobility, carrier recombination, incomplete ionisation and contact resistance.

3.2.1 Temperature Dependent Bandgap Energy and Intrinsic Carrier Concentration

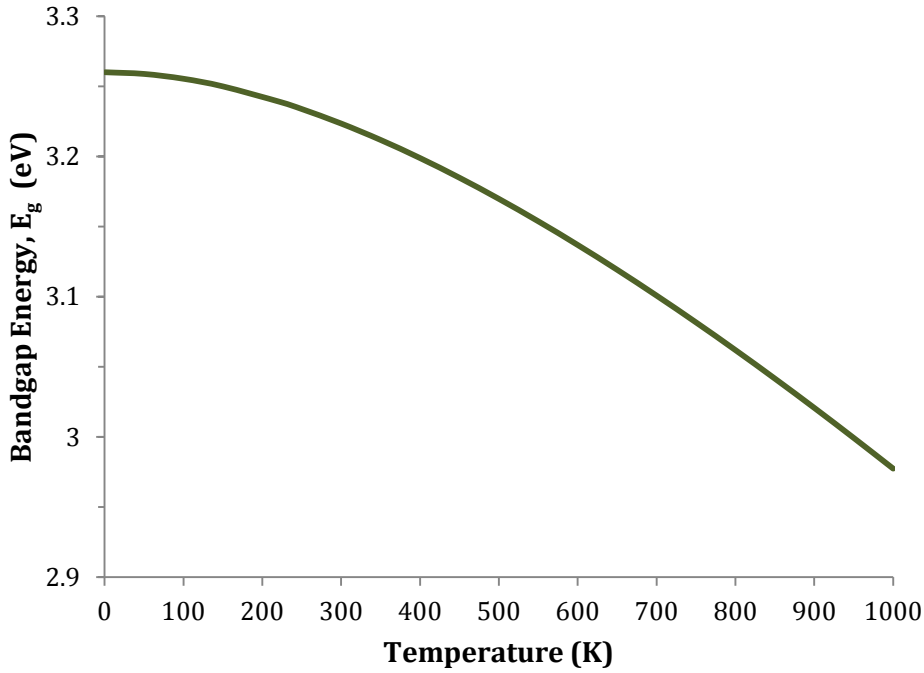


Figure 3.1. Temperature dependence of Bandgap Energy for 4H-SiC polytype.

$$E_g(T) = E_g(0) - \alpha \frac{T^2}{T + \beta} \quad (3.1)$$

One of the key attributes of SiC is its wide bandgap, E_g , which enables the realisation of radiation hardened, high temperature electronics; which is beyond the limits of Si and GaAs technology. Therefore, for high temperature device and circuit simulations, it is imperative to model the temperature dependence of bandgap energy accurately.

In Sentaurus Device⁴ [8], the band structure is simplified to four quantities: the energies of the conduction and valence band edges (or, in different parameterisation, bandgap and electron affinity) and the density of state masses

⁴ Sentaurus Device is a TCAD tool which is used to simulate electrical characteristics for structures defined either using Sentaurus Process or Sentaurus Structure Editor [36].

for electrons and holes (or, parameterised differently, the band edge density of states).

The bandgap is the difference between the lowest energy in the conduction band, E_c , and the highest energy in the valence band, E_v . Expression (3.1) determines the temperature dependence of bandgap energy of 4H-SiC [1], where T is the temperature in Kelvin, $E_g(0)$ is the bandgap energy at 0 K, and α and β are material parameters (see Table 3.1).

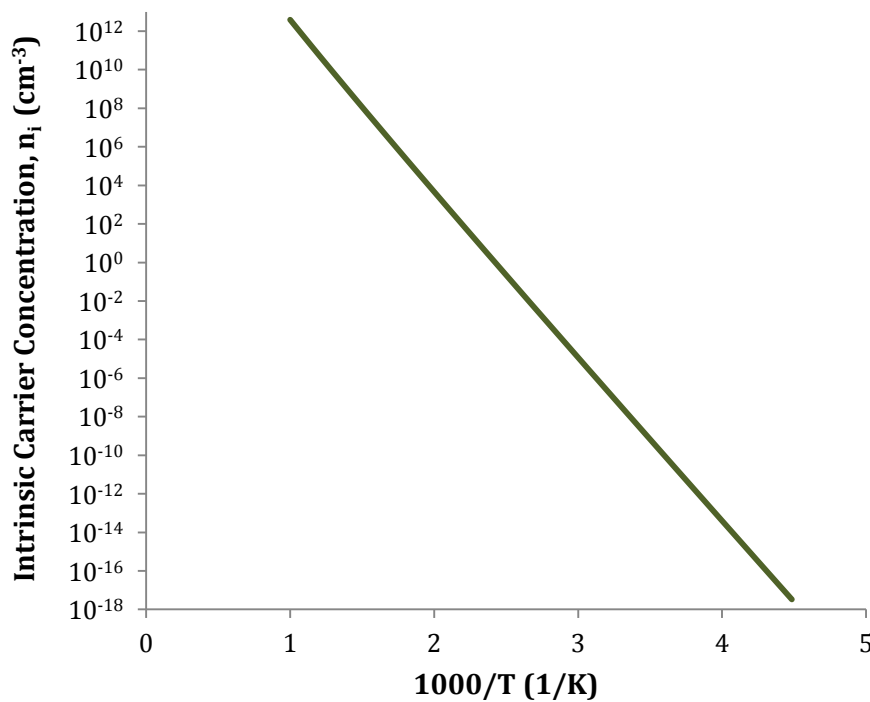


Figure 3.2. Temperature dependence of Intrinsic Carrier Concentration in 4H-SiC polytype.

The intrinsic carrier concentration (n_i) refers to the density of free carriers generated in valence and conduction bands as a result of thermal excitement of carriers from the valence band to the conduction band at a given temperature. The low value of intrinsic carrier concentration of SiC, due to its wide bandgap, is one of the major contributors towards achieving resilient technology.

The temperature dependence of intrinsic carrier concentration is given by [9]

$$n_i = \sqrt{N_c N_v} e^{\left(-\frac{E_g}{2k_B T}\right)} \quad (3.2)$$

where k_B is the Boltzmann constant, N_c and N_v are the effective density of states for conduction and valence band, respectively, and are given by [1]

$$N_c(T) = N_c(300) \left(\frac{T}{300}\right)^{3/2} \quad (3.3)$$

and

$$N_v(T) = N_v(300) \left(\frac{T}{300}\right)^{3/2} \quad (3.4)$$

where $N_c(300)$ and $N_v(300)$ are the values at 300 K (see Table 3.1).

The effect of temperature on bandgap energy and intrinsic carrier concentration is depicted in Figures 3.1 and 3.2, respectively. It is apparent that the bandgap of 4H-SiC decreases at high temperatures. This is because the increase in thermal energy increases the amplitude of atomic vibrations, increasing the interatomic spacing. Consequently, the average potential seen by the electron in the material decreases, which in turn reduces the size of bandgap energy. The reduction of bandgap energy at high temperatures gives rise to an unfavourable increase in the intrinsic carrier concentration. However, even at 1000 K, the value of n_i in 4H-SiC is still lower than the extrinsic doping concentrations used for fabricating most high temperature SiC devices. For example, a typical 4H-SiC JFET has a gate and channel doping concentration of around $1 \times 10^{18} \text{ cm}^{-3}$ and $1 \times 10^{17} \text{ cm}^{-3}$, respectively, which is much greater than its intrinsic carrier concentration (approximately $3.9 \times 10^{12} \text{ cm}^{-3}$) at 1000 K.

3.2.2 Bandgap Narrowing

High doping concentration causes a reduction in the bandgap of the semiconductor. This effect is known as bandgap narrowing and takes place due

to carrier-carrier interactions, carrier impurity interactions and overlapping impurity states. The bandgap narrowing has a significant effect on the device behaviour as the shift in the band edges create a potential barrier which influences the carrier transport across the junction [10, 11].

The model for doping induced bandgap narrowing in SiC was first reported by Lindefelt [10] who considered both n- and p-type materials. The band edge displacement for n-type material is expressed as

$$\Delta E_c = A_{nc} \left(\frac{N_D^+}{10^{18}} \right)^{1/3} + B_{nc} \left(\frac{N_D^+}{10^{18}} \right)^{1/2} \quad (3.5)$$

$$\Delta E_v = A_{nv} \left(\frac{N_D^+}{10^{18}} \right)^{1/3} + B_{nv} \left(\frac{N_D^+}{10^{18}} \right)^{1/2}$$

The band edge displacement for p-type material is expressed as

$$\Delta E_c = A_{pc} \left(\frac{N_A^-}{10^{18}} \right)^{1/4} + B_{pc} \left(\frac{N_A^-}{10^{18}} \right)^{1/2} \quad (3.6)$$

$$\Delta E_v = A_{pv} \left(\frac{N_A^-}{10^{18}} \right)^{1/3} + B_{pv} \left(\frac{N_A^-}{10^{18}} \right)^{1/2}$$

where N_D^+ and N_A^- are the ionised donor and acceptor doping concentrations, respectively. The values of parameter A_{xc} and A_{xv} ($x = n$ for n-type or $x = p$ for p-type) are given in Table 3.2.

4H-SiC	A_{xc}	B_{xc}	A_{xv}	B_{xv}
n-type	-1.50×10^{-2}	-2.93×10^{-3}	1.90×10^{-2}	8.74×10^{-3}
p-type	-1.57×10^{-2}	-3.87×10^{-4}	1.30×10^{-2}	1.15×10^{-3}

Table 3.2. Parameters for band edge displacement in 4H-SiC [10].

Using these expressions, a table of bandgap narrowing as a function of donor and acceptor concentrations was formed and imported in to Sentaurus Device for device simulation.

The effective intrinsic density, n_{ie} , (including doping dependant bandgap narrowing, E_{bgn}) is given by [8]

$$n_{ie} = n_i e^{\left(\frac{E_{bgn}}{2k_B T}\right)} = \sqrt{N_c N_v} e^{\left(\frac{E_{bgn} - E_g}{2k_B T}\right)} \quad (3.7)$$

As illustrated in Figure 3.3, the bandgap narrowing gives rise to the increase in intrinsic carrier concentration and, hence, decreases the built-in potential, V_{bi} , of the p-n junction, given by [9]

$$V_{bi} = \frac{k_B T}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (3.8)$$

where e is the electronic charge and N_A and N_D are the acceptor and donor carrier concentrations, respectively.

It is apparent that E_g , n_i and V_{bi} are all affected by high doping concentrations. The significant decrease in built-in potential gives rise to an undesired forward gate current, especially at high temperatures, and, hence, poses a limit to the maximum applied gate bias of enhancement (normally off) mode JFETs. This will be further discussed later in this chapter.

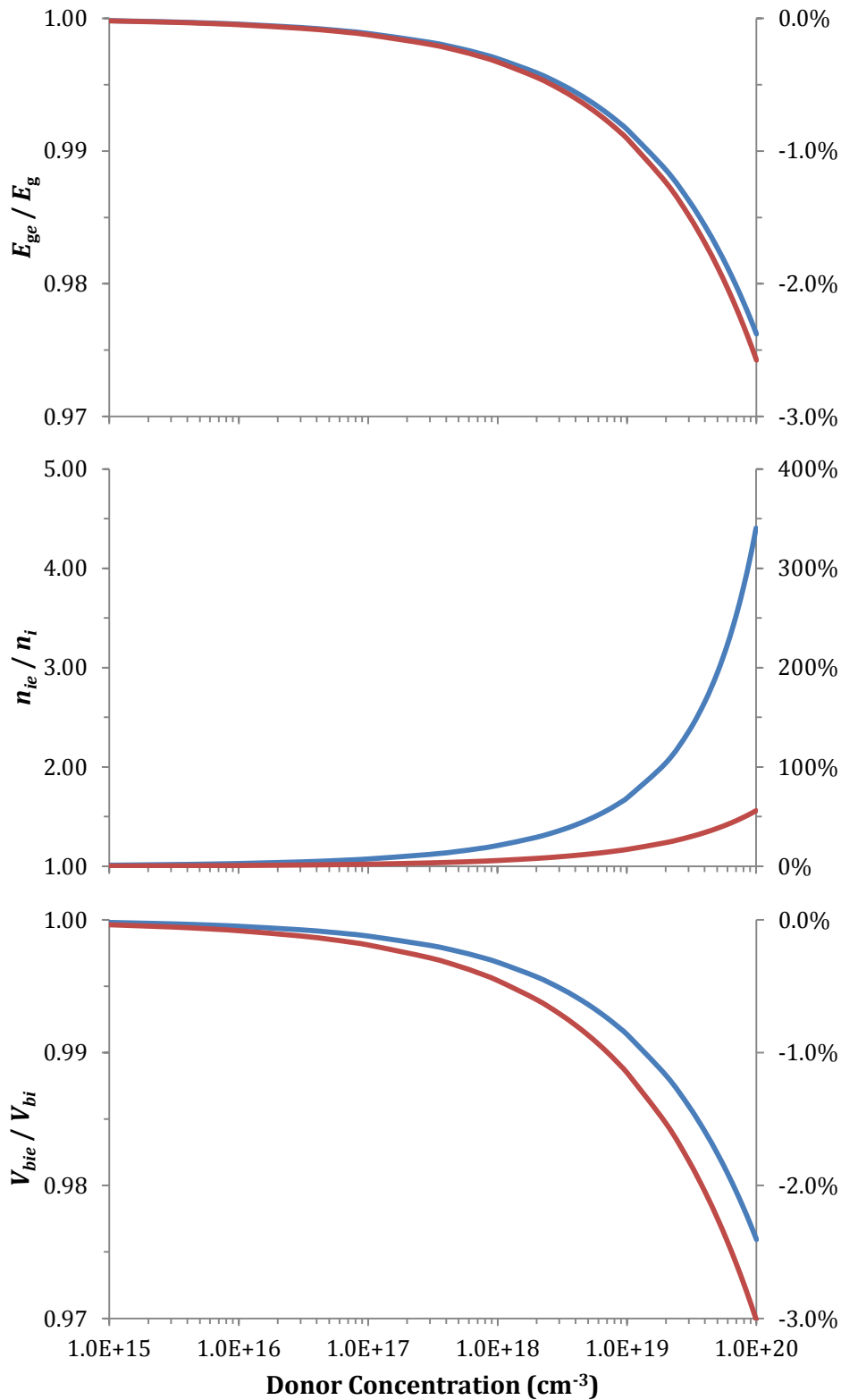


Figure 3.3. Illustrates the effect of donor concentration on the normalised values of effective bandgap energy, effective intrinsic carrier concentration and effective built-in potential ($N_A = 1 \times 10^{18} \text{ cm}^{-3}$) of 4H-SiC, at 300 K (blue) and 1000 K (red). The right hand vertical axis in each figure gives the percentage change of the normalised values.

3.2.3 Doping and Temperature Dependent Mobility Model

The mobility of carriers in a semiconductor is affected both by the total doping concentration and temperature. The lattice (optical phonon) scattering, ionised and neutral impurity scattering and anisotropic scattering [12-15] in SiC confines the mean free path of carriers at low electric fields.

The low field carrier mobility for electrons and holes in 4H-SiC is modelled by the Aurora doping and temperature dependent mobility model [16], given by

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + \left(\frac{N_{tot}}{N_0}\right)^{A^*}} \quad (3.9)$$

where

$$\mu_{min} = A_{min} \left(\frac{T}{300}\right)^{\alpha_m}, \quad \mu_d = A_d \left(\frac{T}{300}\right)^{\alpha_d} \quad (3.10)$$

$$N_0 = A_N \left(\frac{T}{300}\right)^{\alpha_N}, \quad A^* = A_a \left(\frac{T}{300}\right)^{\alpha_a}$$

The parameter μ_{min} represents the minimum mobility of electrons or holes, μ_d is the difference between the maximum, μ_{max} , and minimum mobility values, N_0 represents the reference concentration, while A^* is an exponential factor that controls the slope around $N = N_0$. For these four parameters (μ_{min} , μ_d , N_0 , and A^*), coefficients and exponents of the normalised temperature are represented by A_{min} , A_d , A_N and A_{min} and α_m , α_d , α_N and α_a , respectively. The values of these fitted model parameters are given in Table 3.3.

Schaffer *et al.* [4] carried out the first comprehensive analysis of carrier mobility in SiC. This was later followed by two other studies by Carter [17] and by Nakashima [18]. This data is illustrated in Figure 3.4, along with the best fit of

the Aurora doping dependent mobility model. Furthermore, in order to check the adequacy of the Aurora model parameters, the fit from Aurora is compared with that from the carrier mobility model for SiC device simulation, proposed by Mnatsakanov *et al.* [19]. The Aurora model parameters show excellent agreement with the measured values to nearly six orders of magnitude of doping concentration. Finally, the temperature dependence of the Aurora mobility model and the model by [19] is represented in Figure 3.5 for a doping concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$. At a given temperature, the hole mobility is far smaller than the electron mobility, due to higher hole effective mass, resulting in lower transconductance for p-type JFETs.

Parameter	Electron Value	Hole Value	Unit
A_{\min}	40	40	$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
α_{\min}	-1.538	-1.538	1
A_{d}	910	82	$\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$
α_{d}	-2.397	-2.2397	1
A_{N}	2.0×10^{17}	6.3×10^{18}	cm^{-3}
α_{N}	0.75	0.75	1
A_{a}	0.76	0.55	1
α_{a}	0.722	0.722	1

Table 3.3. Mobility parameters for Arora model (4H-SiC).

Although the anisotropic properties of 4H-SiC resulting from its hexagonal crystalline structure [20] is not significant, accounting for around 5% change in the device current flow, the anisotropic mobility was nevertheless taken into consideration to report trends as close as possible to the real device.

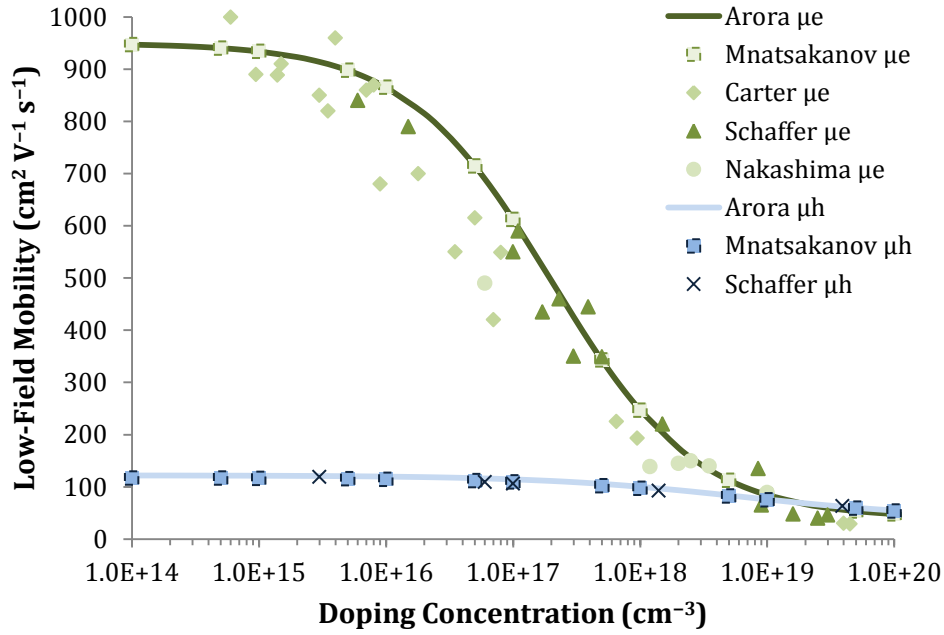


Figure 3.4. Measured and modelled low-field electron (μ_e) and hole (μ_h) mobility versus doping concentration for 4H-SiC, at 300 K [4, 16-19].

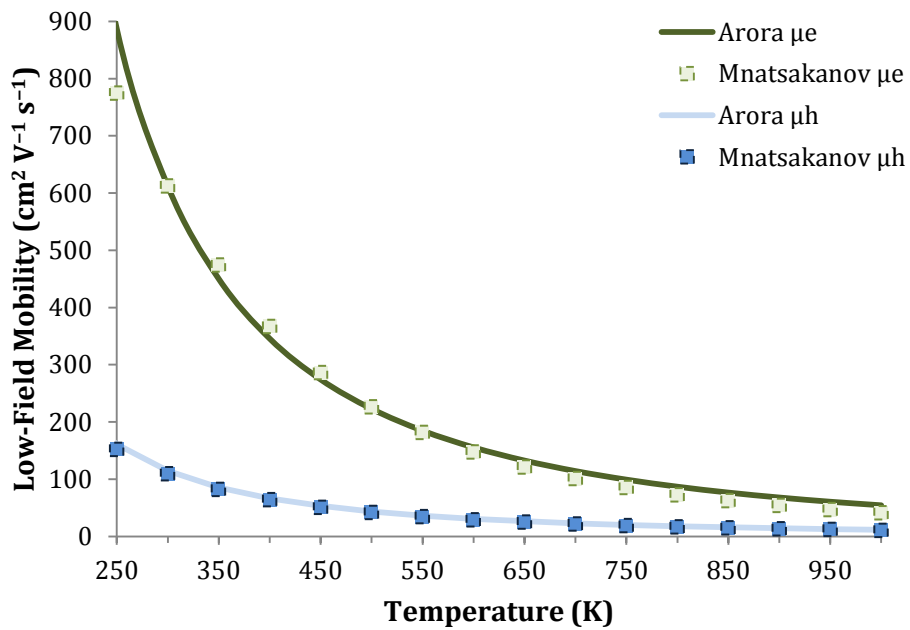


Figure 3.5. Measured and modelled low-field electron (μ_e) and hole (μ_h) mobility versus Temperature for 4H-SiC, at a doping concentration of $1.0 \times 10^{17} \text{cm}^{-3}$ [16, 19].

3.2.4 Carrier Recombination

Generation and recombination are processes through which carriers are exchanged between the conduction and valence band. For example, the injection of excess carriers results in the recombination of injected carriers which restores the equilibrium, i.e. $np = n_i^2$.

The balance equation for each generation-recombination centre yields a Shockley-Read-Hall (SRH) rate within the quasi-static approximation [21]. SRH recombination is defined as a process with phonon transitions through deep defect levels in the bandgap. The SRH recombination rate is given by

$$R_{SRH} = \frac{(np - n_{ie}^2)}{\tau_p \left(n + n_{ie} e^{\left(\frac{E_{trap}}{k_B T}\right)} \right) + \tau_n \left(p + n_{ie} e^{\left(-\frac{E_{trap}}{k_B T}\right)} \right)} \quad (3.11)$$

where E_{trap} represents the difference between the trap energy level, E_t , and the intrinsic Fermi energy, E_i , i.e. $E_{trap} = E_t - E_i$. τ_p and τ_n are the minority carrier life times of holes and electrons, respectively, specified in Table 3.1. The doping and temperature dependence of τ_p and τ_n are given by [8]

$$\tau_c = \tau_{min} + \left(\frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^\gamma} \right) \quad (3.12)$$

$$\tau_c(T) = \tau_c(300) \left(\frac{T}{300} \right)^\alpha \quad (3.13)$$

where $c = n$ for electrons or $c = p$ for holes.

At high doping levels and in the high injection regime, Auger recombination becomes important. This occurs due to the direct band-to-band recombination between an electron and a hole across the forbidden gap, which is followed by the transfer of energy to another free electron or hole [7]. The Auger recombination is given by [22]

$$R_{Auger} = C_n(pn^2 - nn_{ie}^2) + C_p(np^2 - pn_{ie}^2) \quad (3.14)$$

where C_n and C_p are the Auger coefficients for electrons and holes, respectively, given in Table 3.1.

3.2.5 Incomplete Ionisation

In silicon carbide, the energy levels of dopants are much deeper than in silicon and the thermal energy, $k_B T$, at low temperatures (even at RT) is not enough to fully activate all of donor and acceptor impurity atoms. Therefore, the dopants are not fully ionized at low temperatures [23-28], giving rise to a phenomenon known as incomplete ionisation. This effect is also known as dopant freeze-out in Si at low temperatures [29].

The ionised carrier concentration is calculated by solving the charge neutrality equation, i.e. the total negative charge (electron, n , and ionised acceptors, N_A^-) must be equal to the total positive charge (holes, p , and ionised donors, N_D^+):

$$N_D^+ - N_A^- + p - n = 0 \quad (3.15)$$

These are related to the energy levels through the following equations [8, 29, 30]

$$N_D^+ = \frac{N_D}{1 + g_D e^{\left(\frac{E_F - E_D}{k_B T}\right)}} \quad (3.16)$$

$$N_A^- = \frac{N_A}{1 + g_A e^{\left(\frac{E_A - E_F}{k_B T}\right)}} \quad (3.17)$$

$$n = N_c e^{\left(\frac{E_F - E_c}{k_B T}\right)} \quad (3.18)$$

$$p = N_v e^{\left(\frac{E_v - E_F}{k_B T}\right)} \quad (3.19)$$

where g_D and g_A are the degeneracy factors for the impurity levels, E_F is the Fermi energy, E_D and E_A are the energy levels of donors and acceptors, respectively, and are related to activation energy of donor, ΔE_D , and acceptor, ΔE_A , by

$$\Delta E_D = E_c - E_D \quad \text{and} \quad \Delta E_A = E_A - E_v. \quad (3.20)$$

Furthermore, ΔE_D and ΔE_A are effectively reduced by the total doping in the semiconductor. This effect is accounted for in Sentaurus by [8]

$$\Delta E_A = \Delta E_{A,0} - \alpha_A (N_A + N_D) \quad (3.21)$$

$$\Delta E_D = \Delta E_{D,0} - \alpha_D (N_A + N_D) \quad (3.22)$$

In this work nitrogen and aluminium are used as dopant species for donors and acceptors, respectively. The values of the parameters used in the incomplete ionisation model are given in Table 3.4.

Dopant Type	g_x	α_x (eVcm)	$\Delta E_{x,0}$ (eV)
Donor (N)	2	3.1×10^{-8}	0.06
Acceptor (Al)	4	3.1×10^{-8}	0.191

Table 3.4. Incomplete ionisation parameters for 4H-SiC [1].

3.2.6 Contact Resistance

In order to assist the formation of contacts, the source and drain regions of the JFETs are implanted by highly doped, $1 \times 10^{20} \text{ cm}^{-3}$, Al or N for p- and n-channel devices, respectively, and to a depth of 0.1 μm beneath the surface. Unless otherwise stated, all contact resistances in this study are specified as $1 \times 10^{-4} \Omega\text{cm}^2$. This is a typical value of specific contact resistance for both n- and p-type material and reliable contacts on real devices are close to this value [31-33].

3.2.7 SiC Models and Parameters Summary

The 4H-SiC models and parameters for high temperature, low power TCAD FE simulations have been presented in Section 3.2. The model parameters are based on the physical and material properties of 4H-SiC and their values are extracted from published data. The following section details the validation of model parameters using data from fabricated 4H-SiC JFETs.

3.3 Characterisation and Validation of Physical Model – High Temperature 4H-SiC JFET

This section details the validation of model parameters (based on the physical and material properties of 4H-SiC) for TCAD FE simulations⁵ used in this study. The data from high temperature 4H-SiC JFET for low power applications, fabricated and characterised by [34] at Newcastle University, is used to validate the model parameters.

3.3.1 Device Structure

The epitaxial gated lateral JFET was fabricated using a wafer supplied by Cree [35]. The quoted wafer specification illustrated in Figure 3.6 comes with a $\pm 10\%$ variation in epi-layer thickness and doping density from the manufacturer [35].

p-type (Al: $2 \times 10^{19} \text{ cm}^{-3}$)	0.2 μm
n-type (N: $1 \times 10^{17} \text{ cm}^{-3}$)	0.3 μm
p-type (Al: $2 \times 10^{15} \text{ cm}^{-3}$)	5.0 μm

Figure 3.6. Cross-sectional epi-layer characteristics of 4H-SiC wafer used for fabricating epitaxial gated lateral JFETs. The specification includes a $\pm 10\%$ tolerance [35].

In order to calibrate the model parameters for TCAD FE simulation, the cross-section of the fabricated JFET (after incorporating results from secondary ion mass spectrometry (SIMS) depth profile for the substrate, discussed later in this

⁵ Device simulators, such as TCAD Sentaurus Device [8], work on the basis of different device models and their parameter values. Based on the nature of the device being simulated, i.e. high power, low power, high temperature, etc., appropriate models are selected to accurately predict the electrical characteristics of the device. These device simulators come with several models along with their default parameters. However, in the case of SiC, having different polytypes, these default model parameters are not adequate for accurate device simulations. Hence, model parameters based on the physical and material properties for the appropriate SiC polytype can be used to accurately predict the device electrical characteristics.

section) was defined in Sentaurus Structure Editor [36]. This cross-section is shown in Figure 3.7.

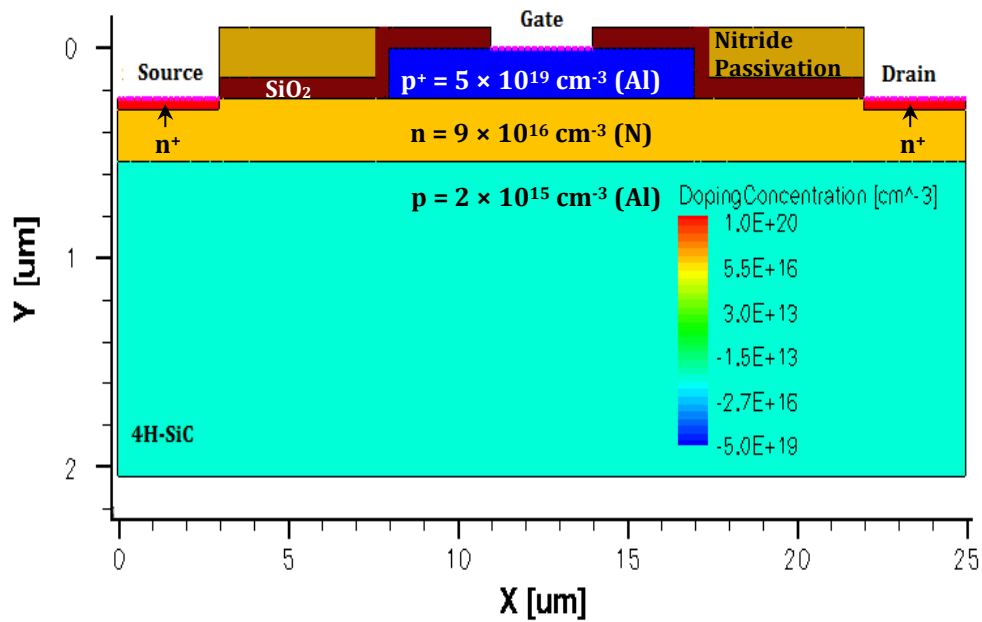


Figure 3.7. Cross-section of the device structure and doping profile of 4H-SiC epitaxial gated lateral JFET.

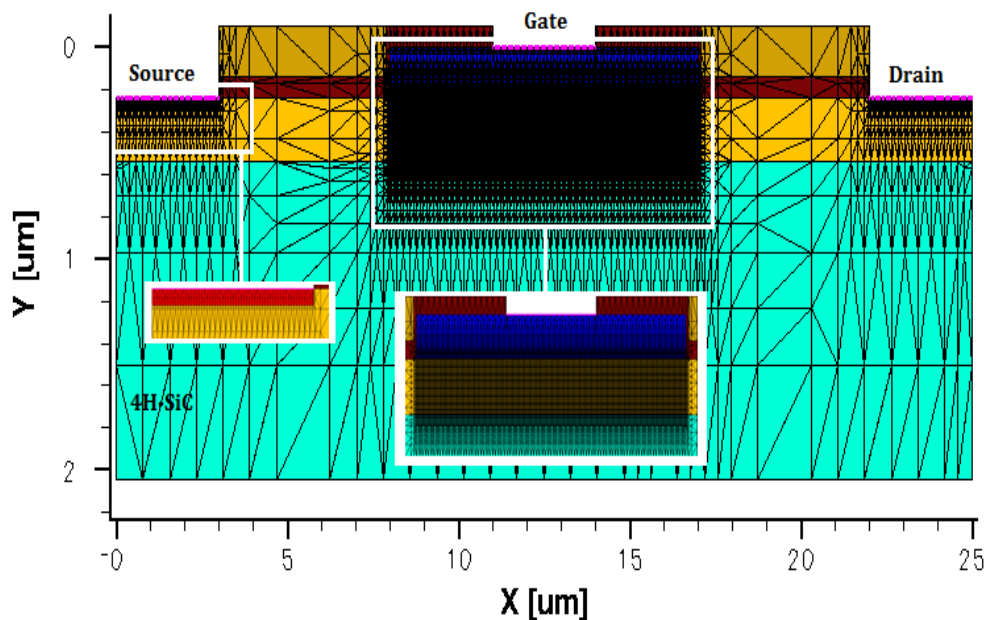


Figure 3.8. Simulation mesh of 4H-SiC epitaxial gated lateral JFET; inset shows the mesh refinement surrounding the critical regions at the contacts and the channel.

The meshed JFET structure used for device simulation is shown in Figure 3.8. In addition to using appropriate models and their parameters for a particular device material, the accuracy of the simulation also depends upon the density of the mesh used to define the device. The inset of Figure 3.8 shows a densely meshed p-n junction and channel regions. Such refinements are required to accurately determine the threshold voltage, V_t , and hence the currents through the device.

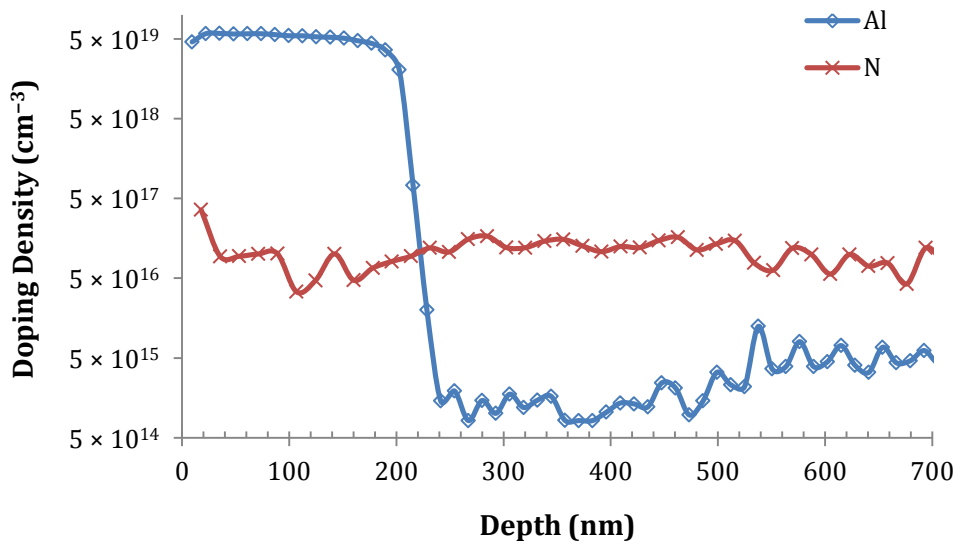


Figure 3.9. SIMS depth profile of aluminium and nitrogen (background noise level: Al = $2.0 \times 10^{14} \text{ cm}^{-3}$ and N = $2.5 \times 10^{17} \text{ cm}^{-3}$) [34].

The SIMS depth profile for the substrate used to fabricate epitaxial gated JFETs is used to further analyse the epi-layer characteristics. This SIMS profile is given in Figure 3.9. The $5 \times 10^{19} \text{ cm}^{-3}$ aluminium gate region at the surface extends approximately 220 nm into the semiconductor. This is followed by nitrogen doped epi-layer, which forms the channel. The background noise level for the SIMS setup used here ($2.5 \times 10^{17} \text{ cm}^{-3}$ for nitrogen) is well above the N doping level. Hence, it is hard to see how deep this region extends. However, the observed small rise in the Al doping profile at around 520 nm below the surface indicates a channel depth of approximately 300 nm. A 10% less value of the specified nitrogen doping concentration (i.e. $9 \times 10^{16} \text{ cm}^{-3}$) is suggested by [37] and is supported by a lower experimental and theoretical value of V_t [34].

The device has a gate of length $9\ \mu\text{m}$ (in the x -direction) and a gate width $150\ \mu\text{m}$ (in the z -direction). The source and drain contact regions ($50\ \text{nm}$ thick beneath the contacts, in the y -direction) are highly doped with a nitrogen concentration of $1 \times 10^{20}\ \text{cm}^{-3}$ to assist contact formation. Finally, the electrical simulations are performed with TCAD Sentaurus Device [8] using physical models detailed in Section 3.2.

3.3.2 Results and Discussion

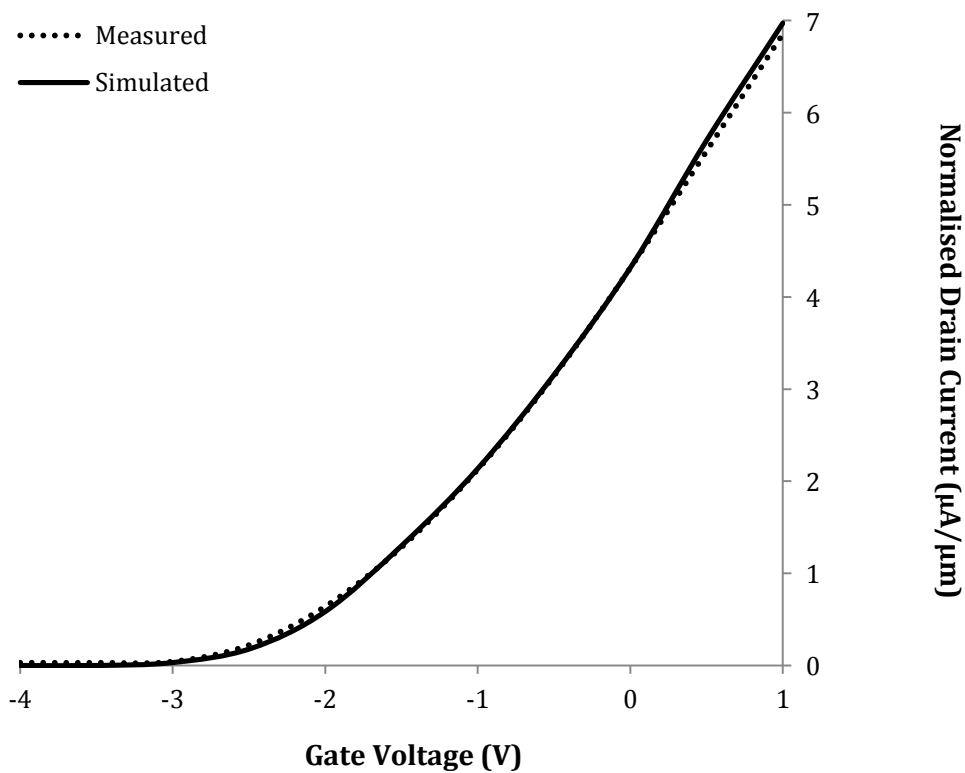


Figure 3.10. Comparison of measured and simulated (normalised, see text) transfer characteristics of 4H-SiC epitaxial gated lateral n-JFET at 300 K ($V_d = 5\ \text{V}$).

The transfer characteristics of a normalised (i.e. device with $1\ \mu\text{m}$ wide channel) 4H-SiC epitaxial gated lateral n-JFET is presented in Figure 3.10. The simulated result shows excellent agreement with the measured data, indicating the accuracy of the calculated threshold voltage and drain saturation currents.

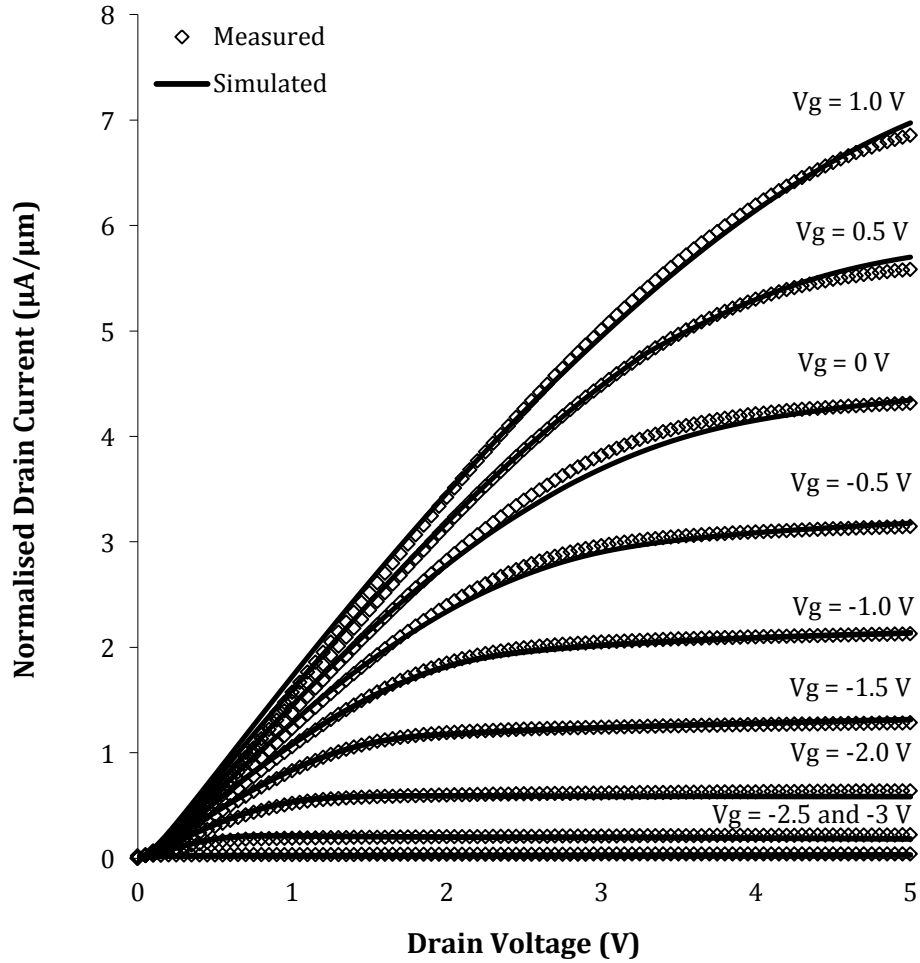


Figure 3.11. Comparison of measured and simulated (normalised) I_d - V_d characteristics of 4H-SiC epitaxial gated lateral n-JFET at 300 K.

The normalised drain current-voltage (I_d - V_d) characteristics for gate bias, V_g , ranging from 1 to -3 V is shown in Figure 3.11. The simulated results are in close agreement with the measured data, emphasising the accuracy of the model parameters. The SIMS surface analysis of the contacts indicates that the fabricated device has a high value of contact resistance. The root of this problem is the variations in deposition and annealing processes which can lead to material parameter deviations, such as in silicide formation and in the poly or metal lines. These material parameter variations suffering from wafer-to-wafer and within-wafer deviations can contribute to reasonable contact and line-resistance variation [38]. This is incorporated in Sentaurus Device by increasing the contact resistance to $4.5 \times 10^{-3} \Omega\text{cm}^2$, which is approximately an order higher than the typical SiC specific contact resistance value of $1 \times 10^{-4} \Omega\text{cm}^2$ [31-33].

3.3.3 Validation Summary

To conclude, the validation of model parameters (based on the physical and material properties of 4H-SiC) for FE TCAD simulations was presented using data from fabricated 4H-SiC JFETs. The results from the FE simulation model were found to be in close agreement with the measured data. The validated model parameters are used for designing and optimising improved 4H-SiC JFETs in the next section.

3.4 Optimisation of Four Terminal 4H-SiC Enhancement Mode JFETs for High Temperature Digital Logic

3.4.1 Background

In the last decade or so, many prototype SiC devices and logic circuits have been demonstrated which have surpassed the performance of Si for the ability to function in extreme environments [39-45]. The advance of silicon carbide technology has now reached a stage where commercialisation of high performance and energy efficient miniaturised devices and circuits is possible. These devices and circuits should be able to operate on the limited power resources available in harsh and hot hostile environments [46, 47]. These improvements require refining, experimenting and perhaps re-designing devices which can rightly claim their share in the current silicon dominant market. Consequently, there is a need for accurate simulation models for device engineers to understand device behaviour, examine performance trade-offs and verify the manufacturability of the design.

The high temperature TCAD FE simulation model, based on 4H-SiC physical and material properties, was developed and is discussed in detail in Sections 3.2 and 3.3. Using two-dimensional TCAD tools (Sentaurus Structure Editor [36] and Sentaurus Device [8]), the calibrated FE model is used to design and characterise high temperature four terminal enhancement mode n- and p-channel JFETs. The normally off nature of these devices is desirable for CJFET logic devices in terms

of reduced gate drive complexity and power dissipation [39]. The advantages of CJFET logic devices over other known logic types were discussed in detail in section 2.3.2. The device structure studied for n- and p-JFET is illustrated in Figure 3.12. The device parameters are defined by: channel length (L), channel thickness (t_c), channel doping (N_D or N_A for p-JFET), back gate doping (N_A or N_D for p-JFET), gate doping (N_{A^+} or N_{D^+} for p-JFET) and gate implant depth (t_g). At this point it is worth noting that although the implanted gate is considered in this work, the trends shown are equally valid for epitaxial gated devices; where the implanted gate is replaced by an epitaxial layer over the channel and the new channel thickness (t_c) = 0.5 – gate implant depth (t_g).

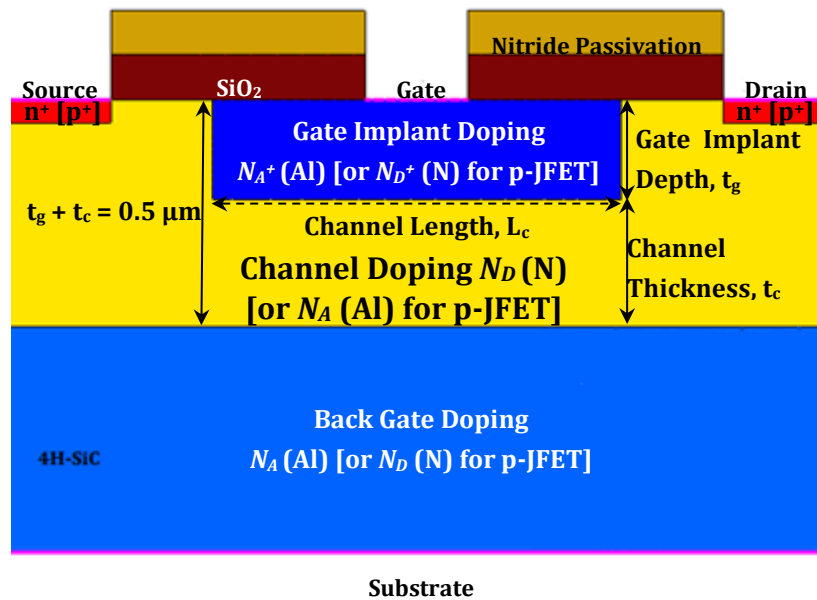


Figure 3.12. Device Structure for n- [and p-] channel lateral JFET.

The next step is to ascertain the optimised process parameters for device design and bias potentials, so that the device can function across a wide temperature range using the same set of drain and gate biases. This will be a milestone in the design of low power logic circuitry. Previous major contributions from Nudeck *et al.* [46, 47] demonstrated prototype devices in SiC which require not just variable, but high values of bias potentials for successful operation across the entire temperature range. These, variable, high bias voltages are not feasible for

commercial/practical SiC devices for operation in extreme environments. Therefore, a new systematic statistical approach, based on DoE and RSM techniques, has been utilised to optimise energy efficient, high performance n- and p-JFET for operation in extreme environments. This methodology is discussed in detail in the next section.

3.4.2 Methodology for Optimisation

The methodology consists of TCAD FE simulations and the use of DoE techniques such as RSM for statistical analysis and modelling. DoE and RSM statistical techniques have been widely used in multidisciplinary fields to model variability and optimise manufacturing processes [48-55]. These techniques have been used in research to model semiconductor process variability and as a tool for optimisation [48, 49, 56-67] because of their computational efficiency and accuracy as compared to Monte Carlo techniques [68]. Hence, these techniques can help to improve existing processes and to develop new products and processes. A detailed review on DoE and RSM methodology was presented in Section 2.5. The overall approach to model and analyse process optimisation is shown in Figure 3.13. The following sub-sections give a step-by-step description of the proposed methodology.

Optimum Bias Potential

The first step is to ascertain a fixed set of maximum drain and gate biases so that the undesired forward gate current (also known as gate leakage) is minimal for the entire temperature range ($27\text{ }^{\circ}\text{C} \leq T \leq 500\text{ }^{\circ}\text{C}$) studied in this optimisation process. Minimal forward gate current is crucial for the design of low power digital logic. High gate leakage currents lead to unfavourable increases in power dissipation within a device. The gate leakage in an enhancement mode JFETs is due to the forward biased p-n junction that forms the gate and is directly related to the applied gate bias and the built-in potential of the junction (see section 3.2.2). In this case, the maximum gate bias should be less than the built-in potential at $500\text{ }^{\circ}\text{C}$, 2.3 V. As a result, a value of $|2|\text{ V}$ is set for both gate and drain biases to minimise excessive gate leakage at high temperatures. The back-

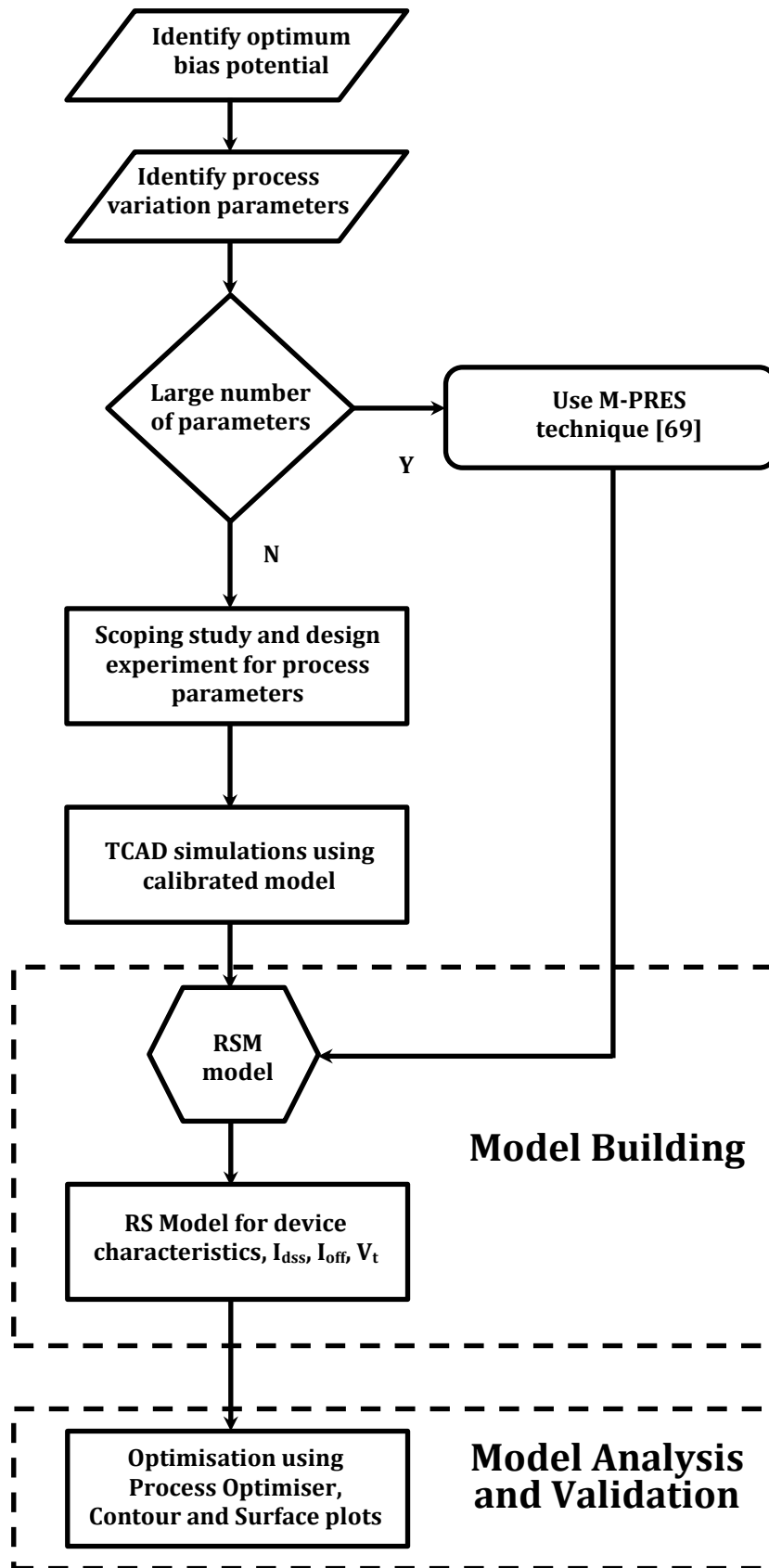


Figure 3.13. Flow diagram illustrating methodology for modelling process optimisation.

gate, which offers an end product, external correction mechanism to counter act process variations, is also set to $|2|$ V to initiate the optimisation process. The role of back-gate bias in controlling device parameters will be discussed in detail in section 3.4.5.

Process Variation Parameters (*factors*), Scoping Study and Design of Experiment

One of the most important steps in optimising the design of 4H-SiC enhancement mode JFETs is to identify the key process parameters (*factors*) and their range. The parameter space considered in this study is provided in Table 3.5. A detailed scoping study based on systematic testing of boundary conditions and worst case scenarios is conducted to obtain the range for varying process parameters, such that the core objectives of device optimisation can be achieved within the studied range. The objectives are listed below:

- For the entire temperature range ($27\text{ }^{\circ}\text{C} \leq T \leq 500\text{ }^{\circ}\text{C}$) studied, the optimised device should have a positive threshold voltage, $V_t > 0$, for n-JFET (and negative for p-JFET, $V_t < 0$), required for enhancement mode operation.
- The threshold voltage at RT should be less than the maximum applied gate bias (v_g), established earlier. That is, $|V_t| < |V_g| < 2\text{ V}$.
- The optimum device should have a high on-to-off state current-ratio. In other words, the device should have as high as possible value of drain saturation current, I_{dss} , and the lowest possible value of drain leakage current, I_{off} , (i.e. drain current at zero gate bias), keeping in mind the constraints of V_t specified in the first two points. A high on-to-off state current-ratio ($> 10^2$) is crucial for low power logic devices with fast switching and high noise margin, especially at high temperatures.
- The optimum point, i.e. the value of the process parameters for optimum device design, should indicate stability in terms of manufacturability of

the design and variability of process parameters (due to *inter-* and *intra-die variations*, discussed in Section 2.4). The influence of process variation at both device and circuit level is discussed in detail in Chapter 5.

If the number of significant *factors* is more than ten, an alternative approach, multi-level partitioned response surface (M-PRES) in [69], can be adopted. This method prevents omitting less significant *factors*, but rather screens and partitions the *response and factors* into groups. The partitioned response surface models are then developed, which take into account the effect of all *factors*. In this case, however, there are only five *factors* and therefore screening of less significant factors is not necessary. Hence, standard RSM is performed directly, giving a model which is a function of all the process parameters/*factors*.

Symbol	Process Parameters (factors)	Units	Lower	Higher
			Value	Value
			-1	+1
x_1	Gate Length, L	μm	2.0	4.0
x_2	Gate Implant Depth, t_g	μm	0.22	0.26
x_3	Gate Implant Doping, N_{A^+}	cm^{-3}	1.0×10^{18}	1.0×10^{19}
x_4	Channel Doping, N_D	cm^{-3}	9.0×10^{16}	1.1×10^{17}
x_5	Back Gate Doping, N_A	cm^{-3}	1.0×10^{17}	1.0×10^{18}

Table 3.5. Key process parameters for optimising enhancement mode 4H-SiC JFETs for CJFET technology.

In order to assist in achieving the set objectives, the threshold voltage (V_t), drain saturation (I_{dss}) and drain leakage (I_{off}) currents are targeted as the device performance metrics (*response*) of interest for optimisation. V_t is extracted from the extrapolated x -intercept of $\sqrt{I_d}$ vs. V_g plot at $V_d = 2$ V. I_{dss} is the drain current (I_d) at $|V_d| = |V_g| = 2$ V and I_{off} is the off- state drain leakage current at $V_d = 2$ V and $V_g = 0$ V.

Next, an experiment is designed in order to carry out the TCAD FE simulations. This is to obtain the *responses* from variations in the process parameters which are later used for optimisation using RSM. The design of this experiment is totally dependent on the type of response surface design used. In this study, the central composite design (the most popular type of RS design method [53]) is considered to approximate a second-order RS model and, hence, to study the second-order effects. CCD is discussed in detail in Section 2.5.1. The CCD for five *factors* ($k = 5$) would require a total of 43 experimental runs (2^5 factorial points, 10 axial points and 1 centre point). Hence, using calibrated FE model parameters, a total of 86 TCAD structure and device simulations, both at RT and 500 °C, are performed and the corresponding *responses* are modelled using RSM.

RS Model Building, Analysis and Validation

The RS model, based on variations in the process parameters (*factors*) and the corresponding *response*, is built on using commercial statistical software, Minitab [70]. A logarithmic transformation of x_3 , x_4 and x_5 was performed due to their values being large in comparison to the other two *factors*. Similarly, while modelling the drain saturation, I_{dss} , and leakage, I_{off} , currents, logarithmic transformation has been used as their values are low with a large variation. The analysis, process optimisation and validation of the model are conducted, keeping in mind the set objectives for optimisation. The model, validation and optimisation results for n-JFET are discussed in the next section.

3.4.3 Optimisation of n-JFET using RSM Technique

Model Building

The first step in the optimisation process is to build a RS model which can precisely relate the *factors-response* variation relationship. Therefore, for each of the *responses*, V_t , I_{dss} and I_{off} , regression analyses are conducted to generate an equation to describe the statistical relationship between the *factors* and the response and this is then used to predict new observations. Regression results indicate the direction, size, and statistical significance of the relationship between a *factor* and *response*. The sign of each coefficient indicates the

direction of the relationship. Coefficients represent the mean change in the response for one unit of change in the *factor* while holding other *factors* in the model constant. Finally, the equation predicts new observations given specified *factor* values. Equation 3.23 gives the RS model for the threshold voltage, V_t , of n-JFET, at 500 °C, in terms of the process parameters (*factors*) – denoted by x_1, x_2, \dots, x_5 in Table 3.5. The model coefficients in this equation are normalised to the coded values of the statistically designed CCD experiment.

$$\begin{aligned}
 V_{t\ 500\ ^\circ\text{C}}(V) = & 1.6025 - 0.0474x_1 + 0.2663x_2 + 0.1233x_3 - 0.2020x_4 \\
 & + 0.3986x_5 + 0.0582x_1^2 - 0.0469x_2^2 - 0.0194x_3^2 \\
 & - 0.0401x_4^2 - 0.1946x_5^2 - 0.0207x_1x_2 + 0.0237x_1x_3 \quad (3.23) \\
 & + 0.0002x_1x_4 - 0.0577x_1x_5 + 0.0013x_2x_3 + 0.0712x_2x_4 \\
 & - 0.1541x_2x_5 - 0.0193x_3x_4 + 0.0150x_3x_5 + 0.1307x_4x_5
 \end{aligned}$$

The models for the other n-JFET device *responses*, constructed using this approach, are given in Appendix A.

Model Validation

In order to check accuracy and validity, the models were checked using the quality of the second-order fit, R^2 and R^2_{adj} (adjusted) [53, 55]. R^2 is the coefficient of determination and statistical measure of how well the regression line approximates the actual data points. The value of R^2 is between 0 (0%) and 1 (100%). The larger it is, the better the model equation fits the actual data. High values of R^2 can, however, be deceiving as including additional parameters to the model, which may not be statistically significant, can artificially increase *its* value. Hence, models with large R^2 values may result in a poor functional fit, leading to poor prediction of the response. This leads to considering R^2_{adj} which is a modified R^2 , adjusted to account for the number of terms in the model. Unlike R^2 , R^2_{adj} may become smaller when unnecessary or additional terms are added to the model. High R^2_{adj} values are desired as values much lower than R^2 indicate inclusion of unnecessary term(s) in the model which could be removed without affecting the quality of the fit. These statistically insignificant terms

could either be identified by trial and error or by further examination of the results, as explained in [53, 55].

The R^2 and R^2_{adj} for the n-JFET *responses* are summarised in Table 3.6. The values close to the desired 100% mark indicate that the second-order RS model captures a large portion of the observed variance. While fitting the model for I_{dss} and I_{off} , the initial values of R^2 and R^2_{adj} were very poor; and were improved by logarithmic transformation.

Device Response	R^2 (%)	R^2_{adj} (%)
V_t at 27°C	98.29	96.73
V_t at 500°C	99.14	98.36
I_{dss} at 500°C	99.55	99.14
V_{off} at 500°C	99.80	99.63

Table 3.6. RS model fits for n-JFET device *responses*.

The model fit for the *responses*, V_t , I_{dss} and I_{off} , is graphically illustrated in Figure 3.14. The straight line with unit gradient represents the ideal fit, where the actual values are scattered. In the *response* model fit for V_t at 27 and 500 °C, Figures 3.14. (a) and (b), the fit values deviate slightly from the actual values. This is also reflected by the lower R^2 and R^2_{adj} values for these two *responses* and can be accounted for by the error in determining the threshold voltage from $\sqrt{I_d}$ vs. V_g plot. Overall, the model with R^2 and R^2_{adj} values close to 100% provides a good fit for optimisation purposes.

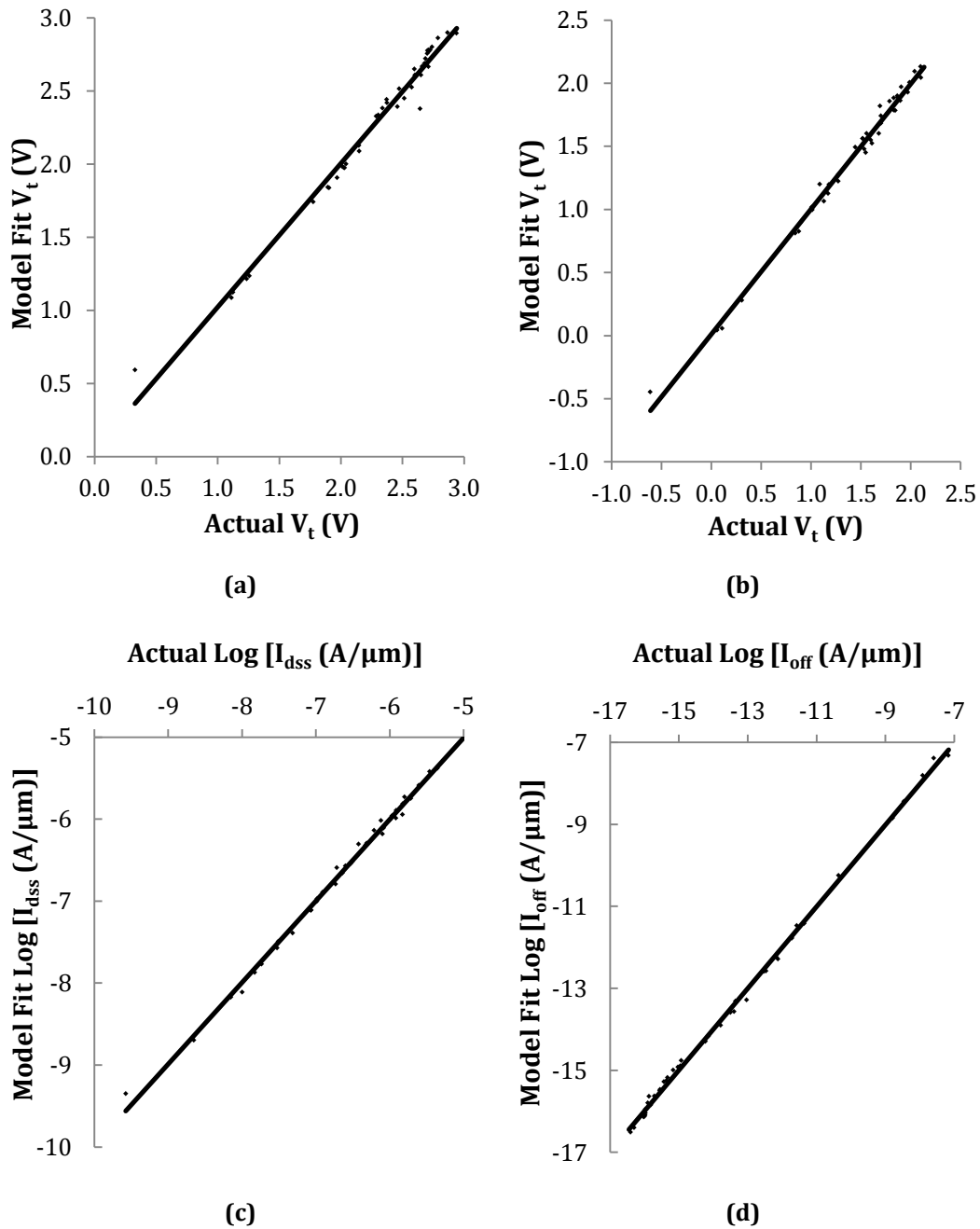


Figure 3.14. RS model fit vs. actual data for n-JFET device responses (a) V_t at 27 °C, (b) V_t at 500 °C, (c) I_{dss} at 500°C and (d) I_{off} at 500°C.

Optimisation Results

Next, the optimisation of process parameters for optimum device design is conducted with the aid of *response optimiser* in Minitab. Based on the objectives of design optimisation, which were discussed in the methodology section, the goals for the *response optimiser* were initialised. These optimisation goals are given in Table 3.7.

Response	Goal	Lower Value	Target	Higher Value
V_t (V)(27 °C)	Minimise	-	1.5	1.8
V_t (V)(500 °C)	Maximise	0.1	0.5	-
Log [I_{dss} (A/ μ m)] (500 °C)	Maximise	-6	-5.5	-
Log [I_{off} (A/ μ m)] (500 °C)	Minimise	-	-10	-9

Table 3.7. Response Optimiser goals to assist in achieving device optimisation objectives.

The results from the response optimiser comprised a number of solutions. Here solution refers to a set of proposed optimum value of the *responses*. The adequacy of each of these solutions is checked using RS plots and further verified by the use of regression tool in Minitab [70], discussed later in this section. This is to ascertain that the solution does not lie at the corner or at a steep slope on the response surface, which are highly susceptible to variability issues and, therefore, not appropriate for manufacturability.

Figure 3.15 indicates the optimised value of the process parameters (in red text). The corresponding *response* value (y), along with its desirability value (d), is given in the first column. The desirability value indicates the proximity of the *response* value to the desired/targeted value given in Table 3.7. The composite desirability (D) value indicates the overall desirability of all *responses*. In this experiment, a slightly lower value of composite desirability (0.92) is a good compromise over solutions which have a composite desirability of 1, but lie on a steep slope, towards the edge of RS plots, discussed ahead, and hence are greatly vulnerable to process variability. It is observed⁶ from the trends shown in Figure 3.15 that the channel length, L , has an insignificant effect on the threshold voltage and, therefore, can be ignored in further analysis. Two of the most influential parameters are the gate implant depth, t_g , (or, in other words, the channel thickness, t_c , for an epitaxial gated device and can be considered as

⁶ For variations in L , the *response* graphs are almost constant along the *response* value y , indicating little effect of L on the *response*. In comparison to the other four *factors*, this is also true for the composite desirability *response* graph which shows a significantly lesser variation in D , due to variations in L .

$t_c = 0.5 - t_g$, refer to Figure 3.12) and the channel doping concentration, N_d . The effects of these two parameters on the *responses* are discussed next.

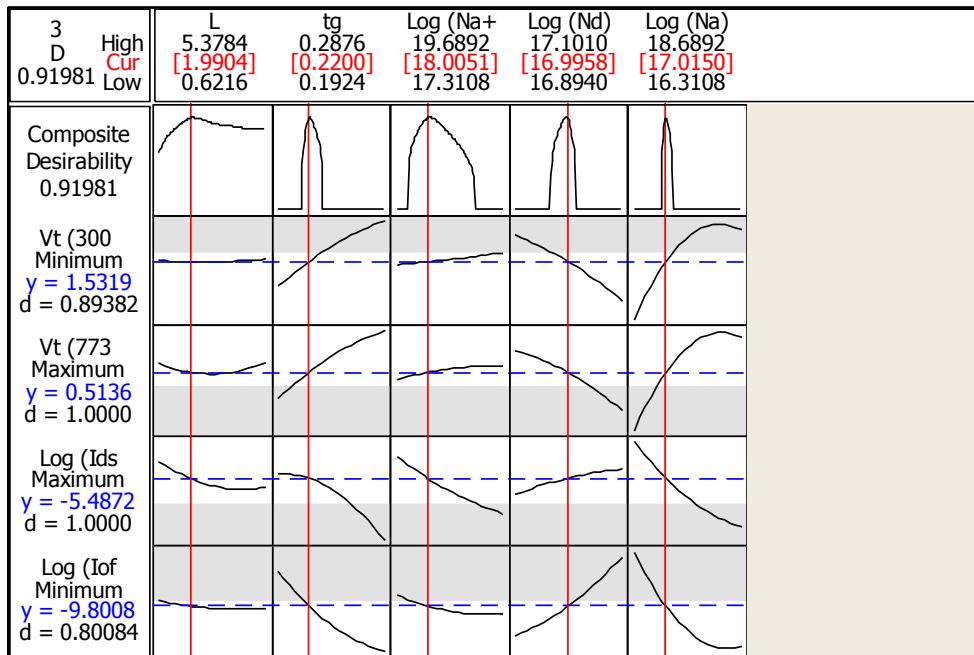


Figure 3.15. Output from *Response Optimiser* illustrating optimum values of factors (in Red text) to achieve the set optimisation objectives. The corresponding response value (y), along with its desirability value (d), is given in the first column. The overall desirability of all responses is given as composite desirability (D).

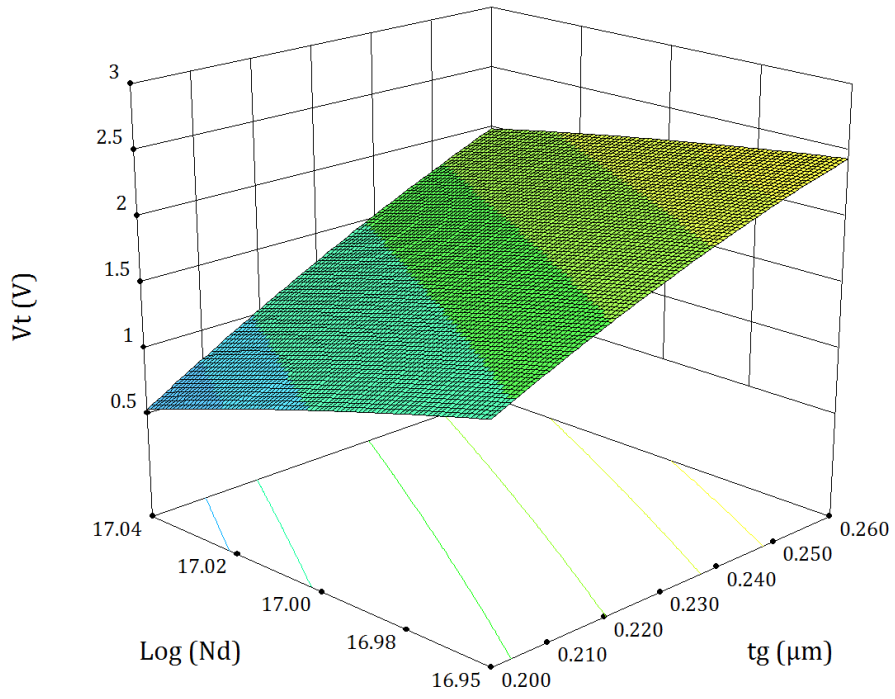
Based on the RS model equations and to verify the optimum solution, RS plots are generated for all responses as a function of the process parameters. Figures 3.16, and 3.17 show RS plots for V_t , I_{dss} and I_{off} , respectively, with respect to t_g and N_D . The other parameters are kept constant at their optimised values, $L = 2 \mu\text{m}$, $N_{A^+} = 1 \times 10^{18} \text{ cm}^{-3}$ and $N_A = 1 \times 10^{17} \text{ cm}^{-3}$. The plots indicate a close to centre value of V_t (1.49 V at 27 °C which reduces to 0.47 V at 500 °C), $\log [I_{dss} (\text{A}/\mu\text{m})] = -5.47$ at 500 °C and $\log [I_{off} (\text{A}/\mu\text{m})] = -9.60$ at 500 °C, at $t_g = 0.22 \mu\text{m}$ and $N_D = 1 \times 10^{17} \text{ cm}^{-3}$. Overall, the responses lie close to the centre of RS plots, away from steep slopes. However, the RS plots are generally tilted at an angle, especially that of I_{off} shown in Figure 3.17 (b). This indicates that the responses will suffer from unavoidable variations due to process variability, especially those responses which are located away from the centre and at steep slope on the RS plot. These response variations are inevitable, especially when high temperatures are involved.

A Regression tool is then used for further verification of optimised parameters. This tool provides, for a given set of parameter values, the fitted value of the *response*, along with the standard error in the fitted value (SE Fit) and the range (95% confidence interval $\approx 2 \times$ SE Fit, depending on sample size) in which the fitted value is expected to fall. The smaller the standard error, the more precise is the estimated *response*. The results from the regression tool for the optimised values of L , t_g , N_{A^+} , N_D and N_A are shown in Table 3.8. The small value of standard error clearly indicates a minute variation in the fitted value of all *responses*. Hence, the *responses* are likely to fall, with 95% confidence, in the desired range chosen for optimisation, given in Table 3.7.

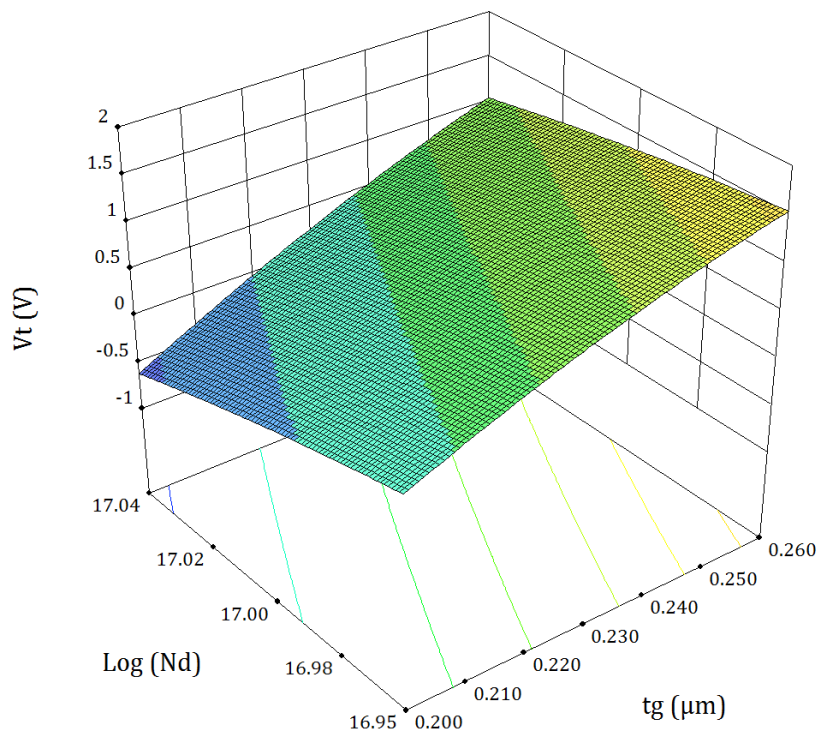
Response	SE Fit	95% Confidence Interval
V_t (V)(27 °C)	0.0952	1.4153, 1.8010
V_t (V)(500 °C)	0.1117	0.3793, 0.8320
Log [I_{dss} (A/ μ m)] (500 °C)	0.1217	-5.5422, -5.0489
Log [I_{off} (A/ μ m)] (500 °C)	0.3720	-10.973, -9.467

Table 3.8. Results from Regression tool illustrating low standard error in fitted values and desired *response* values within the 95% confidence interval.

To conclude the optimisation study, the optimised parameter values are least susceptible to *response* variations due to process variability, as compared to other possible solutions proposed by the response optimiser. The effect of random variations of these process parameters at both device and circuit level is discussed in detail in chapter 5. Furthermore, the addition of the fourth, back-gate, terminal in the lateral JFET design provides a back door to tackle such process variations and is discussed in detail in section 3.4.5. With the optimised parameters, the design of four terminal enhancement mode lateral JFETs shows great feasibility for the manufacturability of low power, high performance CJFET Logic for operation in extreme environments.

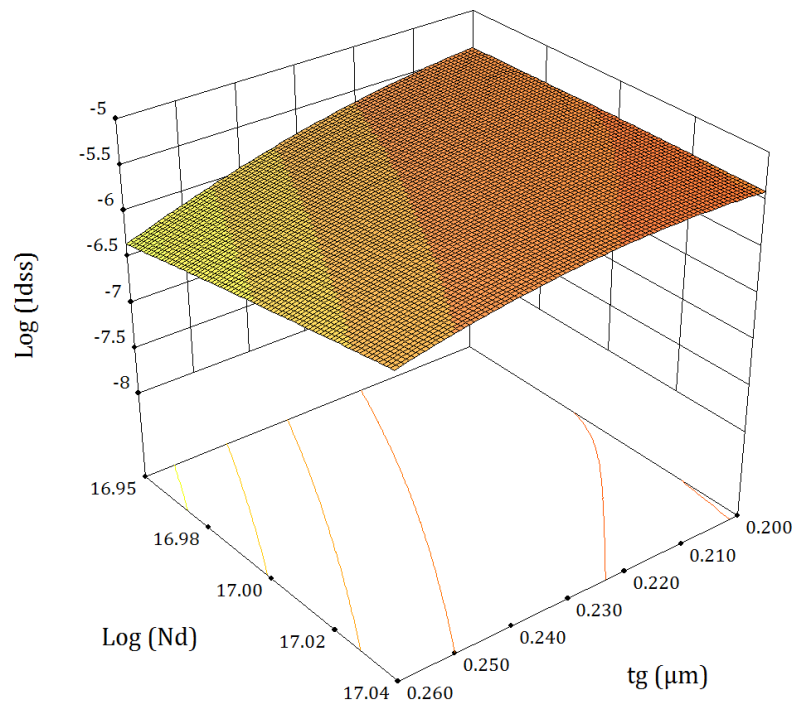


(a)

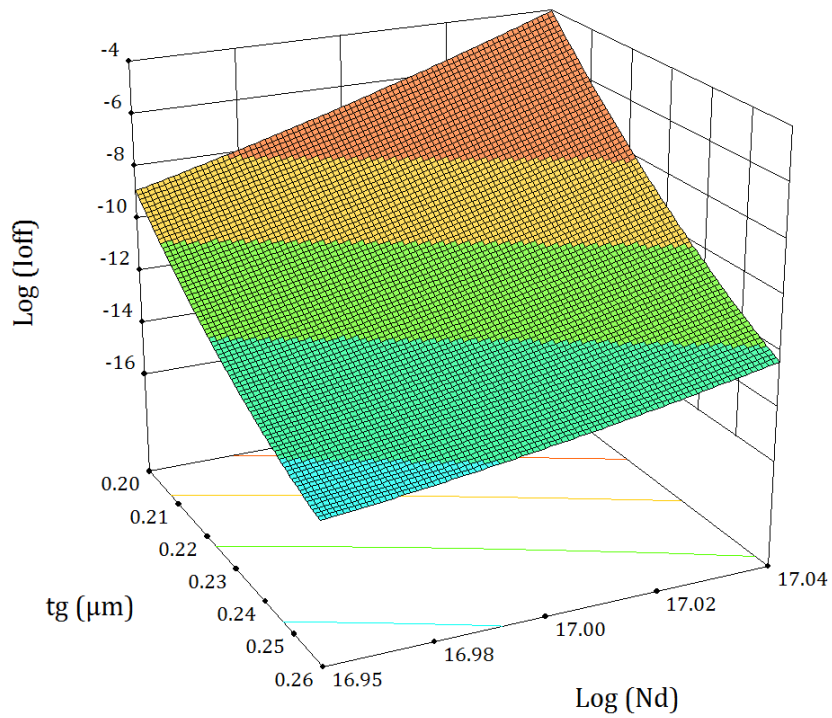


(b)

Figure. 3.16. RS plots for V_t as a function of gate implant depth and channel doping concentration at (a) 27 °C and (b) 500 °C.



(a)



(b)

Figure 3.17. RS plots for (a) I_{dss} and (b) I_{off} as a function of gate implant depth and channel doping concentration at 500 °C.

In the next sections, the electrical characteristics of n- and p-JFETs for the optimised design are presented, along with the comparison of important device characteristics with comparable structures in literature. It is also worth noting that the n-JFET optimised parameter values, but with opposite doping profile, are used for p-JFET to meet the CJFET requirements of both n- and p-JFET having similar input-output characteristics.

3.4.4 Results and Discussion

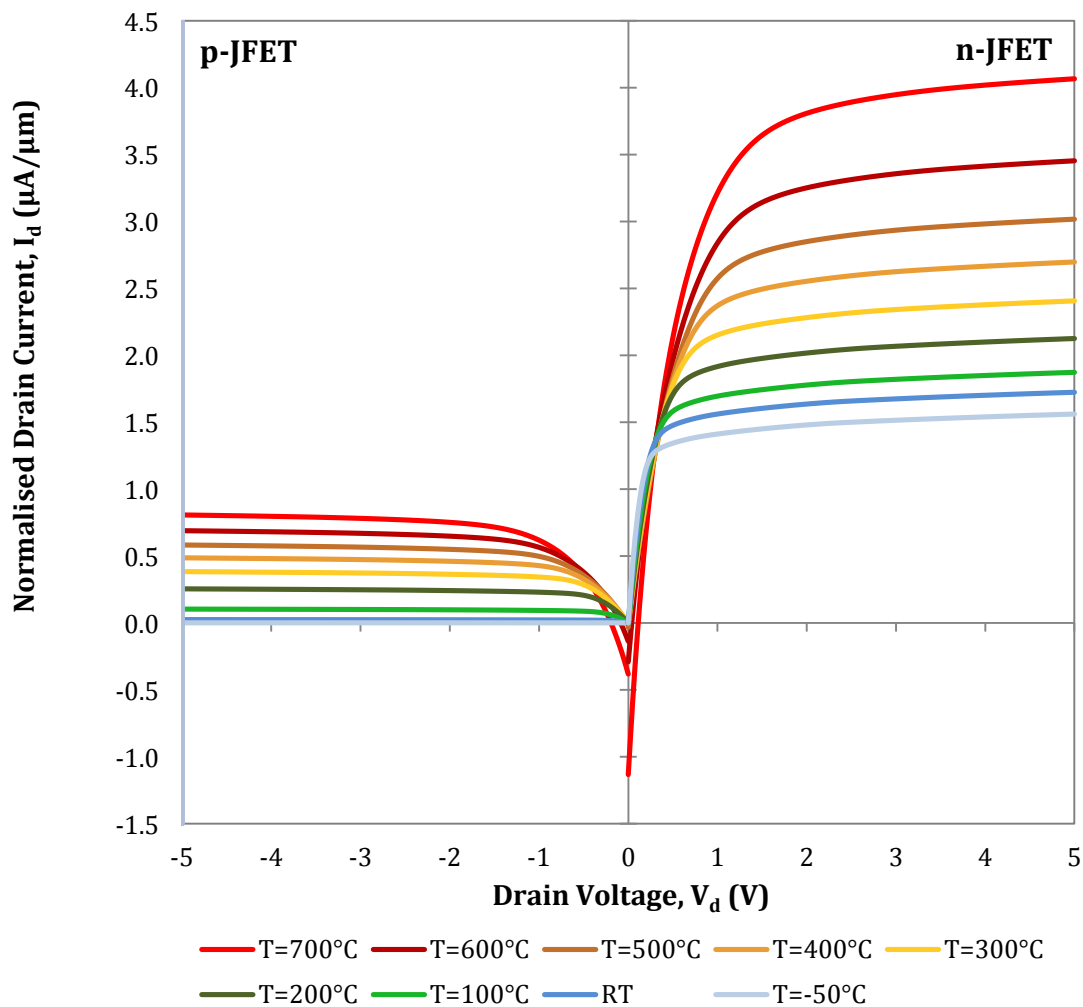


Figure 3.18. Normalised drain current-voltage, I_d - V_d , characteristics of 4H-SiC lateral n- and p-JFETs at high temperature. (For n-JFET: $V_g = 2$ V and $V_{sub} = -2$ V; p-JFET: $V_g = -2$ V and $V_{sub} = 2$ V)

This section presents the electrical characteristics of enhancement mode lateral n- and p-JFETs at high temperatures. Both n- and p-channel devices are designed

to have the same optimised process parameter values from the previous section, with the only exception in the doping profile for the p-JFET being equal and opposite to that of the n- JFET. Table 3.9 summarises the optimum parameters value for n- and p-JFETs.

Process Parameters n-JFET (or p-JFET)	Units	n-JFET	p-JFET
Gate Length, L	μm	2.0	2.0
Gate Implant Depth, t_g	μm	0.22	0.22
Gate Implant Doping, N_{A^+} (or N_{D^+})	cm^{-3}	1.0×10^{18} (Al)	1.0×10^{18} (N)
Channel Doping, N_D (or N_A)	cm^{-3}	1.0×10^{17} (N)	1.0×10^{17} (Al)
Back Gate Doping, N_A (or N_D)	cm^{-3}	1.0×10^{17} (Al)	1.0×10^{17} (N)

Table 3.9. Optimised process parameters of enhancement mode 4H-SiC lateral n- and p-JFETs for CJFET technology.

The high temperature I_d - V_d characteristics of 4H-SiC enhancement mode n- and p-channel lateral JFETs with optimised design parameters is presented in Figure 3.18. The gate leakage current, indicated by negative I_d at $V_d = 0$ V, in both devices tends to increase at temperatures beyond 600 °C. This increase in gate leakage current is mainly associated with the built-in potential, V_{bi} , of the forward biased p-n junction, i.e. the gate of an enhancement mode JFET. The gate V_{bi} decreases with the increase in temperature. At 600 °C, V_{bi} is (≈ 2.16 V, calculated using equation 3.8) close to the applied gate bias ($|V_g|$) of 2 V. The forward gate bias lowers the potential barrier between the conduction and valence bands of the p-n junction and, consequently, gives rise to the transport of carriers through the junction. This leads to the increase in, unwanted, gate drift-current, also known as gate leakage.

Most SiC JFETs [34, 44-47] have been designed so that the drain saturation current decreases with carrier mobility at high temperatures. The low values of drain saturation current greatly reduce the performance of these devices, and resultant circuits, at high temperatures. In contrast, the drain saturation current

of the optimised JFETs increase with temperature. This is achieved by the choice of the optimal point or, in other words, the optimal gate bias, $|V_g|= 2 \text{ V}$. Figure 3.19 depicts the $\sqrt{I_d}\text{-}V_g$ characteristics of n-JFET and highlights the optimal point, where the drain saturation current increases with temperature. The main advantages of having high drain saturation current at high temperatures are high on-to-off state current-ratio, required for low power logic circuitry, and fast switching.

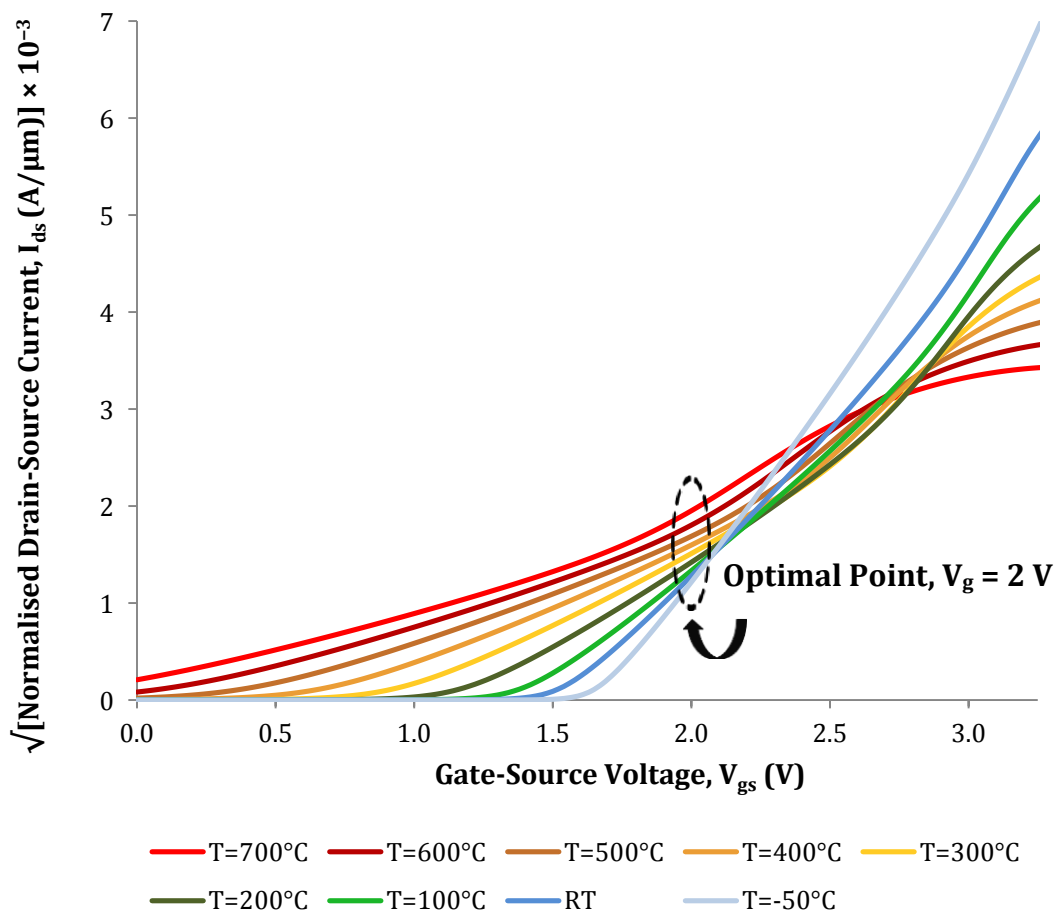


Figure 3.19. Transfer characteristics of enhancement mode n-JFET, emphasising optimal gate bias, V_g , for high performance logic circuits at high temperatures. ($V_d = 2 \text{ V}$ and $V_{sub} = -2 \text{ V}$).

In this study, the drain-source breakdown voltage was not simulated. This is because, unlike some of the previous works on high power SiC devices [71-73], the optimised devices in this study are intended for use in low power (supply voltages $\leq 2 \text{ V}$) complementary logic circuitry.

Apart from the usual three terminals (source, gate and drain), the optimised JFETs have a fourth, back-gate, terminal. Varying the biasing on this terminal changes the depletion width in the channel and hence, with a single structure, both enhancement and depletion mode operations are possible. However, in this work, the back-gate is used to control the effects of process variability on device performance parameters, such as threshold voltage, V_t , drain saturation or on current, I_{dss} , and channel leakage or off current, I_{off} . The effect of varying back-gate bias, V_{sub} , on these device parameters is discussed in the following section.

3.4.5 Optimum Back-Gate Bias (V_{sub})

The p-type (or n-type for p-JFET) gate regions in an n-JFET control the flow of current between the source and drain contacts (Figure 3.12). The current flow between the top and back gates is controlled by the depletion regions formed by the p-n junctions of the gates, each of width W_d . Applying Poisson's equation, W_d is given by

$$W_d = \sqrt{\frac{2\epsilon_s(N_A + N_D)(V_{bi} - V_i)}{q(N_A N_D)}} \quad (3.24)$$

where V_{bi} is the built-in potential, given by equation 3.8, and V_i is the applied gate bias. For the top gate, $V_i = V_g$ and for the back-gate, $V_i = V_{sub}$.

The effect of varying V_{sub} on device parameters is discussed next. Here, the main objective of varying V_{sub} is to provide an external correction mechanism to counteract effects of process (*inter* and *intra-die*) variations on device parameters. The top gate bias, $|V_g| = 2$ V, and drain bias, $|V_d| = 2$ V, are kept constant in all cases.

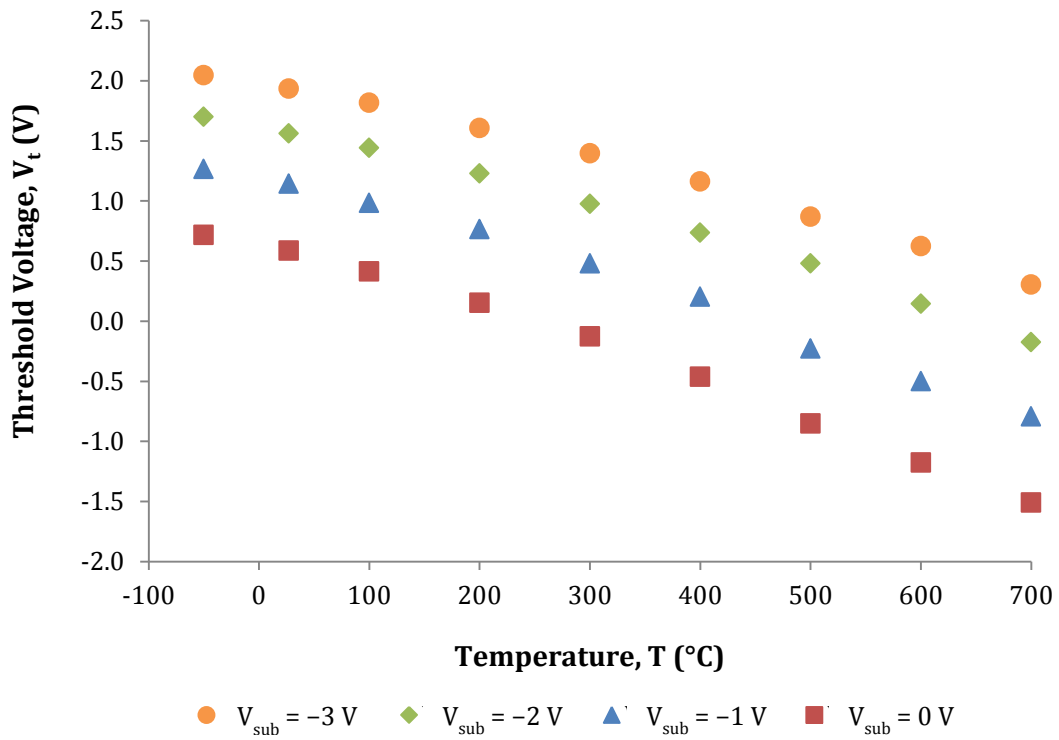
Threshold Voltage

The threshold voltage of an enhancement mode JFET is defined as the minimum applied gate bias which enhances the channel, guarded by the gate, by reducing

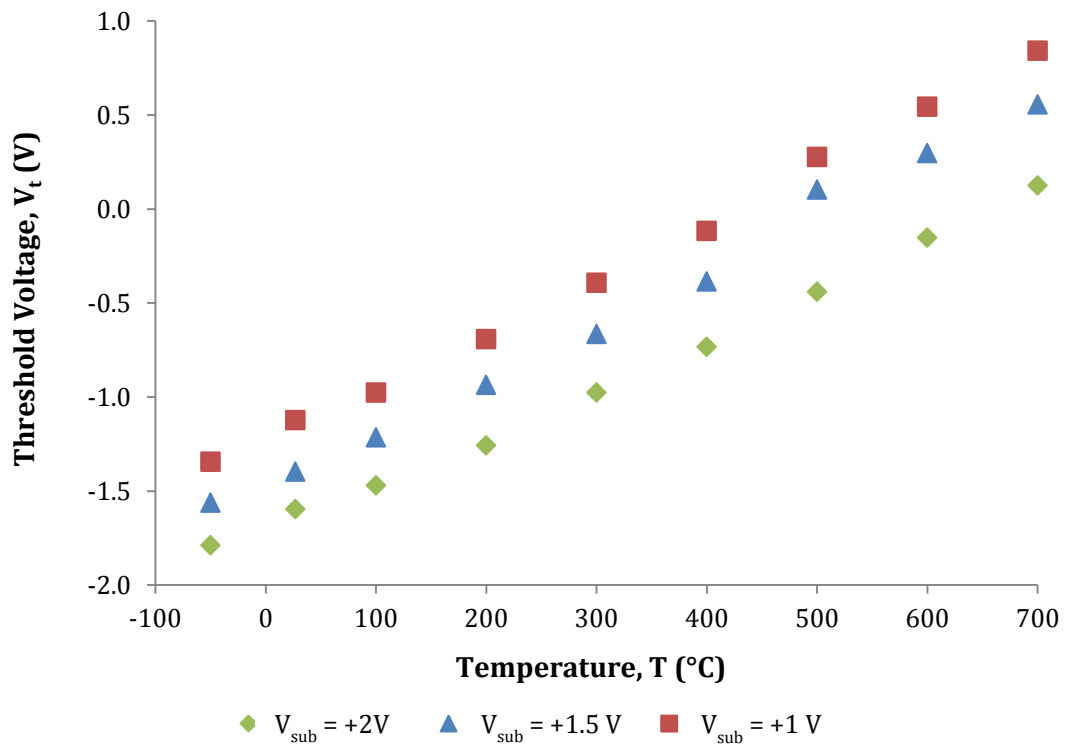
the depletion width of the gate p-n junction. For enhancement mode JFETs, V_t is positive for n-JFET and negative for p-JFET. Figure 3.20 shows the variation of threshold voltage with back-gate bias, V_{sub} across a range of temperatures.

The threshold voltage (V_t) decreases with temperature. This is because as the temperature increases, the excess energy gained by carriers is sufficient to ionise the remaining dopant atoms and to transport the resultant electrons and holes to the conduction and valence bands, respectively. The rise in carrier concentration in the conduction and valence bands reduces the built-in potential of the gate channel junction. Consequently, W_d limiting the channel current goes down, giving rise to the drift current through the channel and, hence, lowers the threshold voltage.

It is apparent from Figure 3.20 (a) and (b) that the magnitudes of V_t for both n- and p-JFET are similar for corresponding values of V_{sub} , at all temperatures. This similarity of V_t for n- and p-JFET is the most crucial requirement of complementary JFET logic. At the optimal point, $|V_d| = |V_g| = |V_{sub}| = 2$ V, the threshold voltage is negative at temperatures over 600 °C and the device no longer counts as an enhancement mode device. At $|V_g| = 2$ V, increasing the back-gate bias, $|V_{sub}|$, from the optimal point increases the depletion width in the channel (Equation 3.24) and, hence, increases the threshold voltage. Similarly, decreasing the back-gate bias, $|V_{sub}|$, from the optimal point decreases the threshold voltage. This shows that the back-gate can be used as an external contact to tackle any variations in the threshold voltage from its optimal value.



(a)

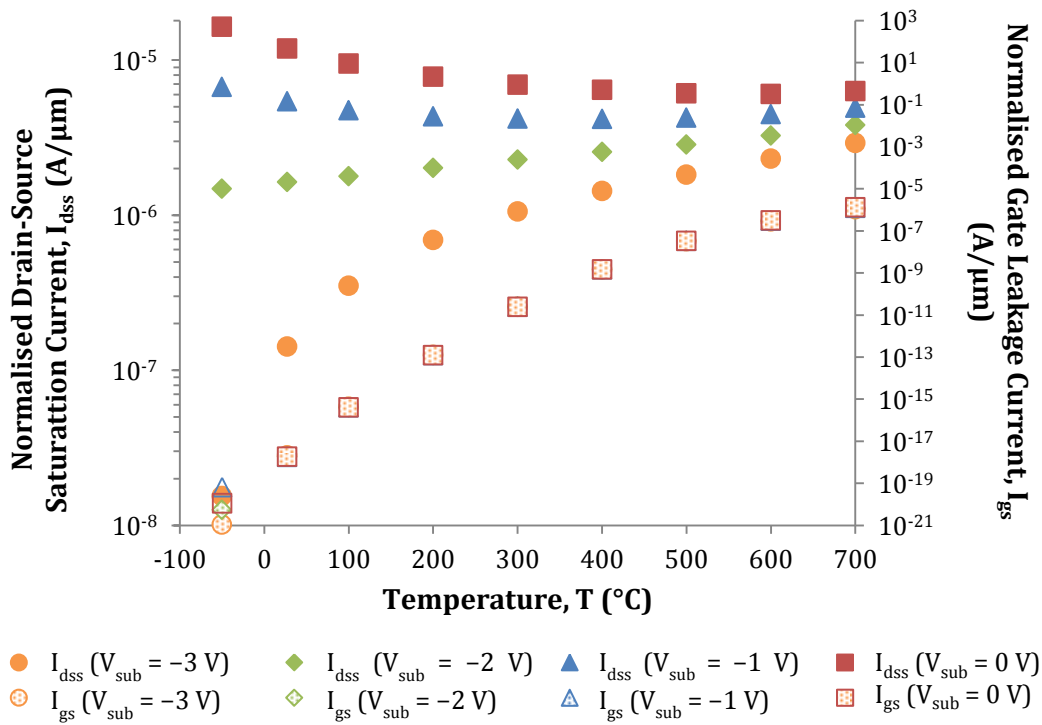


(b)

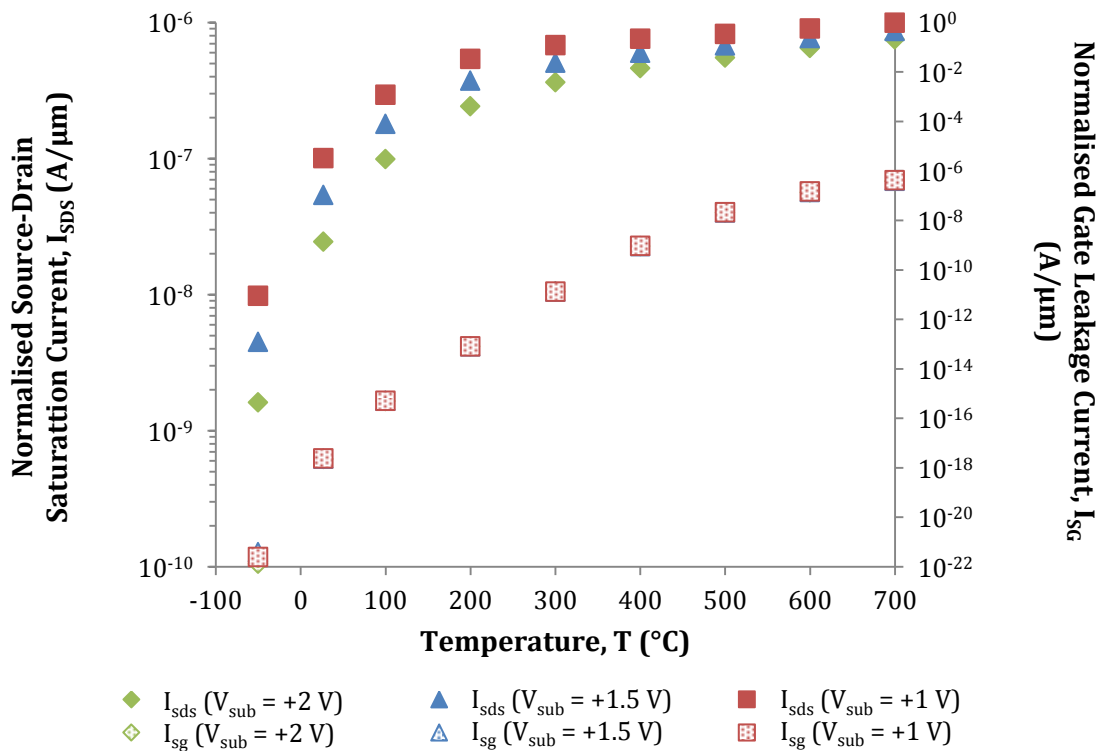
Figure 3.20. Variation of threshold voltage, V_t , with back-gate bias, V_{sub} , at high temperatures (a) n-JFET: $V_g = V_d = 2\text{ V}$ and (b) p-JFET: $V_g = V_d = -2\text{ V}$.

Drain Saturation and Gate Leakage Currents

The drain saturation current for enhancement mode JFETs is the maximum drain current at a particular drain and gate bias. The gate leakage current, on the other hand, is the gate current at zero drain bias and is due to the forward biased gate of the enhancement mode JFET. Both drain saturation and leakage currents for optimal biasing point have been discussed in the previous section. Figure 3.21 (a) and (b) shows the variation in the drain saturation and gate leakage currents of n- and p-JFETs, respectively, with applied back-gate bias, across a range of temperatures. The currents considered here are, normalised, for device with a unit channel width in the z-direction. As expected, the gate leakage current is independent of V_{sub} . However, the drain saturation current is linked to V_{sub} through the depletion region controlled by the back-gate, Equation 3.24. Similar to controlling threshold voltage, high values of $|V_{\text{sub}}|$ increases the depletion width in the channel, resulting in lower drain current through the channel and vice versa.



(a)

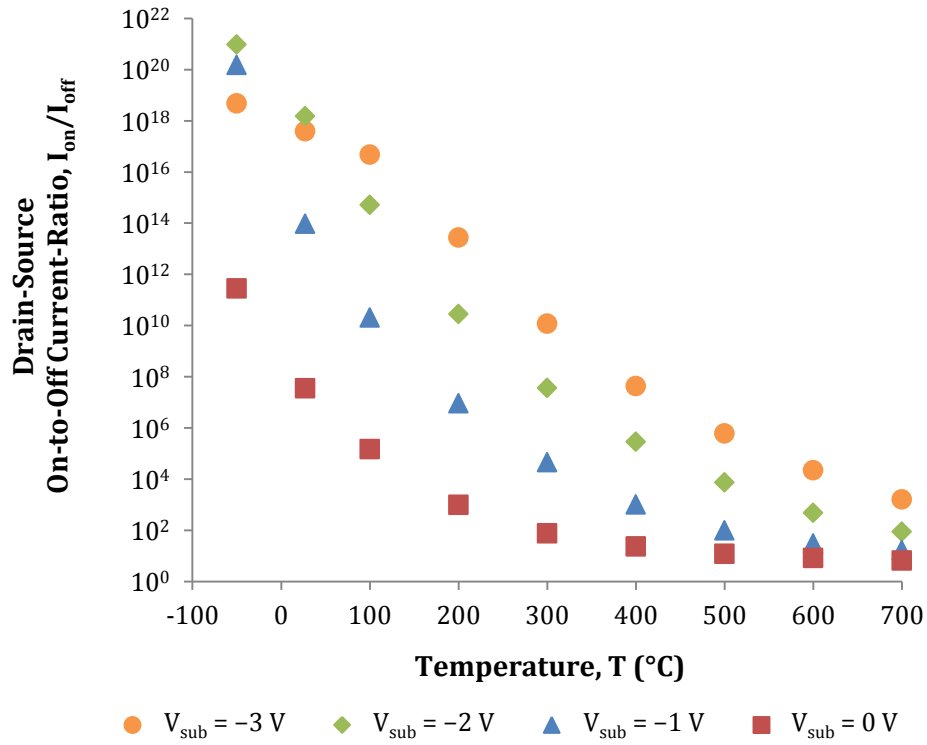


(b)

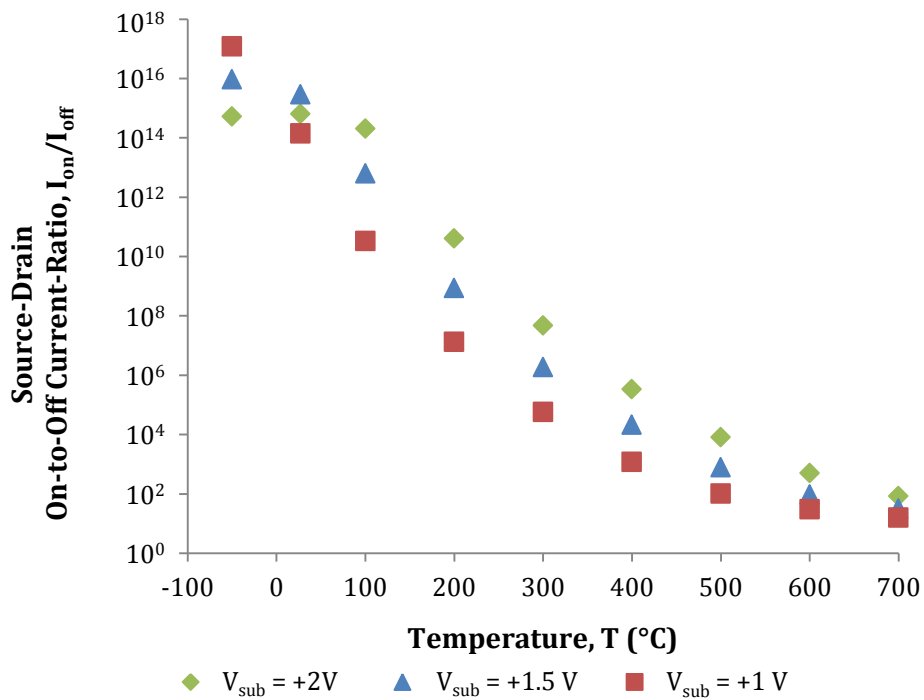
Figure 3.21. Variation of normalised drain saturation current (at $V_d = |2| \text{ V}$) and normalised gate leakage current (at $V_d = 0 \text{ V}$), with back-gate bias, V_{sub} , at high temperatures (a) n-JFET: $V_g = 2 \text{ V}$ and (b) p-JFET: $V_g = -2 \text{ V}$.

Drain On-to-Off Current-Ratio

The variation of drain on-to-off current-ratio for n- and p-JFETs is depicted in Figure 3.22 (a) and (b), respectively. Here, the on-current is the drain saturation current at $|V_g| = |V_d| = 2$ V and the off-current is the channel leakage current, at $V_g = 0$ V and $|V_d| = 2$ V. The on-to-off state current-ratio is an important device parameter for low power complementary logic devices with high noise margin and fast switching at high temperatures. High values of channel leakage current mean the device does not switch off completely and, consequently, leads to excess power dissipation through the device when it is supposed to be off. Like on-state current, discussed in the previous section, the off-state current is linked to V_{sub} through the depletion region controlled by the back-gate, Equation 3.24. At the optimal point, $|V_d| = |V_g| = |V_{sub}| = 2$ V, the on-to-off state current-ratio ranges from 9.46×10^{20} to 87.5 for n-JFET and from 5.21×10^{14} to 84.4 for p-JFET, for a temperature range between -50 to 700 °C, respectively. The on-to-off state current-ratio at high temperatures is mainly contributed to by the channel leakage current. High values of $|V_{sub}|$ decrease the channel leakage current by increasing the depletion width across the channel, hence, giving rise to the on-to-off state current-ratio at high temperatures. Similarly, values of $|V_{sub}|$ lower than the optimal point reduce the depletion width across the channel and, as a result, give rise to a large channel leakage current. This rise in channel leakage reduces the on-to-off state current-ratio at high temperatures.



(a)



(b)

Figure 3.22. Variation of drain on ($|V_g| = 2\text{ V}$) to off ($V_g = 0\text{ V}$) current-ratio, I_{on}/I_{off} , with back-gate bias, V_{sub} , at high temperatures (a) n-JFET: $V_d = 2\text{ V}$ and (b) p-JFET: $V_d = -2\text{ V}$.

3.4.6 Comparison of Optimised JFET with Similar Structures

To conclude, a comparison of critical device parameters is made with those published in the literature for comparable structures [47]. It is apparent from Table 3.10 that the optimised device has a much lower threshold voltage, V_t , (required for low power), a higher transconductance, g_m , (required for high gain) and a higher ratio of on-to-off state drain-source current, I_{on}/I_{off} , (required for low power, high noise margin and fast switching) at 500 °C. A lower value of I_{dss} and higher R_{on} than those reported in [47] is due to the fact that the optimised device is characterised at $V_d = 2$ V, as compared to $V_d = 20$ V.

Device	I_{dss} (mA)	V_t (V)	g_m (μ S)	R_{on} (K Ω)	I_{on}/I_{off}
Optimised n-JFET	0.57	0.48	928	9.31	7.4×10^3
n-JFET [47]	1.36	-11.8	214	4.64	36.8

Table 3.10. Comparison of optimised n-JFET characteristics with published results [47] for 200 μ m wide devices at 500 °C.

3.5 Chapter Summary

This chapter reports the first comprehensive study, to the author's knowledge, on the development and validation of 4H-SiC model parameters for high temperature, low power FE TCAD simulations. The model parameters were based on the physical and material properties of 4H-SiC and their values were extracted using published material data. The validation of these model parameters were performed using high temperature 4H-SiC lateral JFET data, fabricated and characterised at Newcastle University. The simulated result showed excellent agreement with the measured data.

Using DoE and RSM statistical techniques, within the TCAD framework, a new systematic methodology was devised for optimisation of four-terminal, enhancement mode 4H-SiC JFETs for low power logic devices. The methodology

included optimisation of bias potentials and process parameters, such that the optimal device is least susceptible to process variability and can function across a wide temperature range using the same set of gate and drain biases. Five key process parameters (*factors*), namely: gate length, gate implant depth, gate implant doping, channel doping, and back-gate doping, were varied within specified ranges. The corresponding device performance metrics (*responses*), namely: threshold voltage, drain saturation current and drain leakage current, were modelled and analysed using RSM. With the aid of standard process optimisation tool (*response optimiser*) and RS plots, the process parameters for enhancement mode 4H-SiC JFETs were optimised for operation in extreme environments.

Unlike previously reported devices, the optimised SiC JFETs were designed such that not only the gate length was reduced to 2 μm (in contrast to the 10 μm reported elsewhere), but were also able to operate over a wide temperature range of $-50\text{ }^{\circ}\text{C}$ to $600\text{ }^{\circ}\text{C}$ on a fixed voltage of 2 V, in contrast to the 20 V used in other work. Furthermore, the drain saturation current of the optimised JFETs were shown to increase with temperature which allowed high on-to-off state current-ratio ($I_{\text{on}}/I_{\text{off}}$) at elevated temperatures. High $I_{\text{on}}/I_{\text{off}}$ is essential for low power logic circuitry with faster switching. At $500\text{ }^{\circ}\text{C}$, $I_{\text{on}}/I_{\text{off}} \sim 10^3$ for optimised JFET as opposed to $< 10^2$ for n-JFET fabricated by Neudeck *et al.* This was achieved by the choice of optimal gate bias, $|V_{\text{g}}| = 2\text{ V}$.

Finally, the role of back-gate bias in the optimised JFET structure as a means to control process variability was examined. The effect of varying back-gate bias (V_{sub}) on the n- and p-JFET performance parameters, threshold voltage (V_{t}), drain saturation current (I_{dss}) and channel leakage current (I_{off}), were studied in detail. It was shown that by adjusting the back-gate biasing, the variation in device performance parameters could be controlled. Hence, V_{sub} provides a back door to tackle post fabrication fluctuations in device performance parameters, most importantly, without needing to adjust the top gate biasing.

3.6 References

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Chapter 4. Complementary JFET Inverter

4.1 Introduction

In the previous chapter, 4H-SiC (normally off) n- and p-JFETs were optimised for operation in extreme environments, where conventional Si and strained Si based devices cease to operate. Unlike previously reported devices [1-7], the optimised SiC JFETs are designed such that not only the gate length is reduced to 2 μ m (in contrast to the 10 μ m reported elsewhere), but are also able to operate over a temperature range of -50 °C to 600 °C on a fixed voltage of 2V, in contrast to the 20 V used in other work. These features will enable SiC logic circuitry to operate in a wide variety of hostile environments (including applications in aerospace, automotive, energy production and other industrial systems [8]) and achieve a higher performance with reduced power dissipation in comparison with previous structures.

Here, for the first time (to the author's knowledge), logic circuitry based on 4H-SiC CJFET technology is described. Like CMOS, CJFET based logic gates require both enhancement mode n- and p-JFETs for operation. Because of the wide bandgap of SiC, normally off (enhancement mode) JFETs are a realistic proposition. In Si technology, because of the low built in potential of the p-n junction, enhancement mode devices suffered from a high on state resistance and this prevented research in CJFET technology until recently [9]. The advantages of JFET over MOSFETs, MESFETs and BJTs for operation in extreme environments, along with the operation of CJFET logic inverter, were discussed in Sections 2.2 and 2.3, respectively.

In order to assess the potential improvements in performance of digital logic functions as a result of using CJFET technology in their implementation, the static and dynamic characteristics of the most basic logic element, namely the inverter

are analysed. The logic inverter is truly the core of all digital designs. The design and analysis of an inverter enables the design of more complex structures, such as NAND, NOR and XOR gates. These complex structures in turn form the building blocks for modules, such as adders, multipliers and microprocessors.

The CJFET logic inverter is analysed with respect to the following design metrics:

- *Integrity and robustness* – described by the static (or steady state) characteristics.
- *Performance* – determined by the dynamic (or transient) response.
- *Energy efficiency* – controlled by the energy and power consumption.

These are successively discussed in detail in Sections 4.2 to 4.4. This chapter also explores the possibility of performance enhancements in 4H-SiC CJFET logic at high temperatures, in terms of reduced power dissipation with enhanced switching speed. In silicon technology, supply voltage reduction is commonly used to reduce active power [10]. However, this affects the noise margin of the circuit [11, 12]. In this work, emphasis is on the analyses of noise and power performance of the inverter structure and their dependence on the behaviour of individual transistors. In Section 4.5, the feasibility of SiC CJFET ICs to achieve high circuit complexities with low power consumption at 500 °C is analysed. Finally, the chapter is summarised in Section 4.6.

All the results reported in this chapter are obtained using calibrated FE simulations. The static and dynamic characteristics of 4H-SiC CJFET inverter circuits are studied as a function of temperature, supply voltage, fan-out and different rise and fall times of the gate pulse. A comparative analysis of the key parameters of SiC CJFET logic inverter with Si, strained Si and current SiC technologies is also presented.

4.2 Static Characteristics

The main attributes of interest in analysing the static characteristics of 4H-SiC CJFET circuits are the noise margins.

4.2.1 Noise Margin

Digital circuits are highly prone to unwanted voltages (noise) that can either be induced by external sources (i.e. from the surrounding environment) or internally generated at the circuit nodes, subject to the properties of transistors used in the circuit [11]. These unwanted noise signals may result in the incorrect switching of digital circuits, leading to false interpretation of important data at the output. Hence, one of the critical requirements of modern digital circuits is their immunity to noise.

Noise immunity or noise margin (NM) provides a quantitative measure of how resilient a digital circuit is to false switching. The mapping of a voltage range (input/output) for a particular logic state gives the measure of the noise margin of a digital circuit [13]. Figure 4.1 provides a graphical illustration to define and interpret noise margin. The minimum logic “1” (high) input (V_{IH}) and output (V_{OH}) voltages and the maximum logic “0” (low) input (V_{IL}) and output (V_{OL}) voltages are deduced from the DC input-output characteristics, voltage transfer curve (VTC). The VTC is discussed in detail later in this section. Between the two stable logic states, logic “1” or logic “0”, there lies an input voltage range which cannot be mapped to a particular logic level. This input range is termed as the undefined region or metastability window and can be calculated using [11]:

$$\text{Undefined Region} = V_{IH} - V_{IL} \quad (4.1)$$

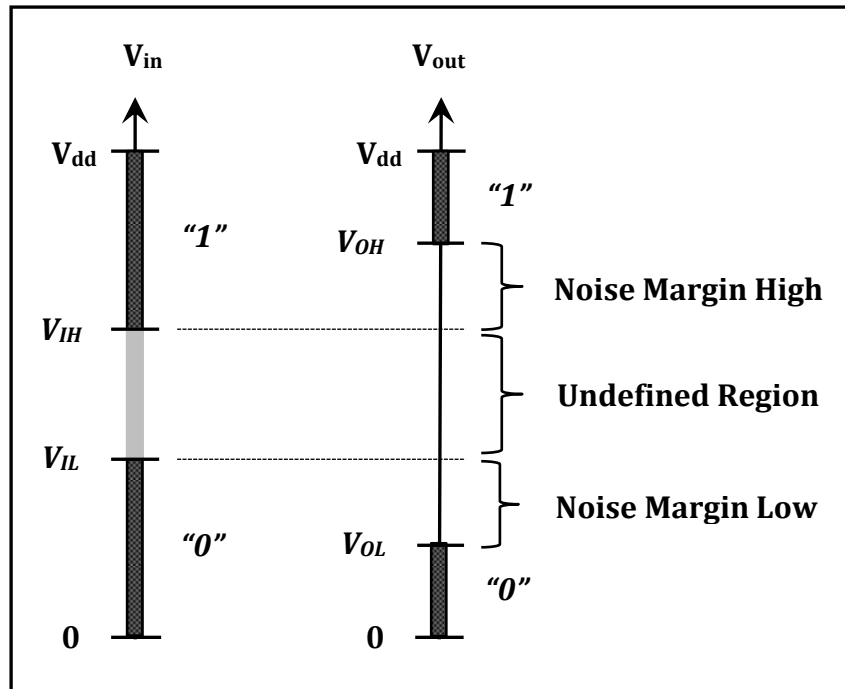


Figure 4.1. Definition of the voltage noise margin in a logic gate. V_{IL} and V_{IH} are the input low (0) and high (1) voltages, respectively. V_{OL} and V_{OH} are the output low (0) and high (1) voltages, respectively.

The noise margin is the difference between what the driver IC output sees as a valid logic voltage and what the receiver IC expects to see as a valid logic voltage. There are two different types of noise margin, one for logic high (termed as NM_H) and one for logic low (termed as NM_L). For a valid logic high, the worst case noise margin for the circuit is the minimum high level voltage output from the driver minus the minimum high level voltage seen at the receiver IC [11]. Therefore, NM_H equals V_{OH} (driving device) minus V_{IH} (receiving device).

$$NM_H = V_{OH} - V_{IH} \quad (4.2)$$

Similarly, for a valid logic low the worst case noise margin for the circuit is the maximum low level voltage input seen at the receiver IC minus the maximum low level voltage output from the driver; i.e. NM_L equals V_{IL} (receiving device) minus V_{OL} (driving device).

$$NM_L = V_{IL} - V_{OL} \quad (4.3)$$

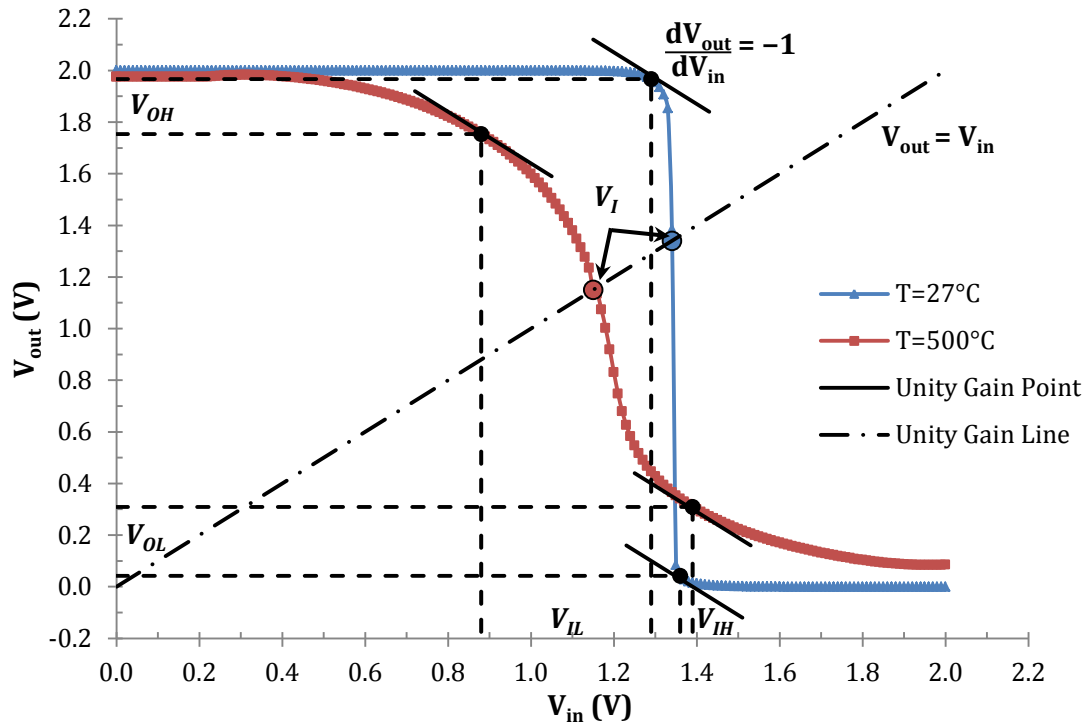


Figure 4.2. Critical voltage transfer curve (VTC) voltages of 2 μm CJFET logic inverter with an aspect ratio (W_p/W_n) of 3/1.

The voltage transfer curve graphically portrays the DC input-output characteristics of the logic gates. All the important DC circuit characteristics, such as noise tolerance, gain and operating logic levels, can be extracted from the VTC [13]. The VTC of 4H-SiC CJFET logic inverter at RT and 500 °C are shown in Figure 4.2. In order to account for higher electron mobility compared to hole mobility in 4H-SiC [14-17], the width of p-JFET used in designing CJFET inverters is taken to be three times the width of n-JFET. This ratio is used to provide a near symmetric VTC across the temperature range studied (-50 °C to 600 °C) [11, 13]. The circuit is supplied with a fixed supply voltage of $V_{dd} = 2\text{ V}$ over the entire temperature range. The common gate input voltage (V_{in}) of the complementary JFET pair is also switched between, $V_{in} = 0\text{ V}$ and $V_{in} = V_{dd}$, at all temperatures. Unlike previously reported SiC logic gates [4, 5], the ability of CJFET logic to operate at positive logic voltage levels precludes the need for level shifter circuitry and, hence, saves both area on the chip and extra power dissipation in the level shifter circuitry. From the commercial perspective, this power and size reduction feature of CJFET circuitry will greatly aid the

realisation of high temperature SiC sensing technology for monitoring hostile environments.

The VTC graph highlights the critical output (V_{OH} and V_{OL}), input (V_{IH} and V_{IL}) and inverter threshold (V_I) voltages. These voltages can be regarded as transition points between “1” and “0” logic states. The inverter threshold voltage (V_I), also known as the midpoint voltage (V_M), is defined by the point where the VTC intersects the unity gain line defined by $V_{out} = V_{in}$. V_I lies between the borders of logic low and high input voltages V_{IL} and V_{IH} . Thus, it can be interpreted that

$$V_{in} < V_I \Rightarrow \text{Input is probably a logic low}$$

and

$$V_{in} > V_I \Rightarrow \text{Input is probably a logic high}$$

However, as shown in Figure 4.1, the input is precisely labelled as *logic low* between 0 V and the maximum input low voltage (V_{IL}). Similarly, the input is precisely labelled as *logic high* between the minimum input high voltage (V_{IH}) and V_{dd} .

The values of V_{OH} , V_{OL} , V_{IH} and V_{IL} are noted from the unity gain points of VTC, i.e. where slope equals -1 , by extrapolating the points to input and output voltage axis. Subsequently, the noise margins of 4H-SiC CJFET inverter are calculated as expressed in equation 4.2 and 4.3.

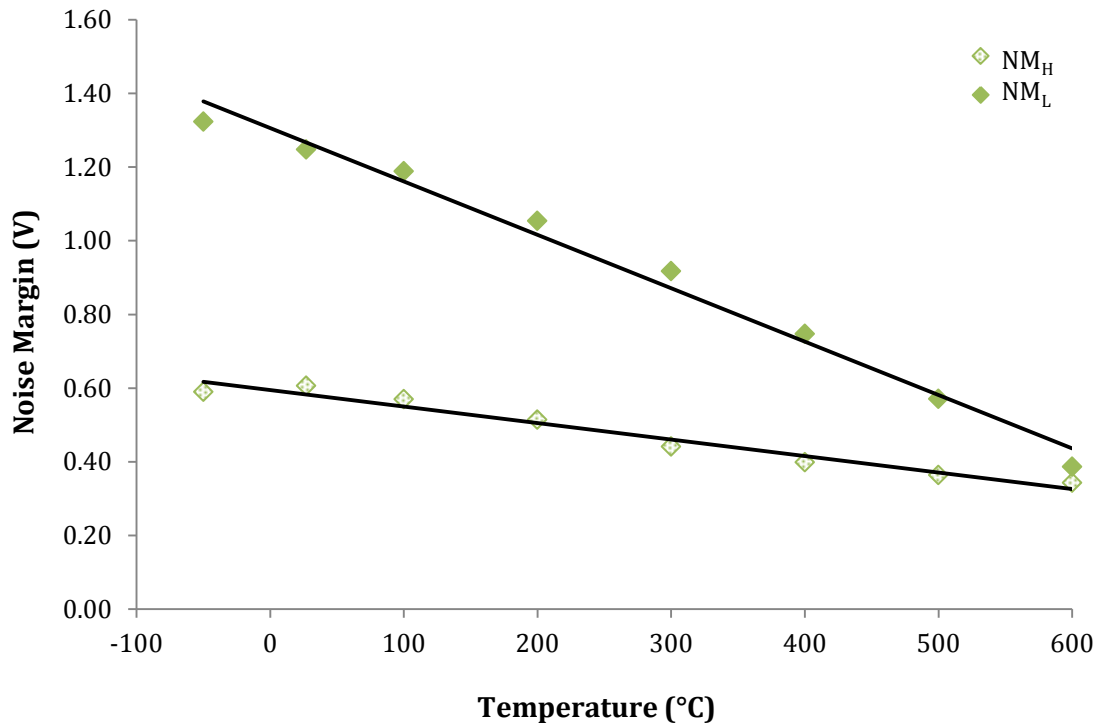


Figure 4.3. Variation of noise margin high (NM_H) and low (NM_L) with temperature at V_{dd} = 2V.

The data in Figure 4.3 show the noise margin high and noise margin low for a 4H-SiC CJFET inverter over the full temperature range studied. The data show three interesting aspects of CJFET inverter noise margins, namely:

1. NM_L is greater than NM_H
2. Both noise margins decrease with temperature
3. NM_L and NM_H converge at high temperatures

Taking into consideration the definition of low and high NM ($NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$) and by examination of the VTC data given in Figure 4.2, these three features are explained in the following paragraphs.

NM_L is greater than NM_H

From the VTC (Figure 4.2) it is apparent that at low temperatures, the output low and high voltages (V_{OL} and V_{OH}) are very close to zero and the supply voltage, respectively. Hence, they can be approximated to 0 V and V_{dd}. Substituting this in the NM equations gives $NM_L = V_{IL}$ and $NM_H = V_{dd} - V_{IH}$. Furthermore, the value

of maximum logic low input voltage⁷ $V_{IL} > V_{dd}/2$. This combined with the fact that the input high voltage (V_{IH}) is greater than the input low voltage (V_{IL}), shows that NM_L is greater than NM_H .

Both noise margins decrease with temperature

It is apparent from Figure 4.3 that noise margin decreases with temperature. This decrease in NM is related to the shift in the threshold voltage (V_t) of the n- and p-JFET devices used to create the complimentary pair. V_t decreases at high temperatures due to complete ionisation of the dopant atoms, which transport the resultant electrons and holes to conduction and valence bands, respectively. The rise of carrier concentration in conduction and valence bands reduces the built-in potential (V_{bi}) of the gate channel junction. Consequently, the width (W_d) of the depletion region limiting the channel current goes down, giving rise to the drift current through the channel and, hence, lowers the threshold voltage. This drop in threshold voltage at high temperatures increases the metastability window by decreasing V_{IL} to the left and increasing V_{IH} to the right of the VTC, causing NM to degrade at high temperatures. Furthermore, the off-state leakage current (I_{off}) also increases with temperature, because of the drop in turn on voltage resulting in the channel not being sufficiently turned off. This increase in leakage current causes a reduction in the I_{on}/I_{off} ratio which leads to the reduction in output voltage swing (V_{os}) at elevated temperatures, as shown in Figure 4.4. Consequently, with $V_{OH} < V_{dd}$ and $V_{OL} > 0$ V, the noise margins decrease at high temperatures.

NM_L and NM_H converge at high temperatures

Finally, NM_L converges with NM_H at high temperatures because V_{IL} undergoes a much bigger change as compared to V_{IH} , due to the drop in device threshold voltage (V_t). This may be attributed to the two main factors of the CJFET inverter design. First, the circuit is supplied with a fixed supply voltage of $V_{dd} = 2$ V and input voltage range of $0 \text{ V} \leq V_{in} \leq V_{dd}$, over the entire temperature range. Secondly, due to high threshold voltage values of n- and p-JFETs at low

⁷ V_{IL} and V_{IH} are directly linked to the threshold voltage of n-JFET (V_{tn}) and p-JFET (V_{tp}).

temperatures, V_{IH} is already close to V_{dd} and changes only slightly as the threshold voltage decreases at higher temperatures. On the other hand, the drop in V_t at high temperatures causes the n-JFET to switch on at a much lower input voltage (i.e. $V_{in} = V_t \sim 0.48$ V at 500 °C as compared to ~ 1.4 V at RT), resulting in a big shift in V_{IL} to the left of VTC. Hence, this dominated change in V_{IL} over V_{IH} causes NM_L to converge with NM_H at high temperatures.

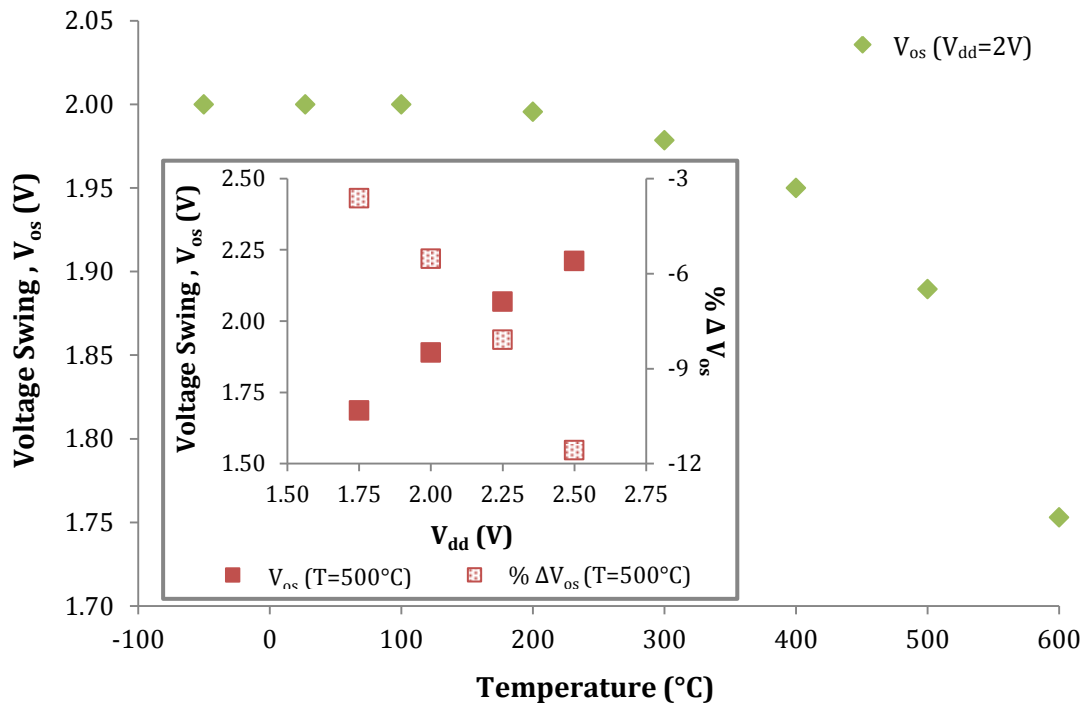


Figure 4.4. Variation of output voltage swing (V_{os}) with temperature at $V_{dd}=2V$. The Inset shows variation of V_{os} with supply voltage (V_{dd}) scaling at 500 °C.

The ideal CJFET design, like CMOS, is intended to give a full rail to rail output voltage swing which should increase with supply voltage. However, as explained previously in this section, the increase in leakage current through the channel at high temperatures degrades V_{os} . This can be observed from the data shown in the inset of Figure 4.4, which plots V_{os} and percentage change of V_{os} from its ideal value (V_{dd}) against supply voltage scaling, at 500 °C. The observed V_{os} increases with V_{dd} , but the change is lower than would be expected for a linear relationship. At $V_{dd} = 1.75$ V, the value for V_{os} is 3.6% lower than the ideal value of 1.75 V. However, this difference in V_{os} from its ideal value increases with

supply voltage and, at $V_{dd} = 2.5$ V, V_{os} is degraded significantly by 11.6%. The effect of supply voltage scaling on noise margin is discussed next.

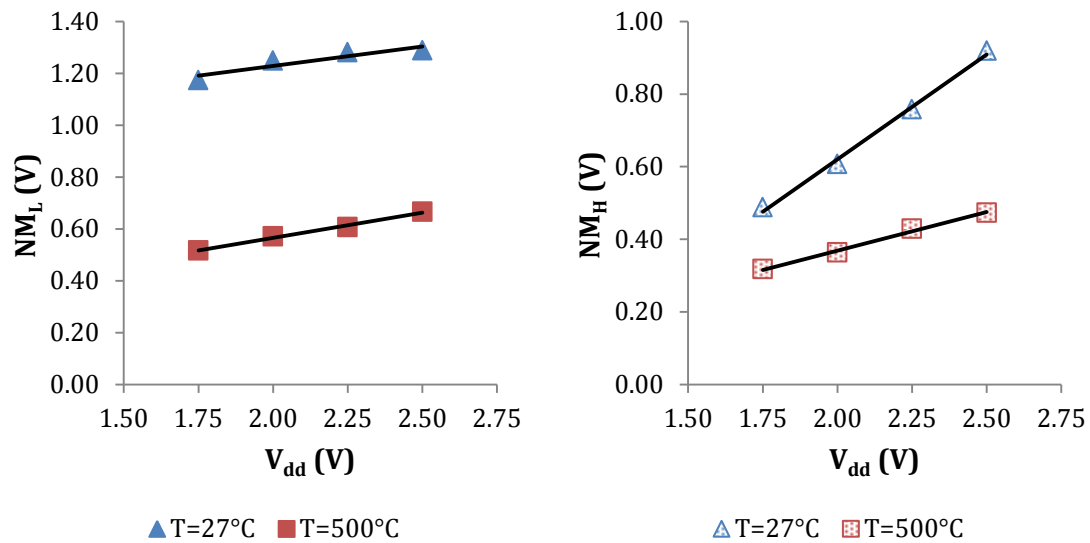


Figure 4.5. Variation of noise margin high (NM_H) and low (NM_L) with supply voltage (V_{dd}) scaling at 27°C and 500°C .

Figure 4.5 shows the variation of noise margin low (NM_L) and noise margin high (NM_H) of the CJFET inverter at both RT and 500°C , as a function of supply voltage. Both NM_L and NM_H degrade with a reduction in supply voltage as would be expected from the NM equations 4.2 and 4.3. This degradation is linked to the inverter threshold voltage (V_I) and, hence, to the input and output transition points (V_{IH} , V_{IL} , V_{OH} and V_{OL}) which scale with the supply voltage. It is also worth noting that as V_{dd} increases, the observed increase in NM_H at 500°C is not as large as would be expected from the change in NM_H at RT. This discrepancy is because the rate of increase in V_{OH} , with respect to V_{dd} , decreases at high temperatures due to the increase in leakage current through the n-channel.

For a supply voltage of 2 V, the CJFET logic inverter $NM_L = 1.25$ V and 0.57 V and $NM_H = 0.61$ V and 0.36 V, at RT and 500°C , respectively. In comparison, the conventional silicon and strained silicon based CMOS logic inverters, operating at RT and $V_{dd} = 2$ V, have $NM_L = 0.28$ V and 0.37 V and $NM_H = 0.84$ V and 0.96 V, respectively [18]. This shows that, at $V_{dd} = 2$ V, CJFET logic inverter has fairly

comparable noise margins, at high temperatures, to those of Si and strained Si CMOS inverters, operating at RT.

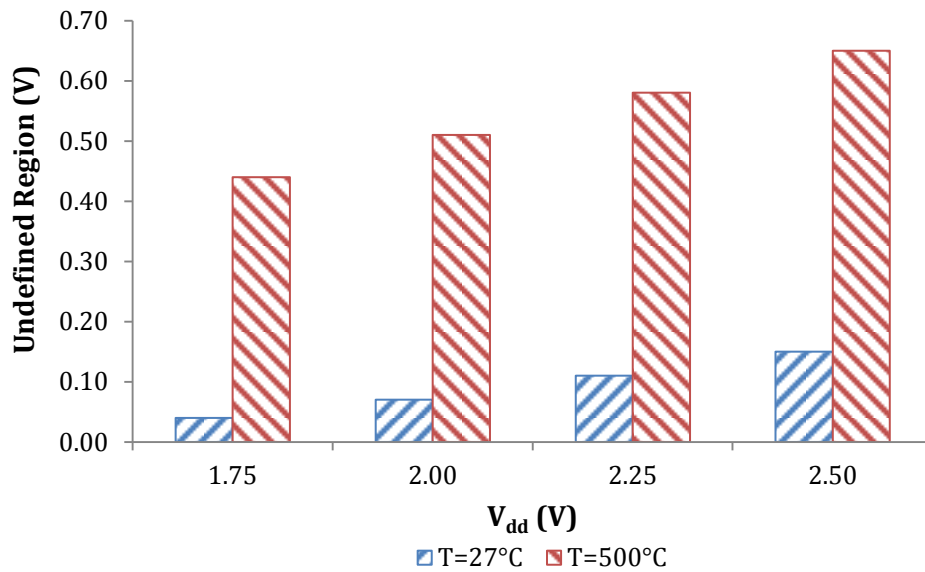


Figure 4.6. Variation of undefined region of 4H-SiC CJFET inverter with supply voltage (V_{dd}) scaling at 27 °C and 500 °C.

Data showing the comparison of the metastable regions in the input voltage range of the CJFET inverter, at RT and 500 °C, as a function of supply voltage scaling is shown in Figure 4.6. The data show that the magnitude of the metastable region ($V_{IH} - V_{IL}$) increases monotonically with temperature. This increase in the undefined region is due to the reduction in the turn on voltage of both n- and p-JFET with temperature, which is controlled by the built in potential of the p-n junction used to form the gate. As a result, both of the transistors in the complementary pair are turned on simultaneously for a wider range of input voltages, shifting V_{IL} to the left and V_{IH} to the right on the input voltage axis. Thus, this increased separation between V_{IL} and V_{IH} at elevated temperatures increases the metastability window. This increase in undefined region at high temperatures is evident from the VTC data shown in Figure 4.2.

Another important aspect which can be observed from the data in Figure 4.6 is that the magnitude of the metastable region increases with the supply voltage. At 500 °C, the metastable region increases by 47.7% as the supply voltage is scaled from 1.75 V to 2.5 V. This increase is because the inverter threshold

voltage (V_I) and, hence, the input and output transition points (V_{IH} , V_{IL} , V_{OH} and V_{OL}) get scaled with the supply voltage.

Metastability is a critical design parameter when CJFET devices are used to build complex structures such as latches and flipflops. If the voltage input to the next stage of a sequential circuit falls within this metastability window, then there will be intermittent failures in the operation of this circuit. Hence, CJFET devices operating at low values of supply voltages are pertained to be better candidates for sequential circuit applications, as the probability of these circuits violating set-up time and hold time requirements (i.e. metastability) is reduced. In strained silicon and silicon CMOS inverters, the undefined region is around 0.41 V and 0.59 V, respectively, for the 250 nm technology node, operating at RT and $V_{dd} = 1.8$ V [18]. In comparison, the 4H-SiC CJFET inverter studied here, operating at a supply voltage of 2 V, demonstrates a similar undefined region of 0.51 V at 500 °C. The smaller undefined region for CJFET inverter at $V_{dd} = 2$ V, compared to that at higher supply voltages, is deemed to be profitable from the perspective of noise margin and input metastability point of view [11].

4.2.2 Static Characteristics Summary

The static characteristics of a 4H-SiC CJFET logic inverter is analysed by studying the noise margins and the undefined region over a wide temperature range (−50 °C to 600 °C) as a function of supply voltage scaling. Both noise margins (NM_H and NM_L) and the undefined region are closely linked to the threshold voltage (V_t) of n- and p-JFET devices used to create the complimentary pair and to the off state leakage current (I_{off}) through the channel of these devices.

At high temperatures, the reduction in V_t and subsequent increase in I_{off} degrades both NM_H and NM_L . The scaling of supply voltage also has a significant effect on noise margins. Both NM_L and NM_H degrade with a reduction in supply voltage, as would be expected from the definition of NM given in equations 4.2 and 4.3. This degradation is linked to the inverter threshold voltage (V_I) and, hence, to the input and output transition points (V_{IH} , V_{IL} , V_{OH} and V_{OL}) which scale

with the supply voltage. For a supply voltage of 2 V, the noise margins of a CJFET logic inverter at 500 °C ($NM_L = 0.57$ V and $NM_H = 0.36$ V) are comparable to those of conventional silicon and strained silicon based CMOS logic inverters ($NM_L = 0.28$ V and 0.37 V and $NM_H = 0.84$ V and 0.96 V, respectively [18]), operating at RT. Furthermore, the metastability in CJFET logic inverter at 500 °C and $V_{dd} = 2$ V (0.51 V) is also similar to that in strained Si and Si based CMOS inverters (0.41 V and 0.59 V, respectively), operating at RT and $V_{dd} = 1.8$ V. These highly comparable results with RT strained Si and Si based CMOS inverters indicate integrity and robustness of SiC CJFET logic inverter operation at 500 °C.

4.3 Transient Characteristics

In real applications logic gates are switched on and off repeatedly every second. Therefore, it is important for circuit designers to determine the performance capabilities of new technologies, by studying the transient characteristics of logic gates. The transient characteristics allow designers to assess the performance of key parameters under different load conditions, operating frequencies, supply voltages and temperatures.

The main attributes of interest in analysing the transient characteristics of 4H-SiC CJFET circuits are the propagation delay, slew rate and switching frequency. The analyses of a logic inverter are presented in the following sections.

4.3.1 Propagation Delay

The transient characteristics of the proposed 4H-SiC CJFET logic inverter at RT and 500 °C are presented in Figure 4.7. From the data it can be seen that there is an improvement in speed (or in other words, improvement in responsiveness to change with the input signal) at high temperatures. The circuit is sourced with a fixed supply voltage of $V_{dd} = 2$ V for the entire temperature range studied (-50 °C to 600 °C). The common gate input voltage (V_{in}) of the complementary JFET pair is switched by a rectangular pulse of frequency 0.83 MHz ($V_{peak} = V_{dd}$, $t_r = t_f = 0.1$ μ s), at all temperatures.

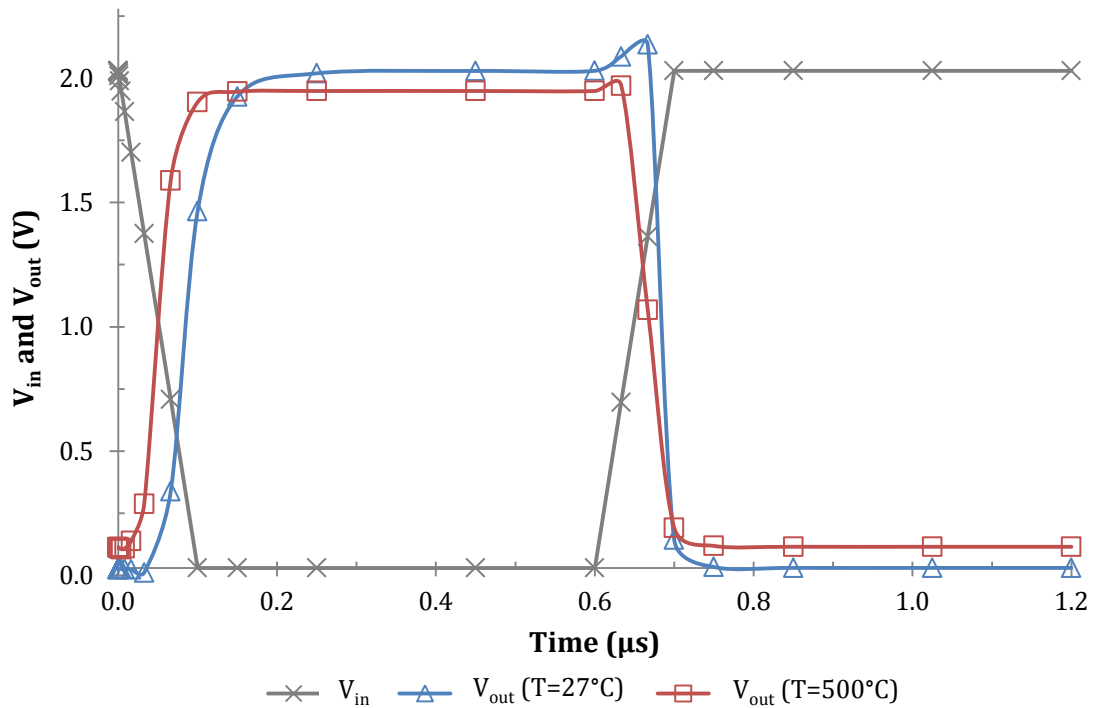


Figure 4.7. Comparison of transient characteristics of 4H-SiC CJFET inverter at 27 °C and 500 °C for a fixed supply voltage of 2 V. The inverter's responsiveness to the change in input signal improves with the increase in temperature. For high to low logic switch, the peak in V_{out} at 27 °C is due to stray capacitance, which diminishes at 500 °C.

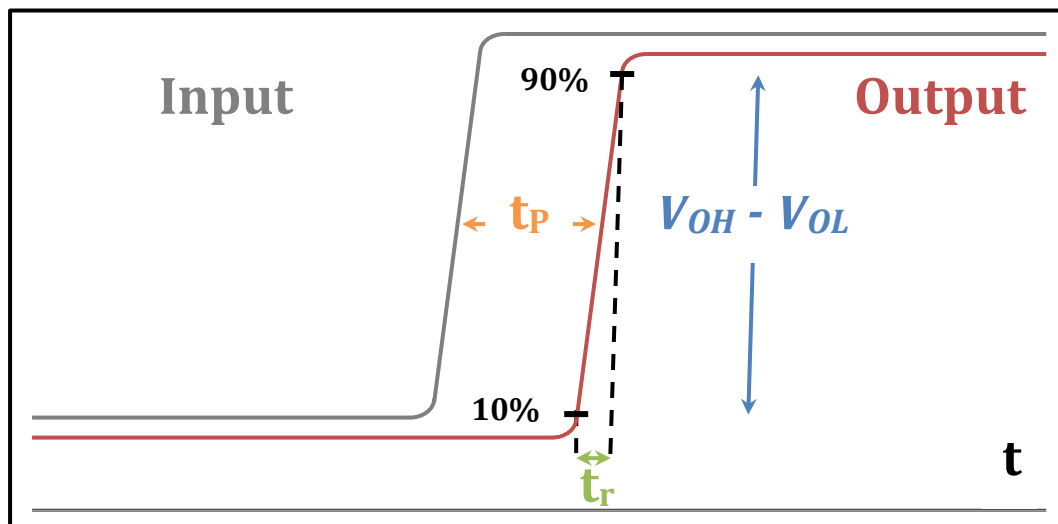


Figure 4.8. Switching diagram of digital logic.

Logic delay through a gate is described by propagation delay time t_p , which can be interpreted as the average time needed for the output to respond to a change in input logic state (as shown in Figure 4.8) and can be expressed as [19]:

$$t_p = \frac{(t_{PHL} + t_{PLH})}{2} \quad (4.4)$$

where t_{PHL} and t_{PLH} are the logic high-to-low and logic low-to-high propagation delays, respectively.

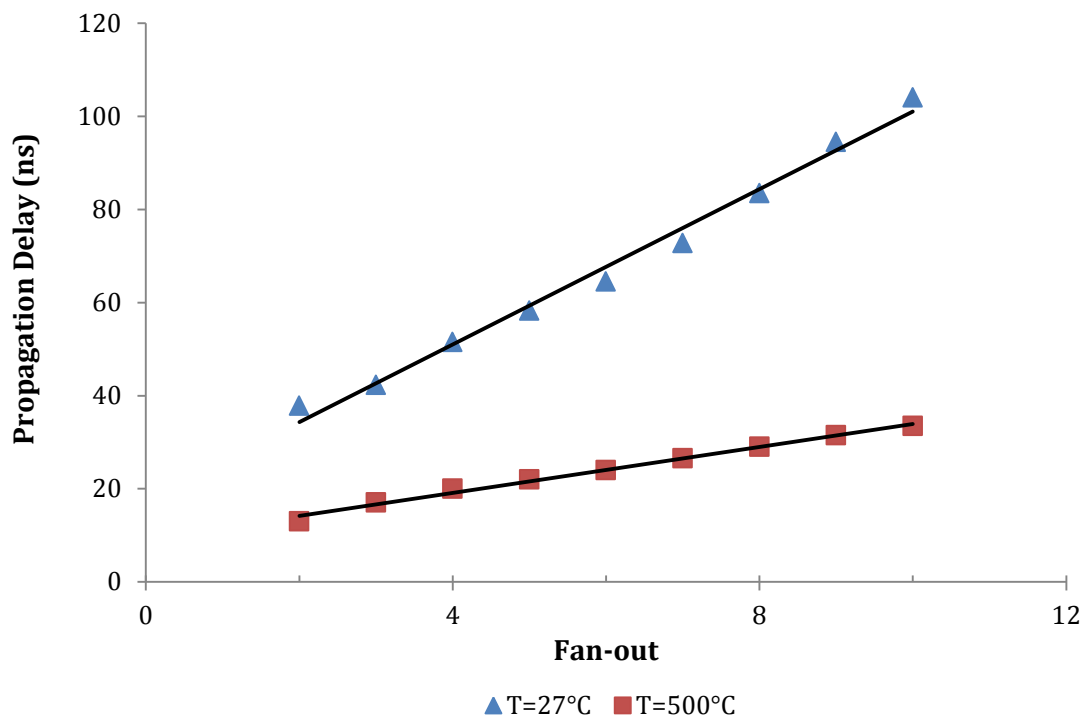


Figure 4.9. Propagation delay as a function of fan-out for 4H-SiC CJFET inverter at 27 °C and 500 °C, $V_{dd} = 2$ V. The improvement in speed at high temperatures is due to the increase in the drain current of the optimised n- and p-JFETs at high temperatures.

In deeply cascaded circuits where the propagation delay becomes additive [20], the 4H-SiC CJFET based circuits show a reduction in delay as the temperature is increased to 500 °C. Figure 4.9 show that the propagation delay of a CJFET inverter increases with fan-out, as expected. Between a fan-out of 2 and 10, the propagation delay has increased by 175.1% and 157.7% at RT and at 500 °C, respectively. Furthermore, the CJFET inverter has a considerably smaller delay

for the same fan-out at high temperatures. For a fan-out of 10, the propagation delay at 500 °C is 33.5 ns, which is 67.8% less than the RT value of 104 ns. This improvement in speed at high temperatures is because the drain current of the optimised n- and p-JFETs which form the complementary pair increases at high temperatures, as discussed previously in Section 3.4.4. In comparison, conventional strained silicon and silicon based CMOS inverters, operating at RT and $V_{dd} = 2$ V, have a propagation delay of around 70 ps and 85 ps, respectively, at the 180 nm technology node [18]. A direct comparison of the data for Si and SiC indicates that the strained silicon and silicon CMOS inverters have outclassed 4H-SiC CJFET inverter with a speed difference of around three orders of magnitude. However, recalling the fact that the SiC devices have a gate length of $L_g = 2$ μ m (section 3.4.3 of Chapter 3) and that propagation delay decays exponentially with L_g , [18], advances in SiC technology in the near future would enable building comparable size devices which will eventually overcome this speed barrier. It is also important to note that such scaling will lead to durability/reliability challenges, especially when high temperatures are involved, and are evident from the development history of silicon based ICs. Hence, by applying similar fundamental understanding of scaling and reliability trade-offs in silicon, extreme temperature SiC ICs can be further developed [4, 5].

Although Figure 4.9 show an improvement in speed of 4H-SiC CJFET inverters at higher temperatures, the static power dissipation will be higher for the same supply voltage due to higher transistor off state leakage current (I_{off}), as discussed previously in Chapter 3, section 3.4.4. Therefore, depending on the the application, a compromise in power and performance will be required. The reduction in power can be achieved by lowering the supply voltage. Figure 4.10 shows the variation in propagation delay of the CJFET inverter, at RT and 500 °C, for a supply voltage variation between 1.75 V to 2.5 V. Interestingly, the inverter consistently shows lower propagation delay (faster circuit) at 500 °C throughout the studied range of supply voltages.

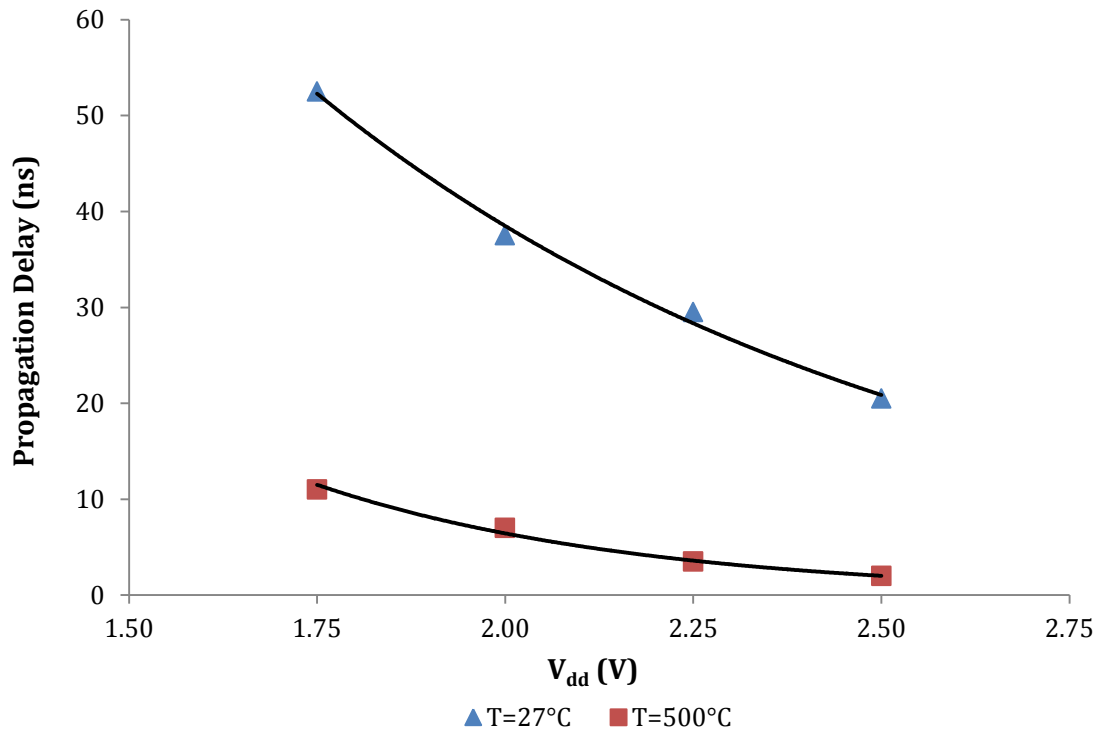


Figure 4.10. Variation of propagation delay of 4H-SiC CJFET inverter as a function of supply voltage (V_{dd}) at 27 °C and 500 °C.

It is apparent from the data presented that the increase in propagation delay with reduction in supply voltage is more severe at RT. As the supply voltage is reduced from 2 V to 1.75 V, the delay increases from 37.5 ns to 52.5 ns at RT and from 7 ns to 11 ns at 500 °C. The smaller delay exhibited by the CJFET inverter at high temperatures is accounted to the reduction of threshold voltage of the complementary pair and higher on state saturation current through the channel at high temperatures. Thus, for applications requiring operation at high temperatures, a similar speed performance can be attained by 4H-SiC CJFET technology at a much lower supply voltage, resulting in significant reduction in static power dissipation and subsequent increase in efficiency. Conversely, at low temperatures and with the reduction of supply voltage, the CJFET circuits will exhibit low power performance, but at reduced switching speed. It is also important to stress here that reducing the supply voltage to achieve low power operation will degrade the noise margins [10, 21], which is a critical design consideration for sensor and communications circuits at high temperatures. The variation of noise margin with supply voltage scaling was discussed in Section 4.3.1.

4.3.2 Slew Rate

The DC and transient characteristics can be used to quantify another performance metric, the slew rate. The slew rate of a device is the rate of change of output voltage, from high to low or from low to high [13]. In particular, this rate of change is considered as the voltage switch between 10% and 90% of its final value in a given time, as shown in Figure 4.8. The slew rate is given by [22]:

$$\frac{dv}{dt} = \frac{(V_{OH} - V_{OL})}{t_r \text{ (or } t_f)} \quad (4.6)$$

where t_r (t_f) is the rise (fall) time of the output signal.

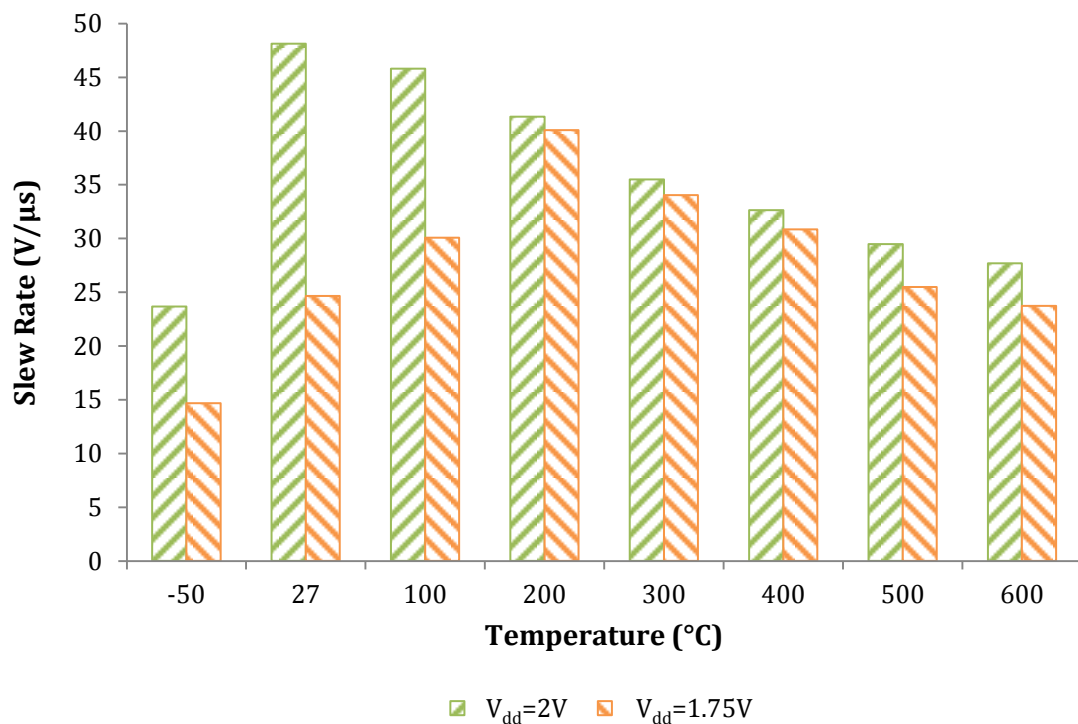


Figure 4.11. Comparison of slew rate of a 4H-SiC CJFET inverter at $V_{dd} = 2$ V and 1.75 V for a wide temperature range.

The slew rate of a 4H-SiC CJFET inverter as a function of temperature is shown in Figure 4.11. The graph compares the slew rate at a supply voltage of 2 V and 1.75 V, across a wide temperature range. The difference in slew rate is due to the change in “On” resistance of the transistors [13]. The slew rate, which reflects

the gradient of the DC and transient characteristics, gradually decreases from RT (or 200 °C) to 600 °C at a supply voltage of $V_{dd} = 2V$ (or 1.75 V). This progressive decrease in slew rate with increasing temperature is related to the decrease in output voltage swing, due to the observed increase in leakage current at high temperatures.

However, for temperatures below 27 °C (or 200 °C) for the $V_{dd} = 2 V$ (or $V_{dd} = 1.75V$) data, the slew rate decreases with temperature due to significant increase in the “On” resistance of the transistors, leading to lower values of drift current flowing through the channel and, hence, increasing the rise (or fall) times. At $V_{dd} = 1.75 V$ this phenomenon is evident for a considerably wider temperature range (i.e. between -50 and 200 °C). This is because with the reduced supply voltage, the circuit is operating at close proximity to the threshold voltage of the complementary pair.

4.3.3 Switching Frequency

The switching frequency is by far the most crucial performance factor of digital circuits, which also has great implications on the noise margin and power dissipation of high temperature CJFET circuitry.

When the switching frequency exceeds the maximum allowable switching frequency (f_{max}), the circuit cannot respond to the fast changing input and causes a reduction in the output voltage swing, which results in a degradation of the noise margin. Furthermore, in some cases fast switching causes the output voltage to never reach 0 V. This not only degrades the noise margin, but also increases the power dissipation in a circuit [19]. Therefore, it is important for a designer to know the maximum switching frequency for the circuit.

The maximum switching frequency (f_{max}) of a logic gate may be defined by [19]:

$$f_{max} = \frac{1}{t_{HL} + t_{LH}} \quad (4.7)$$

where, t_{LH} and t_{HL} are the rise (t_r) and fall (t_f) times for the circuit, respectively.

These switching (or transient) times t_{LH} and t_{HL} are very important as they represent the time required for the output to stabilise to a final, well-defined, logic value in response to changes in the input voltage. The sum of the transient times ($t_{LH} + t_{HL}$), therefore, represents the minimum time needed for a gate to undergo a complete switching cycle, i.e. for the output to change from a logic 0 to a logic 1 voltage, and then back to a logic 0 value.

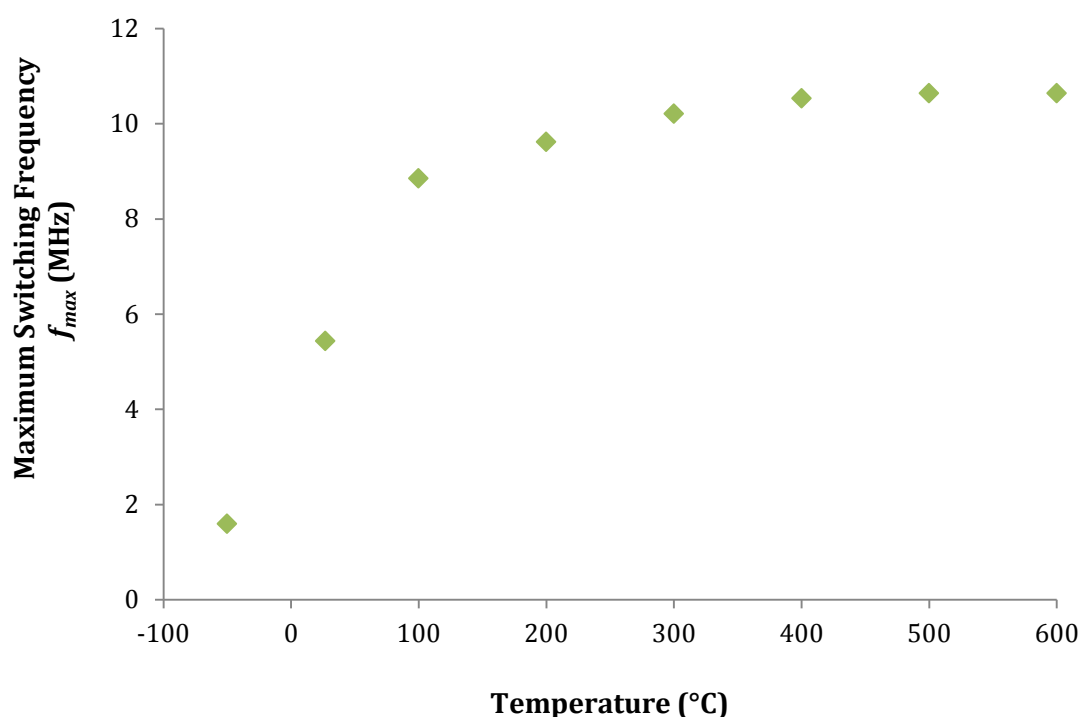


Figure 4.12. Variation of maximum switching frequency (f_{max}) of 4H-SiC CJFET inverter as a function of temperature, at a supply voltage of 2 V.

The maximum switching frequency signifies the maximum rate of data transfer for the gate. The effect of temperature on f_{max} of 4H-SiC CJFET logic inverter is shown in Figure 4.12. It is clear from the figure that f_{max} increases with temperature and then tends to saturate at high temperatures. This behaviour of f_{max} with temperature is similar to that of the drain saturation currents (I_{dss}) of n- and p-JFETs, discussed in chapter 3 section 3.4.5. This is due to the fact that the switching times t_{LH} and t_{HL} are characterised by the current levels of the

complementary pair, which in essence determines the time needed to charge and discharge the output capacitor. At RT, the CJFET inverter can be switched at a maximum frequency of $f_{max} = 5.43$ MHz. However, as the temperature increases, the current flowing through the channel of the complementary pair increases. Hence, at 500 °C f_{max} increases by 95.9% in comparison to the RT value to 10.64 MHz.

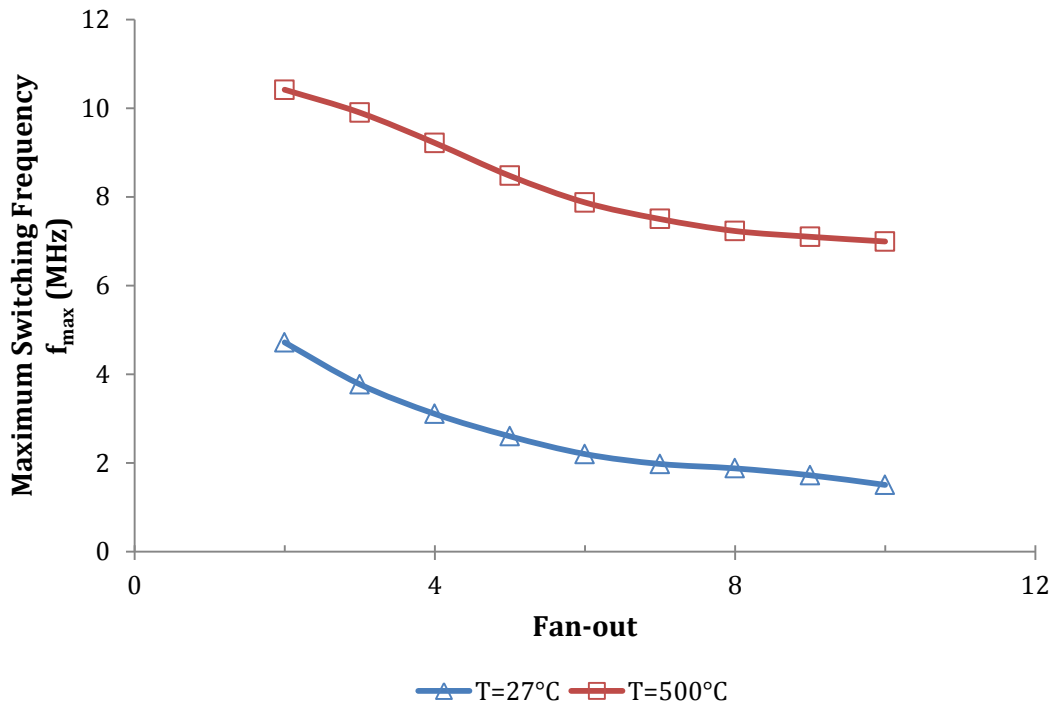


Figure 4.13. Maximum switching frequency as a function of fan-out for 4H-SiC CJFET inverter at 27 °C and 500 °C, $V_{dd} = 2$ V.

The data and analysis presented so far establishes that f_{max} is related to the current levels of the complementary pair. However, the switching times are also influenced by the value of output capacitor. To study this, the CJFET inverters with different number of fan-outs are simulated and the variation of f_{max} as a function of fan-out is plotted in Figure 4.13. From the figure it is obvious that f_{max} decreases with the increase in fan-out. This may be explained by treating each logic inverter in the fan-out as a load capacitor of capacitance c . Thus, for a fan-out of n , n numbers of load capacitors are connected in parallel to the output of the first stage (CJFET inverter), equating to a single large load capacitor of total capacitance $n \times c$. Increasing the number of fan-outs increases the total load

capacitance. Hence, with a fixed current level available at the output of the first stage, the time required for charging and discharging the total load capacitor increases with the capacitor size, leading to a decrease in f_{max} with an increase in fan-out. Between a fan-out of 2 and 10, the maximum switching frequency of CJFET inverter decreases by 68.2% at RT and 32.9% at 500 °C.

4.3.4 Transient Characteristics Summary

The performance of the SiC CJFET inverter is analysed by studying the propagation delay, slew rate and maximum switching frequency over a wide temperature range (−50 °C to 600 °C) and as a function of supply voltage scaling. For a fan-out of 10, the propagation delay at 500 °C ($V_{dd} = 2$ V) is 33.5 ns, which is 67.8% less than the RT value of 104 ns. This improvement in speed at high temperatures is because the drain current of the optimised n- and p-JFETs increases with temperature. Furthermore, the reduction in supply voltage from 2 V to 1.75 V increases the delay from 37.5 ns to 52.5 ns at RT and from 7 ns to 11 ns at 500 °C. Hence, for applications requiring operation at high temperatures, a similar speed performance can be attained by 4H-SiC CJFET technology at a much lower supply voltage, resulting in significant reduction in static power dissipation and subsequent increase in efficiency. However, as discussed previously in Section 4.2, reducing the supply voltage to achieve low power will degrade the noise margins [10, 21], which is a critical design consideration for sensor and communications circuits at high temperatures. Finally, the CJFET logic inverter, at $V_{dd} = 2$ V, has a maximum frequency of $f_{max} = 5.43$ MHz at RT which increases to 10.64 MHz at 500 °C, due to increase in device current levels.

4.4 Power Dissipation

The analyses of results from the previous sections show that 4H-SiC CJFET technology can be used to realise digital circuits at high temperatures and that by scaling the supply voltage, it is suitable for use in low power circuitry. In this

section the energy and power related issues of a 4H-SiC CJFET inverter are discussed.

4.4.1 Static Power Dissipation

Power dissipation is a significant concern when devices are operated in hostile environments. Supply voltage reduction has been the preferred technique for power reduction in Si technology [10]. However, at high temperatures the leakage current through the channel and gate of the transistor increases, which subsequently leads to an increase in the static power dissipation. Figure 4.14 illustrates the variation of the static power dissipation in a 4H-SiC CJFET inverter as a function of temperature, at a constant supply voltage of $V_{dd} = 2$ V. It is apparent from the data in the figure that the static power is around 6 pW at -50 °C and RT, and then increases exponentially thereafter at higher temperatures. At 500 °C, the static power dissipated by the 4H-SiC CJFET inverter is 353 nW. This low value of static power in CJFET inverter, as compared to that of the current SiC logic devices (\sim mW) [4, 5], can be attributed to the complementary structure, where, like CMOS, only one of the JFETs is “ON” at a given time during steady state. This ensures that the inverter consumes power only during switching. On the other hand, the lack of stable high temperature SiC CMOS technology, as discussed in Section 2.3, restricts current SiC logic devices to the use of “constantly ON” resistor(s) as pull-up device(s), where power loss is continuous irrespective of the switching state of the pull-down n-JFET. Hence, the current SiC logic devices, with high static power losses, are not feasible for implementing the much desired high temperature complex circuitries, leaving resilient 4H-SiC CJFET technology as a promising solution in the nearer term.

In comparison to the strained silicon and silicon based CMOS inverters, operating at RT with $V_{dd} = 1.2$ V, the static power dissipation is around 0.15 nW and 2.26 pW, respectively, for the 62 nm technology node [18]. These results indicate that 4H-SiC CJFET inverter dissipates a fairly comparable amount of static power at temperatures below 300 °C.

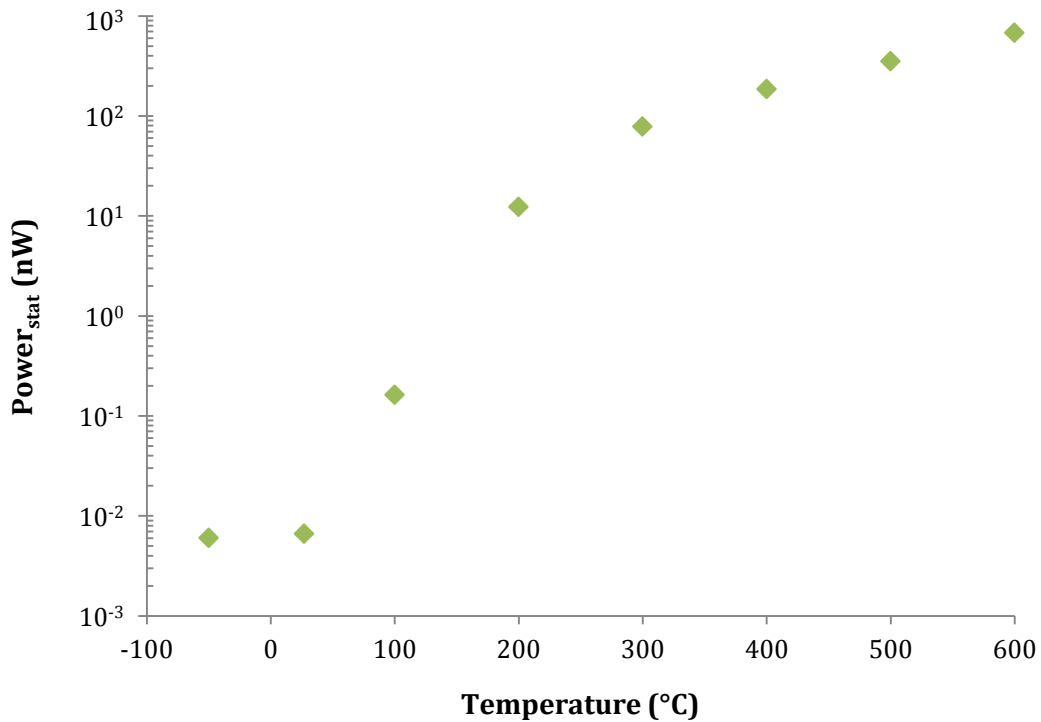


Figure 4.14. Variation of static power dissipation in a 4H-SiC CJFET inverter with temperature at a supply voltage of 2 V.

However, for high temperature operation, both high speed performance and a reduction in the overall power dissipation can be achieved by means of reducing the supply voltage, as discussed earlier in this section and shown in Figure 4.10. The variation of static power dissipation in the CJFET inverter with supply voltage scaling, at RT and 500 °C, is shown in Figure 4.15. It is evident from the figure that the static power decreases with supply voltage reduction, as expected. At 500 °C, the reduction in supply voltage from 2 V to 1.75 V reduces the static power dissipation by 45.9%. Hence, this significant reduction in static power dissipation will be advantageous for designing low power, high speed circuits operating at high temperatures.

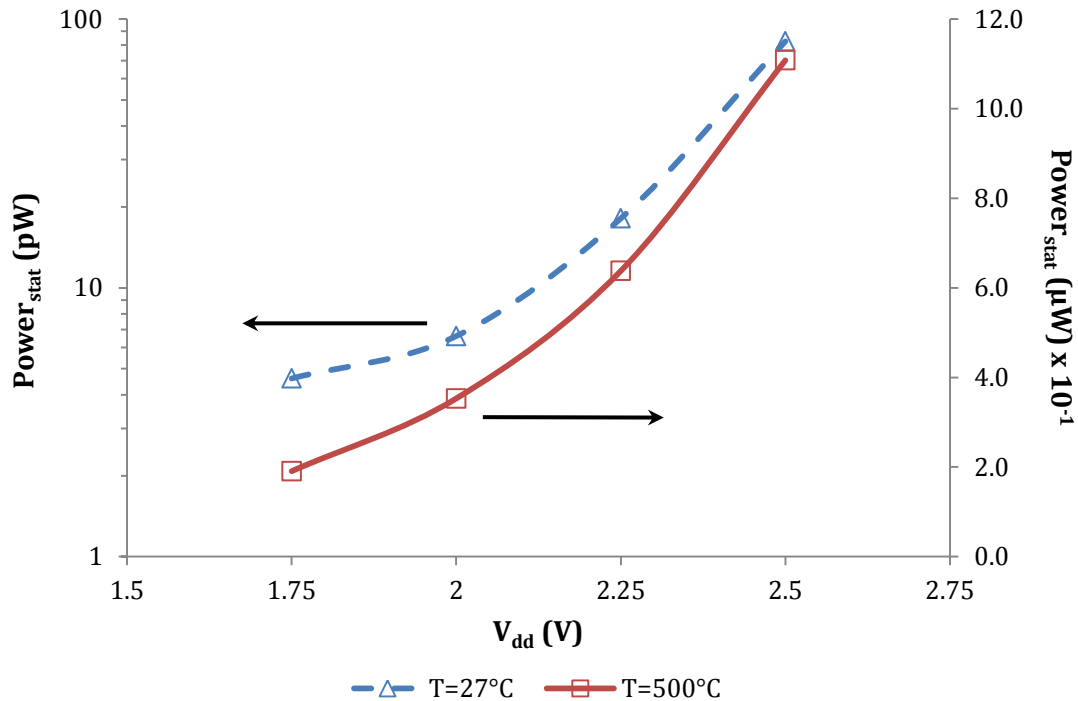


Figure 4.15. Static power dissipation in a 4H-SiC CJFET inverter when the supply voltage is scaled at 27 °C and 500 °C.

4.4.2 Dynamic Power Dissipation

In practical CJFET circuits where the gates are often switched between high and low logic states, a significant amount of power is dissipated during switching, known as the transient power.

In a complete switching cycle, the total dynamic power is the sum of static and transient powers. Figure 4.16 shows the variation of dynamic power dissipation in a 4H-SiC CJFET logic inverter as a function of temperature, at a constant supply voltage of 2 V. The figure shows that the dynamic power increases with temperature. At RT, the dynamic power dissipated in the circuit is 0.18 mW, which increases to 110 mW at 500 °C. This increase in dynamic power loss at high temperatures can be accounted for by the increase in both the static power loss and the transient power loss. At low temperatures, the static power loss is very low, but becomes significant at high temperatures, as discussed in the previous section. The transient power, on the other hand, increases at high temperatures for two reasons. First, the current levels of the complementary

pair increases with temperature. Secondly, at high temperatures, both n- and p-JFETs are switched on, at the same time, for a wider range of input voltage during a switching event. This prolonged and concurrent switching of the complementary pair at high temperatures is in turn for two main reasons. First, due to the decrease in threshold voltage of both JFETs at high temperatures and, secondly, due to the use of a fixed input voltage range and supply voltage across the temperature range studied.

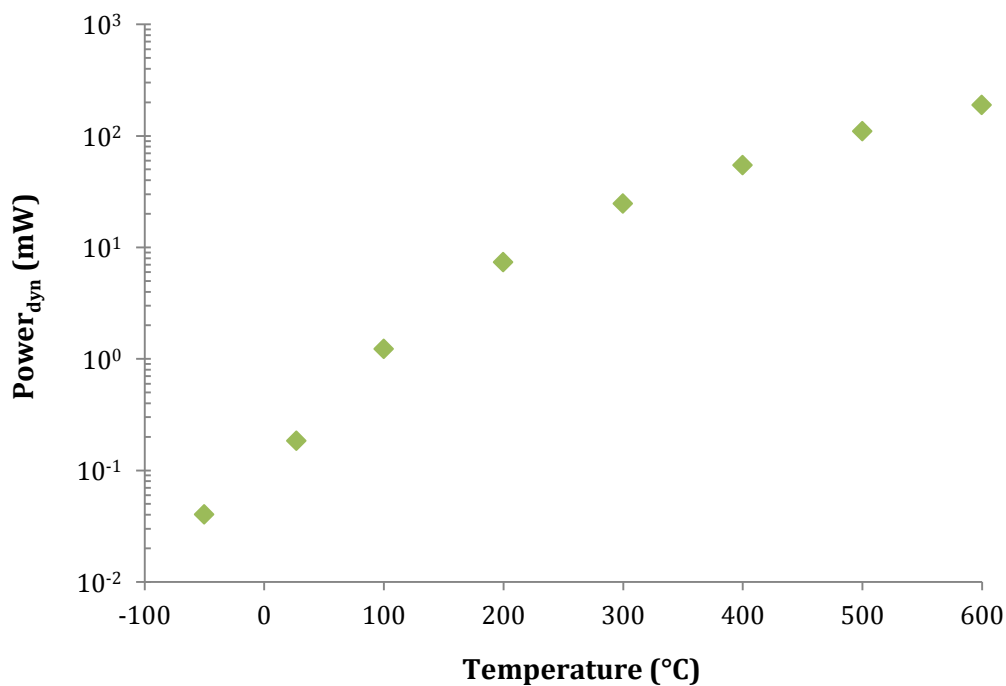


Figure 4.16. Variation of dynamic power dissipation in a 4H-SiC CJFET inverter with temperature at a supply voltage of 2 V ($f = 8.33$ kHz).

In addition to supply voltage and operating temperature, another important parameter which influences the dynamic power dissipation in CJFET circuits is the switching frequency (f). Figure 4.17 shows the effect of varying switching frequency on the 4H-SiC CJFET logic inverter, at RT and 500 °C. As expected, increasing the switching frequency increases the power dissipation [19]. This is because as f is increased, the inverter goes through more complete switching cycles in a given time which, in turn, increases the transient power loss component of the total dynamic power.

For high temperature and low power applications, decreasing the switching frequency with the supply voltage greatly reduces the power dissipation in the circuit [23]. As the switching frequency is reduced from 8.33 kHz to 0.83 kHz, the dynamic power, at 500 °C, reduces from 110 mW to 12 mW at $V_{dd} = 2$ V and 48.6 mW to 5.5 mW at $V_{dd} = 1.75$ V. In comparison, the strained silicon and silicon based CMOS inverters dissipates a similar amount of dynamic power (1.55 mW and 0.9mW) for the 62 nm technology node, operating at RT with $V_{dd} = 1.2$ V [18].

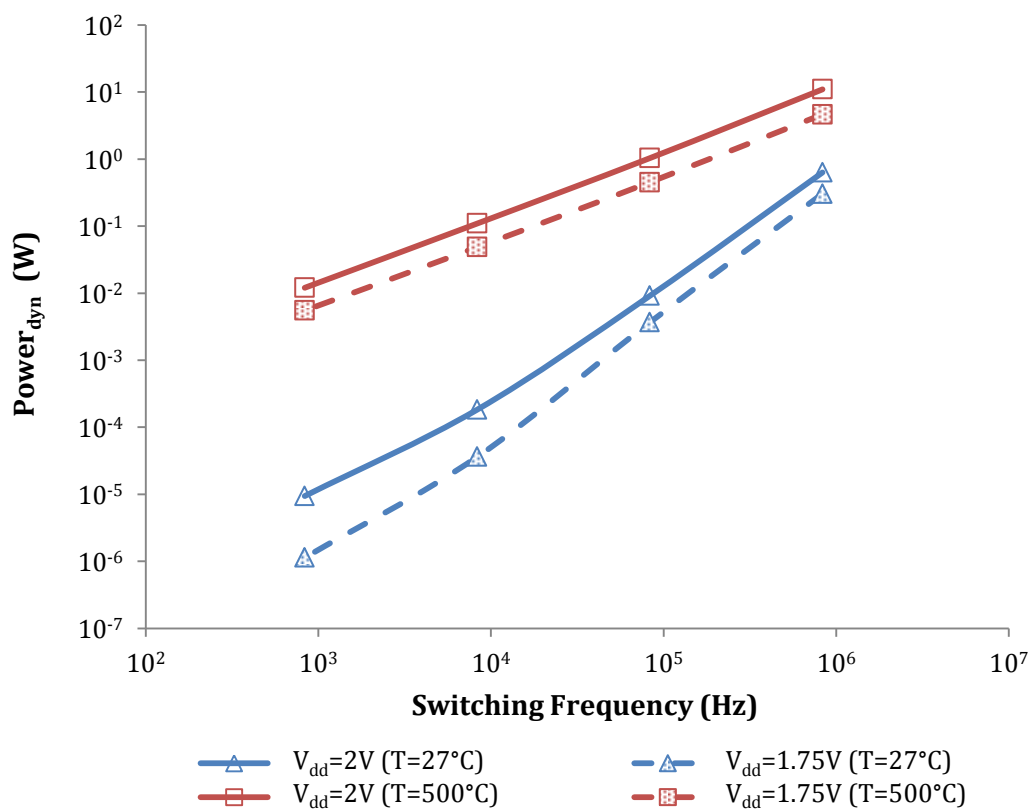


Figure 4.17. Dynamic power dissipation in 4H-SiC CJFET inverter as a function of switching frequency and supply voltage, at 27 °C and 500 °C.

4.4.3 Power-Delay Product

The power-delay product (PDP) is a metric which combines power and performance and enables comparisons between different process technologies [24]. PDP is given by [19]:

$$PDP = P_{av} t_p \quad (4.8)$$

where P_{av} is the average power dissipation over a switching cycle and t_p is the propagation delay time.

The PDP has units of *Watt-sec = Joules*, so that it is often interpreted as the average energy per switch. It is desirable to have small PDP values, as this implies fast switching and small power dissipation [19]. For the supply voltage range studied, it can be seen from the 500 °C data in Figure 4.18 that the PDP increases with supply voltage and then shows saturation for supply voltages above 2V. At low voltages, PDP is dominated by the rapid increase in dynamic power. But, as V_{dd} is increased further, the propagation delay decreases and causes the observed saturation in PDP at higher supply voltages.

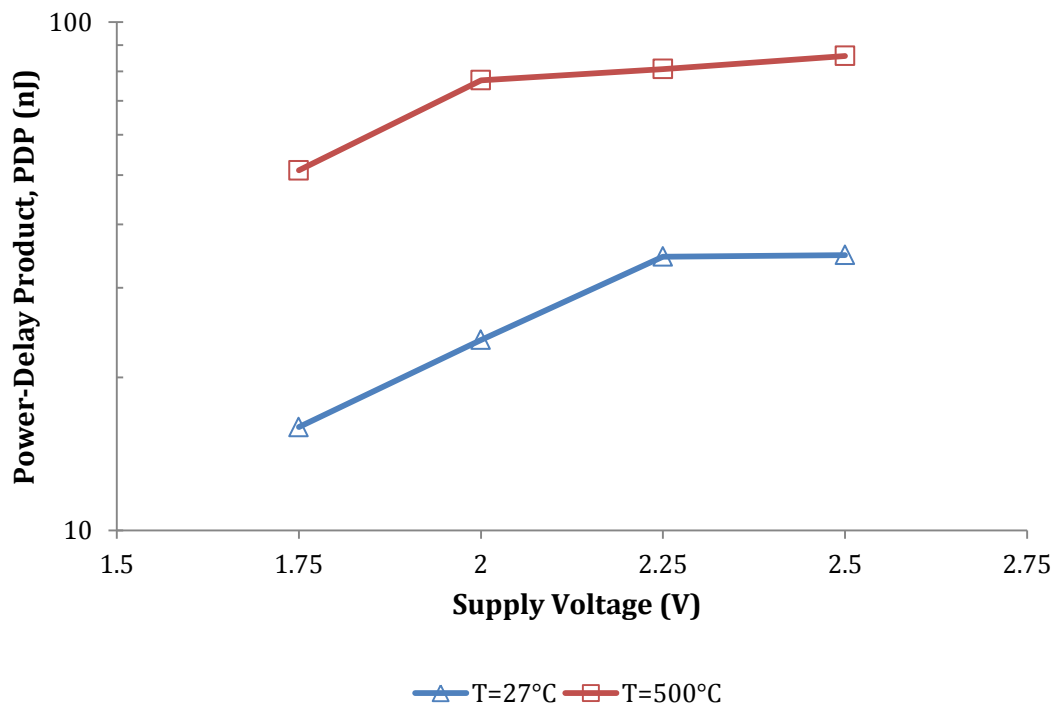


Figure 4.18. Power-delay product of a 4H-SiC CJFET inverter when the supply voltage is scaled at 27 °C and 500 °C ($f = 0.83$ MHz).

It is interesting to note that although the circuit is faster at 500 °C in comparison to RT, the PDP at 500 °C is higher. This shows that at high temperatures

excessive power dissipation degrades the overall performance of the circuit. However, as discussed earlier in Section 4.4.2, the power dissipation in CJFET circuitry can be vastly improved by reducing both the supply voltage and switching frequency.

4.4.4 Power Dissipation Summary

The efficiency of a 4H-SiC CJFET logic inverter is determined by studying the static and dynamic power losses as a function of temperature, supply voltage and switching frequency. Similar to CMOS, the CJFET logic inverter dissipates power only during switching. However, due to an increase in off state (leakage) current at high temperatures, the static power loss in the CJFET inverter at 500 °C is 191 nW (at $V_{dd} = 1.75$ V) as compared to a few mW in current SiC logic devices [4, 5]. Hence, the current SiC logic devices, with high static power losses, are not feasible for implementing the much desired high temperature complex circuitries. The static power loss in the 4H-SiC CJFET inverter, however, can be further reduced for achieving complex logic functions by scaling down the supply voltage. The next section looks in to the feasibility of SiC CJFET ICs to achieve high circuit complexities with low power consumption at 500 °C, which is common for RT Si and strained Si CMOS chips.

4.5 Improvement in Power Dissipation at High Temperatures for Complex Circuitries

From the previous discussions, it is evident that the 4H-SiC CJFET technology demonstrates the feasibility of producing simple integrated circuits which are capable of performing beyond the temperature limits of Si and silicon on insulator (SOI) technologies. In addition, 4H-SiC CJFET technology, with reduced device dimensions and operating biases, provides the best solution to the current challenges⁸ faced by high temperature SiC technology. These challenges were discussed in detail in Sections 2.2 and 2.3.

⁸ Currently, one of the biggest challenges faced by SiC technology is high static power dissipation at 500 °C ($\sim 10^{-3}$ W). This is mainly due to lack of high temperature SiC CMOS technology, which appears to be a very daunting technical challenge to achieve in near future [4, 5]. The 4H-SiC

A further reduction in power, however, will be beneficial for the realisation of 500 °C SiC complex systems, far greater than a few-transistor ICs. This further reduction in power can be easily achieved by scaling the supply voltage down to 1 V. At this point, two important questions can be raised:

1. Why do we need SiC complex systems at high temperatures?
2. What is the justification for reducing the supply voltage to 1 V in regard to the circuit's robustness and performance at 500 °C?

These are discussed in detail in the following paragraphs.

Why do we need SiC complex systems at high temperatures?

Currently, silicon and silicon-on-insulator technologies are commercially available to satisfy the requirements for digital and analogue VLSI circuits up to a temperature limit of 300 °C. However, for applications beyond this temperature range, for example in monitoring gases near volcano vents to predict eruption, in aerospace and car industry for better fuel economy, or inside nuclear reactors, SiC based low power complex systems will be a key enabling technology [25, 26].

What is the justification for reducing the supply voltage to 1 V in regard to the circuit's robustness and performance at 500 °C?

As discussed in Section 3.4.4, the drain current (I_{dss}) of the optimised n- and p-JFETs, which form the complementary pair, increases at high temperatures. This enhancement in I_{dss} at high temperatures allows CJFET based logic devices to perform at higher speed, as discussed in Section 4.3. As a result, the reduction in supply voltage may be used as a means to reduce power loss at high temperatures, without significant degradation of the circuit performance. However, this reduction in supply voltage affects the robustness of the logic gate by degrading the noise margins [11, 12].

CJFET technology, however, dissipates around 10^{-9} W of steady state power at 500 °C, which is similar to that of strained Si technology at RT.

Table 4.1 gives a comparison of the 4H-SiC CJFET logic inverter characteristics (operating at 500 °C, on a reduced supply voltage of 1V) with the current state of the art technologies. With the scaling of supply voltage, the static power of the CJFET inverter has improved significantly by 94.2% from 353 nW at $V_{dd} = 2$ V to 20.6 nW at $V_{dd} = 1$ V. Furthermore, it is evident from the results shown in the table that even after supply voltage reduction to 1 V, the noise margins and the metastability in CJFET logic inverter are comparable to those of Si and strained Si based CMOS inverters operating at RT. However, for applications demanding higher noise margins, the performance of the CJFET logic inverter can be compromised with improvements in noise margins through externally adjusting the threshold voltage of n- and p-JFETs using back-gate biasing control, V_{sub} . The effect of varying back-gate bias, V_{sub} , on the device performance parameters (V_t , I_{dss} and I_{off}) was discussed in detail in Section 3.4.5. The improvements in NM of the CJFET logic inverter using V_{sub} is discussed next.

Characteristics		Si CMOS	Strained Si CMOS	4H-SiC CJFET	Comments
		(27 °C)		(500 °C)	
Noise Margin (V)	NM_H	0.38	0.53	0.15	Similar
	NM_L	0.14	0.21	0.36	
Undefined region (V)		0.35	0.26	0.24	Similar
Max Switching Frequency (f_t)		~ GHz	~ GHz	~ MHz	Low
Static Power		~2 pW	~0.04 nW	20.6 nW	High
Dynamic Power (mW)		0.45	0.8	1.2	Similar

Table 4.1. Feasibility analysis of 4H-SiC CJFET ICs to achieve high circuit complexities at 500 °C with reference to RT Si and Strained Si CMOS technology ($V_{dd} = 1$ V) [18].

Improvement in noise margin using back-gate biasing control

It is evident from Table 4.1 that the CJFET logic inverter has a lower value of NM_H than NM_L . This has been discussed in detail in Section 4.2.1. Taking into consideration the definitions of high and low NM ($NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$), the NM_H could be increased by reducing V_{IH} and by increasing

V_{OH} . This, in turn, could be achieved either by increasing the threshold voltage of the p-JFET or by reducing the threshold voltage of the n-JFET. The latter option is susceptible to giving rise to device off-state (leakage) current at high temperatures, deteriorating both power dissipation and performance of the logic circuit. Hence, a much safer option of increasing the threshold voltage of the p-JFET is adopted. This would improve the circuit's NM and power dissipation, but at an expense of degradation in the circuit's propagation delay.

In this case, the threshold voltage of the p-JFET is increased by increasing the biasing on the back-gate of the p-JFET from 2 V to 2.5 V. Figure 4.19 shows the VTC of the CJFET logic inverter (operating at 500 °C and $V_{dd} = 1$ V) for the two back-gate biasing voltages. It is evident from the figure that by increasing V_{tp} ($V_{subp} = 2.5$ V), the overall VTC, along with all the critical input voltages (V_{IH} and V_{IL}), has shifted to the left. Furthermore, the critical output voltages (V_{OH} and V_{OL}), have also shifted closer to V_{dd} and zero volts, respectively. A comparison of the new set of noise margins and static and dynamic power losses ($V_{subp} = 2.5$ V) with that at $V_{subp} = 2.0$ V is presented in Table 4.2. From the data presented in the table it is evident that the NM_H (at $V_{subp} = 2.5$ V) has improved significantly by $\sim 50\%$, with a slight reduction in NM_L . Both noise margins now have similar values which is also evident from the symmetric VTC at $V_{subp} = 2.5$ V, Figure 4.19. Furthermore, a significant reduction in both static and dynamic power losses is also observed for the $V_{subp} = 2.5$ V data set, at 500 °C and $V_{dd} = 1$ V. This can be accounted for by the reduction in off-state current of the p-JFET, as a result of its increased threshold voltage at $V_{subp} = 2.5$ V. Hence, with these improvements in noise margins and power dissipation, SiC CJFET technology proves to be a better alternative to previously reported SiC based logic devices in the literature [4, 5] for low power complex systems in extreme environments.

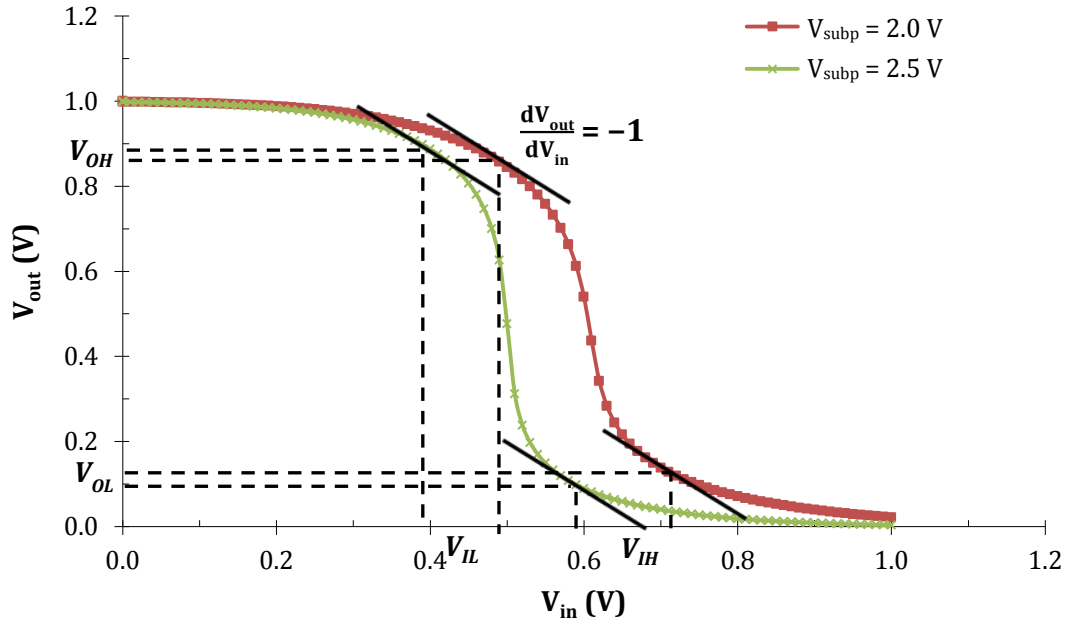


Figure 4.19. VTC of the 4H-SiC CJFET logic inverter for $V_{subp} = 2\text{ V}$ and 2.5 V , at 500 °C and $V_{dd} = 1\text{ V}$.

$V_{subp}\text{ (V)}$	$NM_H\text{ (V)}$	$NM_L\text{ (V)}$	$P_{stat}\text{ (nW)}$	$P_{dyn}\text{ (mW)}$
2.0	0.15	0.36	20.6	1.22
2.5	0.31	0.29	5.84	0.77

Table 4.2. Comparison between noise margins and power dissipation in 4H-SiC CJFET logic inverter (at 500 °C and $V_{dd} = 1\text{ V}$) as the V_{tp} is increased using back-gate bias.

4.6 Chapter Summary

In this chapter, the static and dynamic characteristics of 4H-SiC CJFET logic inverters were studied, using calibrated FE simulations, to assess the potential improvements in performance over previously reported SiC logic families. The static characteristics of the 4H-SiC CJFET logic inverter was analysed by studying the noise margins and the undefined region over a wide temperature range (-50 °C to 600 °C) as a function of supply voltage scaling. Both noise margins (NM_H and NM_L) and the undefined region were found to be closely linked to the threshold voltage (V_t) and to the off state leakage current (I_{off}) flowing through the channel of n- and p-JFETs, devices used to create the complimentary pair. At $V_{dd} = 2\text{ V}$, both noise margins and metastability in the CJFET logic inverter were

found to be comparable to those of conventional silicon and strained silicon based CMOS logic inverters, operating at RT. This indicated integrity and robustness of the 4H-SiC CJFET logic inverter operation at 500 °C.

The performance of the 4H-SiC CJFET inverter was analysed by studying the propagation delay, slew rate and maximum switching frequency over a wide temperature range and as a function of supply voltage scaling. For a fan-out of 10, the propagation delay at 500 °C ($V_{dd} = 2$ V) was 33.5 ns, 67.8% less than the RT value of 104 ns. This improvement in speed at high temperatures was because the optimised n- and p-JFETs were designed such that the drain current increased with temperature. Furthermore, the reduction in supply voltage from 2 V to 1.75 V increased the delay from 37.5 ns to 52.5 ns at RT and from 7 ns to 11 ns at 500 °C. Hence, for applications requiring operation at high temperatures, a similar speed performance could be attained by 4H-SiC CJFET technology at a much lower supply voltage, resulting in significant reduction in static power dissipation and subsequent increase in efficiency.

The efficiency of the 4H-SiC CJFET logic inverter was determined by studying the static and dynamic power losses, as a function of temperature, supply voltage and switching frequency. Similar to CMOS, the CJFET logic inverter dissipates power only during switching. However, the static power losses in the CJFET inverter were shown to increase at high temperatures due to an increase in the off state (leakage) current. High static power losses (in the range of milli-Watts at elevated temperatures) are a serious issue in the current SiC logic devices, limiting them to rudimentary functions only. At 500 °C, the static power loss in the 4H-SiC CJFET inverter was found to be 191 nW at $V_{dd} = 1.75$ V, demonstrating significant improvements in power dissipation over previously reported structures.

It was also shown that with the scaling of supply voltage, the static power loss in the 4H-SiC CJFET inverter can be further reduced for achieving complex logic functions. With the supply voltage scaled to 1 V, the static power of the CJFET inverter was reduced to 20.6 nW, but at the expense of degrading the noise

margin high to 0.15 V and noise margin low to 0.36 V. The noise margins were, however, shown to have improved by adjusting the back-gate bias V_{sub} .

4.7 References

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Chapter 5. Effect of Process Variations on 4H-SiC CJFET Circuit Performance

5.1 Background

Current advances in silicon carbide technology have led to the realisation of many high temperature, radiation tolerant devices and circuits which are not possible with silicon [1-4]. At present, SiC devices are larger ($L \sim 10 \mu\text{m}$) than those fabricated in Si and reduction of device dimensions and operating biases are vital to achieve complex integrated circuitry capable of higher frequency, improved performance and increased functionality [5]. In Chapter 3, a $2 \mu\text{m}$ 4H-SiC Lateral JFET (LJFET) structure was optimised for operation in extreme environments. This structure was designed to be normally-off, which is desirable for logic devices in terms of reduced gate drive complexity and power dissipation [5, 6]. In Chapter 4, the optimised n- and p-JFETs were used to demonstrate logic circuitry based on 4H-SiC CJFET technology, for the first time (to the author's knowledge). Furthermore, the superior advantages and feasibility of 4H-SiC CJFET technology, in terms of high circuit complexities with low power dissipation ($\sim 10^{-7}$ W static power) at high temperatures, over current SiC based logic circuitries in literature ($\sim 10^{-3}$ W static power [5, 7]) were also presented. This chapter binds the work presented in previous two chapters. The focus of this chapter is on the effect of manufacturing process variations on the performance of the CJFET logic inverter evaluated in Chapter 4. As a result of the subsequent variation in the geometric structure and doping profile, the effect on the electrical characteristics of the optimised n-JFET structure and inverter behaviour are shown.

5.2 Introduction

The random variation in manufacturing process parameters is a serious issue in the realisation of complex SiC logic for extreme environments, especially when device dimensions are scaled to achieve high performance. Furthermore, as the process steps required to manufacture circuits are more complex than for individual devices, the overall circuit performance is more sensitive to the underlying process variations [8].

The inter-die and the intra-die variation⁹ in manufacturing process parameters, such as channel length, channel thickness, threshold voltage, gate and channel doping concentrations, result in significant variations in the delay, noise margin and leakage power consumption of digital circuits [8-12]. The impact of random intra-die variations on the yield (parametric and functional) of digital circuits, such as memory cells and logic devices, is a serious issue in current scaled technologies [13]. Among the different sources of random intra-die variations, the most significant effect on Si CMOS technology is the threshold voltage (V_t) variation [14]. The statistical implant variation, dopant channelling through the gate into the channel, poly and diffusion critical dimension (CD) variation are the main causes of the V_t variations [13, 15].

In enhancement mode 4H-SiC JFETs, however, there is no gate oxide layer and, hence, the channel and gate doping fluctuations and variation in channel thickness are found to be the main causes of V_t variations [8, 16]. Furthermore, based on the similarity in operation to Si CMOS technology (discussed in Chapter 2), 4H-SiC CJFET technology is hypothesised to be significantly impacted by V_t variation. In CJFET logic arrays, random intra-die variations can cause significant variation in neighbouring gates or transistors and, therefore, can largely account for the poor yield (both functional and parametric). Hence with the increased sensitivity of CJFET logic to process variations, failure and performance analysis is of paramount importance to enhance the yield of high temperature CJFET logic circuitries.

⁹ The inter-die and the intra-die variations were discussed in detail in Section 2.4.2.

The DoE and RSM based statistical approach, similar to that discussed in Chapter 3, is used to model and analyse the impact of process variations at circuit-level. The statistical methodology is used to study the effect of process variability on the stability and efficiency of a 2 μm 4H-SiC CJFET logic inverter, previously demonstrated in Chapter 4. Statistical models are built for noise margin high (NM_H), noise margin low (NM_L) and static power dissipation (P_{stat}) as a function of the manufacturing process parameters. Subsequently, in Section 5.3, the methodology for modelling process variability is briefly discussed. The CJFET logic inverter's stability, in terms of noise margins, and efficiency, in terms of static power dissipation, are modelled and analysed at RT and 500 °C in Section 5.4. Finally, the chapter is summarised in Section 5.5.

5.3 Methodology - Modelling Variability for CJFET Technology

The methodology to study the effect of process variability at circuit level consists of TCAD FE simulations and the use of DoE and RSM techniques for statistical modelling and analysis. A detailed review on DoE and RSM methodology was presented in Section 2.5. The overall approach to model and analyse process variability is shown in Figure 5.1. The following sub-sections give a step-by-step description of the proposed methodology.

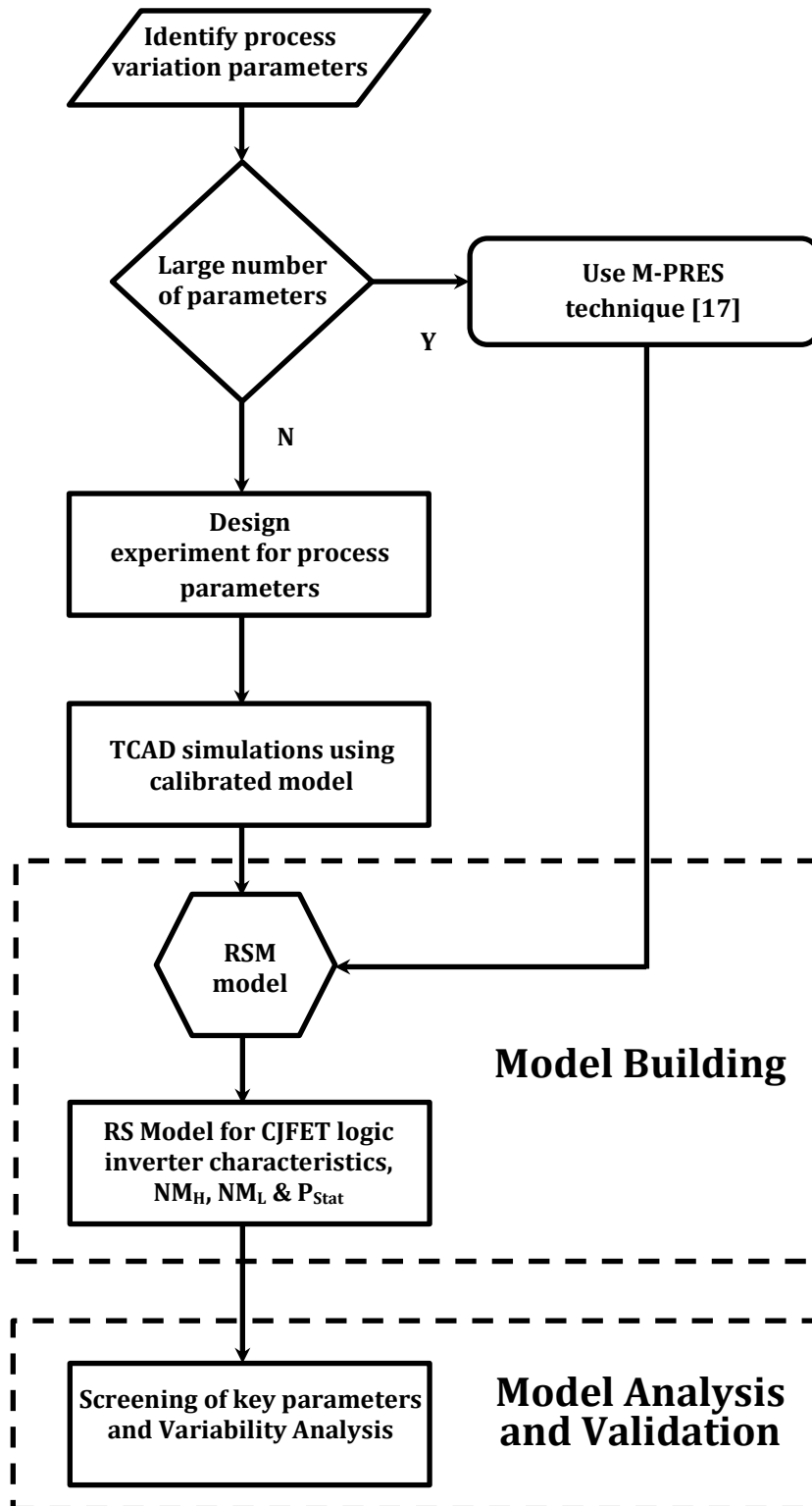


Figure 5.1. Flow diagram, illustrating methodology for modelling process variability for 4H-SiC CJFET logic inverter.

5.3.1 Process Variation Parameters (*factors*)

In a CJFET logic inverter, the variation in the device performance parameters such as V_t , I_{dss} and I_{off} of the complementary pair, i.e. n- and/or p-JFET, affects both the stability and efficiency of the logic gate. The variation in these device performance parameters are in turn mainly caused by the process variations in channel thickness and in channel and gate doping concentrations [8].

In this study, only the device process parameters of n-JFET (from the n- and p-JFET complementary pair) are varied. Varying the process parameters of both n- and p-JFETs would, otherwise, balance the overall effect on circuit performance. Hence, the parameters for p-JFET are kept at their optimum values, as shown in Table 5.1.

The parameter space considered in this study is illustrated in Table 5.1. The standard deviations (σ) for all the process parameters were set to $\pm 10\%$ of their mean/optimal values. For studying variability in a CJFET logic inverter, five significant process parameters were considered. However, for a different circuit the number of process parameters could be different, but the methodology for modelling variability presented will be the same. Also the methodology presented here is applicable to any σ variation, i.e. variation more or less than $\pm 10\%$.

As explained in Chapter 3, if the number of significant *factors* is more than ten, an alternative approach, M-PRES in [17], can be adopted. In this case, however, there are only five *factors*. Hence, standard RSM is performed directly, giving a model which is a function of all the process parameters/*factors*.

Symbol	Process Parameters (<i>factors</i>)	Units	Variations		
			-10% (-1)	Optimal (0)	+10% (+1)
x_1	Gate Length, L	μm	1.8	2.0	2.2
x_2	Gate Implant Depth, t_g	μm	0.198	0.22	0.242
x_3	Gate Implant Doping, N_A^+	cm^{-3}	9.0×10^{17}	1.0×10^{18}	1.1×10^{18}
x_4	Channel Doping, N_D	cm^{-3}	9.0×10^{16}	1.0×10^{17}	1.1×10^{17}
x_5	Back Gate Doping, N_A	cm^{-3}	9.0×10^{16}	1.0×10^{17}	1.1×10^{17}

Table 5.1. Key process parameters for variability study of 4H-SiC CJFET logic inverter performance metrics.

The CJFET logic inverter performance metrics (*responses*) of interest, noise margin high (NM_H), noise margin low (NM_L) and static power dissipation (P_{stat}), are calculated as discussed in Chapter 4.

5.3.2 Design Experiment for Process Parameters and TCAD Simulations

Next, an experiment is designed in order to carry out the TCAD FE simulations. This is to obtain the *responses* (i.e. noise margin high, noise margin low and static power dissipation) of the CJFET logic inverter following variations in the device process parameters (i.e. L, t_g , N_A^+ , N_D and N_A) of the n-JFET, to conduct the variability study using RSM. The design of this experiment is totally dependent on the type of RS design used. In this study, CCD, the most popular type of RS design method [18], is considered to approximate a second-order RS model for each *response* and, hence, to study the second-order effects. A type of CCD, known as face-centred central composite design FCCCD, is used in this study. FCCCD is discussed in detail in Section 2.5.1. The FCCCD for five *factors* ($k = 5$) would require a total of 43 experimental runs (2^5 factorial points, 10 axial points and 1 centre point). Hence, using the calibrated FE model parameters from Chapter 3, a total of 86 TCAD structure, device and circuit simulations are performed, both at RT and 500 °C with $V_{\text{dd}} = V_{\text{in}} = |V_{\text{sub}}| = 2 \text{ V}$, and the corresponding *responses* are modelled using RSM.

5.3.3 RS Model Building, Validation and Analysis

The RS models, based on variations in the device process parameters (*factors*) and the corresponding *responses*, are built on using commercial statistical software, Minitab [19]. A logarithmic transformation of x_3 , x_4 and x_5 is performed due to their values being large in comparison to the other two *factors*. Similarly, while modelling the static power dissipation (P_{stat}) logarithmic transformation has been used as its values are low with a large variation. The model, validation and analysis of variability results for CJFET logic inverter *responses* (noise margins and static power dissipation) are discussed in the next section.

5.4 Modelling Variability for CJFET Technology

5.4.1 Model Building

The first step in the variability study is to build a RS model which can precisely relate the *factors-response* variation relationship. Therefore, for each of the *responses*, noise margin high, noise margin low and static power, regression analyses are conducted to generate an equation to describe the statistical relationship between the *factors* and the *response*. Regression results indicate the direction, size, and statistical significance of the relationship between a *factor* and *response*. The sign of each coefficient indicates the direction of the relationship. Coefficients represent the mean change in the response for one unit of change in the *factor* while holding other *factors* in the model constant. Finally, the equation predicts new observations given specified *factor* values. Equation 5.1 gives the RS model for noise margin high (NM_H) of CJFET logic inverter, at 500 °C, in terms of the process parameters (*factors*) – denoted by x_1 , x_2 , ..., x_5 in Table 5.1. The model coefficients in this equation are normalised to the coded values of the statistically designed FCCCD experiment.

The models for the remaining CJFET logic inverter *responses*, constructed using this approach, are given in Appendix B.

$$\begin{aligned}
NM_{H\ 500\ ^\circ C}(V) &= 0.3661 - 0.0348x_1 - 0.1959x_2 - 0.0085x_3 \\
&+ 0.1948x_4 - 0.0378x_5 - 0.0059x_1^2 + 0.0136x_2^2 \\
&- 0.0044x_3^2 + 0.0061x_4^2 + 0.0021x_5^2 + 0.0053x_1x_2 \quad (5.1) \\
&+ 0.0017x_1x_3 - 0.0051x_1x_4 + 0.0020x_1x_5 + 0.0018x_2x_3 \\
&- 0.0336x_2x_4 + 0.0010x_2x_5 - 0.0007x_3x_4 + 0.0010x_3x_5 \\
&- 0.0032x_4x_5
\end{aligned}$$

5.4.2 Model Validation

In order to check accuracy and validity, the models were checked using the quality of the second-order fit, R^2 and R^2_{adj} (adjusted) [18, 20]. R^2 and R^2_{adj} were discussed in Section 3.4.3. The R^2 and R^2_{adj} for the CJFET logic inverter *responses* are summarised in Table 5.2. The values close to the desired 100% mark indicate that the second-order RS model captures a large portion of the observed variance. While fitting the model for P_{stat} , the initial values of R^2 and R^2_{adj} were poor; and were improved by logarithmic transformation.

CJFET logic inverter <i>response</i>	R^2 (%)	R^2_{adj} (%)
NM _H at 27°C	99.96	99.93
NM _L at 27°C	99.98	99.96
NM _H at 500°C	99.92	99.85
NM _L at 500°C	99.98	99.97
P_{stat} at 500°C	99.96	99.91

Table 5.2. RS model fits for CJFET logic inverter *responses*.

The model fit for the *responses*, NM_H, NM_L and P_{stat} , at RT and 500 °C are graphically illustrated in Figure 5.2. The straight line with unity gradient represents the ideal fit, where the fitted values are scattered. The vertical line in the figure represents the nominal *response* (i.e. at optimal values of the *factors*, given in Table 5.1). Overall, the model provides a good fit for studying variability.

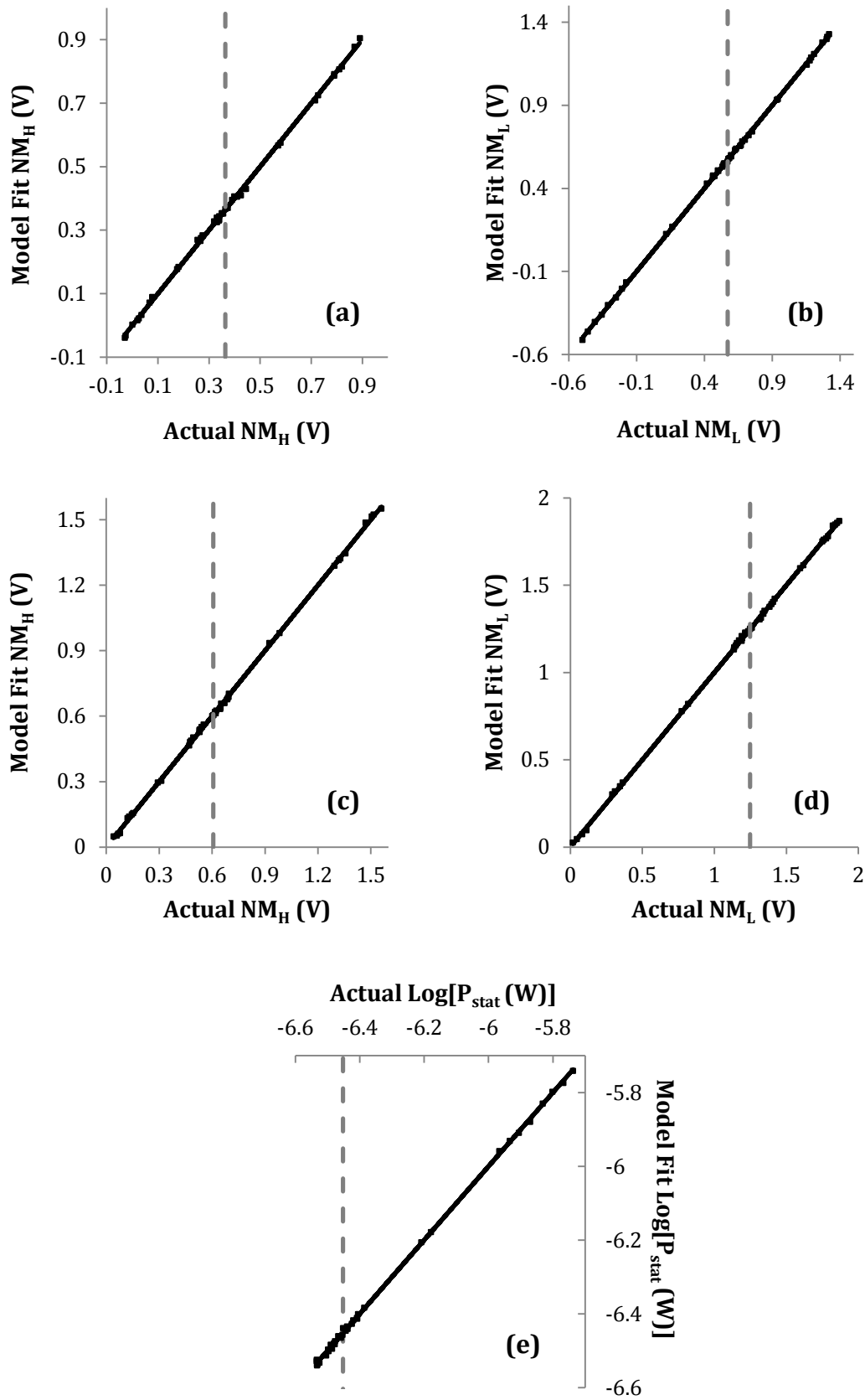


Figure 5.2. RS model fit vs. actual data for CJFET logic inverter *responses* (a) NM_H at 500 °C, (b) NM_L at 500 °C, (c) NM_H at 27 °C, (d) NM_L at 27 °C and (e) P_{stat} at 500°C. The vertical (dashed) line represents the nominal value.

5.4.3 Variability Results and Analysis

In this section, the effect of process variability on the stability (in terms of noise margin high, NM_H , and noise margin low, NM_L) and efficiency (in terms of static power dissipation, P_{stat}) of 4H-SiC CJFET logic inverter are analysed at RT and 500 °C. The most significant process parameters are screened using Pareto analysis [21]. Finally, based on the results from Pareto analysis, RS plots are generated for each of the inverter *responses* (NM_H , NM_L and P_{stat}), as a function of the most significant process parameters, to analyse variability.

Screening of Key Process Parameters

The Pareto analysis (based on the Factorial design¹⁰ for the five process parameters/*factors* listed in Table 5.1) is used as a screening technique to identify the most significant process parameters affecting CJFET inverter *responses*. The Pareto plot compares the relative magnitude and statistical significance of all the *main* (individual) and *interaction* (combinational) effects for the process parameters, ranking them accordingly in order of decreasing absolute value of effect.

The Pareto plot of CJFET inverter *responses* NM_H , NM_L and P_{stat} , at 500 °C and RT, are shown in Figure 5.3, Figure 5.4 and Figure 5.5, respectively. It is evident from these figures that x_2 (gate implant depth, t_g) and x_4 (channel doping concentration, N_D) are the two most significant process parameters causing variation in all inverter *responses* under study, both at RT and 500 °C. At individual device/transistor level, x_2 and x_4 are the two main parameters which control the flow of current through the channel in JFETs and, hence, control the variation in device threshold voltage, V_t , [8]. This justifies the proposed hypothesis that, like Si CMOS technology [14], 4H-SiC CJFET technology is most significantly impacted by V_t variation. Furthermore, x_5 (back gate doping concentration, N_A) is also found to be commonly affecting all of the studied *responses* at both temperatures.

¹⁰ Factorial design was discussed in detail in Section 2.5.1.

Besides these similarities between the RT and 500 °C Pareto plots, there is a common difference for all three studied *responses*. The influence of channel length (L), denoted by x_1 , on all *responses* is found to be more at 500 °C than at RT. This can be explained by comparing x_1 with x_3 (gate implant doping, N_{A^+}) for all *responses*, between RT and 500 °C. At RT, the depletion region width in the channel, due to the gate-channel p-n junction, is already large due to incomplete ionisation of free carriers at low temperatures. Increasing N_{A^+} further increases the depletion width in the channel, which limits current flow, thus increasing V_t . At 500 °C, the depletion width is reduced due to ionisation of free carriers at high temperatures. Thus, in this case, increasing N_{A^+} by 10% does not show a major effect on V_t . However, increasing L increases the input gate capacitance (reducing the device switching speed), as well as, increasing the channel resistance, leading to a considerable increase in V_t at high temperatures, as compared to that by increasing N_{A^+} .

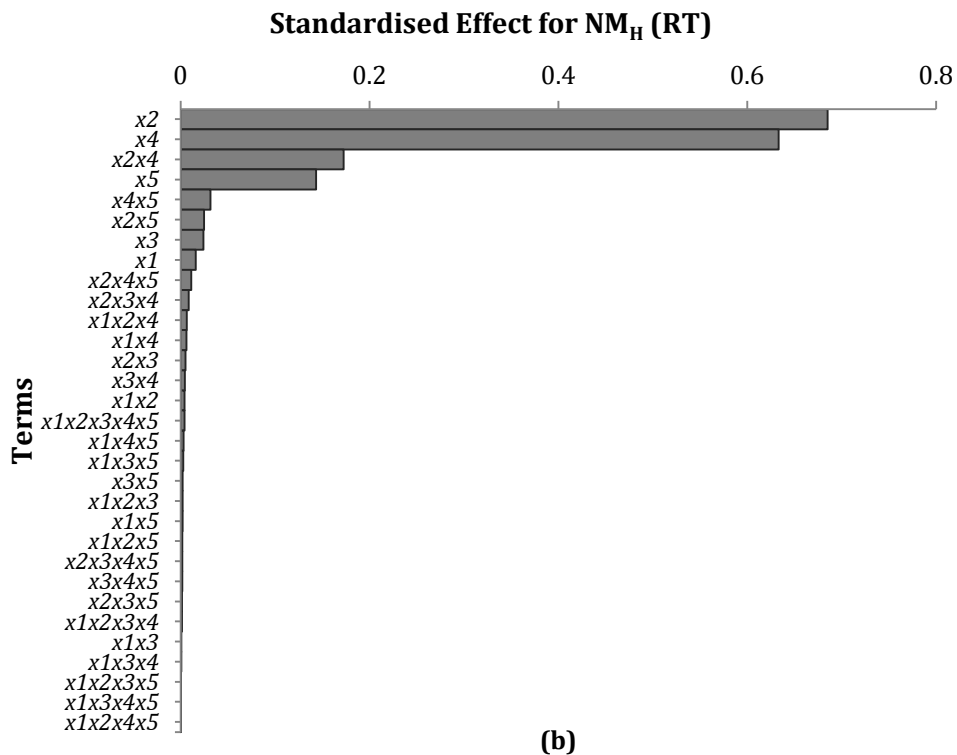
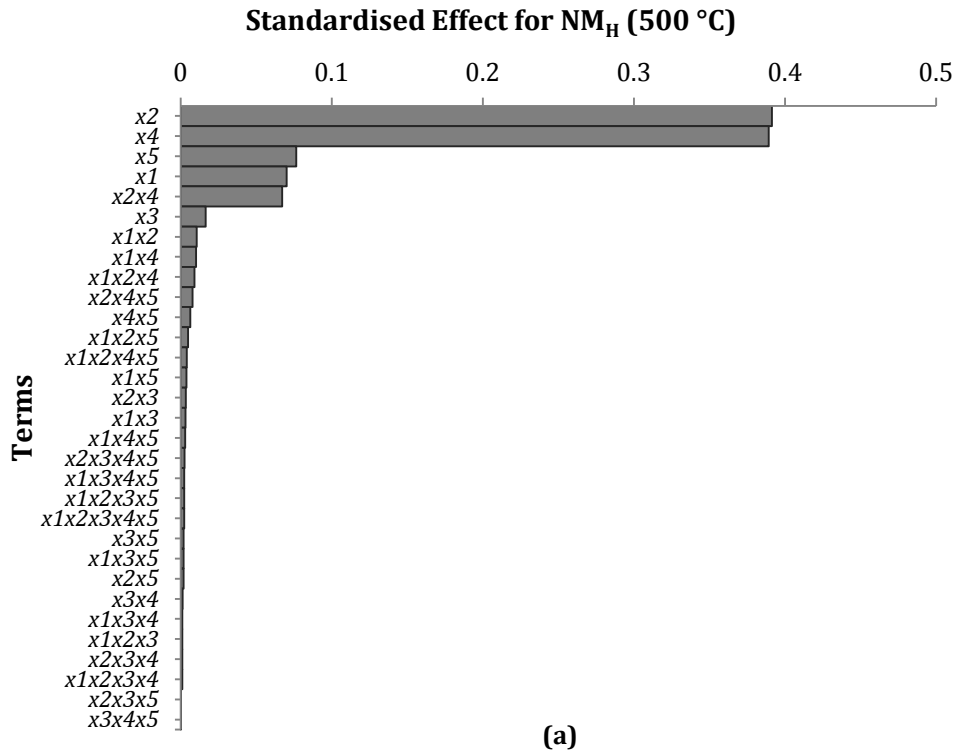


Figure 5.3. Pareto plot of noise margin high (NM_H) at (a) 500 °C and (b) RT.

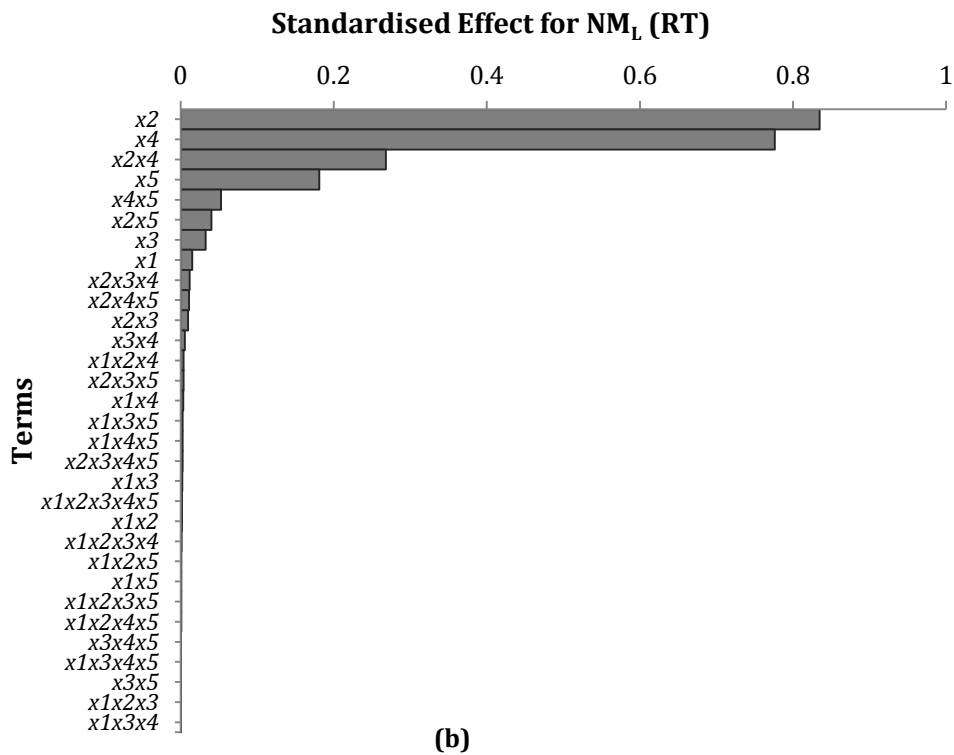
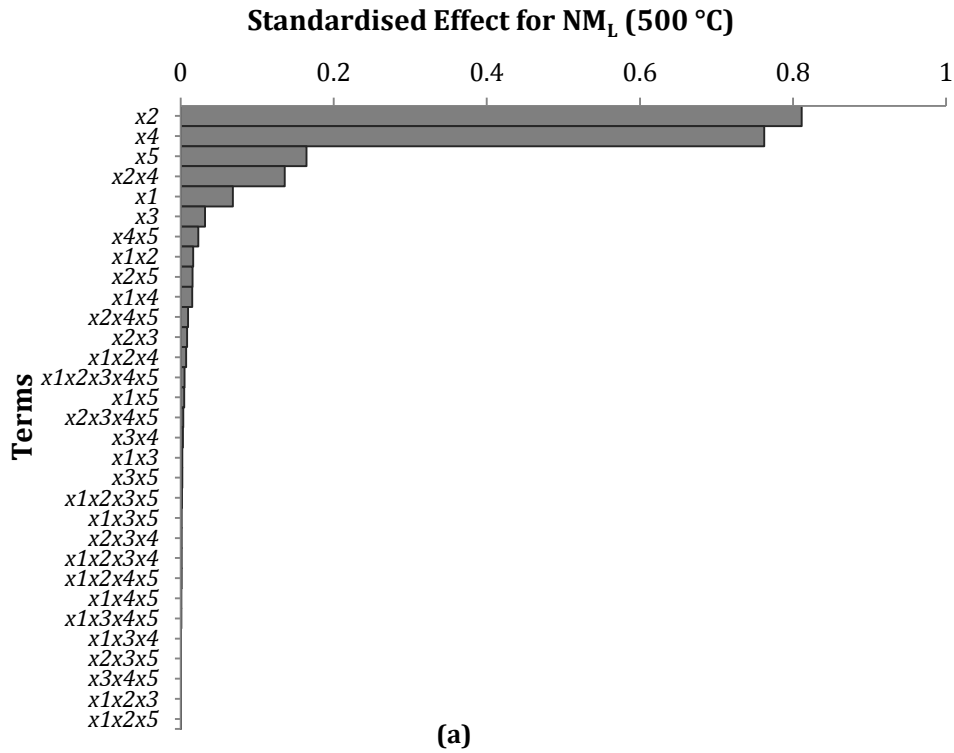


Figure 5.4. Pareto plot of noise margin low (NM_L) at (a) 500 °C and (b) RT.

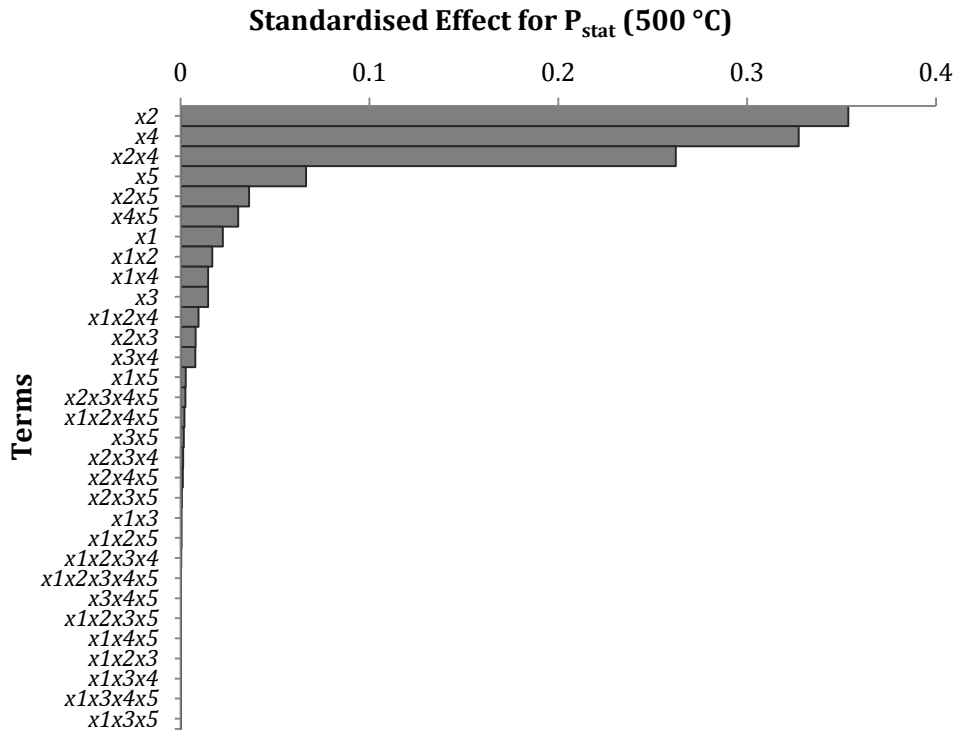
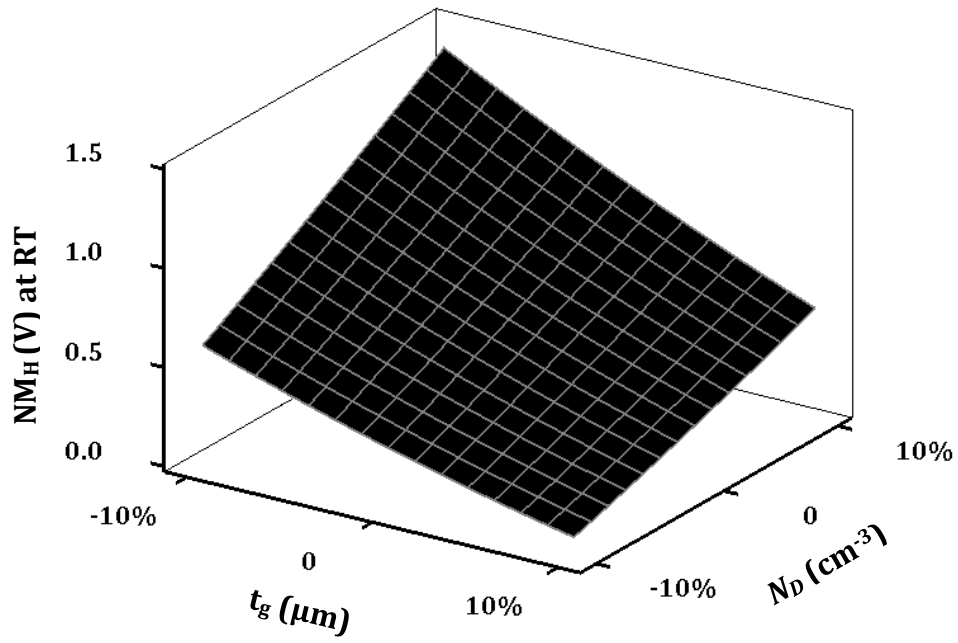


Figure 5.5. Pareto plot of static power (P_{stat}) at 500 °C.

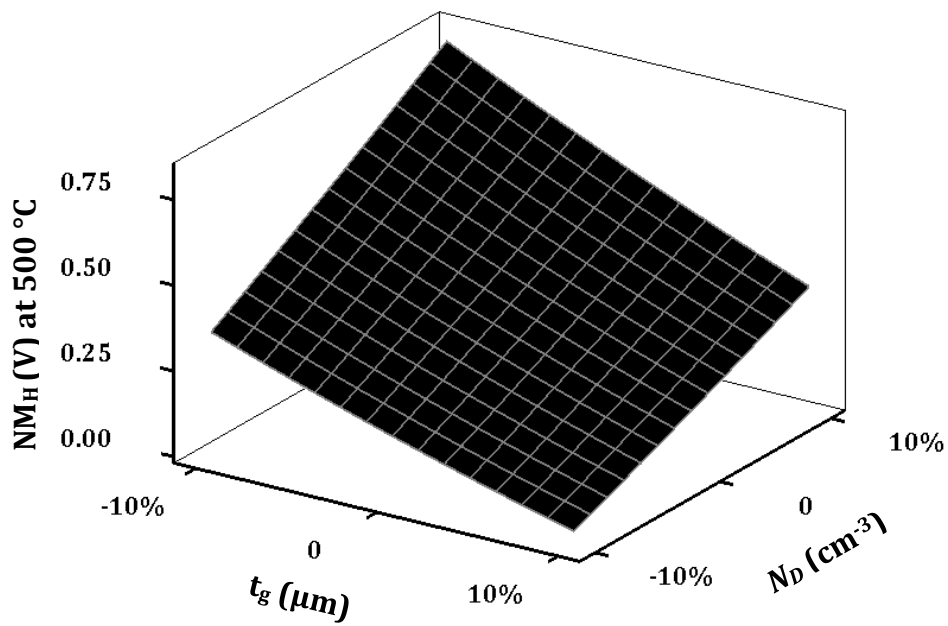
Based on the results from Pareto analysis, the following sub-sections present the variability analysis on the CJFET logic inverter *responses* NM_H , NM_L and P_{stat} , as a function of two of the most significant process parameters t_g and N_D .

Noise Margin High (NM_H)

The RS plot for NM_H as a function of two of the most significant process parameters, x_2 (gate implant depth, t_g) and x_4 (channel doping concentration, N_D), at RT and 500 °C, are shown in Figure 5.6 (a) and (b), respectively. At RT and 500 °C, NM_H has a nominal value of 0.60 V and 0.37 V, respectively. NM_H degrades by $\sim 50\%$ from its nominal value at the high level (10%) of t_g at both temperatures. A similar degradation is observed at the low level (-10%) of N_D , at RT and 500 °C. The degradation in NM_H is because the increase in t_g reduces the channel thickness of the n-JFET, limiting the current flowing through the channel. This in essence increases the threshold voltage (V_t) of the n-JFET by $\sim 26\%$ and $\sim 82\%$ from the nominal value of 1.56 V at RT and 0.48 V at 500 °C, respectively.



(a)



(b)

Figure 5.6. RS plot of noise margin high (NM_H) at (a) RT and (b) 500 °C, as a function of n-JFET parameters, t_g and N_D .

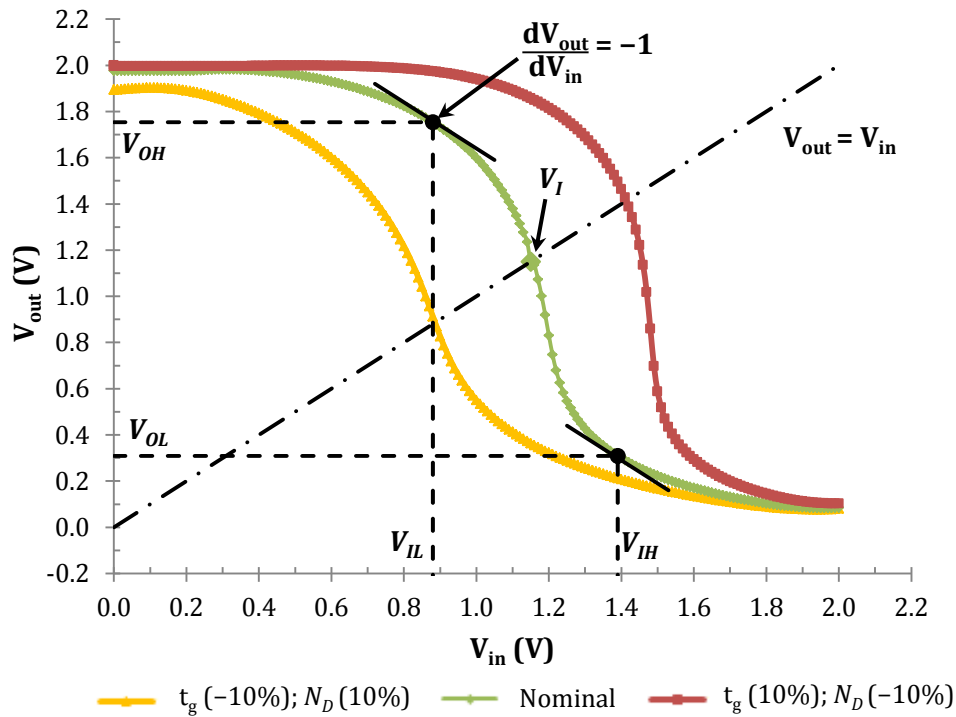


Figure 5.7. Voltage transfer curve (VTC) of the 2 μ m CJFET logic inverter at 500 °C, illustrating the effect of variation in gate implant depth (t_g) and channel doping concentration (N_D) of the n-JFET on the critical VTC voltages (V_{OH} , V_{OL} , V_{IH} , V_{IL} and V_I) and, hence, its impact on the inverter's noise margin ($NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$).

At the circuit level, this fluctuation in the threshold voltage of the n-JFET affects the stability of the logic inverter. This can be explained by exploring the effect of t_g on the voltage transfer curve of the CJFET inverter, as shown in Figure 5.7. VTC and all its critical voltages (V_{OH} , V_{OL} , V_{IH} , V_{IL} and V_I) have been previously discussed in detail in Chapter 4. Under nominal conditions, the complementary pair (n- and p-JFETs) has a threshold voltage of similar magnitude and the corresponding VTC (depicted by the green curve), along with the critical voltages, is illustrated in Figure 5.7. On the other hand, the increase of n-JFET threshold voltage degrades its performance. The output of the CJFET inverter now remains at the high logic level (i.e. close to 2 V) for a significantly wider range of input voltage, i.e. until the inverter input voltage (V_{in}) reaches the new, increased, V_t of the n-JFET, after which the output decays to low logic level (i.e. close to 0 V). The corresponding VTC is now as shown by the red curve in Figure 5.7. This shift in VTC, due to the increased V_t of the n-JFET, in essence

shifts all the critical VTC voltages (and most importantly V_{IH}) to higher V_{in} and, hence, degrades the noise margin high ($NM_H = V_{OH} - V_{IH}$).

Similarly, a decrease (-10%) in the channel carrier concentration, N_D , depletes the free carrier density and hence limits the current flowing through the channel. This results in the observed rise in threshold voltage (V_t) of the n-JFET by $\sim 23\%$ at RT and $\sim 69\%$ at 500 °C, from the nominal value. Consequently, the inverter VTC, along with all the critical voltages, shifts to the higher V_{in} , resulting in the degradation of NM_H .

In addition to the individual effects studied above, the combined effect of t_g , at the high level (10%), and of N_D , at the low level (-10%), on NM_H is $\sim 87\%$ at RT and $\sim 92\%$ at 500 °C. Such high values indicates that careful control of t_g (which in this case is realised by ion implantation) and uniformity in channel doping concentration (which depends on wafer quality) are the critical process steps in the realisation of enhancement mode SiC JFETs for high temperature CJFET logic.

The effect of process variability on the NM_L of CJFET logic inverter is discussed next.

Noise Margin Low (NM_L)

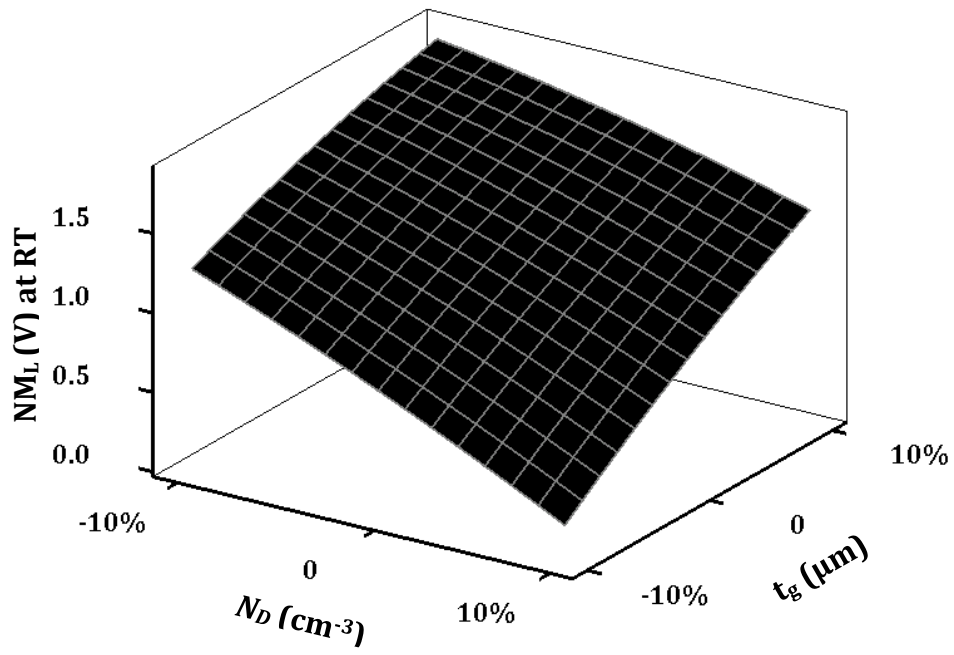
Figure 5.8 (a) and (b) show the RS plots for noise margin low (NM_L) as a function of t_g and N_D , at RT and 500 °C, respectively. NM_L has a nominal value of 1.25 V at RT and 0.56 V at 500 °C. At the low level (-10%) of t_g , NM_L degrades from its nominal value by $\sim 38\%$ at RT and by $\sim 78\%$ at 500 °C. A slightly lower degradation in NM_L , $\sim 34\%$ at RT and $\sim 70\%$ at 500 °C, is observed at the high level (10%) of N_D , from the nominal value. In this case, as t_g decreases, the channel thickness of n-JFET increases, reducing the barrier controlling the current flow through the channel. This results in a decrease in threshold voltage (V_t) of the n-JFET by $\sim 38\%$ at RT and by $\sim 98\%$ at 500 °C from the nominal value. Similarly, the increase in N_D populates the channel with additional carriers, decreasing V_t of the n-JFET by $\sim 28\%$ at RT and by $\sim 90\%$ at 500 °C.

At the circuit level, the effect of this V_t fluctuation on the stability of logic inverter NM_L is analogous to that discussed previously for NM_H . The drop in V_t of the n-JFET enhances its performance. The output of the CJFET inverter now remains at high logic level (i.e. close to 2 V) only for a limited range of V_{in} , until the inverter input voltage reaches the new, reduced, V_t of the n-JFET. The output then decays to low logic level (i.e. close to 0 V). The corresponding VTC is now as shown by the yellow curve in Figure 5.7. This shift in VTC, due to the fall in V_t of the n-JFET, in essence shifts all the critical VTC voltages (and most importantly V_{IL}) to the low values of V_{in} and, hence, degrades noise margin low ($NM_L = V_{IL} - V_{OL}$).

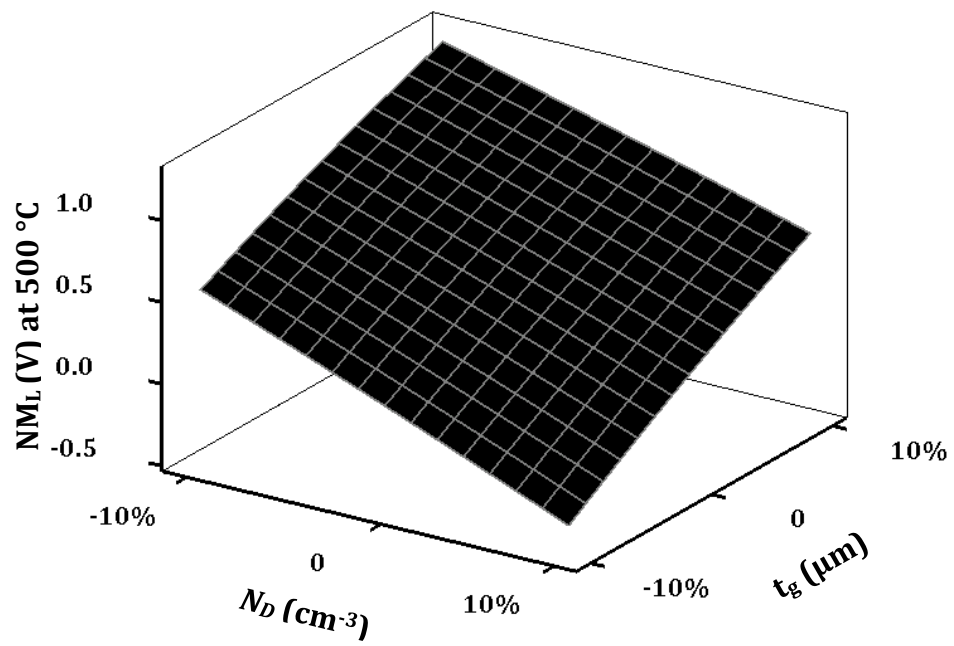
The combinational effect of t_g , at the low level (-10%), and of N_D , at the high level (10%), on NM_L is $\sim 82\%$ at RT and $\sim 159\%$ at 500 °C. The combinational effect of variations in t_g and N_D on NM_L is phenomenally large compared to the effect on NM_H . This is because at high temperatures, where the depletion width formed between the gate channel p-n junction is already reduced (resulting in a drop of threshold voltage), a further opening in the channel (by reducing t_g) and increasing the carrier density in the channel results in a further reduction in V_t , becoming negative. This changes the primary operation of the device from enhancement to depletion mode, resulting in malfunctioning of the logic gate.

Hence, it can be concluded that fluctuations in the process parameters, t_g and N_D , cause variations in threshold voltage of the device which in turn affects the stability of the logic inverter by affecting its noise margins.

The effect of process variability on the static power dissipation (P_{stat}) of CJFET logic inverter is discussed next.



(a)



(b)

Figure 5.8. RS plot of noise margin low (NML) at (a) RT and (b) 500 °C, as a function of n-JFET parameters, N_D and t_g .

Static Power (P_{stat})

Figure 5.9 shows the RS plot for static power dissipation of CJFET logic inverter (P_{stat}) as a function of t_g and N_D at 500 °C. P_{stat} has a nominal value of 6.62 pW at RT and 0.37 μW at 500 °C. At the low level of t_g , P_{stat} increases to 0.66 μW at 500 °C. A similar increase in P_{stat} (0.62 μW) is observed for high channel doping, at 500 °C. This increment in P_{stat} is due to the increased leakage/off-state current flowing through the channel at high temperatures. The reduction in device threshold voltage, due to variations in t_g and N_D , increases the leakage current further by reducing the channel barrier obstructing the off-state current flow. Hence, the combined effect of low t_g and high N_D increases P_{stat} to 1.53 μW , at 500 °C.

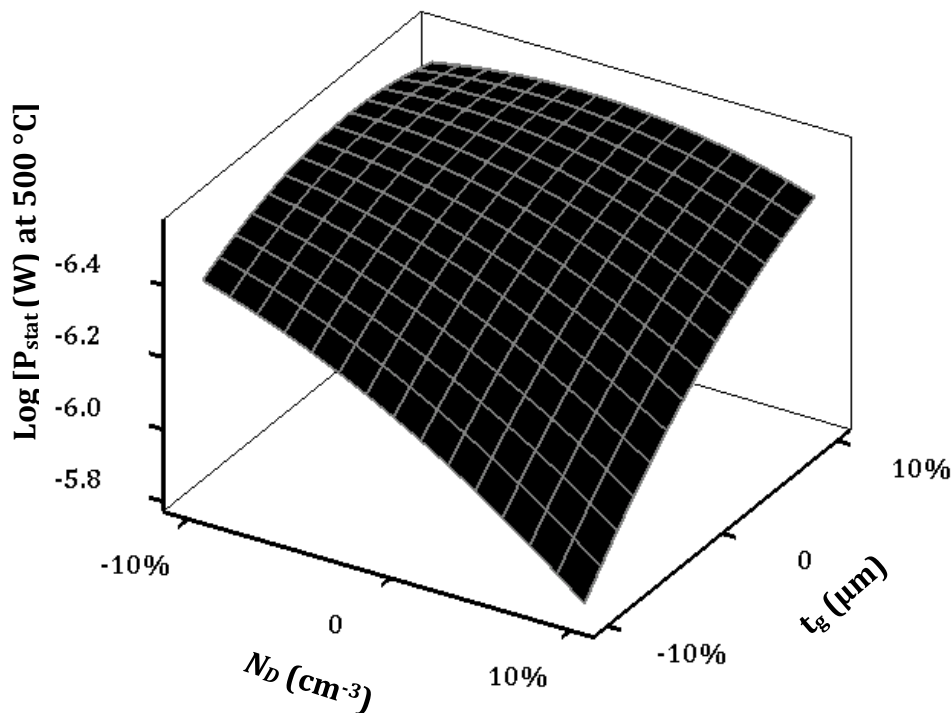


Figure 5.9. RS plot of static power (P_{stat}) at 500 °C as a function of n-JFET parameters, N_D and t_g .

While studying variation in P_{stat} at RT due to process variability, it is observed that the corresponding values of P_{stat} are too small to calculate. Hence, due to software limitations, the variability model for P_{stat} cannot be developed. However, from the variability data set it was apparent that at low t_g and at high N_D , the value of P_{stat} fluctuated from pW to nW. This shows consistency in the

variability of P_{stat} at both RT and 500 °C, in terms of being significantly affected by the device threshold voltage, controlled by the process parameters t_g and N_D .

Temp.	V_t (V) Nominal	Percentage change in V_t from nominal value			
		t_g (+10%)	N_D (-10%)	t_g (-10%)	N_D (+10%)
RT	1.56 V	26%	23%	38%	28%
500 °C	0.48 V	82%	69%	98%	90%

Table 5.3. Summary of variations in threshold voltage (V_t) of the n-JFET as a result of $\pm 10\%$ variations in process parameters t_g and N_D .

From the above analyses of CJFET logic inverter *responses* NM_H , NM_L and P_{stat} , it is evident that t_g and N_D are the two most significant process parameters affecting the inverter's functional stability and energy efficiency at high temperatures. These process parameters control the threshold voltage of enhancement mode SiC JFETs. Variations in t_g and N_D greatly affect V_t (summarised in Table 5.3) and, hence, influence the performance of CJFET logic. Thus, this study suggests that careful control of t_g (which in this case is realised by ion implantation) and uniformity in channel doping concentration (which depends on wafer quality) are the critical process steps in the realisation of enhancement mode SiC JFETs for high temperature CJFET logic.

The effect of process variation on CJFET logic performance can, however, be tackled by adopting the following techniques:

- With the current advance of SiC technology, high quality 4H-SiC substrates and epitaxial wafers are commercially available [22], see Section 2.4.1. Hence, instead of implanted gate JFETs, considered in this study, epitaxial gated devices can be used for high temperature CJFET logic which will reduce the variability in t_g .
- The back gate doping concentration (N_A) was found to be the next major process parameter affecting all of the studied inverter *responses*, both at RT and 500 °C. Hence, adjusting the back-gate biasing can also control the

variations in V_t of enhancement mode JFETs. This provides a back door to tackle post fabrication fluctuations in device performance parameters, most importantly, without the need for adjusting the top gate biasing, which would otherwise seriously deteriorate the performance of CJFET logic circuits. The effect of varying back-gate bias, V_{sub} , on the device performance parameters (V_t , I_{dss} and I_{off}) was discussed in detail in Section 3.4.5.

One of the advantages of SiC JFETs over MOSFETs for high temperature logic devices is that, unlike MOSFETs, JFETs do not have V_t instability issues [23]. This fact has given confidence to various research groups around the world to continue research in high temperature JFETs for use in analogue and digital applications. Furthermore, with the continuing advances in the high temperature SiC wafer quality, with minimum tolerances, it is inevitable that soon SiC CJFET technology will be found in applications for monitoring extreme environments.

5.5 Chapter Summary

In CJFET logic arrays, random variations in manufacturing process parameters can cause significant variations in neighbouring gates or transistors and, therefore, can largely be accountable for poor functional and parametric yield. Using DoE and RSM based statistical approaches, the CJFET logic inverter's stability, in terms of noise margins, and efficiency, in terms of static power dissipation, were modelled and analysed against variability of manufacturing process parameters, at RT and 500 °C. It was found that t_g and N_D have the most significant effect on the studied inverter *responses*. The fluctuation in these process parameters causes variations in device threshold voltage which in turn affects the performance of the logic gate. At 500 °C, the combinational effect of these two parameters was quite high, NM_H (92%), NM_L (159%) and P_{stat} (320%). Hence, this study suggests that careful control of t_g and N_D are the critical process steps in the realisation of enhancement mode SiC JFETs for high temperature CJFET logic. These variations can, however, be tackled by considering epitaxial

gated JFETs over implanted gate devices (which will reduce the variability in t_g) and by adjusting the back-gate biasing (which provides a back door to tackle post fabrication fluctuations in device performance parameters).

5.6 References

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Chapter 6. Conclusions and Future Remarks

6.1 Conclusions

The demand for high performance, energy efficient SiC digital ICs (far greater than a few transistors) for low power applications in extreme environments, requires miniaturisation of device dimensions and reduction of operating biases. With the current advance of SiC technology, such improvements in presently available device prototypes are possible. These improvements require refining, experimentation and perhaps re-design of devices and circuits. This can be achieved with aid of TCAD computer simulations and statistical techniques. Consequently, there is a need for accurate simulation models (based on the physical and material properties of SiC) for device engineers to understand device and circuit behaviour, examine performance trade-offs and verify the manufacturability of the design.

In this work, enhancement mode 4H-SiC JFETs were designed and optimised for high temperature operations; using calibrated TCAD FE computer simulations. Based on these n- and p-JFETs, CJFET logic was described for the first time (to the author's knowledge), evaluating its performance under different operating conditions for low power, complex digital ICs in extreme environments. Finally, the effect of process variations on CJFET circuit performance was studied to identify the key parameters affecting the functional and parametric yield at both room and high temperatures.

Chapter 2 outlined the current advances and challenges faced by SiC technology. The superior material properties, especially the wide bandgap, allow SiC electronics to function across a wide range of high temperature, high radiation and corrosive environments, beyond the scope of narrow bandgap technologies,

such as Si or GaAs. The literature shows the importance of SiC gas sensors for monitoring hostile environments (above 400 °C), such as volcano vents or automotive/aircraft engines, without the need for cooling systems for the support electronics. Consequently, there is a need for high temperature, reliable sensor interface electronics for sensor signal conditioning, digitising and, finally, transmitting the data wirelessly to the base for monitoring.

The issues with reliability and stability of high quality interfaces with SiC crystal limit the functionality of MOSFET, MESFET and BJT device topologies to operation below 400 °C. JFET device topology, on the other hand, has shown to operate reliably for thousands of hours at 500 °C and, hence, is the most suitable structure for high temperature electronics in the nearer term. However, these prototype JFETs are normally-on devices, require high operating bias and have large size. Consequently, the logic gates formed using these prototype JFETs are based on RTL and demonstrate high static power losses. Furthermore, this logic family operates on negative logic voltage levels and require an additional level shifter circuitry to produce correct input voltage levels for succeeding gates. This adds complexity to logic design and results in extra power dissipation in the level shifter circuitry, limiting current SiC logic families to rudimentary functions only. Hence, for high temperature complex logic functions in SiC there is a need for an alternate technology, with low power losses and close to rail output voltage swing. The design and operation of CJFET logic for low power, sense interface electronics was introduced. In Chapters 3 and 4, low power, enhancement mode SiC JFETs and corresponding CJFET logic were evaluated for operation in extreme environments.

Advances in SiC wafer quality, along with the main types of process variations affecting device and circuit performance, were reviewed. Finally, the role of TCAD FE computer simulations and the use of statistical techniques, such as DoE and RSM, for studying process variability and device optimisation were discussed.

In chapter 3, the first comprehensive study, to the author's knowledge, on the development and validation of 4H-SiC model parameters for high temperature, low power FE TCAD simulations was conducted. These model parameters are based on the physical and material properties of 4H-SiC and were derived from published data. The validation of these model parameters were performed using high temperature 4H-SiC lateral JFET data, fabricated and characterised by our group at Newcastle University.

Based on TCAD tools and utilising both DoE and RSM statistical techniques, a systematic methodology was devised to optimise high temperature, four terminal SiC JFETs. Using the calibrated FE simulation model, enhancement mode 4H-SiC (normally off) n- and p-JFETs were optimised for operation in extreme environments. The normally-off nature of these devices is desirable for logic devices in terms of reduced gate drive complexity and power dissipation. Unlike previously reported devices, the optimised SiC JFETs were designed such that not only the gate length was reduced to $2\mu\text{m}$ (in contrast to the $10\mu\text{m}$ reported elsewhere), but were also able to operate over a temperature range of $-50\text{ }^{\circ}\text{C}$ to $600\text{ }^{\circ}\text{C}$ on a fixed voltage of 2V , in contrast to the 20 V used in other work. Furthermore, the drain saturation current of the optimised JFETs were shown to increase with temperature which allowed high on-to-off state current-ratio ($I_{\text{on}}/I_{\text{off}}$) at elevated temperatures. High $I_{\text{on}}/I_{\text{off}}$ is essential for low power logic circuitry with fast switching. At $500\text{ }^{\circ}\text{C}$, $I_{\text{on}}/I_{\text{off}} \sim 10^3$ for optimised (simulated) JFET as opposed to $< 10^2$ (measured) reported elsewhere. This was achieved by the choice of optimal gate bias, $|V_{\text{g}}| = 2\text{ V}$. The fourth, back-gate, terminal in the optimised JFET design provides an alternative route to tackle process variability. The effect of varying back-gate bias (V_{sub}) on the device performance parameters, such as threshold voltage (V_{t}) drain saturation current (I_{dss}) and channel leakage current (I_{off}), was also studied in detail. It was shown that by adjusting the back-gate biasing, the variation in device performance parameters could be controlled. Hence, V_{sub} provides a back door to tackle post fabrication fluctuations in device performance parameters, most importantly, without needing to adjust the top gate biasing.

Using enhancement mode n- and p-JFETs, logic circuitry based on 4H-SiC CJFET technology was described for the first time, to the author's knowledge, in Chapter 4. In order to assess the potential improvements in performance of digital logic functions as a result of using CJFET technology in their implementation, the static and dynamic characteristics of the most basic logic element, namely the inverter were analysed using calibrated FE simulation model. The design and analysis of inverter enables the design of more complex structures, such as NAND, NOR and XOR gates. These complex structures in turn form the building blocks for modules, such as adders, multipliers and microprocessors.

The static and dynamic characteristics of CJFET logic inverter were analysed as a function of operating frequency, temperature, supply voltage and fan-out. At 500 °C, an inverter operating at a supply voltage of 2V showed noise margin high = 0.36 V and low = 0.57 V, undefined region = 0.51 V, propagation delay = 7ns, slew rate = 29.5 V/ μ s, maximum switching frequency = 10.6 MHz and static power = 353 nW. Apart from speed, these static and dynamic characteristics of the CJFET logic inverter, at 500 °C, were found to be comparable to those of silicon and strained silicon technology, at RT. Currently, one of the biggest challenges faced by SiC technology in the development of complex ICs is high static power dissipation at 500 °C ($\sim 10^{-3}$ W). With the supply voltage scaled to 1 V, the static power of CJFET inverter was reduced to 20.6 nW, but at the expense of degrading the noise margin high to 0.15 V and noise margin low to 0.36 V; which could be improved by adjusting the back-gate bias V_{sub} .

In CJFET logic arrays, random variations in manufacturing process parameters can cause significant variations in neighbouring gates or transistors and, therefore, can largely be accountable for poor yield. In Chapter 5, using a DoE and RSM based statistical approach, the effect of ($\pm 10\%$) process variability on the stability of a CJFET logic inverter, in terms of noise margins, and efficiency, in terms of static power dissipation, were modelled and analysed at RT and 500 °C. It was found that the gate implant depth (t_g) and channel doping (N_D) have the most significant effect on the studied inverter *responses*. The fluctuation in these

process parameters causes variations in device threshold voltage which in turn affects the performance of the logic gate. At 500 °C, the combinational effect of these two parameters was quite high, NM_H (92%), NM_L (159%) and P_{stat} (320%). Hence, this study suggests that careful control of t_g (which in this case is realised by ion implantation) and uniformity in channel doping concentration, N_D , (which depends on wafer quality) are the critical process steps in the realisation of enhancement mode SiC JFETs for high temperature CJFET logic. These variations can, however, be tackled by considering epitaxial gated JFETs over implanted gate devices (which will possibly eliminate the issue of t_g variations) and by adjusting the back-gate biasing, V_{sub} , (which provides a back door to tackle post fabrication fluctuations in device performance parameters). Furthermore, with the continuing advances in SiC wafer quality, with minimum tolerances, it is inevitable that soon SiC CJFET technology can be integrated with SiC gas sensors for monitoring extreme environments.

6.2 Future Remarks

The work presented here has shown the potential of SiC CJFET logic devices for operation in high temperature, radiation rich and corrosive environments. The low static power losses demonstrated by CJFET circuits are a key to the challenges faced by current SiC logic families. Hence, the next step would be the fabrication and characterisation of simple logic structures, such as NOT, NAND and NOR gates. This would enable the validation of model parameters for FE TCAD simulations, developed in this work, at a circuit level. Consequently, with the added sophistication to circuit process flow, the simulation model can be used in future studies to analyse the feasibility of much complex structures for operation in hostile environment.

Furthermore, the TCAD simulations and, most importantly, extraction of device and circuit performance parameters demands a lot of time and effort. This problem can, however, be tackled in two distinct ways:

- By developing software code, within the TCAD framework, to automate the parameter extraction of enhancement mode JFETs and resultant circuits.
- Based on previous studies from our group, an analytical model was developed (not included in this thesis) for four-terminal, enhancement mode, SiC JFETs. Incorporating this model into SPICE based simulation tool would greatly improve the time required for circuit simulation and extraction of performance parameters.

The variability study conducted in this work suggested that gate implant depth and channel doping density are the most significant process parameters affecting performance of high temperature CJFET logic inverter. This information helps circuit designers to identify and control key processes from early design phase. Hence, this methodology of modelling and analysing process variability can be extended to study variability in emerging technologies, such as diamond and graphene.

Appendix A

RS Models for Enhancement Mode 4H-SiC n-JFET Characteristics

The model coefficients in this equation are normalised to the coded values of the statistically designed CCD experiment.

$$\begin{aligned} V_{t\ 27^{\circ}\text{C}}(V) = & 2.5098 - 0.0197x_1 + 0.2432x_2 + 0.0596x_3 - 0.1880x_4 \\ & + 0.3758x_5 + 0.0093x_1^2 - 0.0335x_2^2 + 0.0025x_3^2 \\ & - 0.0274x_4^2 - 0.1810x_5^2 - 0.0151x_1x_2 - 0.0037x_1x_3 \\ & + 0.0080x_1x_4 - 0.0107x_1x_5 - 0.0001x_2x_3 + 0.0756x_2x_4 \\ & - 0.1232x_2x_5 - 0.0051x_3x_4 - 0.0052x_3x_5 + 0.1091x_4x_5 \end{aligned} \quad (\text{A1})$$

$$\begin{aligned} I_{DSS\ 500^{\circ}\text{C}}(V) = & -6.6554 - 0.2434x_1 - 0.4833x_2 + 0.0051x_3 \\ & + 0.3527x_4 - 0.5842x_5 + 0.0410x_1^2 - 0.0649x_2^2 \\ & + 0.0221x_3^2 - 0.0135x_4^2 + 0.0488x_5^2 - 0.1036x_1x_2 \\ & + 0.0751x_1x_3 + 0.0838x_1x_4 - 0.1119x_1x_5 + 0.0932x_2x_3 \\ & + 0.0965x_2x_4 - 0.2021x_2x_5 - 0.0679x_3x_4 + 0.0835x_3x_5 \\ & + 0.1377x_4x_5 \end{aligned} \quad (\text{A2})$$

$$\begin{aligned} I_{off\ 500^{\circ}\text{C}}(V) = & -15.0808 - 0.1257x_1 - 1.3167x_2 - 0.2808x_3 \\ & + 1.0369x_4 - 1.6523x_5 + 0.0866x_1^2 + 0.3013x_2^2 \\ & + 0.1460x_3^2 + 0.2034x_4^2 + 0.6782x_5^2 + 0.0321x_1x_2 \\ & + 0.0025x_1x_3 - 0.0149x_1x_4 + 0.0334x_1x_5 + 0.0757x_2x_3 \\ & - 0.3890x_2x_4 + 0.6367x_2x_5 - 0.0585x_3x_4 + 0.1092x_3x_5 \\ & - 0.5181x_4x_5 \end{aligned} \quad (\text{A3})$$

Appendix B

RS Models for CJFET Logic Inverter Characteristics

The model coefficients in this equation are normalised to the coded values of the statistically designed FCCCD experiment.

$$\begin{aligned} NM_{L\ 500\ ^\circ C}(V) &= 0.5618 + 0.0341x_1 + 0.4060x_2 + 0.0162x_3 \\ &\quad - 0.3814x_4 + 0.0821x_5 + 0.0038x_1^2 - 0.0307x_2^2 \\ &\quad + 0.0038x_3^2 - 0.0112x_4^2 - 0.0057x_5^2 - 0.0082x_1x_2 \\ &\quad - 0.0012x_1x_3 + 0.0077x_1x_4 - 0.0023x_1x_5 - 0.0042x_2x_3 \\ &\quad + 0.0680x_2x_4 - 0.0077x_2x_5 + 0.0016x_3x_4 - 0.0012x_3x_5 \\ &\quad + 0.0115x_4x_5 \end{aligned} \tag{B1}$$

$$\begin{aligned} NM_{H\ 300\ ^\circ C}(V) &= 0.6035 - 0.0078x_1 - 0.3428x_2 - 0.0121x_3 \\ &\quad + 0.3161x_4 - 0.0723x_5 + 0.0074x_1^2 + 0.0339x_2^2 \\ &\quad + 0.0084x_3^2 + 0.0149x_4^2 + 0.0039x_5^2 + 0.0022x_1x_2 \\ &\quad - 0.0004x_1x_3 - 0.0031x_1x_4 + 0.0010x_1x_5 + 0.0027x_2x_3 \\ &\quad - 0.0864x_2x_4 + 0.0125x_2x_5 - 0.0022x_3x_4 + 0.0012x_3x_5 \\ &\quad - 0.0159x_4x_5 \end{aligned} \tag{B2}$$

$$\begin{aligned} NM_{L\ 300\ ^\circ C}(V) &= 1.2483 + 0.0076x_1 + 0.4176x_2 + 0.0167x_3 \\ &\quad - 0.3881x_4 + 0.0910x_5 - 0.0057x_1^2 - 0.0523x_2^2 \\ &\quad - 0.0098x_3^2 - 0.0404x_4^2 - 0.0032x_5^2 - 0.0008x_1x_2 \\ &\quad + 0.0011x_1x_3 + 0.0018x_1x_4 - 0.0005x_1x_5 - 0.0048x_2x_3 \\ &\quad + 0.1341x_2x_4 - 0.0202x_2x_5 + 0.0029x_3x_4 - 0.0002x_3x_5 \\ &\quad + 0.0264x_4x_5 \end{aligned} \tag{B3}$$

$$\begin{aligned}
& \text{Log}[P_{stat\ 500\ ^\circ\text{C}}(W)] \\
& = -6.4382 - 0.0110x_1 - 0.1766x_2 - 0.0073x_3 \\
& + 0.1634x_4 - 0.0335x_5 - 0.0154x_1^2 + 0.0835x_2^2 \\
& - 0.0148x_3^2 + 0.0692x_4^2 - 0.0079x_5^2 + 0.0084x_1x_2 \quad (\text{B4}) \\
& + 0.0003x_1x_3 - 0.0073x_1x_4 + 0.0014x_1x_5 + 0.0040x_2x_3 \\
& - 0.1311x_2x_4 + 0.0182x_2x_5 - 0.0039x_3x_4 + 0.0009x_3x_5 \\
& - 0.0153x_4x_5
\end{aligned}$$