Characterisation of Thermal and Coupling Effects in Advanced Silicon MOSFETs

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Abstract

New approaches to metal-oxide-semiconductor field effect transistor (MOSFET) engineering emerge in order to keep up with the electronics market demands. Two main candidates for the next few generations of Moore's law are planar ultra-thin body and buried oxide (UTBB) devices and three-dimensional FinFETs. Due to miniature dimensions and new materials with low thermal conductivity, performance of advanced MOSFETs is affected by self-heating and substrate effects. Self-heating results in an increase of the device temperature which causes mobility reduction, compromised reliability and signal delays. The substrate effect is a parasitic source and drain coupling which leads to frequency-dependent analogue behaviour. Both effects manifest themselves in the output conductance variation with frequency and impact analogue as well as digital performance. In this thesis self-heating and substrate effects in FinFETs and UTBB devices are characterised, discussed and compared. The results are used to identify trade-offs in device performance, geometry and thermal properties. Methods how to optimise the device geometry or biasing conditions in order to minimise the parasitic effects are suggested.

To identify the most suitable technique for self-heating characterisation in advanced semiconductor devices, different methods of thermal characterisation (time and frequency domain) were experimentally compared and evaluated alongside an analytical model. RF and two different pulsed *I-V* techniques were initially applied to partially depleted silicon-on-insulator (PDSOI) devices. The pulsed *I-V* hot chuck method showed good agreement with the RF technique in the PDSOI devices. However, subsequent analysis demonstrated that for more advanced technologies the time domain methods can underestimate self-heating. This is due to the reduction of the thermal time constants into the nanosecond range and limitations of the pulsed *I-V* set-up. The reduction is related to the major increase of the surface to volume ratio in advanced MOSFETs. Consequently the work showed that the thermal properties of advanced semiconductor devices must be characterised within the frequency domain.

For UTBB devices with 7-8 nm Si body and 10 nm ultra-thin buried oxide (BOX) the analogue performance degradation caused by the substrate effects can be stronger than the analogue performance degradation caused by self-heating. However, the substrate effects can be effectively reduced if the substrate doping beneath the buried

oxide is adjusted using a ground plane. In the MHz – GHz frequency range the intrinsic voltage gain variation is reduced ~6 times when a device is biased in saturation if a ground plane is implemented compared with a device without a ground plane.

UTBB devices with 25 nm BOX were compared with UTBB devices with 10 nm BOX. It was found that the buried oxide thinning from 25 nm to 10 nm is not critical from the thermal point of view as other heat evacuation paths (e.g. source and drain) start to play a role.

Thermal and substrate effects in FinFETs were also analysed. It was experimentally shown that FinFET thermal properties depend on the device geometry. The thermal resistance of FinFETs strongly varies with the fin width and number of parallel fins, whereas the fin spacing is less critical. The results suggest that there are trade-offs between thermal properties and integration density, electrostatic control and design complexity, since these aspects depend on device geometry. The high frequency substrate effects were found to be effectively reduced in devices with sub-100 nm wide fins.

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List of abbreviations

2D	Two-dimensional
3D	Three-dimensional
AC	Alternating current
BEOL	Back end of line
BOX	Buried oxide
CESL	Contact etch stop layer
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DIBL	Drain induced barrier lowering
DUT	Device under test
EOT	Equivalent oxide thickness
FDSOI	Fully depleted silicon-on-insulator
FET	Field effect transistor
FinFET	Fin field effect transistor
GAA	Gate-all-around
GP	Ground plane
GSG	Ground-signal-ground
HDD	Highly doped drain
ITRS	International technology roadmap for semiconductors
LDD	Lightly doped drain
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field effect transistor
PDSOI	Partially depleted silicon-on-insulator
RDF	Random dopant fluctuation
RF	Radio frequency
SOI	Silicon-on-insulator
UTB	Ultra-thin body
UTBB	Ultra-thin body and buried oxide
VNA	Vector network analyser
ZTC	Zero temperature coefficient

List of symbols

A	Area
A_v	Intrinsic voltage gain
C_{dd}	Total drain capacitance
C_{ij}	Capacitance between terminals i and j
C_{ox}	Gate dielectric capacitance
C_{Sub}	Substrate capacitance
C_{th}	Thermal capacitance
d_s	Shielding distance
f	Frequency
f_{th}	Characteristic thermal frequency
g_d	Output conductance
g_{d0}	Output conductance at low frequency
g_{dT}	Output conductance at high frequency
g_{ij}	Conductance between terminals i and j
g_m	Transconductance
$g_{m\text{-}max}$	Transconductance maximum
$g_{m\text{-}max\text{-}norm}$	Normalised transconductance maximum
H_{fin}	Fin height
I_d	Drain current
I_{d0}	Drain current at T_0
I-V	Current-voltage
k	Factor of mobility degradation with temperature
k_B	Boltzmann constant
k_{Si}	Thermal conductivity of Si
k_{SiO2}	Thermal conductivity of SiO_2
L_g	Gate length
L_{SD}	Source and drain extension length
m	Inverse of the thermal healing length
n	Body factor
N_{fin}	Number of parallel fins per finger
q	Elementary charge
R_{S+D+G}	Parasitic series resistance

R_{th}	Thermal resistance
$R_{th\text{-}BOX}$	Thermal resistance of BOX
S_{fin}	Fin spacing
T	Temperature
T_0	Reference temperature
T_A	Ambient temperature
t_{BOX}	BOX thickness
T_{ic}	Interconnect temperature
t_{ox}	Gate oxide thickness
t_{Si}	Si thickness
t_{Sub}	Substrate thickness
V_d	Drain voltage
V_{EA}	Early voltage
V_g	Gate voltage
V_{th}	Threshold voltage
W	Width
W_{fin}	Fin width
W_g	Gate width
x	Coordinate along horizontal axis
Z_{th}	Thermal impedance
$\Delta g_{d\text{-}SH}$	Output conductance transition amplitude due to self-heating
$\Delta g_{d\text{-}SUB}$	Output conductance transition amplitude due to substrate effects
ΔT	Temperature rise
ε_0	Vacuum permittivity
ε_{Si}	Relative permittivity of Si
ε_{SiO2}	Relative permittivity of SiO_2
κ	Scaling constant
μ	Mobility
μ_{eff}	Effective mobility
μ_{eff0}	Effective mobility at T_0
τ_g	Gate delay
τ_p	Pulse width
τ_{th}	Thermal time constant
ω	Angular frequency

Chapter 1. Introduction

The transistor is the main building block of an integrated circuit. The principle of the first field effect transistor (FET) was patented by Julius Edgar Lilienfeld in 1925 [1]. The first transistor ever constructed was a Ge-based bipolar point-contact transistor in 1947 at Bell Telephone Laboratories by William Shockley, John Bardeen, and Walter Brattain [2]. The first Si-based transistor was demonstrated in 1954 by Gordon Teal of Texas Instruments [3]. And the first Si-based metal-oxide-semiconductor field effect transistor (MOSFET) was demonstrated by Dawon Kahng and Martin Atalla at Bell Labs in 1959 [4]. The next important step for the Si-based electronics was fabrication of the first MOS integrated circuit in 1963. Now the MOSFET is a cornerstone of the electronics market, and Si is the main building material of modern transistors due to its abundance, low cost and its physical properties.

1.1 MOSFET and its regimes of operation

This section describes the operation of an enhancement mode (normally off) nMOSFET. To understand the principle of a pMOSFET operation, n-type dopants have to be substituted with p-type dopants, electrons with holes, positive terminal voltages with negative and vice versa.

A schematic representation of an nMOSFET is shown in Figure 1.1. Generally, a MOSFET has four terminals: gate, source, drain and substrate. Source and drain are formed by heavy n-type (n^+) doping of the Si substrate which is doped with p-type impurities. The area between the source and the drain is used as the device active region where the current flows. The gate terminal is formed from poly-Si (or metal) and is separated from the device active region by a thin layer of dielectric.

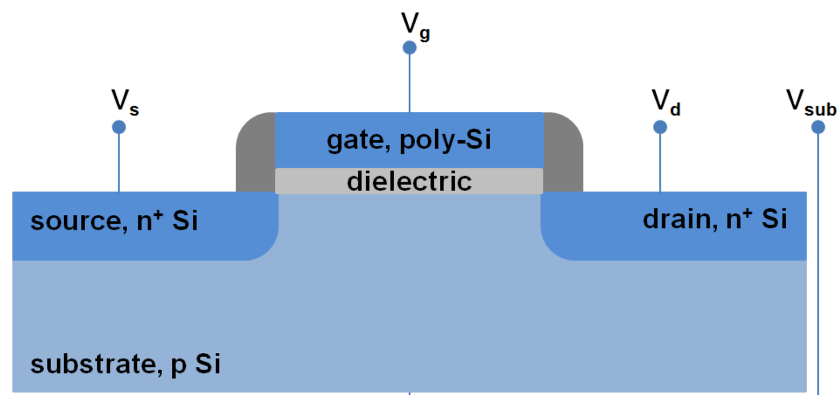

Figure 1.1. Schematics of a four-terminal n-channel MOSFET.

As the substrate is p-type doped, holes are the majority carriers in the device active region (between the source and the drain) when no voltage is applied to the gate. As the positive gate voltage is applied to the gate terminal, due to electrostatic forces, holes are repelled from the active region, thus forming a depletion layer. A further increase of the gate bias leads to the attraction of negatively charged electrons. At a certain gate voltage (threshold voltage, V_{th}) the concentration of electrons in the active region is equal to the concentration of holes in the substrate (roughly equal to the concentration of p-type impurities in the substrate). The layer of electrons on the surface of the semiconductor under the gate dielectric forms an inversion layer. The polarity of this layer is the same as the polarity of the source and drain regions. Therefore, the current can flow between the source and drain terminals (drain current, I_d), if the drain bias (V_d) is higher than the source bias.

Practically, in many applications the source and the substrate terminals are grounded. The gate and the drain voltages are defined as potentials on the terminals with respect to the source terminal which is grounded.

The gate voltage controls conductivity of the channel and therefore the drain current of a MOSFET. The drain current is governed by two mechanisms – drift and diffusion. The diffusion mechanism dominates in the subthreshold regime ($V_g < V_{th}$) and the current flows due to the difference in electron concentration. In the subthreshold regime the drain current varies with the gate voltage exponentially:

$$I_d \propto e^{\frac{qV_g}{nk_BT}}, \tag{1.1}$$

where I_d is the drain current, q is the elementary charge, V_g is the gate voltage, n is the body factor, k_B is the Boltzmann's constant and T is the temperature.

The drift mechanism dominates when the gate voltage is above the threshold ($V_g > V_{th}$). Therefore, the drain current is governed by the electric field. When the drain voltage is smaller than the gate overdrive ($V_d < V_g - V_{th}$) and the gate voltage is above the threshold ($V_g > V_{th}$) the drain current linearly depends on the gate voltage:

$$I_d = \frac{W_g}{L_g}\mu C_{ox}\left(V_g - V_{th} - \frac{1}{2}V_d\right)V_d, \tag{1.2}$$

where W_g is the gate width, L_g is the gate length, μ is the mobility and C_{ox} is the gate dielectric capacitance.

When the drain current exceeds the gate overdrive ($V_d \geq V_g$ - V_{th}, $V_g > V_{th}$), the regime of operation is called the saturation regime. In the saturation regime in long channel MOSFETs, the drain current is drain voltage independent:

$$I_d = \frac{W_g}{2L_g} \mu C_{ox} \left(V_g - V_{th}\right)^2. \tag{1.3}$$

The above models expressed in Equations 1.1-1.3 are valid for long channel MOSFETs. These models can be further extended in order to account for the short channel effects (such as the channel length modulation).

1.2 Moore's law and scaling

For the past few decades the semiconductor industry has been driven by Moore's law. According to Moore's law, the number of transistors per chip doubles approximately every two years. It follows Gordon Moore's publication in 1965 where the trend was predicted [5]. Moore's law can be extended to predict other parameters, many of which roughly improve exponentially with time. Examples include transistor cost, transistor speed and memory capacity. Moore's law has been possible due to constant miniaturisation of device dimensions.

This scaling has been dictated by the need of highly-integrated digital circuits. The scaling rules which enable reduction of the device dimensions were outlined in [6] in 1974. At that time integrated circuits in production featured 5 μm gate length MOSFETs. The steady reduction of device dimensions led to improved circuit speed, integration density and lower power consumption. According to the scaling rules in [6], the gate width, gate length, gate dielectric and supply voltage must be scaled by a factor of κ which is a scaling constant. The doping concentration has to be increased by κ. This leads to the drain current, gate capacitance and gate delay reduced by a factor of κ. Power density is not scaled, but the power dissipation reduces by a factor of κ^2. The scaling rules are summarised in Table 1.1.

Table 1.1. Summary of the scaling rules outlined in [6].

Parameter	Scaling factor
Gate dielectric thickness	$1/\kappa$
Gate length	$1/\kappa$
Gate width	$1/\kappa$
Doping concentration	κ
Supply voltage	$1/\kappa$
Drive current	$1/\kappa$
Gate capacitance	$1/\kappa$
Gate delay	$1/\kappa$
Power density	1
Power dissipation	$1/\kappa^2$

Scaling transistor dimensions using the rules outlined in [6] had been possible until the technology entered sub-100 nm regime. Further reduction of device dimensions is complicated due to intrinsic physical limitations which lead to short channel effects, high current leakage through gate dielectrics, high series resistances and low mobility due to interface effects and extremely high doping levels.

International Technology Roadmap for Semiconductors (ITRS) [7] outlines technological requirements for the evolution of the semiconductor industry. In order to satisfy these requirements, new scaling strategies are adopted. The most common strategies to address the scaling challenges include the introduction of new materials such as high-κ gate dielectrics and metal gates, silicon on insulator (SOI) technology, strain engineering, alternative device architectures, III-V materials, tunnel FETs and other.

This work concentrates on some aspects of SOI technology which is discussed in the next section.

1.3 Silicon-on-insulator

SOI technology is reputed as a promising approach to meet ITRS requirements on MOSFET downscaling [7]. SOI allows a reduction of parasitic capacitances and leakage currents and better control of short channel effects by placing a layer of insulator (buried oxide, BOX) under the device active region. Chips built on SOI platforms are faster and more energy-efficient [8] than conventional MOSFETs on bulk Si, while design flows for SOI devices remain similar to those

used for bulk complementary MOS (CMOS). SOI technology also reduces the number of fabrication steps compared with conventional bulk technology because separate n-well and p-well formation for SOI CMOS is not required.

Devices on SOI platforms can be of two forms – partially depleted (PDSOI) and fully depleted (FDSOI). Full or partial depletion of the channel is determined by the Si thickness and its doping level. PDSOI devices are prone to floating body effects (avalanche ionisation at the drain resulting in charge accumulation in quasi-neutral region) whereas the absence of mobile charges in FDSOI prevents any floating body effects. PDSOIs in production are now approaching their physical limits whereas FDSOI technology is more scalable. Therefore, the main focus of the work is placed on FDSOI devices.

1.4 Fully depleted silicon-on-insulator: UTBB and FinFETs

FDSOI devices can be classified in two forms: planar and non-planar. Planar or two-dimensional devices are similar to conventional bulk MOSFETs where a device is manufactured layer by layer. In contrast, a non-planar device cannot be implemented using layer by layer manufacturing processes and requires consideration of three-dimensional (3D) structures.

Planar FDSOI devices are devices built on the SOI platform with body thickness sufficiently small to achieve full depletion in the body. The state of the body is also controlled by the channel doping level. Lower doping allows for full depletion at lower gate voltages. In advanced FDSOI devices typically no channel doping is used. Due to the very thin Si channel (few nm) planar FDSOI transistors are called ultra-thin body (UTB) devices. For further improvement of UTB devices, the BOX also has to be scaled down significantly. Such devices with an ultra-thin body and ultra-thin BOX are referred to as UTBB in this work. UTBB devices are a special case of UTB devices. In different literature sources UTBB technology is also called UT2B [9], [10], UTB^2 [11], [12], UTBOX [13–15], ETSOI (extremely thin SOI) [16–19], UTSOI (ultra-thin SOI) [20], [21] and SOTB (Si on thin BOX) [22], [23].

Non-planar FDSOI devices can be of various forms depending on the shape of the channel. The most common 3D architectures are FinFETs, tri-gate, pi-gate, omega-gate and gate-all around. Different architectures are schematically shown in Figure 1.2. In this work FinFETs are discussed as these are the most common form of 3D architecture devices. However, in most of the cases the discussion is also valid for other devices, e.g. omega-gate devices. Some FinFETs in the case of imperfectly controlled fabrication processes might have slight features in common

with omega-gate devices (gate extruding under the channel). Generally, non-planar devices can be referred to as multi-gate devices. In multi-gate devices the gate electrode is situated on more than one side of the channel. In some cases of planar design a device might have two gates – one top gate (or front) and one bottom (or back) gate.

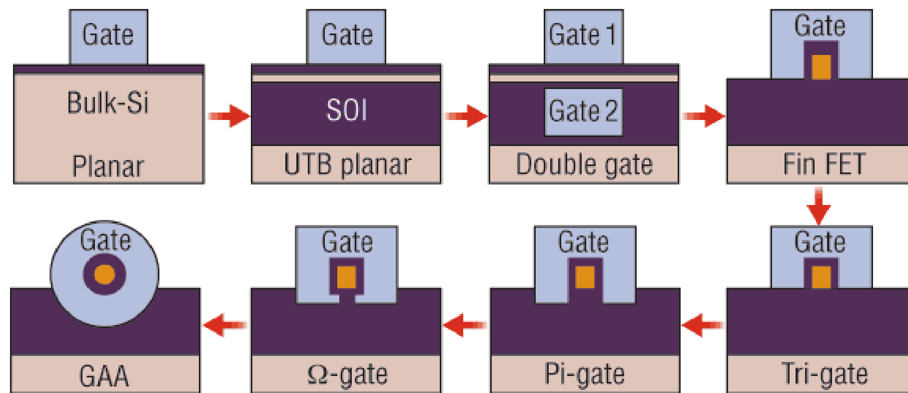

Figure 1.2. Different device architectures from planar bulk MOSFET to gate-all-around [24].

To highlight the difference between a planar UTB device and a non-planar FinFET device, two illustrations can be used. A FinFET can be viewed as a UTB device with the channel turned by 90 degrees while other device features remain the same. Alternatively, a UTB device can be imagined as a special case of a FinFET with fin width much higher than the height of the fin. The latter case can be especially relevant to some UTB devices that might have features of FinFETs. Due to very small dimensions and imperfections during the fabrication process the gate might slightly extend and cover the sidewalls of the body thus leading to some similarities with a FinFET.

Due to small device dimensions, the number of dopants in the channel of an advanced MOSFET is limited to few atoms per device. Because of the doping process nature, the total number of dopants and their location within a device are prone to randomness. Fluctuation in the number of dopants in the channel is translated into variation of the threshold voltage and, consequently, into the variation of the on-state current. Its detrimental effect was shown for FinFETs [25] and for UTB devices [22], [26]. Random dopant fluctuation (RDF) can be overcome in FDSOI devices by leaving the channel undoped [27]. This simplifies the fabrication process, reduces inter-die and intra-die threshold voltage variability, and enhances carrier mobility through reduced impurity scattering.

FDSOI devices can operate in the volume inversion regime. In the volume inversion regime the channel is formed not at the gate dielectric-Si body interface, but deeper in the Si body. As

the channel is formed further from the interface, the carrier mobility is improved due to reduced interface scattering. The full channel depletion and gate proximity result in better charge control in the channel by the gate. Therefore, FDSOI technology enables a reduction of short channel effects, parasitic off-state current and improvements in power consumption.

According to ITRS, FDSOI technology is expected to provide at least another three generations of Si MOSFETs [7], [28]. However, there is an ongoing debate in the semiconductor community on the design of these future generations. FinFETs and UTB devices present two considerably different approaches to device fabrication. Each of them has its own advantages and drawbacks. These are mainly related to the performance, scalability and manufacturability of FDSOI devices which are discussed in the next sections for UTBB MOSFETs and FinFETs separately.

1.5 UTBB

Figure 1.3 shows a schematic image of a planar UTB device. In UTBB devices the thickness of the BOX is comparable to the thickness of the Si body (10-25 nm).

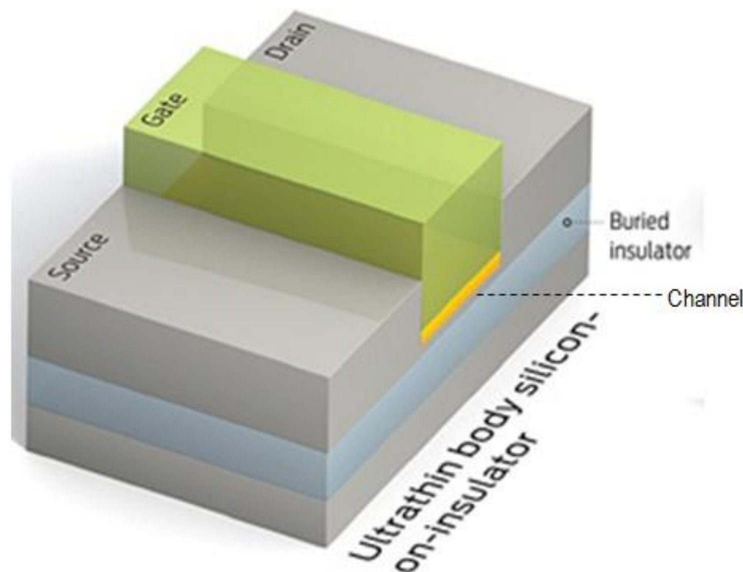

Figure 1.3. Schematic image of a planar UTB MOSFET [28].

1.5.1 Fabrication

In order for the gate to have better control of the charges in the UTB MOSFET active region, silicon body thinning is required, approximately to $t_{Si} < L_g/4$ [18], where t_{Si} is the silicon body thickness and L_g is the gate length. This restriction can be alleviated by optimisation of the gate

workfunction [29], e.g. by scaling the gate dielectric or increasing channel doping. However, the dielectric thickness reaches its limits due to tunnelling and the channel doping is undesirable due to mobility reduction and compromised variability (as discussed in Section 1.4).

In order to control parasitic lateral drain and body coupling, the BOX thickness must also be scaled approximately to $t_{BOX} < L_g/2$, where t_{BOX} is the BOX thickness and L_g is the gate length [30]. Moreover, thin BOX allows charge control from the back gate [10], [15], [31] which can be a useful method to tune the threshold voltage of transistors by adjusting doping under the BOX and carefully selecting bias applied to the back gate [32].

One of the advantages of UTBB technology over the conventional bulk CMOS process arises from the reduction of fabrication steps. Firstly, as it was mentioned in Section 1.3, no separate n-well or p-well formation is necessary for SOI devices. UTBB devices can be realised using a thin BOX wafer or localised SOI process [33], [34]. Secondly, the channel is left undoped which saves a number of fabrication steps and no implant damage is caused. In [28] it was suggested that leaving channel undoped in UTBB saves 20-30 steps out of ~400 in the wafer production process. Halo implants are also not required in UTBB devices [16]. Thirdly, it was reported in [16] that the number of mask levels required to form raised source and drain regions is reduced from four in the bulk process to one in the UTBB process. UTBB fabrication also benefits from simpler isolation, lower number of masks and reduced fabrication complexity, which can potentially compensate for the high cost of a UTBB wafer [16].

In [16], [35] it was shown that UTBB technology is compatible with strain engineering. It was demonstrated in [16] that integration of SiGe raised source and drain for pFET and Si:C raised source and drain for nFET provides considerable channel stress as high as 500 MPa and therefore performance improvement up to 15% in the drive current. In [35] 12% enhancement of the on-state current is demonstrated in UTBB devices with 20 nm thick BOX and tensile contact etch stop layer (CESL) technology.

As mentioned above, UTBB technology allows for back-biasing. This can be achieved by doping the substrate under the ultra-thin BOX (ground plane). Implementation of the ground plane is a relatively simple step and does not add much complexity to the fabrication process [13], [36]. The challenge in the ground plane realisation is to create an abrupt doping profile under the BOX. Also, in order to apply bias to a ground plane, an additional contact has to be implemented. This adds complexity to the layout of metallisation. Also, parasitic resistance and capacitance of such a connection would require additional considerations, especially at high frequencies.

The main challenges in UTBB fabrication arise from high variability and uniformity issues. Sources of variability in nanoscale CMOS devices arise from RDF, line edge roughness, poly-Si granularity, oxide thickness fluctuation [26] and Si channel thickness fluctuation [16], [17]. In [26] it was concluded that the RDF is the main source of the performance variability in nanoscale MOSFETs. As discussed above, the channel is left undoped to avoid RDF and improve variability. However, RDF can arise from the doping in the gate [26], [37] or a ground plane [33], if the ground plane is implemented. RDF of a ground plane is more severe in devices with a thinner BOX than in devices with a thicker BOX due to the ground plane proximity to the channel.

It was shown empirically that the threshold voltage variation is linked to the variation in Si body thickness. It was quantified in [16], [17] and was found to be 25 $mV \cdot nm^{-1}$. However, in [22] a much lower value of ~2 $mV \cdot nm^{-1}$ was reported for a UTBB device with 25 nm gate length. It was also concluded in [22] that the variation of the Si thickness is a much less critical parameter in affecting the threshold voltage variation than the gate length variation or RDF. The global variation of the threshold voltage can be corrected by applying voltage to the substrate [32]. However, application of the substrate voltage might compromise the benefits of UTBB devices which are designed to improve power issues.

In order to limit threshold voltage variation, restriction of the Si thickness fluctuation is set to 1 nm for UTBB devices [38]. It was reported in [21], [38] that 0.5 nm uniformity is already available and 0.2 nm uniformity is achievable with Soitec Smart Cut technology. Figure 1.4 shows the Smart Cut process schematically. The Si wafer A is oxidised in order to create the thin layer of SiO_2. Then H^+ ions are implanted in the wafer A in order to create a weakened layer. Then the wafer A is cleaned and bonded to the Si wafer B. The cleavage takes place at the depth of the mean penetration depth of the implanted H^+ ions. The thin layer of the buried oxide is bonded to the wafer B which can be used for UTBB fabrication. The wafer A can be reused for another process.

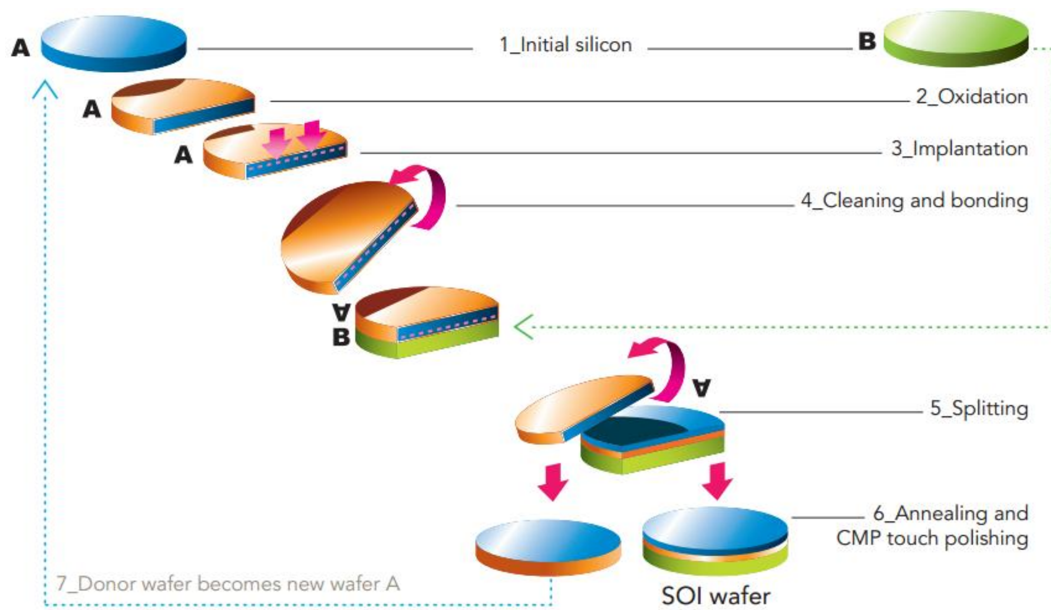

Figure 1.4. Soitec Smart Cut process [39].

Due to ultra-thin layers and ultra-small dimensions the parasitic leakage currents must be considered. This is relevant to all miniature devices. However, in the case of devices with an ultra-thin BOX special care must be taken with leakage through the BOX to the substrate. The substrate leakage may occur if metallisation is not well controlled and the metal spikes go through the source or drain regions and through the ultra-thin BOX, thus shortening the source or drain with the substrate.

Another challenge is Si consumption during the UTBB fabrication process which has to be accounted for. In order to achieve targeted 6-7 nm Si channel thickness as required for the 22 nm technological node the starting Si thickness has to be ~12 nm [21].

Ultimately, the Si body thickness may be limited to 5 nm due to the source and drain resistance as was suggested in [40]. The high series resistance in UTB devices arises from the reduced cross-section of the Si body in UTB (and consequently UTBB) devices. Raised sources and drains can be implemented in order to improve the series resistance. However, this leads to increase of the overlap capacitance.

According to estimations by Mark Bohr from Intel UTBB wafers can add ~10% to the cost of finished wafer [28] due to supply limitations. However, the SOI consortium suggests that UTB SOI wafers will be less expensive [28]. In [21] it was suggested that in the back end of the line finished SOI wafers are comparable or might be even cheaper due to the simplified fabrication process.

1.5.2 Performance

Electrostatics, scalability and variability issues in UTBB MOSFETs as well as their perspectives for low power digital applications are widely discussed in the literature [10–12], [14], [15], [21], [22], [33], [41], [42]. UTBB technology offers excellent control of the short channel effects: threshold voltage roll-off, drain induced barrier lowering (DIBL) [33], reduced off-state current compared with bulk [21] and small threshold voltage variability [33].

Analogue figures of merit of UTBB devices have so far received little attention. There was only one work in this field [43]. However, it is mostly dedicated to UTB MOSFETs with thick BOX. Also, it mostly focuses on RF figures of merit without consideration of the wider frequency range starting from DC.

Numerical simulations predict a degradation in analogue performance due to the substrate effects (parasitic source and drain coupling through the substrate) being more severe in devices employing thinner BOX if the substrate doping is not adjusted [44]. It is anticipated that the introduction of a heavily doped ground plane underneath the BOX in UTBB MOSFETs will help suppress substrate-related output conductance increases and hence reduce analogue performance degradation over the wide frequency range. Incorporating a ground plane should also allow threshold voltage modulation for memory cells [14], low-power applications [15] and further reduce DIBL [30].

It was demonstrated in [45] that a double-gate regime in UTBB devices allows better control of the short channel effects due to improved gate-to-channel coupling. Additionally, the double-gate regime enhances transconductance, drive current and intrinsic gain of UTBB SOI MOSFETs. However, in [45] the double-gate regime was implemented by connecting the bottom of the wafer and the gate together. As the Si substrate and the BOX are much thicker than the gate oxide, such a regime of operation is asymmetric. Therefore the gate terminal has more control over the channel than the substrate terminal. In order to provide more control to the substrate terminal (to make the regime more symmetric) or tune the threshold voltage, a bias has to be applied to the ground plane.

1.6 FinFETs

Evolution of the architecture of MOSFETs follows the increase of the number of gates as shown in Figure 1.2. The conventional planar device has one gate while more advanced architectures incorporate multiple gates and non-planar design for better control of the charge in

the channel. However, manufacturability, device and cross-wafer uniformity, high access resistances and capacitances and self-heating are challenges for multiple-gate MOSFET architectures [43], [46–50]. A schematic representation of a FinFET is shown in Figure 1.5.

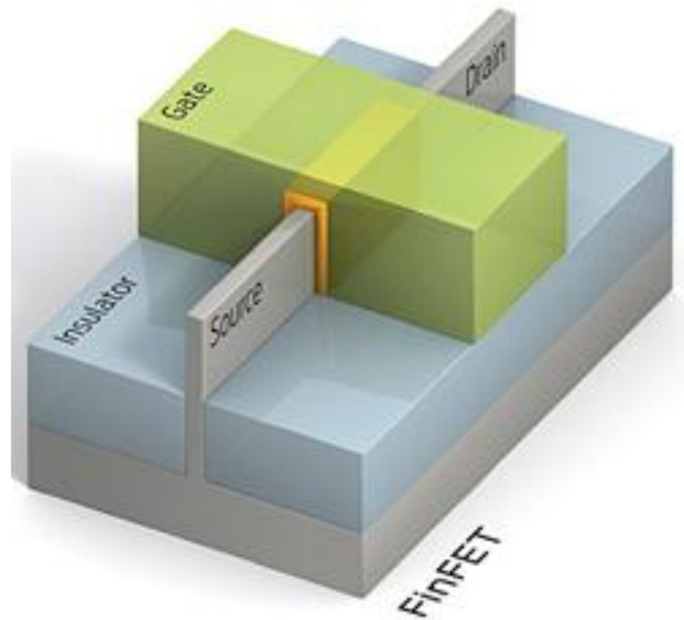

Figure 1.5. Schematic representation of a FinFET [28].

1.6.1 Fabrication

As explained in Section 1.4, one of the main advantages of FinFET technology is its multi-gate design which results in more current per unit of chip area. However, the multi-gate architecture can also be implemented by means of planar technology. Double-gate planar UTB MOSFETs demonstrated improved mobility due to the volume inversion regime [51]. However, their fabrication process introduces complexities related to the alignment of the top and bottom gates [52], [53]. Although a FinFET is a multi-gate device, the alignment problem is solved as a single gate material is deposited over the fin.

As it was discussed in Section 1.5.1, BOX thickness uniformity is a critical parameter for UTBB technology which has to be precisely controlled. Furthermore, there are a limited number of suppliers of wafers for UTBB manufacturing. In contrast to UTBB devices, FinFETs can be manufactured on widely available SOI wafers [21]. Such wafers have a thick BOX (typically 145 nm) and are in mass production for PDSOI devices. Therefore, BOX thickness uniformity is not a critical parameter in FinFETs. Furthermore, any impact of BOX thickness can be eliminated if FinFETs are built on bulk wafers [54–56]. Bulk FinFETs feature improved thermal properties

and reduced defect density. However, bulk FinFETs suffer from increased leakage, fabrication complexity and reduced circuit speed [54], [57].

In all previous device generations, the gate length was the smallest feature defined by lithography. However, in FinFETs, due to their non-planar nature, the smallest feature which has to be defined by lithography is the fin width. The width of the fin defines the thickness of the body which is a critical parameter for the control of short channel effects. In order to have good gate control of the charge in the channel, the fin width W_{fin} has to be scaled as $W_{fin} < L_g/2$ [58], [59]. Note, that in case of UTBB devices, this requirement is stricter as the body thickness has to be approximately a quarter of the gate length (Section 1.5.1). In FinFETs the body thickness requirement is relaxed because the gate wraps the channel. This suggests that ultimately, FinFETs can be more scalable than their planar counterparts.

The fin width is an important parameter of a FinFET due to its impact on device performance. The off-state current reduces as the fin width decreases due to improved gate control over the charge in the channel [58]. The fin width also affects the carrier mobility [60] and the threshold voltage [61], [62].

Lee *et al.* at the Korea Advanced Institute of Science and Technology demonstrated a FinFET with a gate length of 5 nm and fin width of 3 nm [63]. Electron beam lithography was used to define the fin. This work demonstrated the potential of FinFET technology for scaling into sub-5 nm regime. Obviously, fabricating many identical transistors and cramming them on a chip is more challenging than demonstrating only a single transistor. The very important uniformity and variability issues have to be resolved.

Uniformity of the fin is one of the main fabrication challenges that have to be addressed in FinFETs. The fin has to be manufactured as uniformly as possible. The uniformity has to be maintained during all fabrication steps which follow after the fin definition. For example, gate material deposition should be well controlled in order not to incur any damage to the fin. The die-to-die and wafer-to-wafer uniformity of the fin width and height is required. The cross-wafer uniformity is especially challenging in large 300 mm wafers.

The fin width can be defined using optical [64] or, most commonly, electron beam lithography [54], [63], [65]. However, in both cases the line edge roughness [66], [67] and uniformity have to be considered. The quality of the surface and the crystal orientation are crucial because the channels are formed on the sides of the fins [68].

Though channel doping in FinFETs is not required, thus solving the problem of RDF, doping is needed for source and drain regions. Due to 3D architecture and high fin density, fins might cast shadows [69], [70]. This results in uneven distribution of dopants and an increase of the resistance.

Another consideration in FinFET fabrication arising from its 3D architecture is the high aspect ratio [71] which limits the fin height at a fixed fin width. Due to limitations imposed by high aspect ratios, real-life FinFETs feature trapezoidal channel cross-section rather than rectangular. The inclination angle of the fin sidewalls impacts on the device electrical performance parameters such as threshold voltage, output conductance, transconductance, intrinsic gain and others [72–74]. This case confirms again that the FinFET fabrication has to be carefully controlled.

According to estimations by Mark Bohr from Intel 3D transistors add 2-3% to the cost of the finished wafer [28].

1.6.2 Performance

Multiple gate architectures including FinFETs are renowned for good electrostatic control, good subthreshold slope, low leakage current, suppressed short channel effects, higher transistor density and compatibility with other scaling strategies such as strain and high-κ [71], [75–77].

Due to the three-dimensional architecture, FinFETs have channels formed from more than two sides than their planar counterparts. Therefore, FinFETs feature effectively wider gates. This translates into a larger drain current per unit of chip area. In a circuit the output current of one transistor is used to switch on the next transistor by charging its gate capacitor. Improvement of the drain current results in the faster charging of the capacitance which positively reflects on the circuit speed according to:

$$\tau_g = C_g \frac{V_d}{I_d}, \tag{1.4}$$

where τ_g is the gate delay, C_g is the gate capacitance, V_d is the supply voltage and I_d is the drive current.

Figure 1.6 compares the normalised gate delay in 22 nm-node FinFETs and 32 nm-node planar MOSFETs as presented by Intel in [78]. The experimental results were obtained on various microprocessor circuit types. The 32 nm-node results were normalised to 1 at 1.0 V operating voltage. From the gate delay perspective, 22 nm-node FinFETs by Intel are 37% faster

than previous 32 nm-node planar technology chips at the constant supply voltage of 0.7 V. At higher operating voltage of 1.0 V, the improvement reduces to ~18%. Such speed enhancement can be traded off against the operating voltage, thus significantly reducing the power.

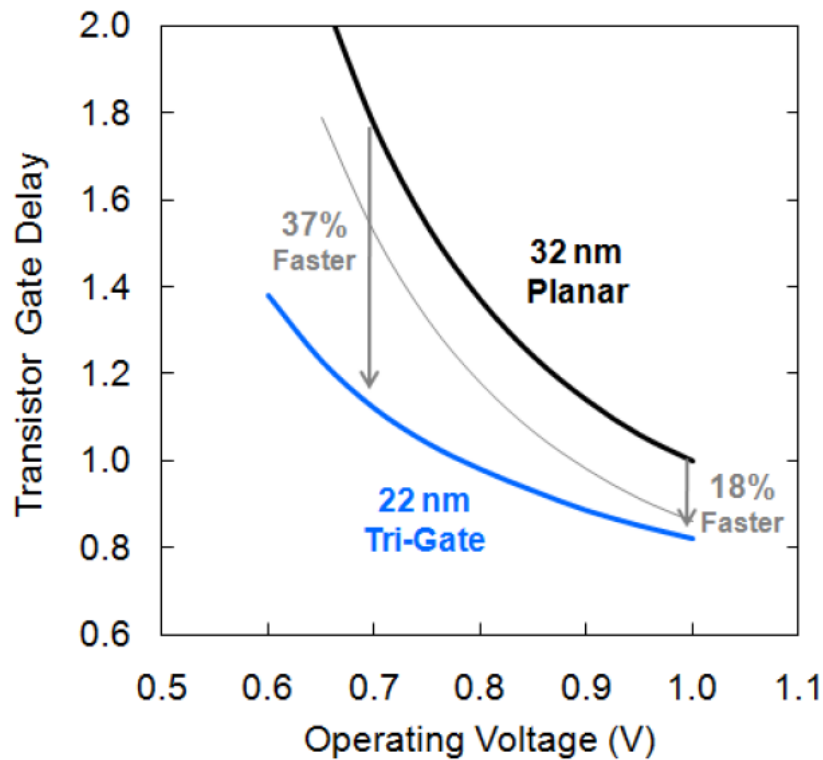

Figure 1.6. Normalised gate delay in 22 nm-node FinFETs and 32 nm-node planar MOSFETs [78].

1.7 Self-heating

Advanced semiconductor devices and particularly SOI MOSFETs are prone to self-heating. This section describes what self-heating is and why it is detrimental for device performance. Previous work on self-heating in both FinFETs and UTBB devices is reviewed.

1.7.1 Origin

Self-heating is heat accumulation in the channel at high power levels. Self-heating in semiconductor devices arises due to device scaling, high current densities and use of materials with low thermal conductivity. Materials such as SiO_2 or SiGe conduct heat significantly worse than Si [79]. If SiO_2 underlies the device channel as in SOI devices (BOX) or surrounds the channel as in the case of FinFETs or GAA, effective heat dissipation from the channel is impeded. The thermal conductivity of SiO_2 is ~1.4 $W \cdot m^{-1} \cdot K^{-1}$, which is about two orders of

magnitude lower than that of bulk Si, ~148 $W \cdot m^{-1} \cdot K^{-1}$ [79]. Self-heating can also be observed in strained Si devices, where strain is globally induced by a SiGe layer under the channel. SiGe thermal conductivity is also significantly lower than in Si. Depending on the Ge fraction in the SiGe, the thermal conductivity can be ~20 times lower than in Si. Thermal conductivity of bulk high-κ dielectrics, e.g. HfO_2 is the same order of magnitude as that of SiO_2. However, films of HfO_2 only a few nm thick exhibit much lower thermal conductivities, in the order of 0.3-0.5 $W \cdot m^{-1} \cdot K^{-1}$ [80]. The low thermal conductivity of high-κ gate dielectrics can contribute to the elevated self-heating in advanced semiconductor devices.

Scaling and reduction of device dimensions also lead to poorer device thermal properties. Increase of the current densities with device downscaling results in higher power densities. Also, interface effects are playing much more important role as device dimensions reduce. Thermal conductivity of Si and SiO_2 reduces dramatically from its bulk value as the device dimensions enter the nanometre regime [79], [81], [82]. In FDSOI technology the thermal conductivity of an ultra-thin Si layer which acts as the channel is aggravated due to the close proximity of the additional interface and confinement. Interface effects such as phonon boundary scattering significantly affect the thermal conductivity in semiconductors when dimensions are of the same order of magnitude as the phonon mean free path, which is ~200-300 nm in Si [81], [82]. Furthermore, the small dimensions of devices result in low thermal capacitance.

The thermal conductivity is further reduced in highly doped films. Phonons, being the main heat carriers in semiconductors, are scattered at interfaces and impurities which results in reduced thermal conductivity. Though in advanced FDSOI devices the channel is usually undoped, the source and the drain regions are highly doped. The thermal conductivity reduction with high doping is especially relevant for the drain as it is the hottest part of a device [83].

1.7.2 Impact

Self-heating is detrimental to devices operating in the analogue regime as the build-up of heat reduces carrier saturation velocity and mobility according to [84]:

$$\mu_{eff} = \mu_{eff0} \left(\frac{T}{T_0}\right)^{-k}, \tag{1.5}$$

where μ_{eff} is the effective mobility, μ_{eff0} is the effective mobility at ambient temperature, T is the average channel temperature, T_0 is the ambient temperature and k is the factor of mobility degradation with temperature. The values of k reported in the literature range from 0.8 to 2.1 in

MOSFETs [19], [84], [85]. A higher device temperature leads to increased phonon scattering and consequently degradation of mobility and reduction of the output current.

Self-heating aggravates performance variability [86], [87] which is anyway imperfect in advanced FDSOI devices as was discussed in Section 1.5.1 and Section 1.6.1.

Self-heating compromises device and circuit reliability. Elevated temperatures caused by device self-heating lead to metallisation lifetime degradation [88] as the time-to-failure of interconnects is proportional to $e^{1/k_B T_{ic}}$, where k_B is the Boltzmann's constant and T_{ic} is the interconnect temperature [89]. Quality of the gate dielectrics is also a function of temperature [88], [90]. Temperature-dependent trap-assisted gate leakage mechanisms such as Poole-Frenkel conduction reduce the gate dielectric time-to-breakdown thus degrading reliability [81]. This degradation is especially aggravated in ultra-thin silicon oxide [90] and in thin high-κ dielectrics [91].

Advanced FDSOI devices are composed of parallel fins or fingers to achieve targeted channel width and length ratios. This results in a temperature gradient within the fin or finger array with higher temperature in the inner fins compared with the outer ones [79]. The temperature gradient across the chip may result in the timing errors, signal delays and aggravated variability. However, in [92] it was concluded that self-heating does not represent a limiting factor for the reliability of ultrathin FDSOI transistors, in particular for fast switch operation.

Due to the finite thermal capacitance of a device, temperature does not follow voltage oscillations instantaneously [84], [93], thus dynamic self-heating is pronounced only in devices operating below a certain frequency. Heat is effectively low-pass filtered. Devices operating in the digital regime are not affected by the dynamic self-heating as they run well above this frequency. However, many of the real-world applications have some part operating in analogue regime. Self-heating dependence on frequency introduces undesirable performance variation with frequency in analogue applications, such as an amplifier's gain being a function of frequency. This is particularly important for circuits which carry signals with various frequency components [84]. Specific thermal characteristic frequencies greatly depend on the device design and technological parameters. Typically the characteristic thermal frequencies are observed in the kHz–MHz range [84], [94], [95], although they may enter GHz frequencies in the most advanced devices [96]. The characteristic thermal frequency is inversely proportional to the thermal time constant which is the product of the thermal resistance and thermal capacitance. The thermal resistance is inversely proportional to the surface area of the device, while the thermal capacitance is related to the device volume. In advanced non-planar devices the volume-

to-surface ratio is significantly decreased which leads to smaller time constants [79]. This translates into high characteristic thermal frequencies which are required for characterisation of self-heating. Characterisation of self-heating and extraction of thermal parameters such as thermal resistance and thermal capacitance allows correction for self-heating in high frequency applications characterised by low-frequency methods. Advantages and limitations of different self-heating characterisation techniques are discussed and compared in Chapter 2.

1.7.3 Self-heating in FinFETs

Previously, self-heating in FinFETs has primarily been studied by numerical simulations [48–50], [97–100]. There are only few works which are based on experimental results [86], [96].

Dependence of the thermal properties on FinFET geometry was studied mainly using modelling. Kolluri *et al.* [49] used an analytical thermal model to simulate the temperature rise in FinFETs as a function of different device geometrical parameters. It was concluded that the fin height and the fin width are the most important parameters while the fin spacing, BOX thickness and thermal conductivity of the passivation layer are less significant from a thermal point of view. Molzer *et al.* [48] also used numerical simulations and considered the thermal resistance dependence on the number of parallel fins. Braccioli *et al.* [50] performed electro-thermal simulations to study the dependence of FinFET thermal properties on the BOX thickness, source and drain extensions length, the fin spacing and the fin height. In [100] the impact of the source and drain extension geometry on thermal properties of FinFETs was studied. It was found that the flared extensions can be beneficial from the electrical and thermal point of view compared with rectangular source and drain extensions. Analysis of the thermal properties in [48–50], [100] was not supported by experimental results and was entirely based on numerical simulations which require certain assumptions about heat conduction paths, device symmetries and boundary conditions.

In [96], [98] modelling of thermal effects was combined with measurements. In [96] the effect of self-heating on FinFET capacitances was demonstrated experimentally and supported by electro-thermal simulations. In [98] a 3D electro-thermal model for nanoscale FinFETs was developed and compared with DC and RF measurements. Experimental work on self-heating in FinFETs was carried out in [86]. In [86] self-heating in nMOS and pMOS FinFETs was compared along with extraction of some analogue figures of merit and variability evaluation but geometry dependence was not studied.

1.7.4 Self-heating in UTB and UTBB devices

Similarly to FinFETs (Section 1.7.3), most self-heating investigations in UTB and UTBB devices in the literature are based on simulations.

Thermal effects in UTB devices were modelled in [50], [81], [83], [101]. Fiegna *et al.* [81] estimated the thermal resistance and the temperature rise in UTB devices with different gate lengths, BOX and source and drain thicknesses based on numerical simulations. Self-heating reduction with BOX thinning from 150 nm to 25 nm and contribution of heat removal by raised source and drain regions was shown.

Braccioli *et al.* in [50] used electro-thermal simulations to evaluate thermal properties in various SOI MOSFETs including a UTB device on 50 nm-thick BOX. It was concluded in [50] that self-heating severely impacts device performance and it was found that dependence of thermal properties on device geometry is weak.

In [83], [101] UTB devices with BOX thicknesses down to 50 nm and Si body channels as thin as 10 nm were modelled. Reported average temperatures agreed with the results in [81]. It was also shown in [83], [101] that the peak temperatures in UTB MOSFETs can reach more than 500 K in short UTB devices with an ultra-thin channel. It was also suggested in [83] that the thermal behaviour of UTB SOI devices with the gate stack formed by HfO_2 and SiO_2 is degraded compared with devices with SiO_2 only.

Rodriguez *et al.* [92] experimentally extracted the thermal resistance and the temperature rise in UTB devices on 145 nm thick BOX using the pulsed *I-V* technique and an assumption about mobility degradation with temperature. However, these values appeared to be much lower (temperature rise of 10-30 °C) than theoretically predicted in [81], [83], [101] especially taking into account extremely thin Si film of 6 nm and thick BOX in devices in [92].

Self-heating in devices with BOX thickness under 50 nm has not been widely studied. Only in [81] simulations were performed with BOX thickness down to 25 nm. However, the main focus of the paper was on UTB devices with thicker BOX. The 50 nm-thick BOX device was used as a reference in [81]. BOX thinning (as in UTBB devices) is predicted to improve the thermal properties and allow for better heat removal from the channel to the heat sink as the thermal resistance is proportional to the square root of the BOX thickness [94]. However, BOX thinning also results in reduction of its thermal conductivity [79], [102], thus compromising improvement from the reduced BOX thickness.

1.8 Substrate effects

In addition to self-heating, SOI MOSFETs have been shown to suffer from source-to-drain coupling through the Si substrate underneath the BOX [30], [44], [103–107]. This parasitic coupling may degrade the digital and analogue performance of the devices [103]. Substrate effects in devices built on SOI platforms were extensively studied in [44], [103–106] mostly using Atlas modelling. This parasitic source and drain coupling can be observed through the output conductance variation over the wide frequency range.

Figure 1.7 shows the variation of the 160 nm gate length FDSOI nMOSFET output conductance with frequency at V_g = V_d = 1.0 V. The results were obtained by 2D Atlas simulations in the presence of self-heating and substrate effects and without taking them into account [103]. As the frequency increases over a few hundred Hz, minority carriers in the substrate do not respond to the AC signal, resulting in the first output conductance increase. The second substrate-related transition of the output conductance occurs at frequencies between hundreds of MHz and a few GHz where majority carriers in the substrate no longer follow voltage oscillations. It can be seen that identical simulations carried out without taking self-heating into account still feature two transitions in the 10-100 Hz and GHz ranges [103]. Contrarily, simulations performed with self-heating but without considering the substrate (with the back contact set below the BOX) yield only one output conductance transition in the MHz range related to self-heating. This confirms that the two transitions in the 10-100 Hz and GHz ranges are indeed caused by the presence of the substrate and have nothing common with either self-heating or with floating body effects [103]. Simulations performed with self-heating and substrate effects turned off result in a flat output conductance curve without any transitions at frequencies up to 1 GHz.

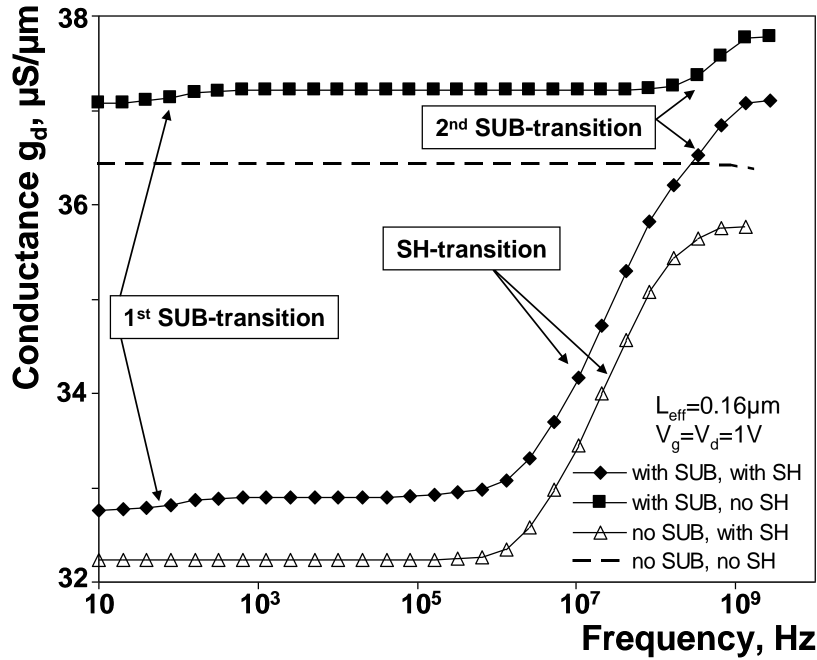

Figure 1.7. 2D Atlas simulations of the output conductance variation with frequency in 160 nm gate length FDSOI nMOSFETs with and without the substrate and self-heating turned on and off at $V_g = V_d = 1.0$ V. The substrate doping is p-type with the concentration of 6.5×10^{14} cm^{-3} [103].

1.9 Summary and thesis outline

The next few generations of chips obeying Moore's law most likely will be based on FDSOI technology. Materials and most of the techniques used in the FDSOI fabrication process are similar to those used in the conventional planar CMOS fabrication process. UTBB technology is naturally derived from planar PDSOI devices by thinning down the Si channel and BOX. FinFET technology brings in more novelty due to its 3D design. One of the biggest challenges for mass production of both types of FDSOI devices is yield. Fabrication costs of FinFETs and UTBB devices are debatable. The cost of the finished product is affected by availability of the starting wafers (limited for UTBB), number of fabrication steps (which is reduced in FDSOI technology compared with bulk CMOS) and fabrication complexity (higher for FinFETs than UTBB). Summarising, UTBB technology is more conventional and will be easier for the industry to adopt, while FinFETs are expected to be more scalable. Both types of FDSOI devices (FinFETs and UTBB) are known to exhibit parasitic self-heating and substrate effects which degrade their performance. Therefore, experimental characterisation of these effects is required.

In this work self-heating and substrate effects in advanced FinFETs and UTBB devices are studied experimentally. The thesis is organised as follows. In Chapter 2 different self-heating

characterisation approaches are analysed. Advantages and limitations of each technique are discussed and compared experimentally by applying them to self-heating quantification in SOI devices. The most suitable characterisation technique for advanced FDSOI devices is selected. In Chapter 3 UTBB devices are characterised over the wide frequency range. Responses to self-heating and substrate coupling are identified and evaluated considering device downscaling. Analogue figures of merit are extracted in order to benchmark UTBB technology with other advanced technologies. Chapter 4 focuses on substrate effects in UTBB devices. The effects are experimentally characterised and the impact of the substrate doping is evaluated. In Chapter 5 thermal properties in the UTBB devices are examined experimentally. Self-heating dependence on the buried oxide thickness is evaluated and two different characterisation approaches are tested. In Chapter 6 self-heating and substrate effects in FinFETs of various geometries are studied. The impact of these parasitic effects on the FinFET performance over the wide frequency range is evaluated. In Chapter 7 all the findings are summarised. Conclusions about FinFET and UTBB technologies are drawn and possible future work is outlined.

Chapter 2. Analysis of self-heating characterisation techniques

2.1 Background, motivation and chapter outline

As discussed in the introduction, advanced semiconductor devices, including those built on SOI platform, are prone to self-heating. Characterisation of self-heating is of interest for device and circuit designers. Temperature rise is important as it affects mobility, on-state and off-state current, threshold voltage, series resistance, saturation velocity, gate leakage and reliability [84], [108]. Design of a device can be modified to improve its thermal properties [82], [109]. Knowledge of the thermal resistance and thermal capacitance allows designers to generate equivalent circuits taking the impact of self-heating into account. If a device operates at high frequencies, its performance is not affected by the dynamic self-heating effect. If such a device is characterised by DC methods, its performance is evaluated inaccurately. However, knowledge of thermal parameters allows for correction.

Besides analytical and numerical models of self-heating in semiconductor devices, a number of methods for experimental characterisation of self-heating are available. A time domain pulsed *I-V* method was described and used in [110] to characterise SOI MOSFETs. In [96] the method was applied to FinFETs, but the pulse width of 100 ns was not sufficient for reliable characterisation. The pulsed *I-V* technique was applied to extract temperature in ultra-thin body (UTB) devices in [92] and in high voltage MOSFETs in [85] using the mobility temperature degradation coefficient. In the pulsed *I-V* method short pulses are applied to the gate. If the pulse is short enough (compared with the thermal time constant), the device does not heat up and the resulting drain current is self-heating free. The self-heating free current can be used to estimate the temperature rise in the channel using the mobility temperature degradation coefficient, as shown in [85], [92]. Another approach is to measure the self-heating free drain current at various chuck temperatures [110]. Its comparison with the drain current with self-heating at room temperature yields the temperature rise in the device due to self-heating.

In addition to self-heating characterisation, the pulsed *I-V* technique is also used to characterise traps. There is a growing interest in trap characterisation because of the increased surface to volume ratio (interfaces and traps start playing more important role) in advanced semiconductor devices compared with older technologies.

The AC conductance technique for measuring self-heating is a frequency domain approach. It was used to characterise a range of devices, including SOI [84], [94], SiGe [109] and Si gate-all-

around nanowire transistors [111]. The concept of the AC technique was extended to the RF [95]. The RF technique was applied to characterise self-heating in FinFETs [86], [96]. In the AC and RF techniques, the thermal resistance and the temperature rise in the channel can be extracted from the output conductance variation with frequency. In the case of the AC technique, the conductance is directly measured with an impedance analyser. In the RF method, the output conductance is obtained from the scattering parameters. Only the RF technique is applied in this work as it allows characterisation at higher frequencies. It will be shown that frequencies typically available with an AC set-up (few MHz) are not sufficient to reach self-heating free characteristics.

The other experimental techniques for self-heating characterisation include noise thermometry [84], [112] and gate resistance [84], [113]. Noise thermometry exploits thermal noise to extract the temperature in the channel. The technique requires special structures: two body contacts which provide a resistive path that is electrically decoupled from the front channel [112]. The gate resistance method also requires special structures for four-point gate resistance measurements [84], [113], [114]. These two techniques are not studied here.

An analytical approach that considers only one heat removal path was applied to SOI devices [94], [113] and to SiGe devices [109]. This method is also considered in this work to complement the experimental techniques.

The aforementioned experimental characterisation methods do not use assumptions about heat evacuation paths and boundary conditions as necessary for numerical or analytical models. However, it is unclear whether the same temperature rise and thermal resistance are obtained using different techniques. Some groups report self-heating results without comparison with other techniques [92], [109], [111]. However there is already evidence for FinFETs that the RF technique is more accurate than the AC conductance and the pulsed *I-V* techniques [96]. The aim of this work in this chapter is to compare the thermal parameters extracted using the various techniques found in literature. Partially depleted (PD) SOI devices are used as they are expected to suffer from self-heating.

In Section 2.2 devices are described. Sections 2.3, 2.4 and 2.5 give details of the three categories of techniques used: pulsed *I-V*, RF and the analytical model, along with the extracted thermal properties of PDSOI devices. A discussion of the results and a comparison of the techniques are presented in Section 2.6. Conclusions are drawn in Section 2.7.

2.2 Devices

The devices are body-tied PDSOI nMOSFETs built on 400 nm-thick BOX. The devices feature 240 nm gate length and are arranged in 15 parallel fingers, each finger being 4 μm wide. Therefore, the effective device width is 60 μm. The Si film thickness is 150 nm and the gate dielectric thickness is 5 nm. The doping in the channel is ~10^{18} cm^{-3}.

The devices are body-tied to prevent the kink effect (also known as the floating-body effect) which is common for PDSOI devices and may cause the history effect [110], [115]. The kink effect is caused by impact ionisation at high electric fields in the drain side of the MOSFET. At high electric fields electrons have enough energy to generate a new hole-electron pair. An excess of holes which are accumulated in the body of an nMOSFET results in an increased potential of the Si body. At some critical point, the body-source p-n junction turns on resulting in an increase of the drain current. This increase is manifested as a kink in the output characteristics. This effect is not typical for FDSOI technology due to lower electric fields at the drain and due to a lower body-source energy barrier. A lower electric field alleviates the impact ionisation and reduces the generation rate of holes. A lower source-body energy barrier improves the removal of holes through the source. In PDSOI technology the floating body effects can be alleviated by employment of a lightly doped drain (LDD). To implement the lightly doped drain, a part of the drain close to the channel is doped with a lower impurity concentration than the rest of the drain, thus reducing the doping gradient between the channel and the drain. The lightly doped drain results in a weaker electric field and, therefore, reduced impact ionisation. However, a lightly doped drain might not be feasible in the most advanced devices. This is because the doping level difference within the drain is subtle (approximately one order of magnitude). It is also hugely affected by the randomness of the doping process, especially in advanced devices where only few tens of doping atoms define the doping concentration. Another solution to overcome the floating body effect in PDSOI devices is tying the body to the source which is grounded. This fixes the body potential and prevents the build-up of positive charge in the body.

2.3 Time domain self-heating extraction (pulsed I-V)

Pulsed *I-V* technique is classified as the time domain characterisation method as signals are generated and captured with respect to time. An oscilloscope, which is a time domain instrument, is used to record voltage pulses at certain time intervals.

In this section two pulsed *I-V* self-heating characterisation approaches are discussed. One is the pulsed *I-V* hot chuck technique. The other pulsed *I-V* method that uses the mobility temperature degradation coefficient will be referred to as the pulsed *I-V k*-coefficient technique, where *k*-coefficient is the factor of mobility degradation with temperature.

Firstly, theory of pulsed measurements and their application to self-heating characterisation is discussed in Section 2.3.1. Then, both of the pulsed *I-V* methods are described and applied to the self-heating characterisation of PDSOI MOSFETs. Finally, they are compared with each other and with the frequency domain characterisation technique in Section 2.6.

2.3.1 Pulsed I-V theory and set-up

Characterisation of self-heating in various SOI devices using time domain methods have been previously reported [85], [92], [96], [110]. These methods use a sufficiently short applied gate voltage pulse (compared with the device thermal time constant) such that the device channel does not heat up. After the voltage pulse is applied to the gate and the DC voltage is applied to the drain, the drain current flows into a shunt (usually 50 Ω) which is connected in series with the drain. The voltage drop across the shunt is recorded using an oscilloscope. Knowing the set drain voltage, the amplitude of the drain voltage pulse and the shunt resistance, the pulsed drain current can be reconstructed. This setup requires the drain current to be very close to zero when the gate pulse is not applied. The current resolution of this set-up is limited by the voltage resolution of the oscilloscope and the shunt resistance. The maximum drain current that can be detected using this set-up is also limited as a large drain current would result in large drain voltage pulse [110]. Therefore, the effective gate width of a device under test (DUT) must be chosen to be large enough not to be limited by the drain current resolution and small enough to satisfy the constraint on the amplitude of the drain voltage pulse. The latter restriction is especially relevant to advanced devices which are arranged in parallel fingers resulting in a large effective gate width.

In this work the set-up consists of an Agilent B1500A semiconductor device analyser, an MSO8104 oscilloscope, an 81110A pulse pattern generator, a bias-T and coaxial and triaxial cables. Agilent EasyExpert software was used to control the equipment. Ground-signal-ground (GSG) 100-μm pitch probes were used for on-wafer characterisation with a SÜSS MicroTec probe station and Temptronic ThermoChuck for hot chuck measurements. The simplified set-up of the pulsed *I-V* measurements is shown in Figure 2.1.

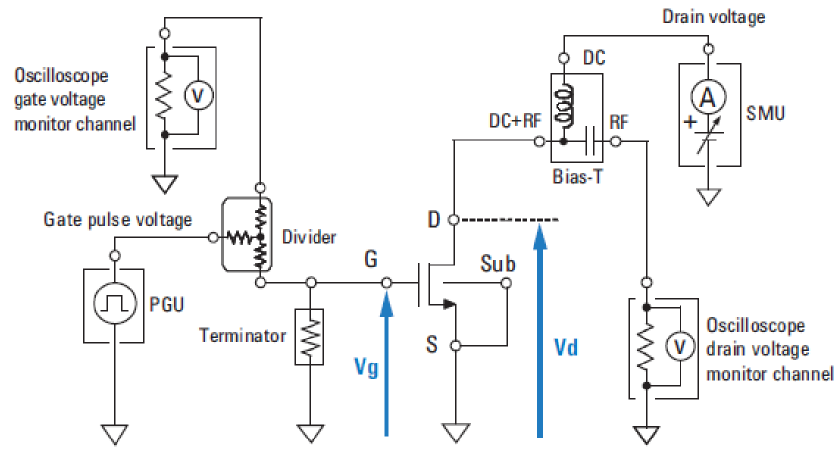

Figure 2.1. Simplified pulsed *I-V* characterisation set-up [116].

The set-up can produce voltage pulses from 10 ns to 1 µs. The available gate voltage range is from -4.5 V to 4.5 V. The current resolution of the set-up is 1 µA. The set-up allows switching from pulsed to DC measurements without any change of cabling. The pulse period is fixed to 100 µs resulting in a duty cycle from 0.01% (10 ns pulse) to 1% (1 µs pulse). Even the maximum duty cycle of 1% is short enough to assume that the device has time to cool down between applied pulses. The set-up allows adjustment of the rise and fall times, pulse base, averaging, pulse smoothing and monitoring of the gate and drain voltages. The pulse base must be chosen at a level, where the device is off and the drain current is as low as possible. To choose the pulse base for characterisation of self-heating in PDSOI devices, transfer characteristics were measured. The resulting curves are shown in Figure 2.2. A pulse base of -0.2 V was chosen as it meets the criteria as shown in Figure 2.2.

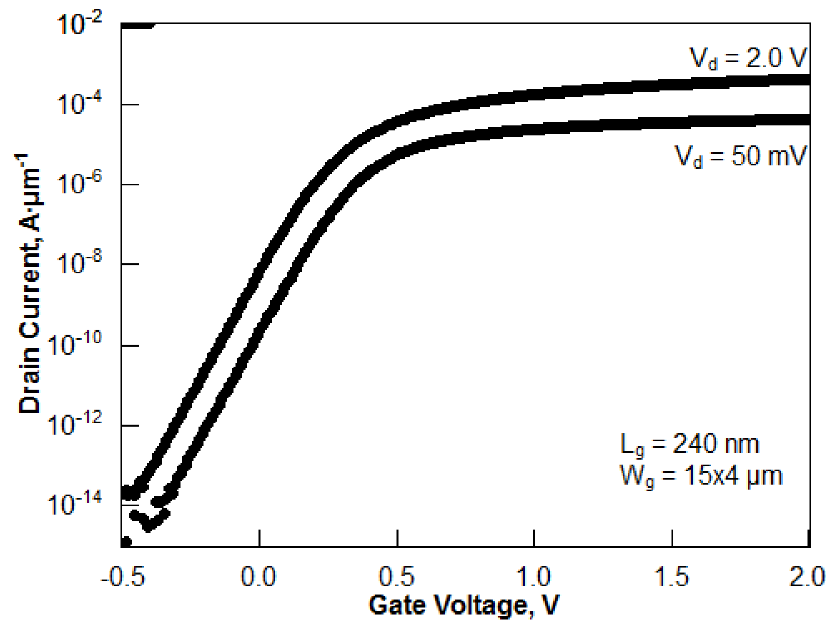

Figure 2.2. Transfer characteristics obtained from DC measurements at V_d = 50 mV and V_d = 2.0 V at room temperature.

In order to verify that the shape of the pulse is sufficiently well-defined, a 50 ns-wide gate voltage pulse was recorded and is presented in Figure 2.3. The top of the pulse was set to 1.8 V and the base was set to -0.2 V. The top of the pulse was found to be sufficiently flat and the rise and fall times were small compared with the pulse duration.

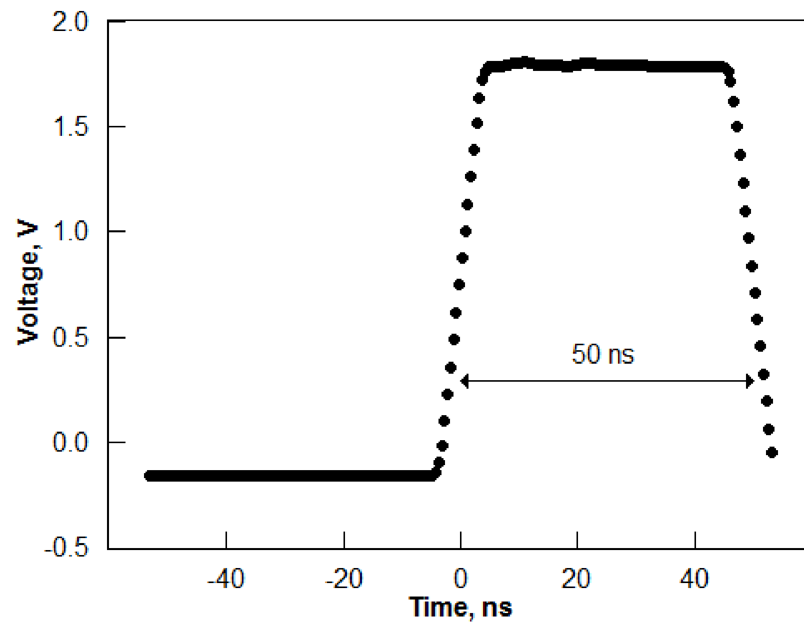

Figure 2.3. A voltage pulse applied to the gate. The pulse width is 50 ns, the pulse top is 1.8 V and the pulse base is -0.2 V.

In order to see the effect of self-heating on current degradation, DC drain current was compared with the drain current measured using different pulse widths as the drain voltage was swept from 0 to 2.0 V at room temperature. The pulse width was changed from 1 μs (the widest available pulse) to 10 ns (the narrowest available pulse). Figure 2.4 shows the resulting I_d-V_d curves. The inset in Figure 2.4 shows the same I_d-V_d curves enlarged at the high drain voltage region. The pulsed *I*-*V* set-up used for this work also allows extraction of the pulsed I_d-V_g curves. The extraction of thermal properties using I_d-V_g curves instead of I_d-V_d uses similar procedures.

Firstly, Figure 2.4 shows the DC I_d-V_d curve coincides with all curves at pulsed conditions in the low drain voltage region. However, all the pulsed curves, even in case of the widest 1 μs pulse, are higher than the DC curve at high drain voltages. At a fixed drain voltage, as the pulse width is reduced the drain current increases. This is explained by reduced heating of the device when the gate voltage is applied for a shorter time. As the pulse width is reduced to 50 ns, the self-heating is completely removed. This is evident as shorter pulses (10 ns and 20 ns in Figure 2.4) result in no further drain current increase. Consequently, 50 ns, 20 ns and 10 ns I_d-V_d curves overlap. Therefore, minimum 50 ns pulses are required to completely remove dynamic self-heating in the PDSOI devices. In other technologies this value may change.

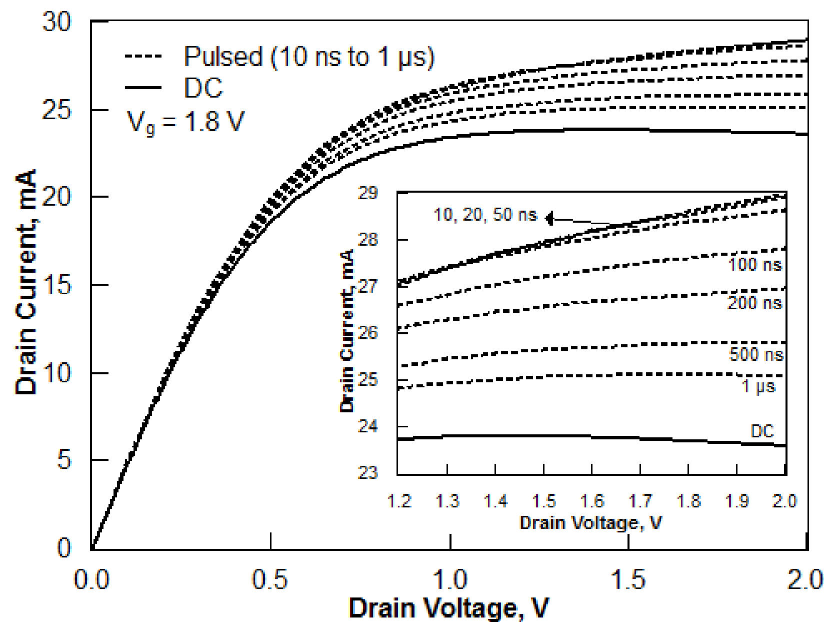

Figure 2.4. Output characteristics obtained from DC and pulsed *I*-*V* measurements with the pulse width from 10 ns to 1 μs at room temperature and V_g = 1.8 V. The high V_d region is shown in the inset.

There are two approaches how the self-heating free drain current can be used to obtain thermal parameters such as the average device temperature and the thermal resistance. In this work one method is referred to as the pulsed *I-V* hot chuck technique and the other method is referred to as the pulsed *I-V* *k*-coefficient technique. These are both described below.

2.3.2 Pulsed I-V hot chuck

In order to evaluate the temperature in the channel the pulsed I_d-V_d curves were measured at different chuck temperatures. The pulse width was set to 50 ns. When 50 ns pulses were applied to the gate, the device was not heated internally. Therefore, the device internal temperature was controlled by the temperature of the chuck. This method was used in [110] to characterise self-heating in SOI devices. Figure 2.5 shows 50 ns pulsed I_d-V_d curves at various temperatures and DC I_d-V_d responses at the room temperature for the PDSOI devices. The chuck temperature was varied from 25 °C to 175 °C during the pulsed measurements. The intersection of the DC I_d-V_d curve (affected by self-heating) and the self-heating free pulsed I_d-V_d curve indicates the temperature of the device at DC conditions. It is assumed that the device temperature is the same as the chuck temperature. However, the device temperature might be slightly smaller than the chuck temperature due to heat transfer from the wafer. This difference is expected to be larger at higher temperatures than at lower temperatures.

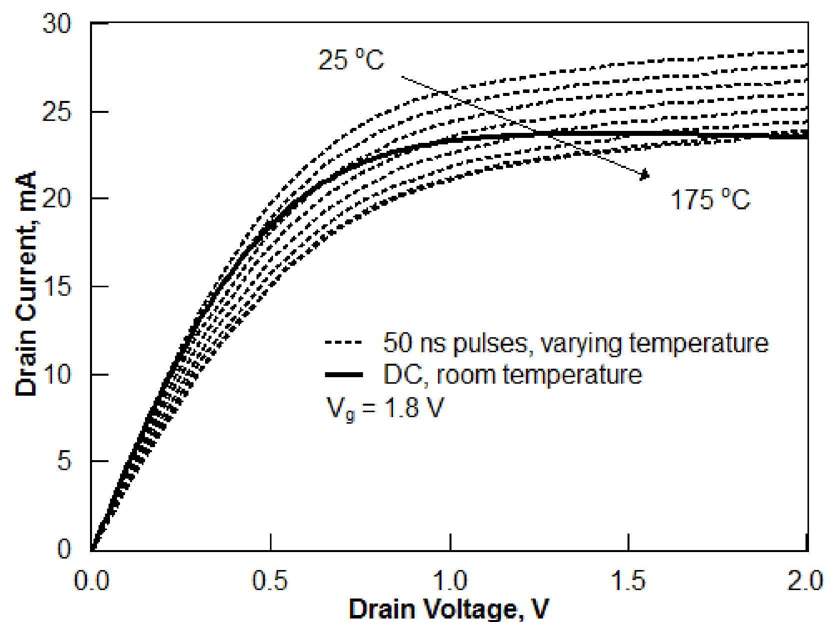

Figure 2.5. Output characteristics at V_g = 1.8 V obtained from the 50 ns pulsed *I-V* measurements at various chuck temperatures and from the DC measurement at room temperature.

The reduction of the pulsed drain current with increasing temperature follows the linear trend as shown in Figure 2.6. The drain current at DC conditions at room temperature is compared with the trend line data. The corresponding temperature of the chuck indicates the device temperature at the specified gate and drain voltages.

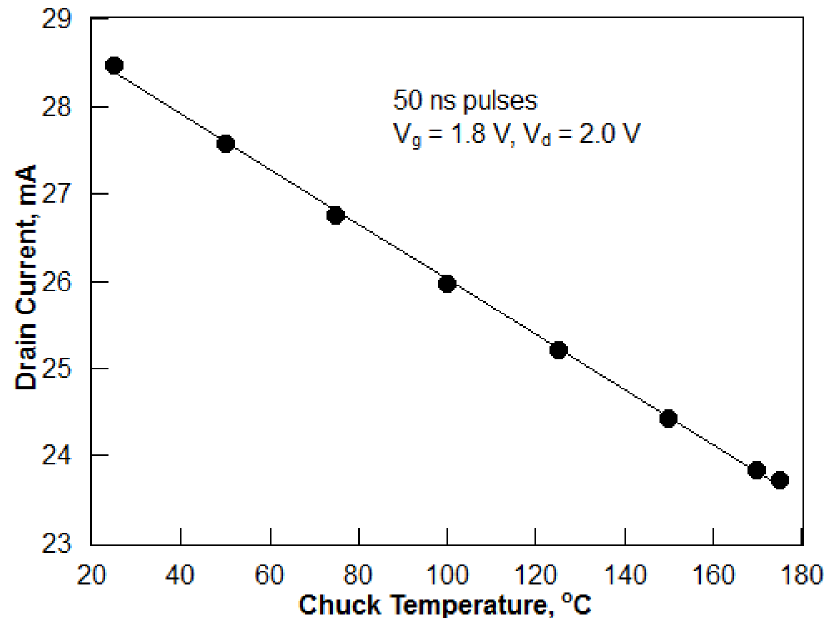

Figure 2.6. Linear fit of the 50 ns pulsed drain current at V_g = 1.8 V and V_d = 2.0 V at various chuck temperatures.

Figure 2.7 shows the increase of the device temperature as the power increases. The data are presented for three identical devices. The temperature in the devices was extracted from 20 ns and 50 ns wide pulses. The results match well, confirming the observation from Figure 2.4 where practically no difference was observed between 20 ns and 50 ns pulsed I_d-V_d curves. The data spread for different devices is insignificant and is likely to arise from the cross-wafer variation in device performance rather than from the extraction method. The thermal resistance can be extracted from the slope of the temperature rise with the power. In the first approximation the temperature varies with the power linearly. Validity of the linear approximation of thermal effects in Si was studied in [117]. It was shown that for Si the error in linear approximation is negligible in the temperature range of interest. Non-linear secondary effects might become more significant at high power levels [95], [117]. The linear fitting of the data in Figure 2.7 was forced to 25 °C at zero power. As the device temperature is presented at varying normalised power, the slope indicates the normalised thermal resistance. The thermal resistance is 0.2 $K \cdot m \cdot W^{-1}$. The data in Figure 2.7 will be compared with the thermal resistance extracted by other methods in Section 2.6.

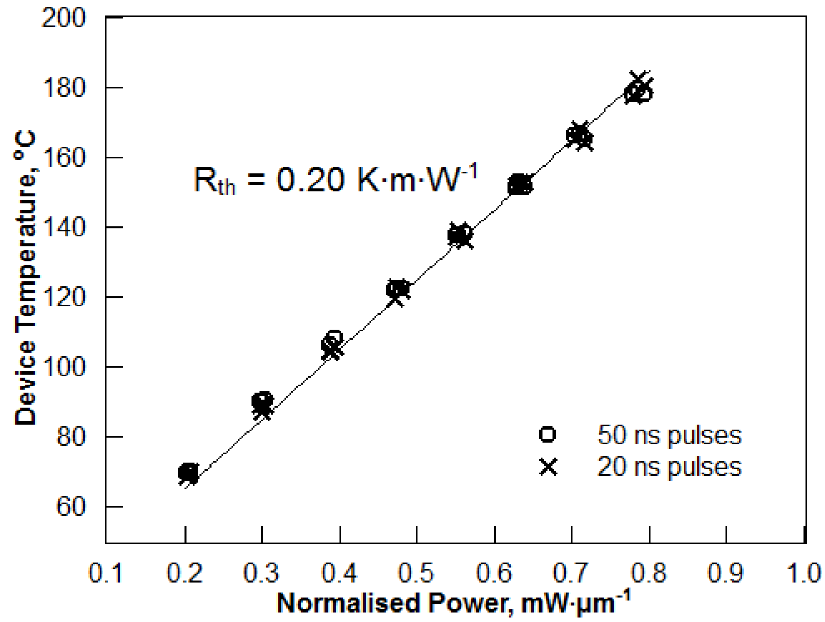

Figure 2.7. The lumped device temperature at various normalised power levels extracted from 20 ns and 50 ns pulsed *I-V* measurements in three identical devices.

2.3.3 Pulsed I-V and mobility degradation coefficient

Another approach to estimate the temperature in the device from the pulsed *I-V* data was used in [85], [92]. It assumes that mobility is the main parameter affected by self-heating and that the current degradation with increasing temperature is a direct consequence of mobility degradation. The temperature rise can be estimated from:

$$\Delta T = T_0\left(\left(\frac{I_{d0}}{I_d}\right)^{1/k} - 1\right), \tag{2.1}$$

where ΔT is the temperature rise, T_0 is the reference temperature (room temperature), I_d is the drain current at temperature T_0 with self-heating present (at DC conditions), I_{d0} is the drain current with self-heating removed (obtained from pulsed *I-V* measurements in this work) and k is the coefficient of the low-field mobility degradation with temperature (in some previous reports k is referred to as mobility temperature exponent [84] or mobility degradation factor [92]). The mobility temperature degradation coefficient can be estimated from the low-field mobility variation with temperature:

$$\mu_{eff} = \mu_{eff0}\left(\frac{T}{T_0}\right)^{-k}, \tag{2.2}$$

where T is the temperature, μ_{eff} is the mobility at temperature T and μ_{eff0} is the mobility at temperature T_0.

In order to evaluate the k-coefficient, mobility was extracted from transfer characteristics at V_d = 50 mV using the $I_d/\sqrt{g_m}$ method as described in [118]. The mobility is extracted from the slope of $I_d/\sqrt{g_m}$ variation with the gate voltage at a low drain voltage. Figure 2.8 shows the low-field mobility variation with the T/T_0 ratio, with the temperature being swept from 298 K to 448 K in three devices. The data is fitted using the power function. In order to extract the k-coefficient, the temperature must be expressed in K and not in °C. In this work, the extracted value of the k-coefficient is 1.2. The values of the k-coefficient reported in literature range from 0.8 to 1.7 for low-voltage nMOSFETs [19], [84] and 2.1 for high voltage MOSFETs [85]. Therefore, the extracted value of 1.2 is reasonable.

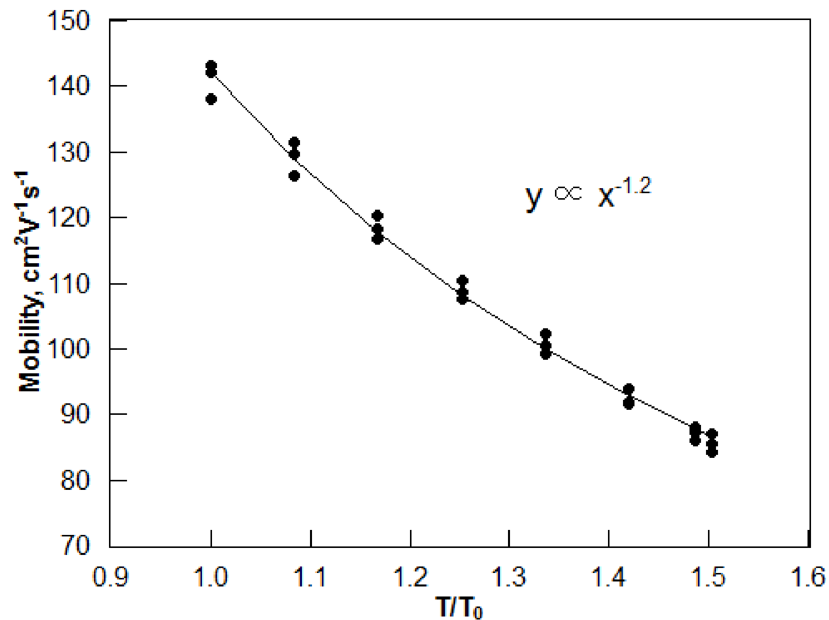

Figure 2.8. The low field mobility at various T/T_0 in three devices. The mobility temperature degradation coefficient is estimated from the data fitting.

Applying the extracted value of the k-coefficient in Equation 2.1, the lumped temperature in the three devices was obtained and is presented in Figure 2.9. The slope of the data forced to 25 °C at zero power provides the value of the normalised thermal resistance. As seen from Figure 2.9 the linear data fitting forced to 25 °C at zero power shows significant discrepancy from the extracted data. Most likely this discrepancy is introduced by the method. A value of the thermal resistance of 0.07 K·m·W^{-1} is found, which is considerably less than obtained by the hot chuck

method. These values will be compared with the data obtained using all the other extraction methods in Section 2.6.

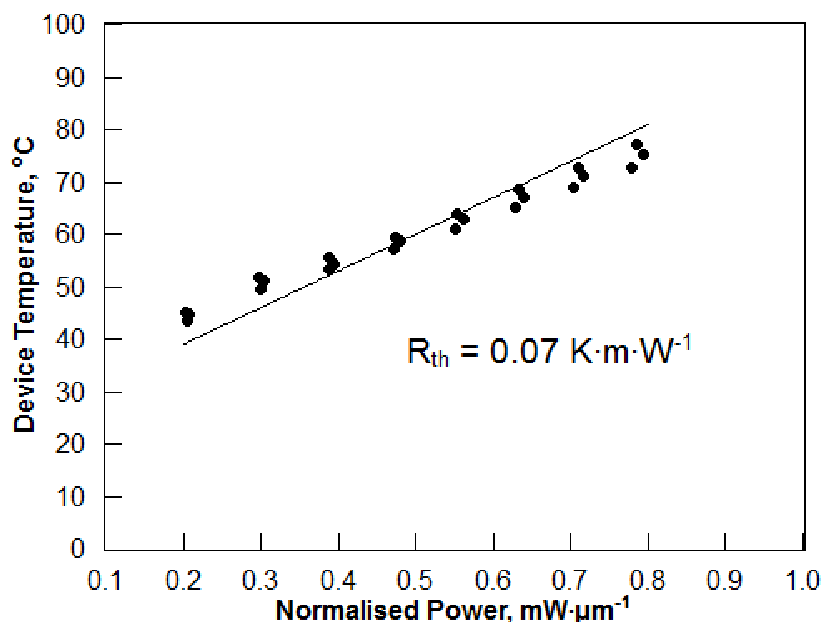

Figure 2.9. The variation in lumped device temperature with the power extracted using the mobility temperature degradation coefficient and pulsed *I*-*V* data in three devices.

2.4 Frequency domain self-heating extraction

In frequency domain characterisation, signals are generated and monitored with respect to frequency. Two techniques used to quantify thermal properties which classify as frequency domain methods are discussed in this section. These are the AC conductance technique and the RF technique. These two techniques are related to each other. The RF technique is applied to extract thermal parameters in the PDSOI devices. The technique and the obtained results are compared with the time domain techniques and corresponding results in Section 2.6.

2.4.1 AC conductance technique

The AC conductance technique has been widely applied to characterise devices on SOI and SiGe platforms [84], [94], [109], [119], [120]. The AC conductance technique is based on the assumption that at high frequencies, the device temperature does not follow voltage oscillations due to finite thermal capacitance [84]. Therefore, at a certain frequency the dynamic self-heating effect is completely removed.

To extract the parameters associated with self-heating such as the temperature rise or the thermal resistance, the output conductance is measured at high and low frequencies. This difference in conductance can be used to extract the self-heating parameters. An impedance analyser can be used to measure the output conductance at high and low frequencies. A simplified set-up is shown in Figure 2.10. A precision impedance analyser is connected between the source and drain electrodes. It supplies a small-signal oscillating voltage and a constant drain bias and either measures conductance variation with frequency at a fixed drain bias, or conductance variation with the drain voltage at a constant frequency. The semiconductor parameter analyser shares a common ground with the impedance analyser and is used as a constant bias source to supply the gate voltage. Once the difference in conductance at low and high frequency is obtained, it can be used to extract the thermal resistance [94]:

$$R_{th} = \frac{\Delta g_{d-SH}}{\frac{\partial I_d}{\partial T_A}(V_d g_{dT} + I_d)}, \tag{2.3}$$

where R_{th} is the thermal resistance, $\Delta g_{d\text{-}SH}$ is the output conductance difference at low and high frequency, $\partial I_d/\partial T_A$ is the dependence of drain current I_d on the ambient temperature, V_d is the drain voltage and g_{dT} is the output conductance at high frequency. Knowledge of the thermal resistance and power enables the extraction of the temperature rise in a device.

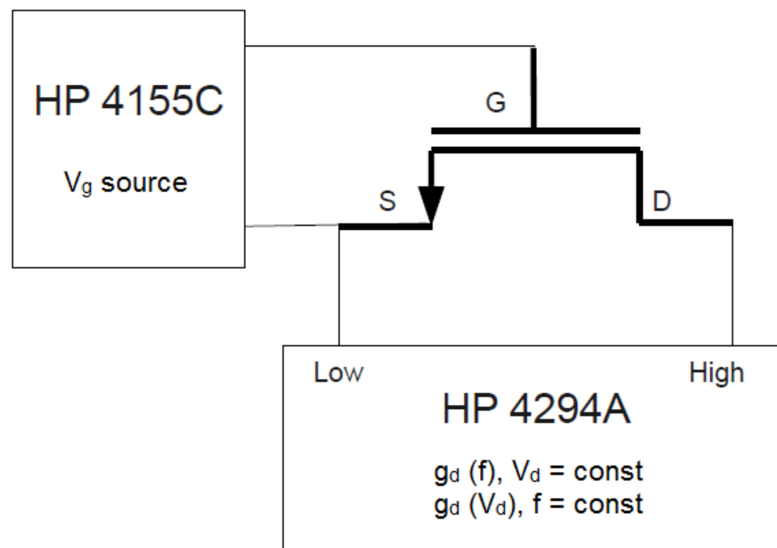

Figure 2.10. The set-up for measuring self-heating using the AC conductance technique.

Another approach to extract the thermal resistance from the output conductance variation with frequency was used in [84], [109]. In [84], [109] coefficients of mobility and threshold voltage variation with temperature as well as an empirical expression of the saturation velocity

dependence on temperature were taken from literature. These values were used to obtain the temperature in a device. A good agreement with results obtained with alternative techniques (noise thermometry, gate resistance and analytical model) was reached in [84], [109] for a few µm gate length MOSFETs. However, this approach requires knowledge of aforementioned coefficients (mobility, threshold voltage and saturation velocity dependence on temperature) which are not always well described in literature for advanced technologies.

In [120] the AC conductance technique was used to obtain the self-heating free output characteristics of PDSOI devices. Due to the set-up limitations, the measurements were limited to 5 MHz. It was assumed that at 5 MHz most of self-heating is removed, however the plateau of the output conductance variation with frequency (which is an indication of the dynamic self-heating removal) was not reached. Such frequency limitation can lead to underestimated self-heating of devices.

The AC conductance technique benefits from the relatively simple set-up and measurements because the output conductance variation with frequency can be directly measured with an impedance analyser. Furthermore, the output conductance variation with the drain voltage can be easily integrated to obtain the self-heating free output characteristics of a MOSFET. The main disadvantage of the technique is its frequency limitation to a few MHz.

2.4.2 RF self-heating characterisation

2.4.2.1 Technique

The RF technique to measure self-heating is derived directly from the AC conductance technique and uses a very similar approach. However, in contrast to the AC conductance method, the RF technique allows measurements at very high frequencies. This is necessary for advanced technologies as the thermal time constants are decreasing in state of the art semiconductor devices [79] and much higher frequencies (tens of MHz – few GHz) are needed to reach self-heating free characteristics.

In this section the frequency range of the RF extraction is limited to 4 GHz. This is because 4 GHz is sufficient to reach the self-heating free characteristics of the PDSOI devices (Section 2.4.2.2.1). However, the RF technique can be extended to much higher frequencies, at least up to 110 GHz.

For RF characterisation scattering parameters (*S*-parameters) must be measured over a wide frequency range. *S*-parameters are elements of a scattering matrix which characterises electrical

behaviour of a linear electrical network. *S*-parameters are related to other parameters that describe behaviour of a linear electrical network, including admittance (*Y*-) parameters, impedance (*Z*-) parameters and hybrid (*H*-) parameters. The size of a scattering matrix depends on a number of ports of an electrical network. If there are two ports in a network, the *S*-matrix consists of four *S*-parameters:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}. \tag{2.4}$$

Each of these *S*-parameters is a complex number and describes the behaviour of the linear electrical network in terms of power transmission and reflection. Each parameter is obtained from a measurement when one port is excited by a power source and the other one is terminated with a load. The parameter S_{11} is an input reflection coefficient on port 1, i.e. a signal is applied to the port 1 and its reflection on the port 1 is measured, while the output port is terminated by a matched load. The S_{12} parameter is a reverse transmission gain with the input port terminated with a matched load. The S_{21} parameter is a forward transmission gain with the output port terminated with a matched load. The S_{22} parameter is an output reflection coefficient with the input port terminated by a matched load [121].

S-parameters can be measured for various electrical networks, including bipolar and field effect transistors. However, as a transistor is an active device, the small-signal condition has to be satisfied so the transistor can be treated as a linear network. Therefore, the oscillating signal has to be small enough compared with the DC bias. In *S*-parameter measurements, power signals are applied to the network ports. Therefore, the oscillating signals are quantified in dB. Knowing the characteristic impedance, one can convert power of the oscillating signal expressed in dB or dBm into the voltage. The resulting voltage has to be significantly smaller than the applied DC bias. In the case of the AC conductance technique when an impedance analyser is used, excitation can be caused by voltage or current signals. Then the oscillating voltage can be directly compared with the DC voltage in order to satisfy the small-signal condition.

In this work MOSFETs are characterised and the gate is assigned as port 1 and the drain as port 2. The other MOSFET terminals are grounded. The characteristic impedance of the system is 50 Ω. Before measurements, the equipment was calibrated for open and short. *S*-parameters were measured with Rohde & Schwarz vector network analyser at frequencies from 40 kHz to 4 GHz. The gate and drain DC voltages were supplied by Keithley 2400 instruments. All instruments were controlled by a Labview programme.

S-parameters were measured in the devices under test at various gate and drain voltages and frequencies. In order to compensate for parasitic effects that arise from the device contacts, the open structures of corresponding devices were measured. After the measurements, all S-parameters were transformed into admittance parameters (Y-parameters) as follows:

$$Y_{11} = \frac{\big((1 - S_{11})(1 + S_{22}) + S_{12}S_{21}\big)}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0, \tag{2.5}$$

$$Y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0, \tag{2.6}$$

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0, \tag{2.7}$$

$$Y_{22} = \frac{\big((1 + S_{11})(1 - S_{22}) + S_{12}S_{21}\big)}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0, \tag{2.8}$$

where Y_0 is the characteristic admittance (derived from the characteristic impedance).

After the conversion the Y-parameters of the open structures are subtracted from the Y-parameters of the devices to obtain Y-parameters which characterise the devices without parasitic impact arising from the contacts.

Y-parameters are also complex numbers and form an admittance matrix (Y-matrix). Elements of this matrix show the relation between currents and voltages at various ports. In case of a two-dimensional Y-matrix:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \frac{i_1}{v_1} & \frac{i_1}{v_2} \\ \frac{i_2}{v_1} & \frac{i_2}{v_2} \end{bmatrix}, \tag{2.9}$$

where i_i and v_i are the small-signal current and voltage on the terminal i, respectively.

In the case of a MOSFET complex parameters Y_{21} and Y_{22} are:

$$Y_{21} = g_m - j\omega C_{dg}, \tag{2.10}$$

$$Y_{22} = g_d + j\omega C_{dd}, \tag{2.11}$$

where g_m is the transconductance, g_d is the output conductance, C_{dg} is the drain-to-gate capacitance, C_{dd} is the total drain capacitance, ω is the angular frequency and j is the imaginary

unit. C_{dd} is one of the 16 intrinsic capacitances in a four-terminal MOSFET. Out of 16 capacitances 9 are linearly independent [122]. Figure 2.11 shows capacitances schematically.

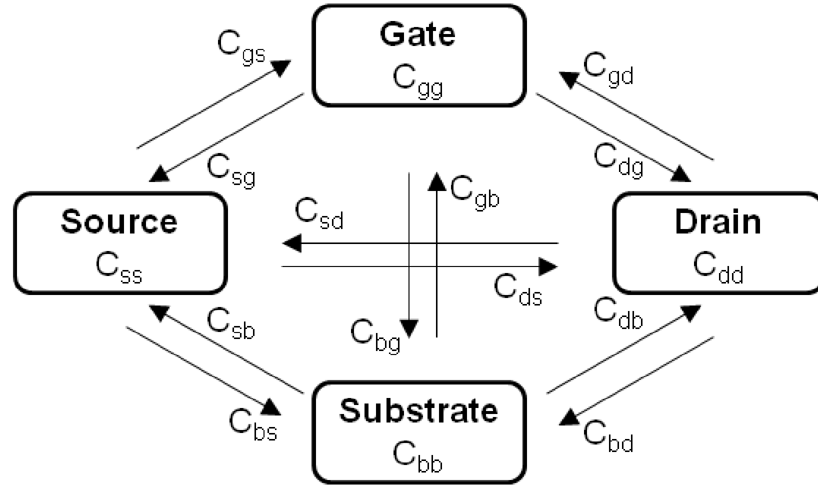

Figure 2.11. Intrinsic MOSFET capacitances shown schematically.

Rinaldi in [95] derived how *Y*-parameters in a two-port electrical network are linked to its thermal impedance. This derivation can be applied to any two-port linear electrical network, including a bipolar junction transistor or a MOSFET under small-signal conditions with certain terminals being grounded.

$$Y_{ij} = Y_{ijT} + Z_{th}\frac{\partial I_i}{\partial T_A}\left(V_g Y_{1jT} + V_d Y_{2jT} + I_j\right), \tag{2.12}$$

where Y_{ij} is a *Y*-parameter expressing ratio of the small-signal current on the terminal i to the voltage on the terminal j, Y_{ijT} is the Y_{ij} parameter at high frequency with the dynamic self-heating removed and Z_{th} is the thermal impedance which is a complex number. Indices *1* and *g*, *2* and *d* are interchangeable in this notation as the gate of a MOSFET is assigned as port 1 and the drain as port 2.

The real part of the thermal impedance Z_{th} is the thermal resistance R_{th}. It can be used to extract the temperature rise ΔT in the channel according to:

$$\Delta T = R_{th} I_d V_d. \tag{2.13}$$

The thermal resistance should be normalised to the gate width to enable fair comparison between different devices or various technologies. If the normalised thermal resistance (units $K \cdot m \cdot W^{-1}$) is used in Equation 2.13 than the drain current should also be normalised (units $A \cdot m^{-1}$).

In general, according to Equation 2.12 any *Y*-parameter can be used to obtain thermal impedance. For example, the frequency dependence of the Y_{21} parameter can be analysed, and converted into the thermal impedance. In such cases the real part of the Y_{21} parameter (transconductance in MOSFETs) at various frequencies can be used to extract the thermal resistance. However, practically the variation of the Y_{22} parameter with frequency is the strongest and, therefore, the transitions are more distinct. Hence, only thermal impedance extraction from the Y_{22} is considered in this work.

In order to obtain the thermal resistance R_{th} only real parts of the terms in Equation 2.12 should be considered:

$$Re(Y_{ij}) = g_{ij} = g_{ijT} + R_{th}\frac{\partial I_i}{\partial T_A}(V_g g_{1jT} + V_d g_{2jT} + I_j). \quad (2.14)$$

It was assumed that the term $Im(Z_{th})Im(Y_{ijT})$ that appears in the real part of the multiplication result of two complex numbers is small compared with the other terms in Equation 2.14.

If the output conductance g_{22} is used for characterising self-heating in a MOSFET, then the term containing g_{12} in Equation 2.14 can be neglected as it is much smaller than g_{22}. Therefore, Equation 2.14 can be rewritten as:

$$g_{22} = g_{22T} + R_{th}\frac{\partial I_d}{\partial T_A}(V_d g_{22T} + I_d), \quad (2.15)$$

which agrees with Equation 2.3 derived in [94] for the AC conductance technique.

The imaginary part of the thermal impedance is obtained if only the imaginary parts of the terms in Equation 2.12 are considered:

$$Im(Y_{ij}) = Im(Y_{ijT}) + Im(Z_{th})\frac{\partial I_i}{\partial T_A}(V_g g_{1jT} + V_d g_{2jT} + I_j). \quad (2.16)$$

Or using Equation 2.11 this can be rewritten in terms of capacitances:

$$C_{ij} = C_{ijT} + \frac{Im(Z_{th})}{\omega}\frac{\partial I_i}{\partial T_A}(V_g g_{1jT} + V_d g_{2jT} + I_j), \quad (2.17)$$

where C_{ij} is the capacitance.

The total drain capacitance C_{22} varies with frequency by over a few orders of magnitude. In this work the measured variation of C_{22} with frequency will be used to extract the imaginary part of the thermal impedance. The imaginary part of the thermal impedance can be translated into

the thermal capacitance C_{th}. This relationship is derived from the analogy with the electrical capacitance derivation from the electrical impedance:

$$C_{th} = \frac{1}{\omega \cdot Im(Z_{th})}. \quad (2.18)$$

2.4.2.2 Results

2.4.2.2.1 Output conductance

Figure 2.12 shows the output conductance variation with frequency in a PDSOI MOSFET at V_g = 1.8 V and V_d = 2.0 V. The DC conductance value extracted from the output characteristics at the same bias conditions is also shown in Figure 2.12.

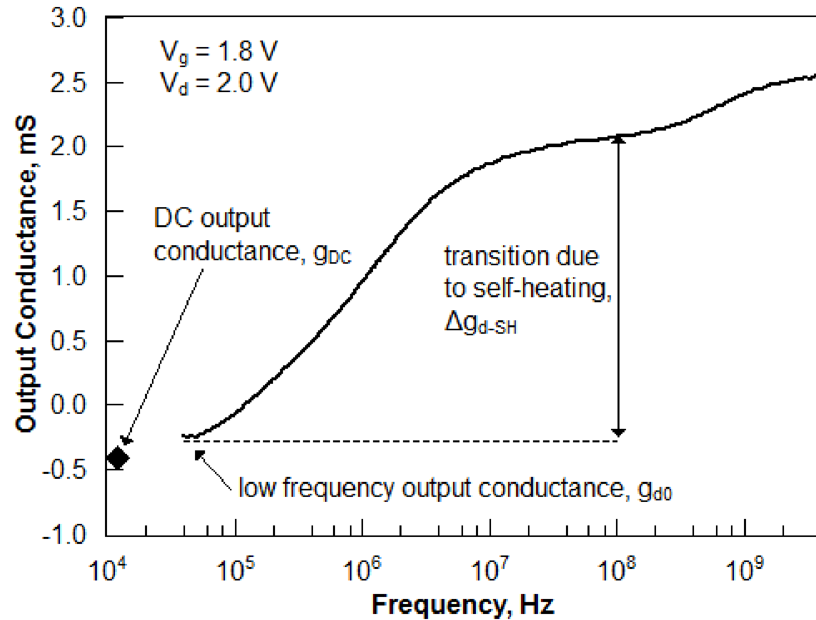

Figure 2.12. The output conductance variation with frequency showing a self-heating transition at V_g = 1.8 V and V_d = 2.0 V. The DC value of the output conductance extracted from DC output characteristics is also shown.

As seen from Figure 2.12 the transition due to self-heating is clearly observed between 40 kHz and few tens of MHz. At low frequencies, where the device is affected by self-heating, the output conductance is negative. As the frequency increases, the dynamic self-heating effect is removed and the output conductance increases. If the drain current is reconstructed, the increase in the output conductance is translated into an increase of the drain current as dynamic self-heating is removed. When evaluating the transition amplitude, it is imperative to select low and high frequency output conductances carefully in order to minimise the error as the low and high

frequency plateaus are not perfectly defined. In most cases the error is insignificant as the output conductance variation within the plateaus is much smaller than the self-heating related output conductance transition amplitude.

The output conductance transition at higher frequencies, between 100 MHz and 4 GHz, is caused by the source and drain coupling through the substrate under the BOX. It was proven that this substrate effect is not related to self-heating [44]. The amplitude and the characteristic frequency of the transition due to the substrate effect depend on a number of factors such as the substrate doping concentration, temperature and BOX thickness. In the PDSOI devices due to the thick 400 nm BOX the substrate effect is relatively weak compared with self-heating as seen from Figure 2.12.

In conductance frequency characteristics the kink effect may appear at low (few hundreds of Hz – kHz) frequencies [94]. In this work body-tied devices are characterised and, therefore, the kink effect is not observed. Both self-heating and kink effects appear in saturation. Their effect on the output characteristics might not be evident as these effects are competing at high drain voltage. Self-heating results in a reduction of the drain current, while the kink effect causes an increase of the drain current. However, in the output conductance frequency response these two effects are well separated due to different characteristic frequencies. The characteristic frequency of the kink effect is related to the lifetime of the carriers and is much lower than the characteristic frequency of self-heating. However, one must consider the effect of the kink in the output conductance frequency characteristics when characterising PD MOSFETs which are not body-tied [94].

2.4.2.2.2 Drain current temperature dependence

According to Equation 2.12 the drain current dependence on temperature $\partial I_d/\partial T_A$ is required to extract the thermal impedance and, subsequently, the thermal resistance and capacitance. In this work $\partial I_d/\partial T_A$ is obtained from the hot chuck measurements. The measured data are shown in Figure 2.13. The slope of the data provides $\partial I_d/\partial T_A$.

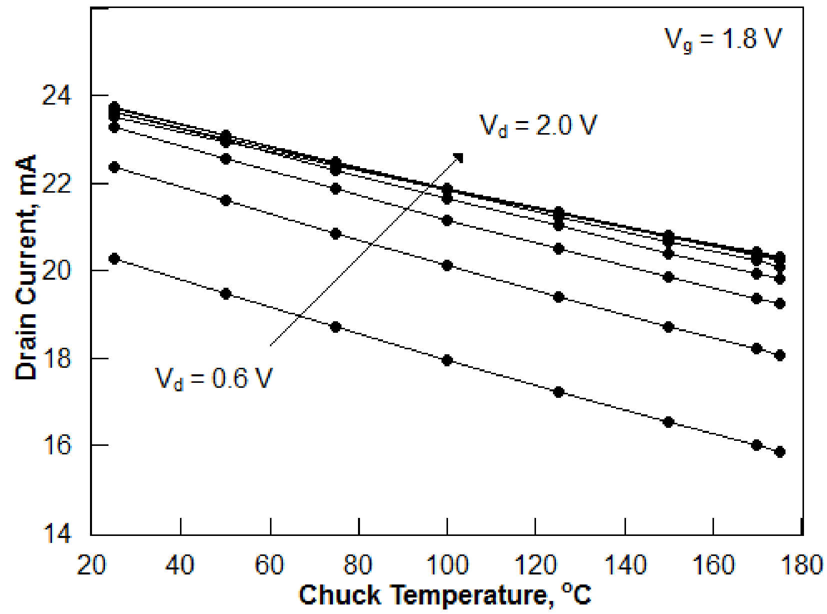

Figure 2.13. Drain current dependence on the chuck temperature at V_d from 0.6 V to 2.0 V and V_g = 1.8 V. The slope of the measured data is used to calculate the thermal resistance.

It is important to perform $\partial I_d/\partial T_A$ measurements in the range close to the expected temperature in the channel and at bias conditions well above the zero temperature coefficient (ZTC) point. ZTC point is defined as the gate voltage at which the drain current or transconductance do not change as the temperature varies. The ZTC point in the transfer characteristics of the PDSOI devices is shown in Figure 2.14 for the saturation regime and in Figure 2.15 for the linear regime of operation.

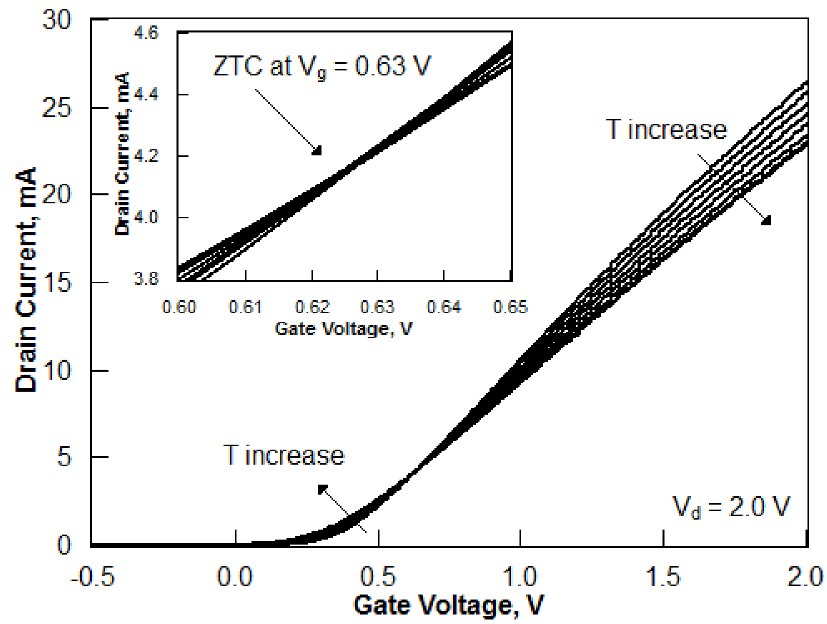

Figure 2.14. Transfer characteristics demonstrating zero temperature coefficient (ZTC) at V_d = 2.0 V. Transfer characteristics around ZTC are shown in the inset.

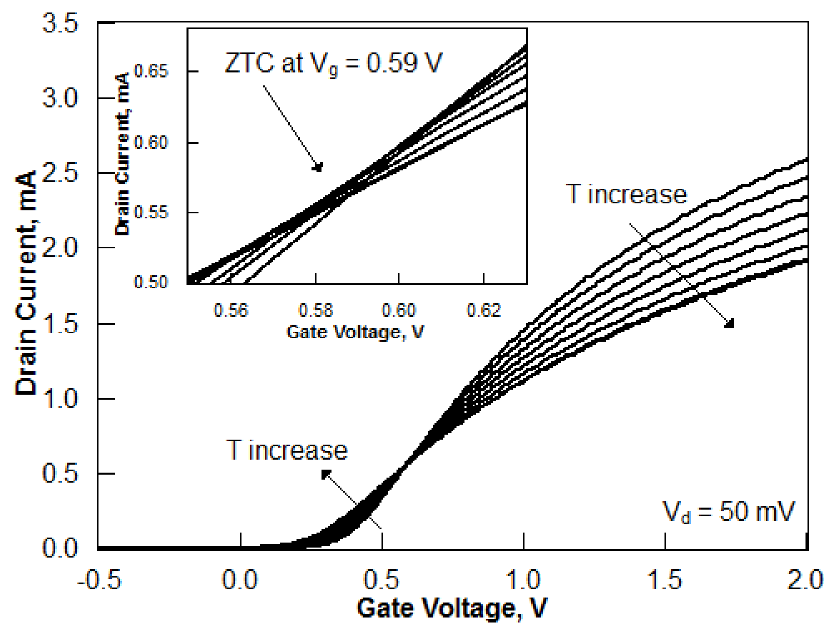

Figure 2.15. Transfer characteristics demonstrating zero temperature coefficient (ZTC) at V_d = 50 mV. Transfer characteristics around ZTC are shown in the inset.

In general there are four ZTC points for a body-tied PDSOI device [123–125]. ZTC points in the linear and saturation regions are typically different. Furthermore, the ZTC point of the drain current is different from the ZTC point of the transconductance. In the case of $\partial I_d/\partial T_A$

extraction, the drain current ZTC point in saturation should be considered. For further RF characterisation the gate voltage was fixed to 1.8 V which is well above the ZTC point.

At the gate voltage above ZTC the drain current and the transconductance dependence on temperature is caused mainly by the mobility degradation with temperature. At the gate voltage below ZTC the drain current and the transconductance dependence on temperature are determined by the threshold voltage shift with temperature. At ZTC point these two effects are balanced and the drain current and the transconductance are constant as the temperature varies.

2.4.2.2.3 Temperature rise, thermal resistance and capacitance

Combining Equation 2.13 and Equation 2.15, the lumped device temperature is extracted. Figure 2.16 shows the device temperature variation with power in three identical devices. The normalised thermal resistance obtained from the slope of the data in Figure 2.16 is 0.22 K·m·W^{-1}. These results will be discussed in Section 2.6 and used to compare different self-heating characterisation techniques.

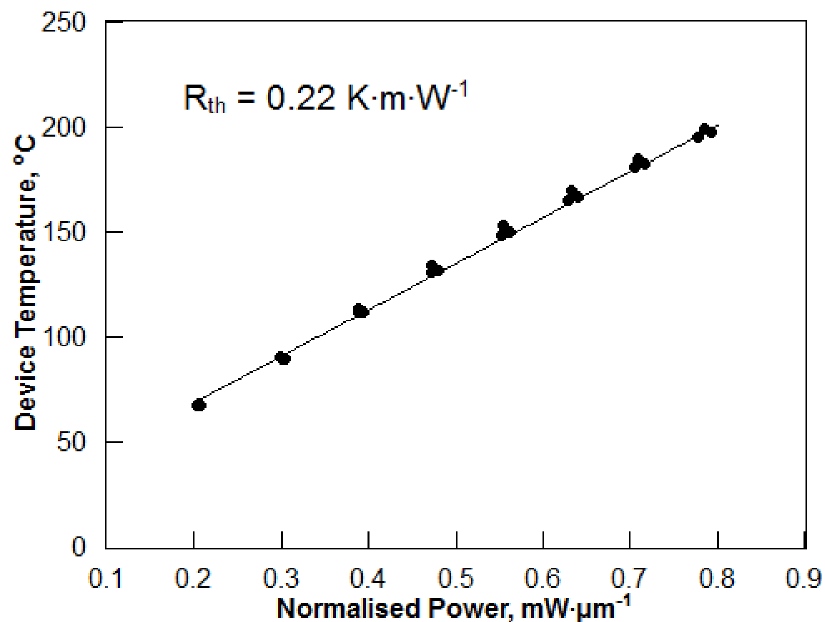

Figure 2.16. The average device temperature in three identical devices at various power levels extracted using the RF self-heating characterisation technique.

The RF technique also allows extraction of the thermal capacitance from the variation of the total drain capacitance with frequency. This is obtained from the imaginary part of Y_{22} according to Equation 2.11 and is shown in Figure 2.17. Firstly, the total drain capacitance changes over few orders of magnitude. Secondly, the transition due to self-heating is observed in the same

frequency range as shown for the output conductance (Figure 2.12). This is expected, as the variation of the total drain capacitance is caused by the same physical phenomenon as the variation of the output conductance.

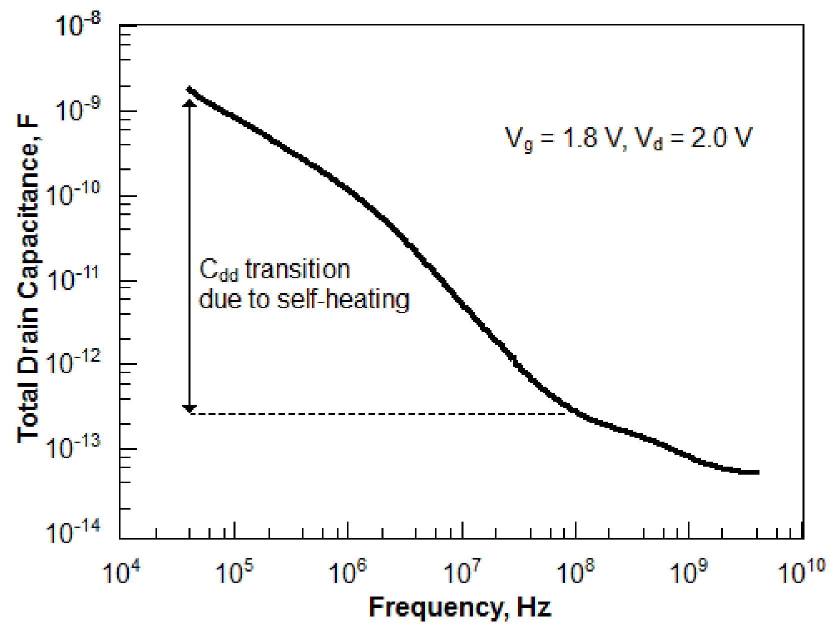

Figure 2.17. Variation of the total drain capacitance with varying frequency at V_g = 1.8 V and V_d = 2.0 V.

Figure 2.18 shows the thermal capacitance variation with the normalised power in three identical PDSOI MOSFETs. As expected, the thermal capacitance is power independent as it is mostly associated with the device volume where heat is contained.

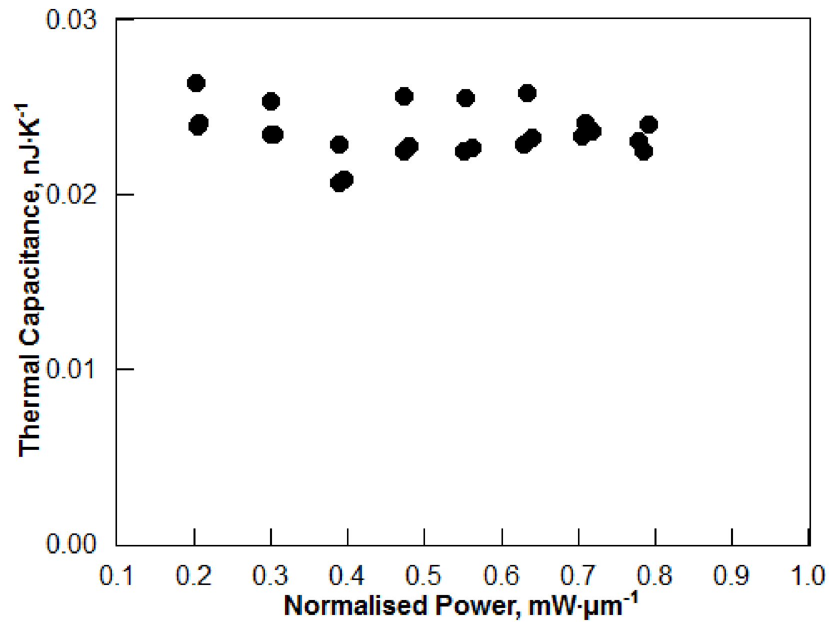

Figure 2.18. Thermal capacitance variation with power obtained from the RF self-heating characterisation in three identical devices.

2.4.2.2.4 Thermal time constant

For device modelling purposes the thermal resistance and capacitance may be used to form a thermal *RC*-network. A simplified model is shown in Figure 2.19. Device power is depicted as the current source in parallel with the thermal resistor and capacitor. Using this model, the thermal time constant τ_{th} can be estimated as:

$$\tau_{th} = R_{th}C_{th}. \tag{2.19}$$

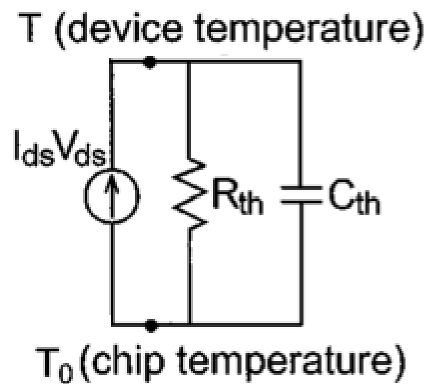

Figure 2.19. Simple self-heating RC-network model [94].

Another method to estimate the thermal time constant empirically was suggested in [94]. The thermal time constant τ_{th} can be calculated from the characteristic thermal frequency f_{th}, which is the frequency at which

$$g_d = g_{d0} + \frac{\Delta g_{d-SH}}{3}, \tag{2.20}$$

where g_d is the variable output conductance and is frequency dependent, g_{d0} is the output conductance at low frequency where self-heating is present and $\Delta g_{d\text{-}SH}$ is the output conductance transition amplitude due to self-heating. The meaning of g_{d0} and $\Delta g_{d\text{-}SH}$ are also explained in Figure 2.12. The characteristic thermal frequency is considerably lower than the frequency at which the self-heating is completely removed. The origin of this empirical method is not explained in [94]. It might be taken from the definition of the time constant of an electrical RC-circuit. In an RC-circuit, the time constant is defined as the time that is needed for the capacitor to discharge to e^{-1} (37%) of its original charge, which is close to the suggested value of 1/3 (compare with Equation 2.20) in the empirical method in [94].

After the characteristic thermal frequency is obtained, it can be transformed into the thermal time constant using

$$\tau_{th} = \frac{1}{2\pi f_{th}}. \tag{2.21}$$

Figure 2.20 compares the thermal time constants obtained using Equation 2.19 with the thermal time constant obtained using the empirical method. The time constants are shown for different power levels in three identical devices. These values of the thermal time constants will be discussed in Section 2.6 and will be related to the duration of pulses used in the pulsed I-V method.

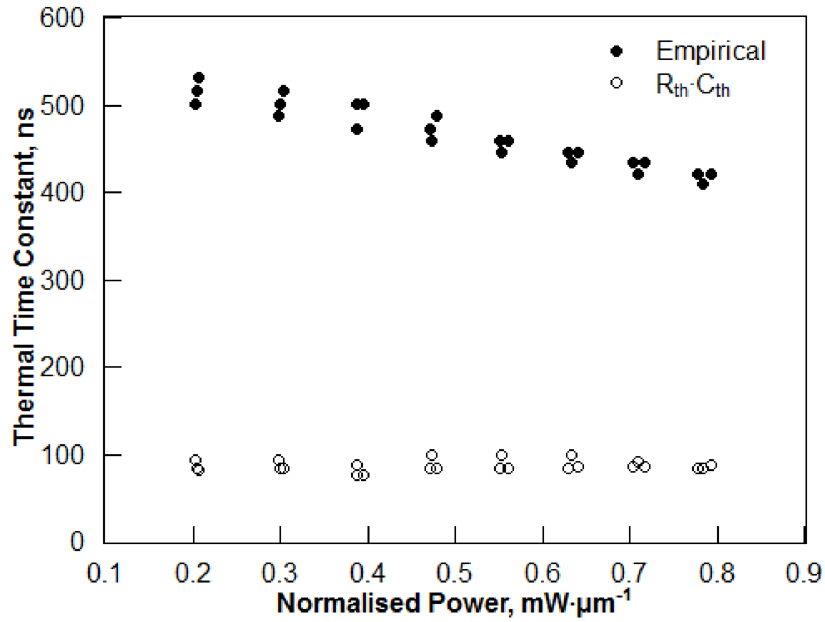

Figure 2.20. The thermal time constant at different power levels in three identical devices extracted with two different methods (empirical and $R_{th}\cdot C_{th}$) from the RF self-heating characterisation results.

2.5 Analytical model

As the device geometry is complex and various heat removal paths exist, it is difficult to set the boundary conditions properly and estimate the lumped thermal resistance of a device using simple analytical models. However, the thermal resistance of an individual heat path can be estimated without using complex numerical simulations. In this work only simple one-dimensional models of the BOX thermal resistance are considered.

A simple one-dimensional analytical model of heat transport in a material relates the thermal resistance to the material thickness and its thermal conductivity [113], [126]. In this case the thermal resistance of the BOX:

$$R_{th-BOX} = \frac{t_{BOX}}{A \cdot k_{SiO_2}}, \tag{2.22}$$

where $R_{th\text{-}BOX}$ is the BOX thermal resistance, t_{BOX} is the BOX thickness, k_{SiO2} is the thermal conductivity of SiO_2 and A is the area of the heat flux. One of the limitations of this approach arises from the difficulty to estimate the area of the heat flux. It can be approximated as a rectangle with one of the sides being the gate width. The other side can be obtained if the heat generation rate variation with the coordinate along the channel is known. The peak of the heat

generation rate can be located either in the drain or in the channel close to the drain. Pop *et al.* in [126] estimated the length to which the heat generation extends to the drain as $8.3 \cdot V_d$ (in nm) for UTB devices. Su *et al.* [113] used the entire drain length to estimate the area of the heat flux.

A more advanced model to estimate the BOX thermal resistance was used in [94], [109], [113]. It is derived in [113] from the model described above and is expressed as:

$$R_{th-BOX} = \frac{1}{2W}\sqrt{\frac{t_{BOX}}{t_{Si}k_{Si}k_{SiO_2}}}, \quad (2.23)$$

where W is the device width, t_{Si} is the Si film thickness and k_{Si} is the thermal conductivity of Si. This model was derived using a concept of the thermal healing length, which is a measure of the length-scale for thermal conduction in a device. The thermal healing length is defined as the length over which the temperature reduces to the temperature of the heat sink. Equation 2.23 is valid if the thermal healing length is smaller than the distance between the channel and metal contacts of the drain, i.e. the distance from the channel to the metal contact is large enough to minimise the impact of the metal contacts on device cooling. The thermal healing length can be estimated from:

$$\frac{1}{m} = \sqrt{\frac{k_{Si}t_{Si}t_{BOX}}{k_{SiO_2}}}, \quad (2.24)$$

where $1/m$ is the thermal healing length. In the PDSOI devices, the thermal healing length is ~1.5 μm. Therefore, the drain region has to be longer than 1.5 μm in order for the model expressed in Equation 2.23 to be valid.

In order to evaluate the thermal resistance of the BOX using Equation 2.23 the value of thermal conductivity of SiO_2 was taken from [79]. The value of the thermal conductivity in a Si film is not precisely known as it depends on a number of factors including the doping concentration, thickness and the temperature [127]. There are a number of publications exploring the thermal conductivities in Si over a wide range of temperatures, film thicknesses and doping levels [128–130]. Using the data from the literature and applying Mathiessen's rule [126] to evaluate the thermal conductivity for the specified Si thickness and doping concentration (150 nm and 10^{18} cm^{-3}, respectively), thermal conductivity is found to be ~50 $W \cdot m^{-1} \cdot K^{-1}$. The obtained normalised thermal resistance from Equation 2.23 is 0.1 $K \cdot m \cdot W^{-1}$. As described, this analytical approach assumes that the device thermal resistance only originates in the BOX and that the metal contacts do not contribute to heat evacuation through the source and the drain. This model also does not account for the thermal resistance caused by the Si film-BOX and the BOX-

substrate interfaces. However, each of these interfaces is in series with the thermal resistance of the BOX and can effectively increase the thermal barrier by ~40 nm [126]. Moreover, this model neglects the thermal resistance of the Si substrate which is in series with the BOX thermal resistance. Furthermore, this model does not account for the reduced thermal conductivity of the BOX. Values in literature are given for bulk SiO_2, while the thermal conductivity tends to reduce as the thickness decreases. Therefore, even if the above model is applicable (i.e. the drain is longer than 1.5 μm), the real value of the BOX thermal resistance may be significantly higher than the extracted value of 0.1 $K \cdot m \cdot W^{-1}$.

2.6 Discussion

Figure 2.21 shows the variation of the lumped device temperature with power extracted with different techniques. The normalised thermal resistance is obtained from the linear fitting of the data forced to 25 °C at zero power. Firstly, the obtained temperatures are reasonable as temperatures higher than 100 °C are expected in SOI devices at such power levels [79], [110], [113] thus giving validity to the methods. Secondly, as expected, the temperature increases with increasing power in case of all extraction techniques, which proves their consistency. Thirdly, the data for three identical devices are grouped together which proves good cross-wafer uniformity and little scattering introduced by each of the extraction methods.

All the experimental self-heating extraction techniques provide information only about the lumped (average) temperature in a device. However, there is a temperature gradient in a device. The drain side of a device is hotter due to the higher power density. In devices with multiple fins in parallel, heat is more efficiently evacuated from the outer fins than from the inner ones [79].

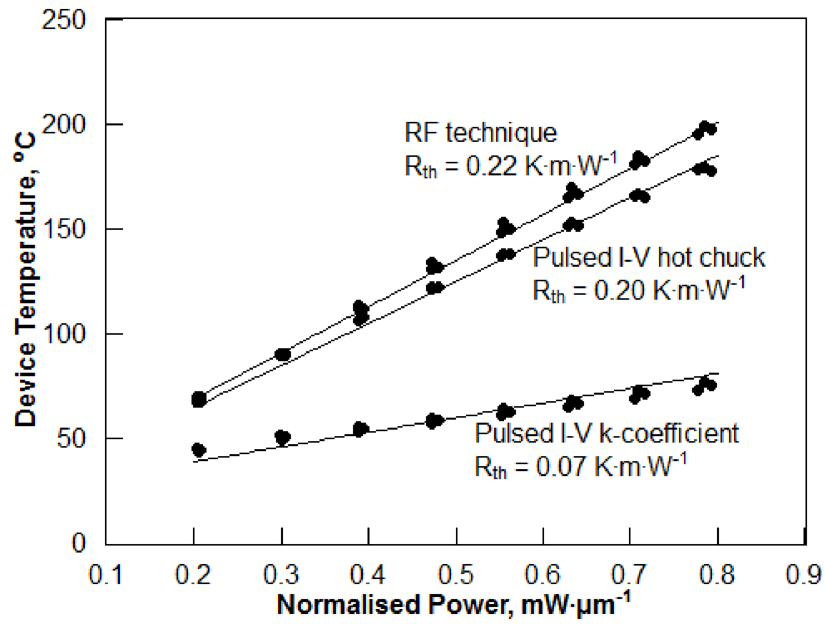

Figure 2.21. The average device temperature variation with normalised power extracted with various self-heating characterisation techniques. The normalised thermal resistance is estimated from linear fitting of the data.

As seen from Figure 2.21, the RF technique and the pulsed *I-V* hot chuck technique produce very similar values of the temperature rise and the thermal resistance. Both of these techniques use fewer assumptions than the other methods. For example, they do not require any assumptions about the heat removal paths or current degradation mechanism. Therefore, they are considered to be more accurate.

However, it is unlikely that the pulsed *I-V* method can be reliably applied for characterising self-heating in more advanced devices. In [96] self-heating was primarily characterised using the RF method. The pulsed *I-V* method with 100 ns-wide pulses was also assessed and it was concluded that the 100 ns pulses were too long. This method with shorter pulses will be tested for advanced devices later in the thesis (Section 5.3.4). Due to technical limitations the minimum pulse width is restricted to a few tens of nanoseconds (or few MHz if translated into frequency domain). This is unlikely to be sufficient for state of the art devices, where the time constants reduce as devices scale down [79]. Additionally, the pulsed *I-V* technique is restricted to devices with a range of gate widths due to the current resolution and limit of the drain voltage pulse. The latter limitation is particularly important for multiple fin devices where the total gate width can be large. Also, the pulsed *I-V* method imposes limits on the off-current of characterised devices.

The RF method has an advantage over the pulsed *I-V* technique as it covers a wide range of frequencies (at least up to tens of GHz). Also it allows a direct extraction of the thermal capacitance using the approach reported in [95] from the variation of the total drain capacitance with frequency. However, the RF technique has some limitations. This technique is sensitive to the accuracy in extracting $\partial I_d/\partial T_A$. Furthermore, the RF technique can be applied only for relatively high gate voltages, where the drain current variation with temperature is dominated by the mobility degradation. However at high gate voltages, the drain current can be strongly affected by the series resistance. This results in a weaker drain current dependence on temperature and hence overestimated thermal resistance and temperature rise in the channel. Another limitation of the RF technique is due to the self-heating-related transition of the output conductance being not easily distinguishable in the frequency characteristics. Output conductance transitions caused by other effects such as the floating body, substrate effects and gate resistance may overlap with the self-heating transition. Especially in thin BOX devices, the transition due to the substrate effects may be comparable with the transition due to self-heating. This is investigated further in Chapter 3.

As seen from Figure 2.21, the *k*-coefficient method results in much smaller values for the thermal resistance and temperature in the devices. This may be caused by several factors. Firstly, the drain current proportionality with mobility might not hold for all bias conditions. Secondly, it is problematic to estimate the value of the mobility temperature coefficient precisely. It is obtained from mobility extraction at various temperatures and therefore depends on the quality of the mobility extraction technique. In this work and in [19], [85] the mobility was extracted using the $I_d/\sqrt{g_m}$ method [118] which has its own limitations, especially in devices with considerable series resistance. More advanced mobility characterisation techniques are available [131] which can be used to improve mobility extraction and may help accuracy of the method. It is difficult to estimate the effective gate length in the PDSOI devices as halo implants were used. The effective gate length is required for the mobility extraction and its value is temperature dependent. In this work the effective gate length was assumed to be equal to the gate length defined by the mask and was considered constant in the entire temperature range. These assumptions introduce an error in the extraction of mobility and the *k*-coefficient. If the lowest value of *k* reported in literature (0.8 in [92]) is used to extract the temperature rise in the devices studied in this work, the resulting device temperature is 36% higher than the value extracted here. However this value is still much lower than those extracted by the RF or the pulsed *I-V* hot chuck method.

The k-coefficient method was used by Rodriguez *et al.* in [92] to characterise self-heating in UTB devices with 145 nm thick BOX. The temperatures extracted in [92] were quite low compared with theoretical predictions [81]. This suggests that the k-coefficient method might underestimate self-heating in SOI devices. The results in [92] will also be compared with thermal properties of UTBB devices with an ultra-thin BOX. Thinner BOX in UTBB is expected to improve thermal properties and this is investigated in Chapter 5.

The one-dimensional analytical model of the thermal resistance associated with the BOX was described in Section 2.5. This model cannot be reliably used to estimate the thermal resistance of the devices due to a number of reasons. Firstly, it does not account for the thermal resistance of the Si substrate under the BOX. Secondly, it does not account for the size effects in BOX, i.e. thermal conductivity reduction in BOX compared with bulk SiO_2. Thirdly, this model does not account for the interface effects. Fourthly, the thermal conductivity of the Si film used to calculate the thermal resistance using the model is only roughly estimated using the approach described in [126], as information about the thermal conductivity of the Si film for specific thicknesses and doping levels is lacking. Finally, other thermal paths which exist in SOI MOSFETs are also not taken into account. A considerable amount of heat might be removed through the source and drain extensions and the gate stack. This is especially relevant for more advanced devices with thinner Si body and shorter gate lengths [81], [92], [126].

Both the RF and the pulsed I-V methods are associated with a thermal time constant. From an equivalent circuit perspective (see Figure 2.19) the thermal time constant τ_{th} is a product of the thermal resistance R_{th} and thermal capacitance C_{th} according to Equation 2.19. Using an empirical approach, the thermal time constant can be extracted as explained in Section 2.4.2.2.4. Results of both extraction techniques were shown in Figure 2.20. Both of these approaches are applicable for frequency domain characterisation.

In the time domain techniques, the thermal time constant can be roughly related to the pulse width. In this work the drain current variation with the pulse width is no longer observed for the pulses under 50 ns as seen in Figure 2.4. Therefore, self-heating is removed when the pulse width is between 50 ns and 100 ns. In order to compare the two self-heating characterisation approaches (in time and frequency domain), the pulse width can be roughly translated into the frequency according to:

$$f = \frac{1}{2\pi\tau_p}, \tag{2.25}$$

where τ_p is the pulse width and f is the corresponding frequency. However, a pulse is formed of a number of different harmonics; therefore relating the pulse width to a single frequency is not exact and does not allow a direct comparison. One can use a Fourier transform to relate the time domain to the frequency domain. Figure 2.22 shows the output conductance variation with frequency in the devices. The corresponding pulse widths are also indicated as obtained using Equation 2.25. The frequency related to the 50 ns pulse is very close to the frequency at which the output conductance plateau (indicating removal of dynamic self-heating) is observed. Note that the characteristic frequency f_{th} used for the empirical extraction of the thermal time constant (as in [94]) is much lower than the frequency at which dynamic self-heating is removed.

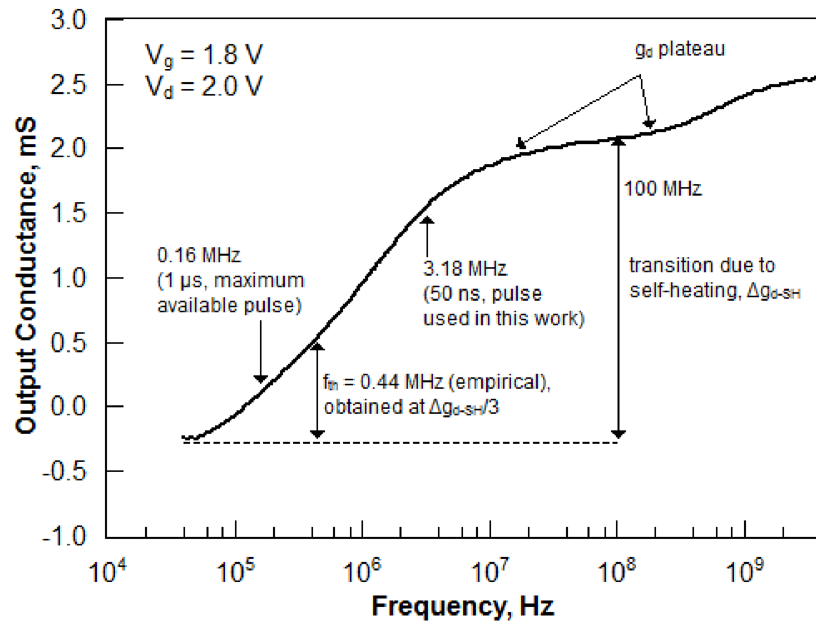

Figure 2.22. The output conductance variation with frequency obtained with the RF technique at V_g = 1.8 V and V_d = 2.0 V. Corresponding pulse widths (estimated) are shown on the curve.

Figure 2.23 shows the thermal time constants for various power levels extracted using the results obtained from the RF technique. An empirical method suggested by Jin *et al.* [94] is compared with the thermal time constant obtained from Equation 2.19. In Equation 2.19 the thermal time constant is obtained from the product of the thermal resistance and the thermal capacitance. From the pulsed *I-V* data, self-heating is removed when the pulse width is between 100 ns and 50 ns (see Figure 2.4). To relate the extracted thermal time constants with the pulsed *I-V* extraction, 50 ns and 100 ns lines are marked in Figure 2.23.

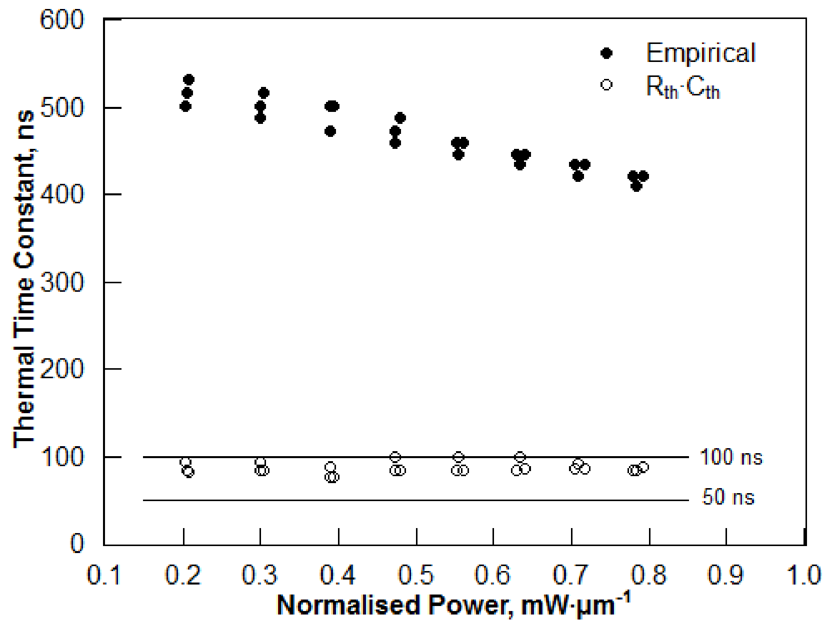

Figure 2.23. Variation of the thermal time constants with normalised power extracted from RF characterisation in three identical devices. 50 ns and 100 ns lines are shown.

As seen from Figure 2.23 the thermal time constant obtained from the product of the thermal resistance and thermal capacitance is lower than the one extracted using the empirical approach. If it is translated into frequency using Equation 2.21 then the frequency is ~1.8 MHz. This value is closer to the frequency at which the dynamic self-heating is removed than the characteristic frequency f_{th} used in the empirical approach. Also, the power dependency of the thermal time constant is not expected, at least in the first approximation.

Knowledge of the thermal time constant can be of interest for devices that operate at various frequencies or at transient conditions. It also helps to choose a suitable technique for characterisation of thermal properties. If the thermal time constant is treated as a product of the thermal resistance and thermal capacitance, then it is related to the surface-to-volume ratio which significantly increases in advanced semiconductor devices such as FinFETs [79] and nanowires [111]. The thermal resistance is related to the surface area which is used for heat evacuation while the thermal capacitance is related to the volume which is available to store the heat. Therefore, an increase of the surface-to-volume ratio results in the reduction of the thermal time constants in modern technologies [79]. Hence, the reduction of thermal time constants is expected as technology moves from PDSOI to more advanced FDSOI such as UTB, UTBB, FinFETs and nanowires. This suggests that frequency domain self-heating characterisation techniques should be used for characterisation of advanced devices as they can accommodate smaller thermal time constants.

During on-wafer measurements, parasitics associated with the probes and device pads aggravate accuracy as signal frequencies are increased above few MHz. Therefore, devices for on-wafer characterisation must be embedded in GSG pads and probed with RF probes in order to minimise parasitic effects for reliable self-heating assessment.

2.7 Summary

Self-heating has been assessed in PDSOI devices with 400 nm-thick BOX using time and frequency domain techniques. Two common approaches of self-heating characterisation in time domain using the pulsed *I-V* technique were considered. One is based on the pulsed *I-V* measurements at different temperature and the other assumes current degradation with temperature being caused by the mobility variation with temperature only. The RF self-heating extraction method is a frequency domain technique and was also considered in this work as well as a simple one-dimensional analytic model.

It was experimentally verified that the RF and the hot chuck pulsed *I-V* techniques provided similar values of the average temperature rise and lumped thermal resistance in the PDSOI devices. However, the RF method can be used for self-heating characterisation in state of the art devices while the pulsed *I-V* method is at its limit. The reduction of the thermal time constants in advanced devices limits the applicability of the pulsed *I-V* technique because such short pulses are not currently available. The RF technique might be applied at very high frequencies covering MHz-GHz range where the dynamic self-heating effect is removed in advanced MOSFETs.

Besides its potential for characterisation of the thermal properties in advanced MOSFETs, the RF technique can be used for thermal characterisation of bipolar transistors and allows direct extraction of the thermal capacitance. However, the RF technique requires consideration of the zero temperature coefficient and, therefore, can only be applied when a device is biased in saturation.

The pulsed *I-V* technique can be applied for thermal characterisation of devices with thermal time constants of ~100 ns or more. It is suggested that this technique with the pulse width of few tens of nanoseconds can be successfully applied to most PDSOI devices. However, in most of the advanced FDSOI devices (UTB, UTBB, FinFETs) self-heating might be underestimated if the pulsed *I-V* approach is used.

It was also shown that the pulsed *I-V* self-heating extraction based on the mobility degradation coefficient might underestimate self-heating in PDSOI devices. This is because it is

difficult to extract an accurate value of the mobility degradation coefficient and multiple output current degradation mechanisms might exist. However, the pulsed *I-V* method combined with the hot chuck measurements, though being more complex and time consuming, is more reliable as it uses fewer assumptions.

For reliable on-wafer characterisation devices must be embedded in GSG pads and probed with RF probes to reduce contribution of parasitics.

In Chapter 5 and Chapter 6 thermal properties of UTBB devices and FinFETs are quantified using the RF technique, since the RF method is found to be the most appropriate technique for self-heating characterisation in FDSOI devices. In Chapter 5 the pulsed *I-V* hot chuck method is also compared with the RF technique in order to confirm the findings of this chapter.

Chapter 3. UTBB devices and analogue figures of merit

3.1 Motivation and chapter outline

As was discussed in the introduction of the thesis, UTBB technology is a promising approach to scale planar MOSFETs for the next few generations. However, UTBB devices suffer from self-heating and substrate effects. Both self-heating and substrate effects result in undesirable variation of the output conductance in a wide frequency range. This leads to the frequency-dependent behaviour of MOSFETs which is important for analogue applications. For example, these parasitic effects might result in amplifier gain dependence on the signal frequency. Characterisation of these two effects helps to identify the corresponding trade-offs and possible solutions in order to minimise undesirable effects and optimise device performance, manufacturing cost and complexity. This chapter aims to understand UTBB device behaviour in a wide frequency range. The objective is to identify the output conductance transitions and their dependence on the gate length and applied biases.

This chapter is organised into four main sections. Firstly, the current-voltage characteristics of UTBB devices with 10 nm BOX are shown. Secondly, the key analogue figures of merit of UTBB technology are presented and compared with the analogue figures of merit of various FDSOI devices reported in the literature. Thirdly, the frequency behaviour of UTBB SOI MOSFETs output conductance up to 4 GHz is experimentally analysed. The effect of the device scaling is analysed as devices with gate lengths from 30 to 100 nm are considered. Finally, the influence of both self-heating and substrate effects on the output conductance frequency response as well as their relative importance in UTBB MOSFETs operating at different bias and power conditions is discussed.

3.2 Experimental details

The UTBB devices were fabricated on SOI wafers with a 10 nm-thick BOX and a standard substrate resistivity of 20 Ω·cm. The Si thickness in the channel regions is 7 nm. The channel and the substrate were left undoped. An HfSiON gate dielectric with an equivalent oxide thickness (EOT) of 1.3 nm and TiN electrode form the gate stack. The height of the raised source and drain regions is 15 nm and the total extension length is 25 nm. Transmission electron microscopy image of a UTBB device is presented in Figure 3.1 [132]. The image shows the ultra-thin 7 nm Si body and the 10 nm ultra-thin BOX.

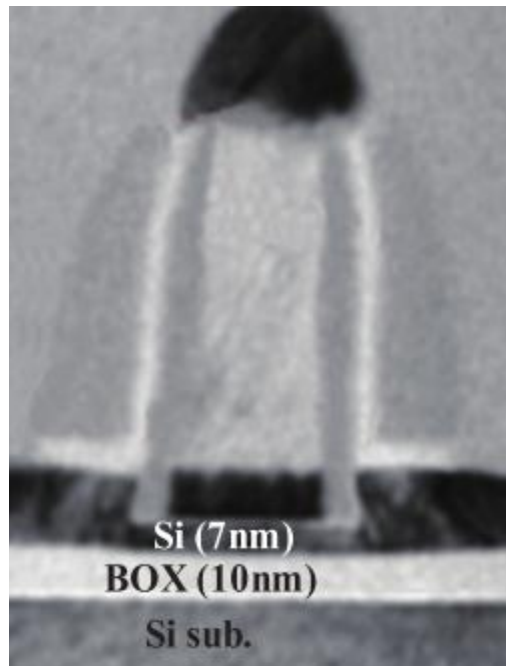

Figure 3.1. Transmission electron microscopy image of the cross-section of a UTBB device showing 7 nm-thick Si body and 10 nm-thick BOX. The image adapted from [132].

In order to extract analogue figures of merit, nMOSFETs with gate lengths L_g from 30 nm to 10 µm and finger widths from 80 nm to 10 µm were characterised. The devices where contacted through DC pads. The analogue figures of merit were extracted from DC characteristics obtained with an Agilent B1500A semiconductor device analyser.

For the RF characterisation devices were embedded in coplanar waveguide access pads in 100 µm pitch GSG configuration. The characterisation was carried out in n-channel MOSFETs with gate lengths ranging from 30 nm to 100 nm. Multi-finger devices with various finger widths W_g and number of parallel fingers N_{fin} were available for the RF characterisation.

For the RF characterisation *S*-parameters were extracted using a Rohde & Schwarz ZVR vector network analyser (VNA) from 40 kHz to 4 GHz. The *S*-parameters were de-embedded and converted into *Y*-parameters as was shown in Section 2.4.2.1. The frequency response of the output conductance was obtained from the real part of the Y_{dd} parameter. The measurements were performed over a wide range of applied gate and drain biases, V_g and V_d, respectively. Static characteristics, including DC output conductance values, were obtained with an Agilent B1500A semiconductor device analyser.

3.3 Results and discussion

3.3.1 Current-voltage characteristics

The UTBB devices were fabricated on a 300 mm wafer which was subsequently quartered. Figure 3.2, Figure 3.3 and Figure 3.4 show transfer characteristics of 30, 50 and 100 nm gate length UTBB devices at the drain voltage of 1.0 V for a number of devices across the wafer. The outliers were not considered. The shown characteristics were obtained in the devices with GSG pads which were subsequently used for the RF characterisation.

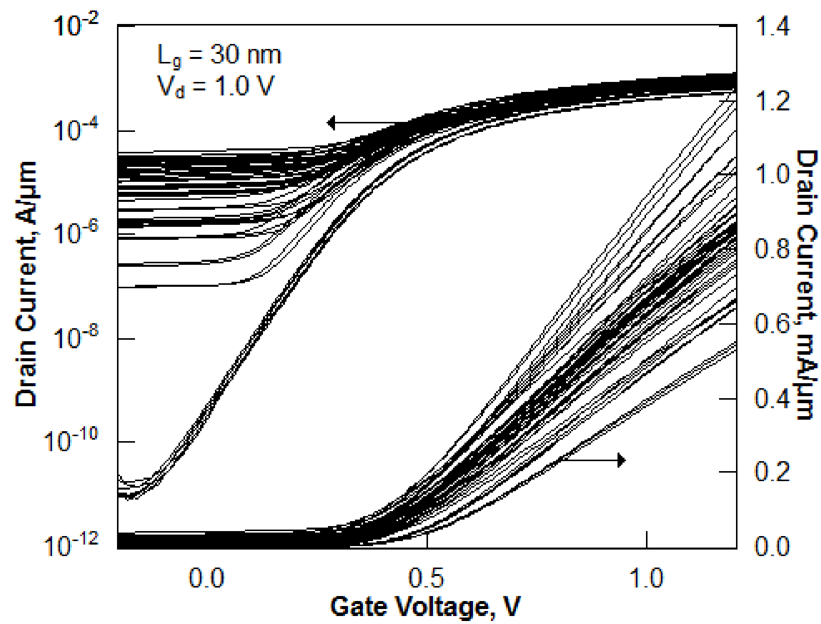

Figure 3.2. Transfer characteristics of 30 nm gate length UTBB devices at $V_d = 1.0$ V.

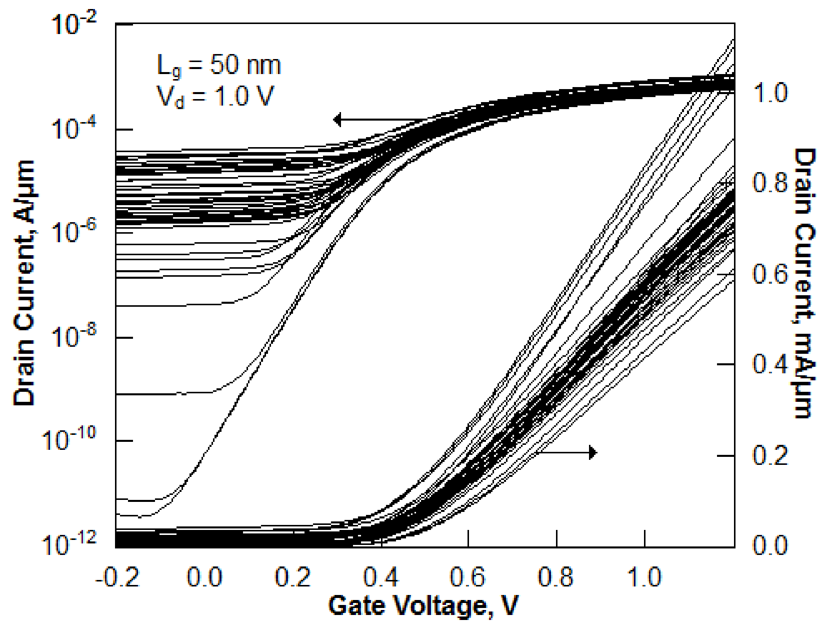

Figure 3.3. Transfer characteristics of 50 nm gate length UTBB devices at V_d = 1.0 V.

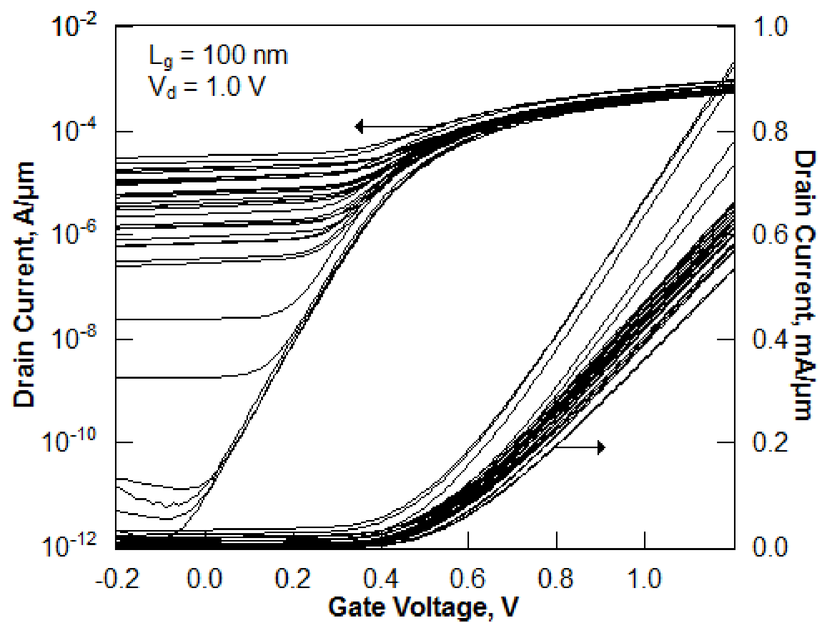

Figure 3.4. Transfer characteristics of 100 nm gate length UTBB devices at V_d = 1.0 V.

Figure 3.5 shows the comparison between the off-state drain current (V_g = 0 V, V_d = 1.0 V) and the on-state drain current (V_g = V_d = 1.0 V) in the UTBB devices with 30, 50 and 100 nm gate lengths. As expected, the on-state drain current increases as the gate length reduces (agrees with Equation 1.3) as most of the data points are grouped according to the gate length along horizontal axis. However, there is no strong correlation between the off-state drain current and the gate length as the data points are equally dispersed along the vertical axis for all gate lengths.

Unexpectedly, devices with the higher off-state current were located closer to the centre of the wafer while devices with the lower off-state current were closer to the edges. This might be related to uneven distribution of materials used in the fabrication process.

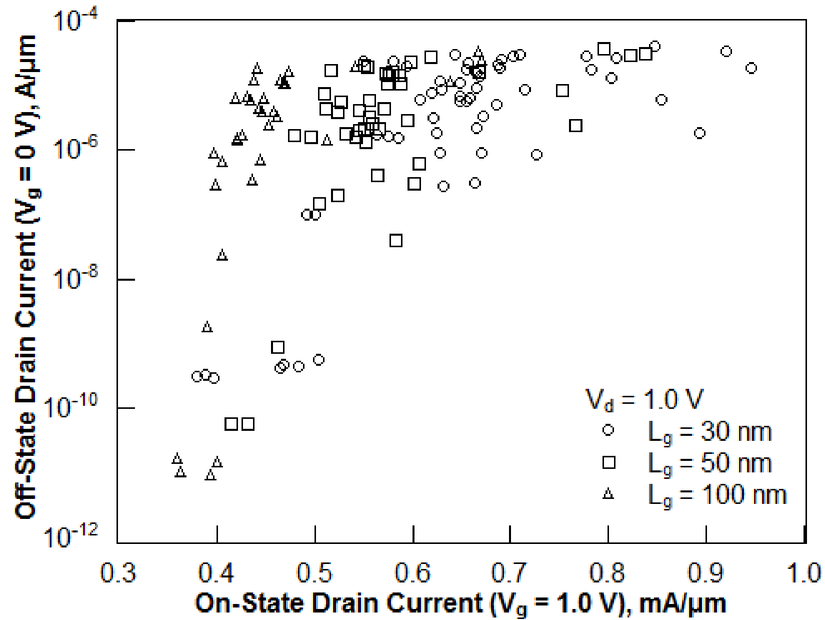

Figure 3.5. Off-state drain current (V_g = 0 V) compared with the on-state drain current (V_g = 1.0 V) in UTBB devices with 30, 50 and 100 nm gate lengths at V_d = 1.0 V.

Figure 3.6 presents a box plot with the statistical data for the drain current at $V_g = V_d = 1.0$ V in devices with 30, 50 and 100 nm gate lengths. The range of all values from minimum to maximum (shown with the crosses in Figure 3.6) is approximately the same for all three gate lengths. As expected, the mean value of the drain current increases (indicated with the squares in Figure 3.6). The dispersion of values that occur in the 25% – 75% range (shown with the boxes in Figure 3.6) in 100 nm gate length devices is considerably lower than in 30 nm and 50 nm gate length devices. This can be caused by some fabrication-induced fluctuations in device dimensions which are relatively stronger in shorter devices. In order to improve overall dispersion of device characteristics, better control of the fabrication process is required.

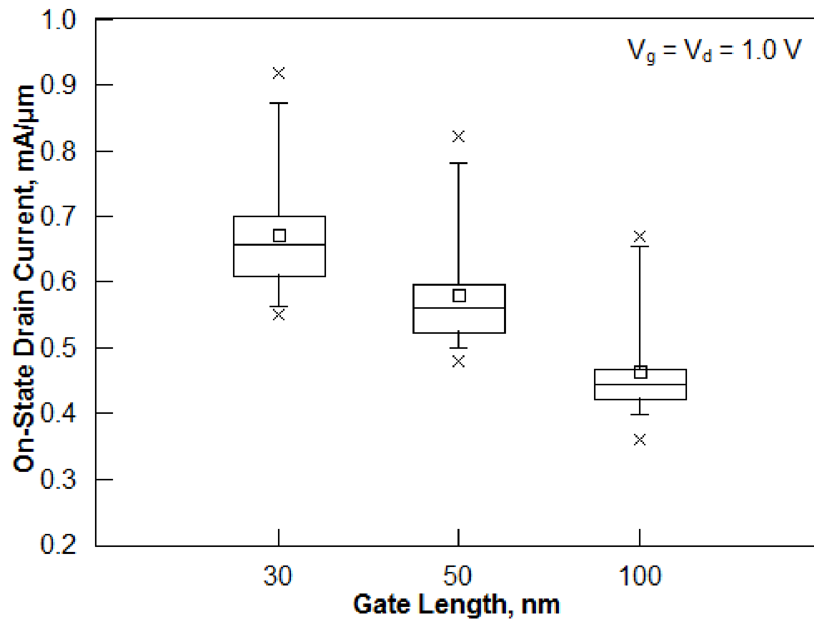

Figure 3.6. Statistical plot of the on-state drain current at $V_g = V_d = 1.0$ V in UTBB devices with 30, 50 and 100 nm gate lengths. The squares show the mean value. The boxes represent the range where 25% - 75% of the values occur. The whiskers show the range where 5% - 95% of the values occur. The crosses indicate the minimum and maximum values.

For further characterisation, 30, 50 and 100 nm gate length UTBB devices with low off-state current were chosen. These devices showed lower on-state drain current than devices with the higher off-state drain current as seen from Figure 3.5. However, these devices exhibited less parasitic leakage, including leakage through the substrate. Due to the ultra-thin BOX, the leakage through the substrate is considerable and might complicate extraction of the output conductance frequency response which is required for accurate self-heating and substrate effects characterisation.

Figure 3.7 shows typical transfer characteristics of the selected UTBB devices with the gate lengths 30, 50 and 100 nm at the drain voltages 20 mV and 1.0 V. Comparable characteristics were previously reported for UTBB devices in [33]. Threshold voltages, V_{th}, extracted in the linear regime at a drain voltage $V_d = 20$ mV were shown to be ~0.38-0.40 V.

As expected, reduction of the gate length results in stronger short channel effects, such as the drain induced barrier lowering (DIBL). Increased DIBL can be observed from the increased separation between low and high drain voltage curves. Also, reduction of the gate length leads to an increase in the off-current as evident from Figure 3.7.

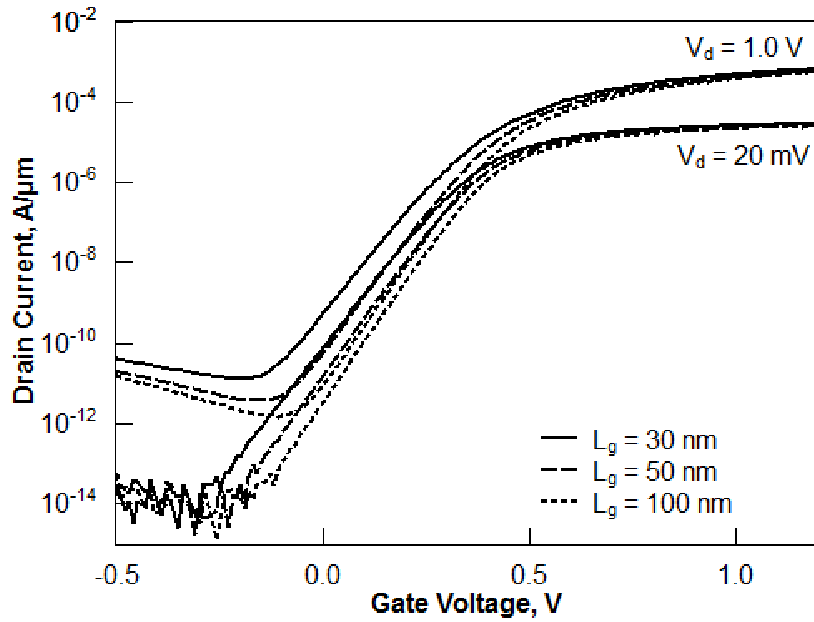

Figure 3.7. Transfer characteristics of the selected UTBB devices with the gate lengths 30, 50 and 100 nm at V_d = 20 mV and V_d = 1.0 V.

3.3.2 Analogue figures of merit

Analogue performance of UTBB devices is assessed through analysis of the normalised transconductance maximum, the Early voltage and the intrinsic gain.

3.3.2.1 Transconductance

The transconductance is used as an analogue figure of merit as it indicates the efficiency of the voltage conversion into the effective current. Higher values of the transconductance mean higher efficiency of the MOSFET. The maximum transconductance was normalised to the gate width and length as in:

$$g_{m-max-norm} = \frac{g_{m-max}}{W_g / L_g}, \tag{3.1}$$

where $g_{m\text{-}max}$ is the maximum transconductance, L_g is the gate length and W_g is the total gate width.

Figure 3.8 shows variation of the maximum transconductance for the UTBB devices with gate lengths from 30 nm to 250 nm and widths of 80 nm and 10 μm. For comparison, the value of the

transconductance maximum reported in [133] for a UTB device with 145 nm-thick BOX is indicated with a cross. Typical degradation of the normalised transconductance maximum is observed for very short gate lengths, as a result of short channel effects and stronger impact of the series resistance with the gate length scaling. Devices with 80 nm-wide channels exhibit up to twice higher normalised transconductance maximum compared with 10 μm-wide devices. This is due to trapezoidal or even omega-like channel cross-section [10]. Such channel shapes result in a larger effective channel width, thus enhancing the performance, and improved body factor as similarly reported previously for FinFETs [134].

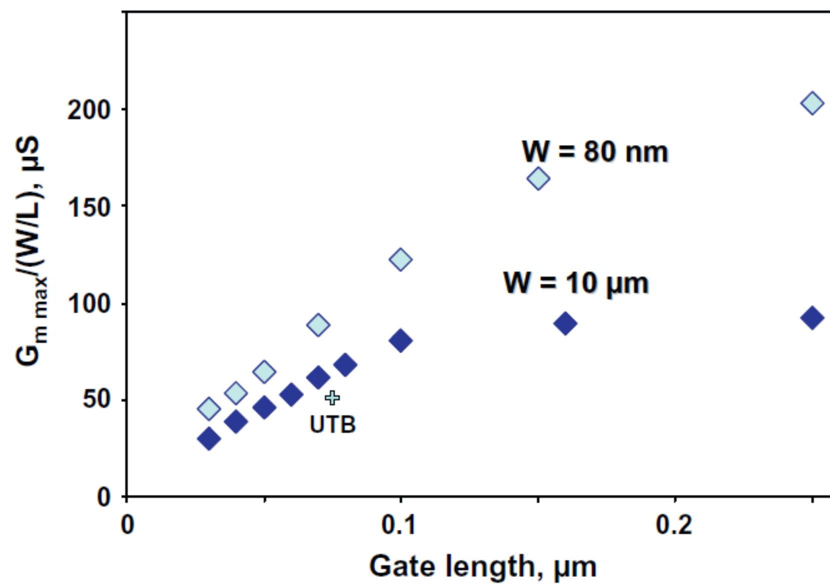

Figure 3.8. The normalised transconductance maximum as a function of the gate length in UTBB devices with channel widths of 80 nm and 10 μm. The cross indicates the value reported previously for a UTB device with BOX thickness of 145 nm [133].

3.3.2.2 Early voltage

The Early voltage is a figure of merit indicating the efficiency of a device to convert the DC power into the gain performance [135]. Use of the Early voltage as a figure of merit enables fair comparison between different devices at various bias conditions as dependence of the output conductance on the drain current is eliminated. Schematically the Early voltage is shown in the output characteristics in Figure 3.9. The slope of the drain current variation with the drain voltage indicates the output conductance. Therefore, the ratio of the drain current and the output conductance can be used to obtain the Early voltage:

$$V_{EA} = \frac{I_d}{g_d}, \qquad (3.2)$$

where V_{EA} is the Early voltage and I_d is the drain current. Though the drain current used in this calculation was obtained in the saturation regime, it can be reliably used to extract the Early voltage when the Early voltage is much larger than the saturation drain voltage.

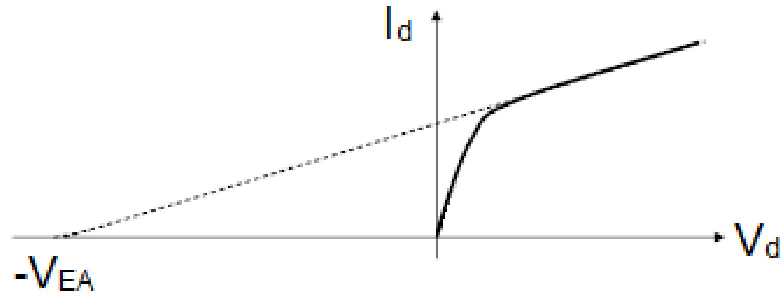

Figure 3.9. Schematic output characteristics showing the Early voltage.

Figure 3.10 reports the Early voltages measured in the UTBB devices with gate lengths from 30 nm to 10 µm at V_g = 0.4 and V_g = 1.0 V, V_d = 1.0 V. It is shown that the Early voltage can be as high as 800 V in long-channel UTBB devices. This is an extremely high value for planar FDSOI MOSFETs which typically exhibit values of the Early voltage of ~10 V per µm of the gate length (shown by the dashed line in Figure 3.10). Such high values of the Early voltage are similar to the ones previously observed in FinFETs (~10^3 V) [76], [136], [137]. The improvement in the Early voltage is caused by the volume inversion regime of operation and improved gate control of the charge in the channel.

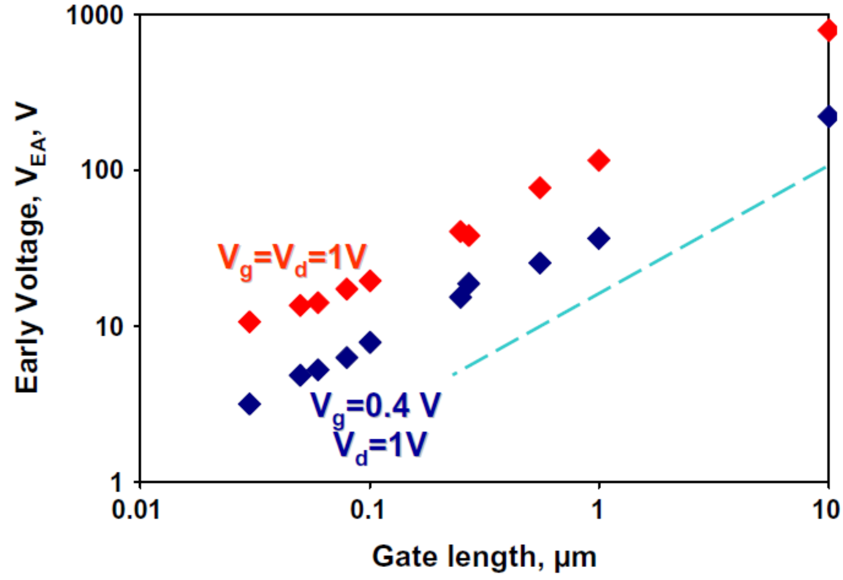

Figure 3.10. The Early voltage as a function of the gate length in UTBB devices at different bias conditions. Channel width is 10 µm. The dashed line indicates typical values for planar FDSOI MOSFETs.

3.3.2.3 Intrinsic gain

The intrinsic gain is an analogue figure of merit indicating the efficiency of the conversion from the input voltage to the output voltage. Therefore, higher values of the intrinsic gain are wanted. Very high values of intrinsic gain are recorded in the UTBB devices as a result of the high Early voltage (as shown in Figure 3.10). The intrinsic gain is proportional to the Early voltage and can be obtained from:

$$A_v = \frac{v_d}{v_g} = \frac{i_d/g_d}{i_d/g_m} = \frac{g_m}{g_d} = \frac{g_m}{I_d} V_{EA}, \tag{3.3}$$

where A_v is the intrinsic voltage gain and g_m is the transconductance.

An intrinsic gain of ~80 dB was achieved in the studied 10 µm gate length device, thus approaching the values previously reported for long-channel FinFETs [136], [137]. Such high values were never previously observed for planar FDSOI MOSFETs.

Figure 3.11 shows the intrinsic gain in short devices with the gate length of 30 nm at gate and drain voltages from 0.2 V to 1.4 V. According to Equation 3.3, the gain is proportional to g_m/I_d which reduces with increased gate voltage. The gain is also proportional to the Early voltage which increases with the gate voltage as shown in Figure 3.10. Therefore, the intrinsic gain reaches its maximum value in the moderate inversion regime at around threshold (V_g = 0.4 V)

which is beneficial for low voltage and low power applications. In saturation the intrinsic gain reaches the plateau as the drain voltage is increased (circled in Figure 3.11).

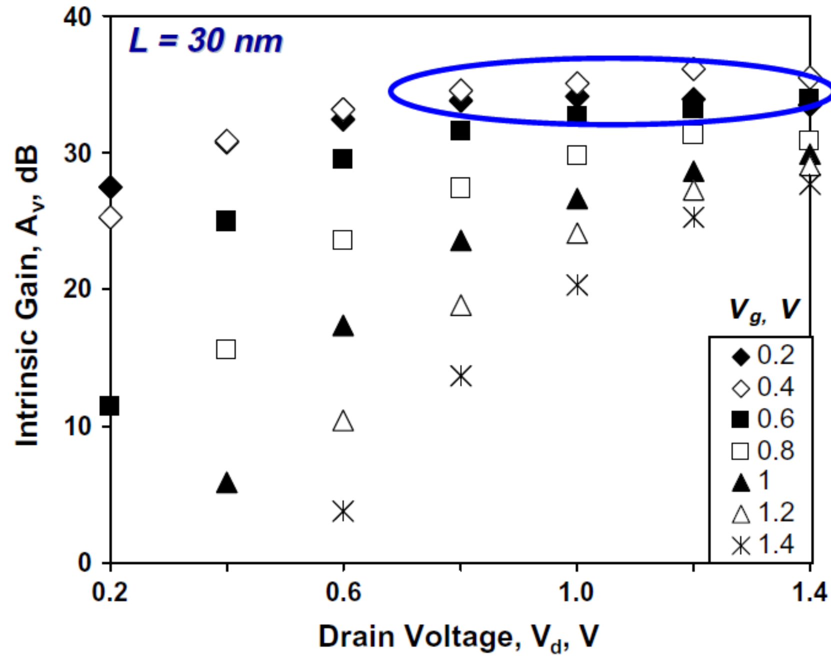

Figure 3.11. The intrinsic gain as a function of applied drain and gate voltages in 30 nm gate length UTBB devices with a channel width of 10 μm.

3.3.2.4 Benchmarking

UTBB technology was benchmarked with other FDSOI technologies. The normalised transconductance maximum, the drive current and the intrinsic gain of UTBB devices were compared with analogue figures of merit published in the literature. Considered technologies were: 0.12 μm-node planar FDSOI MOSFET with doped channel and halo doping [135], [138], [139], FinFETs with doped channel [65], [136], [137], [140], undoped FinFETs with and without global biaxial tensile strain [141], [142] and UTB MOSFETs [43], [133]. The main process details of the aforementioned technologies are summarised in Table 3.1.

Table 3.1. Process details of the benchmarked technologies.

Devices	Gate stack materials	EOT, nm	Body thickness, nm	Channel doping, cm^{-3}	BOX thickness, nm	References
FDSOI MOSFET	Poly-Si/SiO_2	2.5	30	7×10^{17} + halo	200	[135], [138], [139]
Doped FinFETs	Poly-Si/SiO_2	2.0	35	$(1–6)\times10^{18}$	145	[65], [136], [137], [140]
Undoped FinFETs	Metal/HfSiON	1.5	25	Undoped	145	[141], [142]
Strained FinFETs	Metal/HfSiON	1.5	25	Undoped	145	[141], [142]
UTB MOSFETs	Metal/HfO_2	1.7	8	Undoped	145	[43], [133]
UTBB MOSFETs	Metal/HfSiON	1.3	7	Undoped	10	This work

Figure 3.12 shows benchmarking of the normalised transconductance maximum for devices described in Table 3.1. Figure 3.13 presents normalised drain current taken at g_m/I_d = 5 V^{-1} in order to eliminate dependence on the threshold voltage and in the first order on the gate length [135], [143]. The drain current is normalised to both gate width and length. All devices compared in Figure 3.12 and Figure 3.13 feature a gate length of 100 nm, except of planar FDSOI MOSFET and UTB MOSFETs. The gate length reported for the planar FDSOI MOSFET is 0.12 μm. In UTB MOSFETs the gate length is 70 nm.

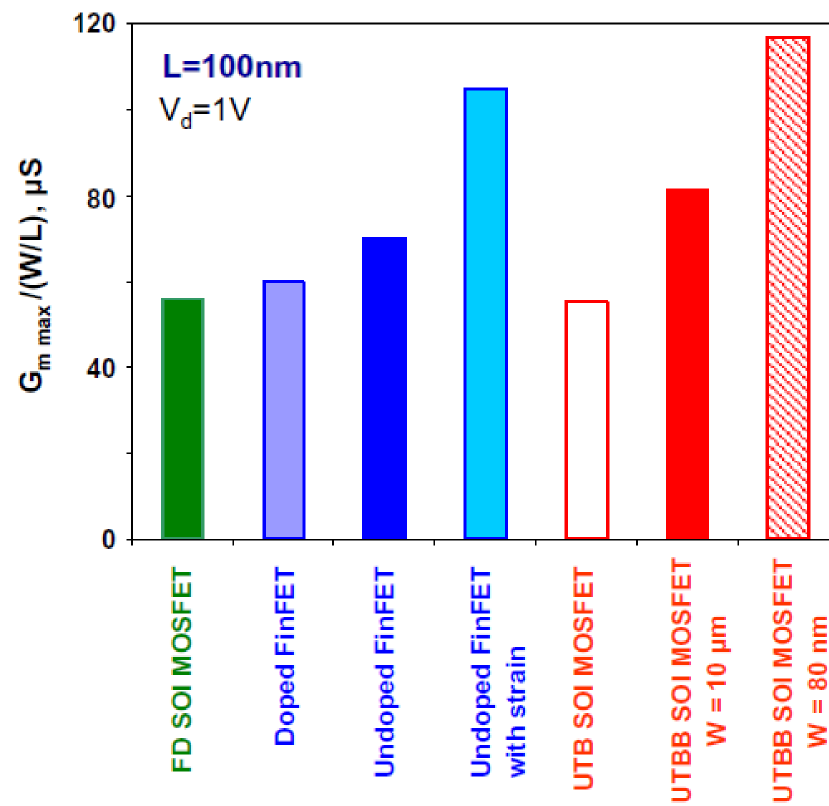

Figure 3.12. Normalised transconductance maximum in the devices listed in Table 3.1 at V_d = 1.0 V. L_g = 100 nm (except in FDSOI MOSFET L_g = 120 nm and in UTB MOSFET L_g = 70 nm).

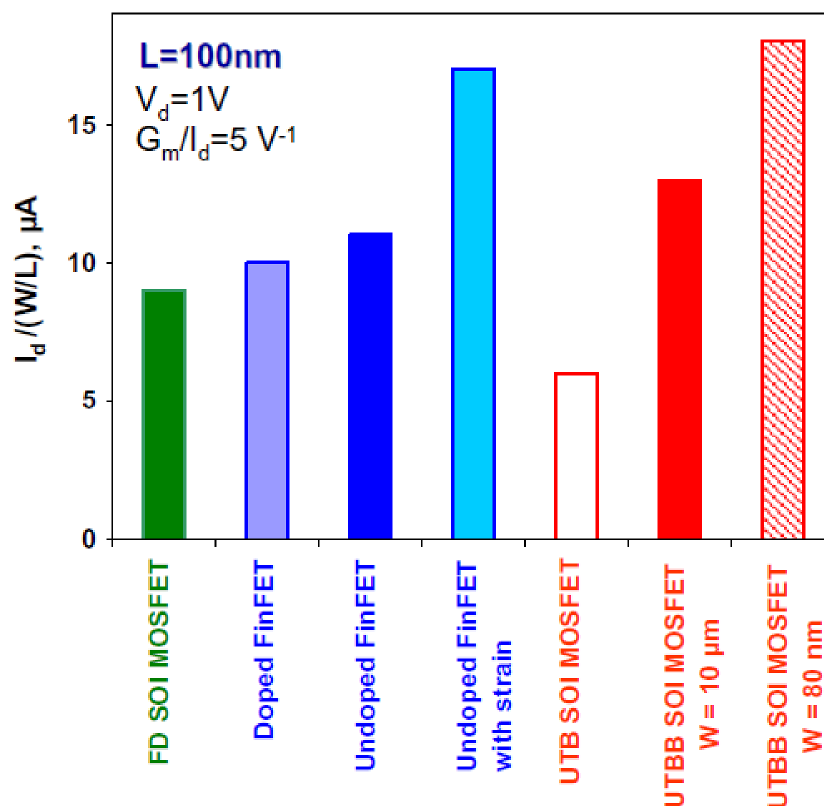

Figure 3.13. Normalised drain current at g_m/I_d = 5 V^{-1} in the devices listed in Table 3.1 at V_d = 1.0 V. L_g = 100 nm (except in FDSOI MOSFET L_g = 120 nm and in UTB MOSFET L_g = 70 nm).

Firstly, UTBB MOSFETs exhibit higher values of the transconductance and the drain current than planar doped FDSOI devices from the 0.12 µm process. This improvement is due to the following reasons. Undoped channel in the UTBB devices results in higher mobility. Electrically thinner gate oxide leads to a higher gate oxide capacitance. A higher gate capacitance is expected to improve the transconductance and the drain current according to Equation 1.2 and Equation 1.3. The thin gate oxide combined with the ultra-thin Si film and BOX improves short channel effects including DIBL [14], [41]. UTBB figures of merit are also higher than these of the doped FinFETs, which have thicker gate dielectrics and bodies (fins), for the same reasons.

Secondly, UTBB devices feature comparable performance in terms of the transconductance maximum and the drive current as the undoped FinFETs. Introduction of the strain leads to a strong improvement of FinFETs performance. Strained FinFETs show ~25% higher analogue figures of merit than 10 µm-wide UTBB devices.

Thirdly, the analogue figures of merit of the UTBB devices are slightly higher than those of UTB devices reported in [43], [133]. This is due to lower EOT which results in higher gate

capacitance. Improved gate capacitance combined with the ultra-thin BOX yields improved control over the short channel effects [14], [41] in the UTBB devices.

Fourthly, the analogue figures of merit in the narrow channel devices are ~35% higher than in the devices with 10 μm-wide channels. The performance improvement is most probably related to the trapezoidal or omega-like channel cross-section in the narrow UTBB channels devices as discussed in Section 3.3.2.1. Such channel cross-section results in the effectively wider gate and improved body factor. Due to this enhancement, narrow-channel UTBB devices outperform all counterparts in terms of the transconductance maximum and the drive current.

Devices listed in Table 3.1 were benchmarked in terms of the maximum intrinsic voltage gain. Figure 3.14 shows the resulting plot. The studied UTBB devices significantly outperform planar FDSOI MOSFETs and doped FinFETs. The intrinsic gain as high as 45 dB is achievable in 100 nm gate length UTBB devices. Furthermore, UTBB devices exhibit higher intrinsic gain than the UTB MOSFETs. This is partially due to improved electrostatic control and reduced short channel effects in UTBB technology. Also it can be due to the fact that the reported values for the UTB MOSFETs were extracted in the GHz frequency range [43], [133] where device performance is expected to degrade.

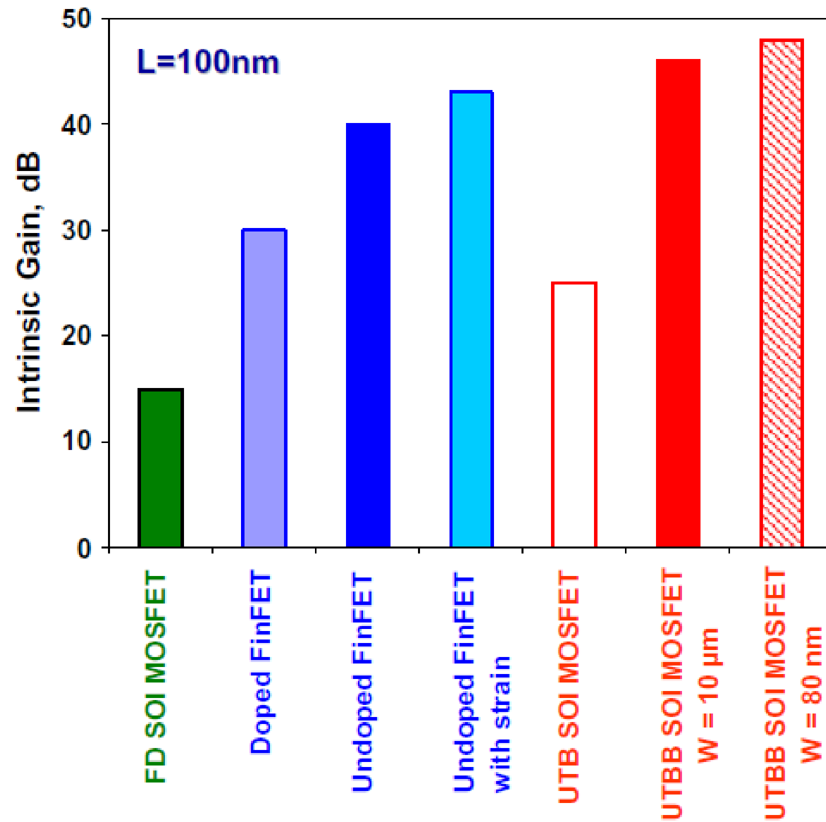

Figure 3.14. Maximum intrinsic gain in the devices listed in Table 3.1. L_g = 100 nm (except in FDSOI MOSFET L_g = 120 nm and in UTB MOSFET L_g = 70 nm).

3.3.3 Output conductance transitions and impact of gate length scaling

In order to understand the output conductance variation over the wide frequency range, RF characterisation was performed in UTBB devices with L_g = 100 nm, W_g = 1 µm, N_{fin} = 30 devices at V_g = 0.6 V, V_d = 1.0 V and V_g = V_d = 1.0 V. Figure 3.15 presents the output conductance variation in the frequency range from 40 kHz to 4 GHz. The output conductance value extracted from the static output characteristics is also indicated in Figure 3.15. The transition of the output conductance due to self-heating occurs between 1 MHz and ~30 MHz, which is slightly higher than reported previously for long-channel FDSOI MOSFETs [84], [94] due to the stronger confinement and higher current level as the gate length is scaled down. Confinement due to the device dimensions results in smaller thermal capacitances and increased interface effects such as phonon boundary scattering [79], [82]. The output conductance transition caused by the inertia of majority carriers in the substrate starts at ~100 MHz and reaches a plateau at a few GHz. The transition due to the inertia of the minority carriers in the substrate can be assumed from the difference between conductance values at DC and 40 kHz and requires additional characterisation covering the frequency range of interest.

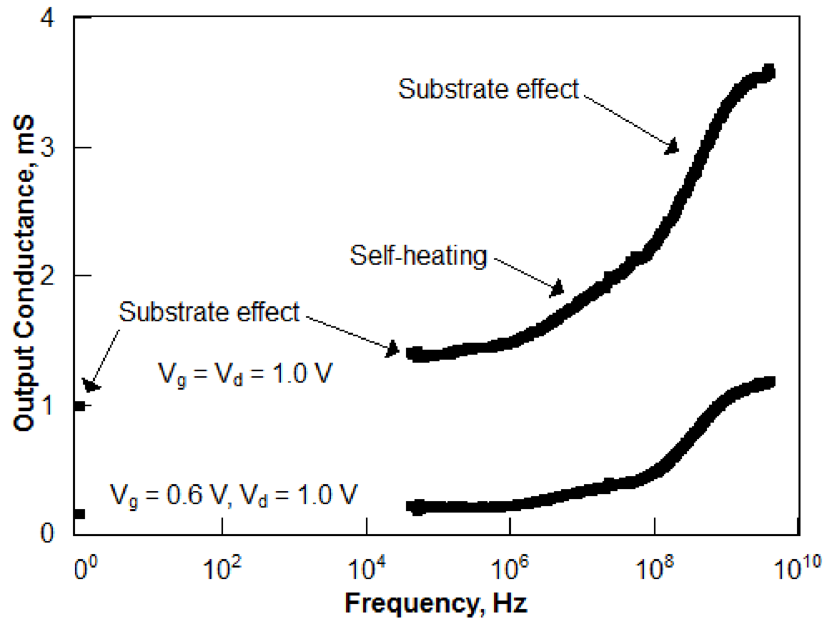

Figure 3.15. Measured output conductance frequency response at V_g = 0.6 V and 1.2 V and V_d = 1.0 V in the UTBB SOI MOSFETs with L_g = 100 nm, W_g = 1 µm and N_{fin} = 30.

Firstly, the extracted DC value of the output conductance is ~3 times smaller than the output conductance values at high frequencies (in GHz range) where neither the dynamic self-heating nor the minority and majority carriers in the substrate can follow the AC signal any longer. Therefore, the performance evaluation of devices for high frequency applications requires wide frequency band characterisation. Secondly, despite its very small thickness (10 nm only), BOX is preventing effective heat dissipation from the channel to the substrate. This is manifested through the output conductance increase with the frequency. In the case of self-heating absence, the output conductance curve is expected to be flat in the kHz-MHz range as shown in Figure 1.7. Thirdly, due to the ultra-thin BOX in the UTBB devices with the undoped substrate, the contribution of the substrate effects becomes greater than that of self-heating. This is evident from the bigger amplitude of the substrate-related output conductance transition. These main experimental trends are confirmed by 2D device simulations shown in Figure 3.16. The simulations were carried out at V_g = 0.6 V, V_d = 1.0 V in devices with Si thickness 7 nm, BOX thickness 10 nm, equivalent gate oxide thickness 1.3 nm, substrate thickness 10 µm and substrate doping 6.5×10^{14} cm^{-3}.

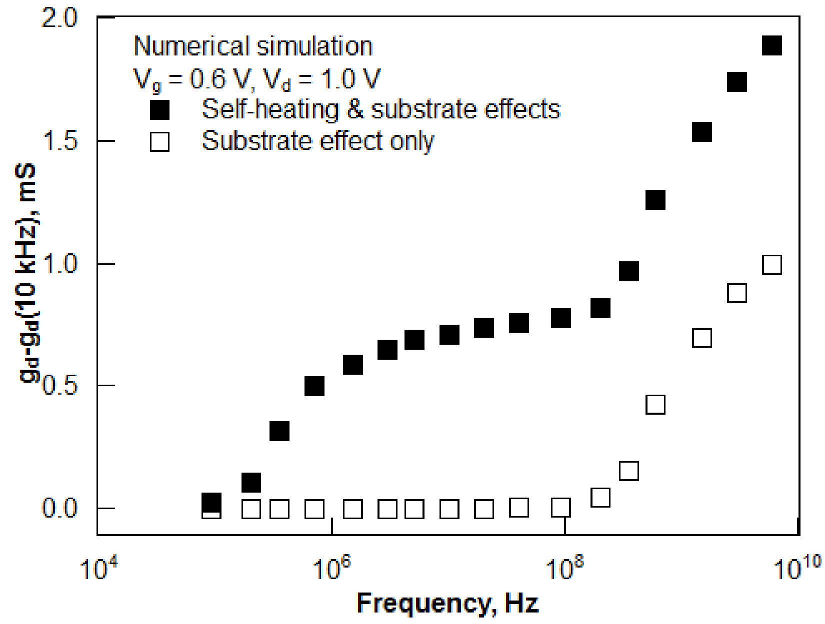

Figure 3.16. Simulated output conductance variation with frequency, showing transitions due to self-heating and majority carriers in the substrate at $V_g = 0.6$ V and $V_d = 1.0$ V. Devices feature 7 nm Si thickness, 10 nm BOX thickness, 1.3 nm equivalent gate oxide thickness, 10 µm substrate thickness and 6.5×10^{14} cm^{-3} substrate doping.

In order to evaluate how the scaling affects output conductance variation with frequency and its transitions, devices with different gate lengths were studied. Figure 3.17 and Figure 3.18 show the conductance variation with frequency for devices with gate lengths of 30, 50 and 100 nm, extracted at around threshold ($V_g = 0.4$ V, Figure 3.17) and at strong inversion ($V_g = 1.2$ V, Figure 3.18), both in the saturation regime ($V_d = 1.2$ V). Figure 3.19 and Figure 3.20 show the self-heating and substrate effects transition amplitudes extracted from the frequency responses in devices with various gate lengths at $V_g = 0.4$ V (Figure 3.19) and $V_d = 1.2$ V (Figure 3.20). The amplitude of the self-heating related conductance transition, $\Delta g_{d\text{-}SH}$ was taken as g_d (30 MHz) - g_d (100 kHz). The substrate-related conductance transition amplitude, $\Delta g_{d\text{-}SUB}$ was extracted as g_d (4 GHz) - g_d (30 MHz). Reduction of the channel length results in an increase of both substrate-related and self-heating-related transition amplitudes. The substrate-related transition increases due to enhanced source-to-drain coupling with source and drain proximity. Some increase of the current density and dissipated power in shorter devices leads to a larger self-heating-related transition. As shown by Figure 3.19 and Figure 3.20, the output conductance frequency response is more affected by the substrate coupling than by self-heating for all devices and under different bias conditions as will be discussed in the following sections. In the moderate inversion regime both self-heating and substrate-related transition amplitudes increase with decreasing gate length

(Figure 3.19). However, in the strong inversion regime the amplitude of the substrate-related transition continues to increase with decreasing gate length, whereas the amplitude of the self-heating related transition tends to saturate (Figure 3.20). It is probably due to deeply downscaled devices having a drain current dependency on the gate length which is strongly attenuated compared with the expected $1/L_g$ behaviour. This deviation from the $1/L_g$ dependence is caused by series resistance and gate voltage dependent mobility effects, which are pronounced at higher gate voltages. As a result, the power $(P = I_d V_d)$ dissipated by 100 nm and 30 nm gate length devices does not significantly differ, especially in strong inversion. Hence the $\Delta g_{d\text{-}SH}$ variation with the gate length saturates for short devices. Also, in devices with a shorter gate length, the contribution of the heat evacuation through the source and drain extensions is greater than in longer devices.

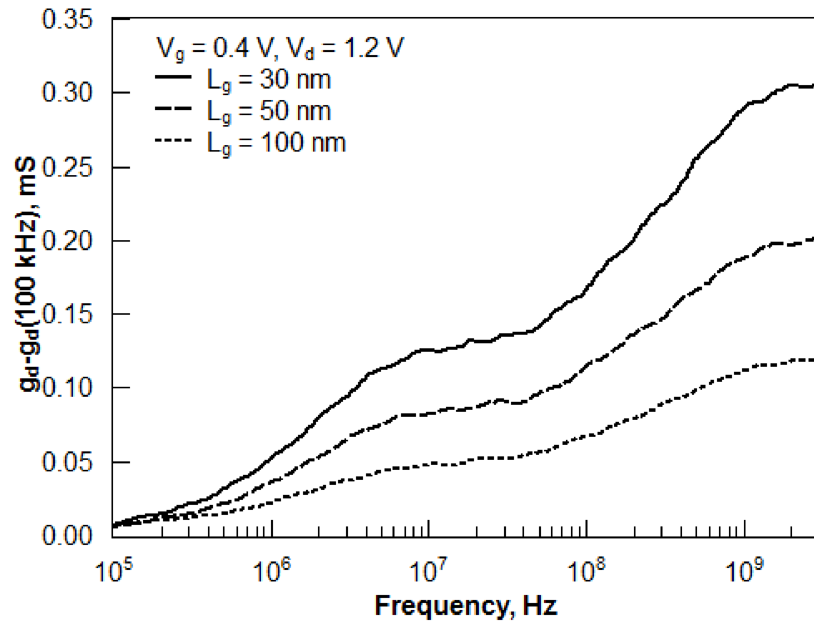

Figure 3.17. The output conductance variation with frequency in the devices with gate lengths ranging from 30 nm to 100 nm, W_g = 250 nm and N_{fin} = 80 at V_g = 0.4 V and V_d = 1.2 V.

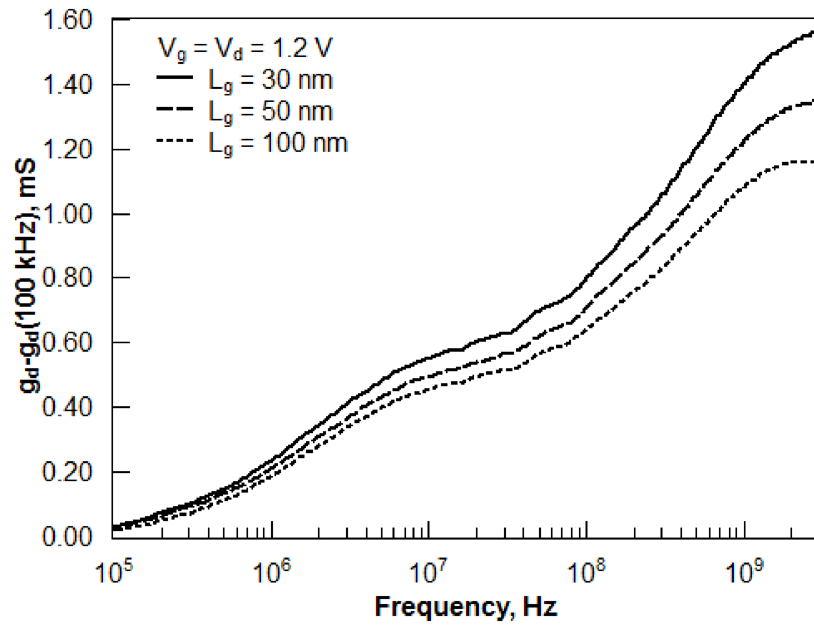

Figure 3.18. The output conductance variation with frequency in the devices with gate lengths ranging from 30 nm to 100 nm, W_g = 250 nm and N_{fin} = 80 at $V_g = V_d$ = 1.2 V.

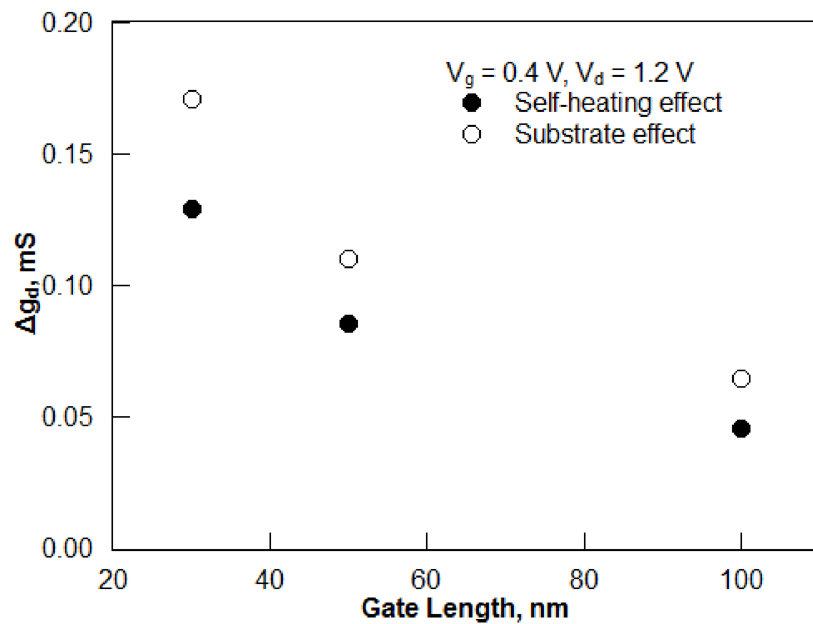

Figure 3.19. Amplitudes of the output conductance transitions in the devices with gate length from 30 nm to 100 nm, W_g = 250 nm and N_{fin} = 80 at V_g = 0.4 V and V_d = 1.2 V.

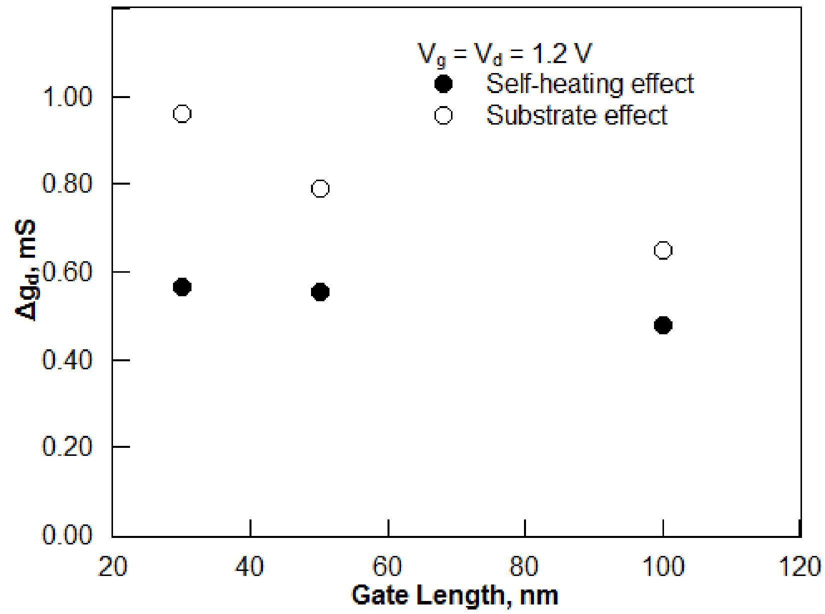

Figure 3.20. Amplitudes of the output conductance transitions in the devices with gate length from 30 nm to 100 nm, W_g = 250 nm and N_{fin} = 80 at $V_g = V_d$ = 1.2 V.

3.3.4 Output conductance variation due to self-heating

Figure 3.21 shows the variation of the self-heating related transition amplitude as a function of the gate voltage. Figure 3.22 shows the same transition amplitude in the case of different drain voltages. In both cases devices with 30, 50 and 100 nm gate lengths were analysed. The transition amplitude dependence on the gate voltage (Figure 3.21) appears to be stronger than on the drain voltage (Figure 3.22). This is because at low gate voltages (in moderate inversion, at about threshold), current flow through the device and in turn dissipated power is low and hence self-heating is not expected to be strongly pronounced. With an increase in the operating power, the temperature in the device rises and results in stronger output conductance degradation, as seen from Figure 3.21 and Figure 3.22. However, the $\Delta g_{d\text{-}SH}$ curves level and approach saturation at higher gate and drain voltages.

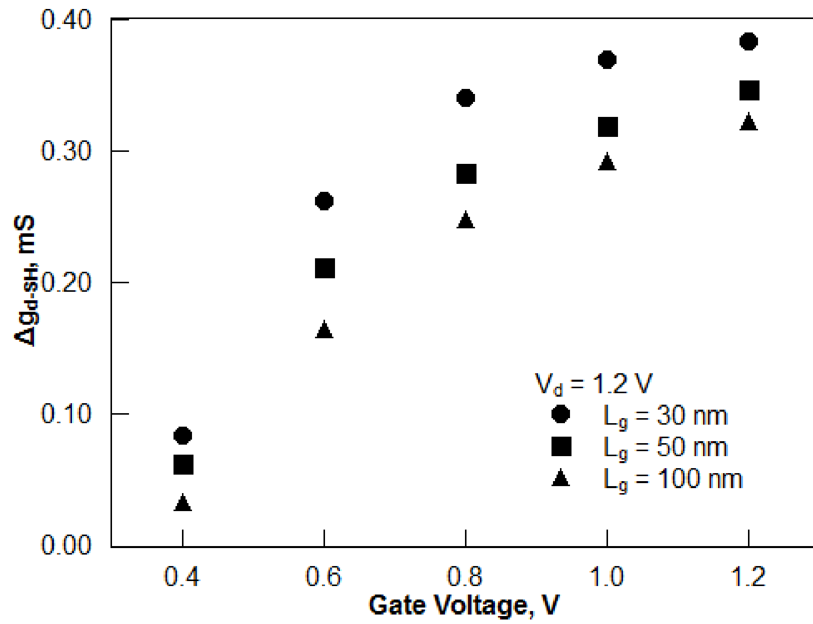

Figure 3.21. Variation of the amplitude of transitions due to self-heating with varying gate voltage in the devices with gate lengths 30 nm, 50 nm and 100 nm, W_g = 250 nm and N_{fin} = 80 at V_d = 1.2 V.

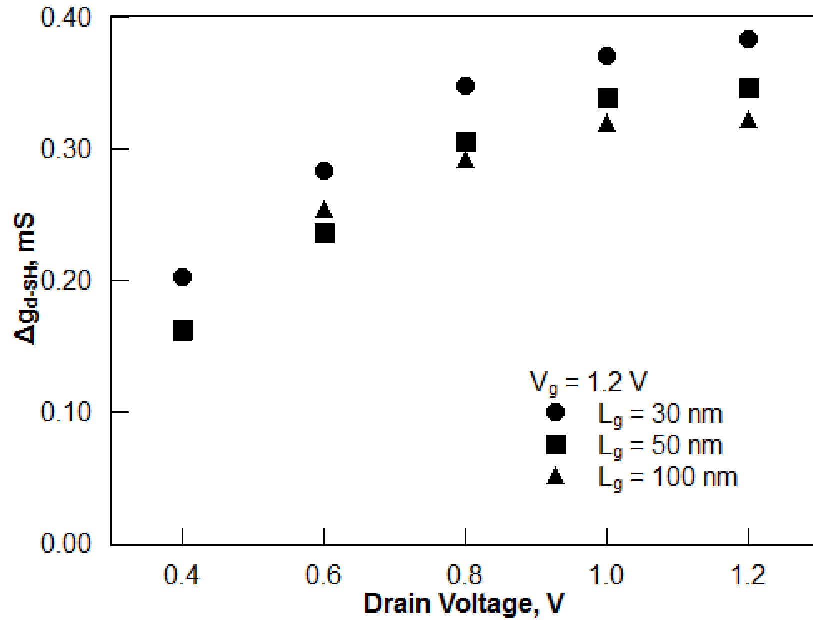

Figure 3.22. Variation of the amplitude of transitions due to self-heating with varying drain voltage in the devices with gate lengths 30 nm, 50 nm and 100 nm, W_g = 250 nm and N_{fin} = 80 at V_g = 1.2 V.

3.3.5 Output conductance variation due to the substrate effect

Figure 3.23 demonstrates the variation of substrate-related transition amplitudes with applied gate voltage at V_d = 1.2 V in UTBB devices with 30, 50 and 100 nm gate lengths. Figure 3.24 and Figure 3.25 show the variation of substrate-related transition amplitudes with the drain voltage at about threshold (Figure 3.24) and in strong inversion (Figure 3.25) in devices with 30, 50 and 100 nm gate lengths. Firstly, at all chosen bias conditions $\Delta g_{d\text{-}SUB}$ increases with reducing gate length, which seems to be intuitive due to the source and drain proximity. Secondly, an increase of the gate voltage (Figure 3.23) from moderate inversion at around threshold to strong inversion results in a very strong (6 to 10 times, depending on the gate length) enhancement of $\Delta g_{d\text{-}SUB}$. Thirdly, at small gate voltage (at about threshold) the drain current increase in saturation from 0.6 V to 1.2 V gives ~10% increase of $\Delta g_{d\text{-}SUB}$, while at high gate voltage in strong inversion the drain voltage variation does not affect $\Delta g_{d\text{-}SUB}$.

These results agree with simulations carried out in previous works for planar FDSOI MOSFETs. The increase of substrate-related transitions with increases of V_g, V_d [105] and gate length reduction [44], [104] was reported previously based on experiments and 2D Atlas simulations for FDSOI MOSFETs with thicker Si film and thicker BOX. In those devices the BOX-substrate interface is normally depleted and the application of high V_d and V_g results in a progressive two-dimensional inversion of this interface [105] (see e.g. the insets in Figure 3.27). Gate length scaling helps inversion extension from drain to source. Simple modification of space-charge conditions at the BOX-substrate interface was proposed as one of the main explanations for V_g, V_d and gate length effects [44], [104], [105]. The situation is rather different in UTBB SOI MOSFETs in which the application of relatively small gate voltage is sufficient to put the BOX-substrate interface in inversion (see e.g. Figure 3.27) due to the ultra-thin BOX. This is possible even at extremely low drain voltage, and hence the application of higher gate and drain voltages is not expected to modify further space-charge conditions at that interface. Hence, from the first interpretation one might not expect to observe the dependencies shown in Figure 3.23, Figure 3.24 and Figure 3.25.

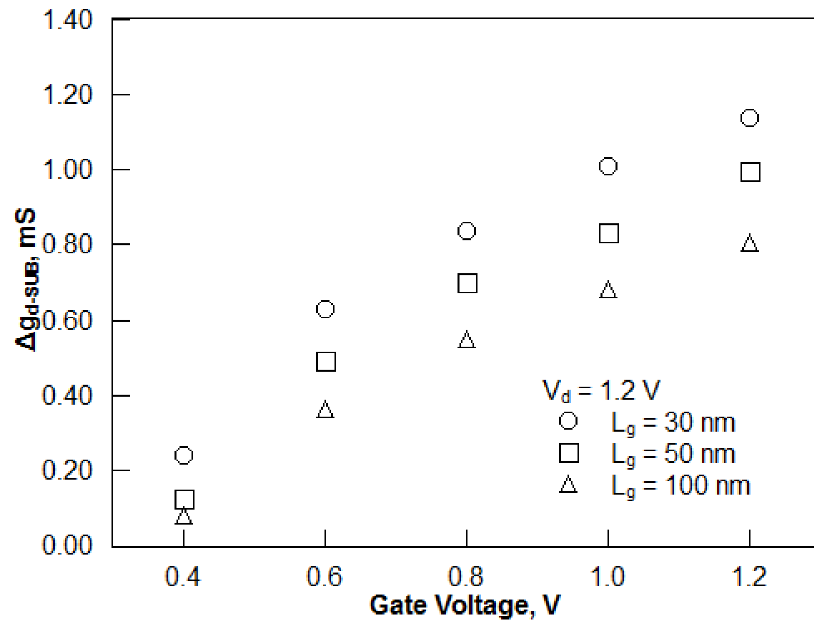

Figure 3.23. Variation of the amplitude of the transitions due to majority carriers in the substrate with varying gate voltage at V_d = 1.2 V in devices with 30, 50 and 100 nm gate lengths, W_g = 250 nm and N_{fin} = 80.

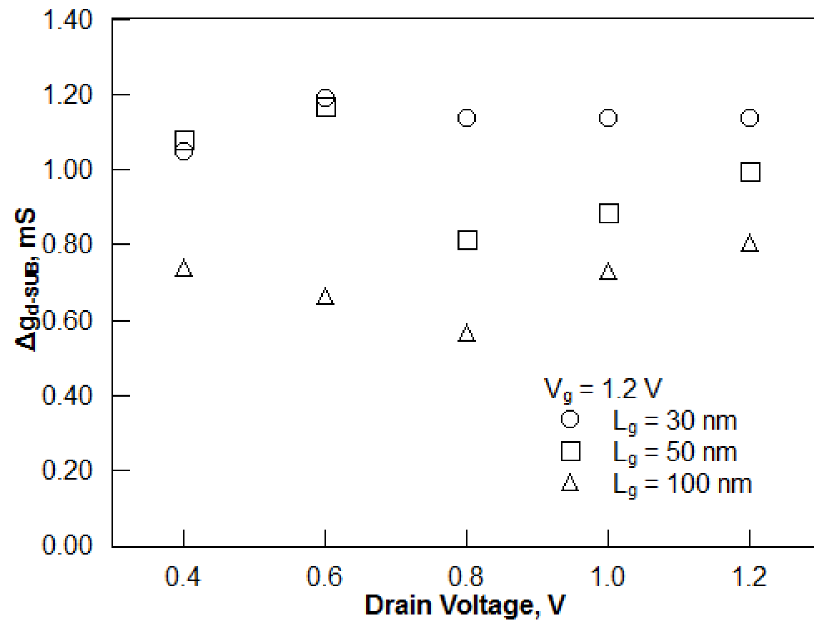

Figure 3.24. Variation of the amplitude of the transitions due to majority carriers in the substrate with varying drain voltage at V_g = 1.2 V in devices with 30, 50 and 100 nm gate lengths, W_g = 250 nm and N_{fin} = 80.

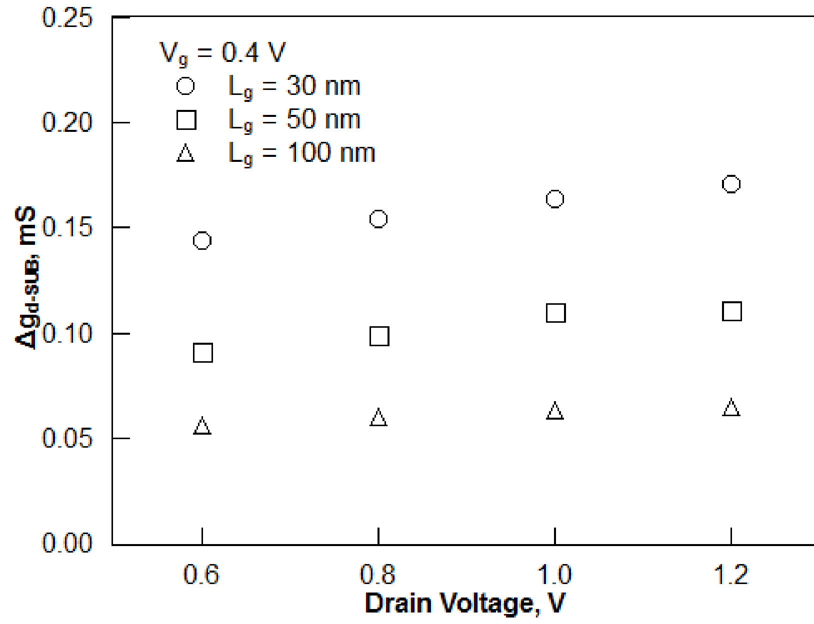

Figure 3.25. Variation of the amplitude of the transitions due to majority carriers in the substrate with varying drain voltage at V_g = 0.4 V in devices with 30, 50 and 100 nm gate lengths, W_g = 250 nm and N_{fin} = 80.

In order to understand and explain V_g, V_d and gate length dependencies featured by substrate-related output conductance transition amplitudes in the studied devices, basic equations relating $\Delta g_{d\text{-}SUB}$ with MOSFETs equivalent circuit elements are presented as obtained in [103]:

$$\Delta g_{d-SUB} = (n-1) \cdot g_m \cdot \frac{v_{BGS}}{v_{DS}} \tag{3.4}$$

$$v_{BGS} = \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{Sub}} v_{DS} \tag{3.5}$$

where g_m is the transconductance, n is the body factor, v_{BGS} is the variation of the back-gate-to-source voltage (i.e. the potential at the substrate-BOX interface), v_{DS} is the small-signal drain source voltage, C_{BGD}, C_{SBG}, C_{GBG} and C_{Sub} are the elements of the equivalent circuit describing the substrate effects. Other equivalent circuit elements are described in [105].

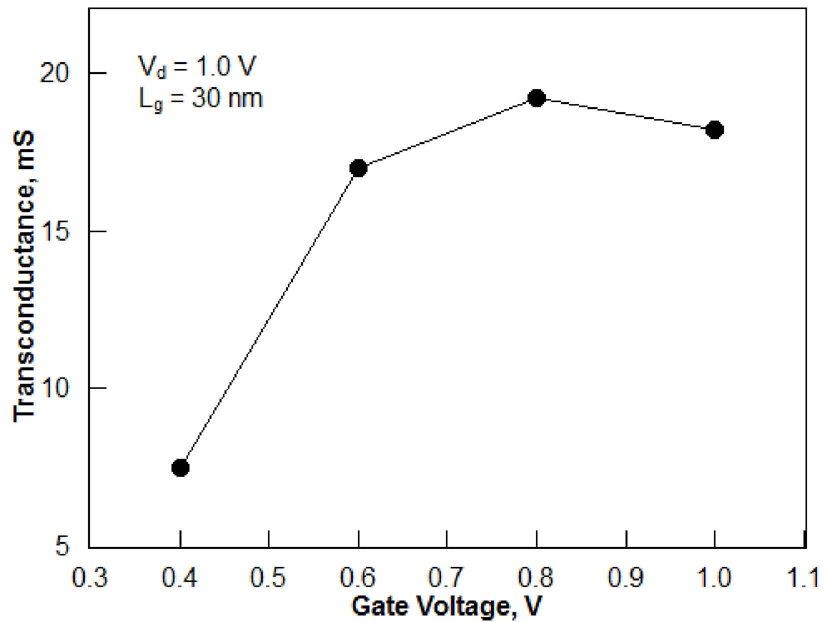

Figure 3.26. Variation of the transconductance in UTBB devices with 30 nm gate length, W_g = 250 nm and N_{fin} = 80 at V_d = 1.0 V.

According to Equation 3.4 and Equation 3.5, gate length, V_g and V_d dependencies can be explained by the corresponding dependencies of the transconductance, which appears as a multiplication factor in Equation 3.4. The transconductance increases strongly with V_g as well as with the gate length, while the dependency on V_d is weak when V_d is in the saturation regime. The transconductance dependence on V_g is shown in Figure 3.26 for 30 nm gate length UTBB devices at V_d = 1.0 V. Furthermore, the C_{Sub} variation should be taken into account, even if the substrate-BOX interface is in inversion at any bias conditions and lengths. Figure 3.27 presents 2D Atlas simulated electron concentrations in the Si substrate underneath BOX along the channel (horizontal cut at the substrate-BOX interface) (Figure 3.27a) and substrate depth (vertical cut in the middle of the channel) (Figure 3.27b) for UTBB MOSFETs with gate lengths of 30, 50 and 100 nm. The simulated structure corresponds to the experimental devices. To give a “reference point” the insets show similar dependencies for the devices with thick BOX, keeping all the other parameters the same. Contrarily to the thick-BOX case, where the application of bias changes the space-charge conditions, for UTBB devices the substrate-BOX interface is inverted everywhere from source to drain for all bias conditions and lengths investigated. Nevertheless, the electron concentrations change noticeably (both x- and y-distribution) which translates in turn to a change of C_{Sub} in Equation 3.5. Moreover, this change is stronger with a variation of V_g than with a variation of V_d, agreeing with the experimental trends.

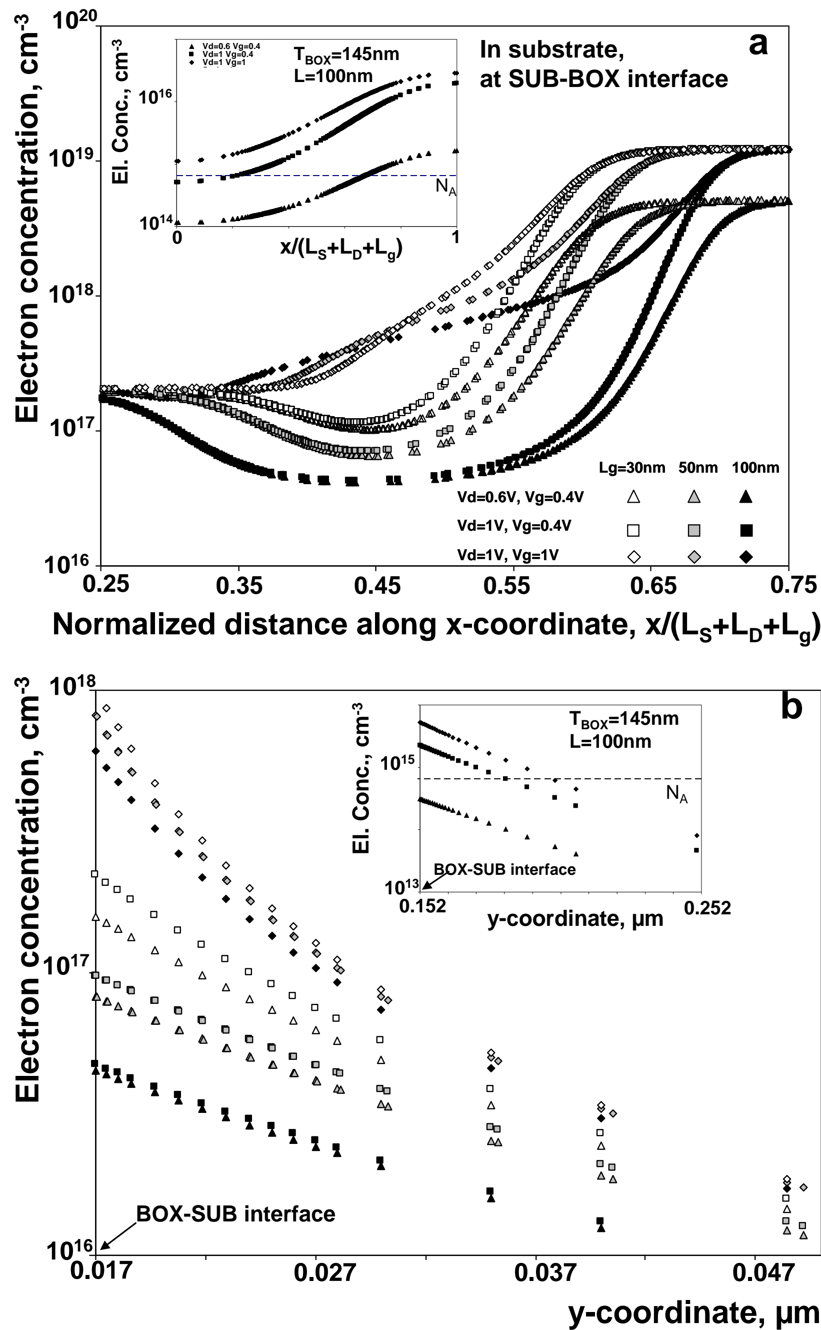

Figure 3.27. 2D Atlas simulations of the electron concentration in the Si substrate (a) at the BOX-substrate interface as a function of normalised distance along the channel length, i.e. horizontal cut and (b) at the point in the middle of the channel as a function of the depth in silicon substrate, i.e. vertical cut. Simulated at different gate and drain biases for UTBB devices with different gate lengths: 30 nm (empty symbols); 50 nm (grey symbols) and 100 nm (full symbols). The length of the source and drain regions is 100 nm; gate oxide thickness is 1.3 nm; Si body thickness is 7 nm; BOX thickness is 10 nm; substrate doping is 6.5×10^{14} cm^{-3} p-type; channel is undoped; (i.e. the same parameters as those in the experimental devices). The insets present the same dependencies for 100 nm gate length devices with BOX thickness of 145 nm; all other parameters are the same.

Incorporation of a ground plane is expected to suppress to some extent substrate-related effects. Characterisation of UTBB devices with a ground plane is presented in Chapter 4.

3.3.6 Discussion

Figure 3.28 compares amplitudes of self-heating and substrate-related output conductance transitions in UTBB devices with 30, 50 and 100 nm gate lengths. The substrate-related output conductance variation is stronger than the self-heating related variation in all devices when the gate voltages are from 0.4 V to 1.2 V, i.e. from moderate to strong inversion. The amplitude of the substrate-related transition can be up to ~50% higher than the amplitude of the self-heating-related transition. Both substrate and self-heating related transitions increase with gate length reduction. This aggravates the frequency-dependent behaviour of downscaled UTBB MOSFETs. Further, while the output conductance degradation is smaller for longer devices, its relative importance compared with the static (or DC) value might be stronger than in shorter devices. This is due to DC output conductance being lower in longer devices. The high frequency output conductance can reach 300% and more of its DC values. This again highlights the need of special care when using only DC assessment for performance predictions (even relative).

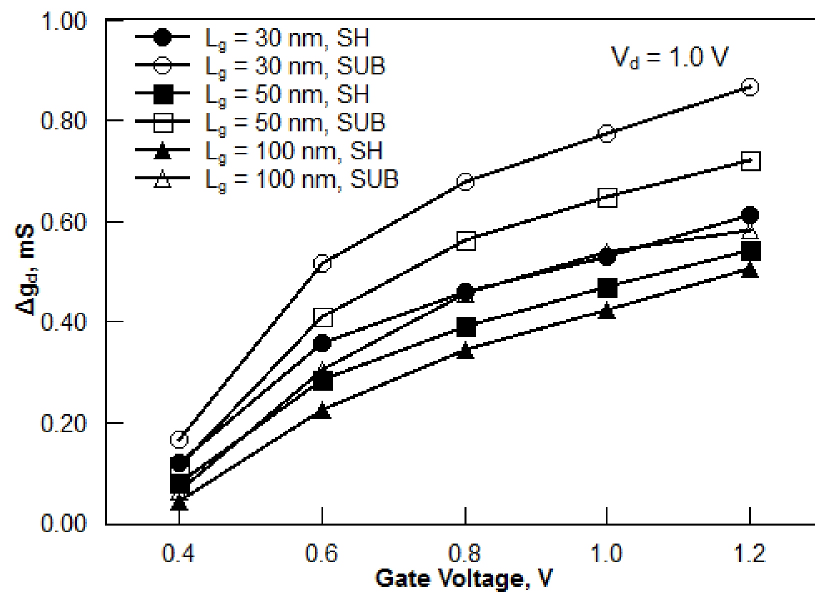

Figure 3.28. Variation of the transition amplitudes due to self-heating and substrate effects with the gate voltage in devices with 30, 50 and 100 nm gate lengths, W_g = 250 nm and N_{fin} = 80 at V_d = 1.0 V.

Figure 3.29 shows the variation of $\Delta g_{d\text{-}SUB}$ and $\Delta g_{d\text{-}SH}$ with the dissipated power in devices with a gate length of 30 nm. The dissipated power is calculated as a product of the drain current and the drain voltage. In the whole range of the dissipated power, amplitudes of the substrate transitions are higher (up to ~56% in the high power region) than the amplitudes of the self-heating related transitions for the same power levels. Moreover, the self-heating related output conductance degradation tends to saturate with the power increase, while the substrate-related degradation continues to increase, thus making their difference larger at higher power.

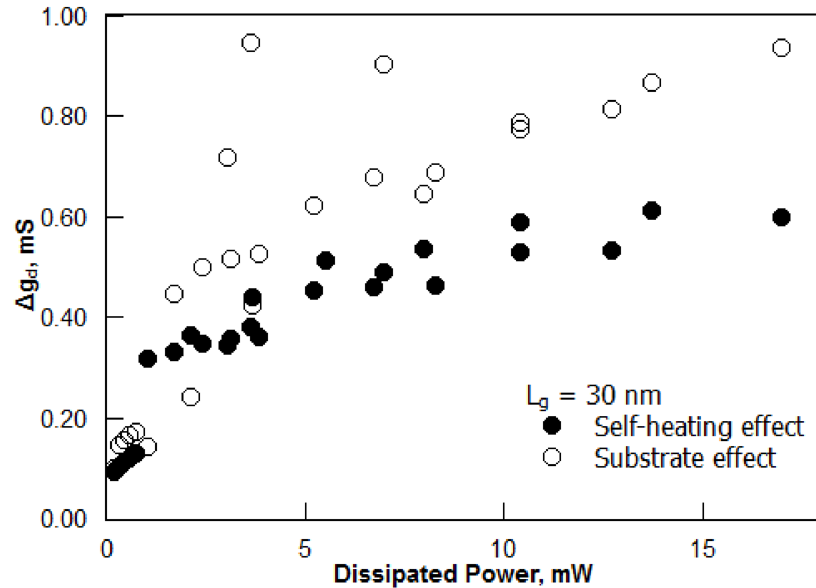

Figure 3.29. Output conductance transition amplitudes due to self-heating and substrate effects as a function of dissipated power in the devices with gate length of 30 nm, W_g = 250 nm and N_{fin} = 80.

The results suggest that in order to improve performance of a UTBB MOSFET over the wide frequency range, both self-heating and the substrate effects should be addressed. This is especially relevant for shorter devices as both self-heating and substrate effects are amplified as devices scale down. The main effort should be placed on the suppression of the substrate-related effects as their corresponding output conductance transitions are larger than the self-heating-related ones. Suppression of these effects is expected to improve device analogue performance, e.g. reduce the intrinsic gain variation with frequency.

3.4 Summary

Analogue figures of merit in the UTBB devices show a good potential of UTBB technology for future analogue applications, especially for low-power applications as the intrinsic gain reaches its maximum in the moderate inversion regime. It was shown that the narrow-channel UTBB MOSFETs outperform other planar FDSOI devices and FinFETs in terms of the transconductance maximum, drive current and intrinsic voltage gain.

The small-signal output conductance of advanced UTBB SOI MOSFETs has been studied in the frequency range from 40 kHz to 4 GHz. The output conductance of UTBB devices without a ground plane has been shown to be strongly affected by both self-heating and substrate effects, which manifest changes in the characteristics at about a few MHz and 100 MHz, respectively. Both substrate- and self-heating-related output conductance transition amplitudes increase with decreasing gate length and increasing applied biases.

Although a 10 nm ultra-thin BOX was used in the studied devices, facilitating heat evacuation from the channel to the Si substrate underneath BOX, degradation of the output conductance caused by self-heating is considerable.

It has also been observed that use of a 10 nm BOX enhances coupling through the substrate and as a result, magnifies the substrate-related output conductance transition. Despite the fact that the substrate-BOX interface in UTBB SOI MOSFETs was shown to be in inversion under all bias regimes and gate lengths used in this work, the substrate-related transition amplitudes increase with increasing gate voltage and decreasing gate length. The most probable reasons have been discussed, and correspond to the increase of the transconductance and inversion charge densities at the BOX-substrate interface (which translates to a variation of the substrate capacitance) and hence increase of $\Delta g_{d\text{-}SUB}$ according to Equation 3.4.

The variation of the output conductance of the UTBB SOI MOSFETs caused by the coupling through the substrate has been demonstrated to be stronger than the output conductance variation due to self-heating in all operating regimes. At high gate voltages the difference increases as the gate length is scaled down. Therefore, it is imperative to minimise the coupling through the substrate, e.g. by adjusting the substrate doping. UTBB devices with substrate doping are discussed in Chapter 4.

Chapter 4. Improved UTBB devices using a ground plane

4.1 Motivation and chapter outline

In the previous chapter it was shown that substrate effects significantly degrade the output conductance of UTBB MOSFETs over the wide frequency range. In this chapter devices with heavily doped Si substrate under the BOX are analysed. Heavy doping under the BOX (ground plane, GP) is expected to alter wide-frequency performance of UTBB devices. In this work a GP is not biased. Therefore, a GP impacts substrate coupling only due to the presence of dopants under the buried oxide.

This chapter is organised as follows. Firstly, the experimental details of UTBB SOI nMOSFET devices and methodology are presented. Secondly, results of numerical simulations of devices incorporating a GP are compared with devices without a GP. Thirdly, devices are experimentally characterised over a wide frequency range in order to evaluate the effectiveness of the GP. Devices without a GP are used for comparison. The improvement offered by introduction of a highly doped GP in UTBB technology is presented. The trade-offs with device architecture are discussed and the dominating factors affecting performance for each frequency range are identified.

4.2 Experimental and simulation details

UTBB devices with BOX thickness 10 nm and gate length 100 nm were simulated using the Atlas 2D simulator. In order to take into account parallel and perpendicular electric fields, Lombardi's carrier mobility model was used [144]. The band gap narrowing (caused by heavy doping) and Schockley-Read-Hall process (trap-assisted generation and recombination) were considered for the carrier statistics and recombination model, respectively. The concentration of p-type impurities in the initial uniformly doped substrate was ~6.5×10^{14} cm^{-3}. Ground planes were implemented using high p- and n-type doping (on the level of ~10^{18} cm^{-3}) in the substrate under the BOX.

For experimental characterisation, UTBB devices were fabricated on SOI wafers with a BOX thickness of 10 nm and a Si substrate having a standard resistivity of 20 Ω·cm. The gate stack was formed using HfSiON dielectric with EOT of 1.3 nm and a TiN electrode. Three different wafers were used for this study: wafers with a p- or n-type GP, and without any GP. The p-type GP was implemented by doping the Si substrate under the BOX with In resulting in the doping

concentration up to 10^{18} cm^{-3}. Heavy doping with As was used to produce an n-type GP. Devices were also fabricated without a GP in which the Si substrate did not receive any additional doping. The Si body thickness in the channel region was 8 nm for the devices incorporating a GP and 7 nm in the devices without a GP. In all cases the channel was left undoped. Raised source and drains were used, which were 18 nm for devices with a GP and 15 nm for devices without a GP. Multi-finger devices embedded in RF pads having gate lengths (L_g) of 100 nm, finger widths of 250 nm and 80 parallel fingers were characterised.

Wideband frequency characterisation was performed using a Rohde & Schwarz vector network analyser. S-parameters were measured at frequencies from 40 kHz to 4 GHz, de-embedded and converted to Y-parameters using Equations 2.5-2.8 as shown in Section 2.4.2.1. Output conductance values were obtained from the real part of Y_{dd} at various frequencies. The total drain capacitance C_{dd} was obtained from the imaginary part of the Y_{dd} parameter according to:

$$C_{dd} = Im\,(Y_{dd})/2\pi f, \tag{4.1}$$

where f is the frequency.

4.3 Results and discussion

4.3.1 Simulations of electron concentration in substrate

Due to the ultra-thin body and BOX, the space-charge conditions at the BOX-substrate interface are controlled by the gate and drain voltages. This is confirmed by the simulation results. Figure 4.1 presents the electron concentration in the substrate just below the BOX along the device, i.e. from the source to the drain. Devices without a GP at V_g = 1.0, V_d = 0 V as well as V_g = -0.1 V, V_{th}, 1.0 V and V_d = 1.0 V are shown. It is clear that an increase in the gate and drain voltages increases the electron concentration as expected. Above threshold (in the typical operating regime of the devices) the BOX-substrate interface is in inversion even at small V_d. Even when the device is off and a positive V_d is applied (e.g. V_g = -0.1 V, V_d = 1.0 V) a part of the substrate under the drain remains inverted.

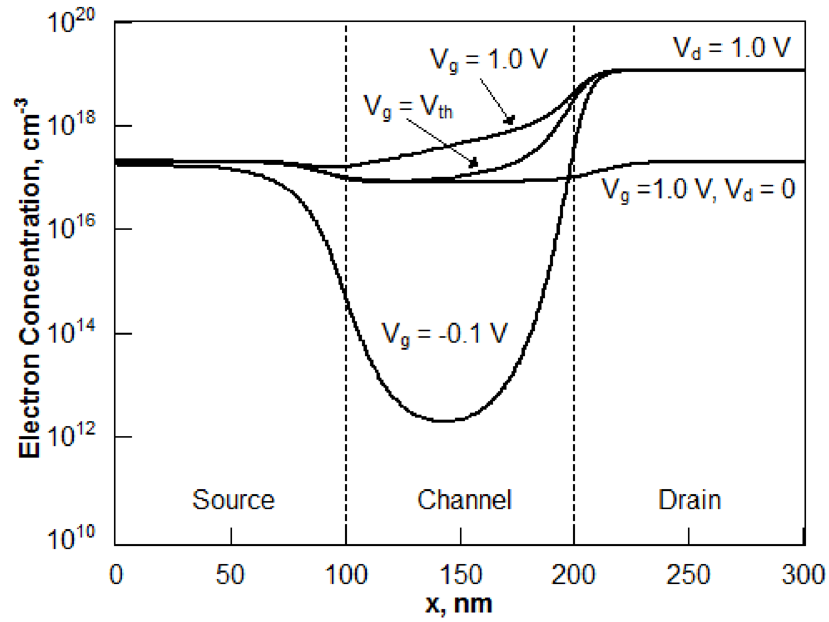

Figure 4.1. Simulated variation of the electron concentration just below the BOX along the device from the source to the drain in a 100 nm gate length device without a GP at V_g = 1.0, V_d = 0 V as well as V_g = -0.1 V, V_{th}, 1.0 V and V_d = 1.0 V.

As the substrate effects are expected to be strongly pronounced when the device operates in saturation, the electron concentration at the BOX-substrate interface in devices with p-type GP, n-type GP and no GP was simulated at $V_g = V_d$ = 1.0 V. The resulting variations in electron concentration are shown in Figure 4.2. For comparison, the same simulations were carried out at $V_g = V_{th}$ and V_d = 1.0 V (shown in Figure 4.3), which is of interest for low power applications.

At high V_g (Figure 4.2) and even at threshold (Figure 4.3) the space-charge conditions in the substrate under the BOX are very similar in devices without a GP and in devices with an n-type GP. Both cases feature inversion conditions at the BOX-substrate interface along the device from the source to the drain. Source and drain coupling is determined by the potential at the BOX-substrate interface. Therefore, under typical operating conditions devices with an n-type GP are expected to demonstrate similar coupling to devices without a GP. However, devices with a p-type GP are expected to behave differently. Consequently, devices with an n-type GP used in this work serve only as a control and the main focus is on understanding the performance of devices with a p-type GP and without a GP. For conciseness, devices with a p-type GP are hereafter referred to as devices with a GP, unless otherwise stated.

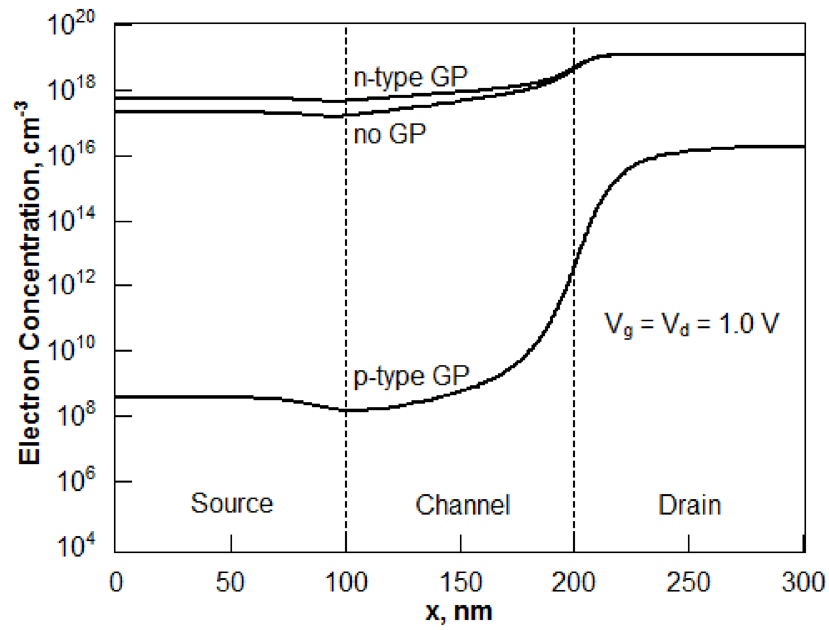

Figure 4.2. Simulated variation of the electron concentration in the substrate just below the BOX along the device from the source to the drain in 100 nm gate length devices with a p-type GP, n-type GP and no GP at $V_g = V_d = 1.0$ V.

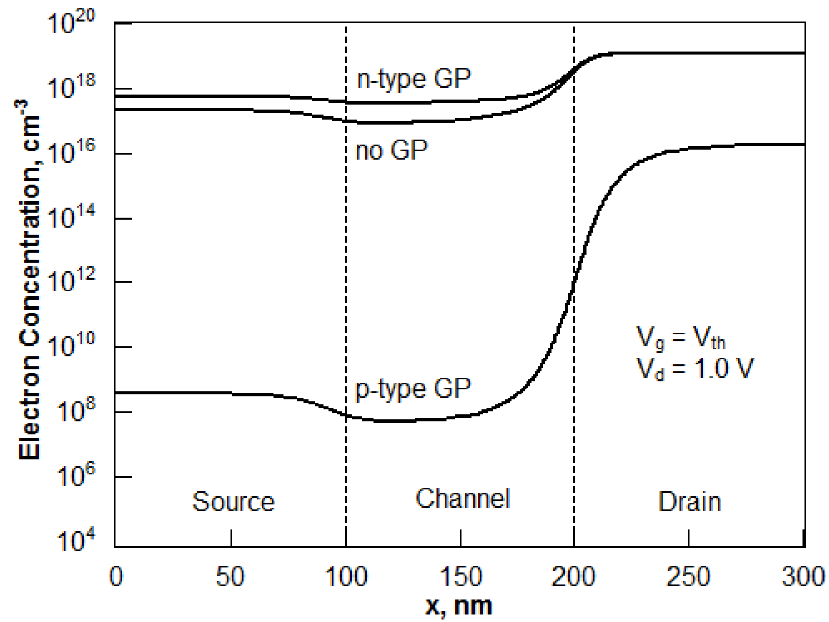

Figure 4.3. Simulated variation of the electron concentration in the substrate just below the BOX along the device from the source to the drain in 100 nm gate length devices with a p-type GP, n-type GP and no GP at $V_g = V_{th}$ and $V_d = 1.0$ V.

4.3.2 Current-voltage characteristics

In order to evaluate the effect of a GP in UTBB devices experimentally, devices with 100 nm gate length were selected for characterisation. 100 nm gate length devices showed the best uniformity among available 30 nm, 50 nm and 100 nm gate length devices, as it was shown in Section 3.3.1 for UTBB devices without a GP. Figure 4.4 shows transfer characteristics of a number of UTBB devices with a GP at V_d = 1.0 V. Non-working devices and outliers are not shown.

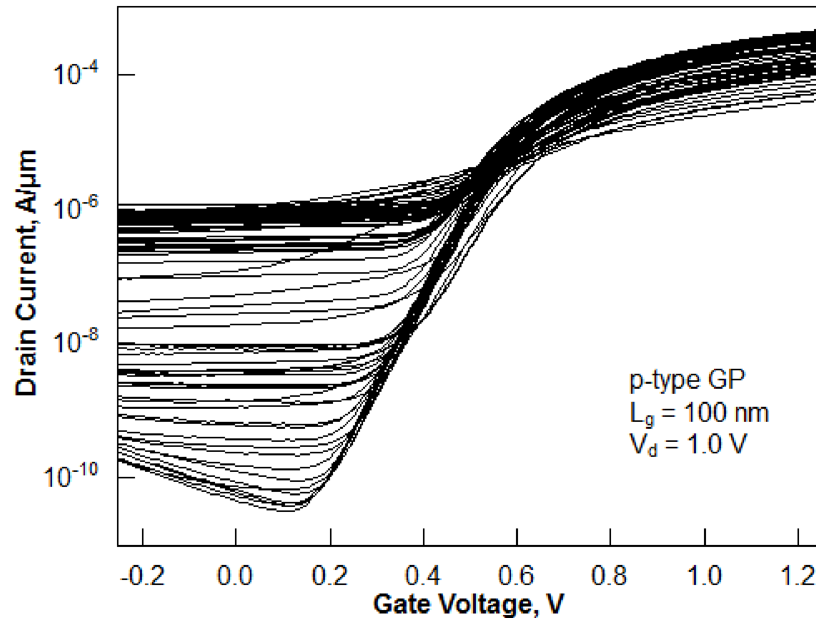

Figure 4.4. Transfer characteristics of 100 nm gate length UTBB devices with a GP at V_d = 1.0 V.

Comparison of the off-state drain current (V_g = 0 V, V_d = 1.0 V) with the on-state drain current (V_g = 0.9 V, V_d = 1.0 V) in 100 nm gate length UTBB devices with a GP is shown in Figure 4.5. It is expected that a higher on-current leads to a higher off-current as it was observed in Section 3.3.1. However, this trend is not observed in Figure 4.5. Many devices showed the off-state current close to 1 $\mu A \cdot \mu m^{-1}$, while the on-state drain current was spread between 20 $\mu A \cdot \mu m^{-1}$ and 180 $\mu A \cdot \mu m^{-1}$. Similarly to the UTBB devices without a GP (Section 3.3.1), GP devices located further from the wafer centre showed lower off-state drain current. This distribution is most probably related to the fabrication process.

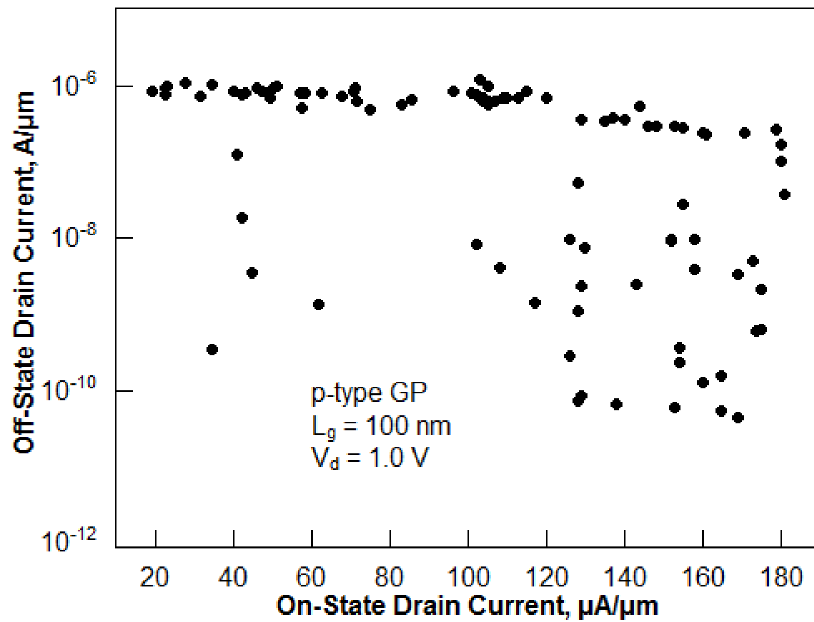

Figure 4.5. The off-state drain current ($V_g = 0$ V, $V_d = 1.0$ V) comparison with the on-state drain current ($V_g = 0.9$ V, $V_d = 1.0$ V) in 100 nm gate length UTBB devices with a GP.

In devices with a GP the threshold voltage V_{th} was found to be 0.5 V. As mentioned in Chapter 3, the threshold voltage in UTBB devices without a GP is 0.4 V (same in n-type GP devices).

For further characterisation of substrate effects, devices with the low off-state drain current where selected. Figure 4.6 shows typical transfer characteristics of 100 nm gate length nMOSFETs with and without a GP selected for study. The output characteristics of the devices with a GP at gate overdrives from 0.1 V to 0.9 V are shown in Figure 4.7. In the devices with a GP, the on-current is 130 $\mu A \cdot \mu m^{-1}$ at a gate overdrive V_g-V_{th} = 0.4 V and drain voltage V_d = 1.0 V. DIBL is 32 $mV \cdot V^{-1}$. Comparable figures were previously reported for UTBB devices which did not incorporate a GP [33]. These characteristics confirm that UTBB technology allows good control of short channel effects and inclusion of a GP does not compromise overall device performance. Figure 4.6 also shows that the DC characteristics of the two types of device are similar, especially above threshold where further analysis is performed. This allows a fair comparison of the devices.

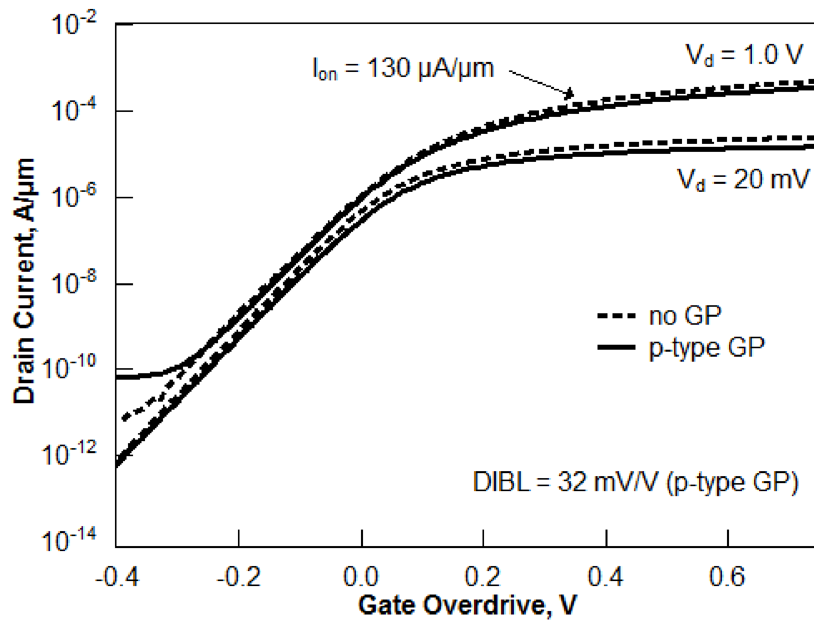

Figure 4.6. Transfer characteristics of the selected 100 nm gate length devices with a GP and without at $V_d = 20$ mV and $V_d = 1.0$ V.

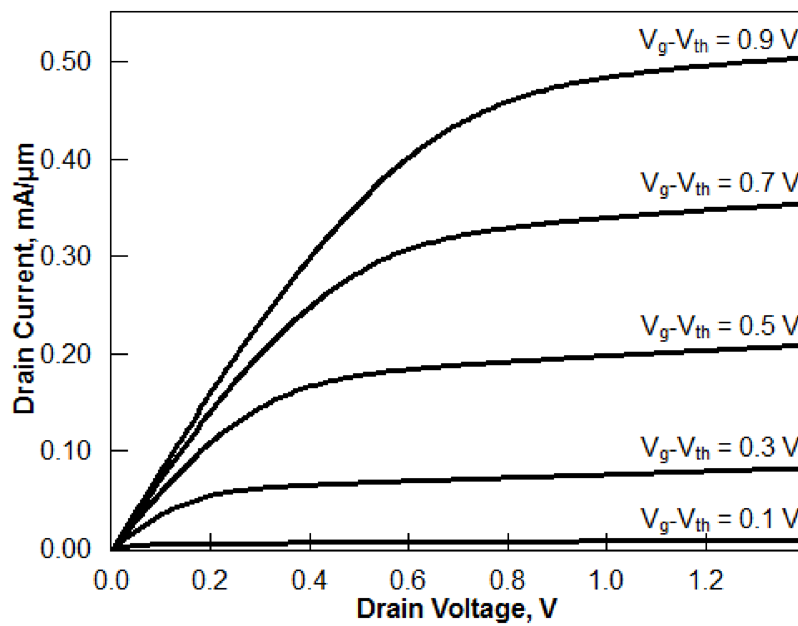

Figure 4.7. Output characteristics of the selected 100 nm gate length devices with a GP at gate overdrives from 0.1 V to 0.9 V.

4.3.3 Substrate effects

In order to characterise substrate effects, the output conductance was measured over the frequency range from 100 kHz to 4 GHz. Figure 4.8 shows the variation in g_d with frequency

with respect to its value at 100 kHz for the devices with a GP and without any GP. Since the presence of the GP alters the device threshold voltage, devices are compared at the same gate overdrive V_g-V_{th}, thus ensuring a fair performance comparison. Figure 4.8 shows that the output conductance increase with frequency appears in both types of UTBB device (with and without a GP). As shown in Section 3.3.3, the plateau in conductance at ~30 MHz for both devices indicates the removal of dynamic self-heating. At this frequency the lattice temperature does not follow the voltage oscillations any longer [84]. The further increase of the output conductance observed after this self-heating plateau is one of the substrate-related output conductance transitions. It is an indication of source and drain coupling due to carriers in the substrate. Such an increase is particularly notable for the devices with no GP, demonstrating that the GP is effective at reducing source and drain coupling. At a few GHz, the output conductance curve levels off.

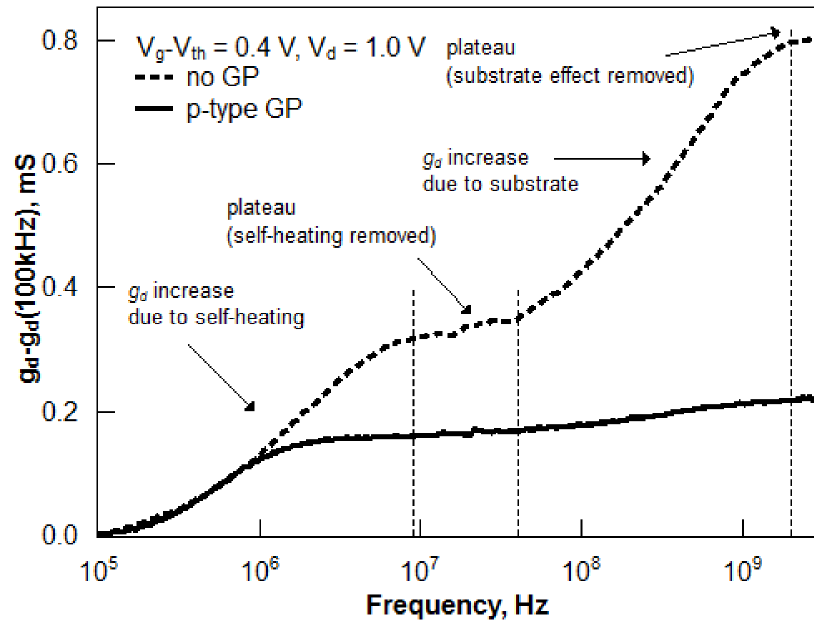

Figure 4.8. The output conductance variation with frequency with respect to its value at 100 kHz in the 100 nm gate length devices with a GP and without a GP at V_g-V_{th} = 0.4 V and V_d = 1.0 V.

The output conductance frequency dependence is usually used to evaluate the substrate effects [103], [104]. However, transitions due to the self-heating and substrate effects also manifest themselves in the frequency response of the total drain capacitance which changes over a few orders of magnitude [95], [96]. Figure 4.9 shows the total drain capacitance and output conductance variation with frequency in the devices without a GP. At ~30 MHz where the dynamic self-heating effect is removed one can observe an inflection in both output conductance and total drain capacitance characteristics. At frequencies ~4 GHz, carriers in the substrate do

not follow voltage oscillations and a plateau is reached in both curves. Characteristic frequencies of these two curves correlate due to the same physical mechanism. The total drain capacitance C_{dd} is a total capacitance as 'seen' from the drain:

$$C_{dd} = C_{dg} + C_{ds} + C_{db}, \tag{4.2}$$

where C_{dg}, C_{ds} and C_{db} are the capacitances between different MOSFET terminals. Therefore C_{dd} accounts for self-heating due to the C_{ds} term (at frequencies up to ~30 MHz) and substrate effects due to the terms C_{db} and C_{ds} (at frequencies between ~30 MHz and ~4 GHz). A variation of the potential at the BOX-substrate interface is caused by the variation of C_{ds} and C_{db} with frequency. This results in the dependence of the parasitic source and drain coupling on frequency. At high frequencies a part of the substrate under the BOX acts as a lossy dielectric effectively increasing the dielectric thickness and thus contributing to the capacitance reduction.

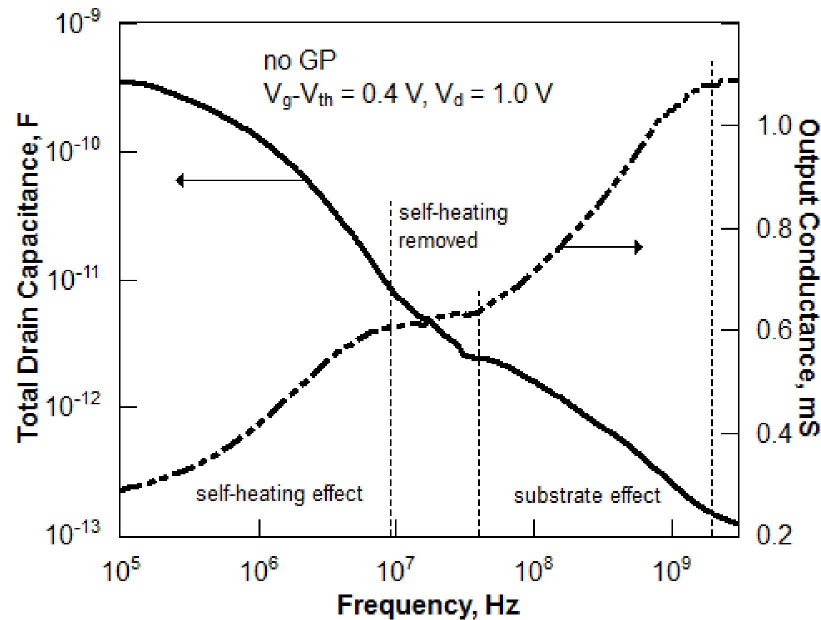

Figure 4.9. Frequency dependence of the total drain capacitance and output conductance in the 100 nm gate length devices without a GP at V_g-V_{th} = 0.4 V and V_d = 1.0 V.

Figure 4.10 shows the C_{dd} frequency dependence in devices with and without a GP. At high frequencies, above a few GHz, C_{dd} approaches ~10^{-13} F for both devices. This high frequency C_{dd} value is bias independent, as shown in Figure 4.11 where the C_{dd} variation with frequency is presented at different gate overdrive voltages for the device with a GP. This value is related to the intrinsic capacitance of the device and includes gate capacitance (~50 fF), BOX capacitance (~7 fF) and other capacitances such as substrate capacitance when the Si substrate behaves as lossy dielectric at high frequencies.

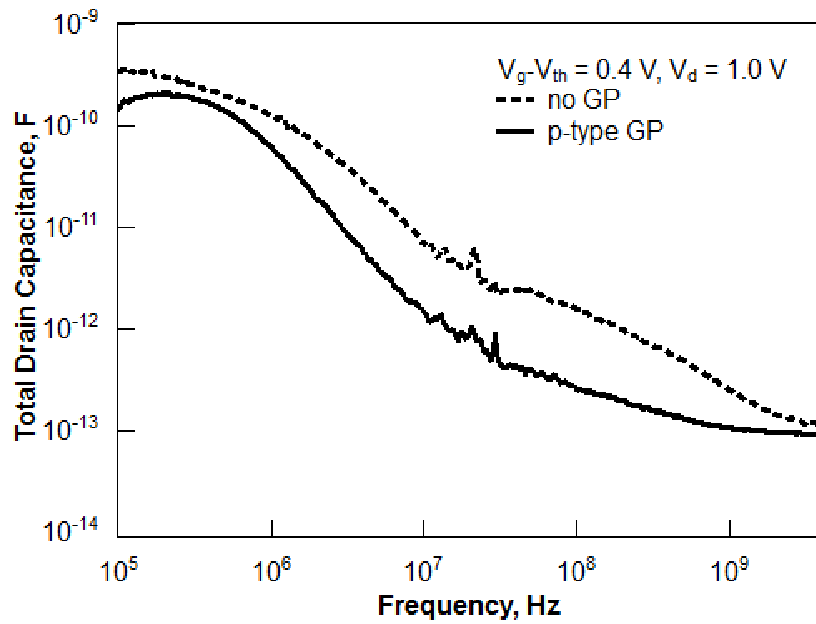

Figure 4.10. Variation of the total drain capacitance with frequency in the 100 nm gate length devices with a GP and without at V_g-V_{th} = 0.4 V and V_d = 1.0 V.

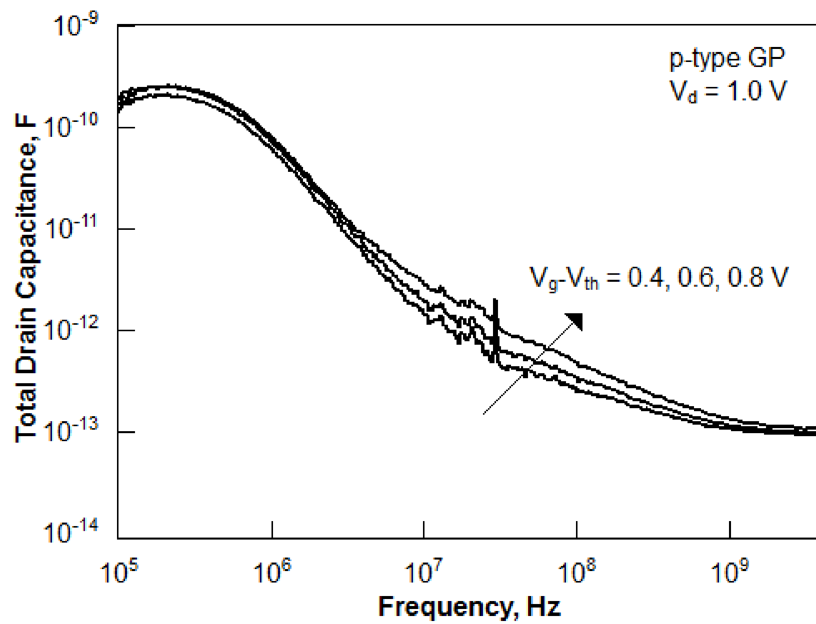

Figure 4.11. Total drain capacitance as function of frequency in the 100 nm gate length devices with a GP at different gate overdrive V_g-V_{th} and V_d = 1.0 V.

In order to evaluate the substrate effects in different regimes of operation, and understand how the GP reduces associated output conductance variation, the degradation due to the substrate has been analysed as $\Delta g_{d\text{-}SUB} = g_d$(~4 GHz)-$g_d$(30 MHz). The change in the output conductance is studied at different bias conditions. The dependence of $\Delta g_{d\text{-}SUB}$ on the gate overdrive V_g-V_{th} in the

saturation regime is shown for the devices with no GP, with a p-type GP and with an n-type GP in Figure 4.13. Firstly, $\Delta g_{d\text{-}SUB}$ in the device with a p-type GP is significantly lower (up to 12 times) than $\Delta g_{d\text{-}SUB}$ in the devices with an n-type and without any GP. This improvement can be translated into enhanced device analogue performance over MHz-GHz frequency range. The substrate transition amplitudes in the devices with the n-type and without GP match well at all gate overdrive values, as expected.

Secondly, in all devices $\Delta g_{d\text{-}SUB}$ increases with the gate overdrive from low values close to zero at $V_g = V_{th}$. Such behaviour can be explained by the transconductance variation with $V_g\text{-}V_{th}$ (Figure 4.14) which results in strong $\Delta g_{d\text{-}SUB}$ dependence on $V_g\text{-}V_{th}$ according to:

$$\Delta g_{d-SUB} = (n-1) \cdot g_m \cdot \frac{C_{BGD}}{C_{BGD}+C_{SBG}+C_{GBG}+C_{Sub}}, \tag{4.3}$$

where g_m is the transconductance, n is the body factor, C_{BGD}, C_{SBG}, C_{GBG} and C_{Sub} are the elements of the equivalent circuit describing the substrate effects [105]. C_{BGD}, C_{SBG}, C_{GBG} are the drain-to-back-gate, source-to-back-gate capacitance and front-gate-to-back-gate capacitances, respectively. The back gate is equivalent to the interface between the substrate and BOX. The equivalent circuit is shown in Figure 4.12.

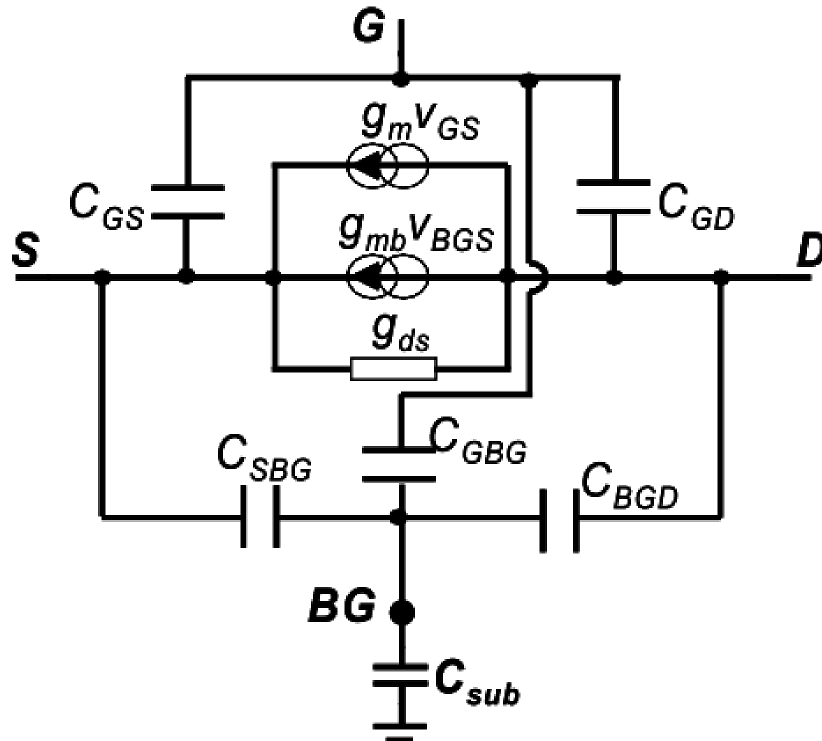

Figure 4.12. Small-signal equivalent circuit showing the substrate capacitance. Adapted from [105].

The effect of C_{Sub} variation with V_g-V_{th}, despite being relatively weak, may play a role in $\Delta g_{d\text{-}SUB}$ bias dependence. This is because the space-charge conditions at the substrate-BOX interface are fixed in strong inversion for the devices with an n-type GP and the devices without a GP and in accumulation in the devices with a p-type GP.

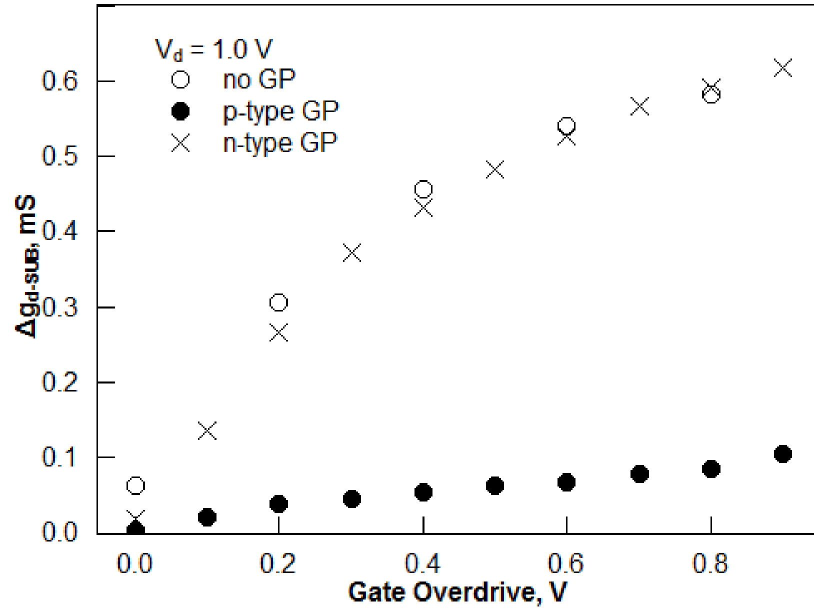

Figure 4.13. Amplitude of the output conductance transition due to the substrate effects as function of the gate overdrive at V_d = 1.0 V in the 100 nm gate length devices with and without GP.

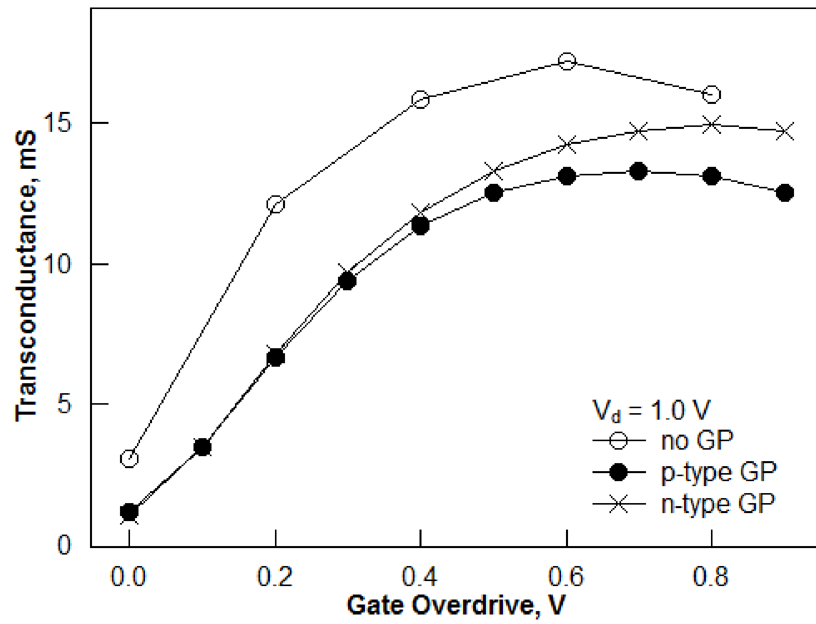

Figure 4.14. Transconductance variation with the gate overdrive at V_d = 1.0 V in the 100 nm gate length devices with and without GP.

Figure 4.15 shows the variation of $\Delta g_{d\text{-}SUB}$ with drain voltage at V_g-V_{th} = 0.4 V. Figure 4.16 shows identical characteristics at $V_g = V_{th}$. An increase in V_d results in an increase of $\Delta g_{d\text{-}SUB}$ in devices without a GP in both regimes of operation. For devices with a p-type GP, the substrate-BOX interface is always in accumulation and an increase in V_d does not affect $\Delta g_{d\text{-}SUB}$.

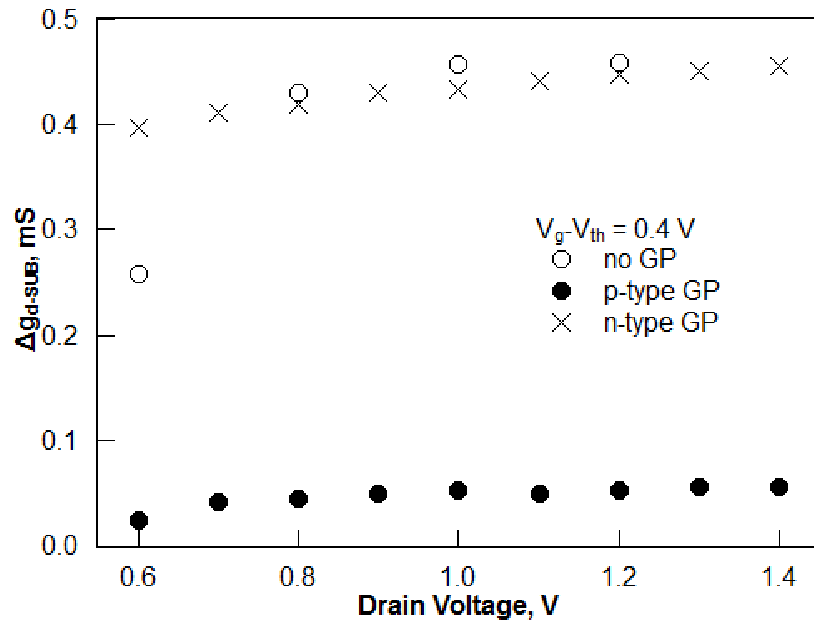

Figure 4.15. Amplitude of the output conductance transition due to the substrate effects as function of drain voltage at V_g-V_{th} = 0.4 V in the 100 nm gate length devices without a GP and with a GP.

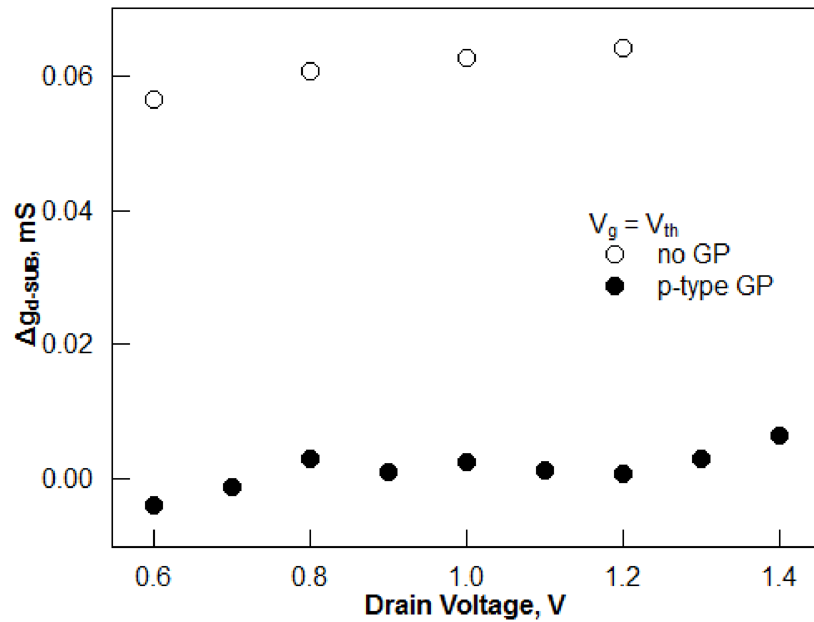

Figure 4.16. Amplitude of the output conductance transition due to the substrate effects as function of drain voltage at threshold in the 100 nm gate length devices without a GP and with a GP.

In order to compare the influence of self-heating on the output conductance for each device type, the variation of g_d due to self-heating is evaluated at different bias conditions. The

amplitude of the g_d transitions caused by self-heating is extracted as $\Delta g_{d\text{-}SH} = g_d(30\text{ MHz}) - g_d(100$ kHz). Figure 4.17 shows the variation in $\Delta g_{d\text{-}SH}$ with the dissipated power. According to ITRS, typical values of power are ~0.3-0.4 mW·µm^{-1} for low operating power and low standby power devices and ~1.2 mW·µm^{-1} for high performance devices of present and next generations [7]. At all power levels, the self-heating-related g_d increase is lower for devices incorporating a GP. This finding is not related to the GP itself because Si doping is not expected to alter its thermal conductivity significantly in the given temperature range [127]. Furthermore, the GP is thin and separated from the heat source. Therefore, it does not have any considerable effect on the heat propagation.

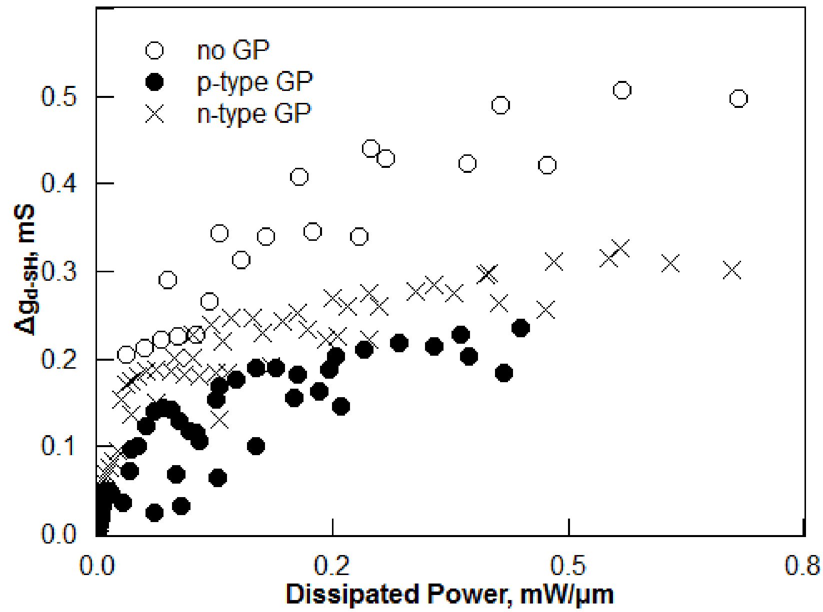

Figure 4.17. Amplitude of the output conductance transition due to the self-heating at various power levels in the 100 nm gate length devices with p-, n-type GP and without GP.

The lower self-heating in devices without a GP is likely to arise from the slightly thicker Si body (8 nm) compared with the devices without a GP (7 nm). Thicker Si films result in improved thermal properties due to weaker confinement and interface effects. Figure 4.18 shows the thermal resistance variation with the Si layer thickness obtained by Fiegna *et al.* in [81] simulating UTB devices with 25 nm gate length ad 50 nm BOX thickness. Figure 4.18 shows that the reduction of the Si thickness leads to the increased thermal resistance. Furthermore, if the Si thickness is under 15 nm (as it is the case for the studied devices in this work), the increase of the thermal resistance is the steepest. Therefore, a small change in Si thickness results in bigger degradation of thermal properties. Also, higher raised source and drain regions in the devices with a GP will contribute to the improved heat removal from the channel as it was shown

by Fiegna *et al.* by means of numerical simulations in [81]. Figure 4.19 is a plot from [81] demonstrating the reduction of the thermal resistance with the increase of the thickness of the raised source and drain regions. Similar work showing the dependence of the thermal properties on the source and drain extension shape was carried out in [50], [100].

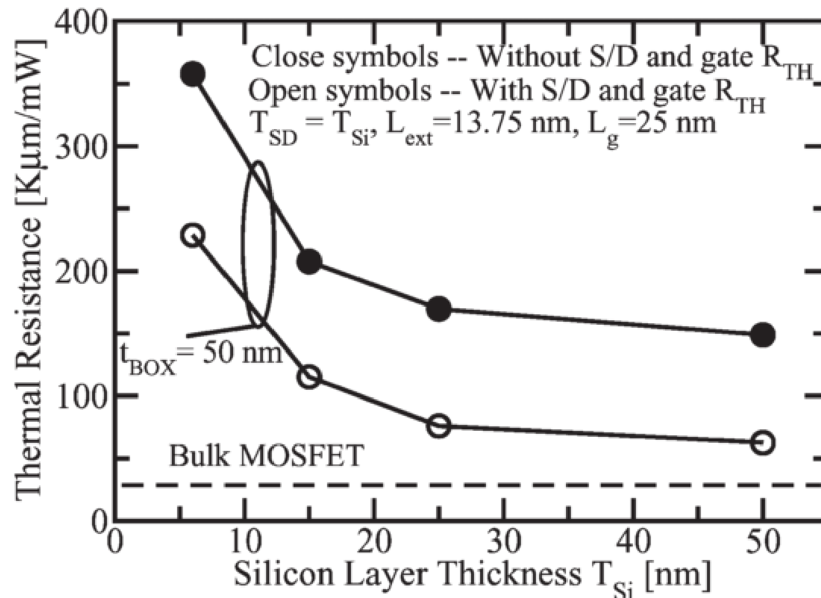

Figure 4.18. Simulated thermal resistance variation with silicon layer thickness in the 25 nm gate length UTB device. Open symbols: cooling effect through the source, drain and gate included. Filled symbols: adiabatic source, drain, and gate contacts. The horizontal dashed line represents the thermal resistance of 25 nm gate length bulk MOSFET. Taken from [81].

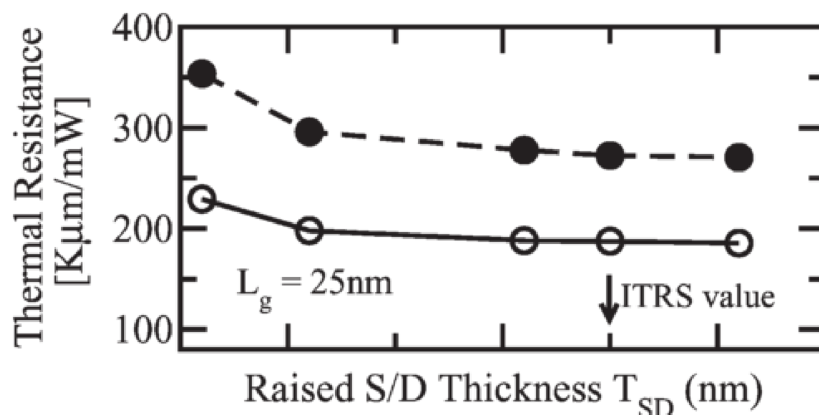

Figure 4.19. Simulated variation of the thermal resistance with the height of the raised source and drain regions in the 25 nm gate length UTB device. The arrow indicates the nominal value of the source and drain extension height prescribed by the ITRS 2005. Si thickness 6 nm, BOX thickness 50 nm, source and drain extension length 13.75 nm. Adapted from [81].

Figure 4.20 shows the ratio of the output conductance transition amplitudes due to substrate and self-heating effects in devices with and without a GP. The data is presented over a range of gate overdrive voltages up to 0.9 V. It can be seen that in devices with no GP, the transition amplitudes due to substrate effects are larger than those arising from self-heating (despite self-heating being stronger in devices without a GP than in the devices with a GP, see Figure 4.17). Conversely, the main source of output conductance degradation in devices with a GP is self-heating. This clearly demonstrates the efficiency of introducing a GP below the thin BOX to lower substrate effects (coupling through the substrate) and shows that UTBB devices have the potential to offer high performance in the analogue regime over the wide frequency range.

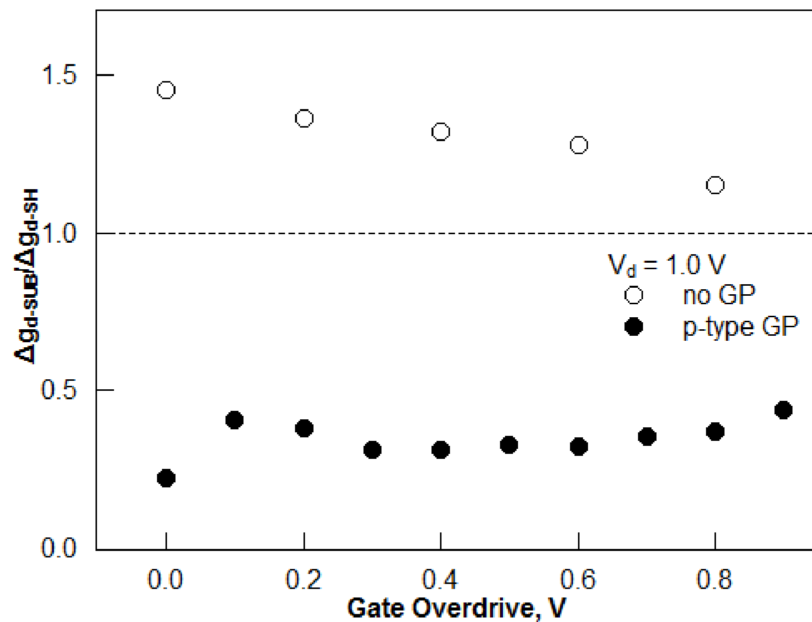

Figure 4.20. Ratio of the output conductance transition amplitudes due to the substrate and self-heating effects in the 100 nm gate length devices at various gate overdrives V_g-V_{th} and V_d = 1.0 V.

Intrinsic gain $A_v=20\cdot log(g_m/g_d)$ (dB) is extracted as a function of frequency in devices with and without a GP to evaluate performance degradation in the wide frequency range due to self-heating and substrate effects. Figure 4.21 shows the relative A_v variation with frequency from its value at 100 kHz. It can be seen that a GP enables considerably improved gain-frequency behaviour compared with the devices with no GP. A decrease of only ~12% from 100 kHz to 4 GHz is observed in the devices with a GP, whereas ~32% degradation is observed over the same frequency range for the devices without a GP. The higher intrinsic gain degradation due to the self-heating in the devices without a GP (20%) compared with the devices with a GP (10%) is primarily attributed to the slightly different structure (body thickness and source and drain

extensions) as discussed above. However, the difference in the gain degradation at high frequency (2% and 12%) in two devices is due to the presence and absence of a GP.

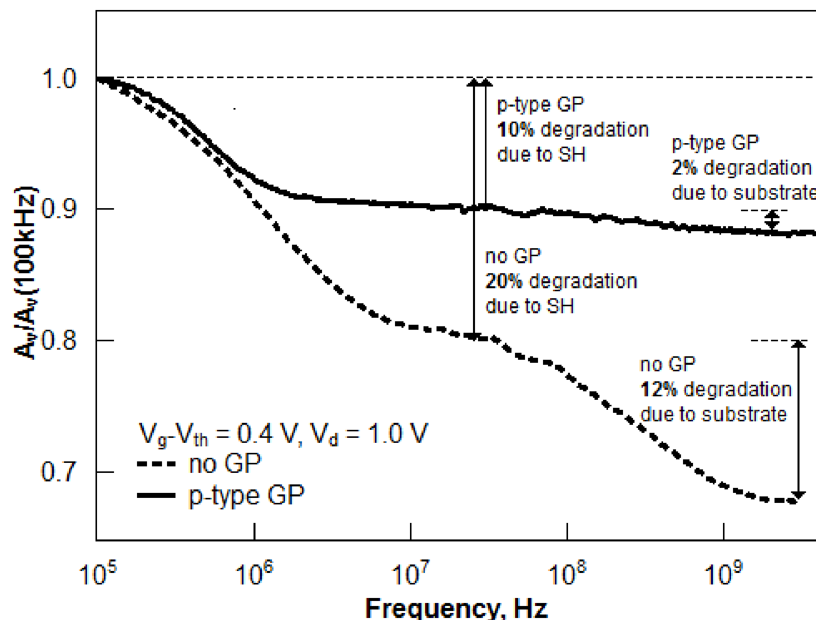

Figure 4.21. Relative intrinsic gain variation with frequency from its value at 100 kHz at V_g-V_{th} = 0.4 V and V_d = 1.0 V in the 100 nm gate length devices with and without GP.

Improved intrinsic gain of the GP devices over the wide frequency band suggests that UTBB technology with a GP may be beneficial for analogue applications. Implementation of a GP adds little complexity to the SOI fabrication process (except introduction of high doping in the substrate near the BOX-substrate interface without damage and contamination of the Si film and BOX) [13], [14], [36]. Multi-gate non-planar devices (e.g. FinFETs) are also known to suffer from the self-heating and are expected to suppress the substrate effects due to channel wrapping [44] (self-heating and substrate effects in FinFETs are further investigated in Chapter 6 in this thesis). However, the FinFET fabrication process requires some novel manufacturing methods (e.g. due to high aspect ratios), whereas the UTBB fabrication process can be naturally derived from bulk CMOS processing.

Since the data shows that the remaining main source of analogue performance degradation in devices with a GP is self-heating, thermal management is the main point to consider for further device improvement. Self-heating in UTBB devices is discussed in Chapter 5.

4.4 Summary

It has been experimentally shown that the output conductance degradation with frequency caused by substrate effects which result in source and drain coupling in UTBB SOI MOSFETs can be significantly reduced if a p-type heavily doped GP is incorporated below the BOX. The nMOSFET devices with 100 nm gate length used an 8 nm Si channel, a 10 nm BOX and a GP. The wideband frequency analysis shows that implementing a GP reduces the intrinsic gain degradation due to substrate effects at high frequencies compared with devices which do not have a GP.

Implantation of a GP adds an extra step to the fabrication process. The maximum of the doping distribution must be placed directly under the BOX without contaminating the channel and BOX. Apart from the suppression of the substrate effects, a GP allows for the threshold voltage modulation.

For UTBB devices with a GP, the major source of the output conductance degradation in a wide frequency range becomes self-heating. Self-heating occurs at frequencies below a few MHz and stabilises by ~30 MHz. It is expected that improvements to heat evacuation from the channel, for example with optimisation of source and drain extensions, will improve analogue performance for a wide range of frequencies.

The work has also demonstrated that substrate effects and self-heating can be observed through a variation of the total drain capacitance with frequency. Unlike the output conductance, which is most commonly used to identify substrate and self-heating effects, the total drain capacitance changes by over a few orders of magnitude and can therefore be readily used to determine the characteristic frequencies for these anomalies. It has been also shown that at high frequencies (above a few GHz) the total drain capacitance becomes independent of self-heating and substrate effects and is instead intrinsic to the device geometry.

Chapter 5. Self-heating in UTBB devices and impact of BOX thickness

5.1 Background and chapter outline

As it was shown in Chapter 3, self-heating impacts the output conductance variation with frequency in UTBB devices along with the substrate effects. The substrate effects and the use of a ground plane for their suppression were characterised and discussed in Chapter 4. It was also shown that further improvement of UTBB device performance over the wide frequency range requires management of the thermal properties. To achieve this, self-heating in UTBB technology has to be experimentally characterised. This includes accurate extraction of thermal parameters, as discussed in Chapter 2. The extracted thermal parameters then can be used to estimate how device performance is affected by self-heating, correct for thermal effects and/or adjust device design to minimise the impact. In Chapter 2 techniques to asses self-heating were compared using partially depleted silicon-on-insulator (PDSOI) devices with 400 nm thick BOX in order to understand the optimum technique. In this chapter the work is extended to UTBB devices, which are anticipated to exhibit improved thermal performance.

The two techniques (pulsed *I-V* hot-chuck method and the RF technique) are applied to quantify self-heating in advanced UTBB devices by extraction of the temperature rise, thermal resistance and the output current degradation caused by self-heating. These two methods were selected because they represent two different approaches in self-heating characterisation (time domain and frequency domain). Chapter 2 showed that the RF technique is expected to be more reliable for characterisation of advanced semiconductor devices as it can be applied to devices with time constants in the nanosecond range.

This chapter is organised as follows. The UTBB device performance is assessed taking the thermal properties into the account. The impact of the BOX thickness on thermal properties is evaluated using the RF methods (Section 5.3.2). In Section 5.3.3 results are discussed and compared with the results of PDSOI devices obtained in Chapter 2 and in the literature. The pulsed *I-V* technique (Section 5.3.4) is also applied and results are compared with the ones obtained with the RF method. Discussion of the heat evacuation paths in UTBB devices is presented in Section 5.3.5. The possible improvements to the future UTBB devices are suggested.

5.2 Device fabrication details

The devices are 100 nm gate length UTBB SOI n-channel MOSFETs with BOX thicknesses of 10 nm and 25 nm. The Si film thickness is 7.0 nm and 7.5 nm, the gate dielectric equivalent oxide thickness is 2.3 nm and 1.9 nm and the height of the source and drain extensions is 18 nm and 15 nm, respectively, for the 10 nm and 25 nm-thick BOX devices. HfSiON dielectric and TiN gate form the gate stack. Cross-sections of the devices co-processed with the studied devices are shown in Figure 5.1. The images were obtained with transmission electron microscopy [41], [132].

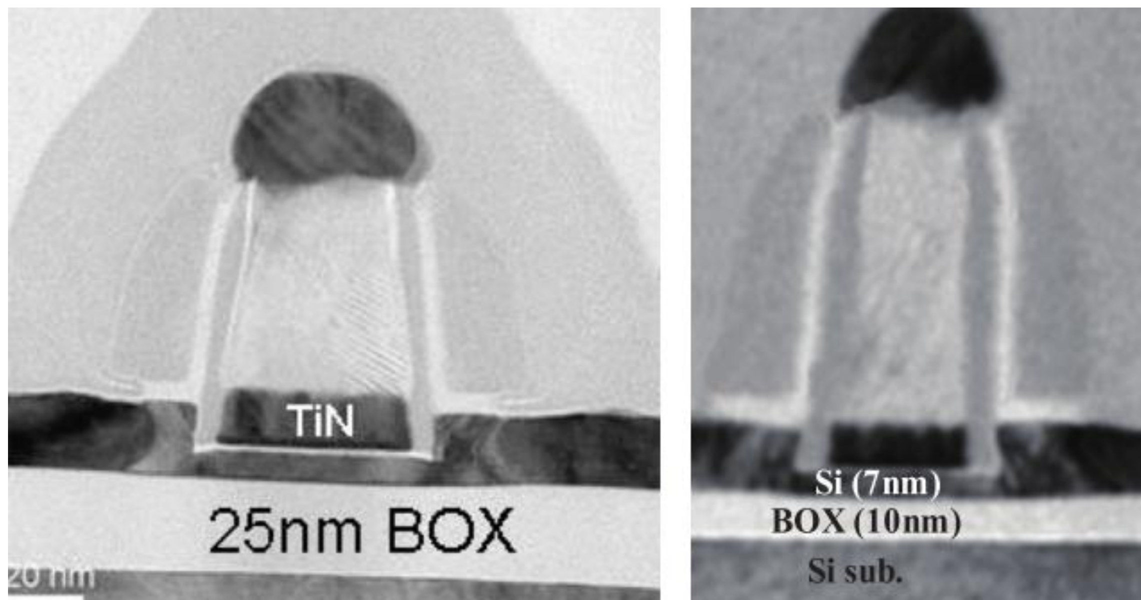

Figure 5.1. Transmission electron microscopy images of the UTBB devices cross-sections with BOX thickness of 25 nm [41] and 10 nm [132]. The devices were co-processed with the studied devices.

5.3 Results and discussion

5.3.1 Current-voltage characteristics

Transfer characteristics and statistical data of the UTBB devices on 10 nm BOX were presented in Section 3.3.1. It was shown that 100 nm gate length devices exhibit better uniformity than their 30 nm and 50 nm gate length counterparts. Therefore, 100 nm gate length devices with 10 nm BOX were selected for self-heating characterisation and comparison with devices built on 25 nm BOX. Figure 5.2 shows transfer characteristics of a number of UTBB devices across the wafer with 100 nm gate length and 25 nm BOX at the drain voltage of 1.0 V.

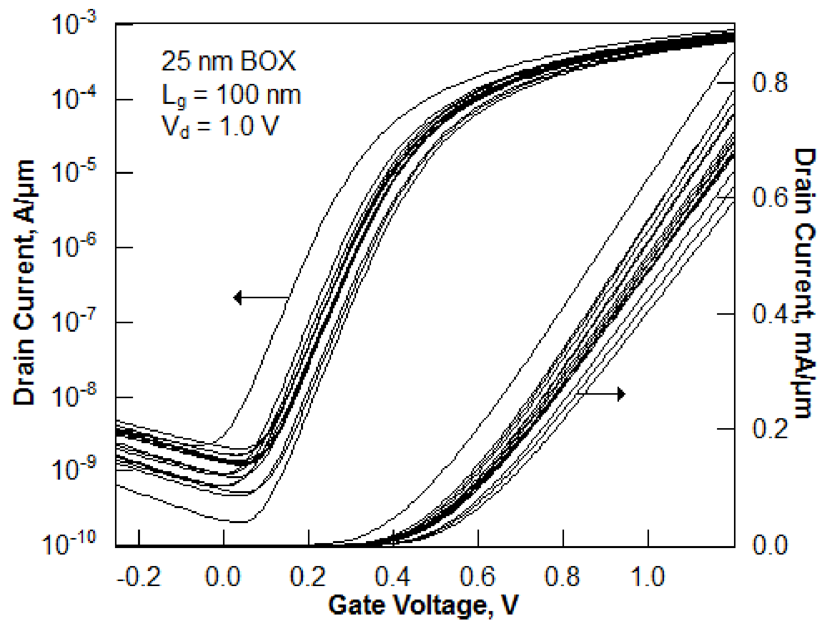

Figure 5.2. Transfer characteristics of 100 nm gate length UTBB devices on 25 nm BOX at V_d = 1.0 V.

In Figure 5.3 the off-state drain current (V_g = 0 V, V_d = 1.0 V) is compared with the on-state drain current (V_g = V_d = 1.0 V) in the UTBB devices with 25 nm BOX and 100 nm gate length. The on-state drain current is dispersed between 0.40 mA·µm^{-1} and 0.65 mA·µm^{-1}. As expected, devices with a higher on-state current exhibit a higher off-state current. There was no correlation observed between the device characteristics and device location on the wafer.

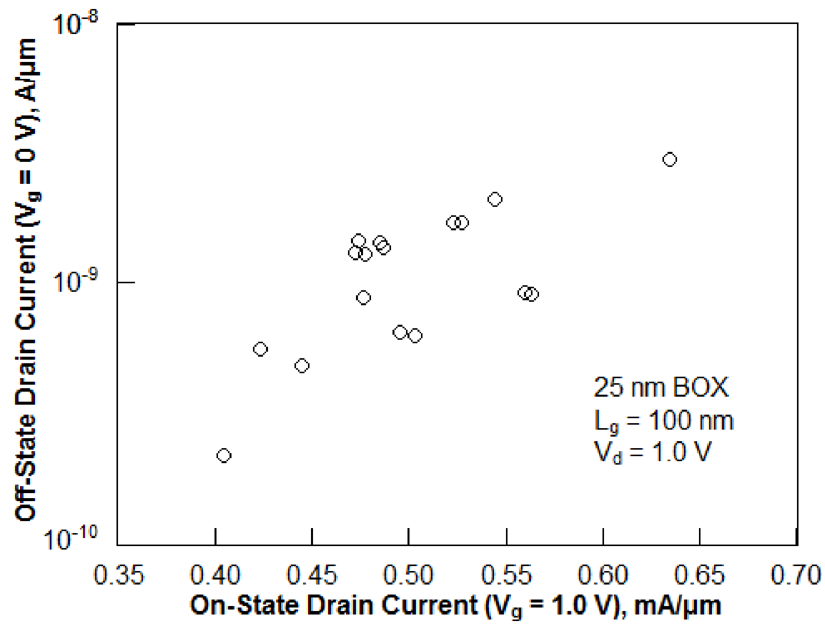

Figure 5.3. Off-state drain current (V_g = 0 V, V_d = 1.0 V) compared with the on-state drain current (V_g = 1.0 V, V_d = 1.0 V) in UTBB devices with 25 nm BOX and 100 nm gate length.

Figure 5.4 shows typical transfer characteristics of 100 nm gate length UTBB devices with 10 nm and 25 nm BOX selected for further self-heating characterisation. Though the characteristics differ at low gate voltages, they are similar at high gate voltages where self-heating characterisation is performed. BOX thinning offers better control over the drain induced barrier lowering (DIBL) as it was shown in [14], [30] for UTBB devices with various BOX thicknesses. DIBL can be evaluated from separation between V_d = 20 mV and V_d = 1.0 V curves in the subthreshold regime in Figure 5.4. As expected, 10 nm BOX devices exhibit better DIBL (35 $mV\cdot V^{-1}$) than 25 nm BOX devices (43 $mV\cdot V^{-1}$).

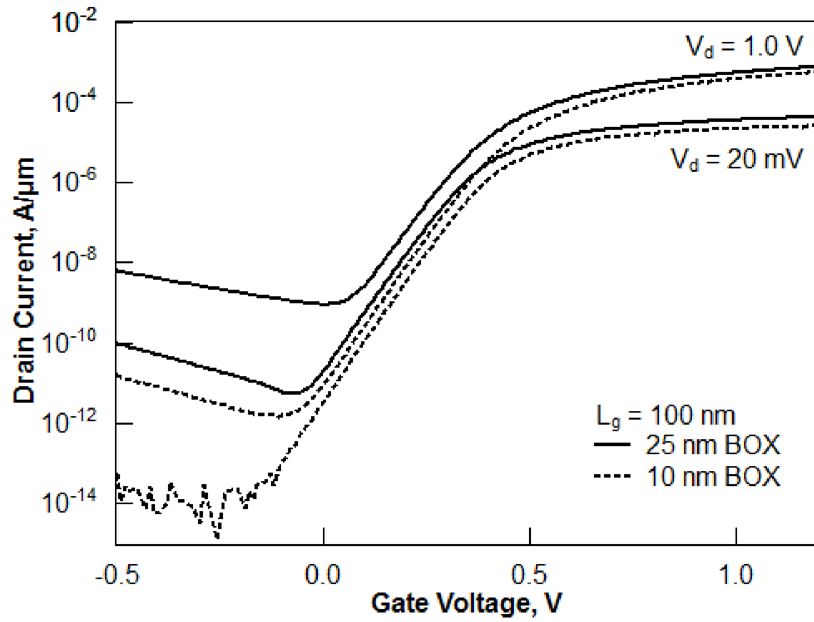

Figure 5.4. Transfer characteristics of the selected 100 nm gate length UTBB devices with 10 nm and 25 nm BOX at V_d = 20 mV and V_d = 1.0 V.

5.3.2 RF self-heating characterisation

In order to extract self-heating parameters such as the thermal resistance using the RF method, Chapter 2 has shown that the output conductance, g_d, has to be extracted over the wide frequency range. S-parameters were measured, de-embedded and transformed into Y-parameters. The real part of the Y_{22} parameter is the output conductance. More detailed explanation of the characterisation procedure using S-parameters was presented in Section 2.4.2.1. Figure 5.5 shows the normalised output conductance variation with frequency in 100 nm gate length UTBB devices with 10 nm BOX with the gate voltage, V_g, varying from 0.4 V to 1.2 V and drain voltage, V_d, fixed to 1.0 V. The frequency was swept from 100 kHz to 4 GHz. In Figure 5.6 identical characteristics are shown for devices with 25 nm-thick BOX. The output conductance variation in this frequency range is expected to be determined by two effects as it was shown in Section 3.3.3. The output conductance transition due to the self-heating effect appears in a frequency range, between a few kHz and up to a few hundred MHz in advanced devices. Dependence of this transition on the applied biases and gate length was presented in Section 3.3.4. The second transition at higher frequencies (between ~100 MHz and few GHz) is caused by the source and drain coupling through the substrate. The amplitude of this transition depends on the applied bias as it was shown in Section 3.3.5 and can be effectively suppressed by a ground plane as it was shown in Chapter 4.

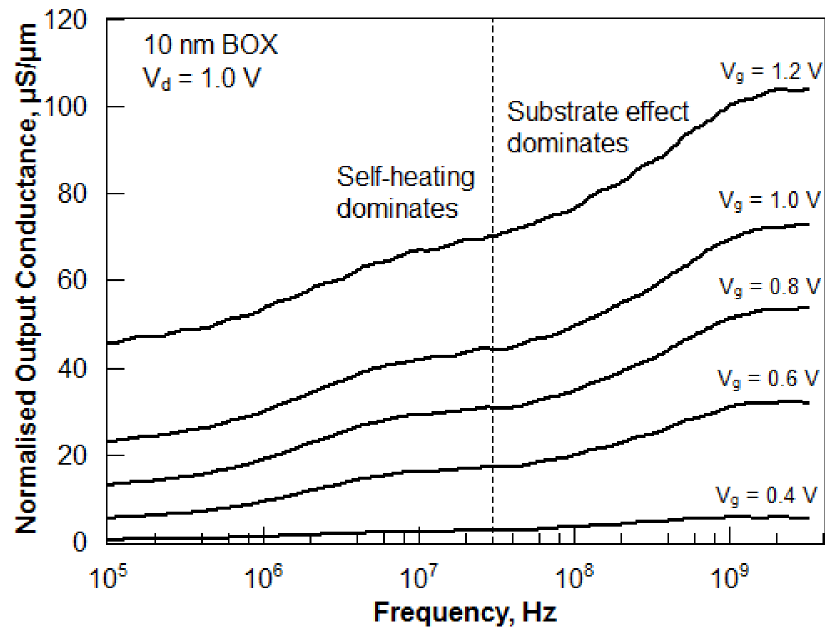

Figure 5.5. The output conductance variation with frequency in 100 nm gate length devices with 10 nm BOX at gate voltages from 0.4 V to 1.2 V and V_d = 1.0 V.

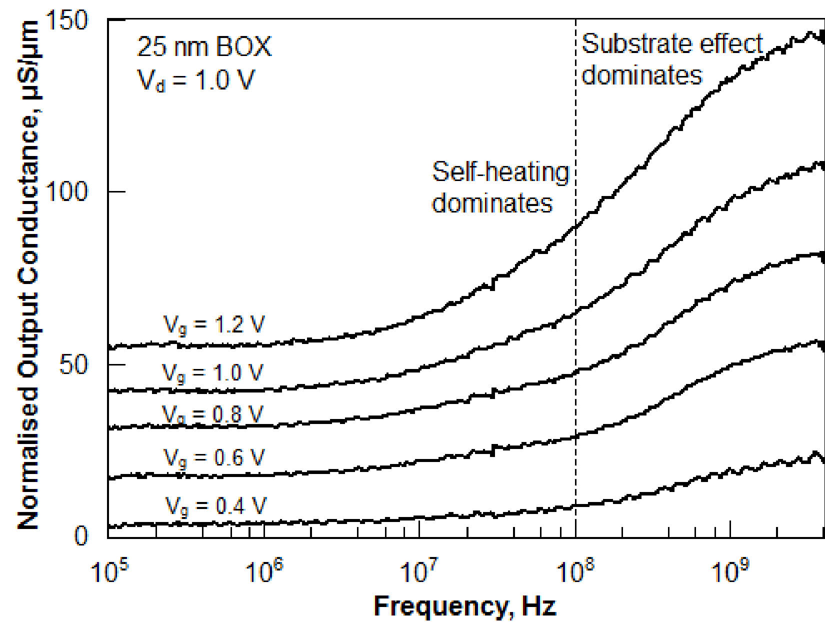

Figure 5.6. The output conductance variation with frequency in 100 nm gate length devices with 25 nm BOX at gate voltages from 0.4 V to 1.2 V and V_d = 1.0 V.

The two transitions are clearly seen at all bias conditions in the output conductance variation of 10 nm-thick BOX devices in Figure 5.5. The self-heating related transition appears between 100 kHz and ~30 MHz and the substrate effect-related transition appears between ~100 MHz and 1 GHz. In order to characterise self-heating, the corresponding output conductance transition has to be clearly

distinguishable. However, in the case of the devices with 25 nm-thick BOX (Figure 5.6) the output conductance transitions caused by two effects are not well separated and not clearly distinguishable at high gate voltage. Since both self-heating and substrate effects depend on bias conditions (Sections 3.3.4 and 3.3.5), the output conductance variation with frequency in Figure 5.5 and Figure 5.6 is presented for various gate voltages. This allows to distinguish between two transitions in UTBB devices with 25 nm-thick BOX. As seen from Figure 5.6, at low gate voltage a bend above ~100 MHz can be observed. It can be supposed that the self-heating characteristic frequency at which dynamic self-heating is removed, does not depend (at least in the first approximation) neither on the gate voltage, nor on the drain voltage [94]. Therefore, the characteristic frequency can be determined. In this case, 100 MHz was found as self-heating free. Further extraction of thermal properties in the UTBB devices with 25 nm-thick BOX was performed assuming the output conductance transition due to self-heating being between 100 kHz and 100 MHz.

The output conductance variation in the UTBB devices with 10 nm-thick BOX showed slightly lower frequency at which the dynamic self-heating is removed (Figure 5.5). This might be related to some differences in the structure of the devices. Larger source and drain extension height in 10 nm BOX MOSFETs (18 nm) compared with 25 nm BOX MOSFETs (15 nm) may result in slightly lower characteristic thermal frequency. Dependence of thermal properties on the source and drain extension geometry has been discussed in Section 4.3.3 (see Figure 4.19) and in [50], [81], [100], [126].

Figure 5.7 shows the amplitude of the output conductance transition due to self-heating, $\Delta g_{d\text{-}SH}$, at gate voltages from 0.4 V to 1.2 V in 100 nm gate length devices with 10 nm and 25 nm BOX. The drain voltage was kept constant at 1.0 V. Due to similar threshold voltages in both devices (0.4 V), the gate overdrive is the same for both types of devices enabling a fair comparison. The amplitude of the transition can reach 30-35 $\mu S \cdot \mu m^{-1}$ in devices with 10 nm and 25 nm-thick BOX. The output conductance transition is almost the same in the case of both BOX thicknesses in the wide gate bias range. Only at very high gate voltages (where self-heating is amplified) the output conductance transition in devices with thinner BOX becomes smaller than in devices with thicker BOX. This is due to improved heat removal through the thin BOX. Also, the relative degradation of the output conductance to its value at the low frequency, $\Delta g_{d\text{-}SH}/g_{d0}$, (extracted from the characteristics shown in Figure 5.5 and Figure 5.6) is similar in devices with 25 nm and 10 nm-thick BOX, ~60% and ~55%, respectively, at V_g = 1.2 V, V_d = 1.0 V. The increase of the output conductance with frequency can be directly translated into the reduction of

intrinsic gain with frequency, thus being of utmost importance for analogue device performance [145].

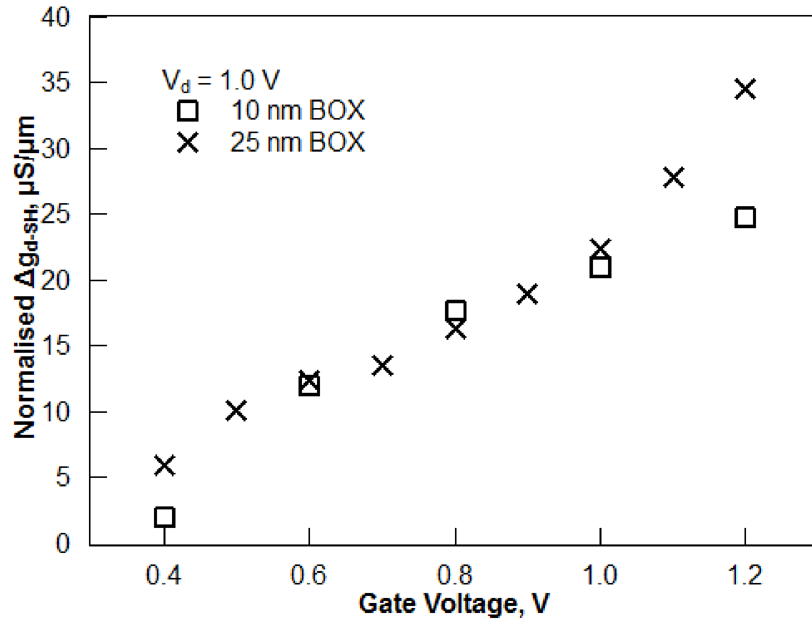

Figure 5.7. Variation in normalised amplitude of the output conductance transition due to self-heating with the gate voltage in 100 nm gate length UTBB transistors with 10 nm and 25 nm BOX.

The amplitude of the output conductance transition due to self-heating was used to extract the thermal resistance, R_{th}, implementing the method described in Section 2.4.2 [95]:

$$g_{d0} = g_{dT} + R_{th} \frac{\partial I_d}{\partial T_A} (V_d g_{dT} + I_d), \tag{5.1}$$

where g_{d0} is the output conductance at low frequency with dynamic self-heating effect present, g_{dT} is the output conductance at high frequency with the dynamic self-heating effect removed, I_d is the drain current, $\partial I_d / \partial T_A$ is the drain current variation with ambient temperature, which was extracted from the linear fit of the hot chuck measurements. The thermal resistance is the main figure of merit used to quantify self-heating.

Section 2.4.2.2.2 discussed how the RF self-heating characterisation technique is sensitive to the accuracy of $\partial I_d / \partial T_A$ extraction. Furthermore, the technique can be applied only for relatively high gate voltage (higher than zero temperature coefficient, ZTC, point), where the drain current variation with temperature is dominated by the mobility degradation. In the both types of the studied devices, ZTC point is at ~0.8 V in the saturation regime. Therefore, the extraction of the thermal resistance was carried out at the gate voltage 1.2 V.

In the UTBB devices with 25 nm-thick BOX the extracted lumped thermal resistance is 84 μm·K·mW^{-1} and in devices with 10 nm-thick BOX the obtained thermal resistance is 70 μm·K·mW^{-1}. The temperature rise ΔT and the thermal resistance are related according to:

$$\Delta T = R_{th} I_d V_d. \quad (5.2)$$

At V_g = 1.2 V and V_d = 1.0 V the resulting average temperature rise is 65 °C and 37 °C in UTBB devices with 25 nm and 10 nm BOX, respectively. The doubled higher temperature rise in the 25 nm-thick BOX devices is due to both higher thermal resistance and higher dissipated power at the fixed bias conditions. As expected, the lumped thermal resistance and the temperature rise in devices with thinner BOX are lower compared to devices with thicker BOX due to improved heat dissipation through the thinner BOX.

5.3.3 Comparison with literature and PDSOI devices

As expected, the experimentally extracted thermal resistance values are lower than predicted by simulations in [81] for a UTB device with 50 nm BOX and non-raised source and drain regions. In [81] the thermal resistance value predicted for a device with 7-8 nm thick Si channel is ~150 μm·K·mW^{-1} for the case when heat evacuation through source and drain regions is considered (see Figure 4.18 in Chapter 4). In this work the BOX is thinner in both types of devices (10 nm and 25 nm). This results in lower thermal resistance. Also, devices used in this work feature raised source and drain regions which facilitate heat removal and lead to improved thermal properties [50], [81]. Due to thinner BOX and raised source and drain regions in the UTBB devices, experimentally obtained values of the thermal resistance approach values of the bulk MOSFET (~35 μm·K·mW^{-1}), also reported in [81] and in Figure 4.18.

In Chapter 2, the thermal resistance was extracted in 240 nm gate length PDSOI devices with 400 nm-thick BOX and 150 nm-thick Si body. The extracted thermal resistance was ~220 μm·K·mW^{-1} and the temperature rise was above 125 °C when the power was above 0.6 mW·μm^{-1} (the power levels of the studied UTBB devices at V_g = 1.2 V and V_d = 1.0 V). These results were shown in Section 2.4.2.2.3. Table 5.1 summarises thermal resistance values of UTBB and PDSOI devices.

Table 5.1. Thermal resistance extracted using the RF technique and main parameters of UTBB and PDSOI devices.

Devices	t_{BOX}, nm	t_{Si}, nm	R_{th}, μm·K·mW^{-1}
UTBB	10	7	70
UTBB	25	7.5	84
PDSOI	400	150	220

The thermal resistance of the PDSOI devices is ~3 times higher than the thermal resistance of the UTBB devices. This is related to the very thick BOX in the PDSOI devices which is up to 40 times thicker than in the UTBB devices. Using a thick Si channel in PDSOI devices (150 nm) is expected to reduce the interface effects and slightly alleviate self-heating. But the body dimensions are still in the order of the phonon mean free path leading to the phonon boundary scattering [79]. These results confirm that UTBB MOSFETs exhibit much better thermal properties than PDSOI devices. Therefore, UTBB technology can be more beneficial than PDSOI technology for applications where high temperatures cannot be tolerated (e.g. in devices with high-κ dielectrics which are prone to trap-assisted tunnelling that is aggravated with temperature).

5.3.4 Pulsed I-V characterisation

The pulsed *I-V* technique is an alternative self-heating characterisation method along with the RF technique. These two techniques represent two different approaches to characterising self-heating and are compared in Chapter 2.

The pulsed *I-V* technique was also applied to the UTBB devices with 10 nm and 25 nm-thick BOX. Figure 5.8 and Figure 5.9 show DC and pulsed output characteristics obtained with various pulse widths from 1 μs to 50 ns at V_g = 1.2 V and fixed chuck temperature 25 °C in the 100 nm gate length UTBB devices with 10 nm and 25 nm BOX, respectively. The drain current increases as the pulse width decreases and, consequently, device heating reduces. However, convergence of the pulsed *I-V* data with pulse reduction was not observed. This might indicate that shorter pulses are required. Though shorter pulses (down to 10 ns) were available, they were distorted due to the set-up and the devices under test limitations and hence are not suitable for fair comparative analysis. Therefore, for the rest of the work, the UTBB devices were studied using the pulsed *I-V* technique with the pulse width of 50 ns.

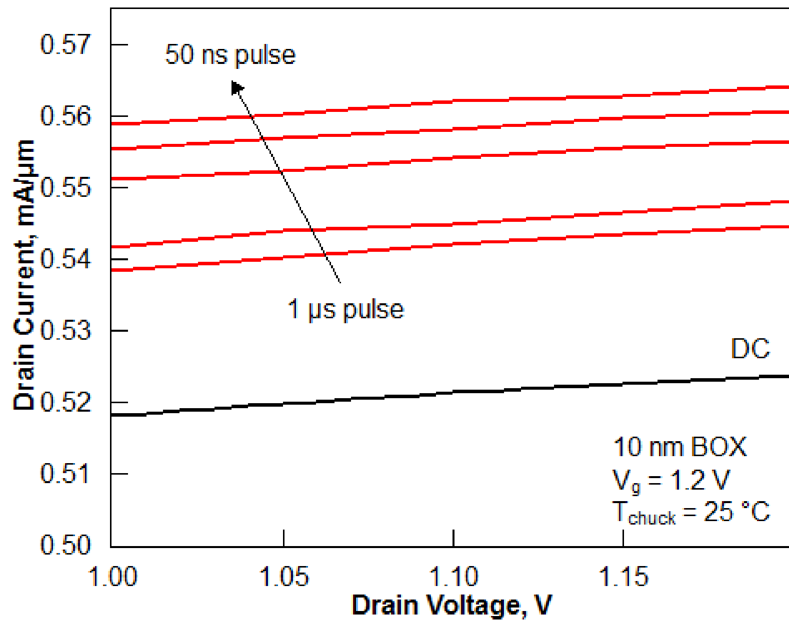

Figure 5.8. DC and pulsed output characteristics with pulse widths 1 μs, 500 ns, 200 ns, 100 ns and 50 ns at V_g = 1.2 V and a fixed chuck temperature of 25 °C in the UTBB devices with 10 nm BOX.

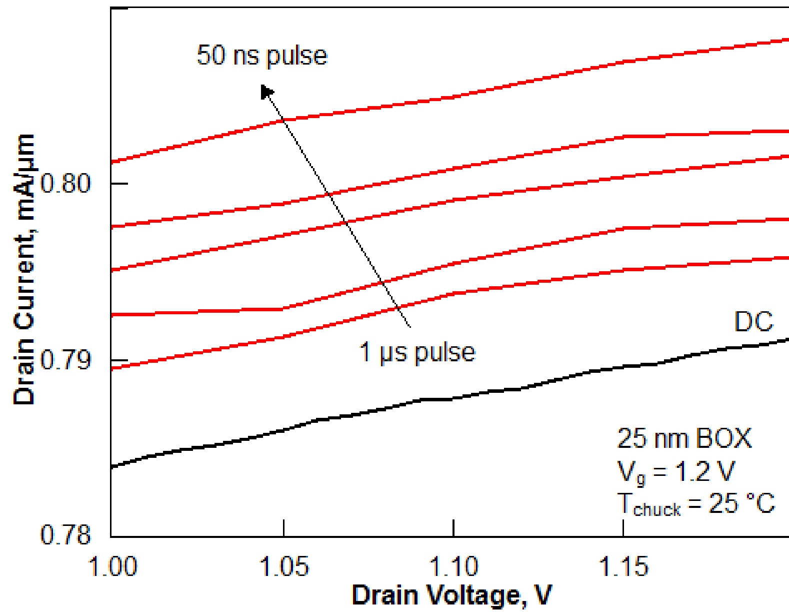

Figure 5.9. DC and pulsed output characteristics with pulse widths 1 μs, 500 ns, 200 ns, 100 ns and 50 ns at V_g = 1.2 V and fixed chuck temperature 25 °C in the UTBB devices with 25 nm BOX.

The pulsed output characteristics of UTBB MOSFETs at temperatures above ambient were compared with the DC output characteristics at room temperature using the method described in

Section 2.3.2 and in [110]. Briefly, the temperature of the chuck at which the self-heating free pulsed drain current coincides with the room temperature DC drain current indicates the temperature in the device. Figure 5.10 shows the resulting output characteristics in UTBB MOSFETs with 10 nm BOX at V_g = 1.2 V. Figure 5.11 shows the same characteristics in the 25 nm-thick BOX UTBB devices. The pulsed measurements were performed at chuck temperatures from the room temperature up to 125 °C.

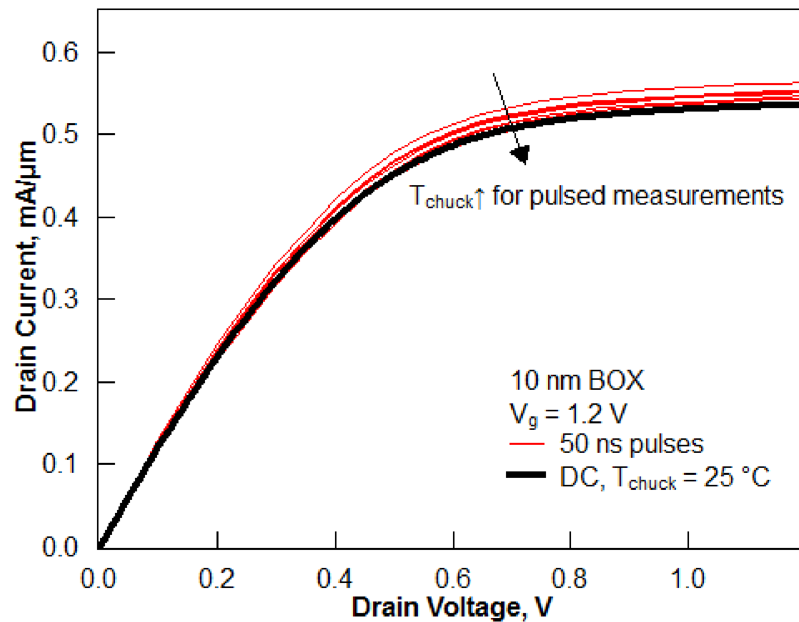

Figure 5.10. DC output characteristics at V_g = 1.2 V at the room temperature compared with pulsed output characteristics at chuck temperatures from the room temperature up to 100 °C in devices on 10 nm BOX. The pulse width is 50 ns.

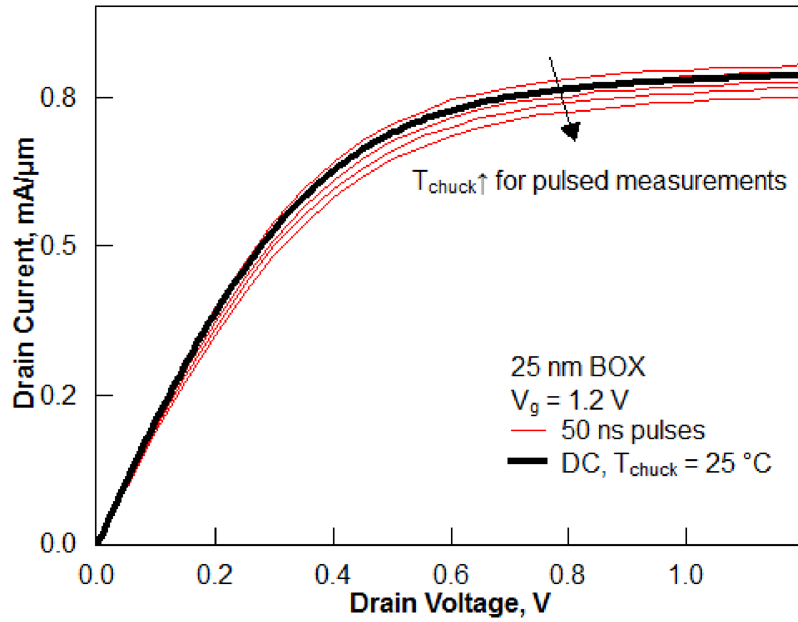

Figure 5.11. DC output characteristics at V_g = 1.2 V at the room temperature compared with pulsed output characteristics at chuck temperatures from the room temperature up to 125 °C in devices on 25 nm BOX. The pulse width is 50 ns.

In 10 nm-thick BOX devices, the lumped temperature rise extracted by the pulsed *I-V* technique is 38 °C at V_g = 1.2 V and V_d = 1.0 V. It agrees well with the temperature rise extracted by the RF self-heating extraction method (37 °C) shown in Section 5.3.2. In the case of 25 nm-thick BOX devices, the temperature rise is 33 °C at V_g = 1.2 V and V_d = 1.0 V. This value is considerably lower than extracted with the RF self-heating extraction method (65 °C) and seems to be underestimated. This may be because 50 ns-wide pulses are insufficient to remove self-heating completely. This agrees with predictions made in Chapter 2 where the pulsed *I-V* and RF techniques were compared. The pulse width can be related to the characteristic frequency as described in Section 2.6:

$$f = \frac{1}{2\pi\tau_p}, \tag{5.3}$$

where f is the frequency and τ_p is the pulse width. The dynamic self-heating is removed only at ~100 MHz in the studied 25 nm-thick BOX devices as seen from Figure 5.6. Therefore, according to Equation 5.3 much narrower, ~2 ns pulses would be required to suppress self-heating in these devices, which was technically unavailable. This may explain the low (underestimated) temperature rise and thermal resistance in UTB devices with 6 nm Si film thickness and 145 nm thick BOX, characterised by Rodriguez *et al.* in [92] using pulsed *I-V* with mobility degradation coefficient. This method was explained in Section 2.3.3 and it was shown

to underestimate self-heating in PDSOI devices in Section 2.6 in contrast with the pulsed *I-V* hot chuck and RF techniques. Pulse width clearly appears as a main limitation of the pulsed *I-V* technique especially for devices with high characteristic thermal frequency where very short pulses are required. Therefore, the pulsed *I-V* technique is only suitable for devices with relatively big thermal time constants which are usually not observed in state of the art semiconductor devices.

An advantage of the pulsed *I-V* technique is that it enables direct extraction of the self-heating free drain current. Comparing this with the DC drain current allows evaluation of degradation of the drain current caused by self-heating. In UTBB devices the drain current degradation due to self-heating is ~6% and ~7% at V_g = 1.2 V, V_d = 1.0 V for 10 nm and 25 nm-thick BOX, respectively. In devices built on 25 nm-thick BOX, the pulsed drain current was extrapolated in order to estimate the current degradation due to self-heating. The obtained output current degradation results agrees with results in [92] where ~5% current degradation was observed in 100 nm gate length UTB devices. The saturation drain current degradation in the studied UTBB devices is smaller compared with devices on thick BOX (up to 32% [94], [101], [110]) and on SiGe buffer (up to 19% [109]). This is believed to be due to the threshold voltage shift and the drain current degradation with temperature being strongly reduced in advanced devices featuring thin gate oxide, undoped channel and relatively high impact of the series resistance. Therefore, the BOX thickness reduction from 25 nm to 10 nm appears to be less critical from the thermal perspective. BOX thickness in UTBB can be relaxed to improve uniformity requirements and simplify fabrication process without significantly affecting thermal properties and degradation of the output conductance and drain current. The high output current is desired as it allows faster charging of capacitors in a circuit, thus improving the circuit speed. Also thicker BOX might be used to reduce coupling (substrate effects) and possible parasitic leakage current through the substrate.

5.3.5 Heat evacuation paths in UTBB MOSFETs

In SOI MOSFETs the main paths by which heat escapes from the channel are through the BOX to the substrate and through the source and drain regions to interconnects. It can be assumed that the dielectric passivation layer above the gate stack is too thick and therefore heat removal through the gate stack is considerably lower than through the BOX, source and drain.

A simple model to evaluate the thermal resistance of the thermal path through the BOX, $R_{th\text{-}BOX}$, is described in Section 2.5. Applying this model and considering the decrease of the

thermal conductivity of Si from 148 $W \cdot m^{-1} \cdot K^{-1}$ in bulk Si to 13 $W \cdot m^{-1} \cdot K^{-1}$ in ~10 nm Si film [79], normalised R_{th-BOX} are found to be 207 $\mu m \cdot K \cdot mW^{-1}$ and 131 $\mu m \cdot K \cdot mW^{-1}$ in 25 nm and 10 nm-thick BOX devices, respectively. These values are significantly higher than the thermal resistance of 84 $\mu m \cdot K \cdot mW^{-1}$ and 70 $\mu m \cdot K \cdot mW^{-1}$ extracted in this work. Moreover, such analytical approach predicts ~1.6 times decrease of the thermal resistance due to BOX thinning from 25 nm to 10 nm, while ~1.2 times reduction of the thermal resistance is extracted from the experimental results. This suggests that the heat removal in UTBB devices occurs not only through the BOX but also through other thermal paths, most likely, through the source and drain regions. This is especially beneficial to shorter devices, where the source and drain regions are situated closer to the heat source. Reduction of the thermal resistance in UTB devices with the gate length scaling under 100 nm was observed in [92], [99].

As multiple thermal paths exist (BOX, source and drain extensions), the overall device thermal resistance is lower than the thermal resistance of any single thermal path (parallel thermal resistors). Therefore, in ultra-thin BOX devices where the heat conduction through the BOX is relatively good, the size and shape of source and drain regions may instead be critical from the thermal point of view [50], [81], [100], [126].

Since the BOX is extremely thin, the thermal resistivity of the Si substrate underneath the BOX should also be accounted for. The thermal resistance of the substrate is in series with the thermal resistance of the BOX and therefore would increase the overall thermal resistance of the thermal path through the BOX.

5.4 Summary

Self-heating in UTBB SOI MOSFETs with two different BOX thicknesses has been characterised by RF and pulsed *I-V* techniques. It has been shown that due to the relatively high characteristic frequency of self-heating in advanced devices (in the range of 10-100 MHz), the RF technique must be used for self-heating assessment in advanced UTBB SOI MOSFETs. The pulsed *I-V* method may underestimate thermal effects in UTBB devices. This was predicted in Chapter 2 which compared various self-heating characterisation techniques.

It has been demonstrated that for 100 nm gate length UTBB devices, despite the ultra-thin BOX, thermal effects are considerable. The average temperature rise reaches 38 °C and 65 °C at V_g = 1.2 V and V_d = 1.0 V in devices with 10 nm and 25 nm-thick BOX, respectively. Such temperature rise results in 6-7% degradation of the drain current for both devices. This

degradation is significantly less than in MOSFETs on thick BOX or SiGe buffers. The main problem caused by self-heating in advanced UTBB devices is the output conductance degradation which may reach 60%. This is an important issue for analogue applications as it results in the undesirable frequency-dependent analogue behaviour.

There is almost no difference in the output conductance and drain current degradation caused by device heating in 10 and 25 nm-thick BOX devices at fixed bias conditions. Therefore, thicker BOX might be used to reduce parasitic coupling and leakage through the substrate, without having much impact on the drain current and the output conductance caused by thermal effects. Thicker BOX also relaxes uniformity requirements imposed on UTBB technology.

The extracted values of thermal resistance in the UTBB devices are ~3 times lower than in PDSOI thick BOX MOSFETs (70-84 $\mu m \cdot K \cdot mW^{-1}$ compared with 220 $\mu m \cdot K \cdot mW^{-1}$). The thermal resistance values of the UTBB devices approach those of bulk Si device, which is an indication of enhanced heat evacuation by source and drain regions and Si substrate. Therefore, UTBB technology with 10 or 25 nm BOX should not be considered a hindrance due to thermal effects. Instead it can be implemented in the analogue applications where the performance is sensitive to thermal properties of devices.

Chapter 6. Self-heating and substrate effects in FinFETs

6.1 Background and motivation

Along with UTBB devices (discussed in Chapter 3, Chapter 4 and Chapter 5), FinFETs are fully depleted SOI devices which are expected to provide a few extra generations of Moore's law. Both FinFETs and UTBB devices exhibit self-heating and substrate effects. However, the difference in UTBB and FinFET architecture (2D and 3D) may be expected to be translated into a difference in the impact of these effects. Self-heating and substrate effects were studied in previous chapters for UTBB devices. In this chapter the self-heating and substrate effects are examined in FinFETs.

As described in the introduction (Section 1.7.3), most publications relating to thermal properties in FinFETs are based on numerical simulations [48–50], [97–100]. Experimental characterisation of self-heating in FinFETs was carried out only in [86], [96]. However, the dependence of the thermal properties on the FinFET geometry has not been studied experimentally. The aim of this chapter is to extract the thermal resistance, thermal capacitance and the temperature rise in FinFETs of various geometries experimentally. The varied FinFET parameters are the fin width, number of parallel fins and the fin spacing. Geometry parameters are expected to have impact on thermal properties as it was predicted by numerical simulations [48–50], [100]. Also, FinFET geometry parameters affect device design and fabrication processes as well as performance. Fin width affects gate control over charge in the channel and therefore device performance. Fins are arranged in parallel to obtain certain gate width and length ratios in order to achieve required drain currents (see Equation 1.3). Therefore, the number of parallel fins per gate finger is an important parameter. Smaller number of fins per finger allows for easier circuit design. Fin spacing is defined as the distance between parallel fins. Smaller spacing enables to pack more fins per unit area. Experimental self-heating characterisation in FinFETs of various geometries can identify trade-offs between device thermal properties and all aforementioned factors.

Frequency dependent behaviour of an SOI MOSFET arises not only from self-heating but also from source and drain coupling through the substrate. Substrate effects introduce output conductance variations at low and high frequencies as it was discussed in Chapter 3 for UTBB devices. Low frequency substrate effects in FinFETs were studied experimentally and by numerical simulations in [44]. It was shown that the low frequency transition can be effectively

suppressed if the fin is sufficiently narrow. It was concluded that low frequency substrate effects are almost negligible in 70 nm-wide fin devices. In this chapter the output conductance transition caused by substrate effects in the high frequency region and its variation with fin width is analysed. Fin width was chosen as a variable because it is a critical FinFET parameter for digital and analogue performance [146].

The intrinsic voltage gain is an important analogue figure of merit. Its variation with frequency can be used to evaluate the overall effect of self-heating and substrate effects on FinFETs performance. The impact of self-heating on the intrinsic gain in FinFETs has previously been studied [86]. It was shown that self-heating causes a more significant gain variation over the wide frequency range in nMOSFETs than in pMOSFETs. Also it was shown that the gain significantly depends on the gate length and can become negative in long channel devices. Dependence of intrinsic voltage gain on fin width is also studied here.

6.2 Experimental details

6.2.1 Device details

40 nm gate length n-channel FinFETs were fabricated on SOI wafers with 145 nm-thick BOX. Fin patterning (resulting in a 60 nm fin height) is followed by gate stack (HfO_2 dielectric + TiN gate) deposition, spacer formation, highly doped drain (HDD) implant, Ni silicidation and Cu Back-End-of-Line (BEOL). The background doping of the silicon fins is 10^{15} cm^{-3}, and no additional fin doping, threshold voltage adjust implants or halo (pocket) implants are used [146]. The FinFETs are composed of parallel gate fingers, each finger containing an array of parallel fins in order to design devices with appropriate channel width/length ratios. The main device parameters are summarised in Table 6.1 and schematically shown in Figure 6.1. The thermal properties of the n-channel FinFETs are examined at fin widths varying from 12 nm to 82 nm, numbers of fins per finger ranging from 5 to 20 and fin spacings between 228 nm and 528 nm. While one parameter is varied, the others are kept constant at nominal values (marked in bold in Table 6.1).

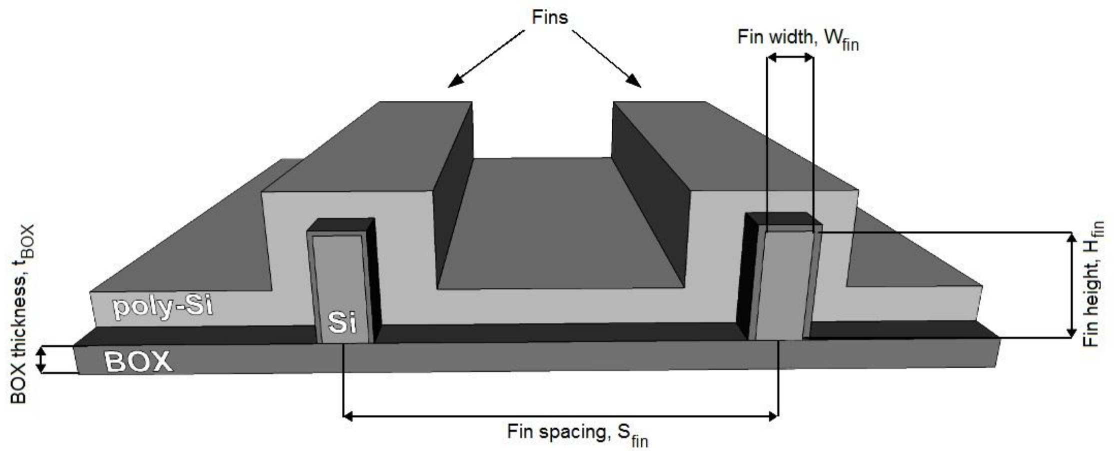

Figure 6.1. FinFET schematic (not to scale) showing one gate finger wrapping two Si fins.

Table 6.1. Main parameters of the FinFETs. Nominal values are in bold characters.

Channel length, L_g	40 nm
Fin width, W_{fin}	12, **22**, 32, 42, 82 nm
Fin height, H_{fin}	60 nm
Fin spacing, S_{fin}	228, 278, **328**, 528 nm
Number of fins per finger, N_{fin}	5, **10**, 15, 20
Number of parallel fingers	48
Buried oxide thickness, t_{BOX}	145 nm
Equivalent gate oxide thickness, t_{ox}	1.8 nm
Source/drain extension length, L_{SD}	100 nm

6.2.2 Methodology

All current-voltage characteristics were obtained with an Agilent 4155C semiconductor parameter analyser and an Agilent B1500A semiconductor device analyser.

In order to obtain the conductance frequency dispersion at moderate frequencies, the small-signal output conductance was measured using an Agilent 4294A precision impedance analyser. Measurements were limited to 10 MHz due to the limitations imposed by the set-up probes and cables and the equipment itself. In order to perform wideband characterisation, scattering (*S*-) parameters were measured from 40 kHz to 4 GHz with a Rohde & Schwarz ZVR vector network

analyser (VNA) and from 40 MHz to 110 GHz with an Agilent 8510XF VNA. *S*-parameters were subsequently de-embedded using dedicated open structures and converted to the elements of admittance matrix (*Y*-parameters) which relate input and output voltages and currents and are complex numbers. The frequency dependence of the real and imaginary parts of the Y_{22} parameter (the ratio between the output current and the output voltage when the transistor input is short-circuited) is analysed in this chapter.

Thermal parameters such as the thermal resistance and the thermal capacitance were extracted using the RF self-heating characterisation technique. The method is described in Section 2.4.2.1 of this thesis.

6.3 Results and discussion

6.3.1 Current-voltage characteristics

The FinFETs were fabricated on a 200 mm wafer and one quarter of it was available for electrical characterisation. In order to choose typical devices for further examination, a large number of devices was initially measured. Figure 6.2 shows transfer characteristics of devices with 12 nm fin width measured at a drain voltage 1.0 V. The devices which did not work were found to be mostly on the edges of the wafer and are not shown.

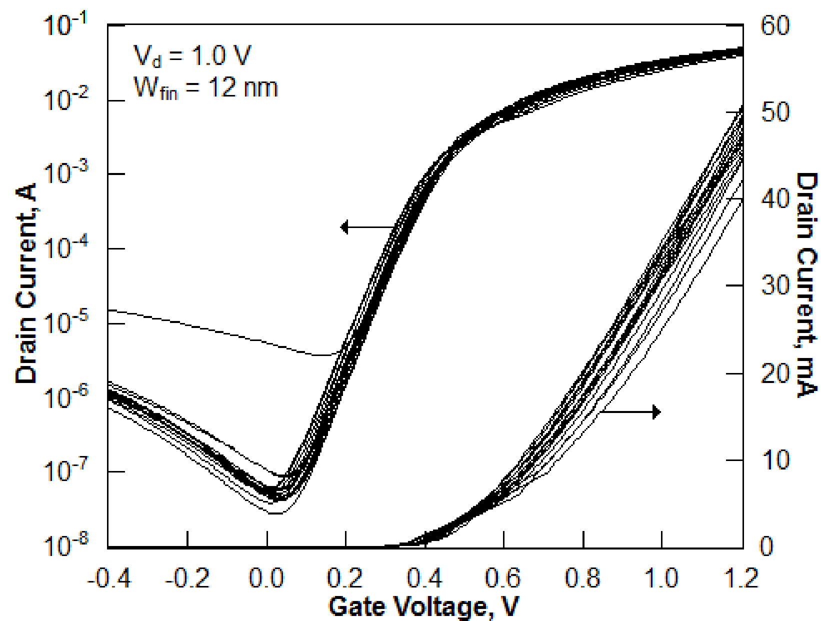

Figure 6.2. Transfer characteristics of FinFETs with 12 nm fin width at $V_d = 1.0$ V.

Figure 6.3 compares the off-state drain current (V_g = 0 V, V_d = 1.0 V) with the on-state drain current (V_g = 1.2 V, V_d = 1.0 V) in FinFETs with fin widths 12, 32, 42 and 82 nm. The yield was lower for FinFETs with 12 nm fin width (~51%) than for devices with wider fins (76-78%). Most probably, this is because in many cases the Si forming the channel of FinFETs was consumed during the fabrication. From Figure 6.3 it can be also seen that the number of reported devices with 82 nm fin width is less than the number of e.g. 32 or 42 nm fin width devices. Due to the larger total gate width in 82 nm fin width devices, the drain current at V_g = 1.2 V, V_d = 1.0 V exceeded the equipment compliance of 100 mA. Figure 6.3 shows that the devices of same geometry are grouped together. An increase of the fin width results in an increase of both off-state and on-state drain currents, as expected (see Equation 1.3).

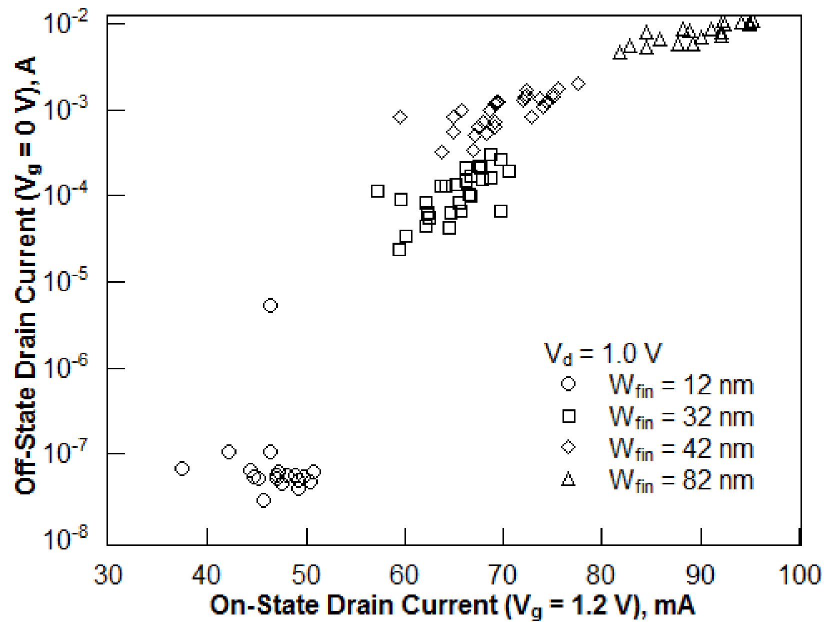

Figure 6.3. Off-state drain current (V_g = 0 V) compared with the on-state drain current (V_g = 1.2 V) in FinFETs with 12, 32, 42 and 82 nm fin widths at V_d = 1.0 V. The shown devices feature S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm.

In Figure 6.4 a box plot representing dispersion of the on-state drain current values in devices with 12, 32, 42 and 82 nm is shown. The on-state current is defined as the drain current at V_g = 1.2 V and V_d = 1.0 V. As expected, an increase of the fin width translates into an increase of the total gate width and, consequently, an increase of the mean drain current (shown with the squares in Figure 6.4) according to Equation 1.3.

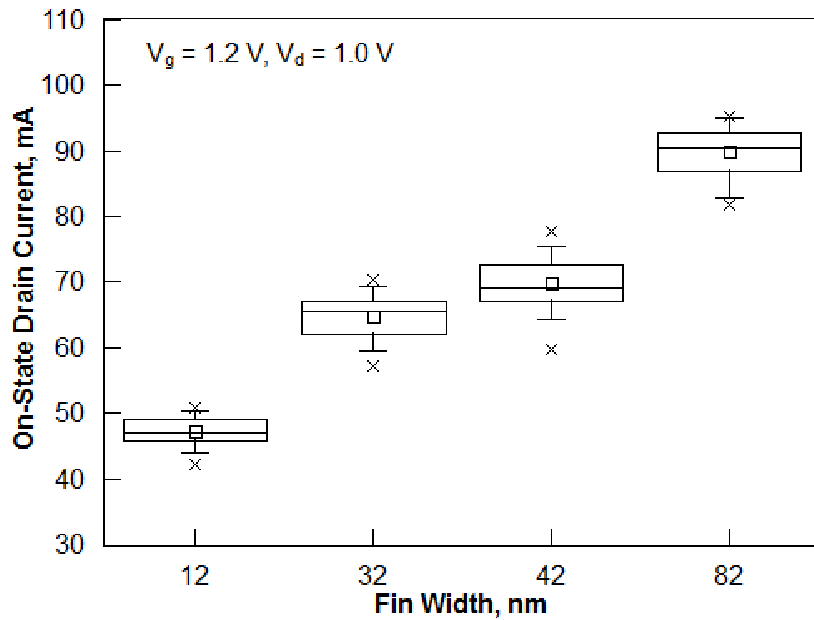

Figure 6.4. Statistical plot of the on-state drain current at V_g = 1.2 V, V_d = 1.0 V in FinFETs with 12, 32, 42 and 82 nm fin widths. The devices shown have S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm. The squares show the mean value. The boxes represent the range in which 25% - 75% of the values occur. The whiskers show the range where 5% - 95% of the values occur. The crosses indicate the minimum and maximum values.

Only FinFETs with typical current-voltage characteristics were considered for further characterisation of self-heating and substrate effects. The results presented in this chapter (e.g. thermal parameters) were obtained from three devices with the median and adjacent characteristics and averaged.

Figure 6.5 shows typical transfer characteristics of the FinFETs chosen for study with a channel length of 40 nm at the drain voltage range from 0.2 V to 1.2 V. The typical output characteristics at gate voltages ranging from 0.4 V to 1.2 V are presented in Figure 6.6. The characteristics are shown for a device with W_{fin} = 22 nm, S_{fin} = 328 nm and N_{fin} = 10 which is a reference device in this work (parameters in bold characters in Table 6.1). These current-voltage characteristics are typical for n-channel FinFETs [71]. For the given device, the threshold voltage is 0.4 V, on-current 475 $\mu A \cdot \mu m^{-1}$ at V_g = 1.0 V, V_d = 1.0 V and off-current 200 $nA \cdot \mu m^{-1}$ at V_g = 0 V and V_d = 1.0 V.

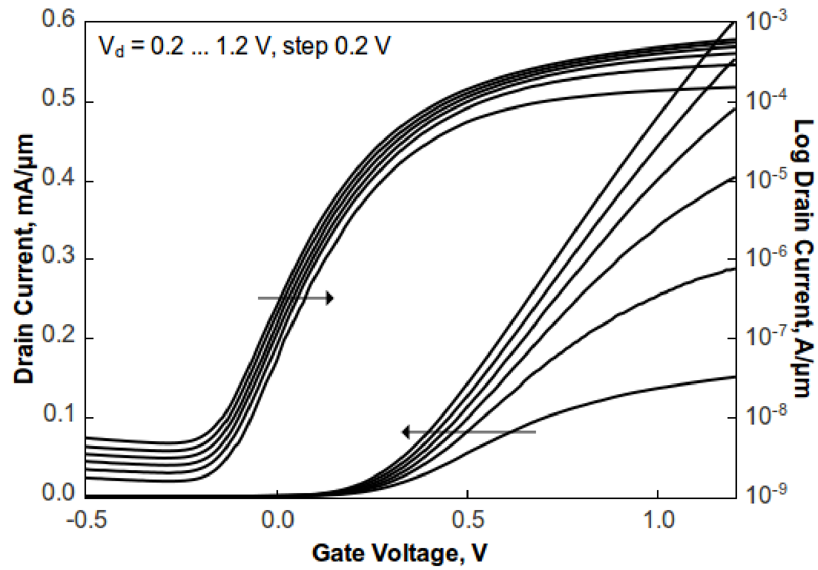

Figure 6.5. Transfer characteristics of the FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm at a drain voltage ranging from 0.2 V to 1.2 V.

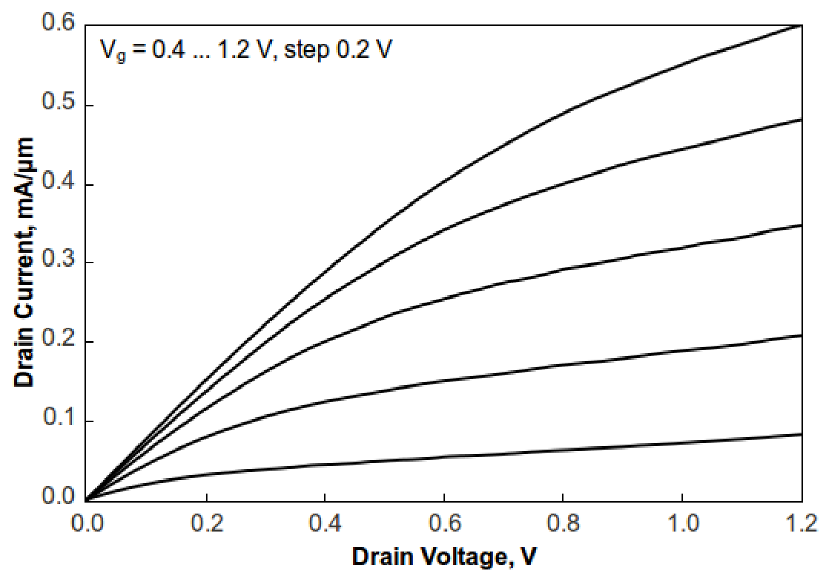

Figure 6.6. Output characteristics of the FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm at a gate voltage ranging from 0.4 V to 1.2 V.

6.3.2 Self-heating in FinFETs

In order to extract thermal resistances and capacitances, the dependence of the drain current on the ambient temperature $\partial I_d/\partial T_A$ must be measured as it was shown in Section 2.4.2.2.2. It is obtained from the linear fit of the hot chuck current measurements as shown in Figure 6.7 for FinFETs with the number of parallel fins per finger ranging from 5 to 20. The measurements

were performed in the region of the expected temperature rise in the channel which is from the room temperature to 65 °C. As these measurements are based on the linear fit of a limited number of data points, they are the main source of inaccuracy for the extraction of the device thermal properties.

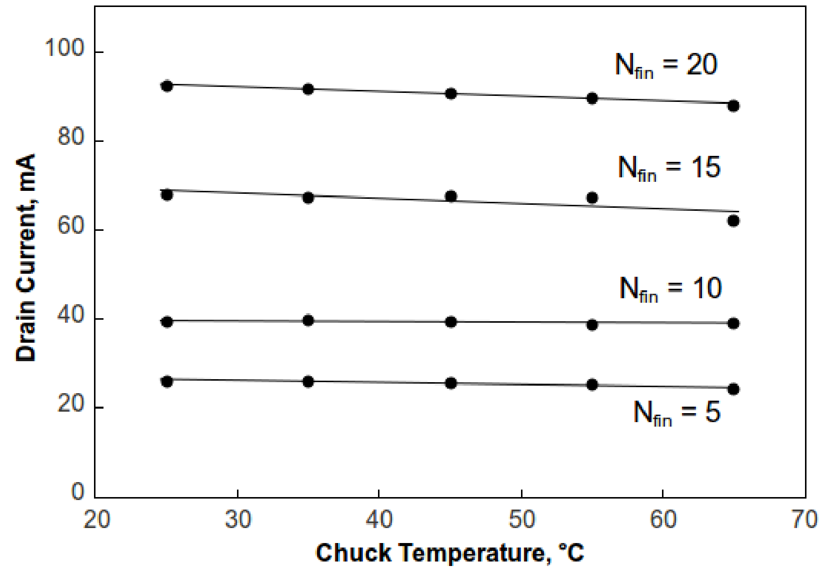

Figure 6.7. The drain current dependence on the chuck temperature in FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 1.0 V.

Figure 6.8 shows a typical output conductance frequency response extracted over a wide frequency band, from 100 Hz up to 110 GHz, using the different instruments. The slight mismatch of some characteristics where frequency bands of the different instruments overlap is due to minor differences in biasing conditions. The output conductance variation over the wide frequency range in short channel SOI MOSFETs is due to different factors: self-heating, substrate-related effects and gate resistance. The first transition occurs at low frequencies (1-100 Hz) and is due to the relaxation of the minority carriers in the Si substrate [103], [106]. In FinFETs this effect is relatively small compared with the other transitions [44] and it is not observed in Figure 6.8. The output conductance transition due to self-heating is observed at MHz frequencies. Inertia of the majority carriers in the substrate causes the output conduction variation at frequencies of a few hundred MHz for a standard resistivity SOI substrate (~20 Ω·cm) [103], [106]. Finally, the gate resistance results in an output conductance rise in the GHz range. To characterise self-heating, knowledge of the isothermal characteristics is required. Therefore, it is imperative to choose a frequency at which dynamic self-heating is removed while the output conductance is affected neither by substrate-related effects nor by the gate resistance. Small-signal AC conductance (dashed line in Figure 6.8) measured with the 4294A up to 10

MHz does not reach isothermal values where self-heating is removed. This is evidenced as the plateau at high frequencies is not observed.

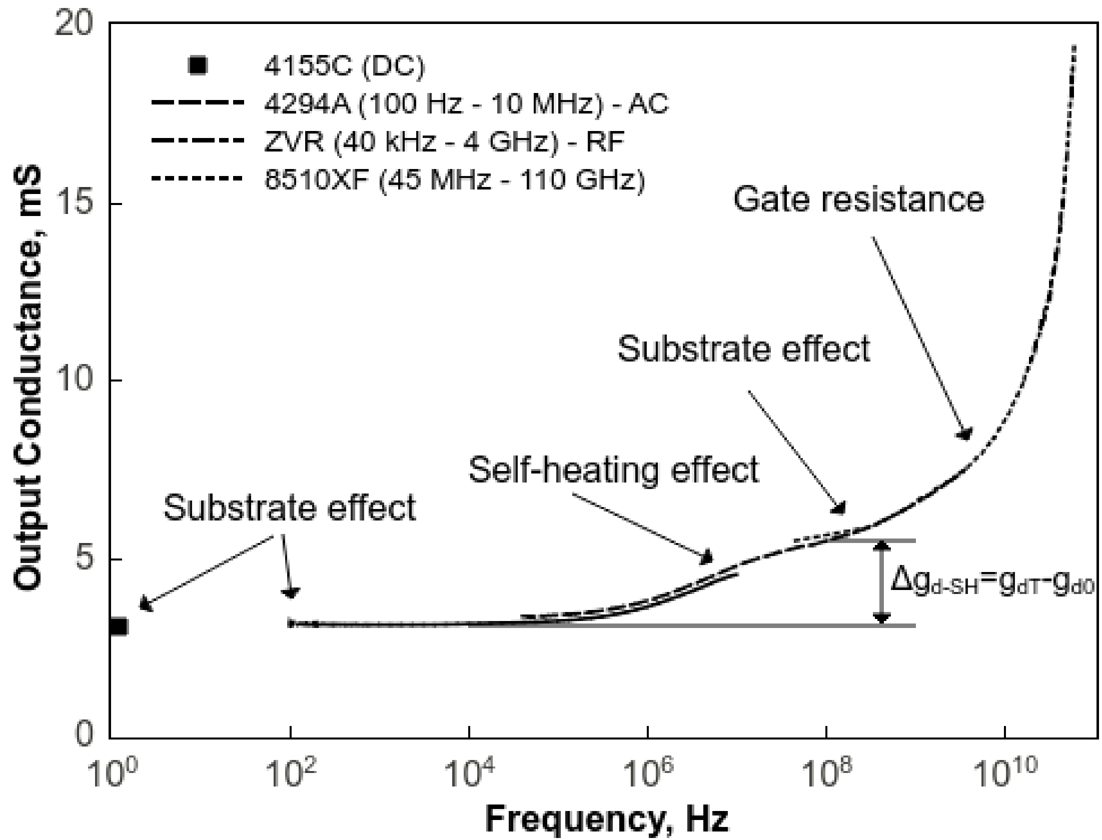

Figure 6.8. Variation in output conductance with frequency measured using different instruments in FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm, N_{fin} = 5 and L_g = 40 nm at V_g = 1.2 V and V_d = 1.0 V.

Figure 6.9 compares the conductance difference at high and low frequencies, $\Delta g_{d\text{-}SH}$, in devices with different fin widths obtained from AC (100 Hz – 10 MHz) and RF (40 kHz – 100 MHz) measurements. The output conductance transition measured by the RF technique is ~40% higher than the output conductance transition measured with the AC technique. As the thermal resistance (*Re(Z_{th})*) is directly proportional to $\Delta g_{d\text{-}SH}$ according to Equation 2.15 in Section 2.4.2.1, underestimation of $\Delta g_{d\text{-}SH}$ may lead to erroneous values of the thermal resistance. This in turn may lead to underestimation of self-heating. Therefore, the measurement frequency has to be extended above 10 MHz into the GHz range for state of the art FinFETs. This also applies to UTBB devices as it was shown in Chapter 5.

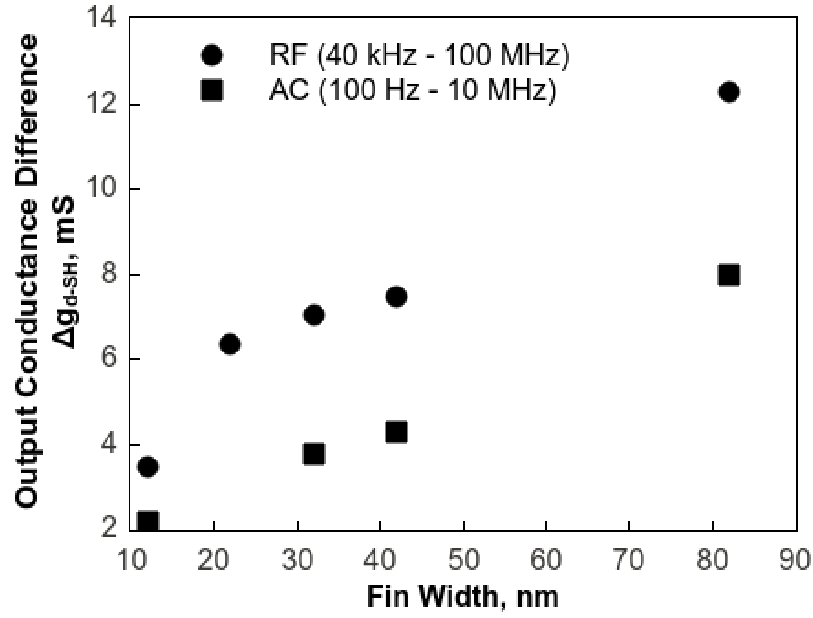

Figure 6.9. The conductance difference at high and low frequencies obtained from AC (100 Hz – 10 MHz) and RF (40 kHz – 100 MHz) measurement setups for the same devices with fin widths from 12 nm to 82 nm.

Scaling and major increase of surface-to-volume ratio in advanced non-planar semiconductor devices result in surface effects playing a more important role. Jin *et al.* studied planar devices and observed no change in the time constant at different effective widths as thermal resistance and capacitance have inverse dependencies on effective width [94]. However, in the case of FinFETs, there is a reduction of the fin width, and consequently the effective width, which results in a higher surface-to-volume ratio. This leads to different effects on thermal resistance (associated with the device surface) and thermal capacitance (associated with the Si volume). This results in a decrease of the thermal time constant with a reduction of the fin width. Figure 6.10 shows thermal time constants in devices with fin widths from 12 nm to 82 nm. The extraction method was described and discussed in Chapter 2 and in [94]. Empirically, the thermal time constant is obtained from the frequency where the output conductance reaches $g_{d0} + (g_{dT} - g_{d0})/3$ as it was described in Section 2.4.2.2.4. The thermal time constant is around 80 ns for the narrowest fins (12 nm). Therefore, extraction of thermal properties must be performed well above 10 MHz (see Equation 2.21) where FinFET characteristics are isothermal. All the following experimental results are then extracted using the Rohde & Schwarz ZVR VNA from 40 kHz to 100 MHz.

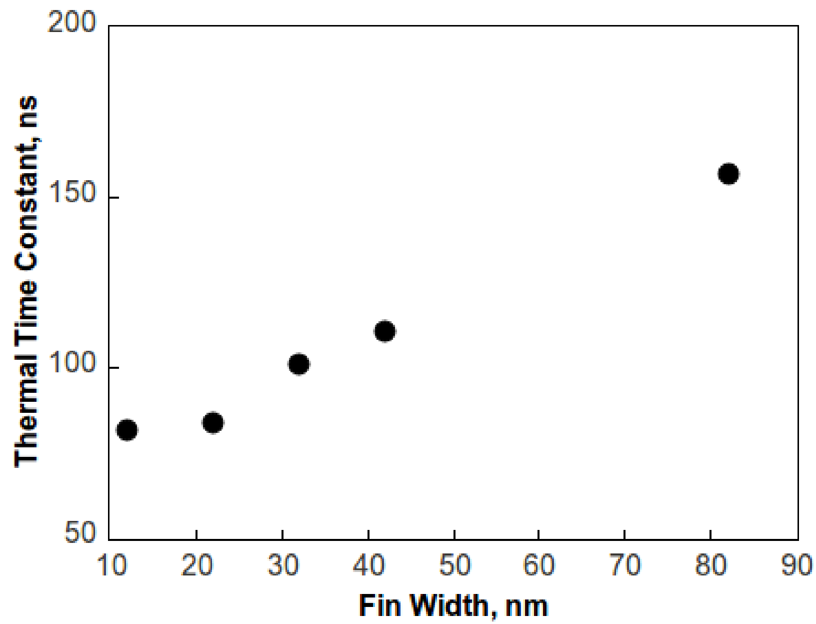

Figure 6.10. Thermal time constants in FinFETs with fin widths from 12 nm to 82 nm extracted using the empirical method from [94].

The output conductance frequency response due to self-heating is strongly dependent on the bias conditions. Figure 6.11 shows the output conductance variation with frequency from 40 kHz to 4 GHz at different gate and drain voltages in the devices with W_{fin} = 22 nm, S_{fin} = 328 nm and N_{fin} = 5 measured with ZVR VNA. At lower power levels (V_g = V_d = 0.5 V) self-heating is almost negligible, therefore the observed conductance variation is only due to the gate resistance. Further thermal analysis is carried out based on the assumption that at 100 MHz the conductance plateau is observed where dynamic self-heating is removed and neither the substrate-related effects nor the gate resistance are present which can be detected from the increase of conductance at higher frequencies.

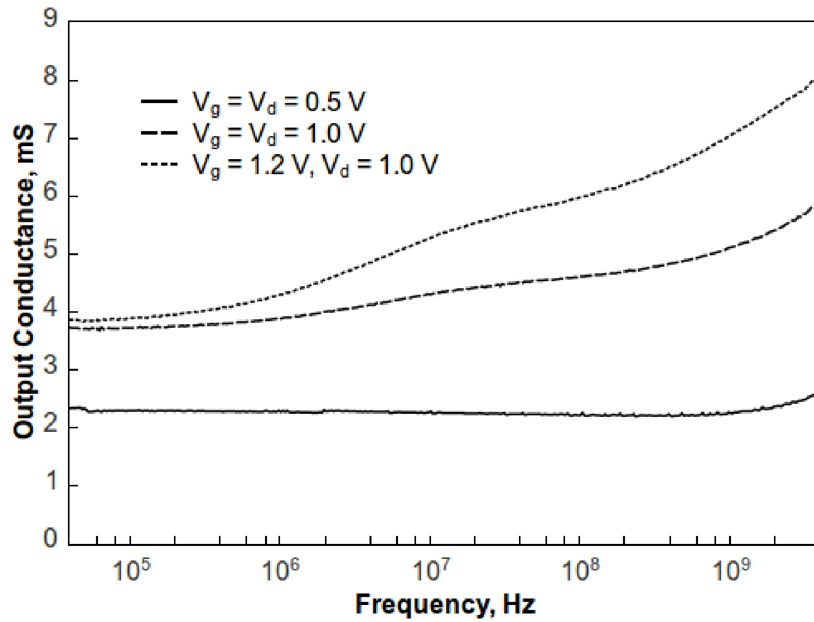

Figure 6.11. Variation in output conductance with frequency at different biasing conditions in FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm, N_{fin} = 5 and L_g = 40 nm.

In order to obtain the thermal capacitance according to Equations 2.17 and 2.18, the total drain capacitance must be extracted from the imaginary part of the of the Y_{22} parameter. Figure 6.12 shows the change of the total drain capacitance over a few orders of magnitude as frequency increases from 100 kHz to 4 GHz. The total drain capacitance is sensitive to biasing conditions, which is an indication of self-heating.

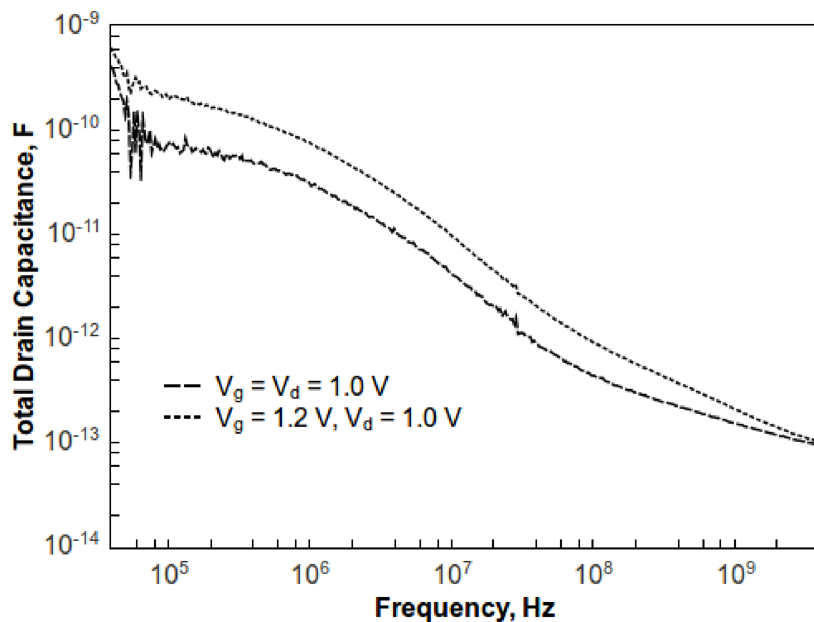

Figure 6.12. Total drain capacitance variation with frequency at V_g = 1.0 V and V_g = 1.2 V, V_d = 1.0 V in FinFETs with W_{fin} = 22 nm, S_{fin} = 328 nm, N_{fin} = 5 and L_g = 40 nm.

6.3.3 Impact of FinFET geometry on self-heating

In order to investigate the impact of FinFET geometry on self-heating, the output conductance and the total drain capacitance values were measured in FinFETs with different fin widths, numbers of parallel fins and fin spacings.

6.3.3.1 Fin width

Figure 6.13 shows the variation of the extracted thermal resistance with the fin width. Increased phonon boundary scattering and confinement result in higher thermal resistance as fin width is reduced. The observed trend agrees with the simulation results presented in [49] where 50 nm gate length FinFETs with fin widths from 10 nm to 50 nm and 100 nm thick BOX were modelled. This trend suggests that improved electrostatic control and higher integration density achieved through reduced fin width are compromised by increased thermal resistance.

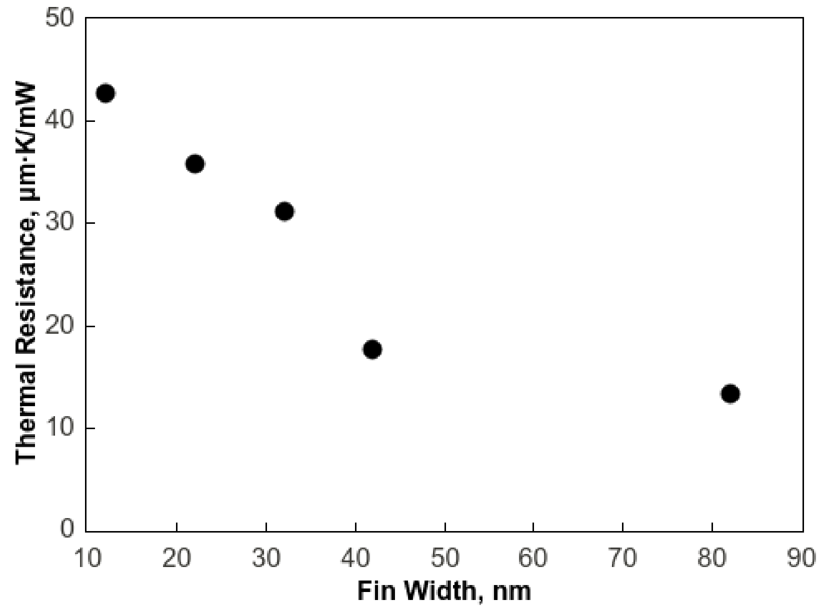

Figure 6.13. Thermal resistance in the devices with varying fin widths, S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm.

The thermal capacitance in devices with the fin width from 12 nm to 82 nm is shown in Figure 6.14. The ability to store heat is related to the Si volume and thus the effective width of the device fins. Therefore, a larger thermal capacitance is observed in devices with larger fins.

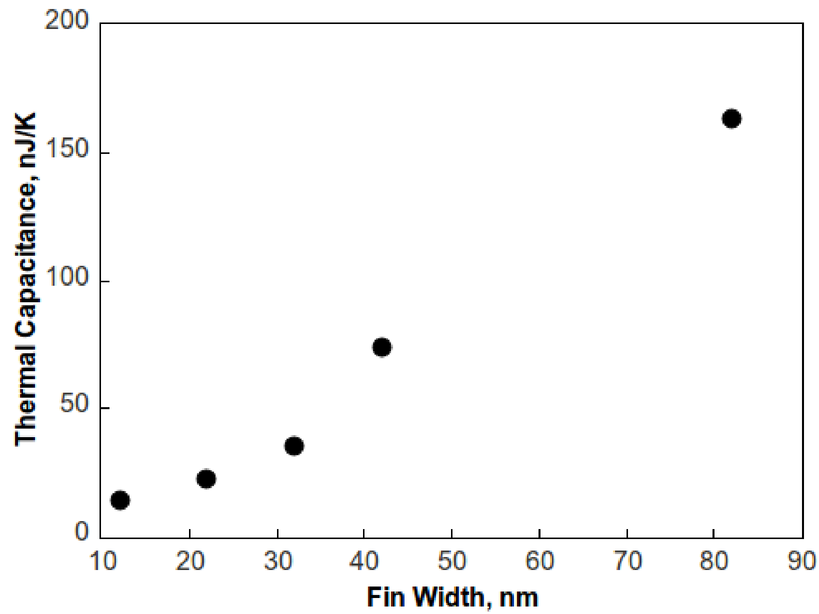

Figure 6.14. The thermal capacitance in the devices with varying fin widths, S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm.

6.3.3.2 Number of parallel fins

In Figure 6.15 the thermal resistance variation with the number of fins per gate finger is shown. Due to the higher temperature gradient in the devices with fewer fins the thermal resistance increases as the number of fins per gate finger reduces. The trend agrees with the results of the simulations carried out by Molzer *et al.* [48]. A higher number of parallel fins results in improved thermal characteristics but introduces some challenges in chip design as larger area structures have to be arranged on the surface area of the chip.

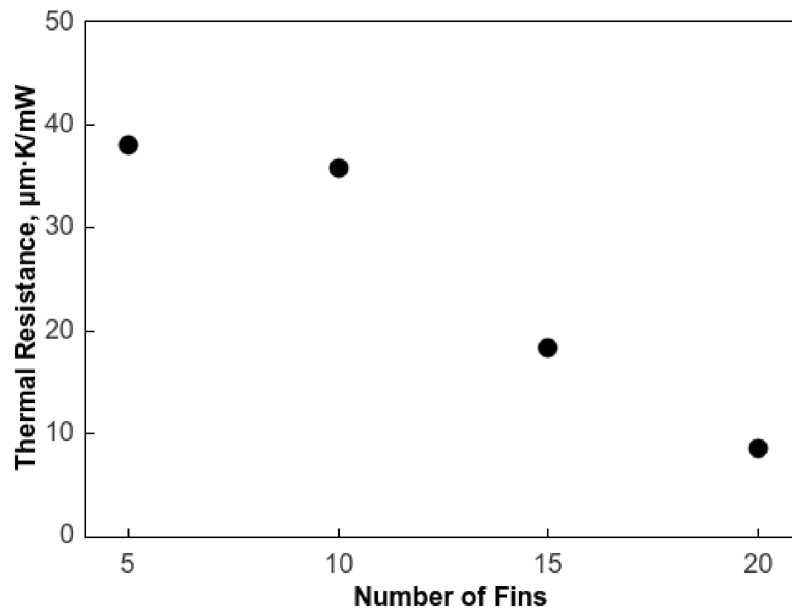

Figure 6.15. Variation of the thermal resistance in the devices with different numbers of parallel fins per gate finger, W_{fin} = 22 nm, S_{fin} = 328 nm and L_g = 40 nm.

In Figure 6.16 variation in the thermal capacitance with the number of fins per gate finger is presented. Again, greater thermal capacitance in devices with more parallel fins is due to the bigger Si volume available for heat storage.

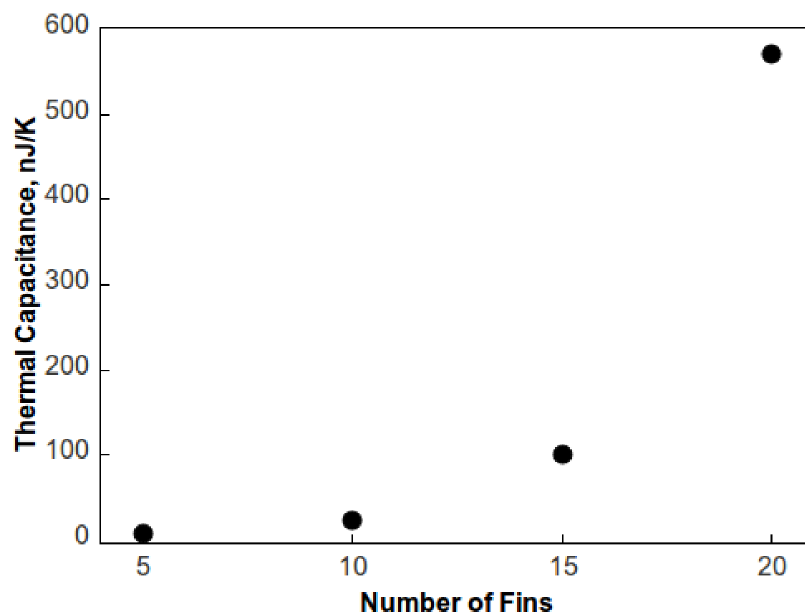

Figure 6.16. Variation of the thermal capacitance in the devices with 5, 10, 15 and 20 parallel fins per gate finger, W_{fin} = 22 nm, S_{fin} = 328 nm and L_g = 40 nm.

6.3.3.3 Fin spacing

As seen from Figure 6.17, a reduction of the fin spacing also leads to an increase of the thermal resistance. This is due to enlarged thermal crosstalk between adjacent fins [50] and poorer heat dissipation. The same trend was observed in simulations by Braccioli *et al.* in [50] where 30 nm gate length FinFETs with 10 nm wide fins on 50 nm BOX were modelled. A weaker dependence of the thermal resistance on fin spacing can be used to improve the integration density without a severe impact on thermal properties.

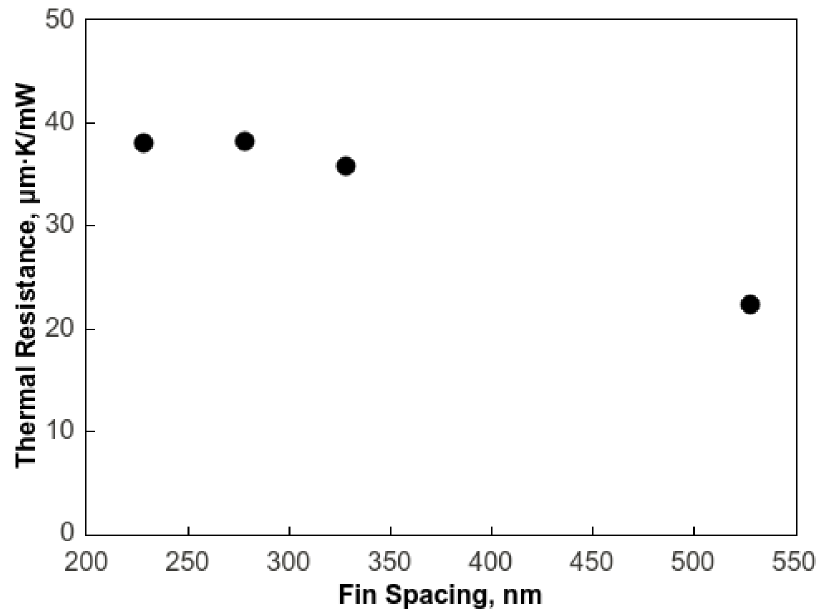

Figure 6.17. Thermal resistance variation with fin spacing extracted in FinFETs with W_{fin} = 22 nm, N_{fin} = 10 and L_g = 40 nm.

For all parameters studied, device thermal resistance shows the strongest dependence on the number of fins and the fin width compared with the fin spacing. This agrees with the simulation results in [50] where it was concluded that the fin spacing is not a critical parameter from a thermal perspective.

6.3.3.4 Temperature rise due to self-heating

The temperature rise is a product of the thermal resistance, the drain current and the drain voltage. Figure 6.18 presents the temperature rise in the device active region above ambient (fixed at 300 K) for different fin widths. The temperature rise in the FinFETs with different numbers of parallel fins is shown in Figure 6.19. The temperature rise is obtained at a constant power of 50 mW which corresponds to the typical power levels in the devices in saturation. The

temperature is smaller in the devices with wider fins and a higher number of parallel fins due to the reduced thermal resistance as expected. Channel temperatures observed in this experiment fit well into the range of temperatures simulated by Kolluri *et al.* in 50 nm gate length FinFETs of various geometries on 100 nm thick BOX [49]. The agreement between the experimental and modelling results suggests reliability of both measurements and simulations.

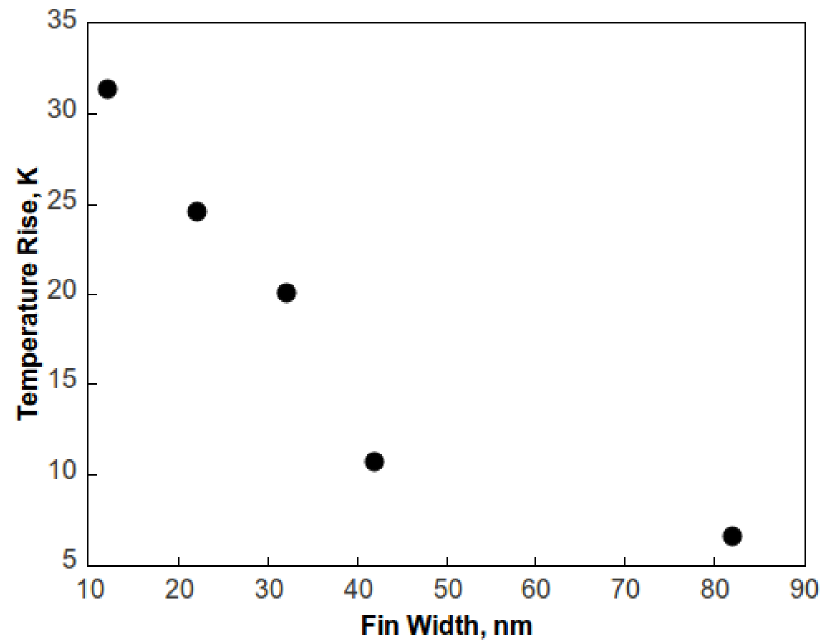

Figure 6.18. The temperature rise above ambient in the channel of devices with varying fin widths, S_{fin} = 328 nm, N_{fin} = 10 and L_g = 40 nm at 50 mW power.

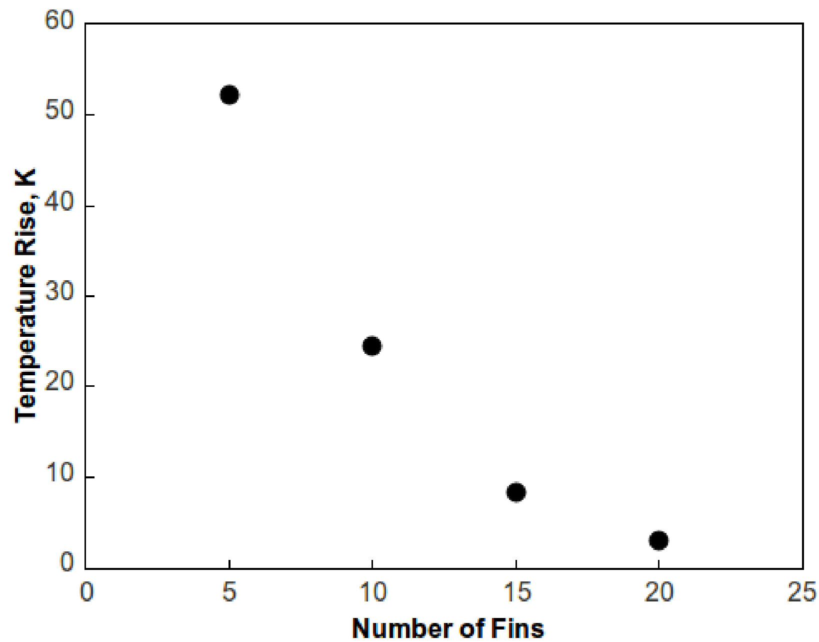

Figure 6.19. The temperature rise above ambient in the channel of devices with varying numbers of fins, W_{fin} = 22 nm, S_{fin} = 328 nm and L_g = 40 nm at 50 mW power.

6.3.4 Substrate effects

6.3.4.1 Frequency range

In the high frequency region (hundreds MHz – GHz), the output conductance is governed by the source and drain coupling through the substrate and the gate resistance (see Figure 6.8). These two effects may overlap obscuring transition frequencies (inflection points). In order to evaluate the impact of the substrate effects, the frequency range has to be chosen carefully. This is particularly important for multi-finger devices as the total effective width is high and therefore the impact of the parasitic gate resistance is significant.

In order to confirm the frequency range where the substrate effects are pronounced in the output conductance frequency response, the output conductance in the high frequency region was corrected for the extrinsic series resistance. In order to obtain the series resistance-free output conductance curve, "cold" *S*-parameters were measured at V_g = 1.0 V and V_d = 0. This procedure enables correction for extrinsic source, drain and gate resistance impact on the output conductance frequency response. The correction method described in [147] was implemented. In Figure 6.20 the output conductance variation at high frequency is shown with and without the parasitic resistance correction. It can be seen from Figure 6.20 that up to ~3 GHz parasitic resistances do not significantly affect the output conductance. And above 3 GHz the two curves

deviate significantly. The transition seen above 3 GHz is attributed to the gate resistance. As the parasitic resistance is removed, this transition is considerably reduced, though it is still visible owing to the imperfect correction for parasitic resistance.

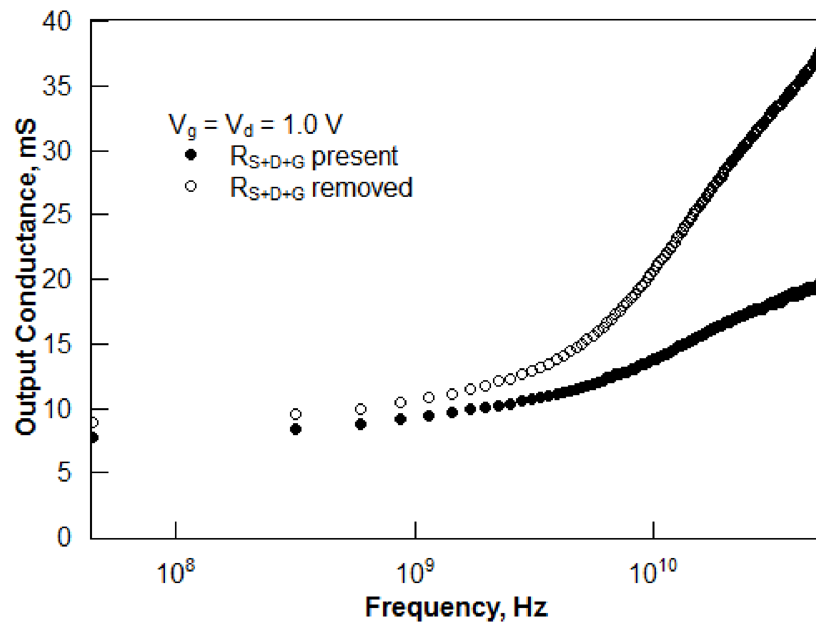

Figure 6.20. Output conductance variation with frequency with and without correction for parasitic series resistance in FinFETs with W_{fin} = 22 nm, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 1.0 V.

Another way to confirm the high frequency range where the gate resistance is pronounced is to observe the output conductance with other mechanisms affecting the output conductance being suppressed. This can be achieved by choosing appropriate bias conditions. At low gate and drain voltages substrate effects as well as self-heating are suppressed but the gate resistance is still expected to impact the output conductance curve at high frequencies. Figure 6.21 shows the output conductance variation with frequency at $V_g = V_d$ = 0.5 V in devices with various fin widths. As can be seen from Figure 6.21, the curves are nearly flat in the entire frequency region below ~1 GHz. This agrees with the results presented in Figure 6.20. Comparison of the output conductance characteristics at various bias conditions is also shown in Figure 6.11.

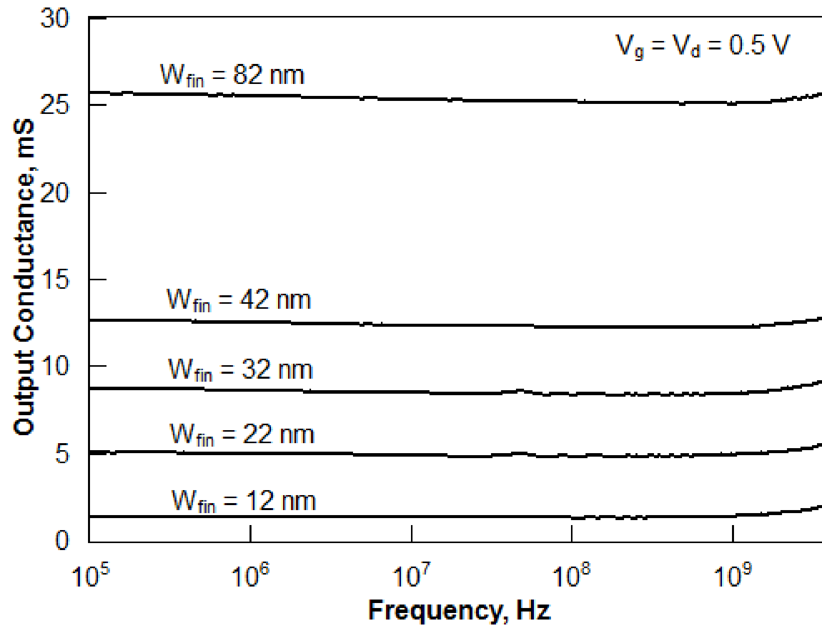

Figure 6.21. Output conductance variation with frequency in devices with different fin widths, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 0.5 V showing the gate resistance transition above 1 GHz with other transitions being suppressed.

6.3.4.2 Impact of substrate effects on output conductance

In order to evaluate the impact of the substrate effects on the output conductance in the high frequency region (see Figure 6.8), the amplitude of the output conductance transition is extracted in devices with various fin widths. The amplitude of the output conductance transition caused by the substrate effects is proportional to the transconductance and depends on the substrate capacitance which is a function of frequency [44]:

$$\Delta g_{d-SUB} = (n-1)g_m \frac{C_{BGD}}{C_{BGD} + C_{SBG} + C_{GBG} + C_{Sub}}, \tag{6.1}$$

where $\Delta g_{d\text{-}SUB}$ is the amplitude of the output conductance transition due to substrate effects, g_m is the transconductance, n is the body factor, C_{Sub} is the frequency dependent substrate capacitance and C_{BGD}, C_{SBG}, C_{GBG} are the drain-to-back-gate, source-to-back-gate capacitance and front-gate-to-back-gate capacitances, respectively. The back gate is equivalent to the interface between the substrate and BOX. At high frequencies the substrate acts as dielectric and the substrate capacitance approaches value which can be estimated from the equation of a parallel plate capacitor [103]:

$$C_{Sub} = \frac{\varepsilon_0 \varepsilon_{Si}}{t_{Sub}}, \quad (6.2)$$

where t_{Sub} is the thickness of the substrate, ε_0 is the vacuum permittivity and ε_{Si} is the relative permittivity of Si. The transconductance and the substrate capacitance dependencies on frequency translate into the output conductance variation with frequency.

In [44] it was shown that low frequency output conductance transition caused by substrate effect reduces with the fin width. In effect, in 70 nm wide fin devices the output conductance was found to be constant in the frequency range up to 10 kHz. However, impact of substrate effects at high frequency was not experimentally investigated. In this work the amplitude of the high frequency transition is analysed. The amplitude of the output conductance transition caused by substrate effect was extracted from the output conductance values at 100 MHz and 1 GHz at V_g = 1.2 V and V_d = 1.0 V. Figure 6.22 shows a decrease of normalised $\Delta g_{d\text{-}SUB}$ in devices with narrower fins. According to Equation 6.1 $\Delta g_{d\text{-}SUB}$ depends on the transconductance and the substrate capacitance. The transconductance is proportional to the effective fin width, i.e. $2H_{fin} + W_{fin}$, while the substrate capacitance is proportional to the fin width only. Therefore, in Figure 6.22 $\Delta g_{d\text{-}SUB}$ is normalised to $(2H_{fin} + W_{fin})/W_{fin}$. The data confirm that substrate effects decrease with decreasing fin width. This suggests that narrow fins can be beneficial for analogue applications where frequency dependent behaviour is undesirable.

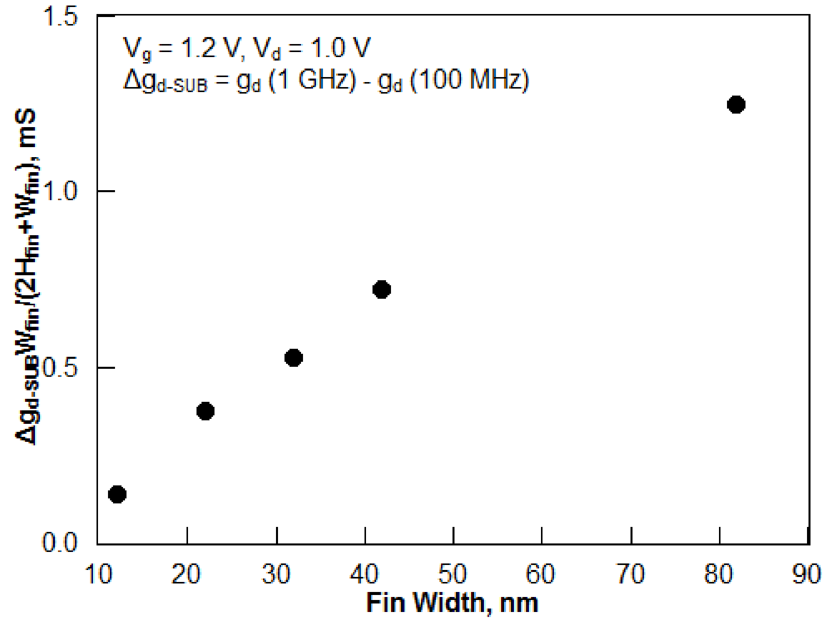

Figure 6.22. Variation in normalised amplitude of the substrate-related output conductance transition with the fin width in FinFETs with N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm. $\Delta g_{d\text{-}SUB}$

was extracted from the values of the output conductance at 100 MHz and 1 GHz at $V_g = 1.2$ V and $V_d = 1.0$ V.

6.3.4.3 Body factor and shielding distance

Due to channel wrapping and improved control of the charge in the channel from the gate, the body factor (or body effect coefficient) approaches ideal value of 1 as the fin width reduces [134]. This results in the suppression of the substrate-related output conductance transition according to Equation 6.1. Therefore, the reduction of normalised $\Delta g_{d\text{-}SUB}$ is caused by the body factor dependence on the fin width. The body factor indicates the front gate threshold voltage dependence on the potential at the back interface [134], [148]. It can be expressed in terms of the front gate to channel and channel to ground capacitances. Therefore, the body factor is determined by device geometry. Knowing device dimensions, the body factor can be estimated using an approach presented in [134]. However, the model in [134] was developed for FinFETs with square cross-sections, i.e. the fin width is equal to the fin height. In this work the model is generalised in order to be applied for FinFETs with different fin height and fin width. The model is based on the capacitance equivalent circuit which is shown in Figure 6.23.

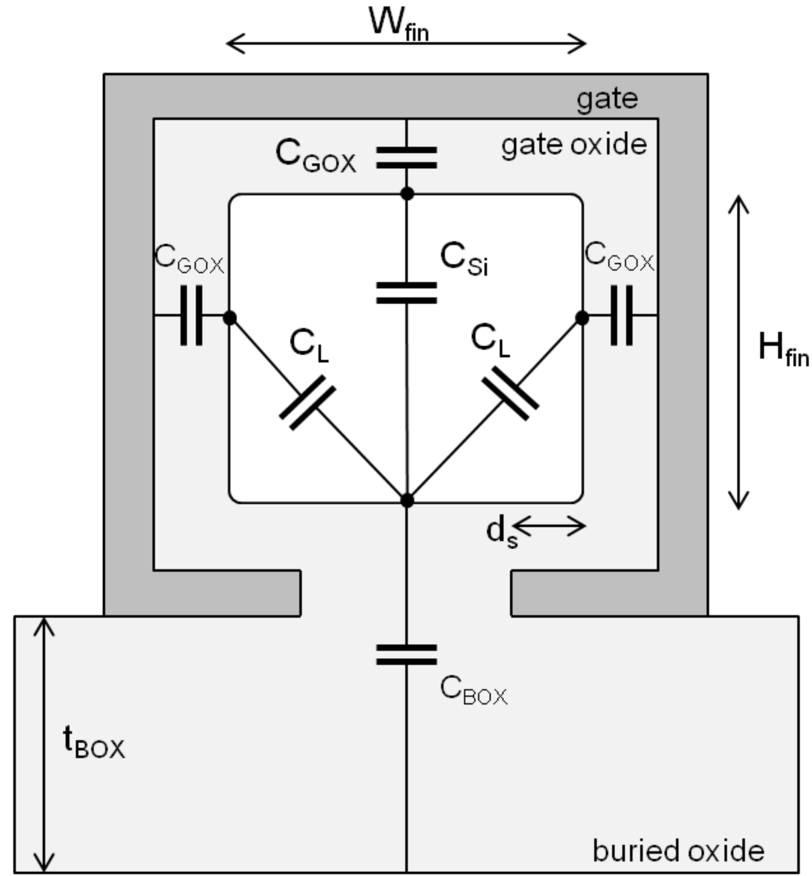

Figure 6.23. Schematic FinFET cross-section, not to scale. Capacitances used for the body factor calculation are shown. Adapted from [134].

From the capacitance equivalent circuit the body factor can be estimated as follows:

$$n = 1 + \frac{C_{CH-GND}}{C_{G-CH}} = 1 + \frac{C_{BOX}(C_{Si} + 2C_L)}{(C_{BOX} + C_{Si} + 2C_L)\left(C_{GOX} + 2\frac{H_{fin}}{W_{fin}}C_{GOX}\right)}, \quad (6.3)$$

where $C_{CH\text{-}GND}$ is the channel to ground capacitance, $C_{G\text{-}CH}$ is the gate to channel capacitance. The other variables are as follows:

$$C_{GOX} = \frac{\varepsilon_{SiO2}}{t_{ox}}, \quad (6.4)$$

$$C_{Si} = \frac{\varepsilon_{Si}}{H_{fin}}, \quad (6.5)$$

$$C_L = \frac{C_{Si}}{\pi}\ln\left(\frac{W_{fin}}{r}\right), \quad (6.6)$$

$$C_{BOX} = \frac{\varepsilon_{SiO2}}{t_{BOX}} \left(\frac{W_{fin} - 2d_s}{W_{fin}} \right), \tag{6.7}$$

where ε_{SiO2} and ε_{Si} is the relative permittivity of SiO_2 and Si, respectively, d_s is the shielding distance and r is the fin corner curvature. The shielding distance indicates how far the gate extends under the fin. Large shielding distance is an indication of the omega-like fin cross-section.

Figure 6.24 shows the calculated body factor variation with fin width for three different values of the shielding distance (0, 3 and 6 nm). The other device dimensions were taken from Table 6.1. The fin corner curvature is assumed to be 1 nm in this work and it was observed that it is not a critical parameter. In all cases the variation of the body factor with the fin width is considerable which explains the variation of normalised $\Delta g_{d\text{-}SUB}$ (Figure 6.22). The body factor affects substrate effects through the term $(n-1)$ according to Equation 6.1. Results shown in Figure 6.24 confirm that $(n-1)$ can change ~5 times as the fin width reduces from 82 nm to 12 nm when the shielding distance is 0 nm. In the case of a larger shielding distance the difference is larger. In Figure 6.22 normalised $\Delta g_{d\text{-}SUB}$ changes ~9 times. Therefore, it can be estimated that the shielding distance in these devices is ~3 nm. A more precise value of the shielding distance can be confirmed by transmission or scanning electron microscopy (TEM, SEM) after a focused ion beam cut. The obtained value of the shielding distance (3 nm) is in a reasonable agreement with typical TEM FinFET cross-sections reported in literature. In [149–151] TEM images show the shielding distance is a few nm in FinFETs with fin widths of ~10 nm.

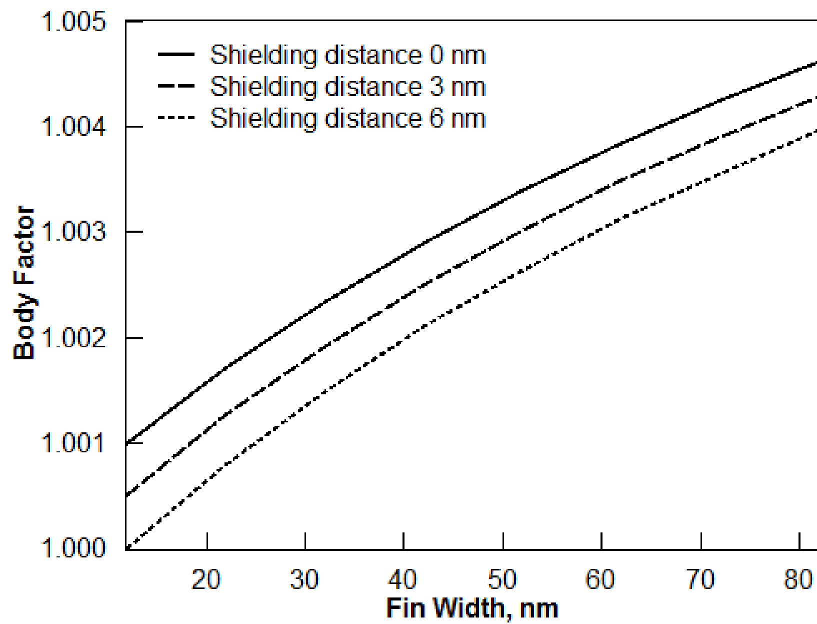

Figure 6.24. Calculated body factor variation with the fin width with three different shielding distances.

6.3.5 Self-heating and substrate effect contribution to output conductance variation

In order to understand the relative contribution of self-heating and substrate effects to the output conductance degradation, frequency response of devices with the widest and the narrowest available fins is shown in Figure 6.25. $\Delta g_{d\text{-}SUB}$ is only ~20-30% of the total g_d variation in the 100 kHz – 1 GHz range in devices with the fin width between 12 nm and 82 nm. The output conductance transition due to self-heating which occurs between 100 kHz and 100 MHz is the main source of the output conductance variation (~70-80%). Therefore, the frequency-dependent behaviour of FinFETs can be further improved by optimisation of thermal properties, for example by optimising device geometry (Section 6.3.3), source and drain engineering as discussed in [50], [81], [100], BOX thinning as described in [49], [50] and in Chapter 5 or implementing bulk FinFETs [54], [55]. However, BOX thinning might introduce additional uniformity issues and bulk FinFET technology suffers from high parasitic leakage currents, complex fabrication process and lower circuit speed [54], [57]. Lowering operating voltage is expected to reduce both substrate and self-heating related output conductance transitions and thus improve device performance over the wide frequency range.

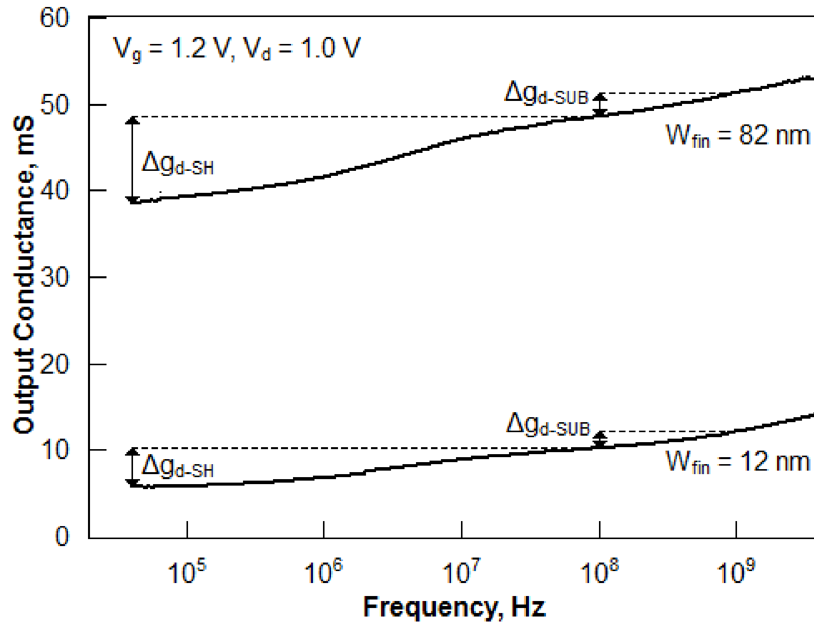

Figure 6.25. Variation in output conductance with frequency in devices with the widest (82 nm) and the narrowest (12 nm) available fins, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at V_g = 1.2 V and V_d = 1.0 V.

6.3.6 Intrinsic voltage gain

The intrinsic voltage gain is an important analogue figure of merit as it indicates the efficiency of the conversion from the input voltage to the output voltage. The intrinsic gain in the studied FinFETs is expressed in dB and was extracted from:

$$A_v = 20\log\frac{V_d}{V_g} = 20\log\frac{g_m}{g_d}, \tag{6.8}$$

where A_v is the intrinsic voltage gain, g_d is the output conductance and g_m is the transconductance.

Figure 6.26 shows the gain variation with frequency in devices with fin widths from 12 nm to 82 nm at $V_g = V_d$ = 1.0 V. As expected [76], [152], improvement of the intrinsic gain is observed in devices with narrower fins. This is caused by the volume inversion and improved control of the charge in the channel from the gate. As seen from Figure 6.26 the intrinsic gain degrades with frequency. This is due to the output conductance increase with increasing frequency as shown e.g. in Figure 6.25. However, according to Equation 6.8 the gain also depends on the transconductance. The transconductance increases with frequency as it is shown in Figure 6.27 for devices with different fin widths at $V_g = V_d$ = 1.0 V. The transconductance variation in the

given frequency range is lower than that of the output conductance, therefore the reduction of the gain at higher frequencies is observed. The oscillations in the high frequency range in Figure 6.26, Figure 6.27 and Figure 6.28 are most probably related to the equipment induced noise during the transconductance measurements.

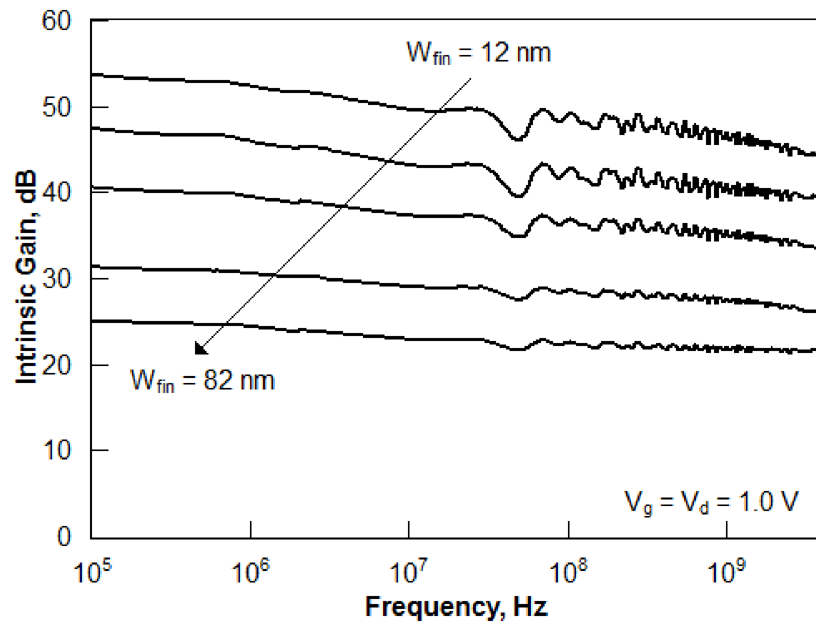

Figure 6.26. Intrinsic gain variation with frequency in devices with different fin widths, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 1.0 V.

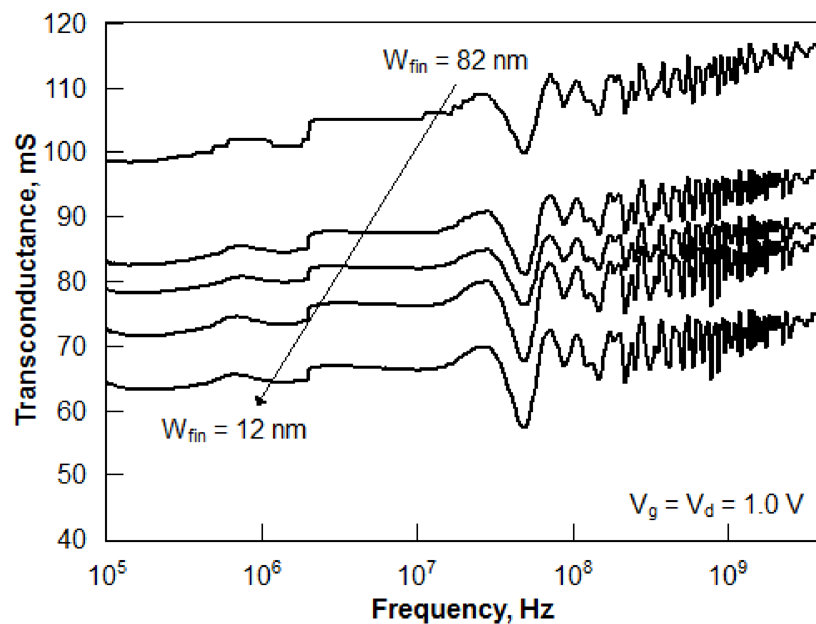

Figure 6.27. Variation of the transconductance with frequency in devices with different fin widths, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 1.0 V.

Figure 6.28 shows the relative variation of the intrinsic gain with respect to its value at 100 kHz. The intrinsic gain reduces by about 20% at 3 GHz from its value at 100 kHz. Its change is nearly independent of the fin width. This arises because self-heating is the dominant effect in the given frequency range and affects both the output conductance and the transconductance. The intrinsic gain is proportional to the transconductance and inversely proportional to the output conductance, as in Equation 6.8. Therefore, self-heating dependence on the fin width to some extent cancels out in the intrinsic gain variation with frequency.

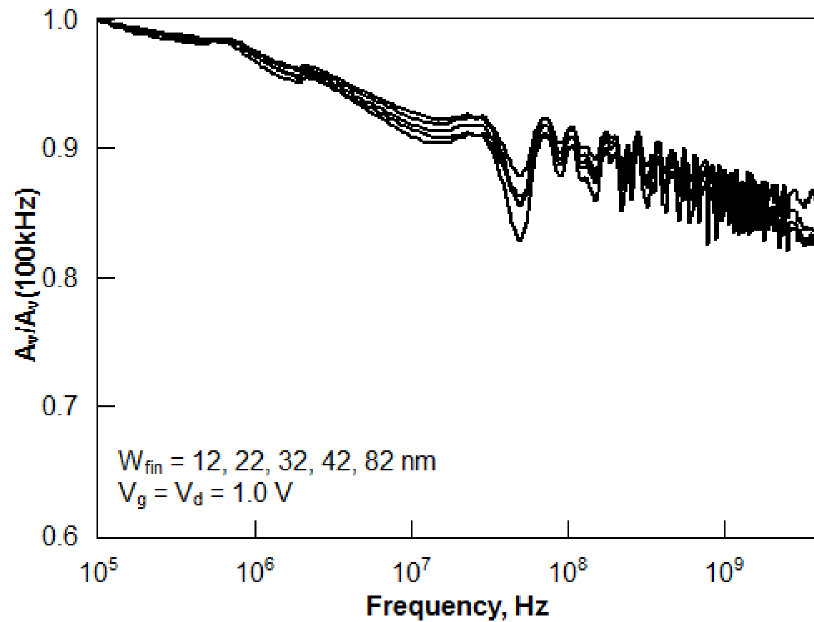

Figure 6.28. Variation of the intrinsic gain with frequency with respect to its value at 100 kHz in devices with various fin widths, N_{fin} = 10, S_{fin} = 328 nm and L_g = 40 nm at $V_g = V_d$ = 1.0 V.

The intrinsic gain variation in FinFETs (20%) in the frequency range from 100 kHz to 4 GHz is comparable to the gain variation in UTBB devices. It was reported in Section 4.3.3 (Figure 4.21) that the gain varies by ~32% in devices without a ground plane and ~12% in devices with a ground plane. Though the gate length is different (40 nm in FinFETs and 100 nm in UTBB devices) as well as gate overdrive (V_g-V_{th} = 0.6 V in FinFETs and V_g-V_{th} = 0.4 V in UTBB devices), the figures of the gain degradation are comparable. The FinFET gain variation is expected to reduce further and approach the values observed in the UTBB devices with a ground plane if a longer gate or lower gate overdrive are used. This suggests that both FinFET and UTBB technology offer similar analogue performance behaviour over the wide frequency range.

6.4 Summary

Due to smaller thermal time constants in advanced nanodevices, self-heating characterisation has to be performed at RF frequencies. The RF extraction technique was applied to determine self-heating and thermal parameters in n-channel SOI FinFETs of various geometries.

An increase of the fin width and the number of parallel fins leads to improved thermal properties of the devices, however it compromises integration density. An increase of fin width also affects electrostatic control as the behaviour of the FinFET becomes more like that of planar devices. Use of a higher number of fins requires more complex chip design as larger area structures have to be arranged on the chip surface area. It also leads to increased gate resistance and delays in signal propagation. Therefore, trade-offs exist between improved thermal properties and analogue performance of devices. However, fin spacing being a less critical parameter for thermal management can be exploited to reduce device area on the chip and improve integration density.

It was shown that the substrate effects are effectively suppressed in the examined FinFETs with the fin widths of few tens of nm. This is due to the reduction of the body factor which arises from the FinFET geometry. It is concluded that in order to improve FinFET performance over wide frequency range optimisation of thermal properties is required. This can be achieved by adjustment of device geometry as discussed in this chapter, source and drain engineering, reduction of operating voltage or implementation of bulk FinFETs. Reduction of the substrate effects in FinFETs results in decreased performance variation with frequency which is desirable for analogue applications.

The intrinsic gain being an important analogue figure of merit showed dependence on the fin width in the studied FinFETs. However, its relative change over the wide frequency range was shown to be independent of the fin width. It was also shown that the gain variation with frequency is comparable to the gain variation observed in the UTBB devices with a ground plane.

Chapter 7. Conclusions and future work

7.1 Summary

In this work thermal and coupling effects were experimentally assessed in advanced fully depleted silicon-on-insulator devices (FinFETs and UTBB). In Chapter 2 time and frequency domain methods of self-heating characterisation were experimentally compared. In Chapter 3 the effect of self-heating and substrate coupling on UTBB device performance was assessed in devices with various gate lengths. Also, analogue figures of merit of UTBB devices were benchmarked against analogue figures of merit of planar UTB devices and FinFETs available in the literature. UTBB devices outperform their counterparts in terms of the transconductance maximum, drive current and intrinsic voltage gain. This case proves that UTBB technology is a viable option for future device generations. The intrinsic gain of UTBB devices reaches its maximum in the moderate inversion regime which is beneficial for low operating power and low standby power applications. In Chapter 4 substrate effects in UTBB devices with various substrate doping (ground plane) were analysed. In Chapter 5 self-heating in UTBB devices and the effect of BOX thinning from 25 nm to 10 nm were characterised. Self-heating and substrate effects in FinFETs of various geometries were assessed in Chapter 6. The following sections summarise the findings relating to self-heating (Section 7.1.1) and substrate effects (Section 7.1.2).

7.1.1 Self-heating

In order to compare self-heating characterisation methods and determine the most suitable technique for further characterisation, time and frequency domain techniques were experimentally compared for a single set of devices expected to exhibit severe self-heating. PDSOI devices with 400 nm-thick BOX were selected to test the techniques experimentally. The RF and the hot chuck pulsed *I-V* techniques provided similar results. However, the pulsed *I-V* method reached its limits and could not be reliably applied to devices with thermal time constants under 100 ns using the existent equipment. Self-heating in advanced FDSOI devices such as UTBB and FinFETs can be underestimated if the pulsed *I-V* method is used. However, the RF technique can be extended to very high frequencies covering MHz-GHz range where dynamic self-heating is removed in advanced MOSFETs. This was also confirmed in Chapter 5 where both pulsed and RF techniques were applied to UTBB devices. The RF technique is required for accurate self-heating characterisation in FDSOI devices as it was found that in both

UTBB devices and FinFETs dynamic self-heating is manifested in the frequency range up to 100 MHz.

It was found that in UTBB devices with a ground plane the output conductance with frequency is mostly degraded by self-heating in the wide frequency range. This contrasts with devices without a ground plane, where substrate effects degrade the output conductance more than self-heating. Thermal properties of UTBB SOI MOSFETs with two different BOX thicknesses were characterised. Although the ultra-thin BOX is expected to improve thermal properties, the thermal effects are significant. The average temperature rise reaches 38 °C and 65 °C in a typical regime of operation in saturation in devices with 10 nm and 25 nm-thick BOX, respectively. Such temperature rise results in 6-7% drain current degradation for both devices which is considerably less than that reported in literature for MOSFETs on thick BOX or SiGe buffers. The main self-heating related issue which is important for analogue applications is the output conductance degradation which may reach 60%. Both 10 and 25 nm-thick BOX devices exhibit very similar output conductance and drain current degradations due to self-heating. This suggests that the BOX thickness can be relaxed in order to improve uniformity, parasitic coupling and leakage through the substrate if a slight temperature rise can be tolerated.

Self-heating was also quantified in n-channel FinFETs of various geometries. It was shown that the thermal properties strongly depend on the FinFET geometry. This suggests that the trade-offs exist between improved thermal properties and integration density, electrostatic control, chip design complexity, gate resistance and delays in signal propagation and analogue performance.

Depending on the device geometry the extracted thermal resistance in FinFETs ranges from ~9 $\mu m \cdot K \cdot mW^{-1}$ to ~43 $\mu m \cdot K \cdot mW^{-1}$. The thermal resistance in UTBB devices is 70 $\mu m \cdot K \cdot mW^{-1}$ in 10 nm BOX devices and 84 $\mu m \cdot K \cdot mW^{-1}$ in 25 nm BOX devices. In planar PDSOI devices the thermal resistance is 220 $\mu m \cdot K \cdot mW^{-1}$ which is ~3 times higher than in the UTBB devices. This is most probably caused by very thick buried oxide which impedes heat dissipation. FinFETs exhibit lower thermal resistance than UTBB devices most probably due to more effective heat removal through the source and drain regions than in UTBB devices as the area of the heat removal cross-section is much bigger in the FinFETs studied than in UTBB devices. Also heat removal through the source and drain regions may be more effective due to the smaller gate length in the FinFETs (40 nm) than in UTBB devices (100 nm).

Figure 7.1 summarises the self-heating results obtained for various devices in this work. Figure 7.1 shows the temperature rise variation with the normalised power in the range from 0.3

mW·μm^{-1} to 1.2 mW·μm^{-1}. The power range is selected according to ITRS requirements for low operating power and low standby power applications (~0.3-0.4 mW·μm^{-1}) and for high performance applications (~1.2 mW·μm^{-1}) for present and next generations. PDSOI device results shown in Figure 7.1 were obtained in Chapter 2, UTBB results in Chapter 5 and FinFET results in Chapter 6. Only the reference FinFET is shown in Figure 7.1 (bold symbols in Table 6.1). Thermal resistances of the aforementioned devices are also presented in Figure 7.1. ITRS imposes limits on the operating temperature due to reliability issues. The limit is set to 90 °C. If the ambient temperature is 25 °C (the reference temperature in all experiments in this work) then the maximum temperature rise allowed by ITRS is 65 °C. The ITRS limit is also shown in Figure 7.1. As seen from Figure 7.1, PDSOI devices do not satisfy the requirement in the 0.3-1.2 mW·μm^{-1} range. As it is shown in Chapter 6, the thermal properties of FinFETs greatly depend on geometry. The given device which features 22 nm wide fin, satisfies the ITRS limit on the operating temperature thus making FinFETs suitable for various applications ranging from low operating power and low standby power to high performance. UTBB devices with 10 nm and 25 nm BOX thicknesses meet the ITRS requirement in the low power range thus making them suitable for low operating power and low standby power applications from the thermal point of view. Note, that in Figure 7.1 the average device temperature is shown. However, the temperature gradient in a device exists. Therefore some parts of a device might be hotter than indicated in the figure.

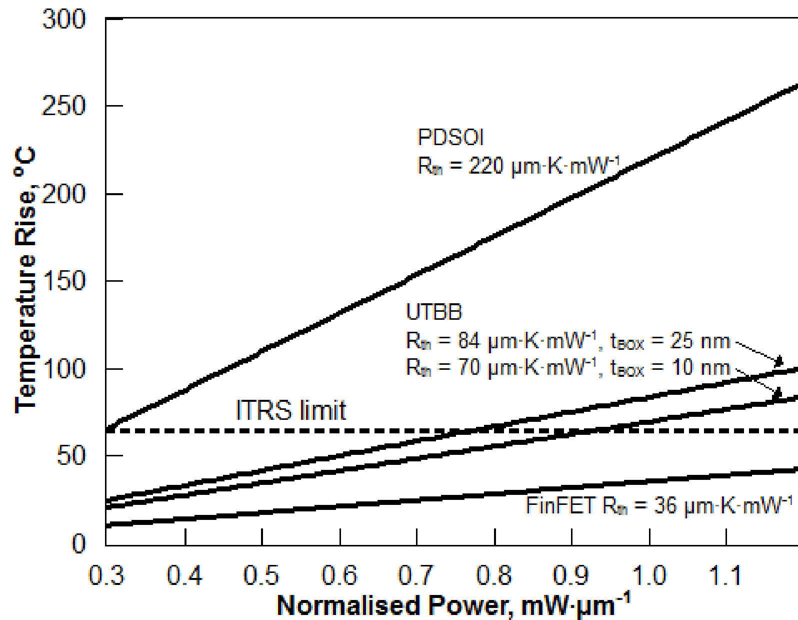

Figure 7.1. Temperature rise variation with normalised power and thermal resistance in PDSOI devices, UTBB devices with 10 nm and 25 nm BOX thicknesses and FinFETs with 22 nm wide

fin (reference device in Chapter 6). The ITRS limit is a requirement imposed to device operating temperature due to reliability concerns.

Thermal properties of advanced FDSOI devices are affected by device geometry and materials. Therefore, optimisation of UTBB geometry (e.g. source and drain extensions, body thickness and gate length) is expected to improve thermal resistance. This suggests that UTBB technology has a potential for a wider power range.

7.1.2 Substrate effects

It was shown for the first time for UTBB devices that the output conductance variation caused by the substrate effect can be stronger than that caused by self-heating if the substrate is undoped. Although the substrate-BOX interface is inverted at all bias regimes in devices with 10 nm BOX, the amplitude of the output conductance transition at high frequencies is bias dependent. An increase of the gate voltage leads to an increase of the output conductance transition. The gate length scaling from 100 nm to 30 nm also leads to the increase of the output conductance transition amplitude as coupling is amplified due to the source and drain proximity. The larger output conductance transitions with increasing bias and decreasing gate length are caused by increasing transconductance and the inversion charge density at the substrate-BOX interface.

Substrate doping in UTBB devices is an effective method to suppress the source and drain coupling through the substrate. Incorporation of a p-type ground plane results in much lower output conductance transition amplitude. Implementation of a p-type ground plane in nMOSFETs introduces little fabrication complexity. Suppression of substrate effects results in improved gain degradation over the wide frequency range compared with UTBB devices that do not have a ground plane. In the frequency range from ~30 MHz to 4 GHz the gain degrades by 2% in the devices with a p-type ground plane and by ~12% in devices without a ground plane at the same bias conditions.

As well as UTBB devices with a ground plane, FinFETs with few tens of nm wide fins show relatively weak substrate effects. Reduction of the body factor with decreasing fin width leads to a smaller output conductance degradation. Suppressed substrate effects in FinFETs result in improved performance variation with frequency as required for analogue applications. Further improvement of the FinFET performance over the wide frequency range requires thermal

management. This can be achieved by optimisation of thermal paths by adjusting device geometry.

7.1.3 Intrinsic voltage gain

Variation of the output conductance and transconductance due to self-heating and substrate effects in FDSOI devices results in voltage gain variation with frequency. This effect is undesirable as it results in the frequency-dependent analogue behaviour. It was shown in this work that the intrinsic voltage gain in FinFETs depends on the fin width. However, its relative degradation in the frequency range from 100 kHz to 4 GHz with respect to the value at 100 kHz is fin width independent. The variation in the aforementioned frequency range is ~20% in 40 nm gate length FinFETs at the gate overdrive 0.6 V and the drain voltage 1.0 V. This degradation is expected to reduce at lower gate voltages or in longer devices and to approach the value of the gain degradation in UTBB devices with a ground plane. The gain variation with frequency is ~12% in 100 nm gate length UTBB devices with a ground plane at the gate overdrive 0.4 V and the drain voltage 1.0 V. It was observed that the intrinsic gain variation in the lower frequency range (from 100 kHz to few tens of MHz) which is caused by self-heating is very sensitive to the channel thickness and source and drain extension parameters.

7.1.4 Final word

From the obtained experimental results it is evident that both FinFET and UTBB with a ground plane technologies offer similar analogue performance behaviour over the wide frequency range. Both UTBB and FinFET technologies can be suitable for future generations of advanced semiconductor devices from the thermal point of view. UTBB devices and FinFETs might be used for low operating power, low standby power and high performance applications. This was demonstrated for FinFET technology and it is expected from UTBB technology if device geometry is adjusted. Results of this work suggest that substrate effects are not a hindrance for FDSOI technology. However, these parasitic effects have to be taken into consideration. Management of the substrate effects introduces little complexity to UTBB technology (achieved by substrate doping) and is achieved in FinFETs due to their 3D nature. Based on the findings of this work it can be suggested that UTBB devices can readily find applications in the low power range because of their enhanced performance in the moderate inversion regime as evident from the analogue figures of merit and their suitability from the thermal perspective. FinFETs can find applications in various power regimes. However FinFETs might be most suitable for high performance applications (due to the multi-gate architecture

causing enhanced current-carrying capability) where potentially high fabrication cost can be tolerated.

7.2 Recommended future work

The work presented in this thesis might be expanded. Study of the impact of device geometry on self-heating in FinFETs might be extended to consider more FinFET parameters, e.g. gate length, fin height, BOX thickness and size and shape of the source and drain extensions. The impact of these parameters on thermal properties of FinFETs was modelled previously [49], [50], [100], however experimental results are lacking. Knowledge of the thermal resistance for a range of FinFET parameters can be used to identify the thermal resistance of each thermal path. This information can be used to predict the thermal resistance for any combination of device parameters. Possible future work might include experimental investigation of self-heating in bulk FinFETs, where thermal effects are expected to be alleviated. It was shown in this work that thermal properties of UTBB devices are sensitive to device geometry. However, experimental results for UTBB devices of various geometries are lacking. Further research can include study of the impact of the channel thickness, BOX thickness, gate length, size of the source and drain extensions and finger spacing in UTBB devices. Further self-heating investigation in FDSOI devices may include analysis of parasitic leakage currents which are amplified at elevated temperatures. Nonlinear thermal effects, e.g. thermal resistance dependence on power, might also be investigated experimentally in advanced FDSOI devices.

Investigation of substrate effects in FinFETs in this work led to the estimation of the shielding distance in FinFETs from electrical measurements. Transmission electron microscopy may be used in future to confirm the findings. Further research of the substrate effects may include measurements of low frequency substrate effects in FDSOI technology as well as complete physical model of the source and drain coupling through the substrate.

FDSOI technology has to address issues like yield, uniformity and parasitic effects. Development of fabrication techniques which would allow acceptable uniformity of BOX and Si channel and well controlled etching of 3D structures might in the future enable building multi-gate structures on ultra-thin BOX with substrate doping. Such structures might combine benefits of FinFETs and UTBB devices – current-carrying capability, suppression of substrate effects and improvement of thermal properties.

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