Minimisation of Output DC Current Component in Grid-Connected Inverters for Solar Power Applications

Farag Hussein Bahri Berba

B.Sc., M.Sc.

A thesis submitted for the degree of

Doctor of Philosophy

April, 2012

School of Electrical, Electronic and

Computer Engineering

Newcastle University

United Kingdom

ABSTRACT

In grid-connected photovoltaic applications, a supply-frequency output transformer is normally used to isolate the inverter from the supply. This transformer is heavy, costly and adds to the overall power loss. However removal of the output transformer can result in unwanted DC components appearing in the inverter output current. Excessive DC current injection into the distribution network can affect distribution components as well as other loads connected to the network.

There are various circuits which can be used to for grid connection without the use of an output transformer. These include the 2-level half-bridge and the H-bridge inverters. These circuits have the disadvantage of the requirement for higher rated power devices or increased EMI problems due to high frequency switching of the DC-link relative to earth.

To overcome these problems, a three-level half-bridge inverter circuit is used, where the DC-link voltage can be twice the device voltage rating allowing the use low rated switching devices. The neutral conductor is connected to the mid-point of a split rail supply from PV array, and therefore the DC-link voltage is not switching relative to earth.

The aim of this research is to minimise the DC current component in the output of a grid-connected inverter when a supply-frequency output transformer is not used. A three-level diode-clamped half-bridge inverter is proposed to interface the PV panel directly to the utility grid. The main contribution of this research lies in the development of an auto-calibration technique for the DC-link current sensors in the multi-level inverter. Combined with a current feedback control scheme this technique allows the minimisation of DC current offset drift in the Hall-Effect current sensors. Auto-calibrated DC-link current sensors in turn allow the inverter output current controller to minimise the output DC current component in spite of sensor drift and other disturbances.

A comprehensive review on the different types of grid-connected PV systems, the problems caused by DC current injection into the grid, and up-to-date techniques to

overcome this problem is included. The performance of the auto-calibration technique is investigated using both computer simulation and an experimental test rig.

Acknowledgment

I would like to express my sincere appreciation to my supervisor, Dr. David J Atkinson, for his guidance, encouragement, continued support throughout the course of this work and patience, while reading and commenting on the thesis. His extensive knowledge, advice and creative thinking have been an invaluable help to this project. I can only wish him all the best for the future. Thank you for everything, David. I would also like to thank my second supervisor, Dr. Matthew Armstrong, for general guidance.

Many thanks are due to all the technical support staff at Electronics Workshop, particularly Darren Mackie, Stephen Robson and Jeffrey Warren for their help in design and manufacturing the printed circuit boards. Thanks also to Jack Noble from the mechanical workshop in helping with the construction of the equipment necessary to carry out the work.

I would like to thank all members of staff within the power electronics, drives and machines (PEDM) group. Thanks also go to John Bennett for helping me to get familiar with programming and to setup the microcontroller. Thanks to all my colleagues in the UG lab for providing an enjoyable educational atmosphere, Special thanks goes to James Richardson and Stephen Mitchell for their significant help when sometimes something went wrong whilst doing the practical work

Finally my deepest thanks are extended to my parents, my wife, my children and my sisters for their continuous support, and providing motivation during the period of this research.

TABEL OF CONTENTS

List of Tables

List of Figure

List of Abbreviations

AC	: Alternating Current
APOD	: Alternative Phase Opposition Disposition
CO_2	: carbon dioxide
DC	: Direct Current
DG	: Distributed Generation
DNOs	: Distribution Network Operator's
DSP	: Digital Signal Processing
dsPIC	: Digital Signal Peripheral Interface Controller
DCMI	: Diode clamped multilevel inverter
DMCI	: Data Monitor Control interface
EMI	: Electro Magnetic Interference
EMC	: Electro Magnetic Compatibility
FCI	: Flying Capacitor Inverter
HBCC	: Half Bridge Capacitor Clamped
HBDC	: Half Bridge Diode Clamped
IEEE	: Institute of Electrical and Electronics Engineers
IGBT	: Insulated Gate Bipolar Transistor
IPCC	: Intergovernmental Panel on Climate Change
LF	: Low frequency
LPF	: Low Pass Filter
MLIs	: Multi-Level Inverters

MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
MPPT	: Maximum Power Point Tracking
MSPWM	: Multilevel Sinusoidal Pulse Width Modulation
NPC	: Neutral Point Clamped
PC	: Personal Computer
PCB	: Printed Circuit Board
PD	: Phase Disposition
PI	: Proportional Integral
PLL	: Phase Locked Loop
PPM	: parts per million
POD	: Phase Opposition Disposition
PV	: Photovoltaic
PWM	: Pulse Width Modulation
RMS	: Root Mean Square
SDCS	: Separate DC Source
STC	: Standard Test Conditions
VT	: Voltage Transformer
ZCD	: Zero Crossing Detection

CHAPTER 1

INTRODUCTION

1.1 Background

World electricity demand is increasing every year, where most of this energy is produced from fossil fuel sources, such as gas, oil and coal. As a result, these sources are being depleted rapidly. Also, the combustion products of these sources are causing global problems, such as the greenhouse effect and pollution, which pose great danger to our environment and eventually all life on our planet. Since the industrial revolution, conventional fuels have been responsible for climate change by producing more than 60% of the carbon dioxide (CO_2) emitted into the atmosphere each year. The Intergovernmental Panel on Climate Change (IPCC) mentioned that the concentration of greenhouse gases in the atmosphere must not be allowed to exceed the equivalent of 450 parts per million (ppm) of CO_2 by volume by 2030, compared with 385ppm at present, and 280ppm before the industrial revolution. This limit of 450ppm of CO_2 was selected for 2030 to reduce CO_2 emissions and limit the increase in temperature to 2°C around the world [1].

In order to reduce the possible damage from these emissions, renewable energy is attracting worldwide attention as an alternative energy source. Many industrial countries in the last two decades have begun to improve and develop a wide range of renewable energy projects involving photovoltaic cells (PV), wind turbines, and hydroelectric and biomass energy conversion technologies to meet their energy requirements. For example, at least 118 countries have a policy to promote renewable power generation by early 2011 compared to 55 countries in early 2005 [2]. This is shown clearly in the growth of renewable energy, which has increased from 207GW in 2006 to 312GW in 2010. The annual investment has increased to reach $211 billion, i.e. more than three times that in 2006, which was $63 billion [2] [3]. The United Kingdom government published an energy white paper[4], which

had the stated goal of increasing the overall amount of renewable energy sources as a proportion of electricity supply sources to 20% by 2020.

The most common photovoltaic generator, which directly converts solar radiation into electricity, is single-phase and low voltage. This generator is directly connected to a distribution network to supply small commercial and industrial units, homes and remote farms.

In the last ten years, the use of single-phase grid connected inverters for the interfacing of photovoltaic panels, to the distribution network has attracted much interest.

The work in this thesis is concerned with research into the grid connected photovoltaic inverter system. In particular, the three-level half bridge single-phase inverter. The inverter operates in a current controlled mode to inject a unity power factor sinusoidal current waveform into the utility system. The inverter can affect the grid by causing a number of problems due to the injection of DC current into the grid. This will increase power loss and overheating in transformer windings and will accelerate the breakdown of cable insulation.

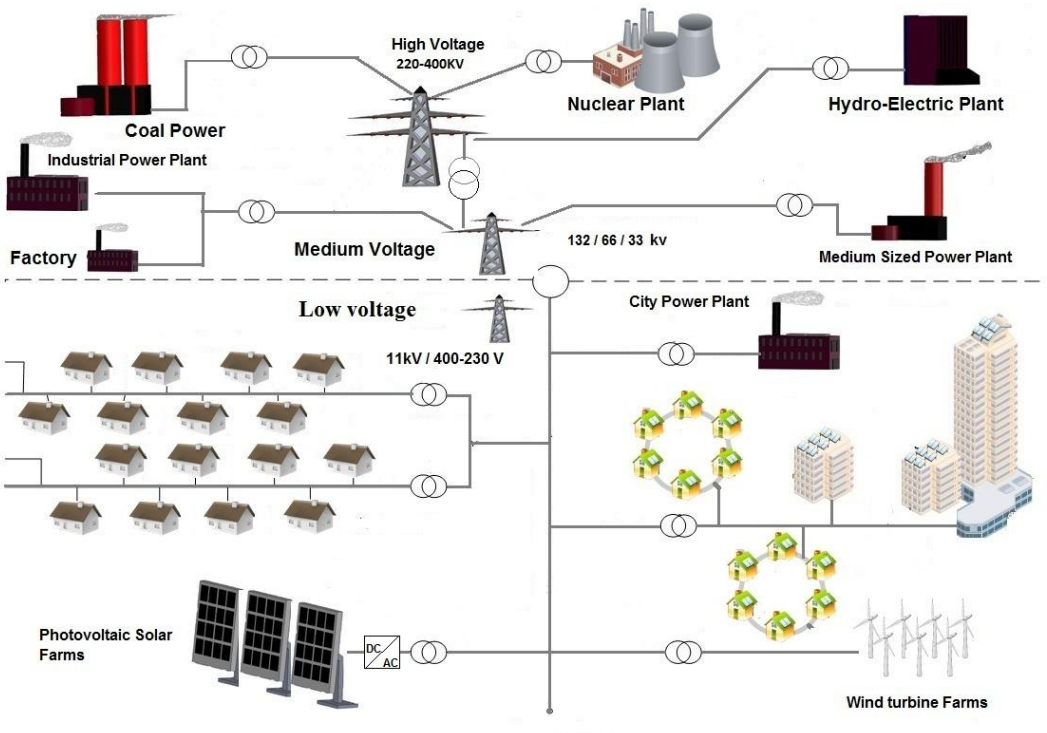


Fig.1.1: Electrical supply sources

Fig.1.1 shows a simplified view of electrical supply sources. The electricity generated by coal, nuclear and hydroelectric power plants is stepped up by power transformers from the generation voltage range, between (11kV to 33kV) and supplied to the national grid at voltages ranging between 220kV to 400kV. This is then stepped down via transformers to the medium voltage range (132kV, 66kV, and 33kV), where some of the medium size power plants, such as gas and steam turbines, are connected at this level of voltage. These types of power plants, typically gas turbines, are usually built next to a heavy industrial load, as well as being used in the peak period to meet electrical demand. Finally, small commercial and industrial loads, homes and remote locations, such as farms, are connected at low voltage level ranges (11kV/400-230V). Other sources of distributed generation, such as renewable sources are connected at this point, and this results in a change in power flow. In the traditional power system design, the power flow is from the central generation plant to the end user. Distributed generation makes the grid more complex due to bi-directional energy flows, but at the same time, has the following potential advantages, as explained by *Yiwei et al.* [5] and *Kuang, Li et al.*[6].

- Improvements in the reliability of power supply
- Reduced feeder loss
- Reduced energy cost
- Reduced cost of building new power distribution stations
- Reduced transmission loss

1.2 Grid Connected Photovoltaic System Overview

A grid-connected photovoltaic system can be defined as the link between the solar cells and the national grid system via a DC to AC converter as illustrated in Fig.1.2. The complete grid-connected photovoltaic system is comprised of a number of units. The first unit is a solar array, which transforms sunlight into electric current. The second unit is an electronic power converter, which in turn is divided into two parts; the DC/DC boost converter is used to step up the relatively low solar panel DC

voltage to the desired level for input to the DC/AC inverter. The inverter is operated in current control mode to inject a unity power factor current waveform into the grid. Finally, a low voltage transformer is used as galvanic isolation between the grid and photovoltaic system [7].

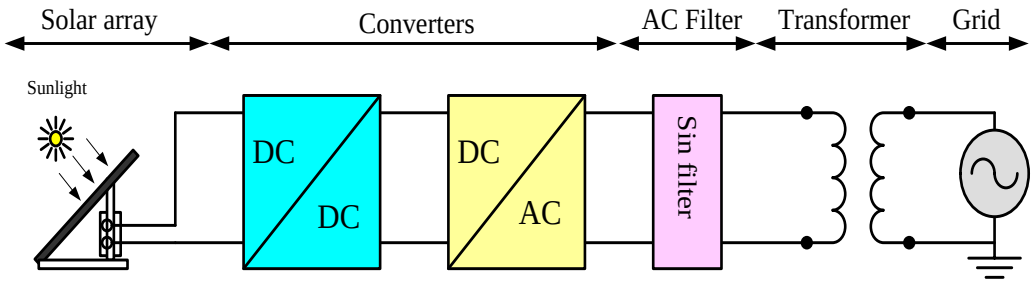


Fig.1.2: Grid connected photovoltaic schematic

1.2.1 Photovoltaic Systems

1.2.1.1 Solar Cell

A solar cell can be defined as a static generator, which converts sunlight into electricity without any moving parts, noise or pollution.

The first photovoltaic cells were manufactured in the 1950s [8], and most of them were made from silicon. Silicon is a "semi-conductor", and has properties of both a metal and an insulator. Fig.1.3 shows the configuration of the solar cell, which consists of two types of semi-conducting material, n-type and p-type. The n-type material has been manufactured to contain one extra electron, while the p-type material contains one electron less than the n-type material.

When the solar cell is exposed to sunlight, this results in the movement of electrons in the semiconductor material; this movement of electrons is the "photoelectric current". By connecting the p- and n-sides to an external circuit or a load, this photo current can be utilized.

Most solar cells available on the market are produced using silicon wafers, which may be mono-crystalline, poly-crystalline or amorphous. The mono-crystalline type has high efficiency with high cost, while the amorphous type has low efficiency with low cost. In the Solar Cell Production and Market Implementation report, July 2011, about 80% of the current production uses wafer-based crystalline silicon technology [9].

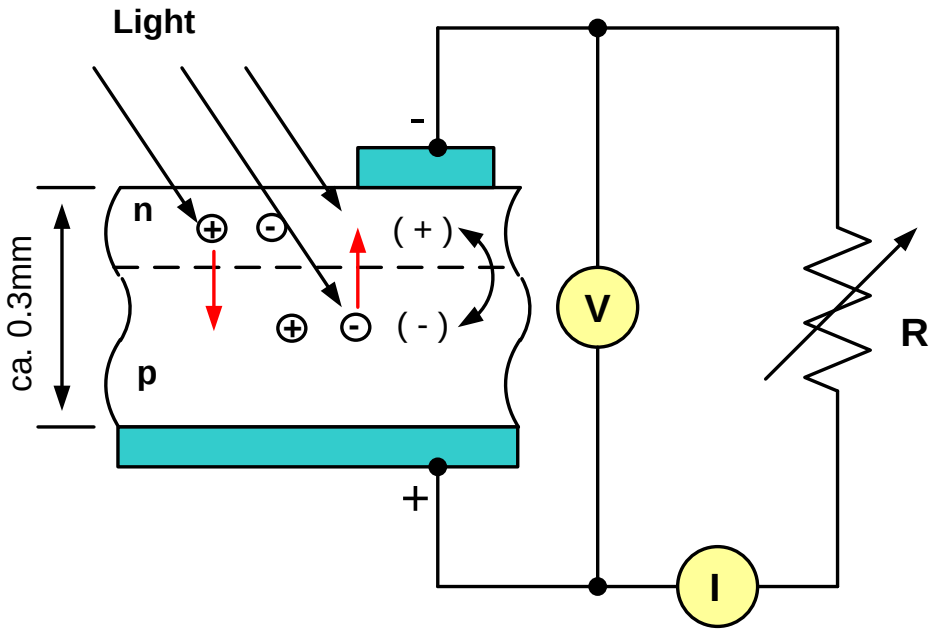


Fig.1.3: Solar cell principle of operation

1.2.1.2 Photovoltaic Modules

In order to provide practical current and voltage levels, the individual solar cells must be connected together to obtain the required level of DC power. This connection will be a series and parallel combination to create a photovoltaic module. The module is protected from environmental damage with a low-iron glass cover and then framed in aluminium-Tedlar.

The module can be used alone or connected to other modules to make up a photovoltaic array. There are different sizes of PV modules to meet different energy demands. Fig.1.4 shows a typical construction of a PV module. It is created by connecting the solar cell in series to form a module. The module is then connected to other modules to create a panel. The panels are then connected to form a PV array.

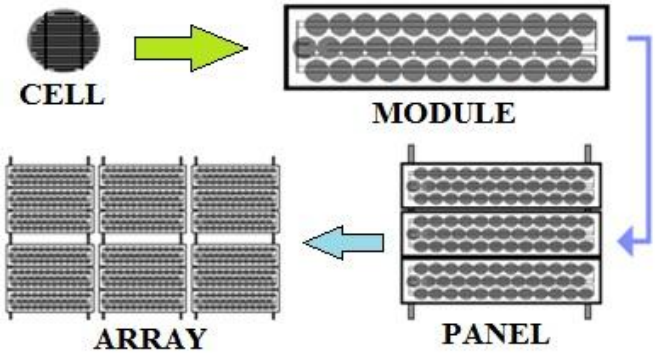


Fig.1.4: Construction of a solar array

1.2.1.3 Solar Insolation

Solar insolation is a measure of solar radiation energy received by an infinitesimal surface area in a given time. It is commonly expressed as average irradiance in watts per square meter (W/m^2). Irradiation is the time integral of irradiance over a specified period and it is commonly expressed as Wh/m^2. The average solar power varies for different geographical locations (see the map of insolation Fig.1.5 and Fig.1.6).

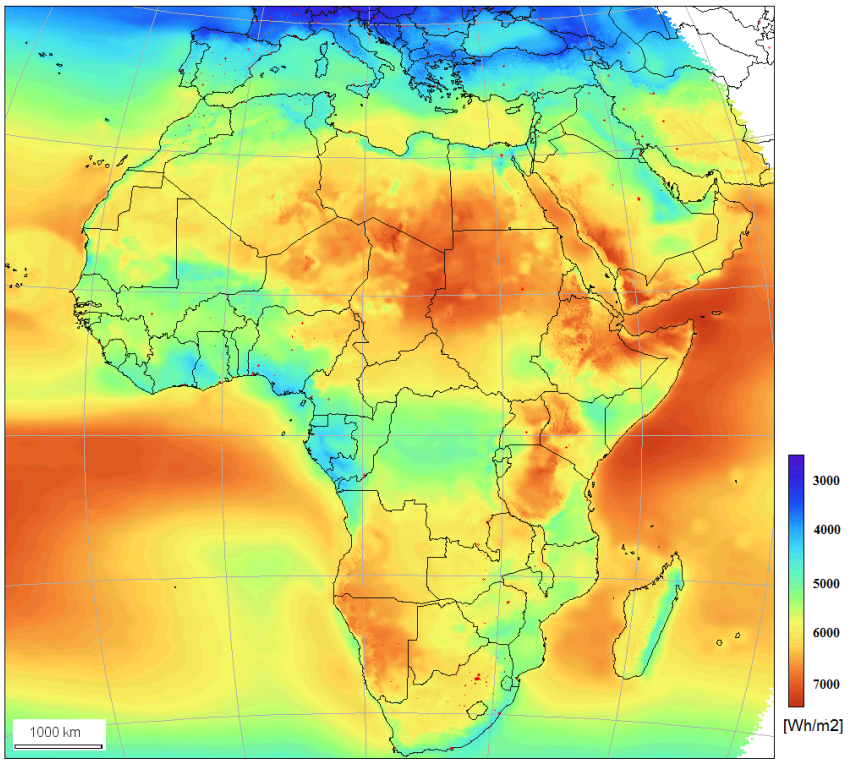


Fig.1.5: Solar irradiation in Africa countries

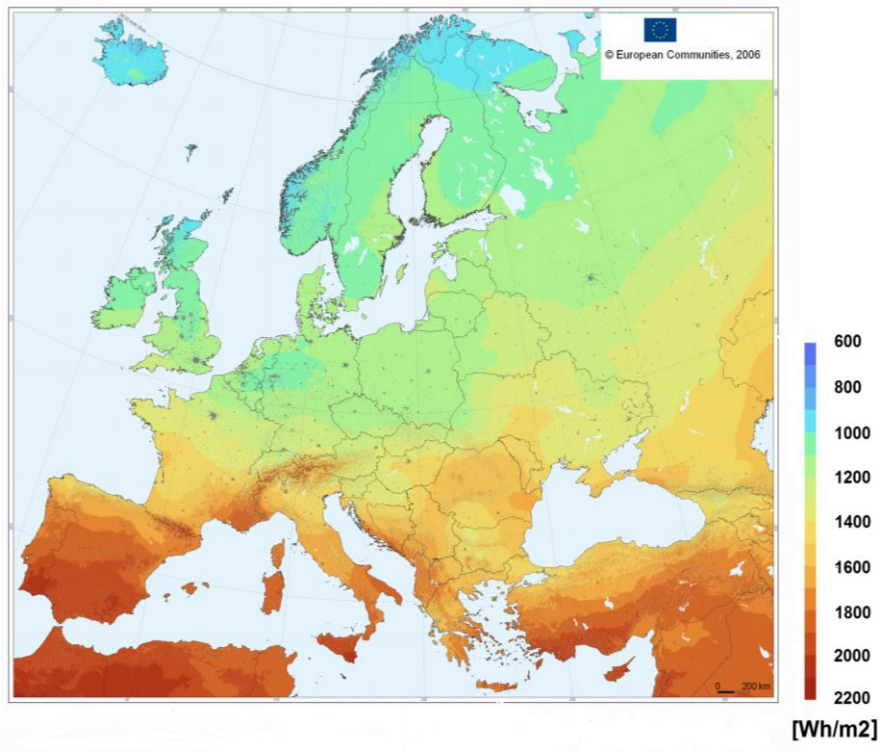


Fig.1.6: Solar irradiation in European countries

Other factors also affect the output power of a PV module, such as module temperature [10]. In general, the PV module Standard Test Conditions (STC) are created at 1000W/m^2 radiation spectrum equivalent to the solar spectrum at air mass 1.5 and an operating temperature of 25°C [11]. However, this condition is not present in most cases, especially in areas with high temperatures. In practice, increased temperature will affect the efficiency of the PV module, and results in an output power reduction of between 0.38 to 0.50 % for every 1°C rise [12] [13]. So in hot countries, where the temperature reaches 50°C in summer, the efficiency of the PV module will be reduced by 12.5%. The efficiency is also affected by wind speed and direction. *Tina and Abate* [12] studied the effect of wind speed and direction on a PV module under varying wind conditions, and found that higher wind speeds produced positive results for the PV module by reducing the temperature. Another factor is the tilt angle, which is the angle between the plane of the module and horizontal. This angle depends on the position of the sun throughout the year. For example, in summer when the sun position is nearly in middle of the sky, a small tilt angle will be required to obtain maximal power and vice versa in the other seasons of the year. The maximum output is usually obtained when the array tilt angle is roughly equal to the latitude angle. The next factor is the ability to carry out sun tracking, which requires a device that ensures that the PV module is pointing directly towards the sun at all times. This tracking can be along one axis or two [11]. One axis tracking follows the Sun's movement from east to west. In this case, the output of the PV module can be increased by 30% for clear sky conditions. In two axes tracking, where the Sun's movement is followed in two directions (from east to west and from north to south) the PV module can achieve a slight difference in output power in summer time, but this is increased in the other months, as reported by *Lepley* [14]. The cost of tracking mechanisms is 2% of the total capital cost, as presented by *Johan et al.* [15]. Moreover the efficiency of any solar array can be improved significantly using Sun tracking. The Sun tracker is an automated solar panel that actually follows the position of the Sun to increase the output power of photovoltaic arrays by placing the panels parallel to the Sun throughout the day. As a result, 33% additional power can be achieved in the PV system's output using this technique, as reported by *Roth et al.* [16]. The final factor is shade, where shading part of the PV module by clouds or other weather phenomena will affect the output of that module.

If this module is connected to other modules in a panel or array, the shade will affect the whole panel or array.

1.2.2 Boost Converter

Many solar arrays have a low level output voltage (25 - 50V) [17]. For this reason, a boost converter is required to boost the low voltage to (380 - 400 DC voltage) for compatibility with the requirements of grid connection. *Bratcu, Munteanu et al.* [18] presented a method, which consists of a series topology of per-panel dc–dc converters; these are connected to a single-phase DC/AC inverter. This method has some advantages over the parallel connection case, as it is possible to operate each boost with a small step-up ratio, resulting in good efficiency at low cost. *Haeberlin* [19] and *Schimpf, Norun* [20] both described different methods of achieving the inverter DC link voltage without the need for a DC/DC converter. Fig.1.7 shows various combinations of series and parallel configurations to get a high DC voltage level from the PV module. The simple method is to use a series connection for only a few PV panels, as illustrated in Fig.1.7a. This approach has high inverter efficiency, simplicity and low cost. This approach is still the first choice for medium and large PV applications, because it has a higher power level, and does not even have Maximum Power Point Tracking MPPT for each string. Fig.1.7b represents the string inverters, where each string has MPPT, but the cost of this module is higher per KW due to the low power rating compared with the centralized inverter. Finally, to avoid a problem occurring as in previous inverters, the PV-plant module inverter is used. This type of inverter operates at low DC power level, and so no DC wiring is needed. Therefore, the DC power's high risk is reduced, with a simple connection to the grid. This inverter has some disadvantages, such as low efficiency and high cost due to the lower power rating per unit.

Another approach, using a fly-back converter, is described by *Ho-sung Kim et al.* [21]. This type of converter provides galvanic isolation between the grid and PV system, giving increased PV system efficiency.

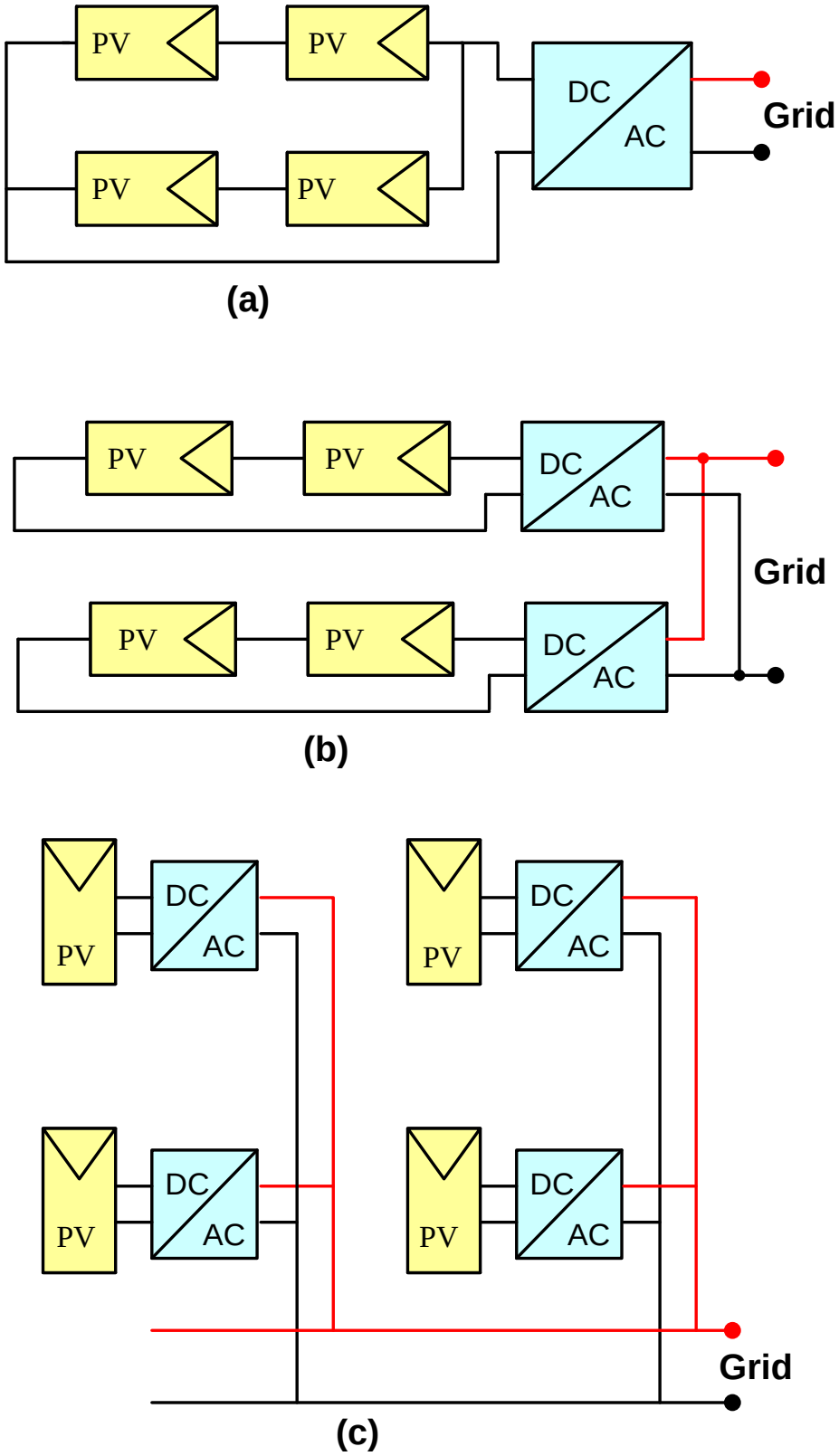


Fig.1.7: Configurations for PV-systems: (a) centralized inverter, (b) string inverters, (c) string and module inverters

1.2.2.1 Maximum Power Point Tracker

The power delivered by the photovoltaic system is dependent on the irradiance, temperature, and current drawn from the cells. For best utilization, most photovoltaic inverter systems use a technique to make the PV module operate effectively known as Maximum Power Point Tracking (MPPT). There have been many different techniques developed to achieve MPPT in a PV system [22] [23]. A simple tracking method that monitors the output voltage of PV module uses current control of DC/DC converter to achieve the highest power level [24]. There are also methods that use a complex mathematical operation to obtain maximum power and high control accuracy, as implemented in space satellites and orbital stations. These methods are used when the cost and complexity of the MPPT technique are not as important as performance and reliability [22].

1.2.3 DC / AC Converter

The DC / AC inverter is the second part of power conversion, and is widely used in many applications, such as grid-connected photovoltaic systems and AC motor drives. The main objective of DC / AC inverters is to convert DC voltage to sinusoidal AC voltage, while controlling magnitude and frequency. In most cases, the grid connected DC to AC converter is required to inject unity power factor sinusoidal current into the grid.

1.2.3.1 Grid Synchronisation

Injecting unity power factor sinusoidal current into the grid, requires a synchronisation technique, such as a Phase Locked Loop (PLL), or a Zero Crossing Detector (ZCD). Both techniques are used to synchronise the DC to AC inverter output current to the distribution network. *Wall* [25] introduced a simple method for detecting zero crossing, capable of minimizing phase detection errors, which had limited success. *Blaabjerg et al.* [26], and *Timbus et al.* [27] reviewed the methods for synchronization of power electronic converters to the distribution network

system. These studies present five methods, namely adaptive PLL, *dq* PLL, *αβ* filter algorithm, *dq* filter algorithm and ZCD. The first two methods, adaptive PLL and *dq* PLL are methods suitable for all grid connected applications. The second two methods, i.e. *αβ* filter algorithm and *dq* filter algorithm, have difficulty in extracting the phase angle, when the grid frequency varies. Finally, the ZCD was not including the test duo to low dynamic performance, and only detected every half cycle.

1.2.3.2 Anti-Islanding Protection

All distributed generation equipment requires anti-islanding protection when connected to the power distribution network. Many islanding protection methods have been proposed. *Teoh and Tan* [28], and *Aghdam, Ghadimi et al* [29] have both reviewed Islanding detection techniques for a distribution system with distributed generation divided into two different categories. *Kern* [30] studied the over/under voltage detection, over/under frequency detection and other islanding protection methods for photovoltaic grid-connected inverters. The test results showed that the inverter was disconnected from the grid, when voltages were above 110% and below 86% of rated voltage. The inverter tripped when the grid frequency varied by ± 1Hz for 100 cycles period time or ±3Hz for 7 cycles period time from the nominal frequency (60Hz).

1.2.4 Transformer Coupling

The aim of transformer coupling in a grid-connected photovoltaic inverter system is to prevent DC current flow from the inverter side into the distribution network. However, if this DC current flow is not prevented, it may saturate and overheat the power transformer in the utility system [31]. The simple method to isolate DC current injection is to install a 50Hz transformer at the output of the inverter, as shown in Fig.1.8. This method has many disadvantages, for example increased cost, size, and weight as well as power losses [32]. If the transformer is removed, the inverter must cover the purpose of the transformer. In this case, two issues will

appear. The first issue is that the galvanic isolation between the photovoltaic generator and the grid is lost, where this was provided by a high frequency transformer. The second issue is that the inverter could inject DC current into the grid, which causes negative effects on the distribution network equipment, such as distribution transformer and underground cables. On this basis, this research concentrated on using a suitable method to minimize DC current injection into the grid.

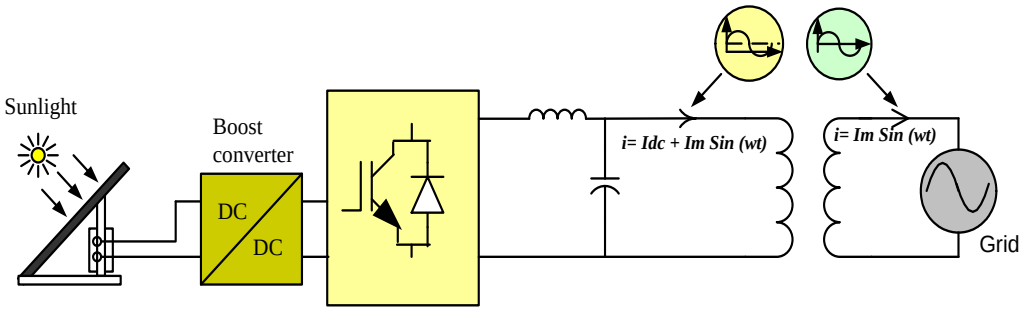


Fig.1.8: Distribution generator connected to the grid through isolation transformer

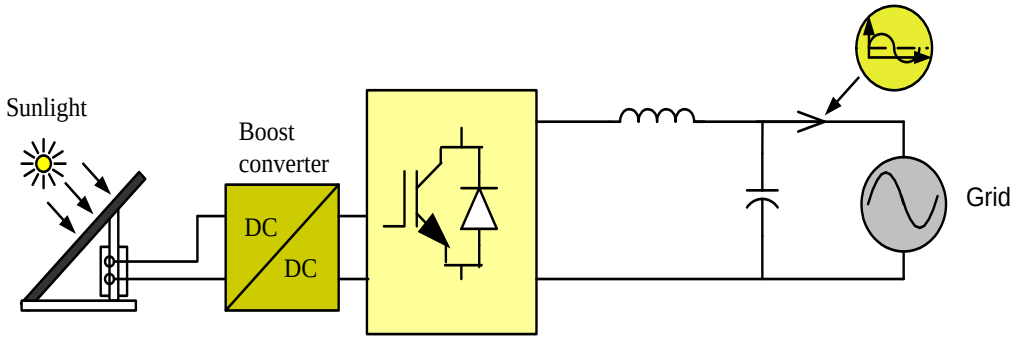


Fig.1.9: Distribution generator connected to the grid without isolation transformer

1.3 Thesis Objective and Contribution

The objectives of this thesis are:

- To develop a comprehensive understanding of the transformerless grid-connected converter for a photovoltaic system.
- To investigate different Sinusoidal Pulse Width Modulation (SPWM) techniques for a three-level half-bridge inverter topology to achieve better harmonic performance using modelling and simulation.
- To study the topology of a three-level, half-bridge inverter for grid applications to improve cost and size of grid connected converters.
- To develop a novel method to prevent DC current in the inverter output using DC link current sensors and an auto-calibration technique.
- To build and test a three-level, half-bridge inverter topology using the proposed technique and the dsPIC based controller.
- To provide experimental results to validate the theoretical analysis.

1.4 Overview of the Thesis

This thesis consists of seven chapters and four appendices. This chapter provides general discussions regarding the photovoltaic grid connected inverter and information on the background of the thesis.

Chapter 2 describes the sources of DC current injection into the distribution network; and explains the effects of this current on the distribution system equipment. It reviews the standards and regulations, which cover DC current injection into the grid in different countries. Moreover, it explores the main techniques used to minimize DC current injection into the grid and the current measurement methods that have been used for these techniques.

Chapter 3 provides a review of the multi-level inverters, including diode clamped multi-level inverters, cascaded multi-level inverters, capacitor clamped multi-level inverters, and other types of multi-level inverter topologies. It also explains the principle of operation of the first three types of such inverters.

Chapter 4 presents the three-level, half-bridge inverter topology. It describes, in detail, the principle of operation and gives simulation results for different switching strategies. Comparison of Multilevel Sinusoidal Pulse Width Modulation (MSPWM) is done to select a high performance MSPWM technique, while the auto-calibration technique and DC current measurement are also discussed.

Chapter 5 describes inverter synchronisation to the grid, including the proposed method used in this investigation. An explanation of DC current measurement is also included.

Chapter 6 describes the design and construction of the 240VA laboratory three-level, half-bridge inverter, and shows the practical results with, and without, a DC offset in output of DC current sensors. The auto-calibration performance is also described.

Chapter 7 concludes the research work carried out in this thesis, and points out the possible areas for further work.

1.5 Summary

This chapter has described the basic information for distributed generation systems, and provides general background on grid-connected, photovoltaic inverter system components, such as solar array, boost converter, grid synchronising methods and transformer coupling. The aim of this research is to improve the power quality of grid-connected, photovoltaic inverters, which can be done in two steps. The first step is to reduce the cost by operating the grid-connected inverter as a transformerless inverter, and the second is to improve the performance of the inverter by minimizing the DC current in the inverter output. More details will be given in the following chapters, as these issues are presented.

CHAPTER 2

DC CURRENT INJECTION INTO THE UTILITY SYSTEM

2.1 Introduction

There is an increasing use of Distributed Generation (DG) systems connected to the grid at low and medium voltage inverter levels. The output of a transformerless inverter can contain a DC current component which will be injected into the grid. Reducing this has become an important factor in the development of grid connected inverters [33]. This chapter describes the sources of DC current injection, and goes on to explain the effect of DC current injected into the utility system. This chapter also describes international standards which regulate DC current injection, and the technical methods which have been used to prevent or minimize the flow of DC current into the distribution network. Also included are all of the methods used for measuring the DC current.

2.2 Sources of DC Current Injection into the Utility System

There are many electrical application connected to the distribution network which can inject DC current into this network, such as PV grid inverters, office equipment, lighting circuits, network failures and railway suppliers [34, 35].

2.2.1 Grid Connected Inverters

Grid connected inverters can be divided into three groups according to the type of transformer they employ: low frequency transformers, high frequency transformers and transformerless, as illustrated in Figs. 2.1-2.3 [36]. Only Low Frequency (LF) transformer based converters can prevent DC current injection into the grid [37]. The other two types of grid interface are directly connected to the grid; *Myzik and Calais* [38] state that most single-phase grid connected development inverters are used in

photovoltaic systems, and that these inverters can inject unwanted DC current into the distribution network.

The source of the DC current component in these inverters is attributed to several factors; for example, small differences in semiconductor switches' characteristics, including on-state resistance and on-state forward saturation voltage. The inverter PWM switching process is affected by the on-off switching delay between PWM signals of upper and lower switches in the same leg [39]. Grid connected inverters employ current control with current sensors to force unity power factor sinusoidal current into the grid [40]. These current sensors suffer from linearity errors and offset drift [41].

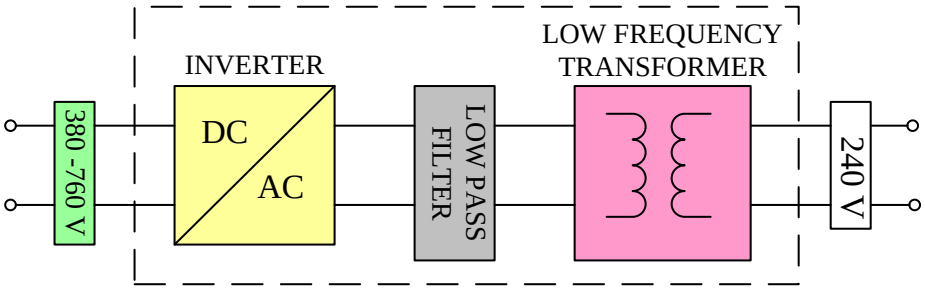


Fig.2.1: Converter topology which uses a low frequency transformer

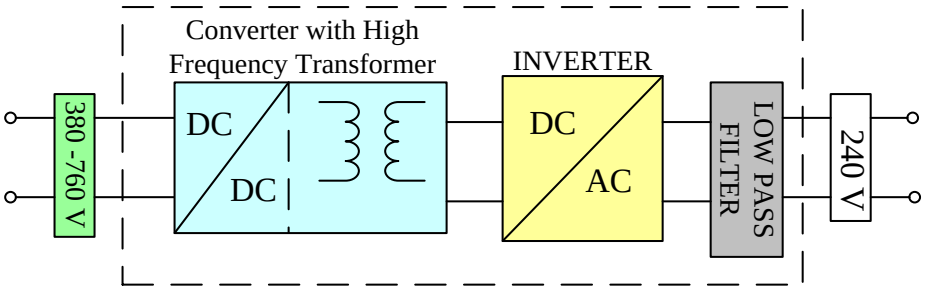


Fig.2.2: Converter topology which uses a high frequency transformer

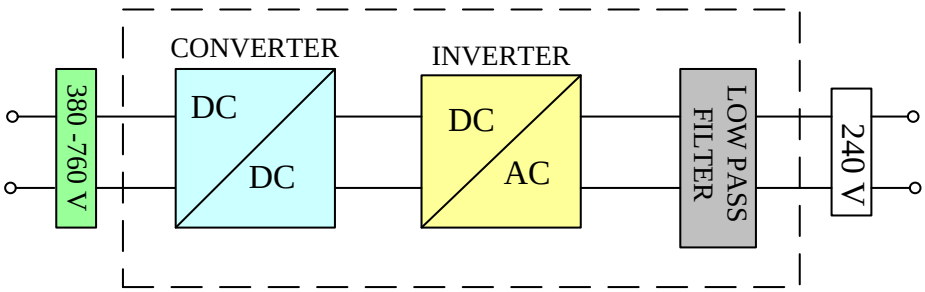


Fig.2.3: Transformerless converter topology

2.2.2 Domestic and Office Equipment

A lot of domestic and office equipment operates using a DC voltage source, including computers, lighting circuits, and laptops. Most of these devices use power converters and become sources of harmonic current including DC current, as reported by *Salas, Olias et al.* [35] and *Knight, Thornycroft et al.*[42]. The level of DC current component was measured as follows: in a laptop computer it was 0.04A DC which is 7.7% of the total rms current, in a desktop computer it was 0.03A DC which is 11.2% of the total rms current, and it was 0.34 DC (0.53% of the total rms current) from the fluorescent lighting load. The most striking result to emerge from the data was that regarding the desktop, as in many office settings such as universities, PCs are widely used which can lead to high levels of DC current entering the distribution network.

2.2.3 Other Sources of DC Current

As described in the previous section, grid connected inverters are not the only applications responsible for injection of DC current into the distribution network as there are many other sources that can produce this phenomenon such as network faults which occur in low voltage systems and geomagnetic phenomena which may cause a series of problems in transformers and electric networks. These problems include significant saturation of the ferromagnetic core, vibration, and overheating of transformers [43] (see Fig. 2.4) and electric machines such as cycloconverters and adjustable speed drives. Other sources of DC current described by *Bo Zhang, Jie Zhao et al.* [44] include using a numerical analysis method of calculating the DC current following a neutral point of substation distribution transformer in an AC power system when the HVDC system uses earth as its current return path. It was concluded that a great DC current can flow through the transformers in the AC substations if their neutral points are grounded.

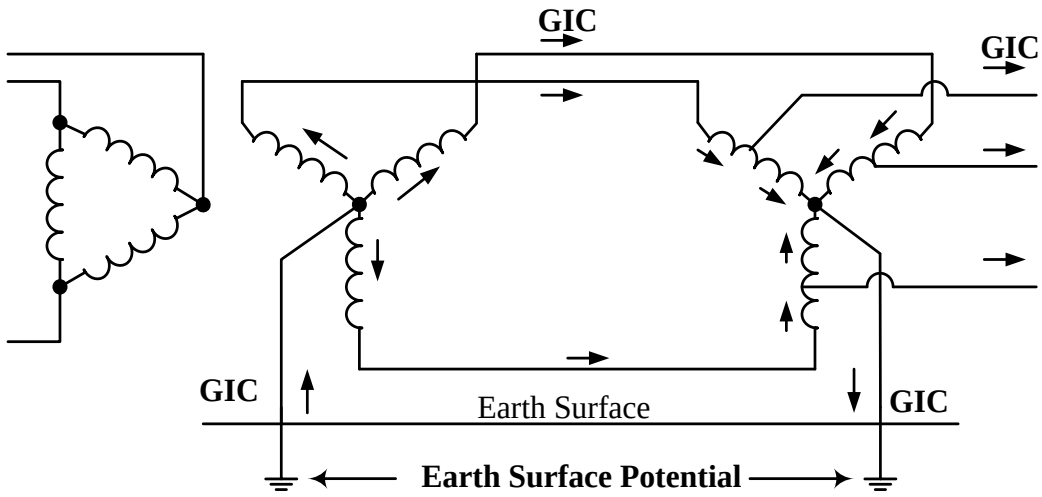


Fig. 2.4: Geomagnetically-induced current in a power system transformer

2.3 Effects of DC Current on the Distribution System

In this section, we will describe the effects of DC current in two main parts of the distribution network, namely static and rotating machines, and underground cables.

2.3.1 Distribution Transformers and the AC Electrical Machine

When DC current flows through the distribution network, it may seriously affect nearby distribution transformers and rotating machines. A small amount of DC current can shift the transformer operation point, which in turn increases the RMS magnetizing current, which may yield additional winding losses [33] [39] [45] [46]. This increase in the primary current may trip the input fuses and overheat the winding of the transformer, which can reduce the lifetime of the transformer [47].

The effect of DC current in AC electrical machine drives is similar to that in a distribution transformer. Small levels of DC current injected into the motor windings cause dynamic braking and additional losses [39]. Pulsating torque and overheating are also reported by *Sang-Bin Lee and Habetler* [48].

2.3.2 Underground Cables and Ground Equipment

Pipelines and cable sheaths are commonly used for grounding. DC current injected into the ground results in stray currents in exposed metallic structures, affecting the domestic pipelines (gas and water pipes) and cable sheaths most significantly [34, 49]. DC current flow through the buried conductors over a period of time causes problems with the contact to earth, due to corrosion of the conductor [39]. Figs. 2.5 and 2.6 [34] show the effect of DC current flow to earth in a gas pipeline and cable sheath.

Aylott [50] also reports that this is a serious concern for tramway networks, resulting in a corrosion management philosophy to minimize the corrosive effect caused by the stray DC current. *Blomberg and Douglas* [51] describe the cause and mitigation of telephone cable sheath corrosion, caused by stray earth currents from electric railways, which can be improved by using a drainage system. Finally, the corrosion effect of underground cables and other equipment is very costly; for example, from 1935-36, the replacement of telephone cables affected by corrosion cost the Post Office of the United Kingdom around £48,000 [52].

Fig.2.5: Pitting in a lead sheathed cable, caused by stray currents from railways

Fig.2.6: Failure of a gas supply pipe due to an earth leakage current

2.4 Standards and Regulations for DC Current Injection into the Grid

Due to the growing use of grid connected generation equipment in recent years [53], regulations have been required to achieve a minimum standard of power quality. Among these standards and recommendations, the limitations of DC on allowable current injection into the distribution network varies from country to country, so there are different considerations depending on the grid type [54] [35]. Table 2.1 shows guideline standards and regulations to limit the DC current injected into the distribution network in various selected countries [55].

Table 2.1: Limitations of DC current injection into low DG with and without a transformer in the selected country

Country	Standard	Maximum DC current permitted with transformer	Maximum DC current permitted without transformer
Australia	AS4777.2	5 mA	5 mA
Austria	ÖVE/Önorm E 2750	No limit set	No limit set
Denmark	EN 61000-3-2	No limit set	No limit set
Germany	DIN VDE 126	No limit set	1000 mA
Italy	CEI 11-20	No limit set	No limit set
Japan	JIS C 8980	1 % inverter rated power	1 % inverter rated power
Netherlands	EN 61000-3-2	No limit set	No limit set
Spain	RD 1663 / 2000	No limit set	No limit set
UK	G 83/1	No limit set	< 20mA
USA	IEEE 929-2000	0.5 % rated power inverter	0.5 % rated power inverter

As can be seen from the table above, the regulation of DC current injection into the grid varies from country to country, highlighting the need for common international

standards for power quality. In this study, the guidelines of the United Kingdom G83/1 [56] will be used as references.

2.5 Methods to Minimize DC Current Injection into the Grid

In this section, the methods for minimizing DC current injection into the distribution network will be discussed. Several methods have been examined. The basic approach is to make use of an isolating transformer. Another technique is to use a half-bridge inverter which has the capability of blocking the DC current flow into the AC side. It is also possible to use a DC blocking capacitor in the inverter output. A more recent method is to use current sensing and control techniques to monitor and calibrate the DC link current sensors.

2.5.1 The use of an Isolating Transformer

The traditional and common method for preventing DC current injection into the grid is through the use of a low frequency transformer, as shown in Fig. 2.7. This transformer has the advantage of providing galvanic isolation between the photovoltaic system and the grid. When no transformer is used, the connection between the array and the ground will be through stray capacitance [57], so the common mode current injection into the ground is only limited by stray capacitance and converter common mode impedances (EMI filter). From that, the transformer is very limiting for a common mode current to flow [58].

Additionally, the transformer can also be used to step up the output voltage of the inverter to match the network voltage. The main disadvantage of using an isolating transformer is the increased cost, weight and physical size of the photovoltaic system, and the lower system efficiency. This encourages research into other transformerless approaches. *Calaisa and Vassilios et al.* [59] estimate the cost of the transformerless PV inverter system as being less than the cost of the system with a transformer by as much as 25%.

Furthermore, the power losses will be reduced in the transformerless case. System efficiency with a mains transformer is reduced by 1.5-2% due to the transformer

power losses. The power losses and efficiency were studied by *Haeberlin* [19] from 1989 to 2000 for different inverter applications in grid connected PV systems. *Kerekes and Rodriguez et al.* [60] described a new high efficiency single-phase transformerless topology; this approach increased the transformerless efficiency by 1-2% when compared with a conventional grid connected method.

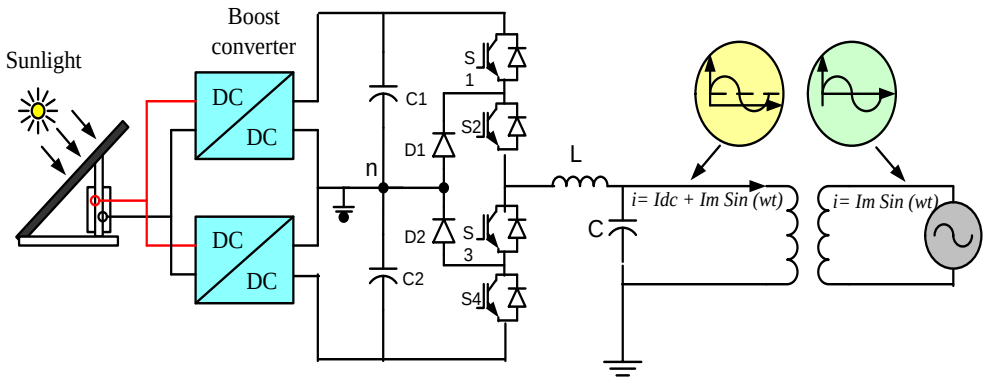


Fig. 2.7: Isolating transformer to prevent DC current inject into the network

2.5.2 The use of a Blocking Capacitor on the DC Side

A common method used to block DC current injection into the distribution network without using a line frequency transformer is a single-phase half-bridge inverter [61] [62] [63] [64]. This circuit is effective because the connecting path of the positive and negative output current is always via one of the capacitors, as shown in Fig.2.8. The main disadvantage of a single-phase half-bridge inverter is the need for a high input DC link voltage of around 800 Vdc to achieve the desired output voltage level of $230V_{rms}$ [40]. This requires 1200V IGBTs switches to be used, compared with the 600V IGBT switches used in a conventional full bridge inverter. As a result of that, the switching losses will be increased and the inverter efficiency will be reduced [65]. *Gonzalez et al.* [66] proposed a new high efficiency topology for a transformerless system, and demonstrated that the half-bridge inverter causes a large current ripple and high switching losses, thus reducing the efficiency of the inverter.

Another problem facing the transformerless half-bridge inverter is that the boost converter duty ratio must be doubled to step-up the low array voltage (50-100V) to the desired level for the DC side of the inverter [67]. Also, the voltage rating of components such as switches and capacitors must be doubled to account for a higher DC bus voltage. Therefore, as a result, the overall cost will increase.

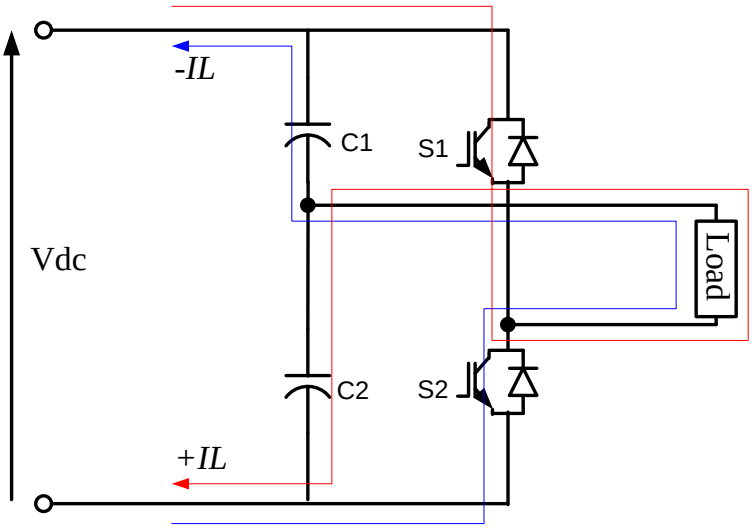


Fig.2.8: Half-bridge inverter

2.5.3 The use of a Blocking Capacitor on the AC Side

As mentioned previously, the use of blocking capacitors is a simple method for preventing DC current injection into the grid for transformerless PV systems, due to their low cost as compared with an LF transformer. *Blewitt et al.* [68] proposed a method using a clamped and offset electrolytic capacitor to prevent DC current injection into the distribution power network. This type of capacitor (aluminium electrolytic capacitor) has advantages such as a low cost and small size compared with an AC capacitor. On the other hand, the AC capacitor reactance depends on the value of the capacitor (µF), so for a high value of the AC capacitor, the capacitive reactance will be quite low; therefore, the size of this capacitor will be large and it will become very expensive. Consequently, the benefit of using a transformerless inverter is not achieved.

Fig.2.9 shows the blocking capacitor technique placing in the inverter output current path, to prevent the DC current injection into grid. This technique uses a clamped diode to prevent any damage caused by reverse polarisation. It can be observed that the clamped diodes are connected in parallel with the block capacitor.

This method was capable of limiting DC current injection into the distribution network to 5mA. This result meets the UK standard recommendation [56].

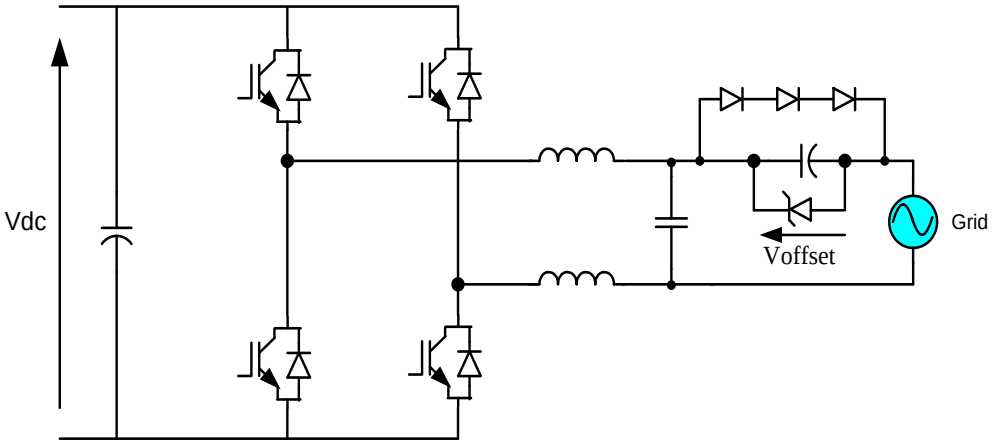


Fig.2.9: Single-phase grid connected inverter using an AC block capacitor

Xiaoqiang et al. [69] also developed a method to prevent DC current injection into the grid, by replacing a capacitor which could block the DC current on the AC side with a novel control strategy to achieve a zero steady-state error control. This proposal was carried out under three assumptions. Firstly, the DC bus voltage was constant. Secondly, it was assumed that the switching frequency was sufficiently high to have a negligible effect on the inverter control loop dynamics. Thirdly, the system controller would not saturate the inverter output, and the grid-connected inverter operated as a liner system. Theoretical analysis and simulation results demonstrated that the DC current injection was minimized below the requirement of the IEEE standard [70].

2.6 Current Sensing and Control Techniques

Current sensors and associated control techniques have been used to minimize the DC current injection into the distribution power network. The problem with these techniques is related to the DC current mixing with the sinusoidal current in the inverter output, as described by *Kitamura et al.* [46], and *Masoud and Ledwich* [45]. If the DC current component can be measured, it is possible to compensate using current control. Once again, the allowable DC current component depends on regulations in the country in which the equipment is to be used. The current sensor and control techniques may be satisfactory for some countries but not for others, due to the lack of a uniform international standard around the world. In this research, the UK Engineering Recommendation G83/1 will be considered as the reference for limiting the DC current injection.

2.6.1 Overview of DC Link Current Sensor measurement techniques

A DC link current sensor has commonly been used in power electronic drives and applications as described in [71] [72]. *Armstrong et al.* [67] proposed a method of continuously calibrating the current sensor in an H-bridge inverter system. *Bojoi, Caponet* [73] studied the DC link current of a six-phase inverter system, and found that the capacitor value is a function of DC link current. *Atkinson* [74] also explained a new control technique for a three-phase motor using a single DC link current sensor. *Filanovsky et al.* [75] used a transformer and RL-multivibrator for sensing and measurement of DC current, and concluded that the circuit can be used as a DC current sensor with an isolation gap. There is a variety of types of current sensors available for power applications [76]. Sensors based on the Hall Effect are very common, because they offer good dynamic performance, natural isolation and low cost. A disadvantage of this type of current sensor is its linearity errors and offset drift [41], which affect the accuracy of current control performance, and may introduce harmonic distortion and DC offset in the output current[67].

2.6.2 Current Measurement Techniques

In this section, several proposed methods for DC current reduction using different types of current transducer will be outlined [77] [78] [79]. For that reason, a review of current sensing device types, such as the Hall effect current sensor [76], the Rogowski coil [80] and other current measurement techniques, will be described in the following sections.

2.6.3 Hall Effect Current Sensors

Hall effect current sensors are widely used in power electronic converters, due to their low cost, small size, provision of galvanic isolation and large bandwidths ranging from the DC up to 200 kHz [81]. In the Hall effect sensor, a current is passed through a semiconducting material which is placed into a magnetic field, as shown in Fig. 2.10, resulting in a Lorentz force being exerted on the current. This force disturbs the current distribution, causing a concentration of charge carriers on one side of the material, resulting in the generation of a small voltage known as the Hall voltage (V_H). This voltage is proportional to the current (I_C) flowing in the semiconductor material and the magnetic field density (B).

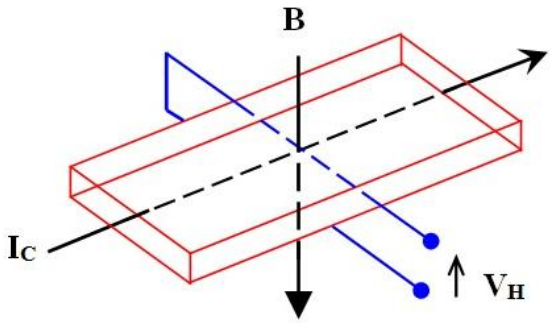


Fig. 2.10: Hall voltage generated (V_H), I_C = current flowing, B = magnetic flux density

There are different sensing configurations of the Hall effect current sensor, namely open loop and closed loop. The open loop configuration illustrated in Fig. 2.11 (a) provides a simple form of the Hall effect sensor. The output of the sensor is connected to the amplifier to increase the low signal level of the Hall voltage. The open loop current sensor has several disadvantages, such as susceptibility to stray external magnetic fields, measurement accuracy affected by a sensitivity factor value, and suffers from the magnetic core loss which rises to the frequency and input current.

The second configuration is the closed loop Hall effect current sensor, which is shown in Fig. 2.11 (b). This type of current sensor is an improvement on the open loop current sensor. A wire coil is wrapped around the core to produce an opposing magnetic flux to that generated by the conductor. This will result in the total magnetic flux in the core being driven to zero. In this case, the current in the secondary winding is an exact image of that flowing in the primary conductor, with an integer ratio defined by the number of turns. The Hall effect closed loop current sensor has several advantages compared with the open loop; it has a very fast response linearity better than 0.1%, and the core losses are significantly reduced [82].

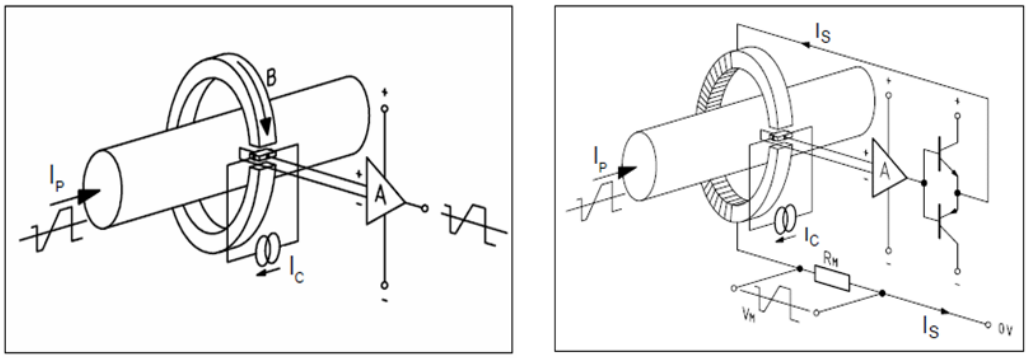


Fig. 2.11: (a) Open Loop Current Sensor, (b) Closed Loop Current Sensor

2.6.4 Current Transformers

The current transformer is a traditional approach to current measurement in protection applications. It provides isolation in the measurement circuit, and a wide bandwidth up to 1MHz [83]. The current transformer consists of a single primary winding which is connected in series with the conductor carrying measured current and a multiple secondary turns wound evenly around the torroid. A burden resistor is required, as illustrated in Fig. 2.12. The current transformer terminal voltage across the external burden resistor can be determined by the following equation [84]:

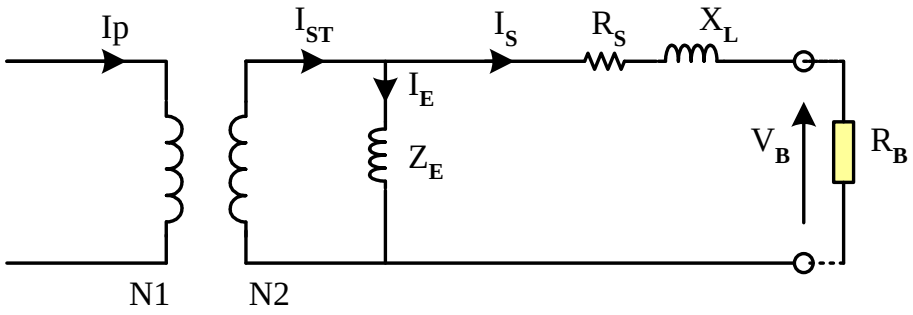


Fig. 2.12: Simplified equivalent circuit of a current transformer

$$V_B = \frac{I_P}{N} R_B \tag{2.1}$$

where $I_P = \left(\frac{N_2}{N_1}\right) \times I_{ST}$

The current transformer is capable of measuring the pulse current up to 5000A, with a 20ns rise time. Primary and secondary windings are insulated from each other and from the core. A disadvantage is that the current transformer can have accuracy limits, because in practice the current measurement ratio is not equal to the ratio between the primary and secondary windings. Many compensation methods have

been proposed to improve the accuracy [85-87], including digital compensation methods.

2.6.5 Rogowski Current Transducers

The Rogowski current transducers, also known as air-cored coils, have been in use since 1912 [88]. The device consists of a number of turns of wire wrapped around a non-magnetic material, and formed into a closed loop as illustrated in Fig.2.13. The basic principle operation of the Rogowski coil is based upon Faraday's law, which states that "the total electromotive force induced in a closed circuit is proportional to the time rate of change of the total magnetic flux linking the circuit".

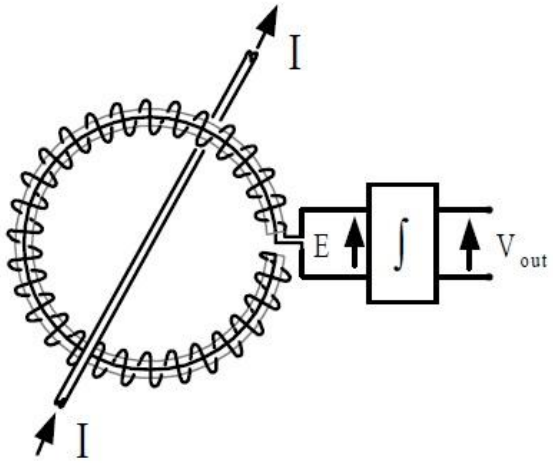


Fig.2.13: Schematic Rogowski current transducer

The current varying in the wire will induce a voltage in each turn of the coil, and can be defined by the following equation:

$$E = \mu_0 N A \frac{dI}{dt} = H \frac{dI}{dt} \quad (2.2)$$

where N is the number of turns (turn/m), A is the cross-sectional area of the non-magnetic material (A m^2), and I is the current to be measured passing through the loop.

The induced voltage in equation (2) must be integrated to obtain the V_{out}, which is proportional to the rate of change of the current flowing in the wire [80]. The Rogowski coil has several advantages, such as ease of use, a high linear current range up to 100kA, the provision of galvanic isolation from the primary conductor, and a typical frequency range of around 10MHz [89] [90]. This type of current transducer is not commonly used as a measurement device in power electronic applications such as a Hall effect device, and is mostly found as a current probe. Unlike the Hall effect current sensor, the Rogowski transducer does not measure the direct current component.

2.6.6 Current Shunts

A current shunt resistor is one of the most sensitive methods used to measure AC or DC electrical currents in different applications, by applying Ohm's law to calculate the current when knowing the resistance of the shunt. This approach does not suffer from linearity errors seen in the Hall effect sensor. It also provides high reliability and non-inductive performance. A disadvantage is a lack of galvanic isolation between the power circuit and the measurement circuit. This shunt is also a source of power loss (I^2R_{shunt}), where (I) is the current flow through shunt resistance and (R_{shunt}) is the value of the shunt resistance [82]. Fig. 2.14 shows the connection of the shunt resistance as a measurement device.

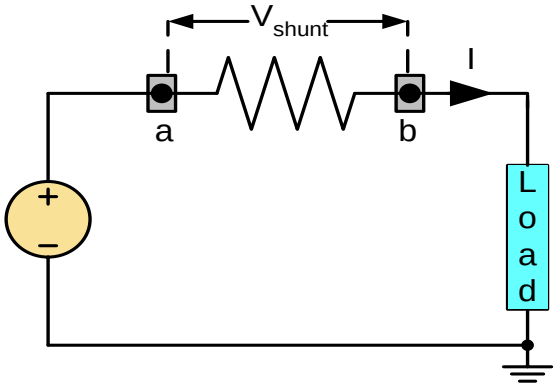


Fig. 2.14: Shunt resistor method for current measurement

If low values of resistance are chosen (such as $0.50m\Omega$), then the losses can be minimized [91]. Therefore, it is possible to minimize the power losses, particularly in grid-connected inverters, where efficiency is an important design consideration. The consequence is that the smaller value of the shunt resistor results in a smaller voltage appearing across the shunt. This will affect the measurement resolution and accuracy, due to noise levels which in some cases become greater than the measured signal (millivolt or less). In this case, a high common-mode rejection shunt amplifier is needed to attenuate unwanted noise and achieve a pure signal.

The resistive shunt current measurement technique has been used to measure a small DC current mixed with a large AC current, by connecting an RC filter across the shunt and using a battery operated Digital Multi-Meter (DMM) to measure the DC voltage, as described in section 5.7

2.7 Novel DC Current Sensor Technologies

The method first introduced by *Sharma* [77] demonstrated how the sensor is connected to detect a small level of DC current in the H-bridge grid-connected inverter. The scheme consisted of a small 1:1 voltage transformer (VT) and an RC circuit, as illustrated by Fig. 2.15. The RC circuit was connected in series with the secondary side of the VT, and the primary side was connected across the grid voltage. The assumption was made that the turns ratio of the VT was perfect (exactly 1:1). In this case, only the DC offset appeared across the capacitor in the RC circuit. This offset voltage was fed back to the PI controller, which in turn adjusted the inverter current reference, resulting in the DC offset being eliminated. However, there was no experimental validation for this work.

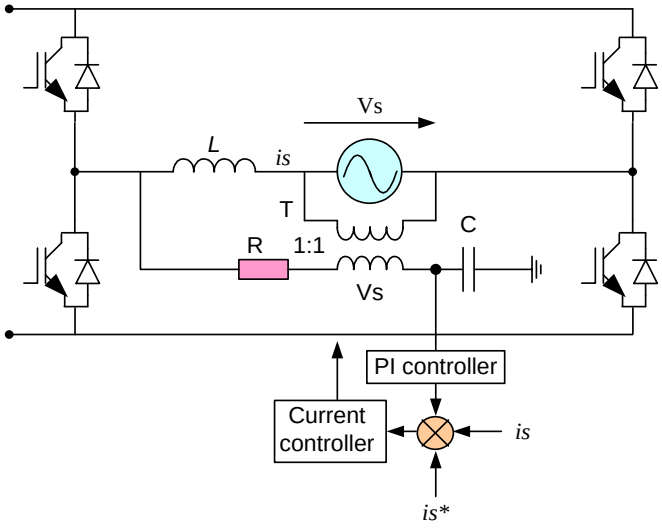


Fig. 2.15: DC offset current control loop

Ahfock and Bowtell [78] studied this method and produced a mathematical model-based controller using the output sensor to drive a feedback system designed to eliminate the DC offset. Fig. 2.16 shows their proposed method using a mutual coupled inductor in series with the inverter output to monitor the DC voltage (V_2), which was proportional to the DC current flowing in the primary winding of the VT. A slowly tuned PI was used to adjust the inverter DC offset to remove the DC current component in the inverter output [77]. A practical result was achieved through this work, but the major problem facing this technique was the size of the inductor core and the significant amount of copper for mutually coupled windings, resulting in additional power losses.

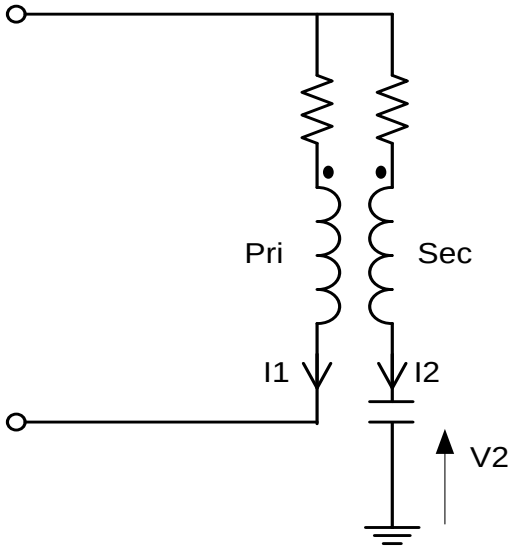


Fig. 2.16: Novel DC current sensor using a mutual coupled inductor

Again, *Ahfock and Bowtell* [92] [93] studied the mutual coupled inductor DC current sensor, and evaluated the previous proposal by connecting the DC offset sensor across the ripple filter, instead of connecting it across the AC supply. In this case, the DC offset sensor was also redesigned and was made up of a two-stage RC filter. This technique successfully reduced the DC current offset to an acceptable level

Buticchi and Bellini et al. [79] proposed a new method to detect and compensate for the DC current in the output with a transformerless full-bridge inverter, by compensating for the DC voltage in the inverter output, which was proportional to the DC current offset. This work was different from that described in [77, 93], where the DC sensor was connected across the AC supply terminals or across the ripple filter inductors. For this method, the compensation DC offset sensor was connected across the inverter terminals and consisted of a magnetic circuit which was implemented with a low power toroidal transformer.

An LC pass filter was inserted between the inverter, the reactor and a closed loop Hall effect sensor, as illustrated in Fig. 2.17. The principle of operation is based on the saturation of the reactor, when the DC voltage appeared at the output of the converter, resulting in distortion in the reactor current. For this scheme, two assumptions were made to achieve good accuracy. Firstly, the magnetic core working voltage needed to be very close to magnetic saturation. Secondly, to operate the reactor as a DC voltage detector, it needed to be in a close loop condition.

Experimental results were obtained and the DC current component was kept below 10*m*A. This was within the limits imposed by some standards such as the United Kingdom (G83/1). But, it was not in compliance with others such as the IEEE P929 in the US.

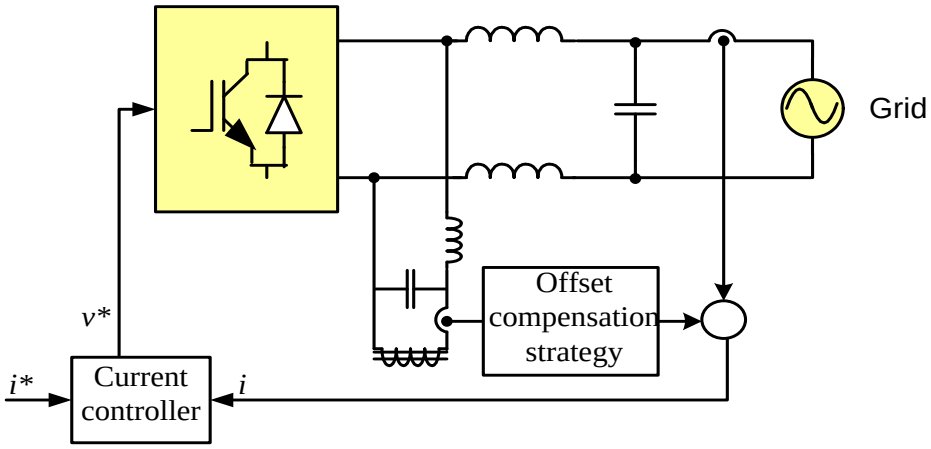


Fig. 2.17: Schematic of the offset compensation strategy

Sonoda, Ueda and Koga [94] presented a high accuracy DC and AC current sensor using zero-flux principles for the flux-gate, and closed loop Hall effect-based magnetic current transducers (the flux-gate principle used a saturable inductor for sensing the field produced by an external current [95]). The accuracy of the proposed sensor was greater than 0.01% for the full range of 20A. However, the bandwidth was limited to a few hundred hertz, and was therefore considered to be unsuitable for current control in grid connected inverters, where bandwidths of tens of kilohertz were commonly used.

2.8 Auto-Calibrating the Current Sensor for the H-Bridge Inverter

The first calibration techniques used to compensate the DC offset current injection into the grid using a DC link current sensor were introduced by *Armstrong et al.* [67]. This is achieved by placing the current transducer between the DC link capacitor and inverter switches, as illustrated in Fig. 2.18. The DC link current sensor is used to

measure the DC link current for the proposed estimation of the output current. The technique depends on knowing the operational state of the inverter. A connecting state is where the output current flows to the load via the DC link sensor, as opposed to a freewheeling state, where no current flows in the sensor. During the freewheeling states, where the current measured by the DC link current sensor collapses to zero, the current sensor output can be sampled and used to remove any offset current present.

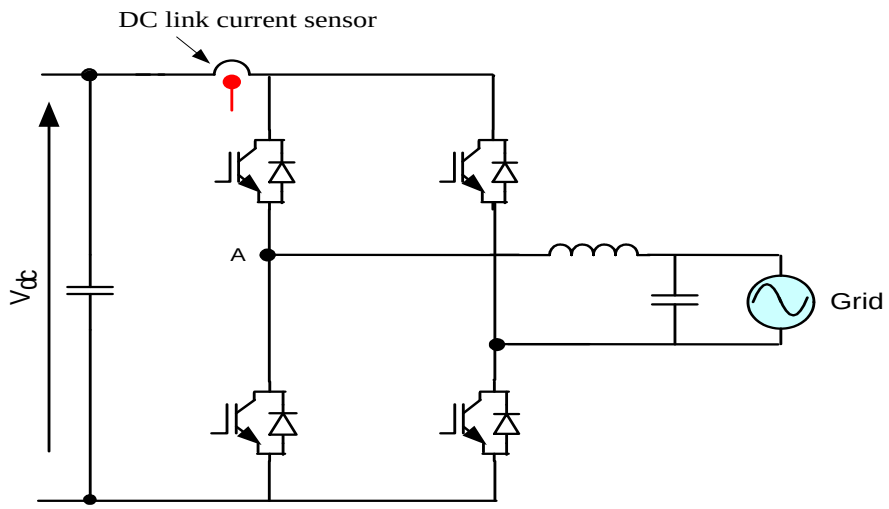


Fig. 2.18: H-bridge inverter using a DC link current sensor

Experimental results were obtained, and the auto-calibration technique shown to be capable of limiting the DC current component below 8.63*m*A for a 10A, 50Hz current component in the inverter output. This method provides the possibility of connecting the inverter without the need for a power transformer for operating as a transformerless grid connected system.

2.9 Summary

This chapter reviews the main sources of DC current injection into the distribution network. It also explains the effects of DC current in distribution network equipment, such as a distribution transformer, AC electrical machines and underground cables. International standards associated with DC current injection have been considered, and the guidelines of the United Kingdom (G83/1) and the United States of America (IEEE P929 Standard) have been selected as references in this thesis. This chapter highlights a review of most types of current sensing devices, such as Hall effect sensors, shunt resistance and current transformers. The Hall effect current sensor is the most recent used in power electronic application circuits, due to good performers providing galvanic isolation and low costs.

This chapter has also considered a number of methods used to minimize or prevent DC current injection into the distribution network. This includes an isolation transformer, a half bridge inverter and a blocking capacitor in the inverter output. The advantages and disadvantages of these topologies have been discussed. In addition, several methods of current sensing and control to minimize the DC current on the AC side for single-phase grid connected inverter topologies have been described.

CHAPTER 3

MULTI-LEVEL INVERTERS

3.1 Introduction

This chapter presents an overview of multilevel inverter (MLI) topologies. The first section describes the general structure and operation of MLIs, including the advantages and disadvantages of these types of inverter. The second section compares three basic multilevel inverter topologies. The final section represents the alternative multilevel inverters topologies.

3.2 Multilevel Topologies

Multilevel inverters are commonly used in a wide variety of applications, including motor drives and utility applications, at medium voltage and high power levels [96, 97]. A multilevel inverter can also be used in renewable energy systems based on photovoltaic, wind and fuel cells, to interface with the power distribution system [98-100]. The first multilevel inverter circuit was introduced more than 35 years ago [101], the first development beginning with a three-level inverter.

The aim of a multilevel inverter is to achieve a high quality voltage waveform by using a number of series switches with several lower voltage DC sources, to generate a number of staircase voltage waveforms. Theoretically, an inverter with an infinite number of levels could produce an ideal sinusoid waveform. However, as the number of levels increases, the switching control becomes more complex.

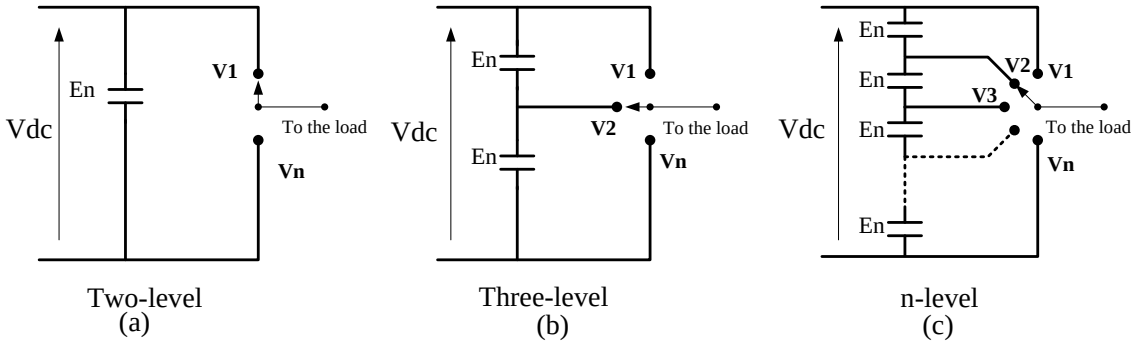


Fig. 3.1: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

Fig. 3.1 shows a schematic of a multilevel inverter with a number of different levels. A two-level inverter produces an output voltage with two levels, with respect to the negative terminal of the DC link capacitor, while the three-level produces three voltage levels, and so on, as reported by *Jose et al.* [102].

The series connected capacitors shown in Fig. 3.1 are assumed to have equal voltage. The voltage across each capacitor, E_n, can be calculated from the following equation [103, 104]:

$$E_n = \frac{V_{dc}}{n-1} \tag{3.1}$$

where n is the number of levels adopted.

There are several advantages with a multilevel inverter when compared with a traditional (two-level) inverter [102]:

- The staircase voltages produce by multilevel inverters lead to a high power quality and reduce the *dv/dt* stresses; as a result, the electromagnetic compatibility (EMC) problems can be reduced.
- The multilevel inverters can draw current with a lower distortion level.
- The common-mode voltage produced by multilevel inverters is noticeably small, and as a result, stress in the motor bearings is reduced [105, 106].

- A specified waveform quality can be achieved at a reduced switching frequency when compared with a two-level inverter. This results in a lower switching loss and increased efficiency [57].

Multilevel inverters also have some disadvantages:

- Although a large number of semiconductor switches are required in multilevel inverters, the cost of those devices will be low due to a lower voltage rating compared with the two-level inverter. However, each device needs a gate drive circuit, and this will affect the cost and layout of the circuit design.
- Control is complicated when the number of levels is increased.
- A multilevel inverter suffers from unbalanced DC link capacitor voltages, so an additional balancing circuit is required for application with a single DC input.

Three different topologies of multilevel inverters have been proposed in industrial applications: diode clamped (neutral clamped) [57, 107], capacitor clamped (flying capacitor) [108, 109] and a cascaded H-bridges multilevel inverter [102, 110].

3.2.1 Diode Clamped Multilevel Inverters

The Diode Clamped Multilevel Inverter (DCMI) is one of the most commonly used types of multilevel topologies [111, 112]. The diode clamped inverter can also easily be extended to more levels in half-bridge or full-bridge inverters, for single-phase or three-phase applications.

Fig. 3.2 shows the topologies of three-level and five-level diode clamped multilevel inverters. The three-level topology was introduced by *Nabae et al.* [107] in 1981, and is also known as the neutral point clamped (NPC) inverter. In recent years, several researchers have published articles which have included an analysis of multilevel inverters, in order to further reduce harmonic components of the output voltage and current [113]. These topologies have higher voltage levels and are derivations from the three-level topology, by adding more switching devices and capacitors in series

with the fundamental circuit. Consequently, as the number of levels is increased, more steps are added to the output waveform, producing a staircase wave which is roughly sinusoidal in shape [104, 114]. The control circuit at higher levels becomes more complex and requires a voltage balancing circuit [115].

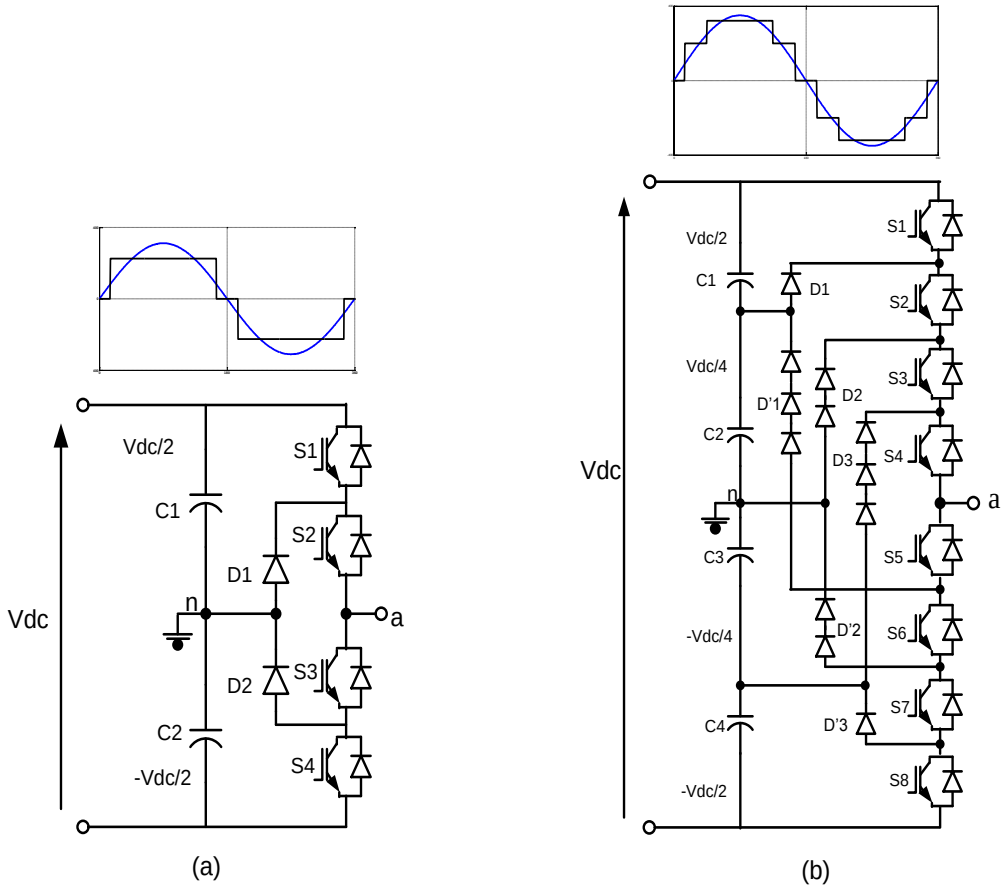


Fig. 3.2: Diode clamped multi-level inverter, (a) three-level and (b) five-level.

The operating states of three-level half-bridge and five-level half-bridge diode clamped inverters are explained below. Table 3.1 shows the output voltage of a three-level half bridge which has three switching states ($V_{dc}/2$, *0 and* $-V_{dc}/2$); the two voltage states are achieved by switching the two upper and/or two lower devices on. The third state is obtained by switching S_2 and S_3 on, as illustrated in Fig. 3.3.

Table 3.1: Switching states and output voltages of a three-level HBDC inverter

State number	Switching states				Output voltage V_{an} (V)
	S_1	S_2	S_3	S_4	
1	1	1	0	0	$V_{dc}/2$
2	0	1	1	0	0
3	0	0	1	1	$-V_{dc}/2$

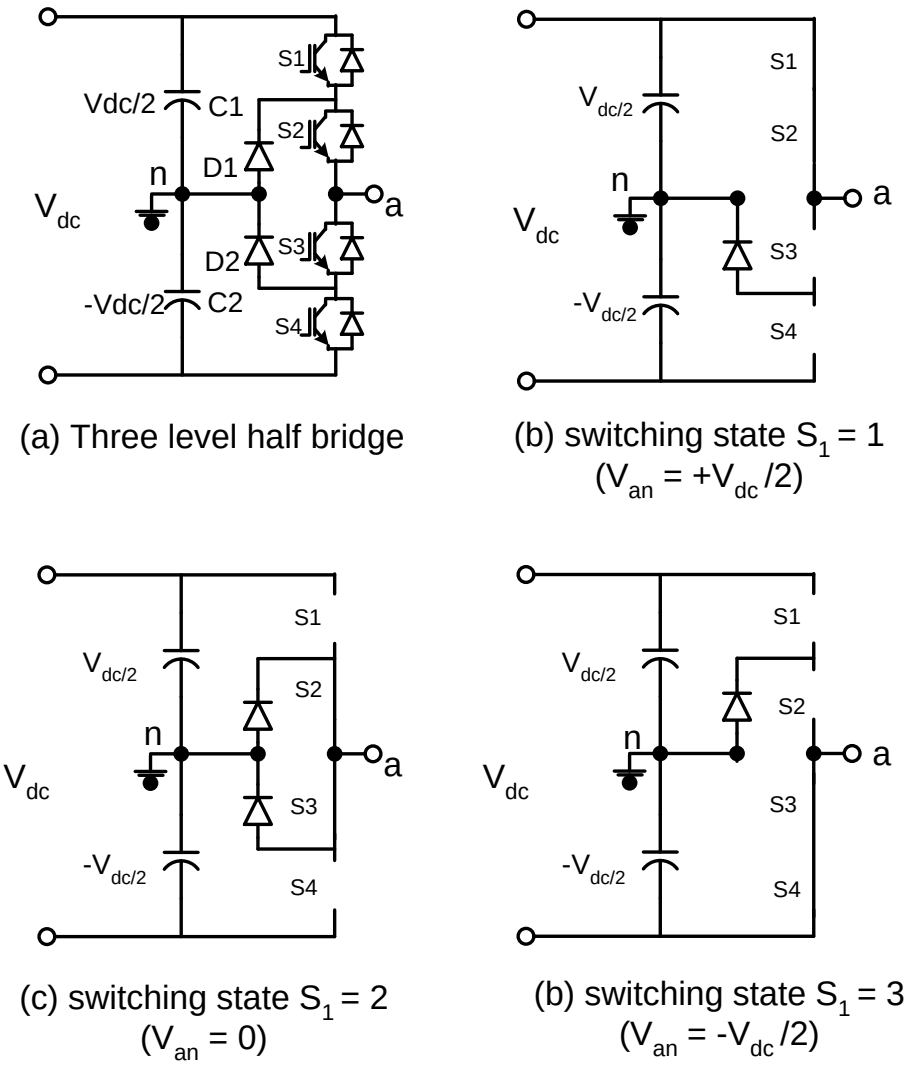


Fig. 3.3: Switching states of a three-level HBDC inverter

Fig. 3.4 shows a MATLAB SimPower Simulation model of the five-level, half-bridge diode clamped inverter. This inverter is controlled using sinusoidal PWM. The switching states of the inverter are presented in Table 3.2.

Fig. 3.5 shows the corresponding terminal inverter voltage waveforms. Fig. 3.6 illustrates the output voltage and current waveforms (resistive load) of a five-level HBDC inverter topology. Only 5 of 16 possible states are used to produce the output voltage for a five-level inverter topology, and the other 11 switching states are known as redundancy states. The voltage level blocked by each switching device is obtained using the following equation:

$$\frac{V_{dc}}{(m-1)} \tag{3.2}$$

The number of clamping diodes required for each phase leg to get the same blocking diode voltage rating as the switching device voltage rating is calculated using the following equation:

$$(m-1)\times(m-2) \tag{3.3}$$

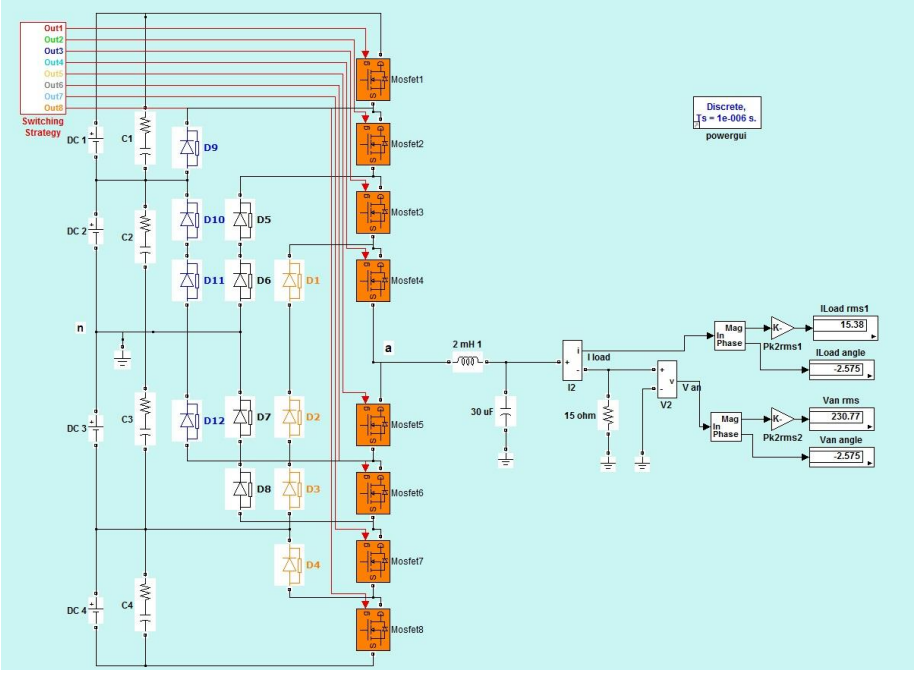


Fig. 3.4: Five-level half-bridge inverter MATLAB/SimPower models

Table 3.2: Switching states and output voltages of a five-level HBDC inverter

State number	Switching states								Output voltage V_{an} (V)
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	1	1	1	1	0	0	0	0	$V_{dc}/2$
2	0	1	1	1	1	0	0	0	$V_{dc}/4$
3	0	0	1	1	1	1	0	0	0
4	0	0	0	1	1	1	1	0	$-V_{dc}/4$
5	0	0	0	0	1	1	1	1	$-V_{dc}/2$

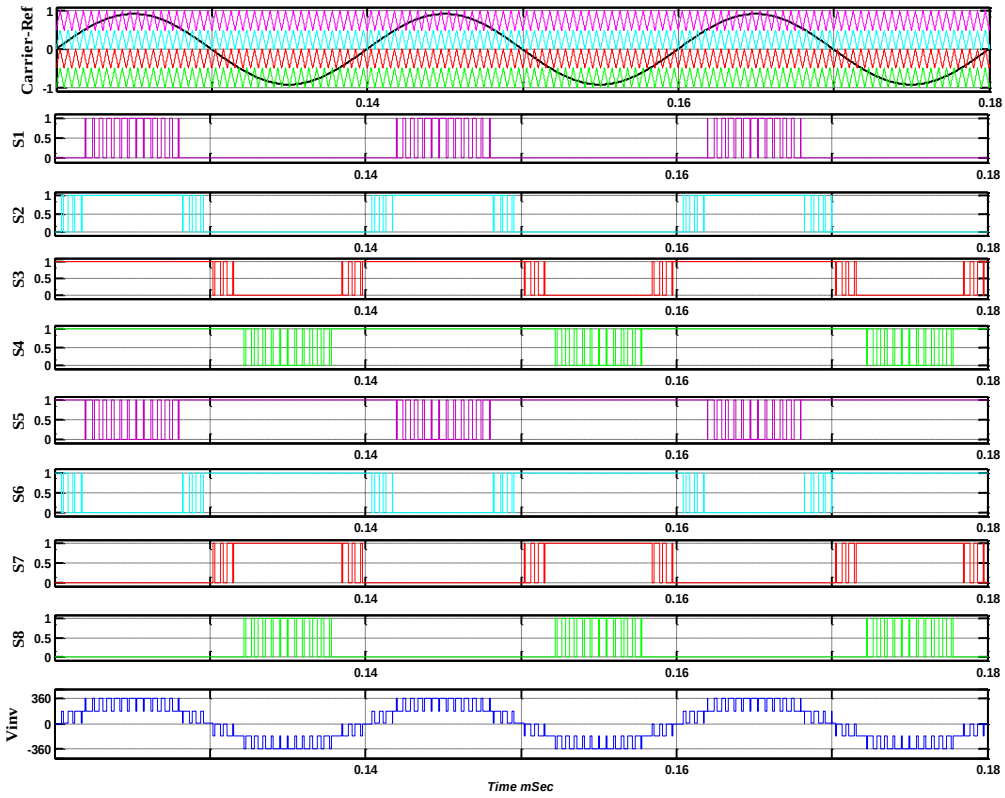


Fig. 3.5: Switching states and the terminal inverter voltage waveform of a five-level HBDC inverter. $m_a = 0.95$, $f_c = 2000$ Hz, $f_m = 50$ Hz

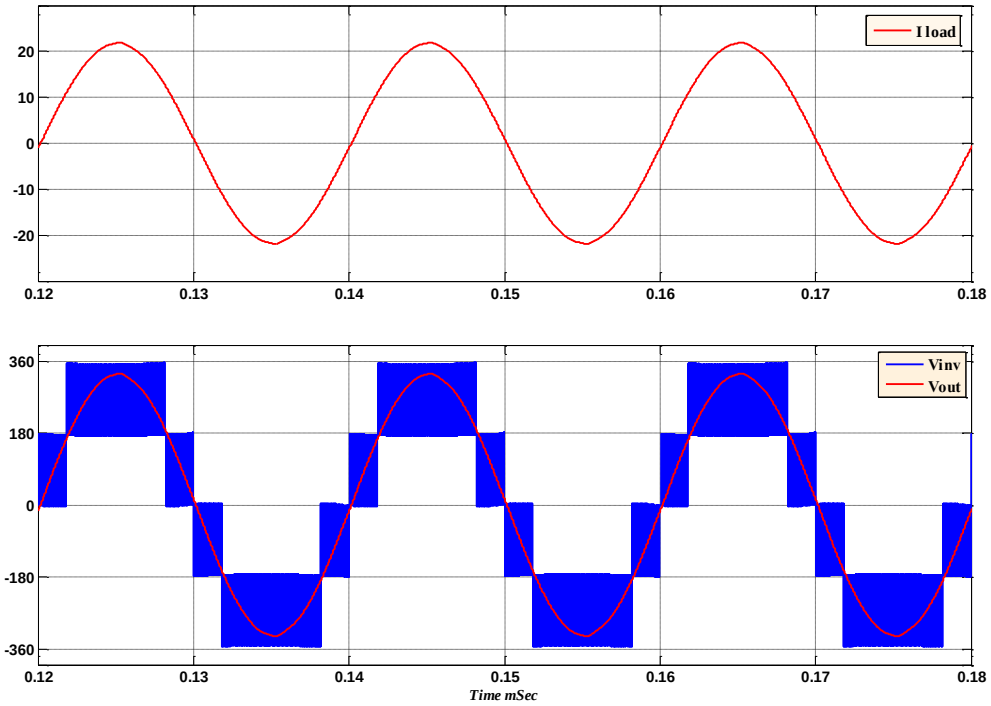


Fig. 3.6: Output voltage and current of resistive load of a five-level HBDC inverter $m_a = 0.95$, f_c = 2000 Hz, f_m = 50 Hz

Fig. 3.7 shows a MATLAB SimPower Simulation model of the three-phase three-level diode clamped inverter. This inverter is controlled using sinusoidal PWM. As can be seen that in Fig. 3.8, the positive or negative DC link current in each phase has opportunity for applying the auto-calibration techniques to minimize DC offset in this inverter.

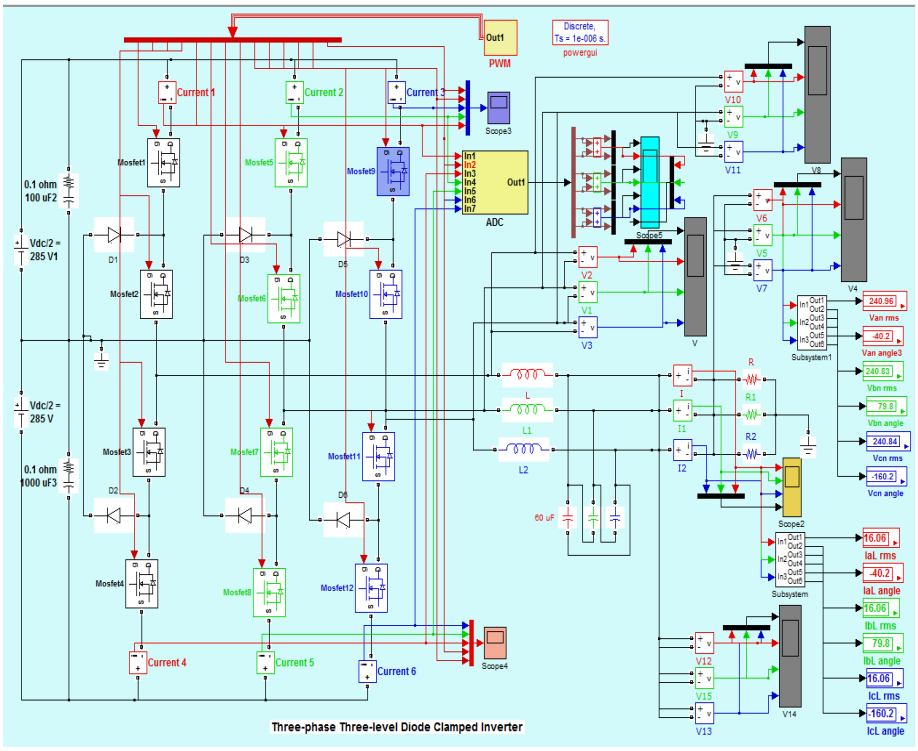


Fig. 3.7: Three-phase three-level inverter MATLAB/SimPower models

.

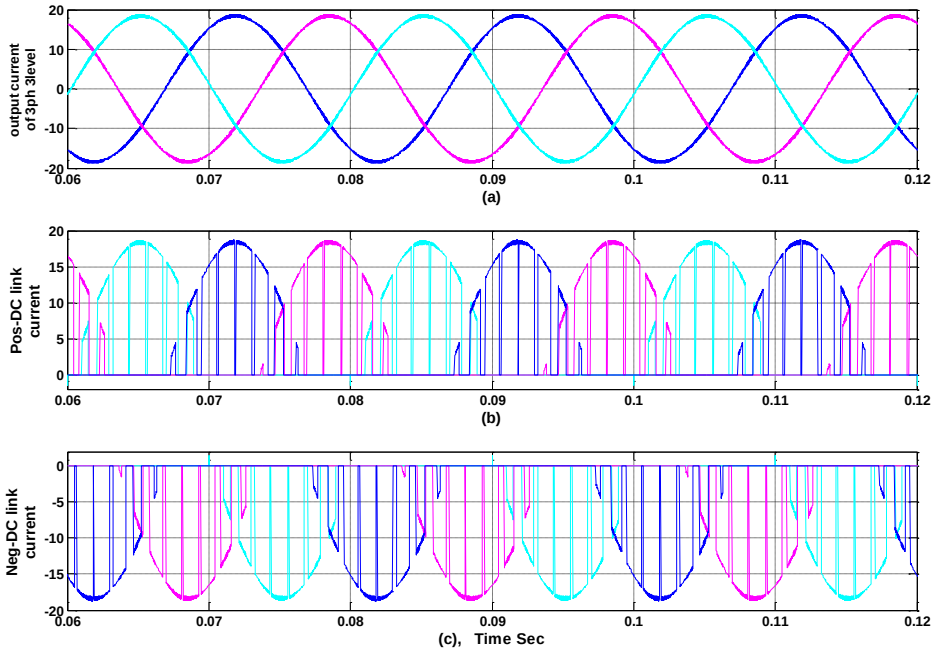


Fig. 3.8: (a) 3Ø output line current, (b) 3Ø positive DC link current and (c) 3Ø negative DC link current

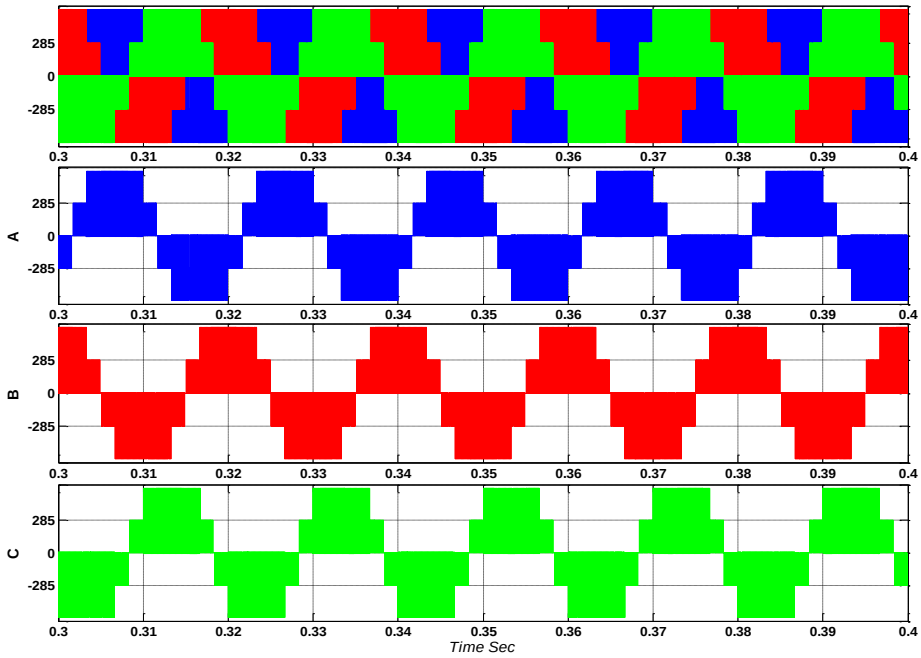


Fig. 3.9: Line to line terminal inverter voltage for 3Ø, 3-level inverter

3.2.2 Capacitor Clamped Multilevel Inverter

Fig. 3.10 illustrates the fundamental building block of a phase-leg capacitor clamped multilevel inverter, which is also known as a flying capacitor inverter (FCI). This topology is similar to the diode clamped topology in terms of the output voltage, but the voltage generated by a flying capacitor inverter has more flexibility when compared with a diode clamped converter, as reported by *Jih-Sheng et al.* [109]. Moreover, the main advantage of this topology is that it has phase redundancies when compared with a diode clamped inverter, which only has line to line redundancies.

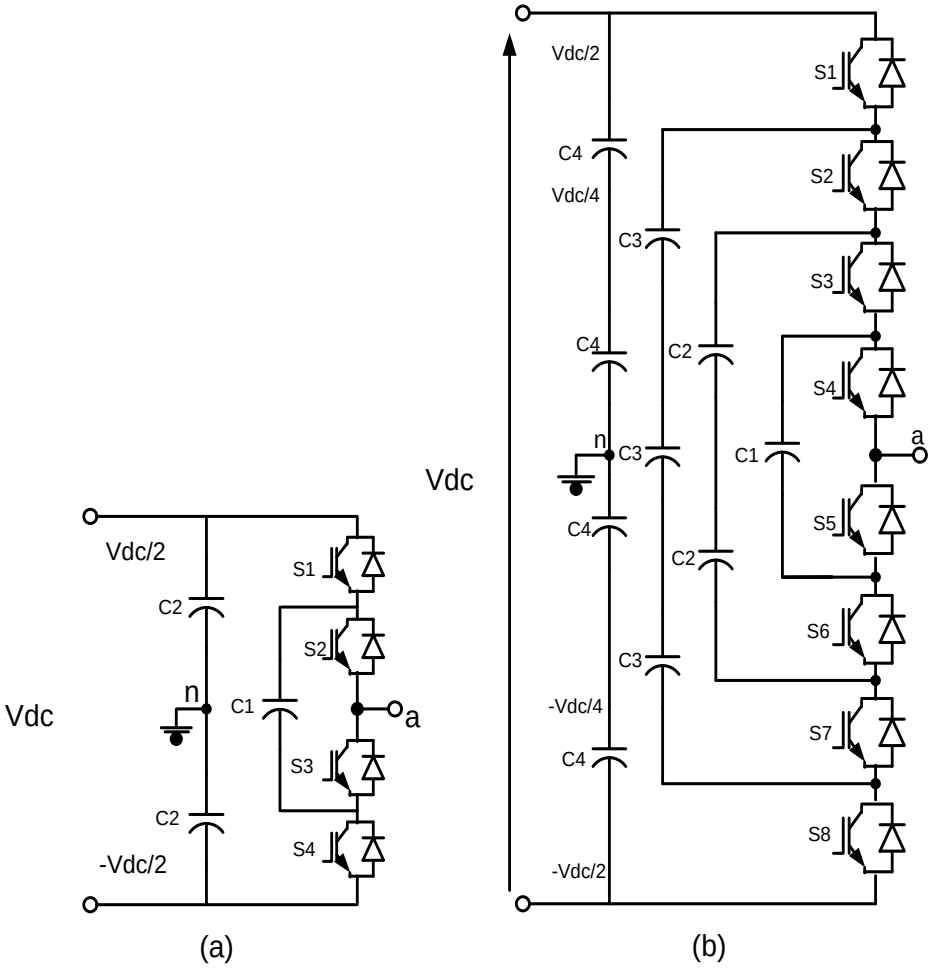


Fig. 3.10: Capacitor clamped multi-level inverter: (a) three-level and (b) five-level.

These topologies also have disadvantages when compared with a diode clamped converter. They need more capacitors than a diode clamped circuit; at the same time, the ratings of these capacitors will be large and the result will be more expensive. Another disadvantage is that the control for tracking the voltage for all capacitors to the same voltage level becomes more complicated.

The operation of a capacitor clamped three-level half-bridge is summarized in Table 3.3. As can be seen, there are three switching states ($V_{dc}/2$, *0 and* $-V_{dc}/2$); two states involve gating of the two upper and/or two lower devices. The third state has two options (a or b state), as illustrated in Fig. 3.11.

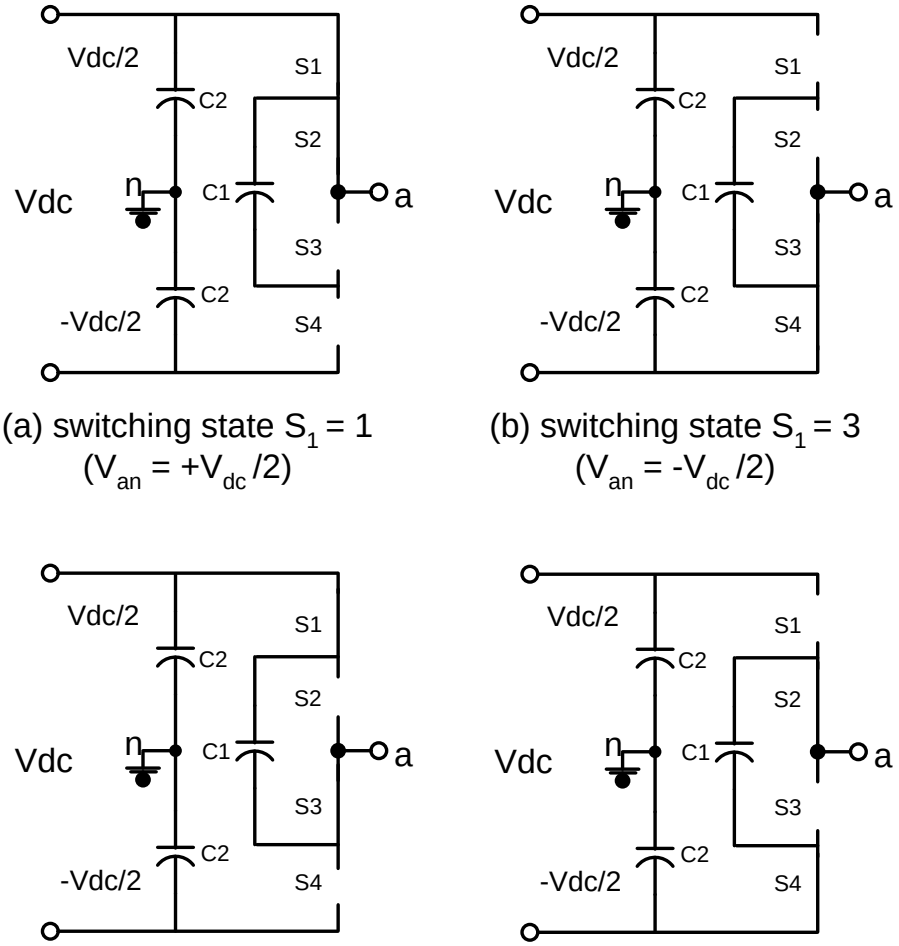


Fig. 3.11: Three-level half-bridge capacitor clamped inverter switching states

Table 3.3: Switching states and output voltages of a three-level half-bridge capacitor clamped inverter

State number		Switching states				Output voltage V_{an} (V)
		S_1	S_2	S_3	S_4	
1		1	1	0	0	$V_{dc}/2$
2	a	1	0	1	0	0
	b	0	1	0	1	
3		0	0	1	1	$-V_{dc}/2$

Table 3.4: Switching states and output voltages of a five-level half-bridge capacitor clamped inverter

State number		Switching states								Output voltage V_{an} (V)
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1		1	1	1	1	0	0	0	0	$V_{dc}/2$
2	a	1	1	1	0	1	0	0	0	$V_{dc}/4$
	b	0	1	1	1	0	0	0	1	
	c	1	0	1	1	0	0	1	0	
	d	1	1	0	1	0	1	0	0	
3	a	1	1	0	0	1	1	0	0	0
	b	0	0	1	1	0	0	1	1	
	c	1	0	1	0	1	0	1	0	
	d	1	0	0	1	0	1	1	0	
	e	0	1	0	1	0	1	0	1	
	f	0	1	1	0	1	0	0	1	
4	a	1	0	0	0	1	1	1	0	$-V_{dc}/4$
	b	0	0	0	1	0	1	1	1	
	c	0	0	1	0	1	0	1	1	
	d	0	1	0	0	1	1	0	1	
5		0	0	0	0	1	1	1	1	$-V_{dc}/2$

As can be seen from Table 3.4, there are 16 possible states to produce the output voltage for a five-level inverter topology [102, 109]. For any multilevel inverter, the relationship between the number of redundant switching states (S_{redun}) and the system's level is expressed as:

$$S_{redun} = 2^{(m-1)} - m \tag{3.4}$$

The total number of clamping capacitors required for each m-level inverter per phase leg is obtained from:

$$\left(\frac{(m-1)\times(m-2)}{(2)}\right) \tag{3.5}$$

added to $(m-1)$ capacitors in the dc-bus.

3.2.3 Cascaded Multilevel Inverter

The general structure of a cascaded multilevel inverter can be introduced by any number of single-phase cell inverters connected in series on the AC side, to introduce a high level voltage and obtain high power quality. These inverters can be built from the same type, such as a single-phase cascaded H-bridge *m*-level inverter [116], and can also be made from different inverter topologies; thus, they are known as hybrid inverters.

Corzine et al. [117] presented work on a new cascaded multilevel H-bridge inverter by cascading five-level inverters with a three-level H-bridge inverter (cascade-5/3H inverter), to introduce a 15-level or 11-level, depending on the percentage of DC source setting of a five-level to H-bridge inverter. *Zhong et al.* [118] [119] presented a cascade multilevel inverter using a single DC source and capacitors; the nominal value of the first capacitor voltage was half that of the DC source, and the second capacitor voltage was a fourth of the DC source. This type of cascade inverter can be used in hybrid electric vehicle applications, and can be built using different topologies, whether single-phase and three-phase, full-bridge or half-bridge.

Fig. 3.12 shows the single-phase cascaded H-bridge topology; each cell of the full-bridge is supplied by a separate DC source (SDCS) [111], and is connected in series on the AC side [102] [109]. Each inverter level can generate three different voltages at the output: $+V_{dc}$ by turning on S_1 and S_4, 0 output voltage by switching on S_1 and S_2 or S_3 and S_4 , and $-V_{dc}$ by turning on S_2 and S_3. Fig. 3.13 shows the switching states for one H-bridge inverter. The number of output phase voltage levels in a cascaded multilevel inverter is defined by:

$$m = 2 \times s + 1 \tag{3.6}$$

where *m* is the output phase voltage level and ***s*** is the number of DC sources.

From Fig. 3.12, the output voltage is synthesized by summing each of the H-bridge outputs, and is given as:

$$V_{an} = V_1 + V_2 + \ldots + V_{\frac{m-1}{2}-1} + V_{\frac{m-1}{2}} \tag{3.7}$$

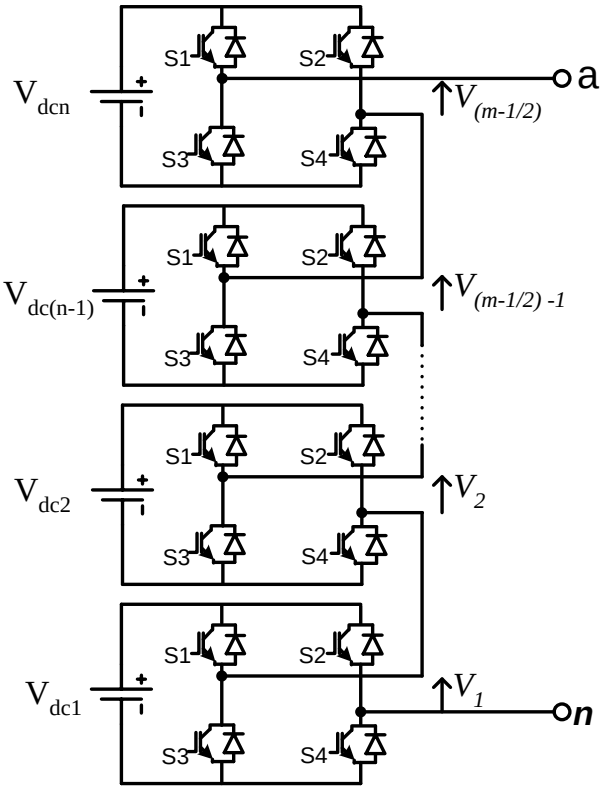


Fig. 3.12: Cascaded multilevel inverter

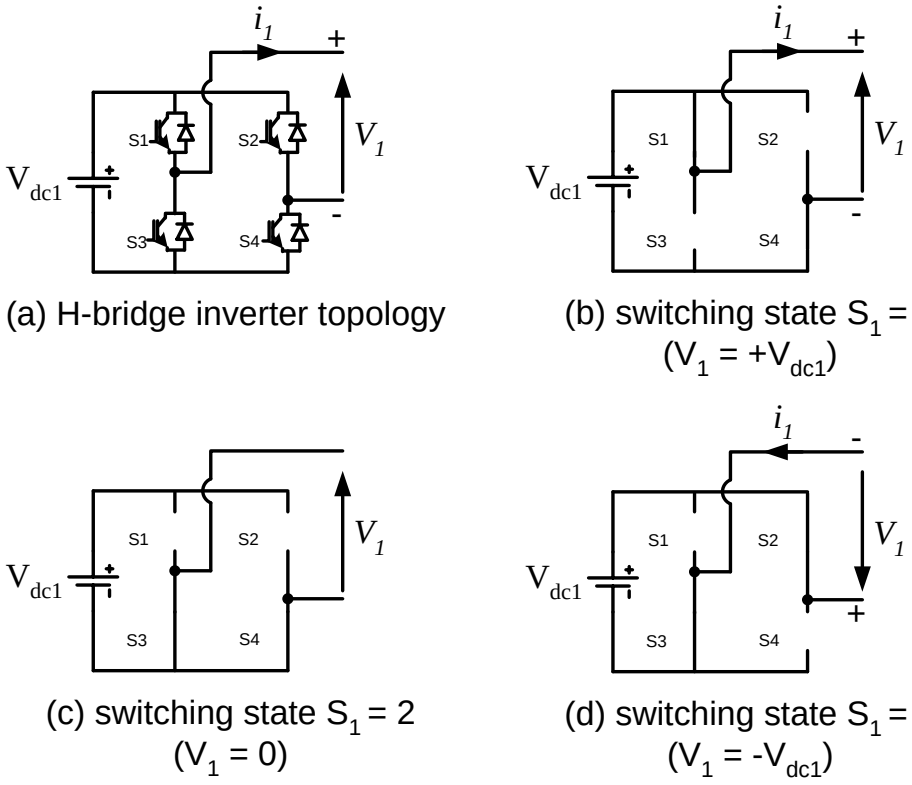


Fig. 3.13: Switching states of the H-bridge.

The basic structure of a five-level single-phase cascaded H-bridge inverter is shown in Fig. 3.14. This inverter consists of two conventional H-bridges connected in series with separate isolated DC voltage supplies. The operating states for this topology are listed in Table 3. 5. To avoid a shoot-through condition, the switches (S_1, S_3) and (S_2, S_4) operate as complementary pairs.

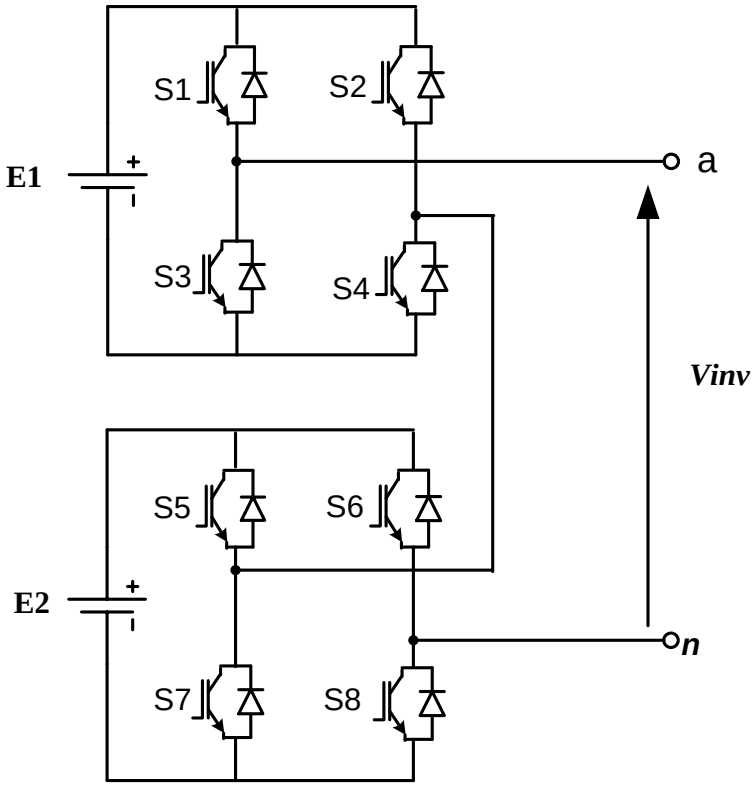


Fig. 3.14: Five-level cascaded H-bridge inverter

Table 3. 5: Switching states and output voltages of a five-level cascaded H-bridge inverter

State number	Switching states								Output voltage V_{an} (V)
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	1	0	0	1	1	0	0	1	$E_1 + E_2$
2	1	0	0	1	1	1	0	0	E_1
3	1	0	0	1	0	0	1	1	
4	1	1	0	0	1	0	0	1	E_2
5	0	0	1	1	1	0	0	1	

6	1	0	0	1	0	1	1	0	$E_1 - E_2$
7	1	1	0	0	1	1	0	0	0
8	1	1	0	0	0	0	1	1	
9	0	0	1	1	1	1	0	0	
10	0	0	1	1	0	0	1	1	
11	0	1	1	0	1	0	0	1	$-E_1 + E_2$
12	0	1	1	0	1	1	0	0	$-E_1$
13	0	1	1	0	0	0	1	1	
14	1	1	0	0	0	1	1	0	$-E_2$
15	0	0	1	1	0	1	1	0	
16	0	1	1	0	0	1	1	0	$-E_1 - E_2$

As can be seen from Table 3.5, there are 16 possible states used to produce the output voltage in a five-level cascaded H-bridge inverter [120] [59]. In the case of $E_1 = E_2 = E$ volt, the inverter will generate the following possible states: one possible state for both 2E and -2E, four possible states for both E and -E, and six possible zero voltage states.

In recent years, many new and novel cascaded multilevel inverter topologies have also been proposed. For example, in some applications, such as motor drives and static var compensators, where medium and high voltage is required, a novel multilevel DC link inverter is used to reduce the number of power switches and clamping diodes or capacitors, as compared with a traditional cascaded multilevel inverter, as explained by *Gui-Jia Su* [121], and *Khomfoi and Praisuwanna* [122].

3.3 Comparison of Multilevel Inverters

A comparison in terms of the power component requirements per phase leg among clamped-diode, flying-capacitor and cascaded multilevel inverters is provided in Table 3.6. This comparison is based on key factors, such as the number of switching devices, DC bus capacitors, clamped diodes and clamped capacitors [109]. A comprehensive review and comparison between different multilevel inverters is also presented by *Panagis and Stergiopoulos et al.* [123].

Table 3.6: Comparison of power components per phase leg of multilevel inverters

Inverter type	Cascaded inverter	Flying capacitor	Diode clamped
Total number of switching devices	$2 \times (m-1)$	$2 \times (m-1)$	$2 \times (m-1)$
Total number of DC bus capacitors	$(m-1)/2$	$(m-1)$	$(m-1)$
Total number of clamping diodes	0	0	$(m-1) \times (m-2)$
Total number of clamping capacitors	0	$\frac{(m-1) \times (m-2)}{2}$	0

3.4 Other Multilevel Inverter Topologies

In the previous sections, three basic multilevel inverter topologies were discussed. However, multilevel inverters can be designed in such a way as to create the most complex hybrid inverter topologies. *Rodriguez and Lai et al.* [102], and Zheng [124] both describe a generalized multilevel inverter structure. Fig. 3.15 shows the five-level generalized multilevel inverter, also known as a P2 multilevel inverter, because the basic cell is a two-level phase leg. A three-level diode clamped multilevel inverter is referred to as a 3PD generalized multilevel inverter, while a three-level capacitor clamped multilevel inverter, it is referred to as a 3PC generalized multilevel inverter [124].

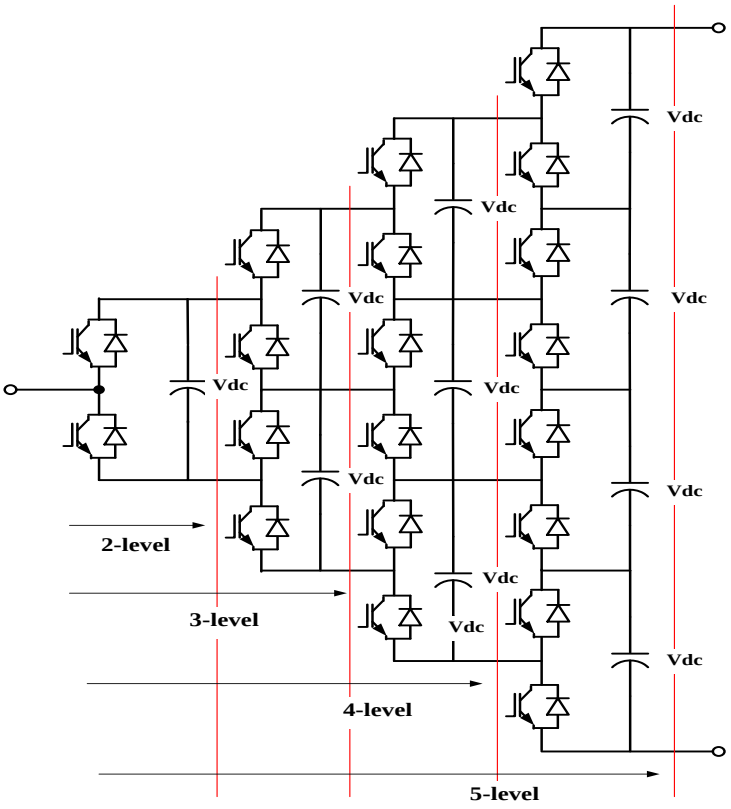


Fig. 3.15: Five-level generalized multilevel inverter

Calais and Agelidis et al. [125] describe a scheme of a cascaded transformer type multilevel inverter. For this type of inverter, the primary winding is connected at the midpoint of the H-bridge inverter, and the secondary windings of the transformers are connected in series (see Fig. 3.16). Each inverter produces three different voltage levels (positive, negative and zero), however, by changing the turn ratio of each primary winding of the transformers, a 27-level can be obtained [126].

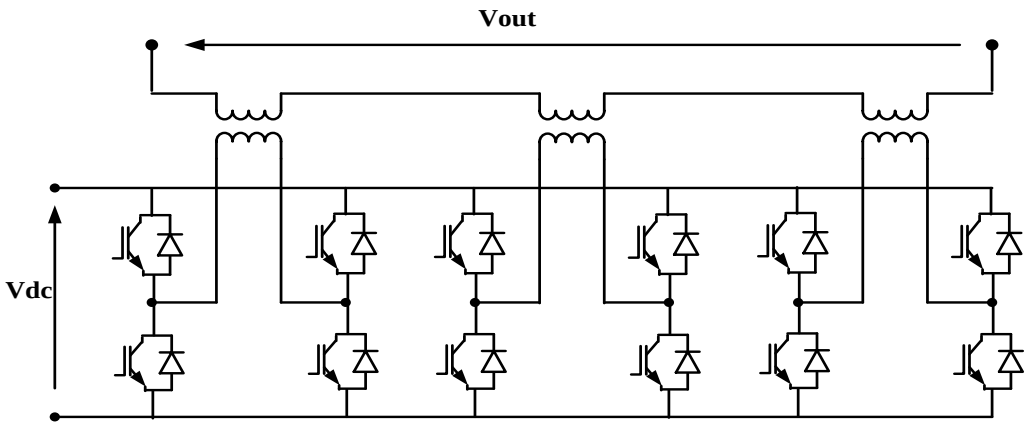


Fig. 3.16: Cascaded multilevel inverter with transformer

In addition to the basic types, a number of mixed-level hybrid multilevel inverters have also been described, as reported by *Madhav and Lipo et al.* [127], and *Kumar and Kim* [128]. *Song and Kim et al.* [129] describe new soft-switching flying capacitor multilevel inverters. These types of inverters can be generalized, and can extend to any number of levels from a basic three-level inverter design by adding auxiliary switches, blocking diodes and coupled inductors.

3.5 Features of Transformerless Three-Level HBDC Grid-Connected Inverter for PV system

The three-level half-bridge diode clamped inverter has several advantages when used as a transformerless interface for a photovoltaic system compared with other single phase inverters. These advantages are listed below.

- Eliminating the capacitive earth current and EMC by grounding the midpoint of the PV array. So no common mode voltage can be generated by three-level HBDC inverter.
- Each device has to block half of the DC link voltage compared with a conventional two level inverter.
- Lower rated devices, hence less $\frac{dV}{dt}$ improves electromagnetic capability and stress on filter
- Lower ripple current component in three-level HBDC inverter for the same switching frequency due to more voltage steps.
- The three-level HBDC topology provides an additional benefit over the H-bridge inverter. When the DC link current sensing and auto-calibration techniques are applied to eliminate DC current injection into the grid, there is no current flow in each DC link sensor for one half of a mains period. This provides plenty of time to sample the DC link current offset.

- The three-level HBDC topology provides an additional benefit over the three-level HBCC inverter. The clamping capacitor must be set up with required voltage level, before the capacitor-clamped can be modulated

3.6 Summary

This chapter has presented a number of multilevel inverters topologies deemed suitable for different applications such as grid connected inverters, electrical drive and flexible AC transmission systems. The main aim of this chapter was to give a background to multilevel inverters and identify the structure of each inverter type. Three basic multilevel inverters have been compared, which are the cascaded multilevel inverter, flying capacitor inverter and clamped diode inverter, and their power component requirements are shown in Table 3.5. This chapter has also described other multilevel inverter topologies such as the generalized and cascaded transformer type multilevel inverters.

CHAPTER 4

THREE-LEVEL HBDC INVERTER OPERATION AND SIMULATION RESULT

4.1 Introduction

This chapter presents the development of a three-level Half-Bridge Diode Clamped (HBDC) transformerless grid-connected PV inverter system model in Matlab/SimPower. This model is used to study, in detail, the sources of DC current offset in the inverter output, which is often difficult to carry out experimentally. Generally, the grid-connected inverter system converts DC power from the solar panels to AC power which is injected into the grid. Ideally, the output current of the inverter should be purely AC, but in practice, it will contain a small amount of DC current. Different types of DC current offset have been introduced in the simulation model, such as offset drift in the Hall effect current sensors and other sources are simulated.

The main contribution of this research lies in the development of an auto-calibration technique for the DC link current sensors in the multi-level inverter. Combined with a current feedback control scheme this technique allows the minimisation of DC current offset drift and linearity errors in the Hall effect current sensors as well as the effects of the PWM switching asymmetry, dead time delay, current control errors and on-state resistance and on-state forward voltage.

The second section of this chapter describes the basic circuit of three-level HBDC inverter. The third section presents the PWM switching strategy, including PD (POD or APOD) and anti-phase sine PWM controller used in inverter. The fourth section of this chapter presents the principles of operation of the grid-connected three-level half-bridge inverter, including the connecting and freewheeling states of DC link

current waveforms. The final section presents the proposed methods of introducing DC offset, and applying the current sensing and controller techniques to minimize the DC current injected into the grid.

4.2 Three-Level Half-Bridge Inverter Circuit

Fig. 4.1 shows the circuit diagram of a three-level half-bridge inverter. This circuit consists of four semiconductor switches, S1 to S4, connected in series to produce three voltage levels with four states. The inverter contains two bulk capacitors, C1 and C2, connected in series. Voltage clamping is performed by two diodes, D1 and D2. The middle point (n) of the two capacitors and the two diodes is grounded; hence, the circuit is also known as Neutral Point Clamped (NPC) inverter. Two DC series connected voltage sources are needed to supply the inverter. The switching signals of S1 and S2 are complementary to the switching signals of S3 and S4. The following section will describe the power switching strategy used for the three-level half-bridge inverter.

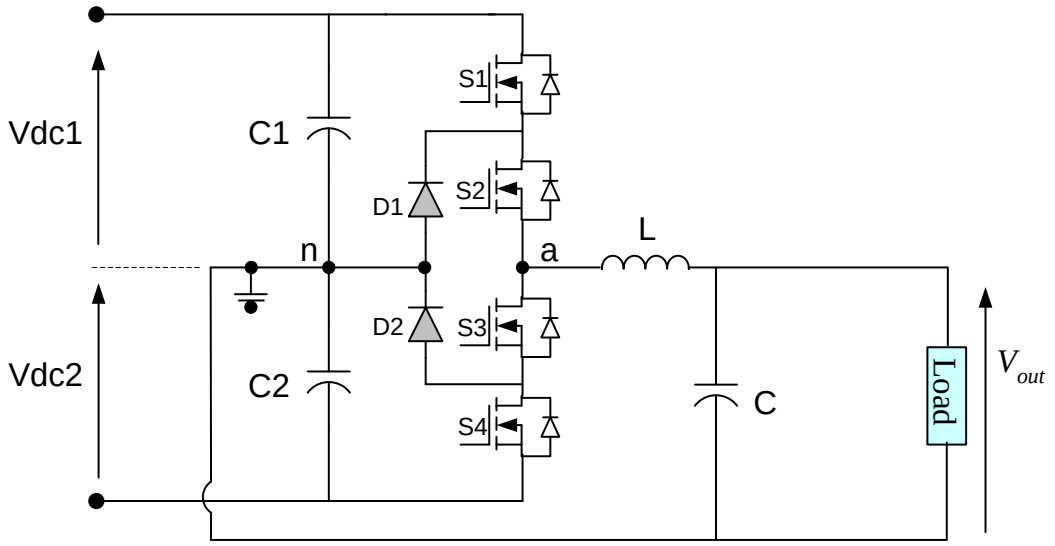


Fig. 4.1: Three-level half-bridge inverter

4.3 PWM Switching Strategies

Choosing the correct switching strategy to achieve better output voltage and current waveforms with minimum harmonic distortion and low switching losses is important [130]. The switching technique can also be used to balance the DC link capacitor in a multilevel inverter, as proposed by *Yo-Han,Lee el al.* [131]. This used a novel SVPWM strategy to balance the DC link capacitor voltage when the voltage source is shared.

The use of Pulse Width Modulation (PWM) to drive a power electronic converter is not a new concept. In 1975 and later, *Bowes, Bird et al.* [132-136] published work detailing the PWM technique used for drives and control of power inverter applications.

There are different techniques used to generate sinusoidal PWM switching signals for single-phase inverters. These techniques are based on two methods, namely bipolar and unipolar PWM schemes (*Mohan and Robbins* [137]). These methods generate a sinusoidal AC output with the desired amplitude and frequency. This is obtained by comparing a sinusoidal control signal $V_{control}$ at frequency f_m with a triangular waveform $V_{carrier}$ at frequency f_c, which is known as the inverter switching frequency. When the control signal $V_{control}$ is greater than $V_{carrier}$, the PWM output is positive, and when $V_{control}$ is less than $V_{carrier}$, the PWM output is negative. The frequency of the control signal f_1 is called the fundamental frequency of the inverter output. The inverter output voltage obtained is not perfectly sinusoidal, and contains harmonics at frequency f_m.

The amplitude modulation ratio m_a is defined as:

$$m_a = \frac{V_{control}}{V_{tri}} \tag{4.1}$$

Where $V_{control}$ is the peak amplitude of the control signal, while V_{tri} is the peak amplitude of the triangular signal.

The frequency modulation ratio is defined as:

$$m_f = \frac{f_c}{f_m} \tag{4.2}$$

4.3.1 Bipolar PWM

Fig. 4.2 shows the bipolar PWM scheme applied to an H-bridge inverter. The instantaneous output voltage V_{out} does not have a zero state, which means the inverter output voltage changes between +Vd and –Vd. As illustrated in Table 4.1, the transistor switching strategy is as follows: T_{A+} and T_{B-} are ON, while $V_{control}$ is greater than V_{tri} , and T_{B+} and T_{A-} are ON while $V_{control}$ is less than V_{tri}.

Table 4.1: Bipolar switching strategy

Transistor	T_{A+}	T_{B-}	T_{B+}	T_{A-}	V_{out}
$V_{control} > V_{tri}$	ON		OFF		$+V_d$
$V_{control} < V_{tri}$	OFF		ON		$-V_d$

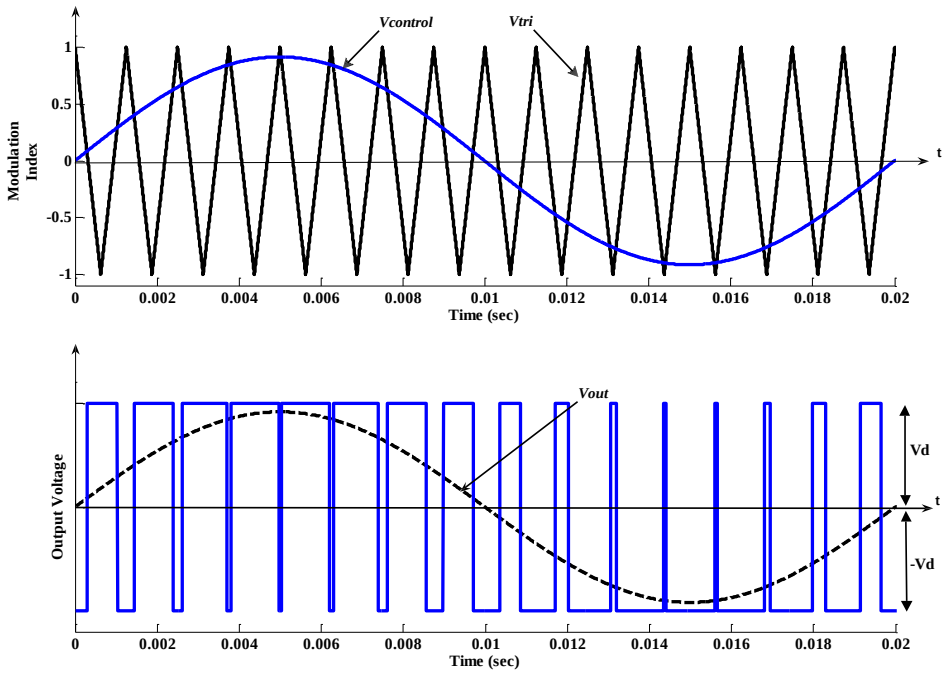


Fig. 4.2: Bipolar PWM

4.3.2 Unipolar PWM

Fig. 4.3 shows the unipolar PWM technique. In this scheme, the switching of the H-bridge inverter legs is independent. As shown below, each leg is controlled by comparing V_{tri} with a different signal of $V_{control}$ (+ or -). As a result, the output voltage of the inverter changes between 0 and V_{dc} and/or 0 and $-V_{dc}$. In this case, four switching states are produced, as shown in Table 4. 2.

Table 4. 2: Unipolar switching strategy

Transistor	T_{A+}	T_{B-}	T_{B+}	T_{A-}	V_{AN}	V_{BN}	$V_{out} = V_{AN} - V_{BN}$
$V_{control} > V_{tri}$	ON		OFF		V_d	0	V_d
$V_{control} < V_{tri}$	OFF		ON		0	V_d	$-V_d$
$-V_{control} > V_{tri}$	ON	OFF	ON	OFF	V_d	V_d	0
$-V_{control} < V_{tri}$	OFF	ON	OFF	ON	0	0	0

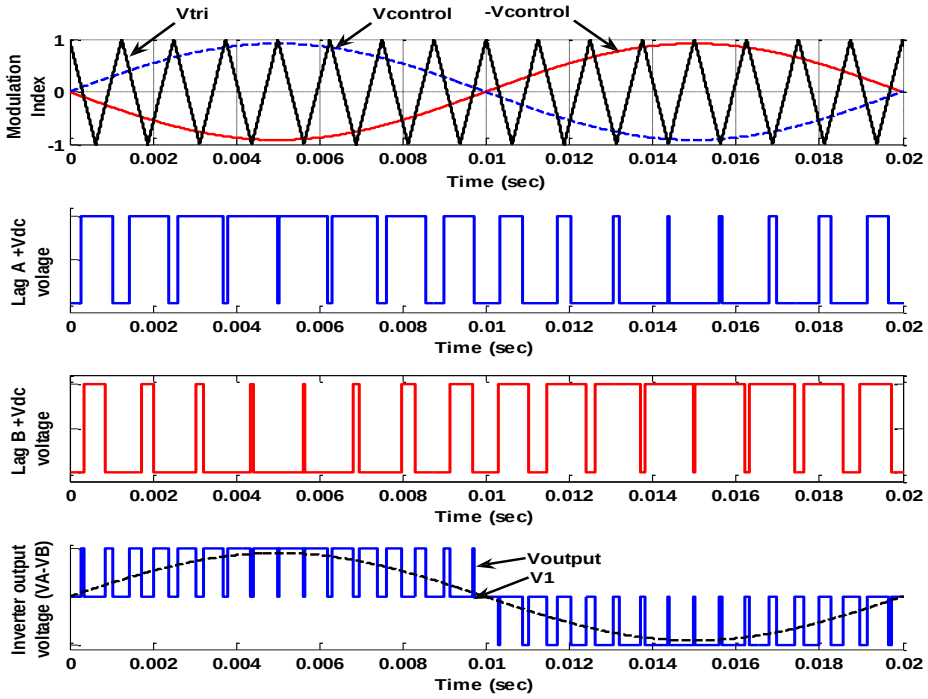


Fig. 4.3: Unipolar PWM

Unipolar PWM switching has advantages compared to bipolar PWM switching, such as reducing the switching losses, achieving better output sine waveform quality and less electro-magnetic interference (EMI) [138].

4.3.3 Multilevel Sinusoidal Pulse Width Modulation (MSPWM)

In multilevel inverters with more than two levels, *(N-1)* carrier signals are required, where N is the number of inverter levels and is an odd number. The sinusoidal reference is then compared with each triangular carrier, and the output of this comparison produces two complementary signals. This method was first introduced by *Carrera et al.* [139] and became widely used in multilevel inverter control. In this method, the frequency and the peak-to-peak amplitude of the carriers have to be the same. In addition, it has been shown that the placement of the carriers can be organized in such a way as to produce different types of Multilevel Sinusoidal Pulse Width Modulation (MSPWM). *Aspalli et al.* [140] studied this technique to minimize THD in a five-level inverter. The carrier arrangement was shown to affect THD performance. *Manimala, Geetha et al.* [116] utilised MSPWM techniques to reduce

THD in five-level cascaded inverter. It was concluded that by increasing the modulation indices for all the MSPWM techniques, the THD is reduced; the THD values in various MSPWM techniques are comparatively close, and high reduction can achieved by selecting an appropriate modulation index.

Fig. 4.4 shows three categories of alternative carrier dispositions for MSPWM, as follows:

- Phase Disposition (PD), where all carriers are in phase, see Fig. 4.4 (a)
- Phase Opposition Disposition (POD), where the carriers above the sinusoidal reference zero point are 180 degrees out of phase with those below the zero point, see Fig. 4.4 (b)
- Alternative Phase Opposition Disposition (APOD), where each carrier is phase shifted by 180 degrees from its adjacent carrier, see Fig. 4.4 (c)

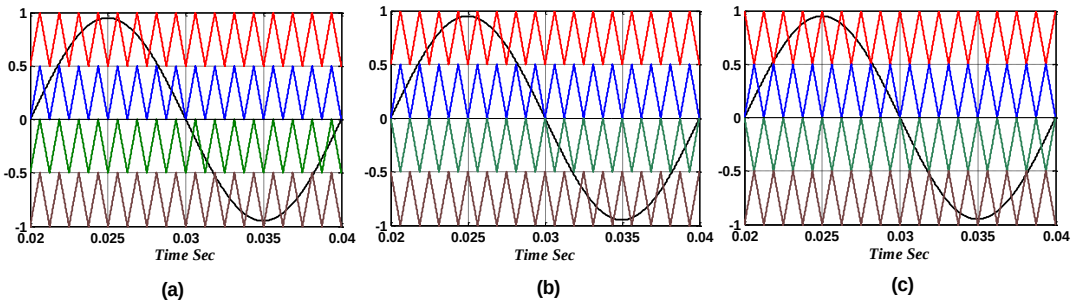


Fig. 4.4: Modulation waveforms (a) PD; (b) POD; (c) APOD.

As can be seen from the above figure, the APOD and POD approach are equivalent in a three-level inverter. Another approach may also be used for a three-level half-bridge inverter.

- Anti-phase sine, where two anti-phase sine waveforms are compared with one carrier, see Fig. 4.5

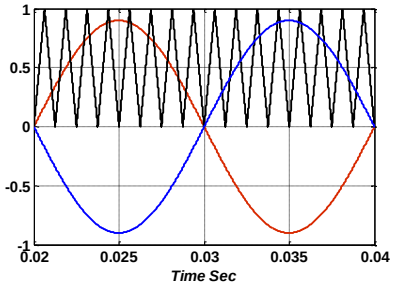


Fig. 4.5: Anti-phase sinusoidal with one carrier

In this chapter, the three switching strategies are applied to the three-level inverter operating with a resistive load. The aim of this study was to investigate which method produces the lowest switching harmonics and is most convenient for experimental software implementation. The inverter components for comparing the different PWM carrier schemes are shown in Table 4.3.

Table 4.3: Inverter parameters

Parameter	Value	Units
DC link voltage (V_{dc1} & V_{dc2})	360 & 360	V
DC link capacitance (C_1 & C_2)	400	μF
Capacitor resistance R_{c1}, R_{c2}	0.01	Ω
Inductor L	2.2	mH
Inductor resistance R_L	*0.047*	Ω
Filter capacitor C	*2.6*	μF
Switching frequency	20	kHz
Load resistance	15	Ω

4.3.4 Phase disposition (PD) PWM

Fig. 4. 6 shows the PD switching technique, involving two in-phase triangular carriers. These carriers have the same peak-to-peak amplitude A_c and the same frequency f_c and are compared with the sine wave reference to produce two complementary signals. Fig. 4.6 also shows the switching states of a three-level HBDC inverter, the DC link current waveform during the positive and negative half cycles, the inverter terminal voltage and the output voltage.

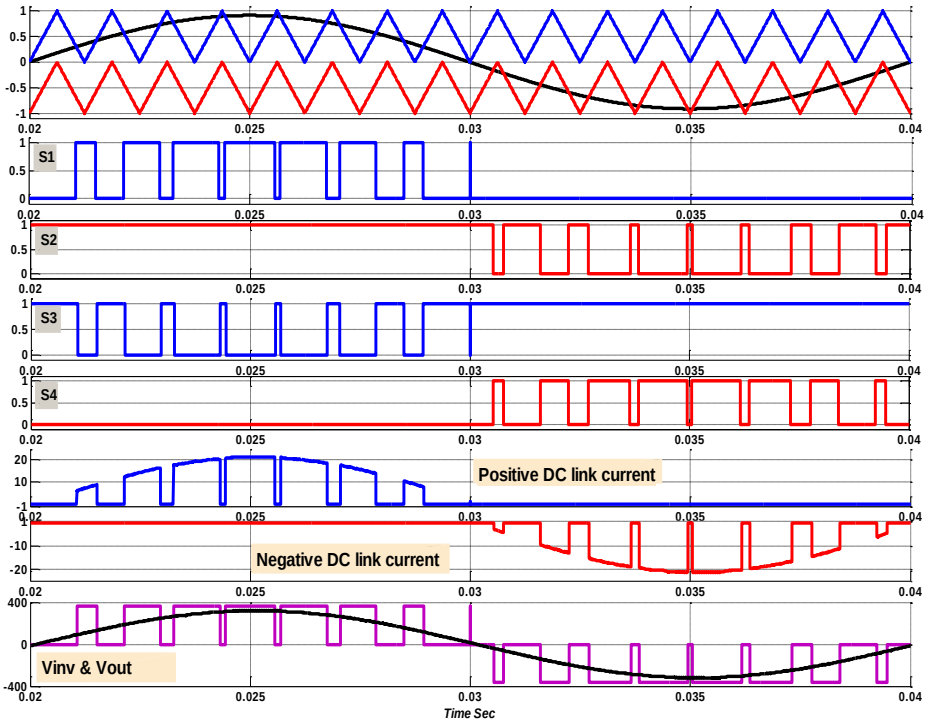


Fig. 4. 6: Modulation waveforms of PD PWM for three-level HBDC inverter. m_a = *0.95*, f_c = 800 Hz, f_m = 50 Hz.

Fig. 4.7 shows the simulated result of FFT analysis of output current spectra for the PD PWM scheme under the conditions given in section 4.3.1.3. As can be seen from the graph, the current spectra contain both odd and even harmonics. However, the magnitudes of the even harmonics are lower than those of the odd harmonics. The THD produced by this technique is 0.72% with the magnitude of fundamental harmonic (coloured in black) being 22.66A.

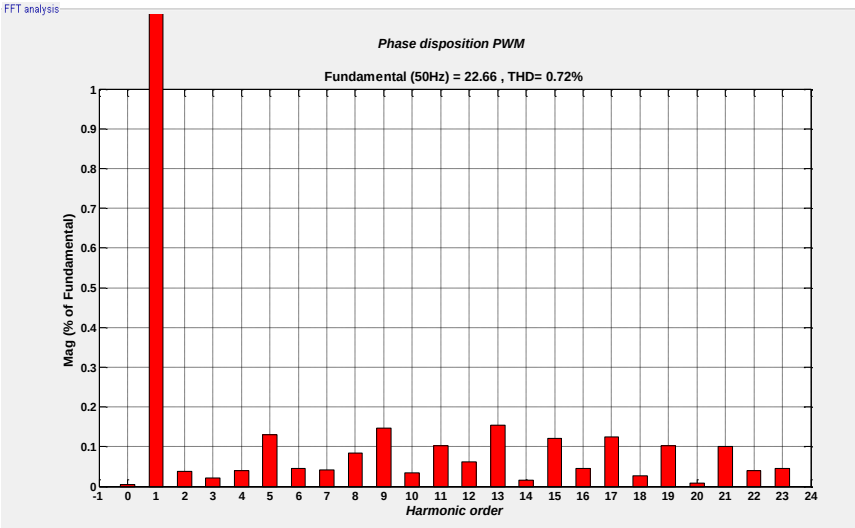


Fig. 4.7: The current spectra of the inverter output current for PD PWM, @ m_a = 0.95, m_f = 400

4.3.5 Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) PWM

The carrier position of the POD and APOD schemes is the same in a three-level half-bridge inverter, because only two carriers are used. In this case, the carrier above zero reference is out of phase with the carrier under zero reference, as shown in Fig. 4.8. These carriers have the same amplitude and frequency. However, when these carriers are compared with the reference sinusoid a pair of complementary PWM outputs is produced, as illustrated in Fig. 4.8. The figure also shows the switching state of the inverter, the positive and negative DC link current waveforms of one cycle, the inverter terminal voltage and the output voltage.

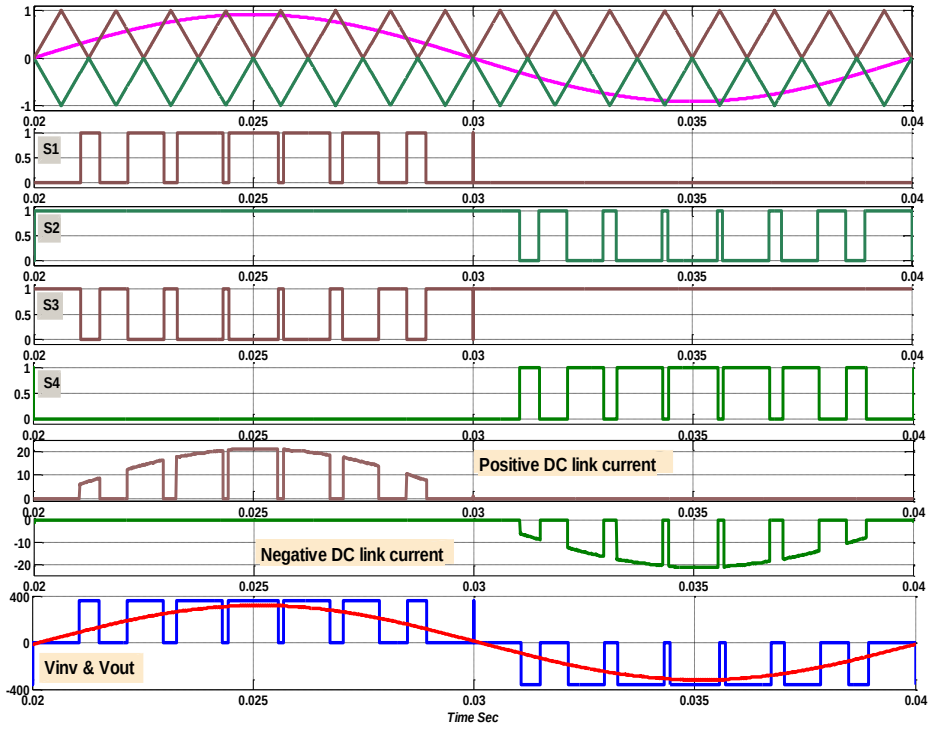


Fig. 4.8: Modulation waveforms of POD & APOD PWM for three-level HBDC inverter. m_a = *0.95*, f_c = 800 Hz, f_m = 50 Hz.

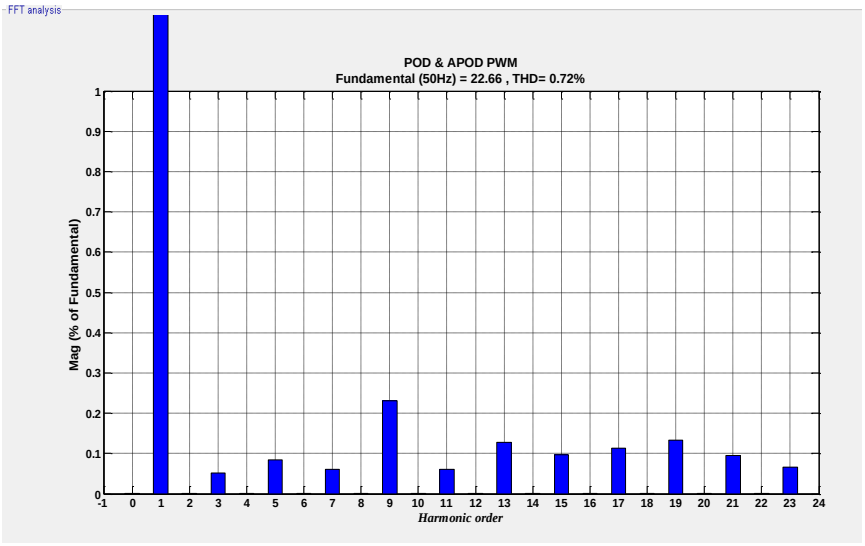


Fig. 4. 9: The current spectra of the inverter output current for POD & APOD PWM, @ m_a = 0.95, m_f = 400

The simulated results of the FFT analysis of output current spectra for the POD and APOD PWM schemes are shown in Fig. 4. 9. The results are obtained using the parameters specified in Table 4.3. From Fig. 4.9, we can see that the characteristic of

the current spectrum is unlike that produced by the PD PWM method. In this case, the output current only contains the odd harmonics; at the same time, the magnitude of the fundamental harmonic, which is coloured in black, is 22.66A, and the THD for both these techniques are equal.

4.3.6 Anti-Phase sine PWM

The anti-phase sine PWM technique is not new; it was first introduced by *Velaerts et al.* [141], using a single carrier and sinusoidal references to drive a three-level inverter. However, the anti-phase method has been used to drive a three-level half bridge, because it is easy to understand and offers a good reduction in the output current harmonics compared with PD, yet giving the same results when compared with POD or APOD PWM for a three-level half-bridge inverter. A comparison between these methods will be given in the next section (4.4).

Fig. 4.10 shows the fixed frequency triangular wave with two anti-sinusoidal references to produce the switching control signals for the three-level inverter.

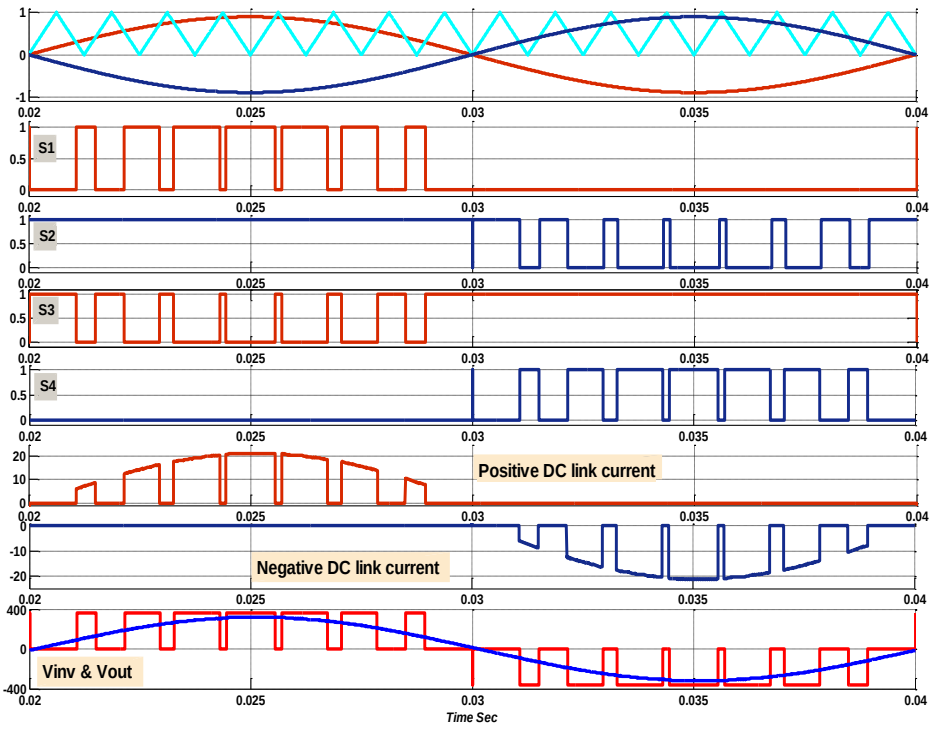


Fig. 4.10: Modulation waveforms of anti-phase sin for three-level HBDC inverter. m_a = *0.95*, f_c = 800 Hz, f_m = 50 Hz.

The simulated result of FFT analysis of output current spectra for anti-phase PWM scheme is shown in Fig. 4.11. This result indicates that this is the same as that obtained with POD and APOD under the conditions specified in Table 4.3. From the graph above, we can see that the characteristic of current spectrum is similar to that of POD and APOD, but does not resemble that of the PD scheme.

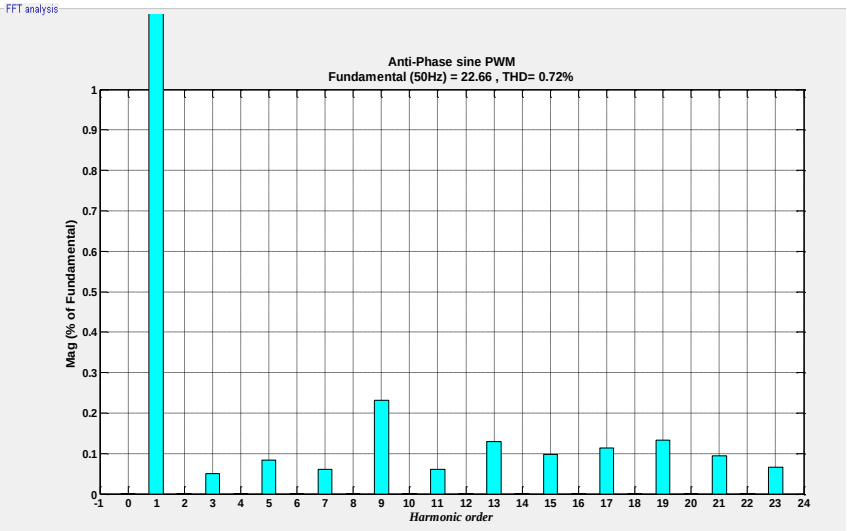


Fig. 4.11: The current spectra of the inverter output current for anti-phase PWM, @ m_a = 0.95, m_f = 400

4.4 Comparison of the three Multilevel SPWM Schemes

The three different SPWM schemes are modelled and simulated in MATLAB SimPower to investigate the output current harmonic issues for a three-level half-bridge inverter. The aim of this study was to select the best SPWM scheme that produces a lower THD.

After simulations were run on all SPWM techniques, the output harmonic performance for each technique is compared in Fig. 4.12. The total harmonic distortion value for all schemes, PD, POD or APOD, and the anti-phase sine PWM, is the same. It can also be seen from the graph that the PD scheme current spectra contain both odd and even harmonics. However, the even harmonics in this technique are less compared to odd harmonics.

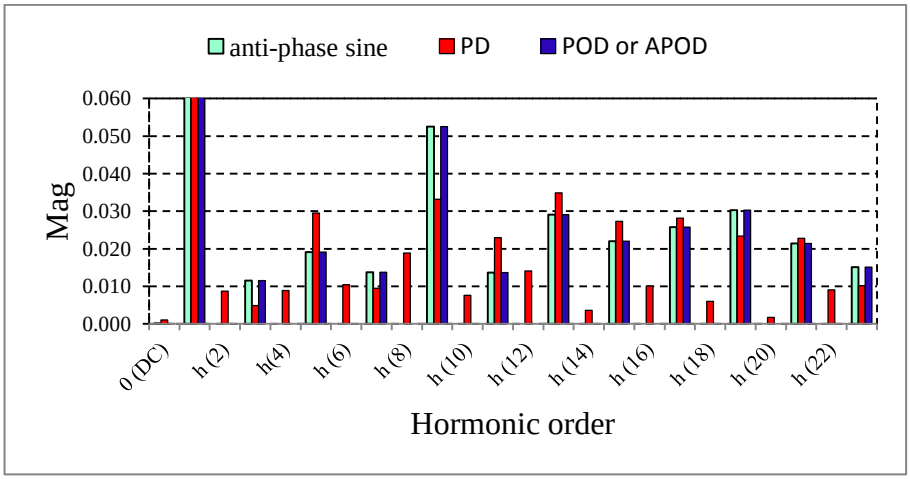


Fig. 4.12: current spectra for all SPWM, @ $m_a = 0.95$, $m_f = 400$

Fig. 4.13 shows the average set of harmonic data for each of the three schemes under test. This average set is calculated using a sixth order polynomial function, as demonstrated by *Armstrong et al.* [142].

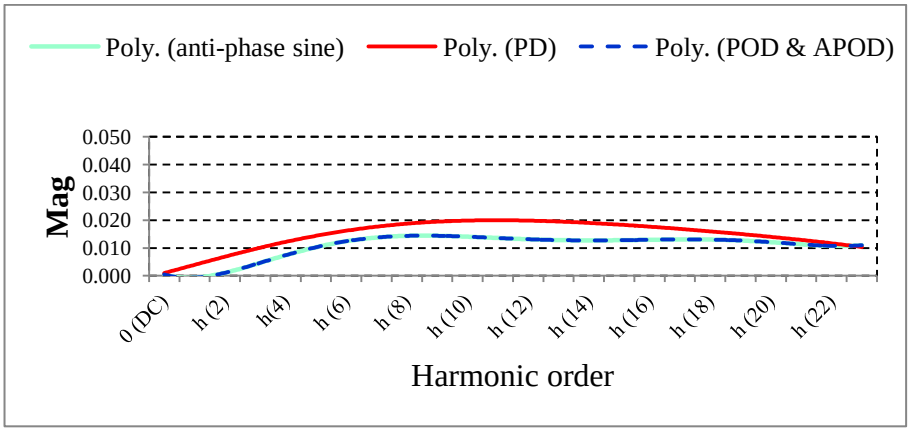


Fig. 4.13: Average current spectra for all SPWM, @ $m_a = 0.95$, $m_f = 400$

From the results, in Figs. 4.12 and 4.13, the anti-phase sine and the POD or APOD schemes produce an output current with the lowest harmonic distortion, and are therefore likely to be the best PWM schemes for a transformerless three-level half-bridge inverter.

Fig. 4. 14 presents the comparison between the anti-phase sine and (POD or APOD) methods, and provides an explanation of why they produce the same harmonic spectrum in the inverter output current. The anti-phase sine method is mainly derived

from the (POD or APOD) method by replacing the lower carrier with an anti-sine reference. As can be seen from Fig.4.14, in the first half cycle, both methods give the same results as the PWM characteristic waveform. In the second half cycle, when the lower carrier in the (POD or APOD) method is replaced by anti-sine in the (anti-phase sine) method, the PWM characteristic waveform will be equal, due to the symmetry between the anti-phase carriers. Hence, the waveform S_1 produced by the POD or APOD method is equal to S_1' produced by the anti-phase sine method, and S_4 produced by the POD or APOD method is equal to the invert of S_4' produced by the anti-phase sine method. Consequently, the harmonics spectrum produced by both methods will be the same.

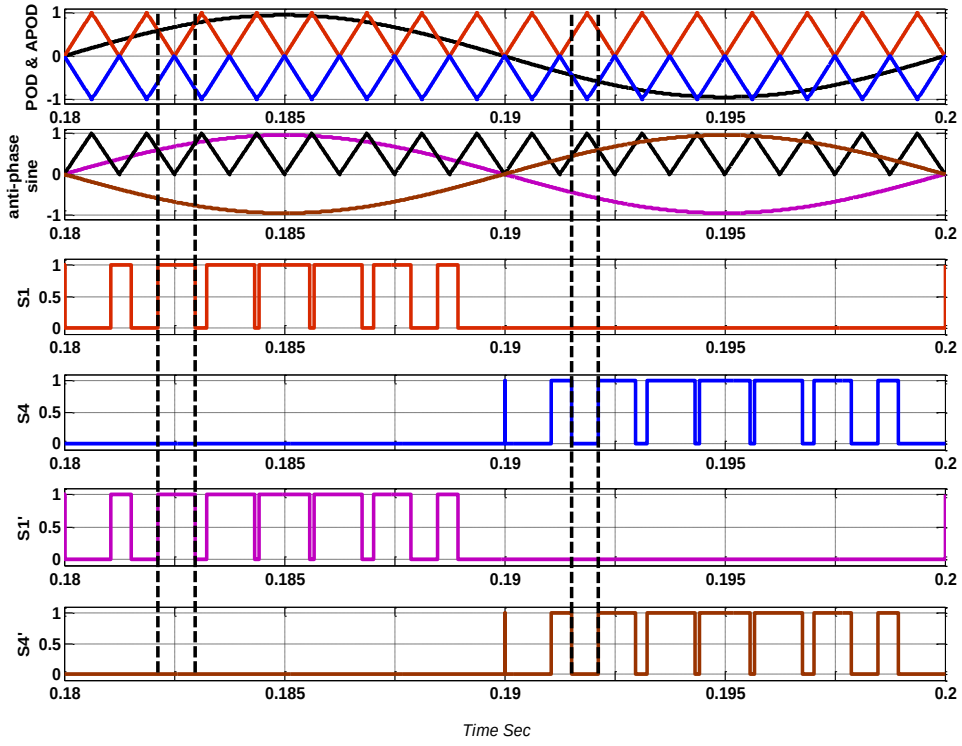


Fig. 4. 14: Comparison of PWM characteristic waveforms between the anti-phase sine and (POD or APOD). $m_a = 0.95$, f_c = 800 Hz, f_m = 50 Hz.

4.5 Principles of Operation of the Grid-Connected Three-Level Half-Bridge Inverter

Fig. 4.15 illustrates a transformerless three-level half-bridge grid connected inverter, which uses the DC link current sensor technique [67]. This technique requires two current sensors, the first is located between the upper switches and DC link capacitor, and the second is located on the opposite side between the lower switches and DC link capacitor.

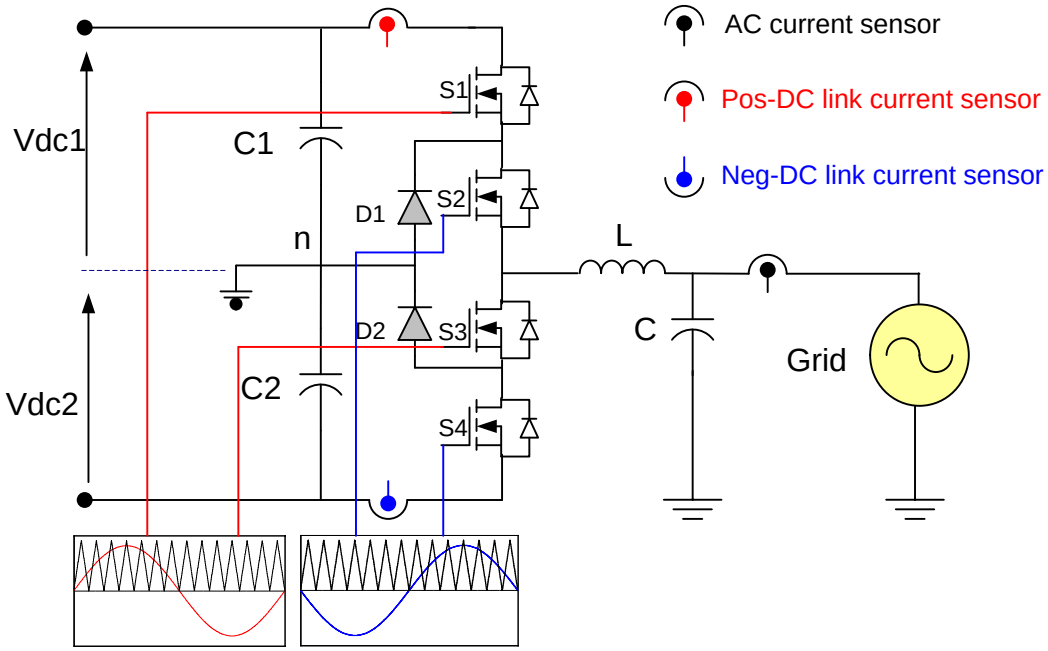


Fig. 4.15: Three-level inverter controlled by anti-phase PWM

The anti-phase sine PWM has been selected to drive the three-level HBDC inverter. The principle of operation of this topology is explained in this section. The circuit can be controlled to produce three output voltage states in four steps, as presented in Table 4.4. When the inverter is switched using the anti-phase sine wave scheme, the output voltage V_{an} has four states. During States 1 and 3 (known as the connecting states) the output current flows through the DC link current sensors to the load, as shown in Fig. 4.16. During these states, the output current will be measured by the positive states and negative states DC link current sensors.

Table 4.4: Three-level inverter output states

State number	Switching states				Output voltage V_{an} (V)
	S_1	S_2	S_3	S_4	
1	ON	ON	OFF	OFF	$V_{dc}/2$
2	OFF	ON	ON	OFF	0
3	OFF	OFF	ON	ON	$-V_{dc}/2$
4	OFF	ON	ON	OFF	0

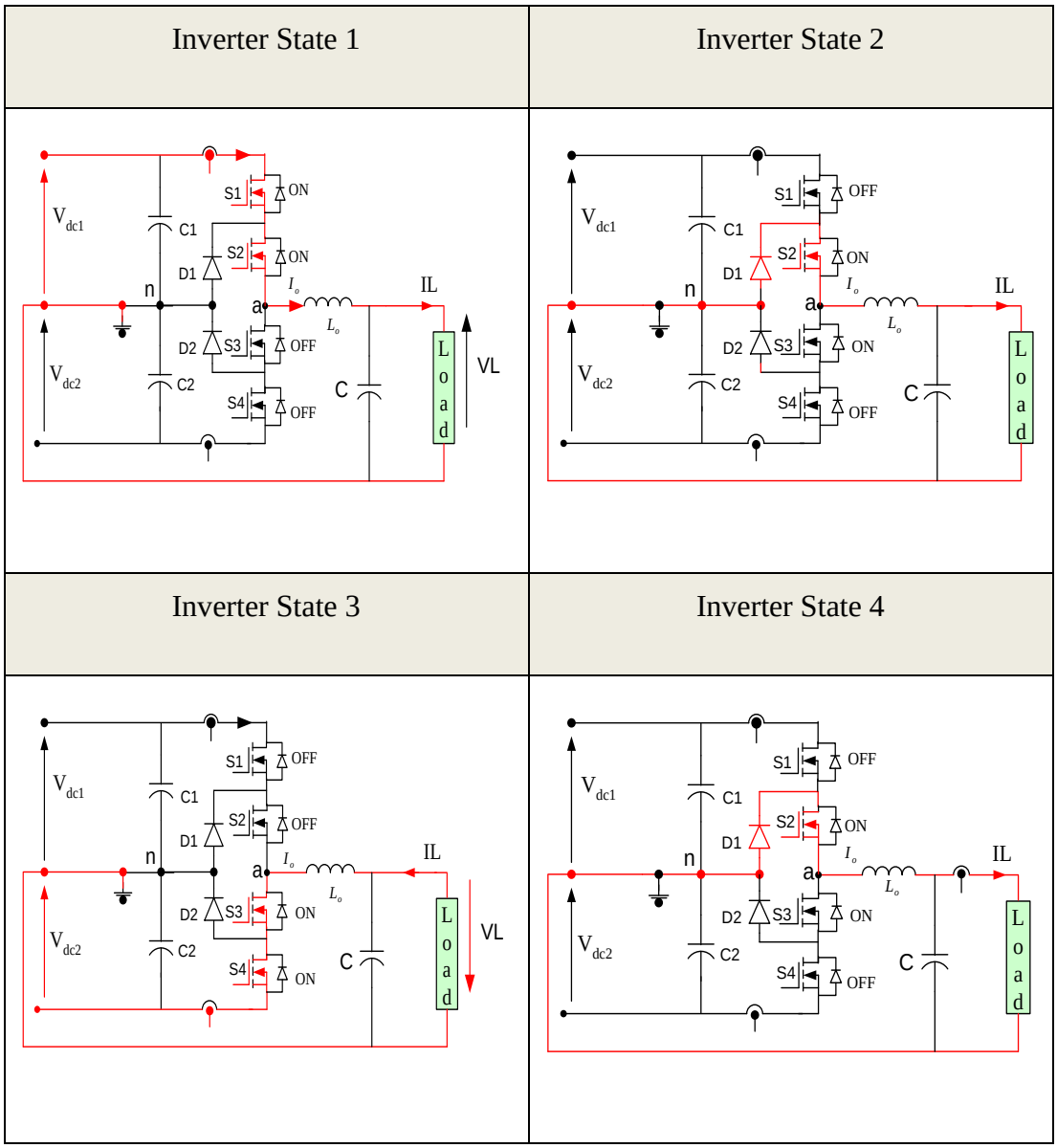


Fig. 4.16: Connecting and freewheeling states of three-level half bridge inverter

In states 2 and 4, which are freewheeling states, the output voltage across the inverter is zero and the inductor freewheeling current flows in one of two loops, depending on the polarity of the previous connecting loop, as shown in Fig. 4.16. In the positive half cycle, the freewheeling current goes through D1 and S2, as shown in Fig. 4.17. In the negative half cycle, the freewheeling current path is via D2 and S3, as shown in Fig. 4.18. During the freewheeling state, the current flowing in both DC link sensors goes to zero. This presents an opportunity to auto-calibrate the offset of each sensor. In practice, however, this freewheeling period is too narrow, especially at the beginning and end of each half cycle. The three-level half-bridge topology provides an additional advantage over the H-bridge for this application. There is no current

flow in each DC link sensor for one half of a mains period. This results in plenty of time to sample the DC link current to carry out the auto-calibration function.

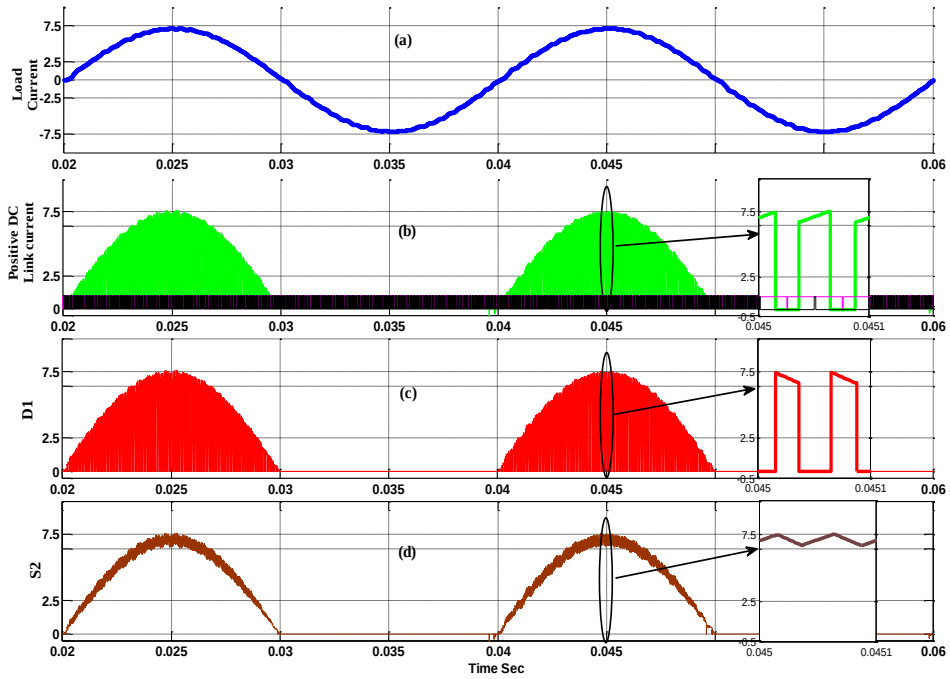


Fig. 4.17: (a) Output current, (b) Positive-DC link sensor current, (c) freewheeling current through D_1 and (d) connecting and freewheeling current through S2.

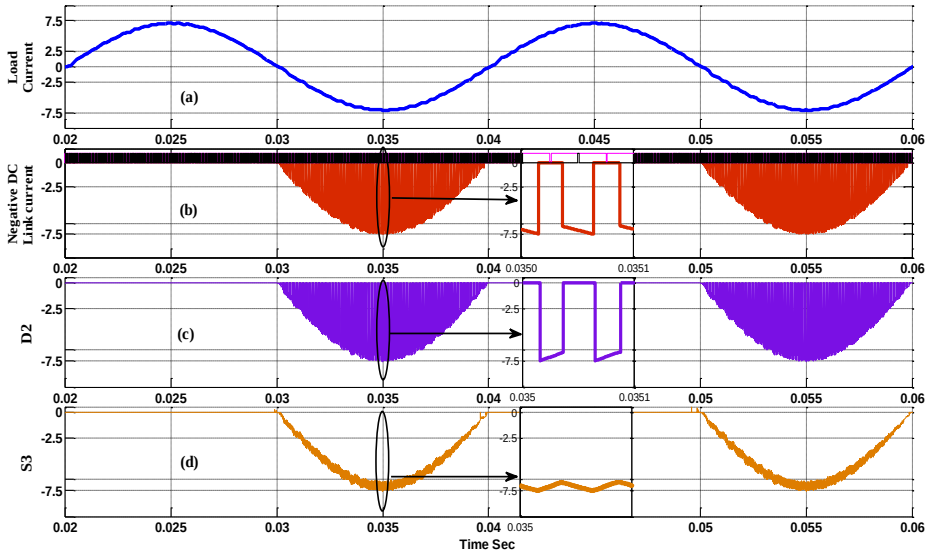


Fig. 4.18: (a) output current, (b) Negative-DC link sensor current, (c) freewheeling current through D_2 and (d) connecting and freewheeling current through S3.

4.6 Circuit analysis and DC Link current sensing techniques

Fig. 4.19 show a transformerless three-level half bridge grid connected inverter, modelled and simulated in MATLAB SimPower to apply the auto-calibration technique using two current sensors to minimize the DC current injected to the AC side in the power system network. The upper sensor is connected between C1 and the upper switches to measure positive DC link current. The lower sensor is connected between C2 and the lower switches to measure negative DC link current.

Two 30 V DC sources were connected in series across the input of the inverter to produce a total input voltage of 60V DC. The inverter is switched at 20 kHz . The inverter feeds an LC filter, which in turn feeds the grid. The rated output current is 5A rms. Current control is achieved using the two DC link current sensors.

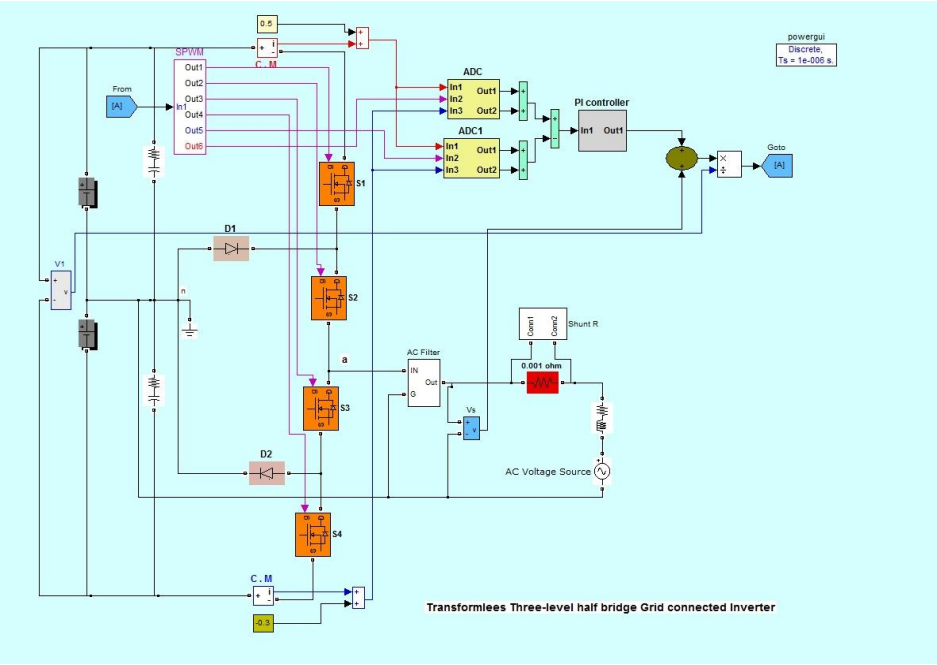


Fig. 4.19: Simulation circuit of transformerless three-level half bridge grid connected inverter

4.6.1 DC link current Measurement Timing

Fig. 4.20 and Fig. 4.21 show the connecting and freewheeling state sample times of the positive and negative DC link current sensors. The sample time is taken in the centre of PWM and tuned to avoid misreading the pulse, when it becomes narrow around the zero crossing. The first figure represents S1 and S2 switching states, the current that flows through these switches, the positive freewheeling current through D1 and the positive DC link current. The second figure represents S3 and S4 switching states, the current that flows through these switches, the negative freewheeling current through D2 and the negative DC link current. The time period in these figures is short, (0.4mS) to zoom in on the behaviour of connecting and freewheeling currents.

In this case, the PWM is not over-modulated and the current can be measured at the bottom of the triangular waveform. At this point, the three-level inverter will be in either State 1 or State 3, both of which are current conducting states. On the other hand, the freewheeling loop current can be measured at the top of the triangular carrier when no current goes through the DC link current sensors. At these points, the three-level inverter will be in either State 2 or State 4, both of which are freewheeling states.

During the freewheeling states, the inductor current will flow in one of two directions. In the positive half cycle, the path will be through D1 and S2, and in the negative half cycle, the path will be through D2 and S3. In this case, the freewheeling time in both current sensors can be used to calibrate sensors to remove DC current offset.

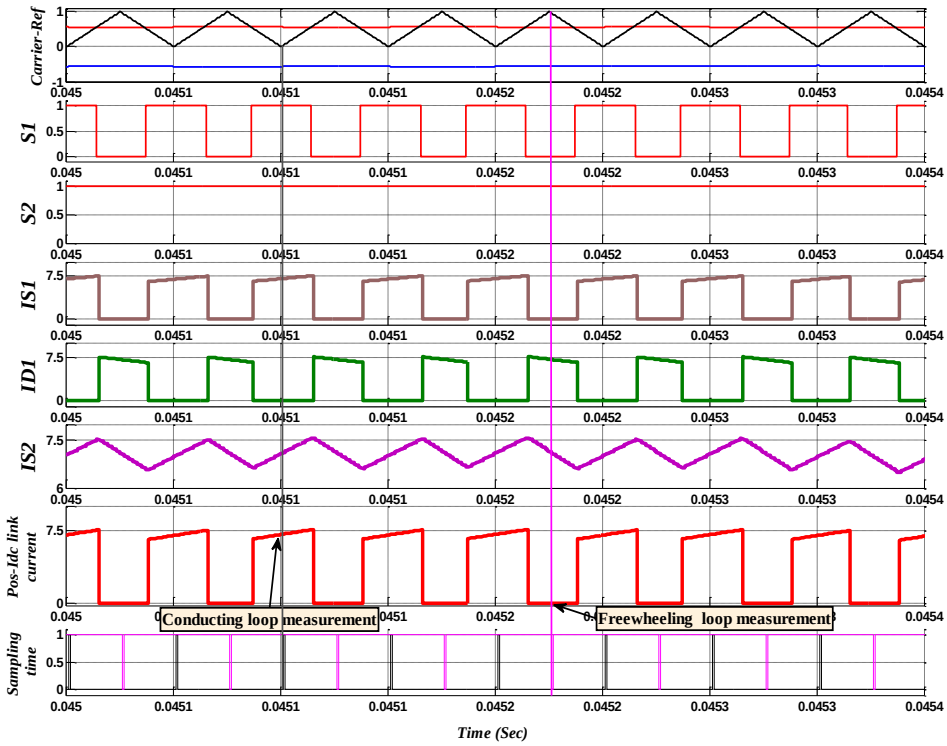


Fig. 4.20: Sampling time, semiconductors and positive current sensor states

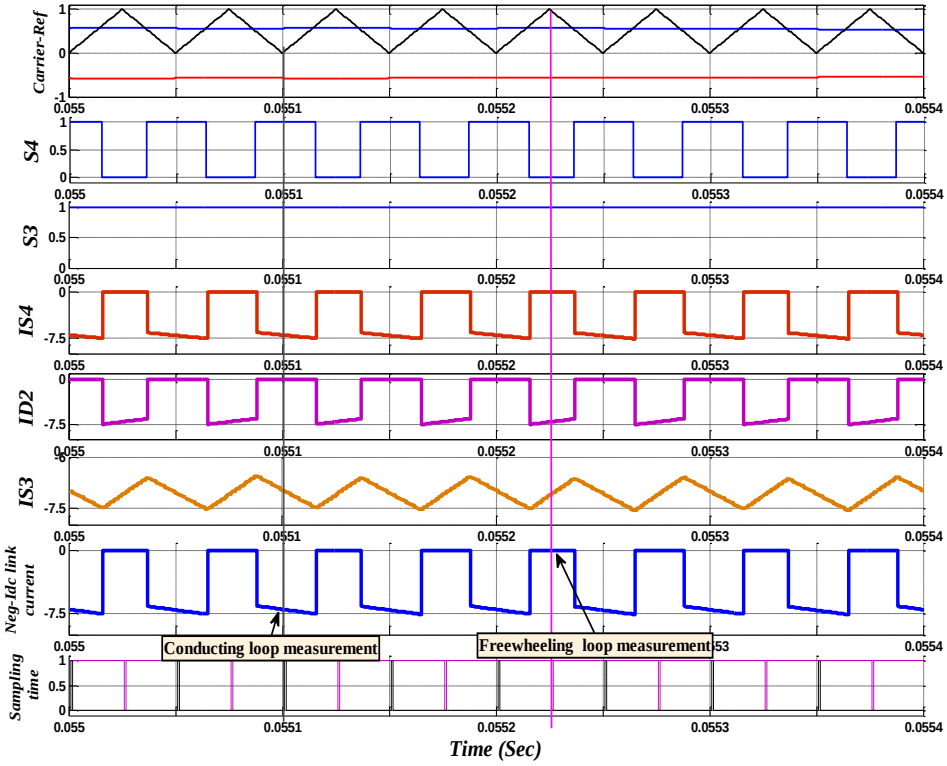


Fig. 4.21: Sampling time, semiconductors and negative current sensor states

4.6.2 Current control Method

There are different types of current control methods that have been implemented in single-phase inverters, such as conventional PI control, Proportional Resonant (PR) control [143], vector control [144], sliding mode control [145], fixed frequency hysteresis [146] and predictive deadbeat control [147].

In this study, a PI controller is chosen, because it is simple to implement and well understood. Fig. 4.22 shows that grid voltage feed-forward is added to improve the dynamic performance of the current controller; this is similar to back EMF feed-forward in motor drives, as reported by *Rahman, Lim and Low* [148].

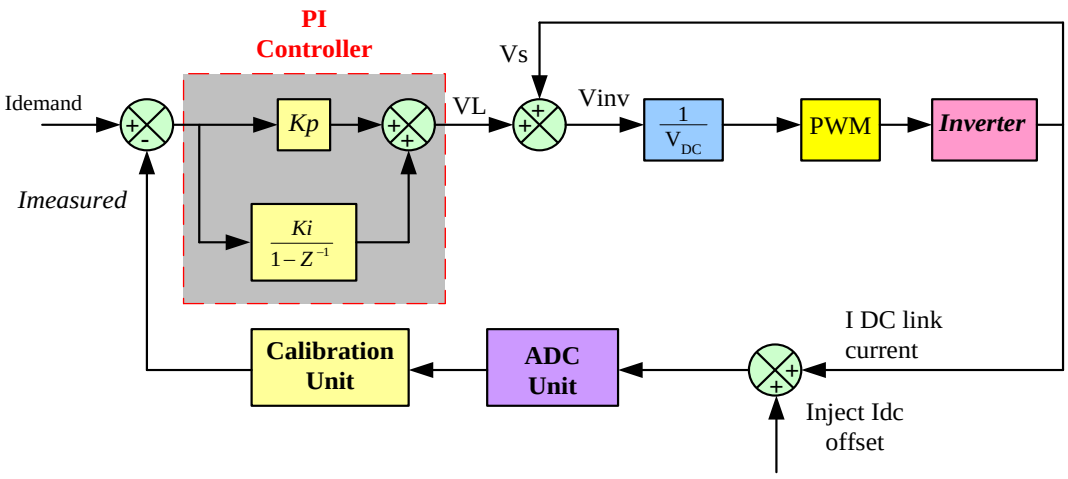


Fig. 4.22: PI current controller and calibration techniques

In Fig. 4.22, K_p is the proportional gain, k_i is the integral gain, V_L is the inductor voltage, V_S is the supply voltage, V_{inv} is the converter terminal voltage and V_{dc} is the DC link voltage. The inverter current reference source (I_{demand}) is generated internally from a sinusoidal table inside the controller.

The use of feed-forward voltage results in only the inductor voltage being effectively controlled when the inverter injects current to the grid. As shown in the phasor diagram of Fig. 4.23, the converter terminal voltage is obtained from V_L and V_S.

However, to achieve the current demand, the inverter terminal voltage is divided by the DC link voltage V_{dc}. The output of the calculation is the modulation signal for input to the PWM unit. The amplitude of this PWM was limited to ± 0.95 to provide a minimum pulse width, and to avoid overmodulation. Also, the calibration unit in Fig. 4.22, can be defined as the unit where subtraction of positive and negative DC current offset loop measurements from positive and negative conducting loop measurements occurs.

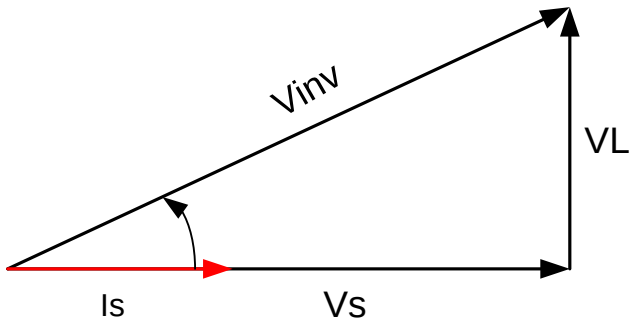


Fig. 4.23: Phasor diagram for unity power factor operated inverter

The divination of conventional PI is derived as follows:

Proportional divination (P),

$$u = k_p e \tag{4.3}$$

Where k_p is the proportional gain and e is the error

Integral divination (I),

$$u = k_i \int e.dt \tag{4.4}$$

Where k_i is the integration gain factor

So for the PI combination

$$u = k_p e + k_i \int e.dt$$

or

$$u = k_p \left(e + \frac{k_i}{k_p} \int e.dt \right) \tag{4.5}$$

4.6.3 DC Offset and Auto-Calibration Method in the Simulation Circuit

In order to test the ability of the scheme to compensate for DC current offset errors, an artificial offset in the current sensor is introduced. These DC offset errors can be represented in different ways; for example, the on-state resistance of the power MOSFETs are set at different values (0.03 and 0.02 Ω), the dead time is set at different periods of delay (1.6 µSec and 1.2 µSec) (see Fig. 4.24) and the artificial offset in the current sensor is represented by a current measurement device, as shown in Fig. 4.18. In this case, constant values of 0.7 and 0.3 are added, respectively, to the output of the positive and negative DC link current sensors in the simulation circuit.

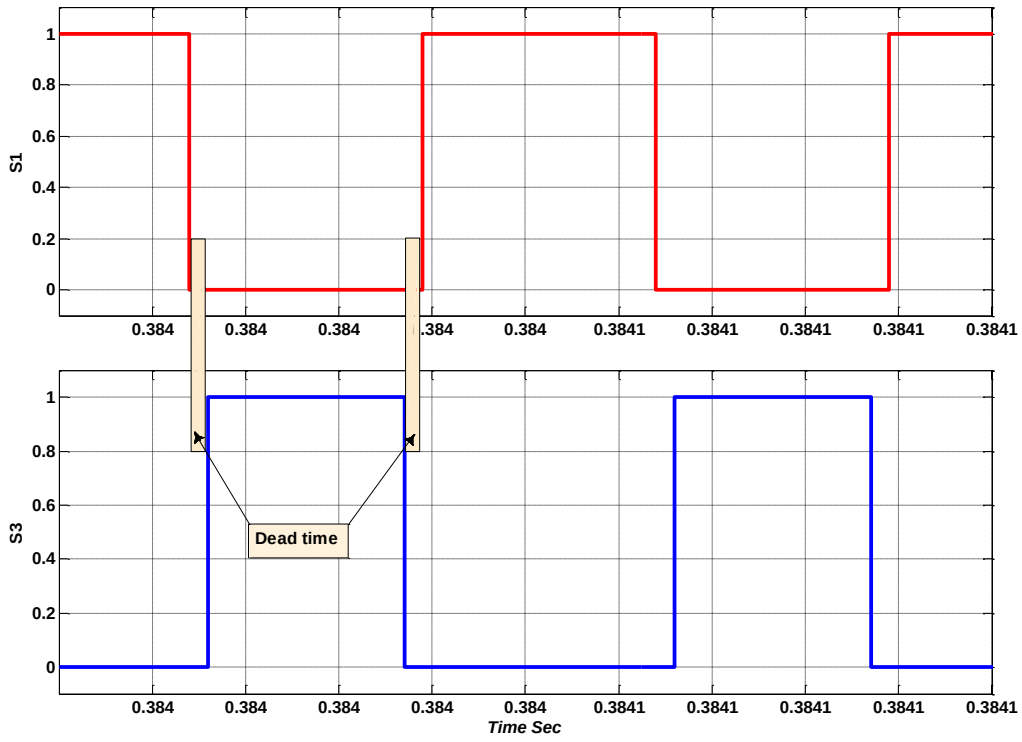


Fig. 4.24: Switching dead time

Fig. 4.25 shows the positive and negative DC link current, with and without DC offset, in the grid connected circuit. The figure also includes the analogue to digital converter signal of positive and negative DC link current, and the sum of these signals, with and without calibration. The waveforms in Fig 4.25(d) clearly show the difference with and without the auto-calibration technique.

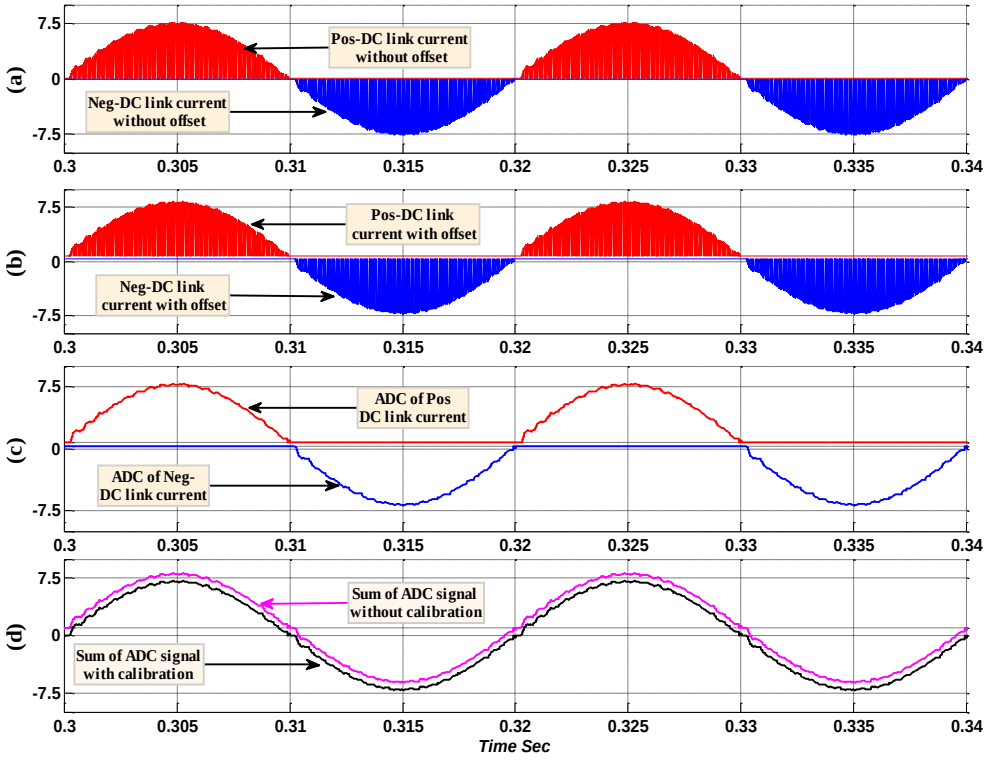


Fig. 4.25: Inject DC offset and auto-calibration method

From the graph above, we can see that the output current measurement is the sum of positive and negative conducting loop measurements, and can then be calibrated by subtracting positive and negative DC offset loop measurements. The outcome of this measurement is then fed to a conventional PI current controller. The output of the PI controller is the modulation signal used as the input to the PWM signal generator, as shown in Fig. 4.22.

4.6.4 DC Current Measurement in the Output of Inverter

It is not necessary to measure the DC current offset at the inverter output using a shunt resistance in the simulation scheme, as it is possible to do so directly. But the purpose of measuring DC offset is to represent the behaviour of the voltage across the shunt. The voltage across this shunt is passed through a RC low-pass filter with a cut-off frequency of 1 Hz to reject the 50Hz AC component.

Fig. 4.26 and Fig. 4.27 show the voltage across the RC filter, with and without calibration. In Fig. 4.26, the auto-calibration technique is not applied, and the V_{mean} across the RC filter is approximately 1×10^{-4} volt, which is the expected value, when a sum of 0.1 Amp is injected through DC link sensors and the shunt resistor was 0.001Ω. In the next case, the auto-calibration technique is applied, and the V_{mean} across the RC filter is nearly zero volts.

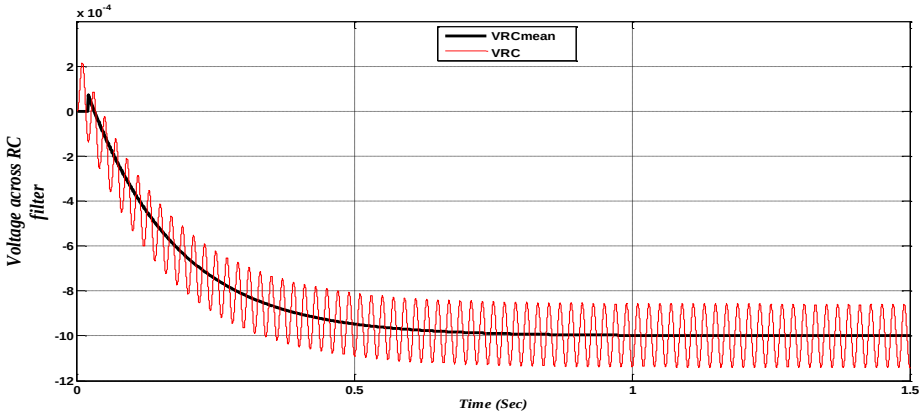


Fig. 4.26: Voltage across RC filter without calibration

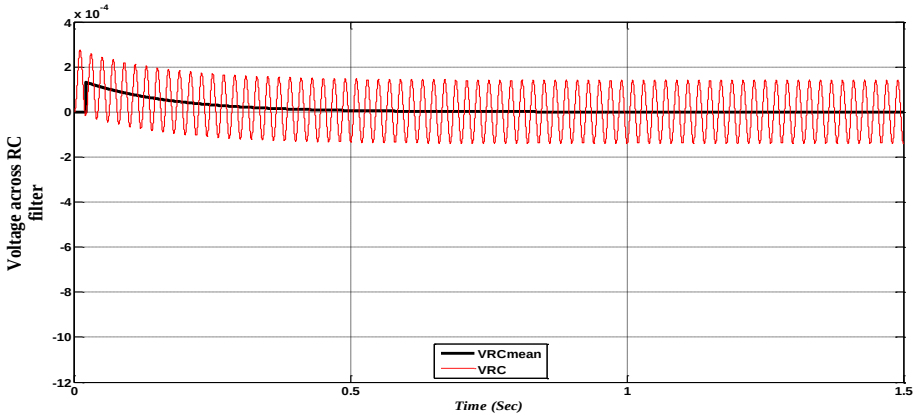


Fig. 4.27: Voltage across RC filter with calibration

4.7 Summary

This chapter has presented the investigation into the operation of the three-level half-bridge inverter using MATLAB simulation. The switching strategy was also presented and different multilevel SPWM schemes were studied to select the one that produces a low harmonic order, with a lower THD component. A comparison of three SPWM schemes was carried out, and the anti-phase sine method was selected to drive the three-level half-bridge inverter. In this chapter, the principles of inverter operation were demonstrated, and the auto-calibration technique applied using positive and negative DC link current sensors, in order to minimize DC current injected into the grid. Also, the ability of auto-calibration methods to compensate for different types of DC offset current introduced during the inverter operation had been demonstrated, including device mismatch or unbalanced PWM control, non-linearity errors and artificial offsets in the current sensors.

CHAPTER 5

EXPERIMENTAL TESTING

5.1 Introduction

This chapter describes the experimental test equipment for the grid-connected power electronic converter system, using a three-level, half-bridge inverter with DC link sensor current controller. An overview of the grid-connected experimental hardware is presented, before applying an auto-calibrating DC link current sensing technique to the three-level half-bridge inverter. This chapter also includes a description of the method used to synchronise the inverter to the grid.

5.2 Grid-Connected Layout of the Three-Level Half-Bridge Inverter

Fig. 5.1 shows the layout for the experimental test rig containing the three-level half-bridge inverter DC link current sensing controller. The circuit consists of two series-connected DC sources, which provide the DC link for the inverter via a main switch. The inverter feeds an LC filter, the output of which is connected to an isolation transformer. The secondary side of the transformer is coupled to the grid via a Variac and a switch. The following outline will provide more details about the experimental hardware.

5.3 DC Supply

For grid-connected inverters, which have to interface to the 230V network, it is appropriate to have a DC bus voltage in the region of 720V. For correct operation of the three-level topology, the DC bus must therefore consist of two series-connected supplies of 360V each. The laboratory test rig was designed to operate at a reduced voltage and used two 30V DC power supplies to produce an overall DC bus voltage of 60 V. These sources were connected through a three pole switch, which is used as an operating switch to connect the power sources to the inverter. It is also used to protect the inverter against short circuits.

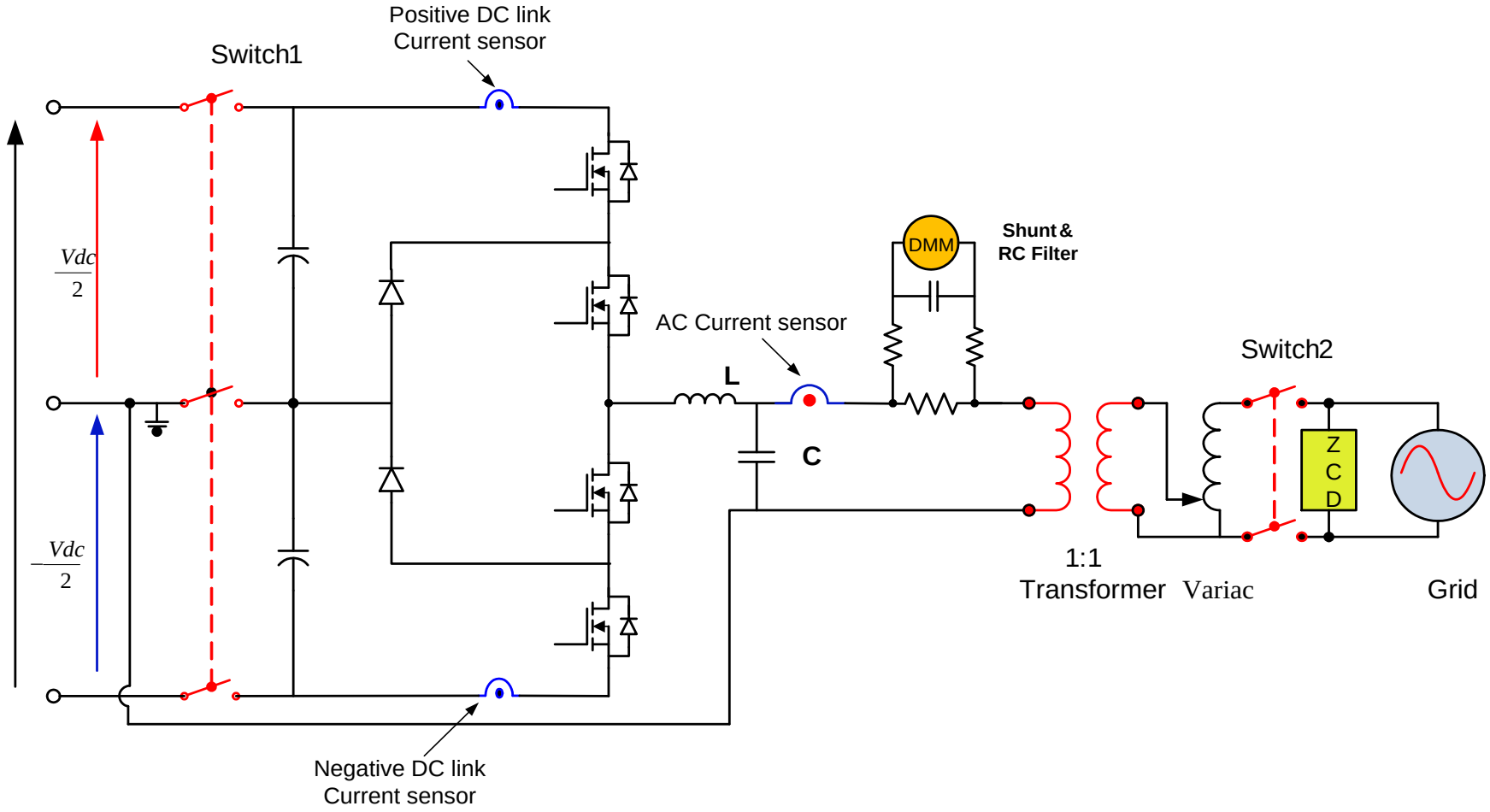


Fig. 5.1: Schematic depicting inverter experimental setup

5.4 AC-Side Filters

Passive AC filters at the inverter output are used to reduce voltage harmonics and current distortion in the inverter output, in order to meet the power system quality standards. There are three different filter topologies commonly used to attenuate harmonics in grid-connected inverters, as shown in Fig. 5.2. These topologies vary from one application to another depending on cost, performance and efficiency.

5.4.1 First Order Filter (L)

The first order L filter is not able to provide sufficient attenuation of the current ripple due to low attenuation, which is -20dB/decade over the frequency range. In order to use this type of filter, either a high switching frequency is required or the inductance would need to be large enough to achieve acceptable harmonic emissions in the inverter output.

5.4.2 Second Order Filter (LC)

Second order, passive LC type filters are widely used in grid-connected inverters. This topology has the advantage of having a higher attenuation rate of -40dB/decade.

As shown in Fig. 5.2 (b), a shunt capacitor is added to an L filter, to improve the output voltage waveform and reduce the high frequency components. The resonant frequency can be calculated from equation (5.1). It is important that the filter resonant frequency is chosen such that it is not close to the inverter switching frequency.

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{5.1}$$

5.4.3 Third Order Filter (LCL)

As mentioned earlier, first order filters are not able to provide sufficient attenuation of the current ripple. For this reason, an additional series inductance is added. The main advantage of using an LCL filter is to produce better attenuation of inverter

switching harmonics compared with the previous filters. In doing so, it is possible to use a lower switching frequency, and as a result reduce the switching losses. The LCL filter provides attenuation of -60 dB/decade. On the other hand, adding an additional inductor to the filter will increase the overall inverter cost.

There is also the fact that the LCL filter provides better decoupling between filter and grid impedance, and a lower ripple current in the grid inductor. In other words, as the current ripple is reduced by the capacitor, the grid side impedance will suffer less stress compared with the LC filter topology [149]. The resonant frequency of LCL filter can be obtained from the following equation.

$$f_o = \frac{1}{2\pi} \times \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{5.2}$$

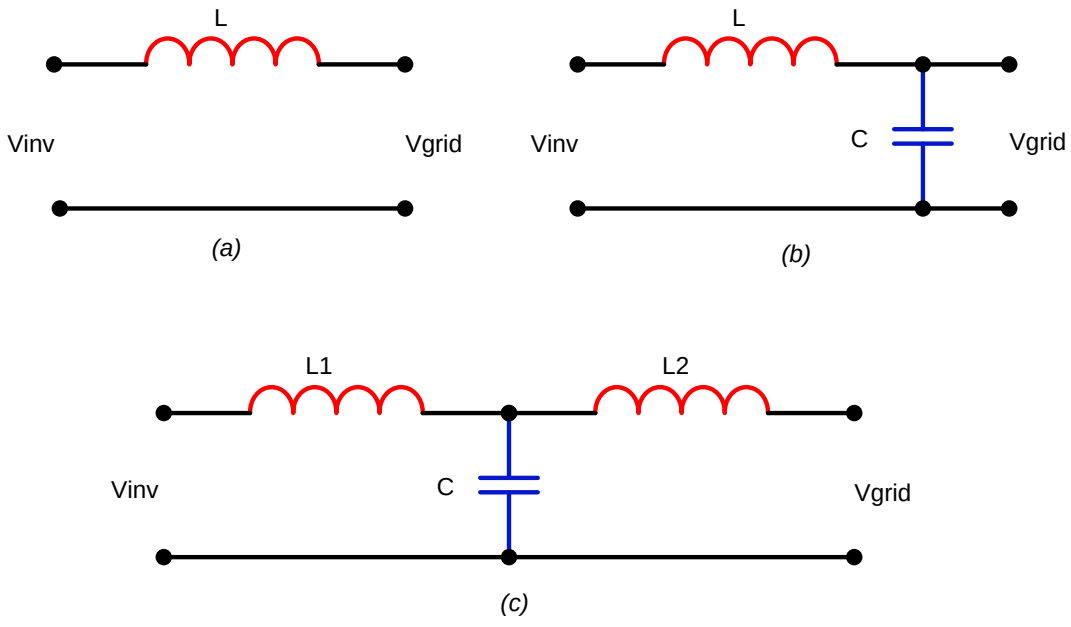


Fig. 5.2: AC Filter circuits

It is common in industrial applications to increase the size of the filter capacitor and reduce the size of the inductor whilst retaining the same filter cut-off frequency [150]. This is because the power losses caused by the equivalent resistance (R_L) of the filter inductor can be reduced. In this case, the cost, size and weight of the overall filter can normally be reduced with lower inductance values. However, if a large capacitor is used, the inductor current ripple will tend to increase [137], and this will also increase the losses in the inductor. In addition, the maximum output current ripple depends on the modulation scheme and the switching frequency [151]. *Benjamin et al.* [152] designed the AC filter for the Neutral Point clamped inverter and explained that the maximum AC current ripple, which is linked to the inductor should not exceed 10-25% of the rated amplitude value of the inverter output current.

For the filter inductance design, the three-level HBDC inverter can be modelled as one half wave buck converter, and the grid is modelled as a half sinusoidal waveform voltage, as illustrated in Fig 5.3 [152]. In this case, the filter inductance can be calculated from the following equation:

$$L_{inv} = \frac{\frac{V_{dc}}{2} - V_s}{2 \cdot \Delta I_L} \cdot \frac{D}{f_{sw}} \tag{5.3}$$

where the output current ripple is a function of time, D is the duty-cycle ($D(t) \approx M\,Cos(wt)$), and M is the modulation index.

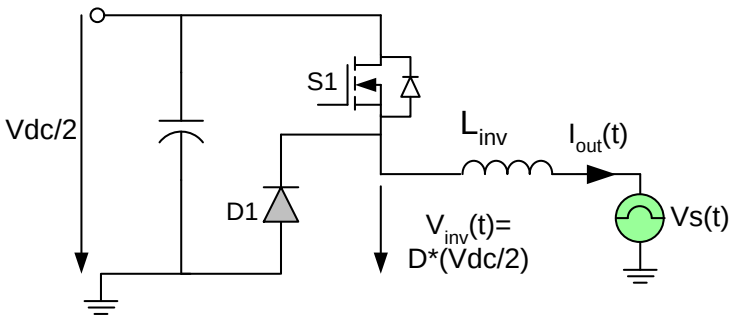


Fig 5.3: Simplified circuit of NPC

The current ripple at the output is the largest for a duty cycle of 50% [152]. Therefore:

$$L_{inv} \approx \frac{V_{dc}}{16 \cdot f_{sw} \Delta I_{L\,max}} \tag{5.4}$$

In this research, an LC low-pass filter was used in an experimental grid connected inverter PV system. The cut-off frequency of this filter was 1450Hz. This LC low-pass filter is made up of a 0.4mH inductor and a 30μF of capacitor. However, as measured by a RCL meter, in practice, the exact value of the inductor and capacitor are 0.497mH (approximately 0.5mH) and 30.092μF (approximately 30μF), and hence the actual cut-off frequency of the LC low-pass filter is approximately 1300Hz instead of the designed 1450Hz.

5.5 Isolation Transformer

The three-level half-bridge inverter is connected to the supply network via an isolation transformer and a Variac. An isolation transformer is used to protect the mains supply from any DC current component during the experimental tests, and the Variac is used to match the inverter`s output voltage to the supply. It is important to point out that the isolation transformer is only present in the test rig, and the purpose of this research is to operate the inverter as a transformerless grid-connected configuration.

The use of an isolation transformer will present additional impedance to DC current, due to the primary winding resistance of the transformer. Hence, its inclusion should have little impact on the tuning of the PI controller.

5.6 Grid-Connected Inverter Connection Sequence

The process of the inverter connection to the grid can be summarized with the following points in conjunction with Fig. 5.1.

- Initially, switches 1 and 2 are both switched OFF. Resulting in, no applied voltage on the DC link of the inverter, and no network voltage appears at the inverter output.
- Microcontroller operation is started, which is used to create a unipolar PWM signal to control the switches.
- Switch 1 is switched ON, so that a DC link voltage is established at the inverter input. The current demand of the inverter is set to the reference level
- Switch 2 is now switched ON. At this point, the Variac output voltage is zero, and is then gradually wound up, and the voltage across the secondary side of the isolation transformer is increases. At this point, the inverter controller has to work hard in order to counter balance the network voltage and the inverter output voltage.
- The Variac is gradually wound up until the output voltage of the inverter reaches the maximum allowable given the DC link voltage. At this point, the inverter is fully grid-connected.

5.7 External Measurement of the current DC Component

In order to assess the performance of the scheme, the output DC current component is measured. This measurement is achieved by connecting a series shunt resistance in the inverter output between the load and AC filter. The voltage across this shunt is passed through an RC Low Pass Filter (LPF) with a cut-off frequency of 1 Hz to reject the 50Hz AC component. This circuit is housed in an aluminium box and fixed to a large heat sink with a fan, as shown in Fig. 5.4, to ensure no loss of accuracy due to resistance heating effects. In order to eliminate the possibility of common-mode leakage affecting accuracy, a battery-operated Digital Multi-Meter (DMM) is used to measure the DC voltage. The DC voltage measured by the DMM

is then scaled by the shunt resistance value to determine the DC current component in the inverter output.

This measurement is not necessary for normal operation of the inverter, and is only introduced here to evaluate the performance of the auto-calibration technique.

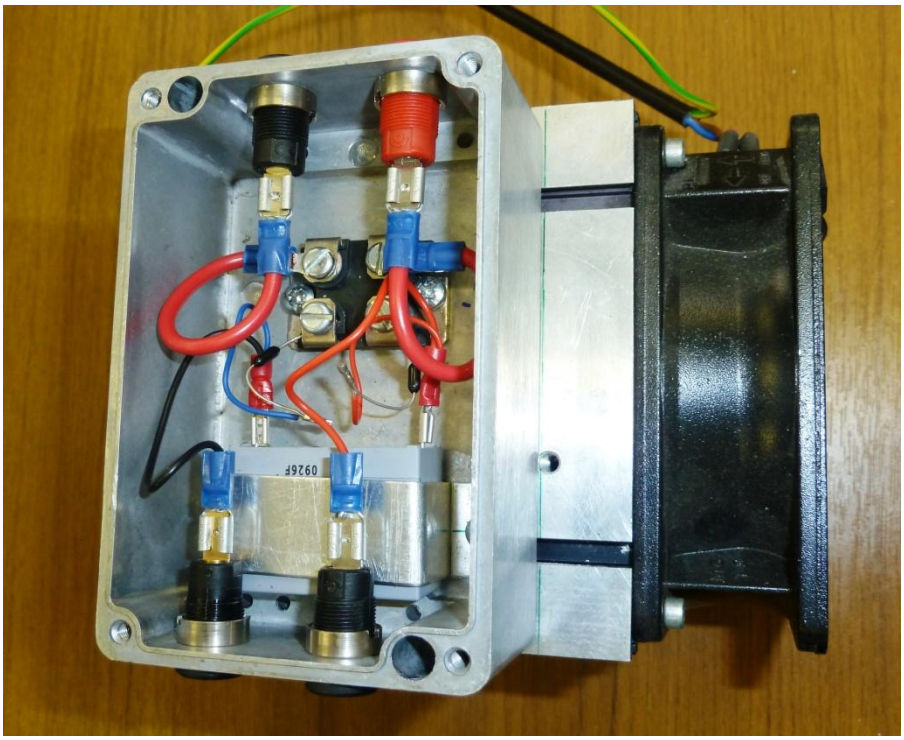


Fig. 5.4: DC current measurement in inverter output

5.8 Controller Circuit

The microchip dsPIC33FJ256MC710 is used to control the devices by executing a user program. This device is a high-performance, 16-bit digital signal controller (DSP). Some features of the controller are briefly presented in Table 5.1. Further details can be found in the dsPIC33F family data sheet [153].

Table 5.1: Some Features of the dsPIC33F

Features	Unit
Program Flash Memory (kbyte)	256
Pins	100
I/O Pins	85
CPU Speed (MIPS)	40
RAM (kbyte)	30
Timer 16-bit	9
Internal Oscillator	7.37 MHz
ADC	2 ADC, 24 channels
Motor Control PWM	8 channels
Temperature Range C	(-40°C to +85°C)
Operating Voltage Range (V)	3 to 3.6 volt

The full FLEX base board shown in Fig. 5.5 is used to control the three-level half-bridge grid-connected circuit. The dsPIC 33FJ256MC710 is programmed using MPLAB IDE software (v8.46), which is an Integrated Development Environment (IDE). This software was installed and run on a PC to provide a development environment for embedded system design. The code was compiled using the MPLAB C30 compiler. The PC hardware is connected with the MPLAB ICD 2 through a USB port to program the microchip (dsPIC33FJ256MC710). More details of the software settings are provided in Appendix A.

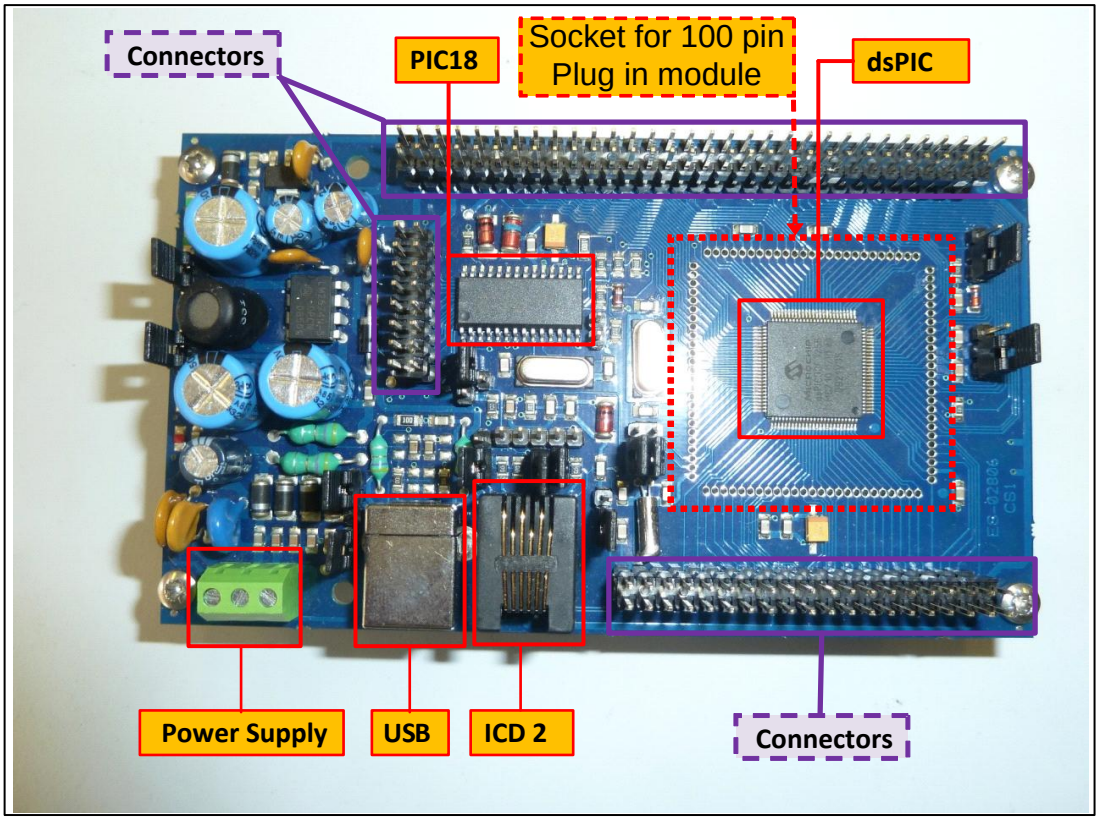


Fig. 5.5 The full FLEX base board of dsPIC33FJ256MC710.

5.9 Inverter Printed Circuit Board (PCB) Design

There are many basic rules and guidelines for the design of Printed Circuit Board (PCB), which should be followed to improve the performance of the inverter. Relevant application notes are produced by Texas Instruments [154], SGS Thomson [155] and *Jones* [156]. For the purpose of minimising loop inductance between positive and negative DC link traces, both traces should be run directly over each other. Also to minimise the noise, which is produced by the microcontroller, the bottom layer area of the microcontroller should be grounded and the area should extend about ¼ inch outside the outline of the device.

The experimental test circuit of a three-level DCHB inverter (Fig. 5. 6) consisted of four main switches in one leg (S1, S2, S3 and S4), two diodes and two power supplies (Vd1and Vd2). Moreover, it consisted of five sub-circuits: controller, gate

driver, current sensors, voltage sensors, and protection circuit. Each of these sub-circuits is briefly described in the following sections.

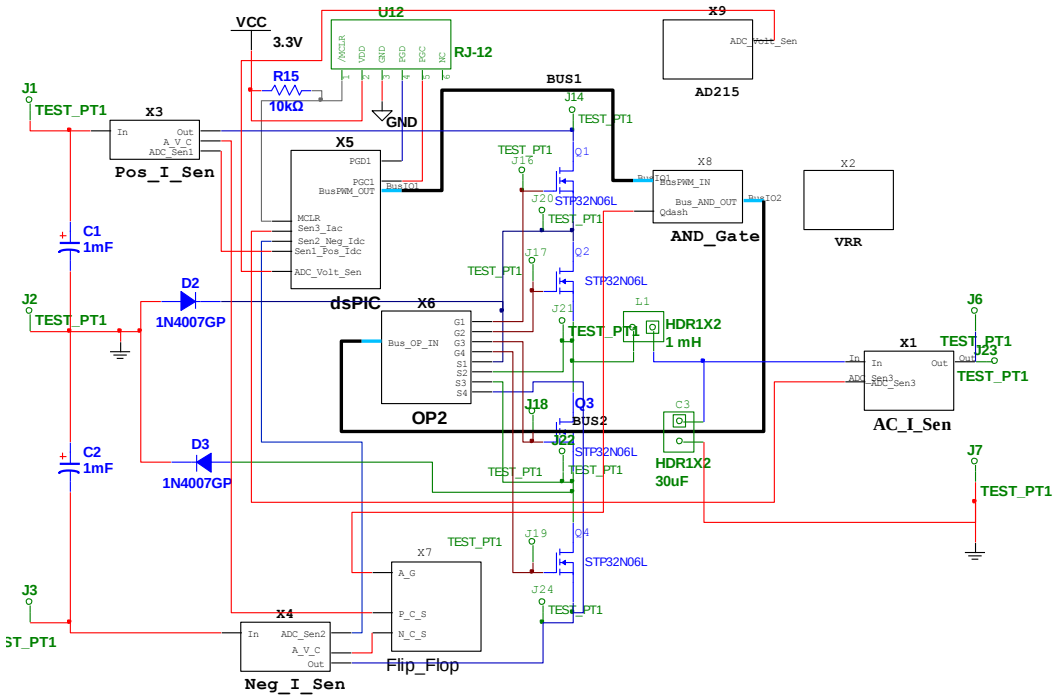


Fig. 5. 6: Schematic circuit for the test circuit of three-level DCHB inverter

5.9.1 Microcontroller Circuit

Two microcontrollers are used; the first one is dsPIC33FJ128MC706 which has been designed with the inverter circuit in one circuit (see Fig. 5.7). The second one is used as an external circuit and is a separate package, which is mentioned in section 5.8. The reason for using two is that more than one circuit has been designed and this is due to the noise interface. This is also related to why poor technology has been used to make a printed circuit board and only two layers are used. Table 5. 2 shows peripheral features of both controllers.

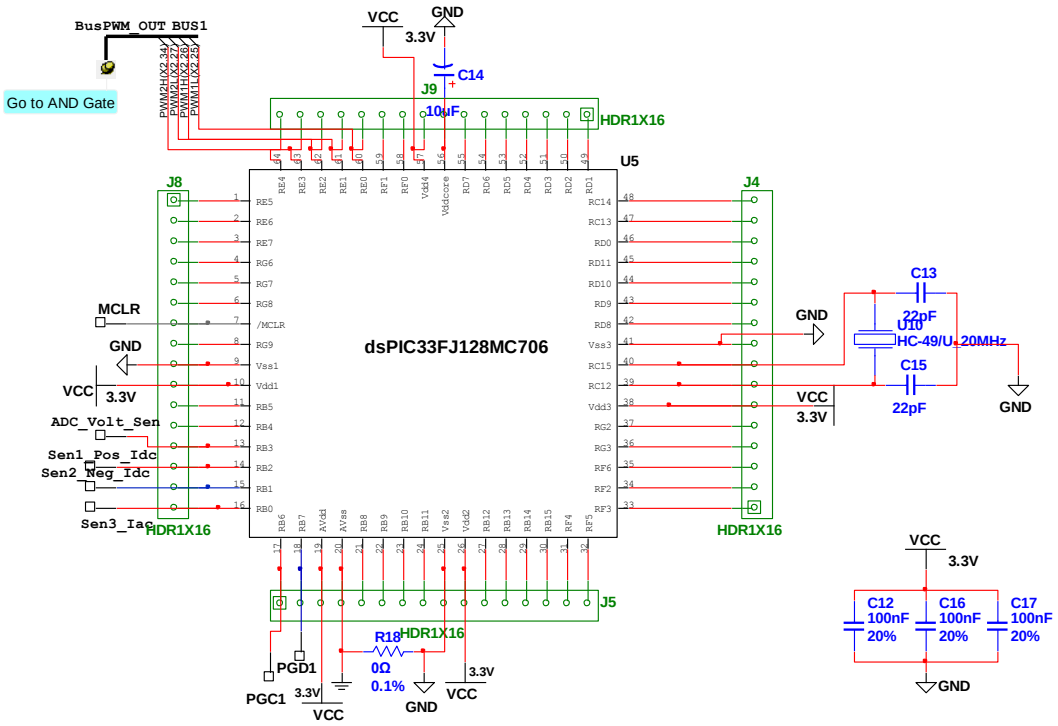


Fig. 5.7: Schematic circuit for the controller circuit

Table 5. 2: dsPIC33F Specifications

Device	Pins	Program Flash Memory (Kbyte)	RAM (Kbyte)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	ADC	UART	SPI	I2C™	Enhanced CAN	I/O Pins	Packages
dsPIC33FJ128MC706	64	128	16	9	8	8	8ch	2AD 16 Ch	2	2	2	1	53	PT
dsPIC33FJ256MC710	100	256	30	9	8	8	8ch	2AD 24 Ch	2	2	2	2	85	PF, PT

5.9.2 Current Sensor Circuit

An LTS25-NP current transducer is used. This type of current sensor is flexible in terms of connection and can be used with different rates of current (see Table 5.3). The LTS25-NP consists of 9 pins. Pins 1-6 represent the connection layout of the current transducers according to Table 5.3. The other three pins, shown in Fig. 5.8, are connected as following. The output pin is connected to the input pin of dsPIC33FJ128MC706 through a voltage divider and clamped diode and is also

connected to protection circuit before voltage divider. Supply voltage pin is connected to 5V supply. The zero volt pin is connected to digital ground.

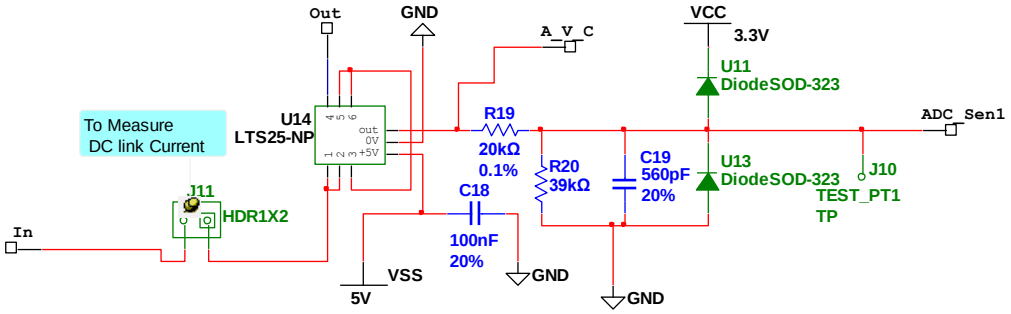
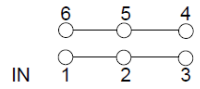
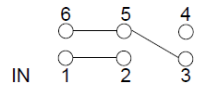
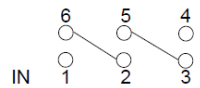


Fig. 5.8: Schematic of DC link current sensor

Table 5.3: Different connection of LTS25-NP

Number of primary turns	Primary nominal r.m.s. current I_{PN} [A]	Nominal output voltage V_{OUT} [V]	Primary resistance [mΩ]	Primary insertion inductance [µH]	Recommended connections
1	LTS 6-NP ±6 LTS 15-NP ±15 LTS 25-NP ±25	2.5 ± 0.625	0.18	0.013	
2	LTS 6-NP ±3 LTS 15-NP ±7,5 LTS 25-NP ±12	2.5 ± 0.600 2.5 ± 0.625 2.5 ± 0.625	0.81	0.05	
3	LTS 6-NP ±2 LTS 15-NP ±5 LTS 25-NP ±8	2.5 ± 0.600 2.5 ± 0.625 2.5 ± 0.625	1.62	0.12	

5.9.3 Voltage Sensor

An AD215 high speed isolation amplifier is used to sense the output voltage and it is used as forward voltage in PI control method. Fig. 5.9 shows the circuit connection of the isolation amplifier, which consists of ± 15 VDC, an auxiliary circuit to produce 2.5V offset and input terminal connection.

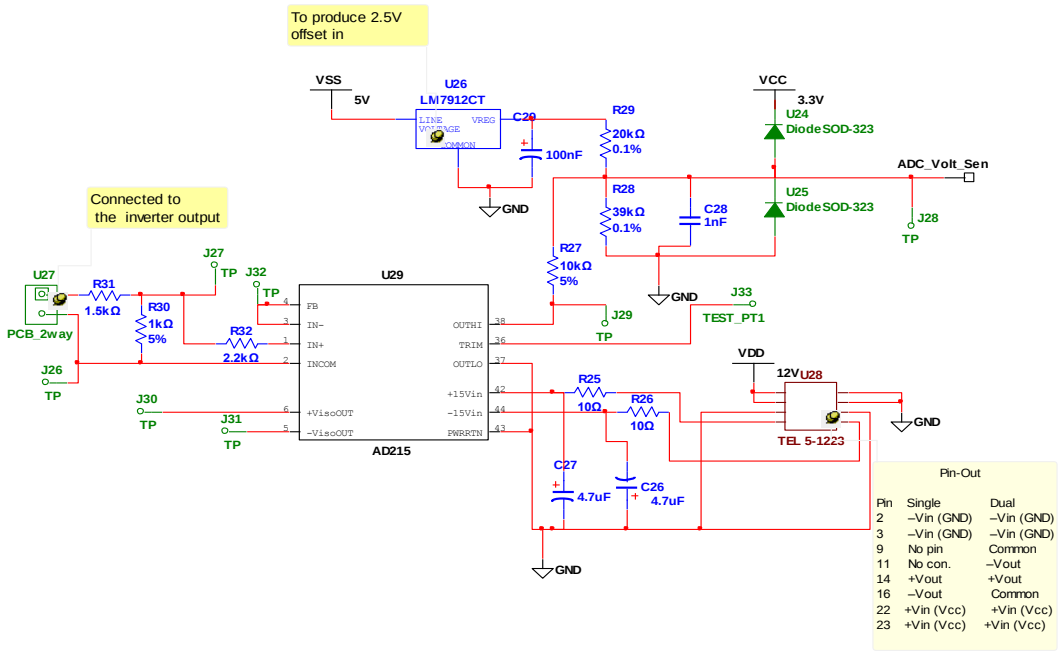


Fig. 5.9: Schematic circuit of AD215

5.9.4 Protection Circuit

Protecting the inverter circuit against over current can be done by switching the power MOSFT OFF. The output of a positive and negative DC link current sensor is connected to a dual LM393, as shown in Fig. 5.10. The output of LM393 is connected to SN74LVC74 and the output of SN74LVC74 is connected to an AND gate, as shown in Fig. 5.11. In case of fault the comparator will activate the flip-flop. The flip-flop will send a signal to active an AND gate, which in turn isolates the PWM signals between the microcontroller and optocoupler.

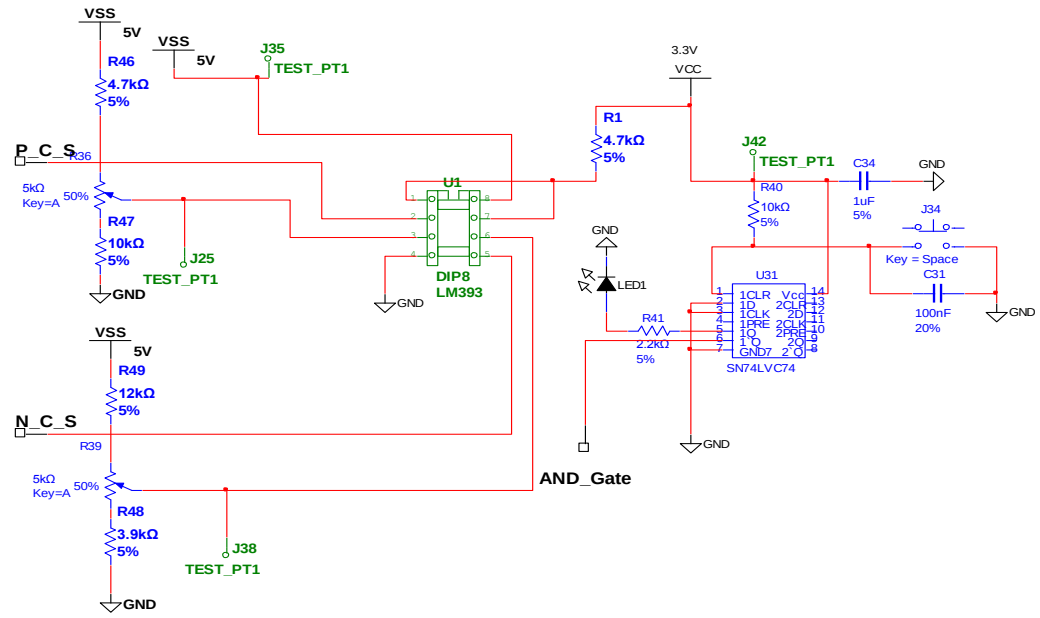


Fig. 5.10: Schematic circuit of LM393 and SN74LVC74

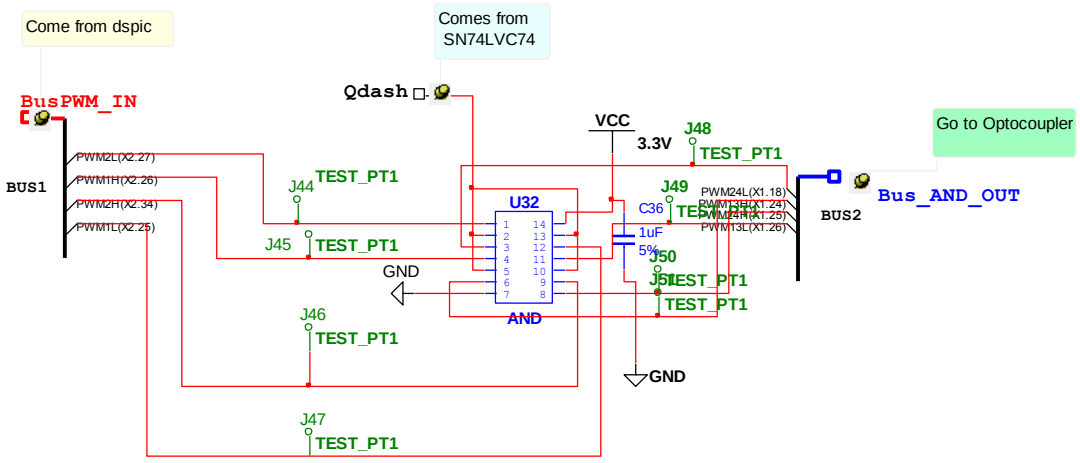


Fig. 5.11: Schematic circuit of AND Gate

5.9.5 Circuit Layout

Fig. 5.12 shows the printed circuit board layout where the microcontroller area is ground to minimise the effect of stray inductance in the three-level half-bridge inverter circuit design.

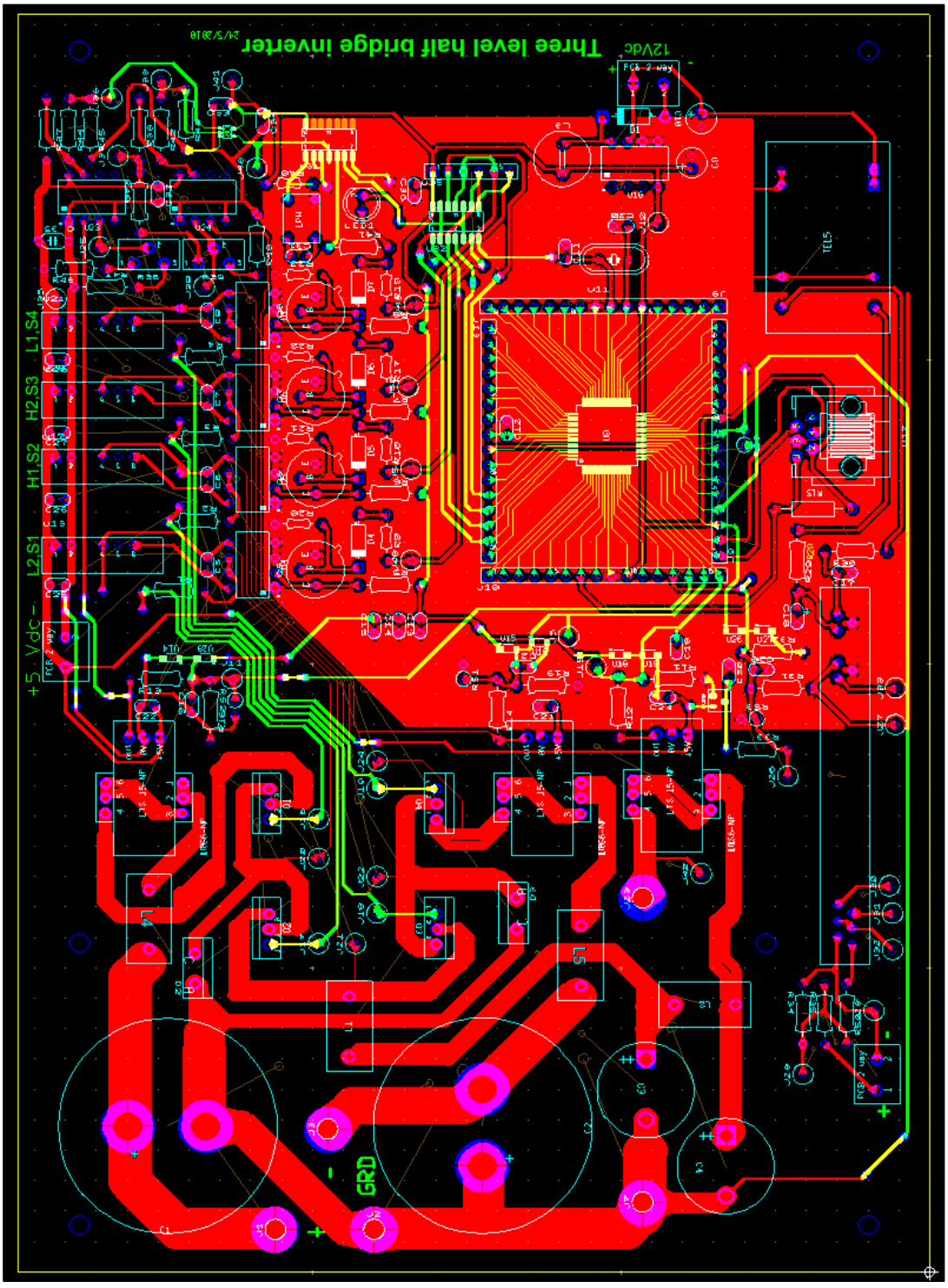


Fig. 5.12: Three-level half bridge printed circuit board circuit

Bottom copper Top copper

5.10 Zero Crossing Detection (ZCD)

There are many methods of synchronisation to the grid, such as Phase-Locked-Loops (PLL) and Zero Crossing Detection (ZCD). ZCD is a classic method of grid synchronization, because it consists of a simple circuit and an uncomplicated software program. At the same time, this method has disadvantages compared to the PLL method. The first problem is that the zero crossing points only occur once every half cycle, and this can affect the dynamic performance in a circuit connected to a weak grid [157]. The second problem is that the noise occurring around the zero crossing points on a mains signal, may produce multiple zero crossings, which will corrupt phase tracking.

The input of the ZCD was connected to the grid voltage, at the inverter to grid connection point, as illustrated in Fig. 5.1. The 230V AC at that point was converted to 9V AC using a 1.5VA isolated transformer. A simple LPF is required to remove the noise and high frequency components in the voltage supply, which could cause spurious zero crossing detections. The use of a LPF at the input of the ZCD can introduce a delay. The lower the cut-off frequency of LPF, the greater will be the delay appearing in the filtered signal.

The output of the filter is passed through a comparator that produces a square wave output (V_{out1}) as shows in Fig. 5.13. The output waveform of the comparator (LM393N) is applied to the base of the transistor through a base resistor, and then passed through the isolated gate to isolate the ZCD signal (see Fig. 5.14). The output gate signal (HCPL2601) is applied to the buffer (AD820AN), and the output of this buffer is connected to the ADC pin in the control circuit.

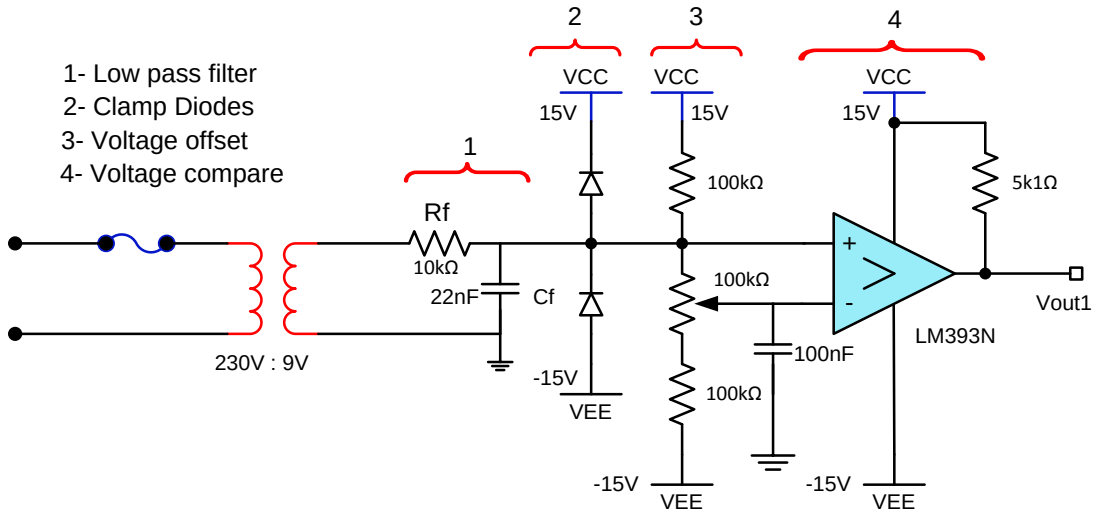


Fig. 5.13: Basic ZCD circuit

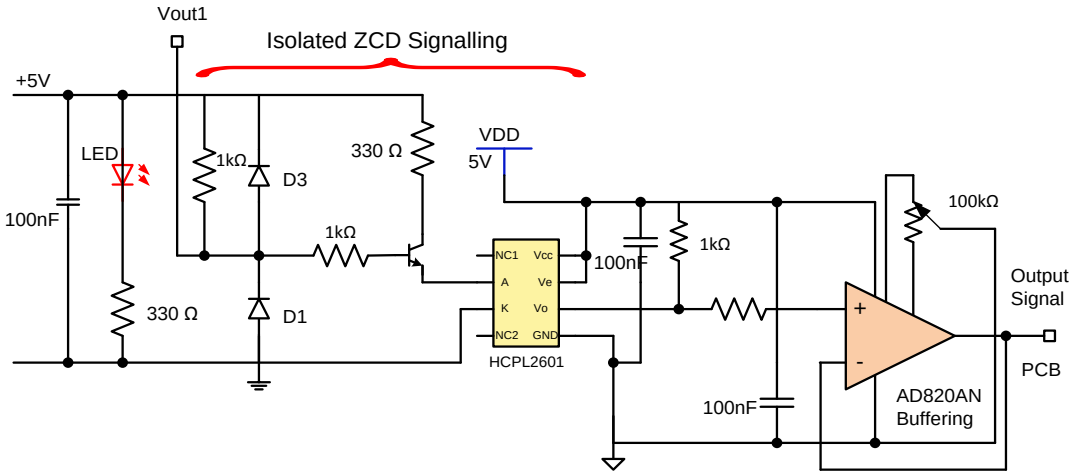


Fig. 5.14: Isolated ZCD circuit

5.11 Circuit Calibration

Initial test and calibration was carried out before using the zero crossing detection to synchronise the inverter to the grid. In this test, the Variac was connected to the input of the ZCD circuit as mentioned in the previous section. The ZCD circuit output was connected to the input of the ADC pin in the microcontroller using coaxial cable to minimise interference on the signal. Fig. 5.15 shows the photograph of the ZCD circuit.

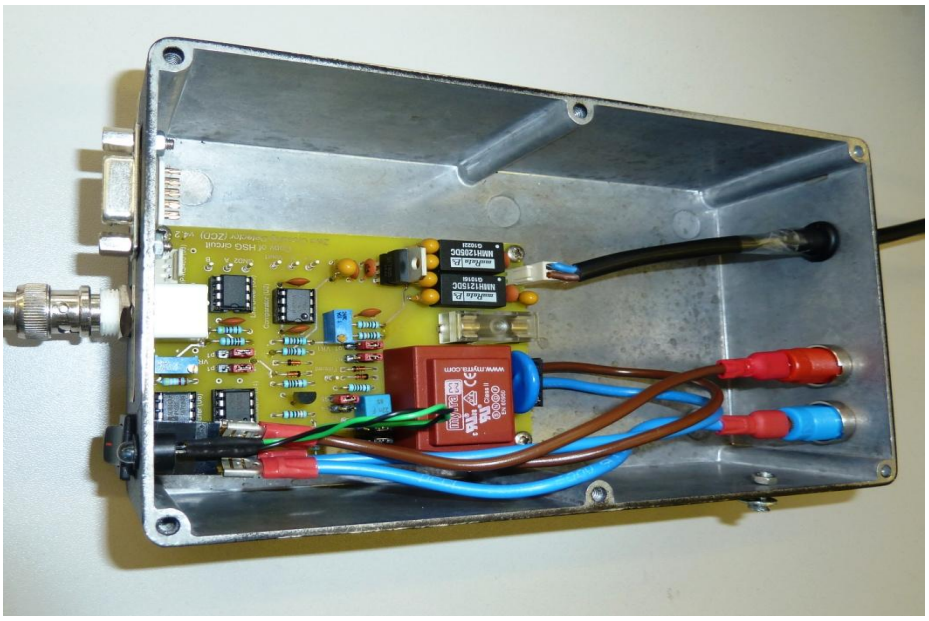


Fig. 5.15: Layout of ZCD circuit

When the Variac output voltage is applied to the ZCD input, the output square wave signal of the ZCD or the input signal of ADC pin will vary from 0.0 to 3.3V, which equates to (-1 to 1) in signed fractional logic format on the dsPIC33F; more details are provided in Appendix A. The period of this square wave can then be measured using a digital counter. The software program produces a sinusoidal reference signal, which is synchronised with the square wave signal from the ZCD. For diagnostic purposes, these signals are recorded in an array and presented via a Data Monitor Control interface (DMCI). Fig. 5.16 shows the ZCD and the reference signals running simultaneously. The X-axis in this figure represents the sample number of storage array; the length of it (1200) represent's three cycle's length of the waveform. The use of a large array describes the change, which is even occurring in the waveform for more than one cycle. The Y-axis shows the magnitude of the ADC signals in signed fractional logic format (-1 to 1) [153], which is equal to the normal operating voltage of ADC pins (0 to 3.3V). For example, the current output can be calculated from the following equation [81].

$$V_{out} = 2.5 \mp (0.625 \times I_P / I_{PN}) V \tag{5.4}$$

Where:

I_{PN}: Primary nominal r.m.s. current (At)

I_P: Primary current (At)

V_{out}: Analog output voltage @ I_P

When I_P = 0, in this case, V_{out} = 2.5V. As described before, the normal operating voltage of the ADC pin may vary between 0 to 3.3V. So in this instance, the output voltage of the current sensor will be reduced using a voltage divider to coincide with the midpoint of the ADC pin maximum voltage, i.e. around 1.65V, which represents zero in signed fractional logic format (-1 to 1). The magnitude of inverter reference current is 7 A, which is equivalent to (0.13) in Q15 format.

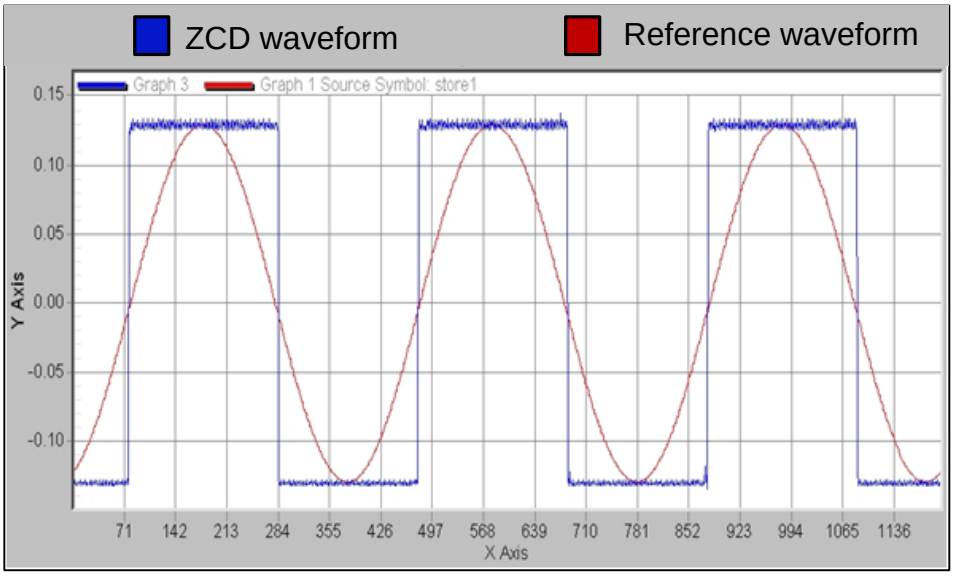


Fig. 5.16 ADC waveforms of reference and ZCD
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).
I_{mRef} = 7 A = Q15 (0.13)

For more information, Fig. 5.17 shows the basic circuit of the current sensor interface. This circuit consist of two parts, where the first is a voltage divider with LPF. The voltage divider was used to reduce sensor output voltage to a desirable level, and the LPF was used to remove any high frequency components. However, the compromise between noise reduction and avoiding signal delay should be taken into account when selecting the cut-off frequency of the filter. The second part is a clamp diode protection circuit, before the analogue signal is fed to the ADC pin of

the microcontroller. The clamp diode protection circuit is used to protect the microcontroller input from overvoltage.

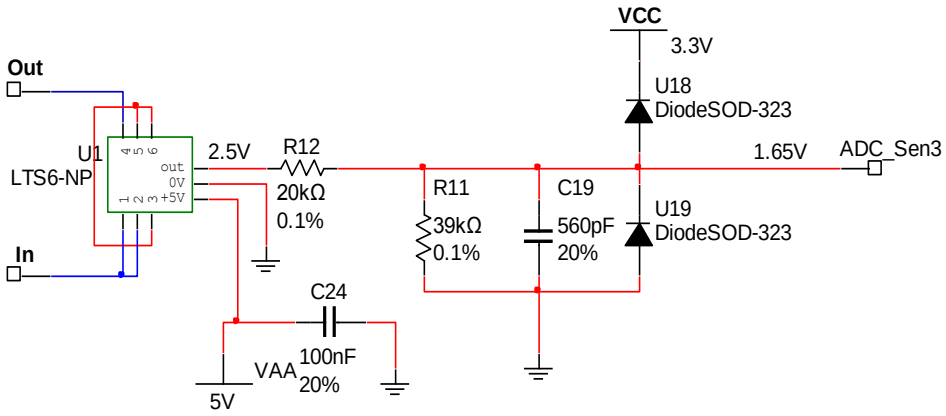


Fig. 5.17: Basic circuits of current sensor and voltage divider

Fig. 5.18 illustrates the sum of DC link current measurement, and ADC signal of ZCD and Reference waveforms. The measurement of DC link current was obtained by adding the positive and negative components of the DC link current waveforms. From the Fig.5.18 below, we can see that the ZCD waveform is synchronised with the sum of DC link current measurements. This test used a resistive load under a closed loop condition, and the magnitude of DC link current was 7A, which is equivalent to (0.13) in signed fractional logic format.

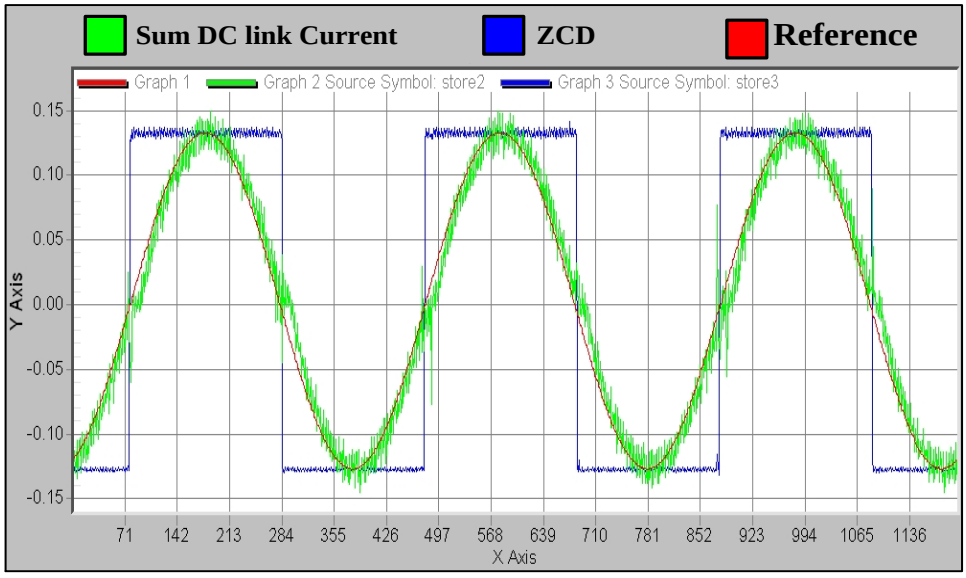


Fig. 5.18: Sum of DC link current measurement, ADC signal of ZCD and Reference waveform
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).
$I_{m\ DC\ link}$ = 7 A = Q15 (0.13)

Fig. 5.19 shows the result obtained from the three-level half-bridge inverter circuit operated to supply a resistive load under closed loop conditions. This result shows the performance of the ZCD, and how it is synchronising to the grid voltage with switching PWM of the inverter.

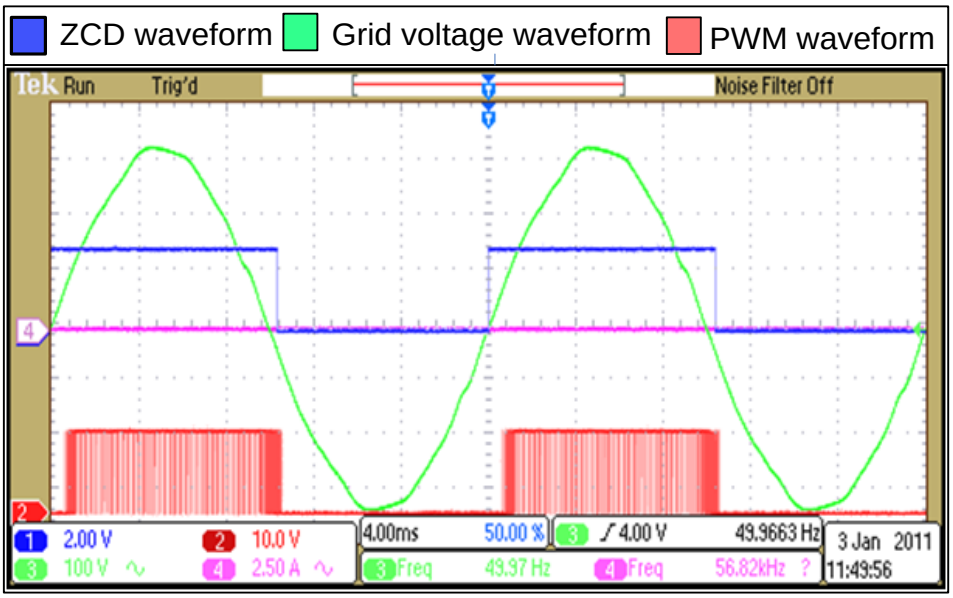


Fig. 5.19: Schematic of first ZCD test

5.12 Summary

This chapter has described the initial experimental test of a three-level half-bridge inverter using a resistive load. The inverter and ZCD test circuit were designed using Multisim software, after making the PCB. The circuit's components were selected with suitable values of voltage and current rating. A description of the grid-connected hardware has been provided, as described in early chapters. This test used a resistive load in a closed loop condition to observe the behaviour of DC link current sensors. This was done when applying the auto-calibration technique and injecting DC offset to these current sensors. The inverter output current was also synchronised with the grid voltage using a ZCD.

CHAPTER 6

TEST INVERTER, RESULTS, AND DISCUSSION

6.1 Introduction

This chapter describes the experimental setup and results for the grid-connected three-level half-bridge inverter. The chapter is divided into three sections. Section 6.2 gives a general description of the experimental setup of the test circuit. This is includes ratings of power devices and diodes, drive circuit description, software implementation and PWM signal generation. Section 6.3 discusses the operation of the three-level half-bridge inverter and associated current measurements. Section 6.4 presents the inverter performance with auto-calibration in operation. Finally, Section 6.5 provides a brief summary of results.

6.2 Experimental Setup of the Grid-Connected Inverter Test Circuit

The test rig consists of three main parts, namely the input DC source, the three-level-half bridge inverter, and the grid. Fig. 6.1 shows the experimental setup of the test circuit. The inverter is fed by two 30V DC power supplies, connected in series across the input of the inverter to produce a total input voltage of 60V DC. The inverter is designed to work with a current level of up to 10A rms. Due to the lack of availability of an isolation transformer with this rating, the inverter was operated in 5A rms current level.

Two series 2200μF, 100 V DC aluminium electrolytic capacitors are connected across the inverter input terminals. These capacitors are located close to the power MOSFET bridge devices to minimize stray series inductance. A DC link current measurement is provided using two LTS25-NP Hall Effect current sensors. This type

of current transducer has been widely used in power electronic drives and applications, as described in [71] [72].

The Hall Effect current sensor is capable of sensing DC, AC, pulse and mixed current signals, [81] and also provides full isolation between the power and the controller circuits.

Fig. 6.2 shows the complete test circuit of the three-level half-bridge grid-connected inverter. This circuit was first tested using a resistive load bank before being operated in grid-connected mode. This ensured safe operation and allows integrating ZCD into current control, as will be described in section 6.3.

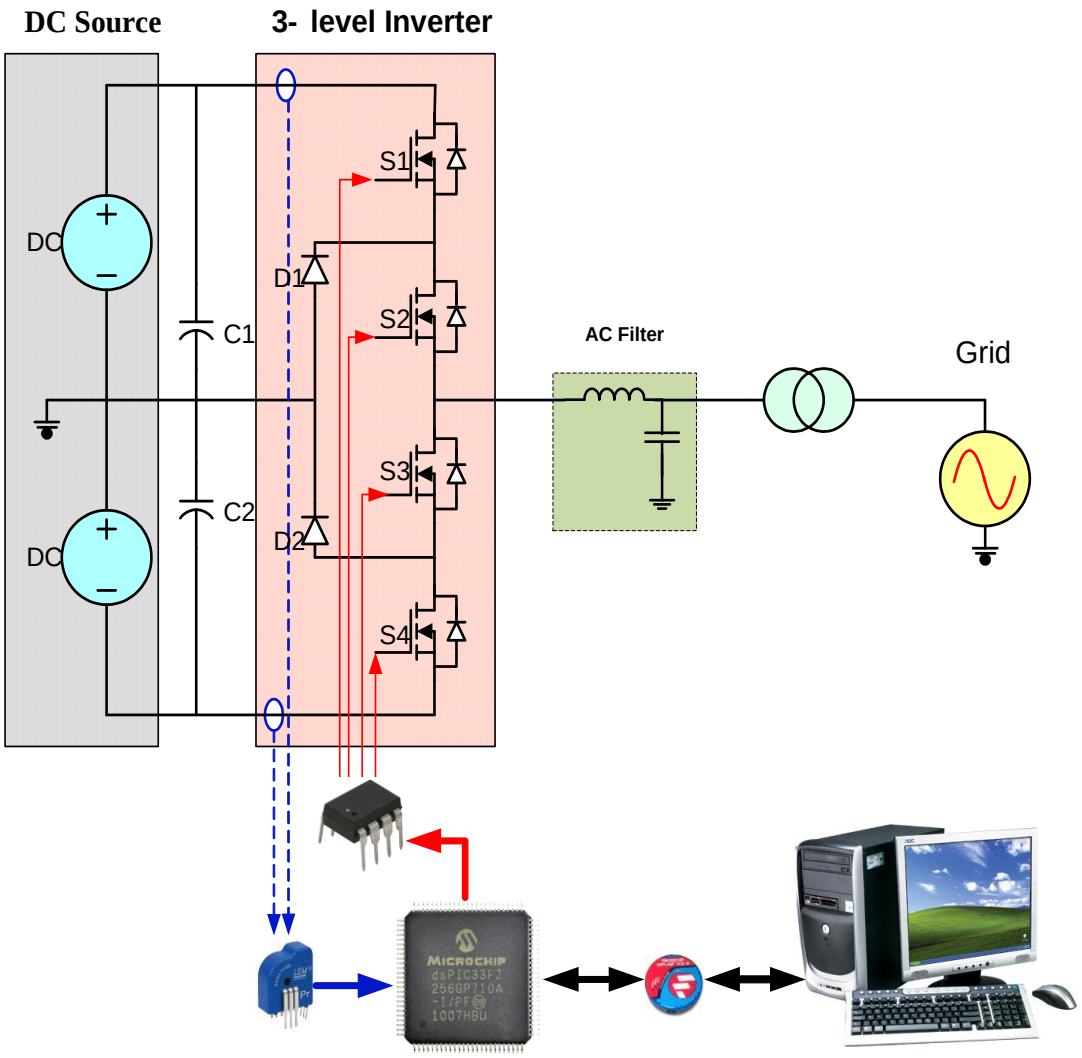


Fig. 6.1: Schematic of the experimental test rig

Fig. 6.2: Complete test rig of three-level half-bridge grid connected inverter

6.2.1 Power Devices and Diodes

The converter circuit shown in Fig. 6.1 consists of four switches and two diodes. There are a number of factors which should be considered in the choice between IGBTs and power MOSFET devices. IGBTs have become widely used in many power applications due to their low conduction losses and high voltage and current ratings [158]. On the other hand, an external anti-parallel diode is needed in inductive load applications, where freewheeling current flow is required. Also, with IGBTs, the turn off time is affected by a tail current [159], which is not found in power MOSFETs.

Unlike IGBTs, MOSFETs have an internal body diode between the drain and the source as part of the fabrication process. The diode allows the conduction of freewheeling currents through the MOSFET when the switch is turned off, which is convenient in circuits with inductive loads. A major advantage of MOSFET is the

absence of tail current device switch off. This is an advantage for the auto-calibration technique used in the grid-connected inverter.

A new development in fabrication technology of power MOSFETs has increased the operating voltages up to 800V with reduced channel resistance value $R_{DC(on)}$. This improvement in fabrication technology has increased the use of MOSFETs in higher power inverter applications, such as three-phase motor drives.

In addition, the switching speed of MOSFETs is higher than IGBTs, and can be used to reduce the size of the filter components.

Two ultrafast recovery diodes were used as the clamping diodes. Table 6.1 summarises the main components used in the three-level half-bridge inverter.

Table 6.1: Main component list of the proposed inverter

Component	**Manufacturer**	**Part Name**	**Voltage rating**	**Current rating**
Power diodes D_1-D_2	STMICROELECTRONICS	STTH3010	1000V V_f=1.3V	30A
MOSFET S_1-S4	FAIRCHILD Semiconductor	FDP3682	100V V_{GS}=15V	32A
DC capacitors C1-C2 2200μF	BHC Aerovox	ALS30A2 22DA100	100 V	--
AC filter capacitor C = 30μF	--	BB-11-77	250 V_{AC}	--
AC filter Inductor L = 0.400*m*H	--	--	--	25 A RMS

6.2.2 Driver Circuit

In most power converter applications, the output signal of the microcontroller does not have the appropriate characteristics to drive power switches efficiently. Also, to protect the microcontroller from a possible overvoltage or over-current fault, it is necessary to isolate the low power side from the high power side, while the switching signal is still allowed to pass through. Therefore, it is recommended to have an isolated gate driver (optocoupler). The HCPL-3180 isolated gate driver was selected to drive the power devices in the three-level half bridge inverter, because it is suited for high frequency driving of power IGBTs and MOSFETs [160]. The output power of the optocoupler gate drive was provided by isolated DC/DC converters, which step-up the supply voltage from 5V to 15V.

6.2.2.1 Gate Driver Circuit Design

The power MOSFET gate driver circuit (HCPL-3180) consists of a primary side and secondary side circuit, as shown in Fig. 6.3. There is no electrical connection between the two sides. In the primary side, pin 2 is connected to a PWM signal through an auxiliary circuit, which will be explained later, and pins 1, 3 and 4 are connected to the digital ground of a microcontroller (dsPIC33FJ128MC706). In the secondary side, pin 8 is connected to a positive output DC/DC converter which is used to isolate and step up the voltage from 5V to 15V. Pin 5 is connected to a negative output DC/DC converter and the source of the MOSFET. A 1uF decoupling capacitor is connected across two sides of the DC/DC converter (NMF0515S) to overcome the noise generated from the power circuit. Pin 6 is connected to the gate resistance of the MOSFET.

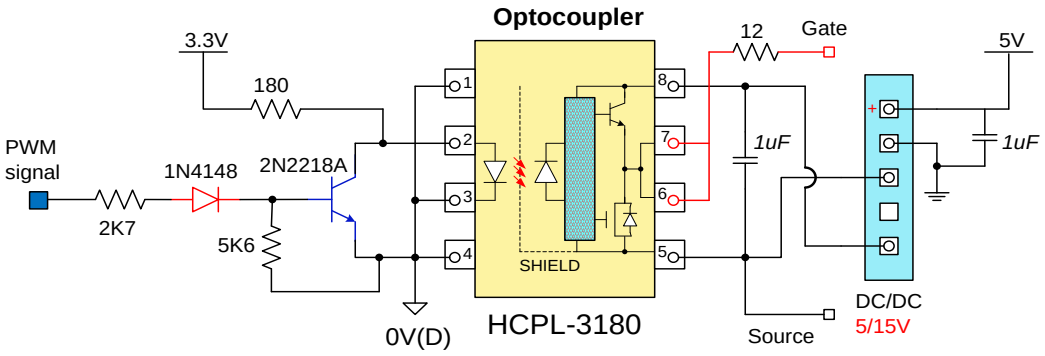


Fig. 6.3: Schematic circuit for the gate driver circuit

6.2.2.2 Auxiliary Circuit Analysis

The auxiliary circuit is used to minimise common mode rejection voltage (*dv/dt*) and protect the microcontroller and optocoupler from any over current.

To design a gate drive circuit, electrical characteristics of the involved devices (microcontroller, optocouplers, and power switches) are needed. Table 6. 2 describe the rating of microchips that is used to determine the resistance to limit the current in both sides of the optocoupler circuit. The current limiting resistor R_1 is used to limit the output current of the microcontroller pin. The diode (1N4148) is used to prevent any reverse current to the microcontroller. R_d is used to limit the input current of the optocoupler, as determined in equation (6.1). R_2 is used to adjust base current (I_B) of the transistor.

Table 6. 2: Data sheet information.

Data sheet	Parameter	Symbol	Unit
HCPL-3180	Input Forward Voltage	V_F	1.5 V
	Input Current (ON)	IF(ON)	10 mA
Transistor 2N2218A	DC Current Gain	h_{FE}	35 @ 10mA
dsPIC33F family	I/O ports	V_{OH}	2.4 V
	Maximum output current sourced by any I/O pin		0.4 mA

$$R_d = \frac{V_{DD} - V_F}{I_{F(ON)}} \quad (6.1)$$

$$R_d = \frac{3.3 - 1.5}{10} = 180\Omega$$

On state

$$I_1 = I_2 + I_B \quad (6.2)$$

From information given in above table

$$I_B = \frac{DC\ current\ Gain}{h_{FE}} = \frac{10\ mA}{35} = 0.28\ mA \quad (6.3)$$

$$I_2 = I_1 - I_B = 0.4 - 0.28 = 0.12\ mA \quad (6.4)$$

$$R_2 = \frac{V_{IGBT}}{I_2} = \frac{0.7\ V}{0.12\ mA} = 5.8k\Omega \approx 5.6\ K\Omega \quad (6.5)$$

$$R_1 = \frac{V_{OH} - V_{diode} - V_{IGBT}}{I_1} = \frac{2.4 - 0.7 - 0.7}{0.4} = 2.5\ K\Omega \approx 2.7\ K\Omega \quad (6.6)$$

6.2.2.3 Selecting the Gate Resistor (Rg)

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OL\ peak}} \quad (6.7)$$

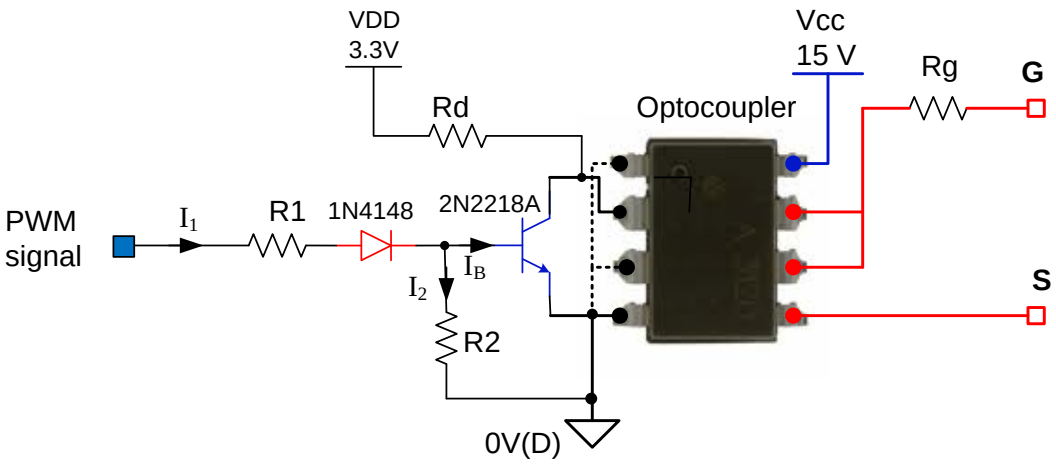


Fig 6.4: Recommended LED drive circuit for ultra-high CMR

6.2.3 Software Implementation

Fig. 6.5 shows the basic structure of the software programme written in C, then compiled and downloaded to the dsPIC for execution. Sequencing of the code is summarised below:

Initialization Setup:

Setup oscillator ();

    SetupTimer2 ();

    Setup PWM ();

    Setup variables ();

    Setup ports ();

    Setup ADC ();

    Setup A2D inputs ();

    Setup DMA0 ();

Setup Interrupt Priority Levels

Interrupt Serves Routine (ISR):

    Analogue signal acquisition

Inverter synchronisation using ZCD

PWM Interrupt

DMA Interrupt

Auto-calibration

Closed loop current control with feed-forward and output digital signals

More details of all the C program codes, the dsPIC settings, and the interrupt serves routines are given in Appendix A.

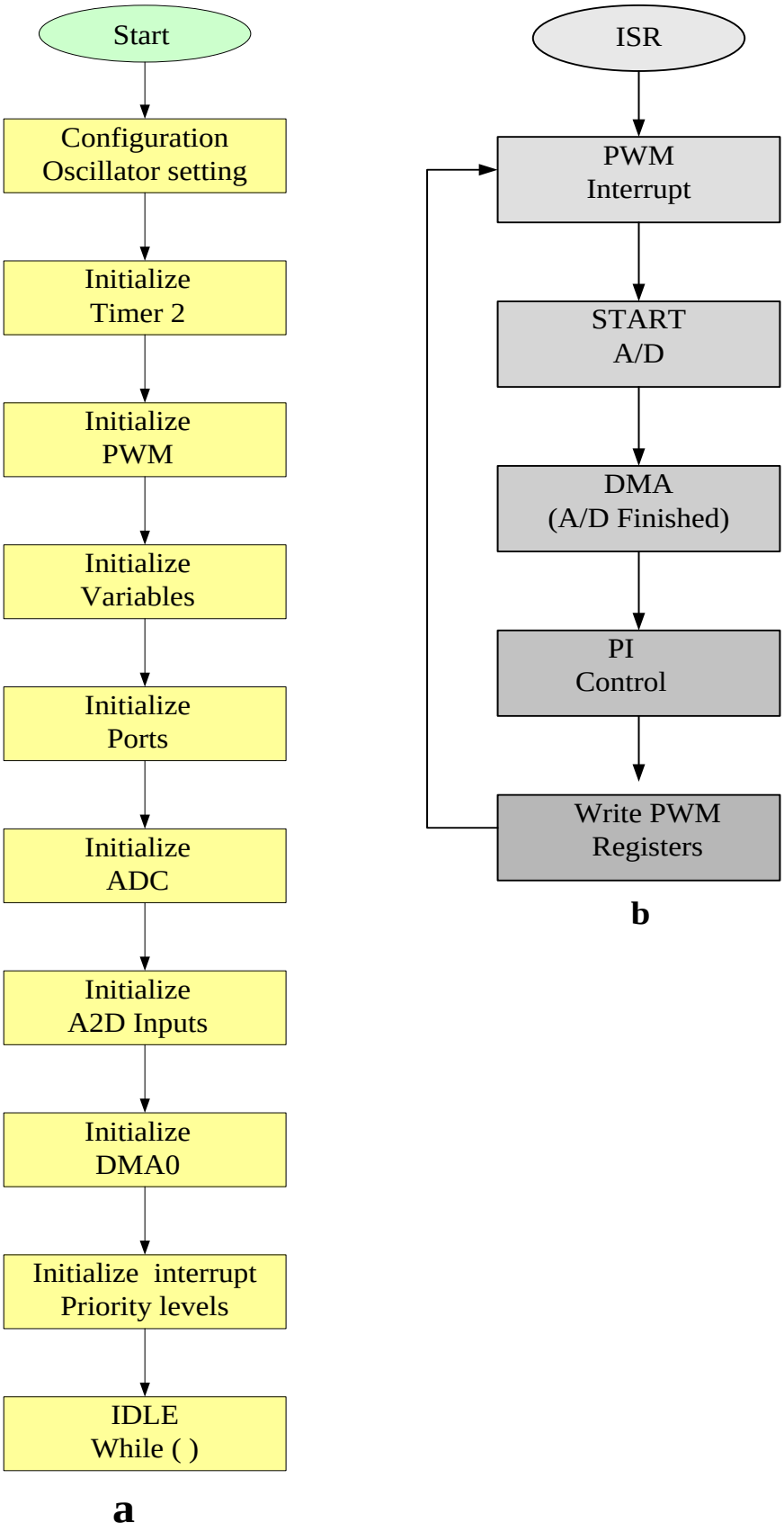


Fig. 6.5: Software flow diagram (a) Initialization Setup and (b) Interrupt Serves Routine

6.2.4 PWM Signal Generation

For this scheme, it is important to know the switching states of the three-level half-bridge inverter. This is necessary to determine the behaviour of DC link current during each of these different states. Fig. 6.6 shows the unipolar PWM scheme used to drive the inverter switches. The PWM signal is generated using a continuous Up/Down counting mode register [153], and the reference sine wave was created from a sine look up table, which can be summarized in three stages. The first stage is to calculate the PWM time period (P_XTPER) of these signals. This is done using the follow equation:

$$P_X TPER = \frac{F_{CY}}{F_{PWM} \times (P_X TMR\ Prescaler) \times 2} - 1 \qquad (6.1)$$

where F_{CY} is the device operating frequency, F_{PWM} is the PWM switching frequency and P_X TMR Prescaler is the PWM time base register.

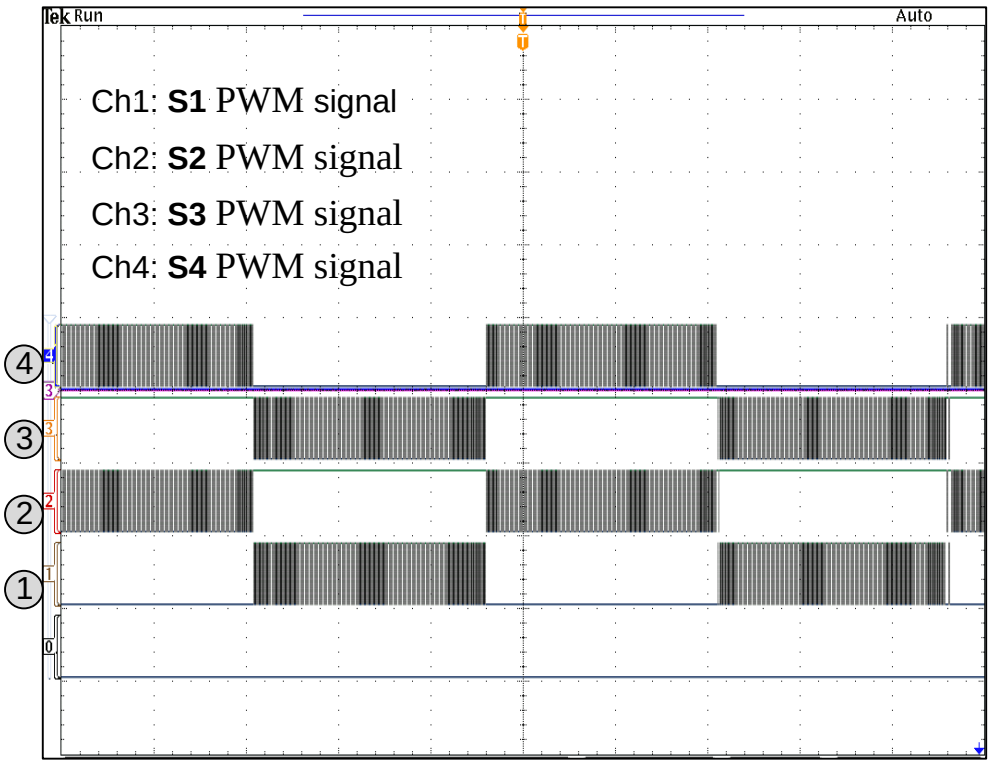


Fig. 6.6: Measure gate drive input signals, Time (4ms/div), Voltage (4V/div)

The internal clock (F_{CY}) was calculated in oscillator setup, which is equal to 40 MHz, the switching frequency F_{PWM} was selected as 20 KHz. As a result, the PWM time period (P_XTPER) from the equation above at 1:1 P_X TMR Prescaler is equal to 999.

The second stage involves selection of the PWM output mode. Fig. 6.7 shows the PWM module producing center-aligned PWM signals

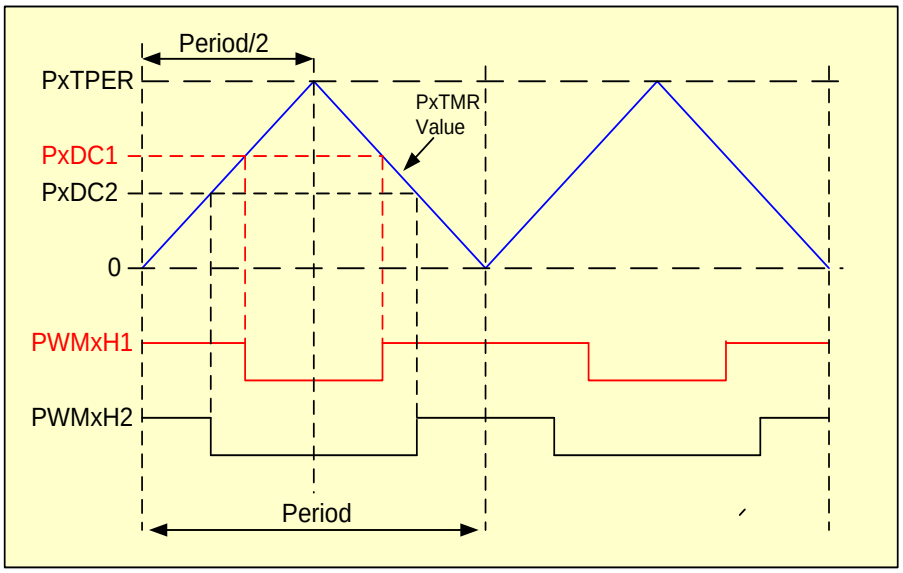


Fig. 6.7: Centre-aligned PWM module

The third stage sets the PWM dead time control, which is divided into two parts. The first part involves setting the dead time control register 2 (PxDTCON2), which includes two dead time assignment control bits for each PWM. For example, the dead time for complementary PWM1 (PWMxH1/PWMxL1) referred to 'dead-time-select-active' (DTS1A), was inserted before the high-side output (PWMxH1) and 'dead-time-select-inactive' (DTS1I), which was inserted before the low-side PWM output.

The second stage of the dead time range contains two units (A and B). These units are set by selecting input clock value and a 6 bit unsigned dead time count value, as shown in Fig. 6.8.

The suitable range of dead times is based on device operating frequency and input clock prescale. Also each unit of dead time can be select through the clock prescaler independently, such as Dead Time Unit A Prescale Select (DTAPS) and Dead Time

Unit B Prescale Select (DTBPS) in the Dead Time Control Register 1 (PxDTCON1). The following equation was used to calculate the dead time DT.

$$DT = \frac{Dead\ Time\ Range}{Prescale\ Value * T_{CY}} \tag{6.2}$$

where, Dead Time (DT) ranges between 25 ns – 1.6µs @ T_{CY} (F_{CY}) = 25ns (40 MHz) and prescaler = 1, otherwise DT ranges between 10 ns – 7µs @ T_{CY} (F_{CY}) = 25ns (40 MHz) and Prescaler = 4

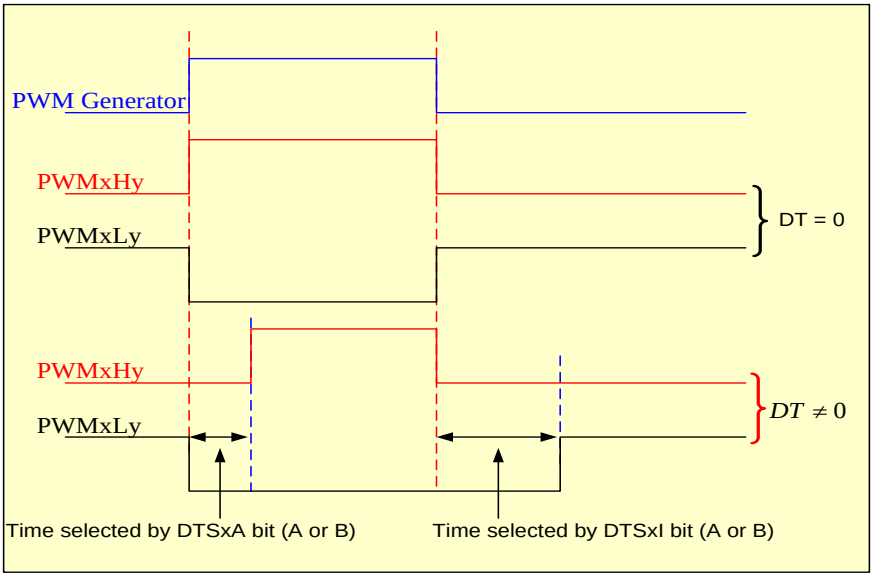


Fig. 6.8: Dead time setting

6.2.5 Analogue to Digital Converter Signal

The inverter is controlled with a Microchip dsPIC33FJ128MC706 microcontroller. The 10-bit ADC was used to sample the sensor signals at 20 kHz sampling frequency. For diagnostic purposes these signals are recorded in an array and represented via a Data Monitor Control Interface (DMCI). This technique is a powerful tool for watching the behaviour of ADC signals. Also, this technique is used to monitor the reference signal with a measured signal when tuning the PI controller and monitoring the ZCD signal when the inverter is synchronised with the grid.

6.2.6 Impact of the Noise on Analogue to Digital Signal

To reduce the noise in A/D signals the distance between the signal source and microcontroller should be short. Fig. 6.9 and Fig. 6.10 show the noise of the A/D signal and how to use co-axial cable instead of the track to minimize the noise.

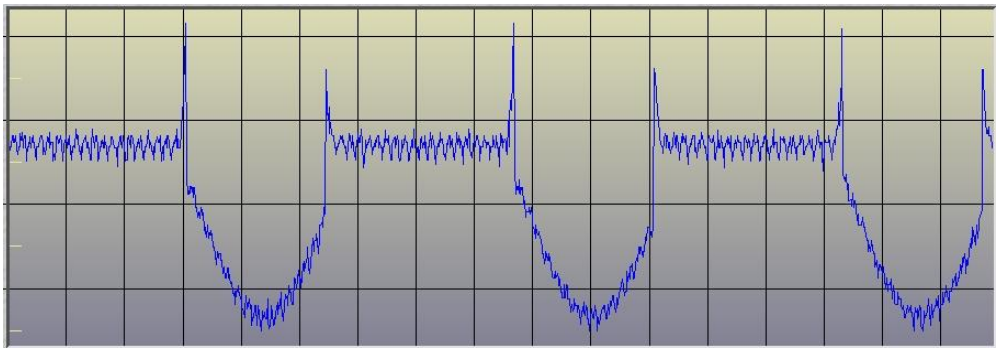


Fig. 6.9**:** A/D of output negative DC link current sensor without using a co-axial cable
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).

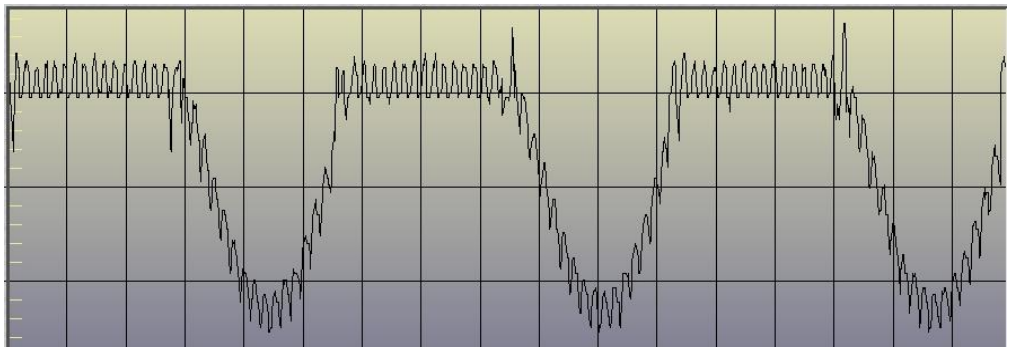


Fig. 6.10: A/D of output negative DC link current sensor with use a co-axial cable
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).

6.2.7 Impact of DC Offset Current on PWM Signal

The DC current offset can affect the PWM signal, as shown in Fig.6.11, and make the signals unsymmetrical. The result is that it will affect the waveforms of current and voltage. This effect is also represented by MATLAB SimPower by adding 0.5 offset to the reference signal, as shown in Fig. 6 12 and Fig. 6.13 .

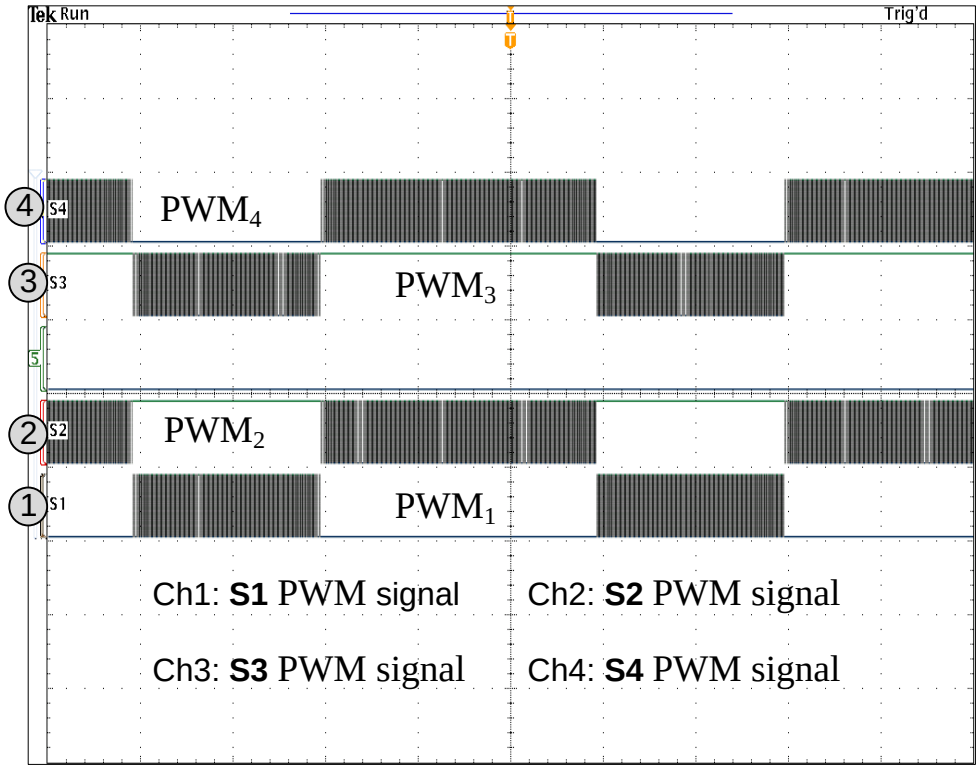


Fig.6.11: Effects of DC current in the PWM signal

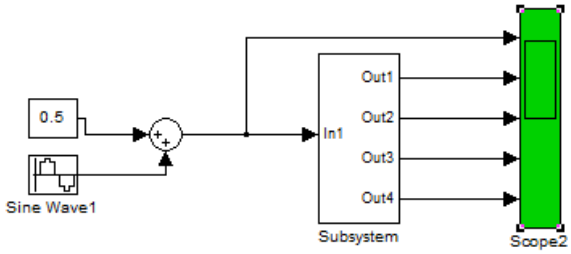


Fig. 6 12: PWM signals schematic circuit for three-level half-bridge inverter

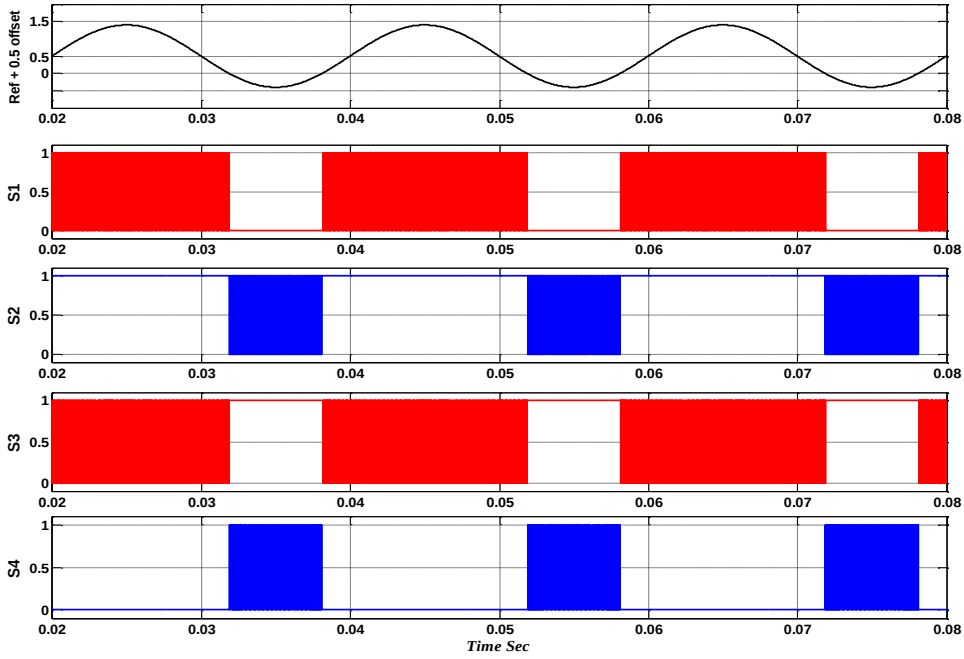


Fig. 6.13: Effects of DC current in the PWM signal at offset = 0.5

6.3 General Operation of the Three-Level Half-Bridge Inverter

In this section, the general operation and output measurement of the three-level half-bridge inverter is described. Generally, the inverter can be controlled using either the output current sensor or the DC link current sensors. In this case, control of the inverter with the output current sensor has no means of compensating for the DC offset, because it is a continuous sinusoidal waveform, and so this sensor is only used in the test circuit. However, to compensate the DC offset using the auto-calibration technique, two DC link current sensors are used, as shown in Fig. 6.14.

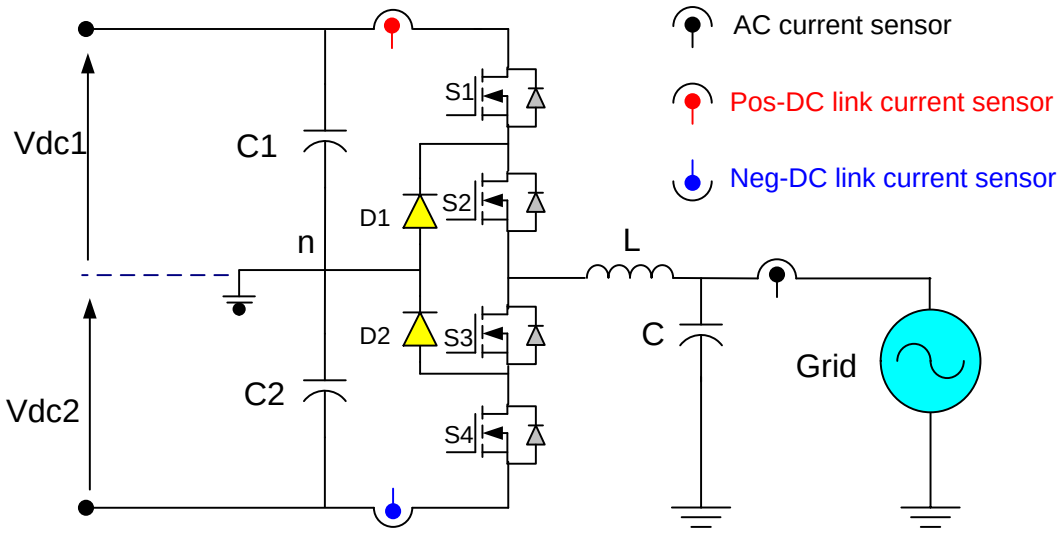


Fig. 6.14: Circuit diagram of three-level half-bridge inverter

The upper sensor is connected between C_1 and the upper switch S_1 to measure positive DC link current during the positive half of the mains cycle. The DC offset of this sensor is calibrated during the negative half cycle, when the positive DC link current drops to zero. The lower sensor is connected between C_2 and the lower switch S_4 to measure negative DC link current during the negative half cycle. In this case, the DC offset is removed during the positive half cycle when the negative DC link current drops to zero during the positive half mains cycle. Fig. 6.15 shows positive and negative DC link current measurement for grid-connected inverter over two 50Hz cycles. The two current sensor signals are connected to the analogue input pins of ADC, which are read by the microcontroller software.

The actual current measurement is taken at the centre point of the PWM cycle, where the carrier waveform reaches zero in the first half cycle of the positive DC link current sensor, and in the second half cycle of negative DC link current sensor. On the other hand, the DC offset measurement is monitored during the second half period of the positive current sensor and in the first half period in the negative current sensor. The output current measurement is estimated from the sum of positive and negative conducting loop measurements, and can then be calibrated by subtracting positive and negative DC offset loop measurements. The outcome of this measurement is then fed to a conventional PI current controller. The output of the PI controller is the modulation signal for input to the PWM unit. In summary, the

inverter output current reconstruction process is described by the flow chart shown in fig. 6.16.

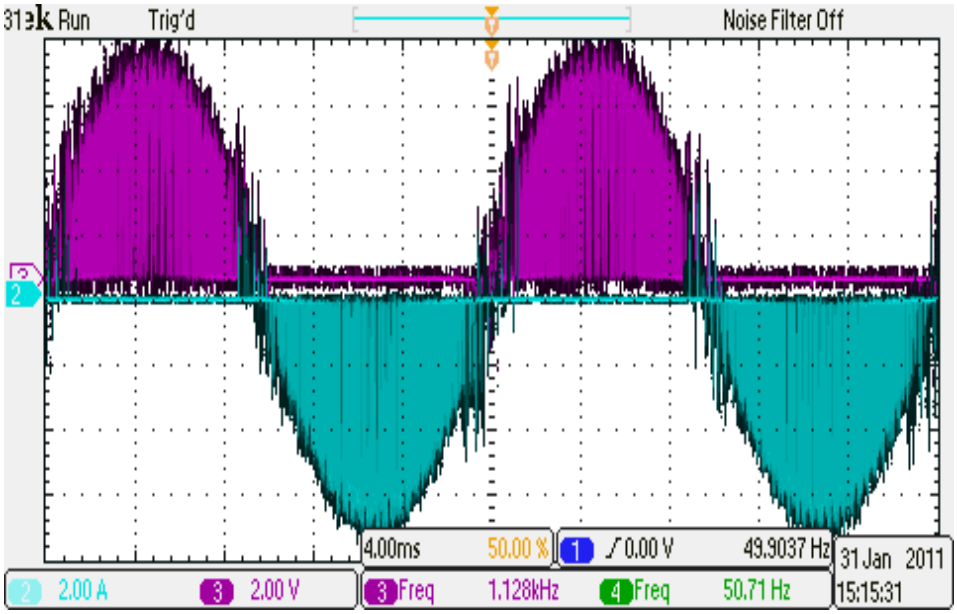


Fig. 6.15; Trace 2: Negative DC link current 2A/div and Trace3: Positive DC link current 2A/div

Compared to the single-phase H-bridge [67], the three-level half-bridge topology provides an additional advantage over the H-bridge for this application. There is no current flow in each DC link sensor for one half of a mains period. This results in plenty of time to sample the DC link current to carry out the auto-calibration function.

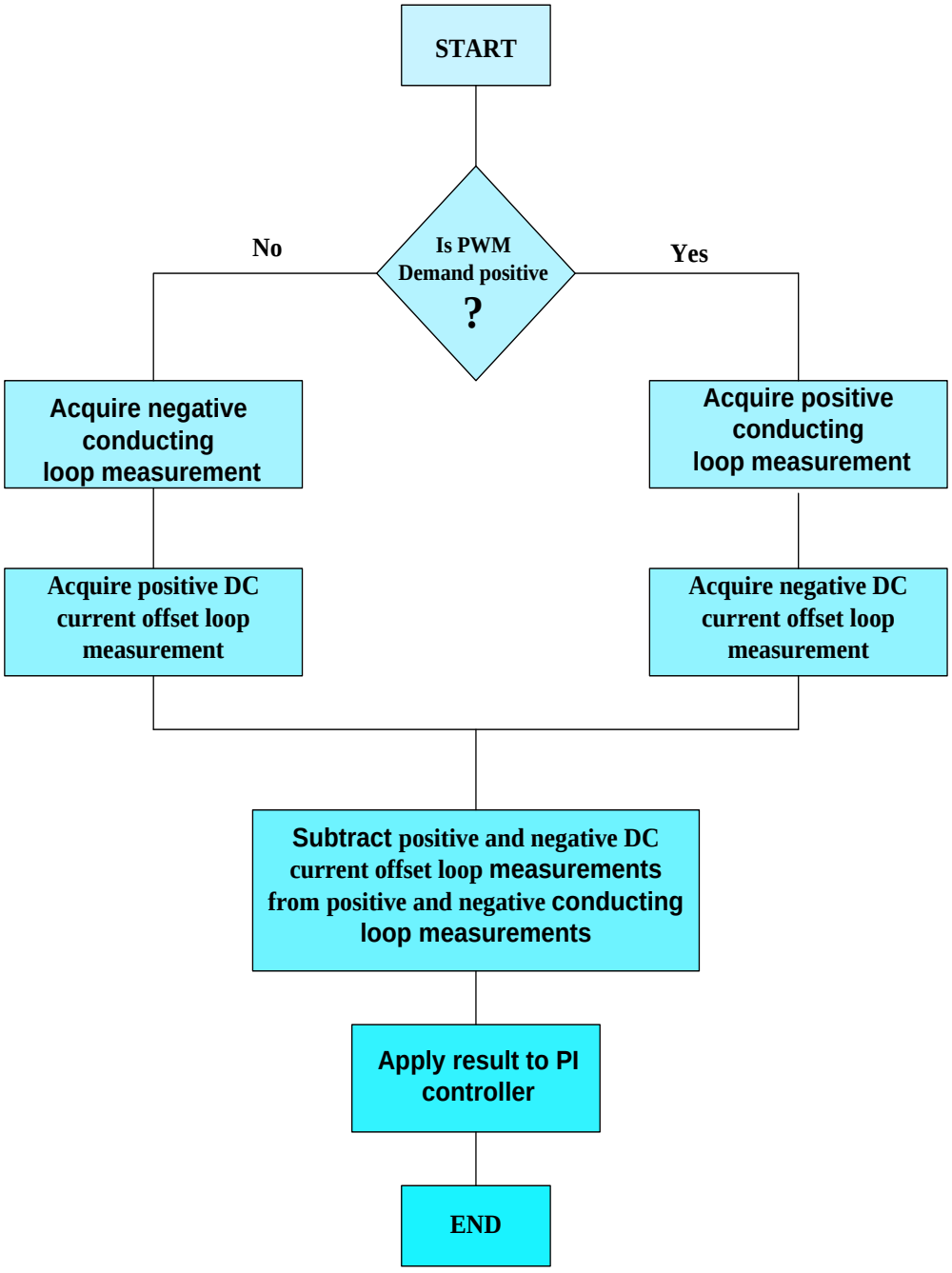


Fig. 6.16: Process of DC Link Current sensing technique

6.3.1 Three-Level Half-Bridge Inverter Measurements

The grid voltage and the inverter output voltage waveforms shown in Figs. 6.17-6.19 are measured using an isolated differential voltage probe (Tektronix P5200), and the output current and DC link current waveforms are measured using current probes (Tektronix A622 and TCP303). The measurement method of DC link current using current probe is provided in Appendix A.

The figures show grid voltage and inverter output current waveforms with related waveforms obtained under the grid connection operating condition. The first trace of Fig. 6.17 shows the ZCD signal, which is used to synchronise the inverter to the grid voltage and the second trace shows the PWM signal for switch S_1. The third and fourth traces show the grid voltage and inverter current waveforms in phase for unity power factor operation.

By looking at the waveforms in Fig. 6.17, we notice that the ZCD waveform is controlled by the rising edge of the grid voltage waveform. Also, Fig. 6.17 shows that the instantaneous frequency of grid voltage and the inverter output current are 49.97 Hz and 50 Hz respectively. This difference in frequency of grid voltage and output inverter current is attributed to three factors. The first factor is the delay of code execution time in the program. The second factor is the poor performance of the ZCD, as it only detects every half cycle. The third factor is the instantaneous change that occurred in the grid voltage frequency. Appendix A shows the cases where the output inverter current frequency lags behind the grid voltage frequency and other cases where the opposite is true, as shown in Fig. 6.17. However, in some cases, the frequencies of grid voltage and output current are very close. This value is within the nominal frequency operation, which is 50 Hz (+/- 1%) as recommended by G83/1 for all grid-connected photovoltaic installations in the United Kingdom.

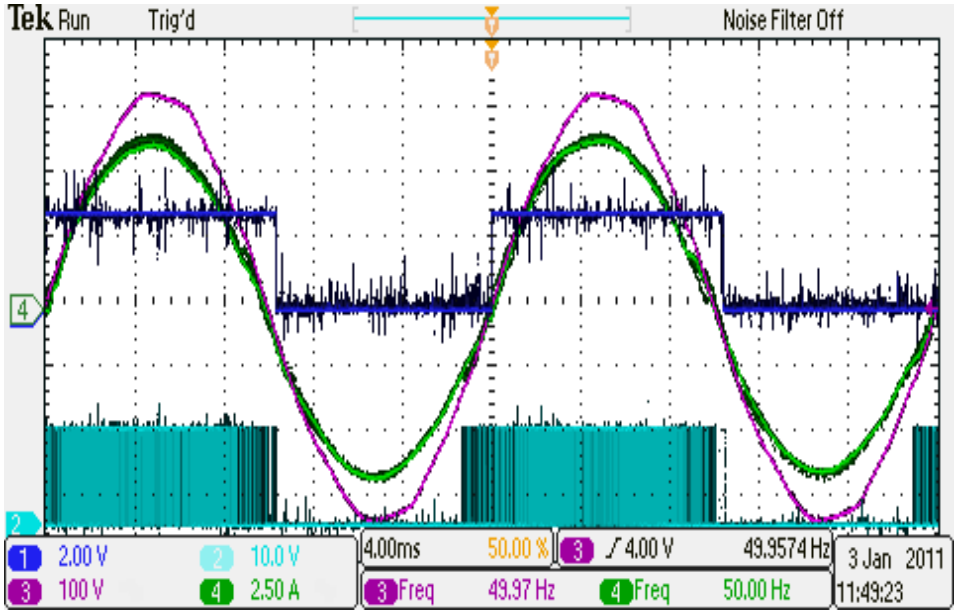


Fig. 6.17; Trace1: ZCD 2V/div, Trace2: switch1 signal 10V/div, Trace3: grid voltage 100V/div and Trace4: inverter output current 2.5 A/div

The measured positive and negative DC link currents, inverter output current and grid voltage waveforms are shown in Fig. 6.18. This figure represents the behaviour of the inverter output current, and positive and negative DC link current waveforms, where the inverter output current has the same magnitude and polarity of the positive and negative DC link current waveforms. This is significant in the three-level half-bridge inverter compared with single phase full bridge inverter when an auto-calibration technique is applied. The graph also shows the grid voltage in phase with the inverter output current. Finally, the measurement of grid voltage and inverter terminal voltage waveforms is shown in Fig. 6.19. This figure represents the PWM signals of the main switches the in three-level half-bridge inverter. S_1 controls the positive half cycle, while S_4 controls the negative half cycle.

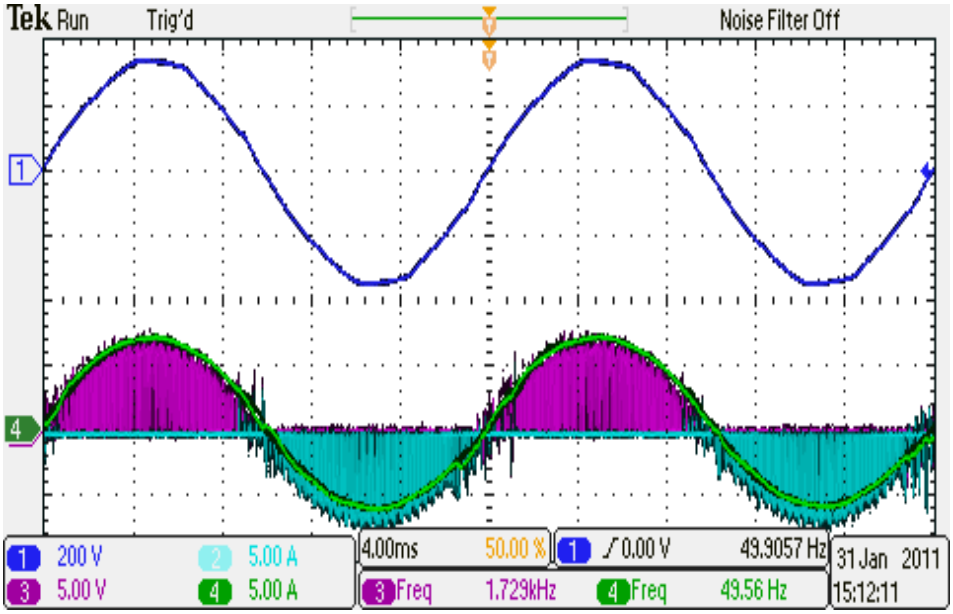


Fig. 6.18; Trace1: grid voltage 200V/div, Trace2: negative DC link current 5A/div, Trace3: positive DC link Current 5A/div and Trace4: inverter output current 5 A/div.

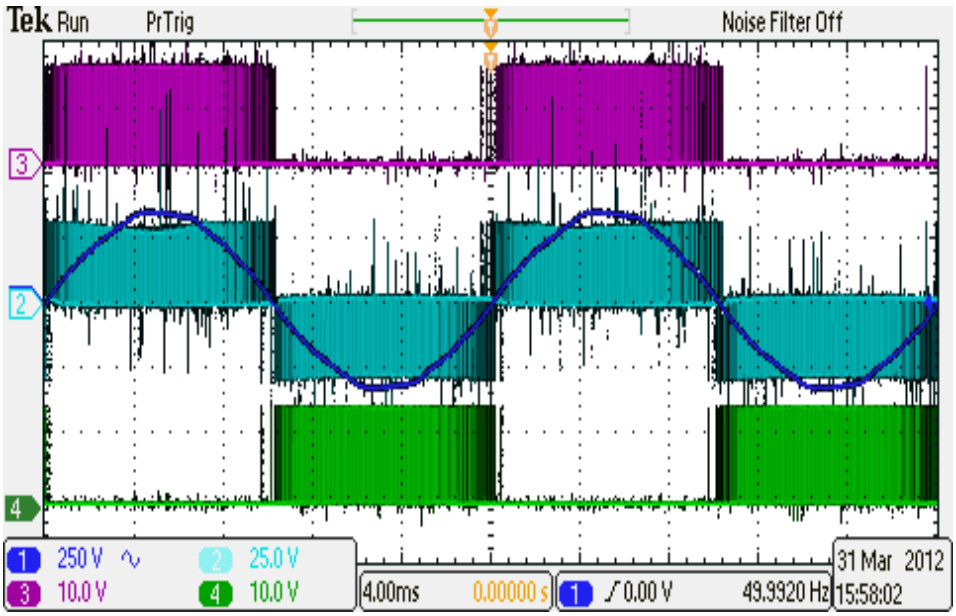


Fig. 6.19; Trace1: grid voltage 250V/div, Trace2: inverter terminal voltage 25V/div, Trace3: S_1 signal 10V/div and Trace4: S_4 10A/div.

6.4 Injection of DC Offset into the DC Current Sensors

In order to test the ability of the auto-calibration scheme to compensate for a sensor offset error, an artificial offset is applied to the current sensor output. This is achieved with a DC test current flowing in an extra primary turn through the hole in the sensor (see Fig. 6.20). This primary turn is connected in series to a DC power supply through a potentiometer and an ammeter. The multimeter is used to measure the artificial DC offset, and the potentiometer is used to introduce a variable DC sensor offset in both current transducers at the same time. When varying the DC current by varying the value of potentiometer, the result will be that both current measurements contain a DC offset depending on the value of potentiometer. In addition, Fig. 6.20 shows the direction of DC link current in each current sensor, and the direction of DC current offset.

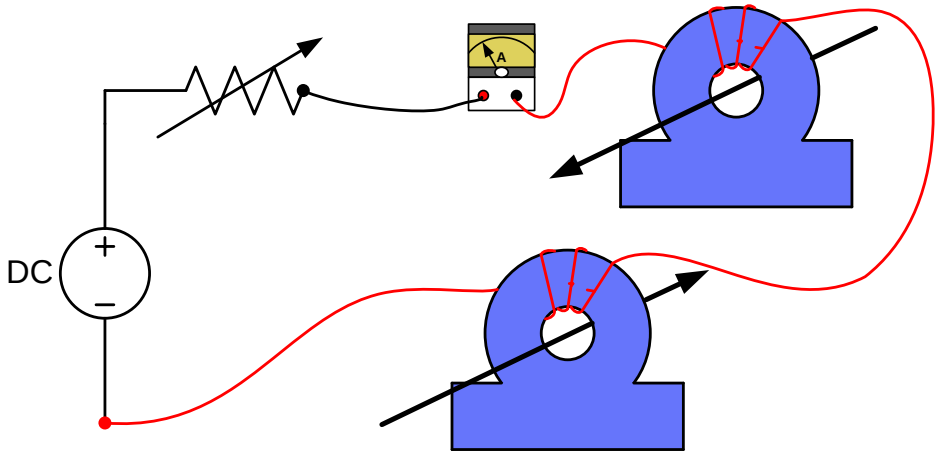


Fig. 6.20: Direction of DC link current and DC offset into Hall Effect current transducers

This additional DC current offset will affect the output waveform of the current sensors, which will be seen by the current controller. This process can be represented in a signal block diagram (Fig. 6.21). Fig. 6.22 shows a photograph of the DC offset injection circuit used in the experiment rig of the three-level half-bridge inverter.

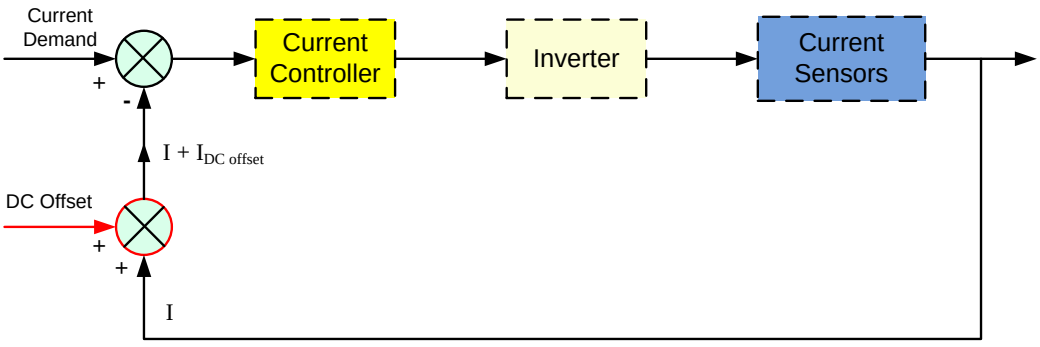


Fig. 6.21: Signal block diagram of injecting DC offset

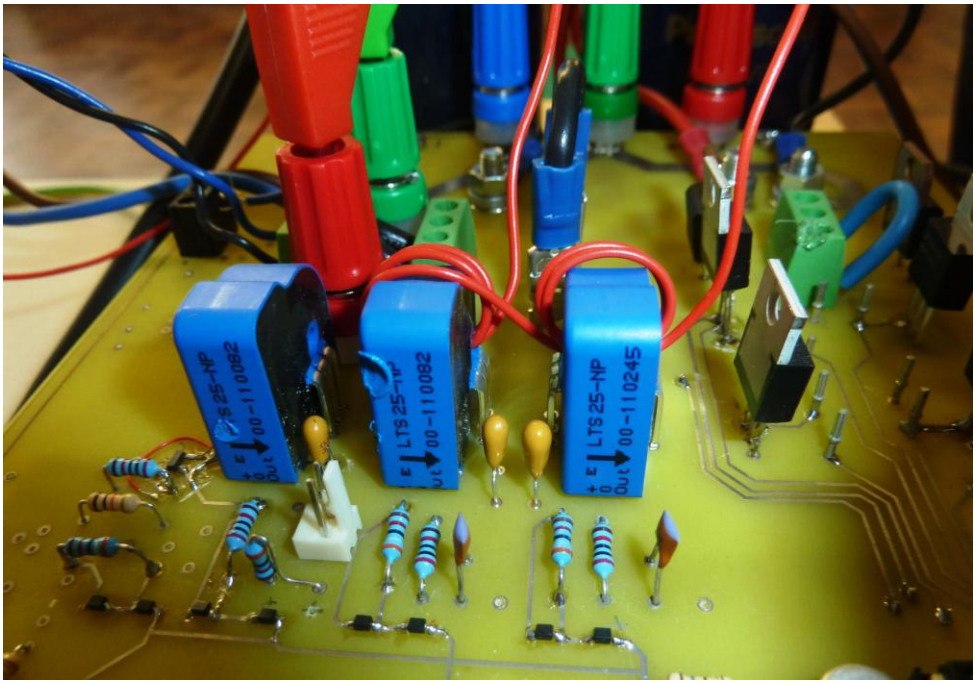


Fig. 6.22: Additional turns of cable added sensor to produce DC offset

6.4.1 Performance With, and Without, Auto-Calibration

In order to test the performance of the auto-calibration scheme, an external artificial DC injection is introduced into the current sensors. This artificial DC offset is adjusted by the potentiometer, and is increased from zero to 120mA in steps of 10mA. For comparison, the test is applied with, and without, auto-calibration engaged. The results of this test are shown in Fig. 6.23. It is clear that the auto-calibration scheme produces a significantly smaller offset error. The proposed DC link method is capable of limiting the DC component to 6.88mA in a 50Hz 5 A_{rms} inverter output current. In addition, the performance of the auto-calibration scheme can be observed clearly in analogue to digital signals, which are recorded in microcontroller memory and presented using the Data Monitor Control Interface (DMCI), as shown in Fig. 6.24 and Fig. 6.25

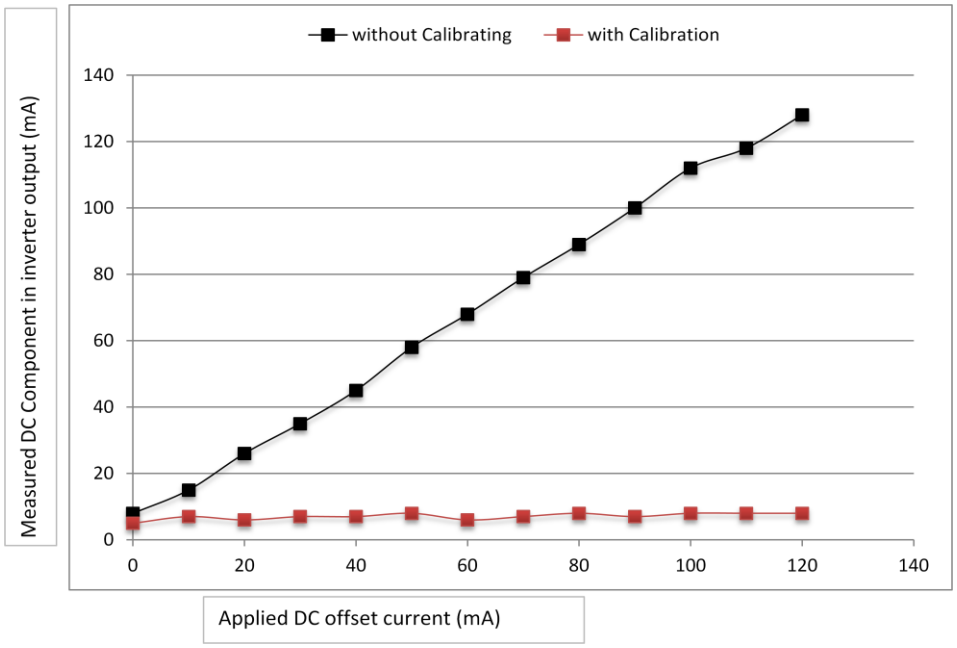


Fig. 6.23: Comparison of inverter output DC current, with and without calibration.

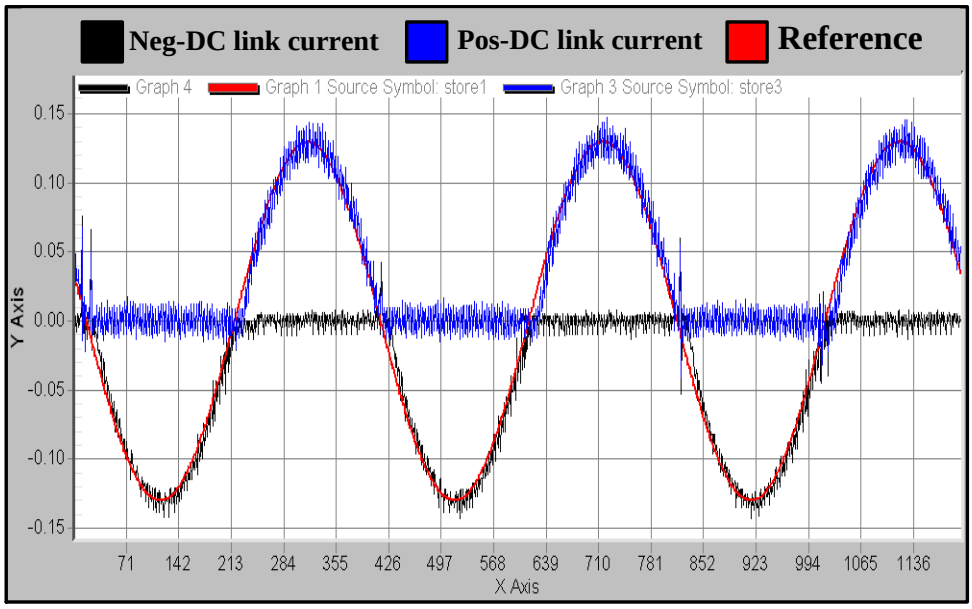


Fig. 6.24: ADC waveforms with calibration of Pos-DC link current, Neg-DC link current and Reference
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).

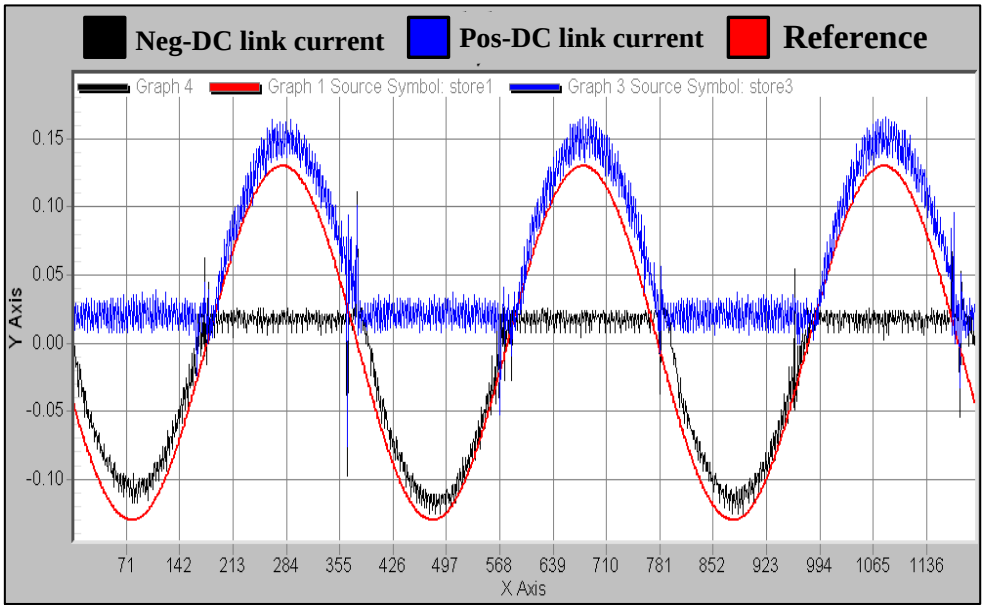


Fig. 6.25: ADC waveforms without calibration of Pos-DC link current, Neg-DC link current and Reference
X- Axis; sample number of storage array
Y- Axis; represents signed fractional logic (1, -1).

6.5 Summary

This chapter has presented the experimental results obtained from the auto-calibration DC link current sensing technique applied to a three-level half-bridge inverter. The results clearly show that the auto-calibration DC link current sensing technique is capable of compensating for the applied DC current offset for positive and negative DC link current sensors. The compensation is applied during the negative half cycle when the positive DC link current drops to zero, and for the negative DC link sensor, the compensation is applied during the positive half cycle when the negative DC link current drops to zero. It is clear that the auto-calibration scheme offers a significantly smaller offset error. The proposed DC link method is capable of limiting the DC component to 6.88mA in a 50Hz 5 A_{rms} inverter output current.

The experiments confirmed that the auto-calibration method when applied to a three-level half-bridge inverter can reduce the DC current injected into the grid. The scheme would therefore reduce the overall cost of the grid-connected inverter by avoiding the need for a 50Hz transformer. Reducing DC injection will minimize the possibility of saturation of the distribution transformer core, and reduce the effect on other distribution network equipment.

CHAPTER 7

THESIS CONCLUSION AND FURTHER WORK

7.1 Conclusion

In recent years, electrical demand has increased, along with a concomitant rise in fuel prices. This has also led to an increase in pollution and greenhouse gas emissions, caused by the burning of fossil fuels, such as gas, oil, and coal. All these factors and others made it necessary to find alternative energy sources, such as PV and wind generation systems, in what is known as distributed generation. PV energy is the cleanest power supply, and does not have moving parts. It has found wide use, and can be installed in most places, for example, roofs and windows of houses. However, the basic cost of this energy conversion technology is still high.

The research in this thesis has been focused on the development of a three-level, half-bridge transformerless grid-connected inverter that is capable of minimizing DC current injection into the grid, and so achieve the standards and guidelines of connecting to the grid without the need for an isolation transformer. If the isolation transformer is removed, the cost and size of the system will be reduced, and a higher efficiency will be obtained.

The damaging effects of DC current on distribution network equipment is explained, where the main concern centres on the distribution transformer. DC current can shift the transformer operating point, and in turn, increasing the RMS magnetizing current, which may yield additional winding losses. The second concern regarding DC current effect is in AC electrical machine drives, where the effect is similar to that in the distribution transformer. Small levels of DC current injected into the motor windings cause dynamic braking and additional losses. The final concern of DC current effect is in underground cables, where DC current injected in the ground results in stray currents in exposed metallic structures, which will adversely affect cable sheaths.

A method of minimizing DC current injection in a single-phase three-level half-bridge inverter has been presented, using auto-calibration DC link current sensing and control techniques. This technique uses two Hall Effect current sensors, the first located between the upper switches and the DC link capacitor, while the second is located on the opposite side, between the lower switches and the other DC link capacitor. Current control is achieved by using these two DC link current sensors.

Auto-calibration techniques, which are designed to deal with non-linearities and offset drift found typically in Hall Effect current sensors, can potentially provide a greater opportunity to implement transformerless grid-connected inverter systems. This is because of their high reliability and the accuracy of determining the DC components, which is essential in terms of conforming to DC current injection standards.

The experiments carried out as part of this investigation have confirmed that the auto-calibration technique gives a good result when applied to a three-level half-bridge inverter. It reduced the DC current injected into the grid without the need for a mains frequency transformer connected to the output. This technique is capable of minimizing the DC current offset in the inverter output to 6.88mA in a 50Hz, $5A_{rms}$ inverter output current, which may be compared favorably to the UK G83 recommendation, which limits this to 20mA.

The transformerless grid-connected inverter has the benefit of reducing the overall losses, and cost and size of the PV system. Moreover, preventing DC current injection into the grid, will minimize the possibility of saturation of the distribution transformer core, and reduces the effect on other distribution network equipment.

Finally, the three-level half-bridge topology provides an additional advantage over the H-bridge for transformerless grid-connected inverter. There is no current flow in each DC link sensor for one half of a mains period. This results in plenty of time to sample the DC link current, and carry out the auto-calibration function.

7.2 Further Work

The auto-calibration technique of DC link current sensing and current control applied to a three-level half-bridge inverter has minimized the DC current offset injection into the grid in compliance with the UK G83 Engineering Recommendation. Yet there are still some areas which need further investigation, such as the Total Harmonic Distortion (THD) in inverter output current waveform.

Another area for investigation is three-phase three-level grid connected inverters. Three-phase three-level inverters are widely used for the connection of renewable energy sources to the utility grid on the medium power level. The DC bus voltage on three-phase, three-level inverters is slightly less compared with three-phase inverters, and even lower compared with three-level half-bridge inverters. However, the number of components required for three-phase three-level inverters is three times that for a single-phase half-bridge inverter.

REFERENCES

[1] M. Liebreich and C. Greenwood, "Green Investing Towards a Clean Energy Infrastructure," *World Economic Forum USA Inc,* January 2009.

[2] E. Martinot and J. L. Sawin, "Renewables 2011 Global Status Report," *Renewable Energy Policy Network for the 21st Century REN21 2011*.

[3] E. Martinot and J. L. Sawin, "Renewables Global Status Report; 2009 update," *Renewable Energy Policy Network for the 21st Century REN21 2011*

[4] DEPARTMENT OF TRADE AND INDUSTRY (DTI). (2007). *UK "Meeting the Energy Challenge. Awhite Paper on Energy May 2007" ISBN 978-0-10-171242-2* [www.dti.gov.uk/energy].

[5] Y. Ma, P. Yang, and H. Guo, "Distributed generation system development based on various renewable energy resources," in *Control Conference (CCC), 2011 30th Chinese*, 2011, pp. 6203-6207.

[6] K. Honghai, L. Shengqing, and W. Zhengqiu, "Discussion on advantages and disadvantages of distributed generation connected to the grid," in *International Conference on Electrical and Control Engineering (ICECE)* 2011, pp. 170-173.

[7] H. Hinz and P. Mutschler, "Voltage Source Inverters for Grid Connected Photovoltaic Applications," *2nd World Conference and Exhibition on Photovoltaic Solar Energy Conversation, Vienna,* pp. 2045 - 2048, July 1998.

[8] H. Spanggaard and F. C. Krebs, "A brief history of the development of organic and polymeric photovoltaics," *Solar Energy Materials and Solar Cells,* vol. 83, pp. 125-146, 2004.

[9] A. Jager and Waldau, "PV status report 2011; research, solar cell production and market implementation of photovoltaics," *European Commission - Joint Research Centre; Renewable Energy Unit, Italy,* July 2011.

[10] M. Suri, T. A. Huld, E. D. Dunlop, and H. A. Ossenbrink, "Potential of solar electricity generation in the European Union member states and candidate countries," *Solar Energy,* vol. 81, pp. 1295-1305, 2007.

[11] T. Huld, M. Suri, and E. D. Dunlop, "Comparison of potential solar electricity output from fixed-inclined and two-axis tracking photovoltaic modules in Europe," *Progress in Photovoltaics: Research and Applications,* vol. 16, pp. 47-59, 2008.

[12] G. M. Tina and R. Abate, "Experimental verification of thermal behaviour of photovoltaic modules," in *The 14th IEEE Mediterranean Electrotechnical Conference (MELECON).* , 2008, pp. 579-584.

[13] G. Kleiss, A. Raicu, and K. Bucher, "Temperature-dependent influence of a-Si:H cell degradation on the energy delivered under realistic reporting conditions," in *the Twenty Third IEEE Photovoltaic Specialists Conference*, 1993, pp. 896-900.

[14] T. Lepley, "Results from Arizona Public Service Company's Star Center," in *Photovoltaic Specialists Conference, 1990., Conference Record of the Twenty First IEEE,* 1990, pp. 903-908 vol.2.

[15] J. H. R. Enslin, M. S. Wolf, D. B. Snyman, and W. Swiegers, "Integrated photovoltaic maximum power point tracking converter," *Industrial Electronics, IEEE Transactions on,* vol. 44, pp. 769-773, 1997.

[16] P. Roth, A. Georgiev, and H. Boudinov, "Cheap two axis sun following device," *Energy Conversion and Management,* vol. 46, pp. 1179-1192, 2005.

[17] B. Lindgren, "Topology For Decentralised Solar Inverters With a Low Voltage AC Bus," *(EPE'99) 8th European Conference on Power Electronics and Applications, Lausanne, Switzerland,* pp. P.1-P.10, September 1999.

[18] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC-DC Converter Photovoltaic Systems: Power Optimization Issues," *IEEE Transactions on Industrial Electronics,,* vol. 58, pp. 403-411, February 2011.

[19] H. Haeberlin, " Evolution of inverters for grid connected systems from 1989 to 2000," *17th European Photovoltaic Solar Energy Conference,* Oct 2001.

[20] F. Schimpf and L. E. Norum, "Grid connected converters for photovoltaic state of the art, ideas for improvement of transformerless inverters," *Nordic Workshop on Power and Industrial Electronics,* June 2008.

[21] H.-s. Kim, J.-H. Kim, B.-D. Min, D.-W. Yoo, and H.-J. Kim, "A highly efficient PV system using a series connection of DC-DC converter output with a photovoltaic panel," *Renewable Energy,* vol. 34, pp. 2432-2436, 2009.

[22] T. Esram and P. L. Chapman, "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques," *Energy Conversion, IEEE Transactions on,* vol. 22, pp. 439-449, 2007.

[23] C. Jaen, C. Moyano, X. Santacruz, J. Pou, and A. Arias, "Overview of maximum power point tracking control techniques used in photovoltaic systems," in *15th IEEE International Conference on Electronics, Circuits and Systems (ICECS)* 2008, pp. 1099-1102.

[24] T. Kamezawa, M. Hirakata, M. Ohsato, T. Shimizu, G. Kimura, N. Ito, S. Fukao, N. Sunaga, M. Tsunoda, and K. Muro, "Photovoltaic system with generation control circuit," in *Industrial Technology, 1996. (ICIT '96), Proceedings of The IEEE International Conference on,* 1996, pp. 242-246.

[25] R. W. Wall, "Simple methods for detecting zero crossing," in *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE,* 2003, pp. 2477-2481 Vol.3.

[26] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *Industrial Electronics, IEEE Transactions on,* vol. 53, pp. 1398-1409, 2006.

[27] A. Timbus, R. Teodorescu, F. Blaabjerg, and M. Liserre, "Synchronization Methods for Three Phase Distributed Power Generation Systems. An Overview and Evaluation," in *Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th,* 2005, pp. 2474-2481.

[28] W. Y. Teoh and C. W. Tan, "An overview of islanding detection methods in photovoltaic systems," *World Academy of Science, Engineering and Technology 58 2011,* pp. 674 - 682, 2011.

[29] H. N. Aghdam, N. Ghadimi, P. Farhadi, F. Hashemi, and R. Ghadimi, "Detecting the anti-islanding protection based on combined changes of active and reactive output powers of distributed generations," in *3rd International Conference on Computer Research and Development (ICCRD)* 2011, pp. 285-289.

[30] G. A. Kern, "SunSine300, utility interactive AC module anti-islanding test results," in *Conference Record of the Twenty-Sixth IEEE on Photovoltaic Specialists Conference* 1997, pp. 1265-1268.

[31] A. Kitamura, F. Yamamoto, and H. Matsuda, "Test results on dc injection phenomenon of grid connected PV system at Rokko Test Center," in *Conference Record of the IEEE Photovoltaic Specialists Conference*, 1996, pp. 1377-1379.

[32] E. Winfried and H. Weiss, "Photovoltaic power conversion with efficiency weight optimisation," in *Industrial Technology, 2003 IEEE International Conference on*, 2003, pp. 1166-1168 Vol.2.

[33] L. Gertmar, P. Karlsson, and O. Samuelsson, "On DC injection to AC grids from distributed generation," in *Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 10 pp.-P.10.

[34] U. o. Strathclyde. (June 2005). *DC injection into low voltage AC networks, DTI commissioned report*.

[35] V. Salas, E. OliÌ • as, M. Alonso, and F. Chenlo, "Overview of the legislation of DC injection in the network for low voltage small grid-connected PV systems in Spain and other countries," *Renewable and Sustainable Energy Reviews*, vol. 12, pp. 575-583, 2008.

[36] B. D. Min, J. Lee, J. H. Kim, T. J. Kim, D. W. Yoo, C. Y. Won, and H. G. Kim, "A new topology for grid-connected photovoltaic system using the converter with flat efficiency curve for all load range," in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, Orlando, FL, 2007, pp. 1250-1254.

[37] V. Salas, E. Olias, M. Alonso, F. Chenlo, and A. Barrado, "DC Current Injection Into the Network from PV Grid Inverters," in *Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference on*, 2006, pp. 2371-2374.

[38] J. M. A. Myrzik and M. Calais, "String and module integrated inverters for single-phase grid connected photovoltaic systems - a review," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 2003, p. 8 pp. Vol.2.

[39] A. E. Emanuel, D. J. Pileggi, and F. J. Levitsky, "Direct Current Generation in Single-Phase Residential Systems DC Effects and Permissible Levels," *Power Apparatus and Systems, IEEE Transactions on*, vol. PAS-103, pp. 2051-2057, 1984.

[40] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *Industry Applications, IEEE Transactions on*, vol. 41, pp. 1292-1306, 2005.

[41] L. Cristaldi, A. Ferrero, M. Lazzaroni, and R. T. Ottoboni, "A linearization method for commercial Hall-effect current transducers," *Instrumentation and Measurement, IEEE Transactions on*, vol. 50, pp. 1149-1153, 2001.

[42] H. Gilbert. (2000). *Industry consultation on grid connection of small PV systems, ETSU S/P2/00332/REP* [www.bis.gov.uk/files/file16648.pdf].

[43] "Geomagnetic disturbance effects on power systems," *Power Delivery, IEEE Transactions on*, vol. 8, pp. 1206-1216, 1993.

[44] Z. Bo, Z. Jie, Z. Rong, and H. Jinliang, "Numerical Analysis of DC Current Distribution in AC Power System Near HVDC System," *Power Delivery, IEEE Transactions on*, vol. 23, pp. 960-965, 2008.

[45] K. Masoud and G. Ledwich, "Grid Connection Without Mains Frequency Transformers," *IEEE Journal of Electrical and Electronic Engineering, Australia*, vol. 19, pp. 31-36, June 1999.

[46] A. Kitamura, F. Yamamoto, H. Matsuda, K. Akhmad, and Y. Hamakawa, "Test results on DC injection phenomenon of grid connected PV system at Rokko test center," in *Photovoltaic Specialists Conference, 1996., Conference Record of the Twenty Fifth IEEE*, 1996, pp. 1377-1379.

[47] A. Ahfock and A. J. Hewitt, "DC magnetisation of transformers," *Electric Power Applications, IEE Proceedings* -, vol. 153, pp. 601-607, 2006.

[48] L. Sang-Bin and T. G. Habetler, "An online stator winding resistance estimation technique for temperature monitoring of line-connected induction machines," *Industry Applications, IEEE Transactions on*, vol. 39, pp. 685-694, 2003.

[49] P. J. Lagace, J. L. Houle, H. Greiss, and D. Mukhedkar, "Computer aided evaluation of pipeline current near toroidal HVDC ground electrodes," *Power Delivery, IEEE Transactions on*, vol. 4, pp. 216-222, 1989.

[50] P. J. Aylott, "Stray current is for life-not just for Christmas. Stray current corrosion management strategies for DC traction systems," in *DC Traction Stray Current Control - Offer a Stray a Good Ohm? (Ref. No. 1999/212), IEE Seminar on*, 1999, pp. 7/1-7/6.

[51] J. B. Blomberg and N. Douglas, "Cable Sheath Corrosion -Causes and Mitigation," *American Institute of Electrical Engineers, Transactions of the*, vol. 54, pp. 382-387, 1935.

[52] W. G. Radley and C. E. Richards, "The corrosion of underground cables," *Electrical Engineers, Journal of the Institution of*, vol. 85, pp. 685-704, 1939.

[53] L. Tzung-Lin and C. Zong-Jie, "A transformerless interface converter for a distributed generation system," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, 2008, pp. 1704-1709.

[54] V. Salas, M. Alonso-Abella, E. Olías, F. Chenlo, and A. Barrado, "DC current injection into the network from PV inverters of <5 kW for low-voltage small grid-connected PV systems," *Solar Energy Materials and Solar Cells*, vol. 91, pp. 801-806, 2007.

[55] I. E. Agency, "PV System Installation and Grid-Interconnection Guidelines in Selected IEA countries," *Report IEA PVPS T5-04:2001,Nov 2001*.

[56] "ENERGY NETWORKS ASSOCIATION "Recommendations for the connection of small-scale embedded generators (up to 16 A per phase) in parallel with public low-voltage distribution networks, Engineering Recommendation G83/1, UK," September 2003.

[57] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems - an overview," in *IEEE International Symposium on Industrial Electronics*, Pretoria, S Afr, 1998, pp. 224-229.

[58] E. GubiÌ • a, P. Sanchis, A. UrsuÌ • a, J. LoÌ • pez, and L. Marroyo, "Ground currents in single-phase transformerless photovoltaic systems," *Progress in Photovoltaics: Research and Applications*, vol. 15, pp. 629-650, 2007.

[59] M. Calais, V. G. Agelidis, and M. S. Dymond, "A cascaded inverter for transformerless single-phase grid-connected photovoltaic systems," *Renewable Energy*, vol. 22, pp. 255-262, 2001.

[60] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *Industrial Electronics, IEEE Transactions on*, vol. PP, pp. 1-1, 2009.

[61] R. M. Fiorello and Z. M. Salameh, "Stand-alone transformerless sinusoidal inverter for PV systems," in *Applied Power Electronics Conference and Exposition, 1991. APEC '91. Conference Proceedings, 1991., Sixth Annual*, 1991, pp. 484-490.

[62] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1002-1016, 2006.

[63] T. Shimizu, O. Hashimoto, and G. Kimura, "A novel high-performance utility-interactive photovoltaic inverter system," *Power Electronics, IEEE Transactions on*, vol. 18, pp. 704-711, 2003.

[64] W. Tsai-Fu, N. Hung-Shou, H. Hui-Ming, and S. Chih-Lung, "PV Power Injection and Active Power Filtering With Amplitude-Clamping and Amplitude-Scaling Algorithms," *Industry Applications, IEEE Transactions on*, vol. 43, pp. 731-741, 2007.

[65] R. Gonzalez, J. Lopez, P. Sanchis, E. Gubia, A. Ursua, and L. Marroyo, "High-Efficiency Transformerless Single-phase Photovoltaic Inverter," in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, 2006, pp. 1895-1900.

[66] R. GonzaÌ • lez, E. GubiÌ • a, J. LoÌ • pez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 2694-2702, 2008.

[67] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, "Auto-Calibrating DC Link Current Sensing Technique for Transformerless, Grid Connected, H-Bridge Inverter Systems," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 1385-1393, 2006.

[68] W. M. Blewitt, D. J. Atkinson, J. Kelly, and R. A. Lakin, "Approach to low-cost prevention of DC injection in transformerless grid connected inverters," *Power Electronics, IET*, vol. 3, pp. 111-119, 2009.

[69] X. Guo, w. Wu, H. Gu, and G. San, "DC injection control for grid-connected inverters based on virtual capacitor concept," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on*, 2008, pp. 2327-2330.

[70] "IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems," *IEEE Std 929-2000*, p. i, 2000.

[71] A. C. Clothier and B. C. Mecrow, "Inverter topologies and current sensing methods for short pitched and fully pitched winding SR motors," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, 1999, pp. 416-423 vol.1.

[72] J. T. Boys, "Novel current sensor for PWM AC drives," *Electric Power Applications, IEE Proceedings B*, vol. 135, pp. 27-32, 1988.

[73] R. Bojoi, M. C. Caponet, G. Grieco, M. Lazzari, A. Tenconi, and F. Profumo, "Computation and measurements of the DC link current in six-phase voltage source PWM inverters for AC motor drives," in *Power Conversion Conference, 2002. PCC Osaka 2002. Proceedings of the*, 2002, pp. 953-958 vol.3.

[74] D. J. Atkinson, "Three phase bridge current controller with single sensor," *Electronics Letters*, vol. 32, pp. 1842-1843, 1996.

[75] I. M. Filanovsky and V. A. Piskarev, "Sensing and measurement of DC current using a transformer and RL-multivibrator," *IEEE transactions on circuits and systems*, vol. 38, pp. 1366-1370, 1991.

[76] F. Costa, P. Poulichet, F. Mazaleyrat, and E. Laboure, "The current sensors in power electronics, a review," *EPE JOURNAL*, vol. 1, pp. 7-18, 2001.

[77] R. Sharma, "Removal of DC offset current from transformerless PV inverters connected to utility," presented at the 40th International Universities Power Engineering Conference (UPEC 2005), Cork, Ireland, 2005.

[78] T. L. Ahfock and L. Bowtell, "DC offset elimination in a single-phase grid-connected photovoltaic system," presented at the AUPEC 2006, Melbourne, Australia, 2006.

[79] G. Buticchi, G. Franceschini, E. Lorenzani, C. Tassoni, and A. Bellini, "A novel current sensing DC offset compensation strategy in transformerless grid connected power converters," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 3889-3894.

[80] W. F. Ray and C. R. Hewson, "High performance Rogowski current transducers," in *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, 2000, pp. 3083-3090 vol.5.

[81] *"Isolated current and voltage transducers Characteristics - Applications – Calculations", LEM, Applications Guide, available at* [www.lem.com].

[82] S. Ziegler, R. C. Woodward, H. H. C. Iu, and L. J. Borle, "Current Sensing Techniques: A Review," *Sensors Journal, IEEE*, vol. 9, pp. 354-376, 2009.

[83] L. Ghislanzoni and J. A. Carrasco, "A DC current transformer for large bandwidth and high common-mode rejection," *Industrial Electronics, IEEE Transactions on*, vol. 46, pp. 631-636, 1999.

[84] "IEEE Guide for the Application of Current Transformers Used for Protective Relaying Purposes," *IEEE Std C37.110-2007 (Revision of Std C37.110-1996)*, pp. C1-67, 2008.

[85] Y. C. Kang, J. K. Park, S. H. Kang, A. T. Johns, and R. K. Aggarwal, "An algorithm for compensating secondary currents of current transformers," *Power Delivery, IEEE Transactions on*, vol. 12, pp. 116-124, 1997.

[86] N. Locci and C. Muscas, "A digital compensation method for improving current transformer accuracy," *Power Delivery, IEEE Transactions on*, vol. 15, pp. 1104-1109, 2000.

[87] Y. C. Kang, S. H. So, T. Y. Zheng, S. I. Jang, Y. G. Kim, and Y. S. Lyu, "Compensating Algorithm for a Measurement CT Considering the Effects of the Hysteresis Characteristics," in *Developments in Power System Protection, 2008. DPSP 2008. IET 9th International Conference on*, 2008, pp. 556-561.

[88] L. Kojovic, "Rogowski coils suit relay protection and measurement [of power systems]," *Computer Applications in Power, IEEE*, vol. 10, pp. 47-52, 1997.

[89] W. F. Ray and R. M. Davis, "Wide bandwidth Rogowski current transducers : Part 1 - The Rogowski coil," *EPE journal*, vol. 3, pp. 51-59, March 1993.

[90] W. F. Ray, "Wide bandwidth Rogowski current transducers : Part 2 - The integrator " *EPE Journal*, vol. 3, pp. 116-122, June 1993.

[91] *Precision Current Sense Resistors, TGHG Series, Applications Guide, available at* [www.ohmite.com].

[92] L. A. Bowtell and A. L. Ahfock, "Dynamic analysis of a DC offset controller for grid-connected inverters," in *Universities Power Engineering Conference (AUPEC), 2010 20th Australasian*, 2010, pp. 1-5.

[93] L. Bowtell and A. Ahfock, "Direct current offset controller for transformerless single-phase photovoltaic grid-connected inverters," *Renewable Power Generation, IET*, vol. 4, pp. 428-437, 2010.

[94] T. Sonoda, R. Ueda, and K. Koga, "An AC and DC current sensor of high accuracy," *Industry Applications, IEEE Transactions on*, vol. 28, pp. 1087-1094, 1992.

[95] *High precision current transducers, LEM, Applications Guide, available at;* [www.lem.com].

[96] C. Ying, Q. Chang, M. L. Crow, S. Pekarek, and S. Atcitty, "A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM With Energy Storage," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1512-1521, 2006.

[97] L. M. Tolbert, P. Fang Zheng, and T. G. Habetler, "Multilevel converters for large electric drives," *Industry Applications, IEEE Transactions on*, vol. 35, pp. 36-44, 1999.

[98] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing Renewable Energy Sources to the Utility Grid Using a Three-Level Inverter," *Industrial Electronics, IEEE Transactions on*, vol. 53, pp. 1504-1511, 2006.

[99] B. M. Han and P. Mattavelli, "Operation analysis of novel UPFC based on 3-level half-bridge modules," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 2003, p. 6 pp. Vol.4.

[100] H. B. Zhang, S. J. Finney, A. M. Massoud, J. E. Fletcher, and B. W. Williams, "Operation of a three-level NPC active power filter with unbalanced and nonlinear loads," in *Power Electronics, Machines and Drives, 2008. PEMD 2008. 4th IET Conference on*, 2008, pp. 22-26.

[101] R. H. Baker and L. H. Bannister, "Electric Power Converter," U.S Patent 3 867 643, Feb. 1975.

[102] J. RodriÌ • guez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 724-738, 2002.

[103] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE*, 1991, pp. 96-103.

[104] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *Industry Applications, IEEE Transactions on*, vol. IA-19, pp. 1057-1069, 1983.

[105] E. Cengelci, S. U. Sulistijo, B. O. Woo, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A new medium voltage PWM inverter topology for adjustable speed drives," in *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE*, 1998, pp. 1416-1423 vol.2.

[106] L. Poh Chiang, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *Industry Applications, IEEE Transactions on*, vol. 39, pp. 1386-1395, 2003.

[107] A. Nabae, I. Takahashi, and H. Akagi, "New neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, pp. 518-523, 1981.

[108] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, 1992, pp. 397-403 vol.1.

[109] J. S. Lai and F. Z. Peng, "Multilevel converters - A new breed of power converters," *IEEE Transactions on Industry Applications,* vol. 32, pp. 509-517, 1996.

[110] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *Industry Applications, IEEE Transactions on,* vol. 33, pp. 202-208, 1997.

[111] M. D. Manjrekar and T. A. Lipo, "A generalized structure of multilevel power converter," in *Power Electronic Drives and Energy Systems for Industrial Growth, 1998. Proceedings. 1998 International Conference on*, 1998, pp. 62-67 Vol.1.

[112] R. W. Menzies and Z. Yiping, "Advanced static compensation using a multilevel GTO thyristor inverter," *Power Delivery, IEEE Transactions on,* vol. 10, pp. 732-738, 1995.

[113] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," in *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE*, 1990, pp. 363-371.

[114] Y. Y. Mon, W. W. L. Keerthipala, and T. L. San, "Multi-modular multi-level pulse width modulated inverters," in *Power System Technology, 2000. Proceedings. PowerCon 2000. International Conference on*, 2000, pp. 469-474 vol.1.

[115] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, "Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode," *Industrial Electronics, IEEE Transactions on,* vol. 55, pp. 3088-3099, 2008.

[116] V. Manimala, N. Geetha, and P. Renuga, "Design and simulation of five level cascaded inverter using multilevel sinusoidal pulse width modulation strategies," in *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*, 2011, pp. 280-283.

[117] K. Corzine and Y. Familiant, "A new cascaded multilevel H-bridge drive," *Power Electronics, IEEE Transactions on,* vol. 17, pp. 125-131, 2002.

[118] D. Zhong, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "A cascade multilevel inverter using a single DC source," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 5 pp.

[119] D. Zhong, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "DC-AC Cascaded H-Bridge Multilevel Boost Inverter With No Inductors for Electric/Hybrid Electric Vehicle Applications," *Industry Applications, IEEE Transactions on,* vol. 45, pp. 963-970, 2009.

[120] M. Calais, V. G. Agelidis, L. J. Borle, and M. S. Dymond, "A transformerless five level cascaded inverter based single phase photovoltaic system," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, 2000, pp. 1173-1178 vol.3.

[121] S. Gui-Jia, "Multilevel DC-link inverter," *Industry Applications, IEEE Transactions on,* vol. 41, pp. 848-854, 2005.

[122] S. Khomfoi and N. Praisuwanna, "A hybrid cascaded multilevel inverter for interfacing with renewable energy resources," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 2912-2917.

[123] P. Panagis, F. Stergiopoulos, P. Marabeas, and S. Manias, "Comparison of state of the art multilevel inverters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 4296-4301.

[124] P. Fang Zheng, "A generalized multilevel inverter topology with self voltage balancing," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 611-618, 2001.

[125] M. Calais, V. G. Agelidis, and M. Meinhardt, "Multilevel converters for single-phase grid connected photovoltaic systems: an overview," *Solar Energy*, vol. 66, pp. 325-335, 1999.

[126] F.-s. Kang, S. E. Cho, S.-J. Park, C.-U. Kim, and T. Ise, "A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system," *Solar Energy*, vol. 78, pp. 727-738, 2005.

[127] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *Industry Applications, IEEE Transactions on*, vol. 36, pp. 834-841, 2000.

[128] M. R. Pavan Kumar and J. M. S. Kim, "Current control of a hybrid multilevel switiching converter," in *Power Electronics, Drives and Energy Systems for Industrial Growth, 1996., Proceedings of the 1996 International Conference on*, 1996, pp. 346-352 vol.1.

[129] S. Byeong-Mun, K. Juhyung, L. Jih-Sheng, S. Ki-Chul, K. Hae-Jong, and P. Sun-Soon, "A multilevel soft-switching inverter with inductor coupling," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 628-636, 2001.

[130] T. L. Grant and T. H. Barton, "Control Strategies for PWM Drives," *Industry Applications, IEEE Transactions on*, vol. IA-16, pp. 211-216, 1980.

[131] L. Yo-Han, K. Rae-Young, and H. Dong-Seok, "A novel SVPWM strategy considering DC-link balancing for a multi-level voltage source inverter," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, 1999, pp. 509-514 vol.1.

[132] S. R. Bowes and B. M. Bird, "Novel approach to the analysis and synthesis of modulation processes in power convertors," *Electrical Engineers, Proceedings of the Institution of*, vol. 122, pp. 507-513, 1975.

[133] S. R. Bowes and M. J. Mount, "Microprocessor control of PWM inverters," *Electric Power Applications, IEE Proceedings B*, vol. 128, pp. 293-305, 1981.

[134] S. R. Bowes and J. Clare, "Steady-state performance of PWM inverter drives," *Electric Power Applications, IEE Proceedings B*, vol. 130, pp. 229-244, 1983.

[135] S. R. Bowes and R. Bullough, "Steady-state performance of current-fed pulse-width-modulated inverter drives," *Electric Power Applications, IEE Proceedings B*, vol. 131, pp. 113-132, 1984.

[136] S. R. Bowes and A. Midoun, "Suboptimal switching strategies for microprocessor-controlled PWM inverter drives," *Electric Power Applications, IEE Proceedings B*, vol. 132, pp. 133-148, 1985.

[137] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design* 2nd ed.: John Wiley & Sons, 1995.

[138] R. Sharma and J. A. R. Ball, "Unipolar switched inverter low-frequency harmonics caused by switching delay," *Power Electronics, IET*, vol. 2, pp. 508-516, 2009.

[139] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *Power Electronics, IEEE Transactions on,* vol. 7, pp. 497-505, 1992.

[140] M. S. Aspalli and A. Wamanrao, "Sinusoidal pulse width modulation (SPWM) with variable carrier synchronization for multilevel inverter controllers," in *Control, Automation, Communication and Energy Conservation, 2009. INCACEC 2009. 2009 International Conference on*, 2009, pp. 1-6.

[141] B. Velaerts, P. Mathys, E. Tatakis, and G. Bingen, "A novel approach to the generation and optimization of three-level PWM wave forms for induction motor inverters," in *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE*, 1988, pp. 1255-1262 vol.2.

[142] M. Armstrong, D. J. Atkinson, C. M. Johnson, and T. D. Abeyasekera, "Low order harmonic cancellation in a grid connected multiple inverter system via current control parameter randomization," *Power Electronics, IEEE Transactions on,* vol. 20, pp. 885-892, 2005.

[143] A. Maknouninejad, N. Kutkut, I. Batarseh, Q. Zhihua, and E. Shoubaki, "Detailed analysis of inverter linear control loops design," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, 2011, pp. 1188-1193.

[144] M. J. Ryan and R. D. Lorenz, "A synchronous-frame controller for a single-phase sine wave inverter," in *Applied Power Electronics Conference and Exposition, 1997. APEC '97 Conference Proceedings 1997., Twelfth Annual*, 1997, pp. 813-819 vol.2.

[145] T. Tsang-Li and C. Jian-Shiang, "UPS inverter design using discrete-time sliding-mode control scheme," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 67-75, 2002.

[146] L. Malesani and P. Tenti, "A novel hysteresis control method for current-controlled voltage-source PWM inverters with constant modulation frequency," *Industry Applications, IEEE Transactions on,* vol. 26, pp. 88-92, 1990.

[147] S. Takamatsu, E. Shimada, and T. Yokoyama, "Digital Control Method for Single Phase Utility Interactive Inverter Using Deadbeat Control with FPGA Based Hardware Controller," in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, 2006, pp. 1436-1441.

[148] M. F. Rahman, K. W. Lim, and K. S. Low, "Evaluation of an EMF injection scheme for a permanent magnet brushless DC drive," in *Industrial Electronics, 1992., Proceedings of the IEEE International Symposium on*, 1992, pp. 625-629 vol.2.

[149] S. V. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines," in *Power Electronics, 2007. ICPE '07. 7th Internatonal Conference on*, 2007, pp. 1133-1138.

[150] J. H. R. Enslin and P. J. M. Heskes, "Harmonic interaction between a large number of distributed power inverters and the distribution network," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1586-1593, 2004.

[151] M. Preindl and S. Bolognani, "Optimized design of two and three level full-scale voltage source converters for multi-MW wind power plants at different

voltage levels," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 3634-3639.

[152] B. Saban, F. L. M. Antunes, and A. Engler, "Design and Benchmark of a Multilevel Converter for Large-Scale Wind Power Systems," *European Wind Energy Conference & Exhibition*, 2007.

[153] *dsPIC33F Data Sheet,High-Performance, 16-Bit Digital Signal Controllers, 2009 Microchip Technology Inc. Avalibale at;* [www.microchip.com].

[154] (November 1999). *PCB Design Guidelines for Reduced EMI. Texas Instruments Inc. Avalible at;* [www.ti.com].

[155] *SGS-THOMSON MICROELECTRONICS "Environment design rules of MOSFETs In Medium Power Applications". Application Note. Avalible at;* [www.st.com].

[156] D. L. Jones. (2004). *PCB Design Tutorial. Avalible at;* [www.alternatezone.com].

[157] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A New Single-Phase PLL Structure Based on Second Order Generalized Integrator," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1-6.

[158] *INTERNATIONAL RECTIFIER, Application Note: AN-983, IGBT Characteristics, available at;* [www.irf.com].

[159] J. Dodge. (April 2003). *Latest Technology PT IGBTs vs. Power MOSFETs, Advanced Power Technology Research Paper, Available at:* [www.microsemi.com].

[160] *HCPL-3180 2Amp Output Current, High Speed IGBT/MOSFET Gate Drive Optocoupler, Avago Technologies, available at;* [www.avagotech.com].

AUTHOR PUBLICATION

"Minimisation of DC current component in transformerless Grid-connected PV inverter application"

Published in *Environment and Electric Engineering (IEEEC), 2011 10th International Conference*, 2011,pp1-4

"A Review of Minimisation of Output DC Current Component Methods in Single-Phase Grid-Connected Inverters PV Applications"

Published in *2nd International Symposium on Environment-Friendly Energies and Applications (EFEA 2012)*

APPENDIX A:

A.1. Measurement of DC link current

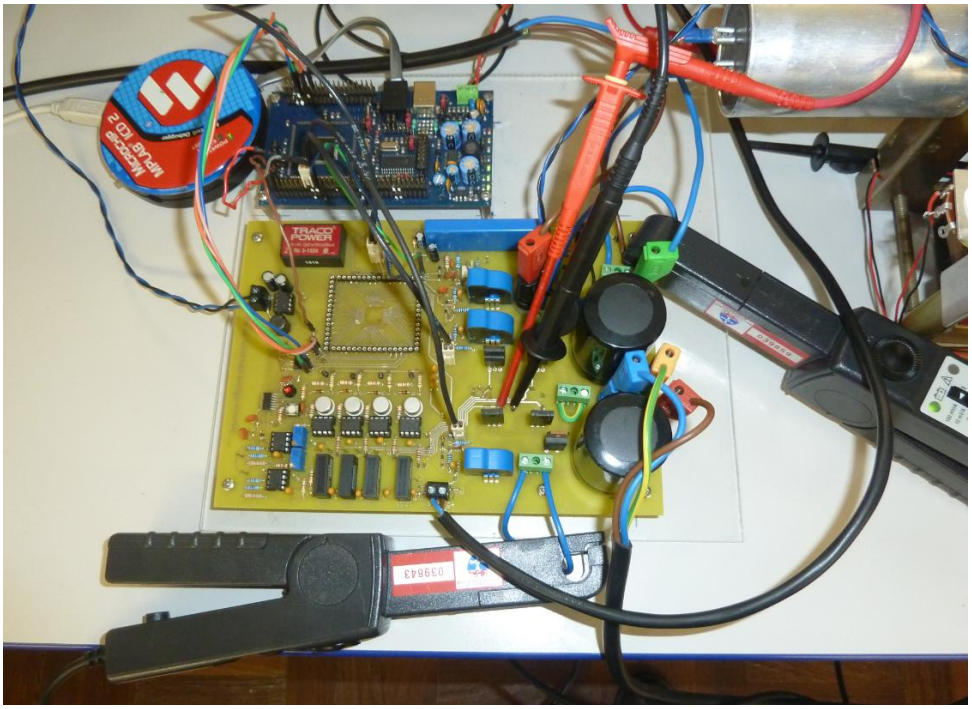


Fig. A1: measurement of DC link current in both side

A.2. Numeric Formats

A. 2.1 Integer and Fractional Data

The dsPIC33F devices support both integer and fractional data types. Integer data is inherently represented as a signed two's complement value, where the most significant bit is defined as a sign bit. For a 16-bit integer, the data range is -32768 (0x8000) to 32767 (0x7FFF), including 0.

Fractional data is represented as a two's complement number, where the most significant bit is defined as a sign bit, and the radix point is implied to lie just after the sign bit. This format is commonly referred to as 1.15 (or Q15) format, where 1 is the number of bits used to represent the integer portion of the number, and 15 is the

number of bits used to represent the fractional portion. For a 16-bit fraction, the 1.15 data range is -1.0 (0x8000) to 0.999969482 (0x7FFF), including 0.

Tables A.1-A.2 show the numerical equivalent codes for 10-bit and 12-bit modes

Table A.1: Numerical Equivalents Codes for (10-bit Mode)

VIN/VREF	**10-bit Output Code**	**16-bit Integer Format**	**16-bit Signed Integer Format**	**16-bit Fractional Format**	**16-bit Signed Fractional Format**
1023/1024	11 1111 1111	0000 0011 1111 1111 = 1023	0000 0001 1111 1111 = 511	1111 1111 1100 0000 = 0.999	0111 1111 1100 0000 = 0.499
1022/1024	11 1111 1110	0000 0011 1111 1110 = 1022	0000 0001 1111 1110 = 5 10	1111 1111 1000 0000 = 0.998	0111 1111 1000 0000 = 0.498
…					
513/1024	10 0000 0001	0000 0010 0000 0001 = 513	0000 0000 0000 0001 = 1	1000 0000 0100 0000 = 0.501	0000 0000 0100 0000 = 0.001
512/1024	10 0000 0000	0000 0010 0000 0000 = 512	0000 0000 0000 0000 = 0	1000 000 0000 0000 = 0.500	0000 0000 0000 0000 = 0.000
511/1024	01 1111 1111	0000 0001 1111 1111 = 511	1111 1111 1111 1111 = -1	0111 1111 1100 0000 = 0.499	0000 0000 0000 0000 = 0.001
…					
1/1024	00 0000 0001	0000 0000 0000 0001 = 1	1111 1110 0000 0001 = -511	0000 0000 0100 0000 = 0.001	1000 0000 0100 0000 = -0.499
0/1024	00 0000 0000	0000 0000 0000 0000 = 0	1111 1110 0000 0000 = -512	0000 0000 0000 0000 = 0.000	1000 0000 0000 0000 = -0.500

Table A.2: Numerical Equivalents Codes for (12-bit Mode)

VIN/VREF	**12-bit Output Code**	**16-bit Integer Format**	**16-bit Signed Integer Format**	**16-bit Unsigned Fractional Format**	**16-bit Signed Fractional Format**
4095/4096	1111 1111 1111	0000 1111 1111 1111 = 4095	0000 0111 1111 1111 = 2047	1111 1111 1111 0000 = 0.9998	0111 1111 1111 0000 = 0.9995
4094/4096	1111 1111 1110	0000 1111 1111 1110 = 4094	0000 0111 1111 1110 = 2046	1111 1111 1110 0000 = 0.9995	0111 1111 1110 0000 = 0.9990
…					
4049/4096	1000 0000 0001	0000 1000 0000 0001 = 4049	0000 0000 0000 0001 = 1	1000 0000 0001 0000 = 0.5002	0000 0000 0001 0000 = 0.0005
4048/4096	1000 0000 0000	0000 1000 0000 0000 = 2048	0000 0000 0000 0000 = 0	1000 000 0000 0000 = 0.500	0000 0000 0000 0000 = 0.000
4047/4096	0111 1111 1111	0000 0111 1111 1111 = 2047	1111 1111 1111 1111 = -1	0111 1111 1111 0000 = 0.4998	1111 1111 1111 0000 = 0.0005
…					
1/4096	0000 0000 0001	0000 0000 0000 0001 = 1	1111 1000 0000 0001 = -2047	0000 0000 0001 0000 = 0.0002	1000 0000 0001 0000 = -0.9995
0/4096	0000 0000 0000	0000 0000 0000 0000 = 0	1111 1000 0000 0000 = -2048	0000 0000 0000 0000 = 0.000	1000 0000 0000 0000 = -1.000

A.3. **Interrupt Service Routines (ISRs) C Code**

A.4. **Instantaneous Change of Frequency**

As mentioned earlier in section 6.3.1 the instantaneous change of frequency in the inverter output is due to the low performance of zero crossing detector which is because it only gives an indication once in half cycle. As well as the instantaneous change in grid voltage within the permissible limits, these factors are causing the change in frequency and non-conformity to each other. But including the standard limit [56] see Figs. A.2-3.

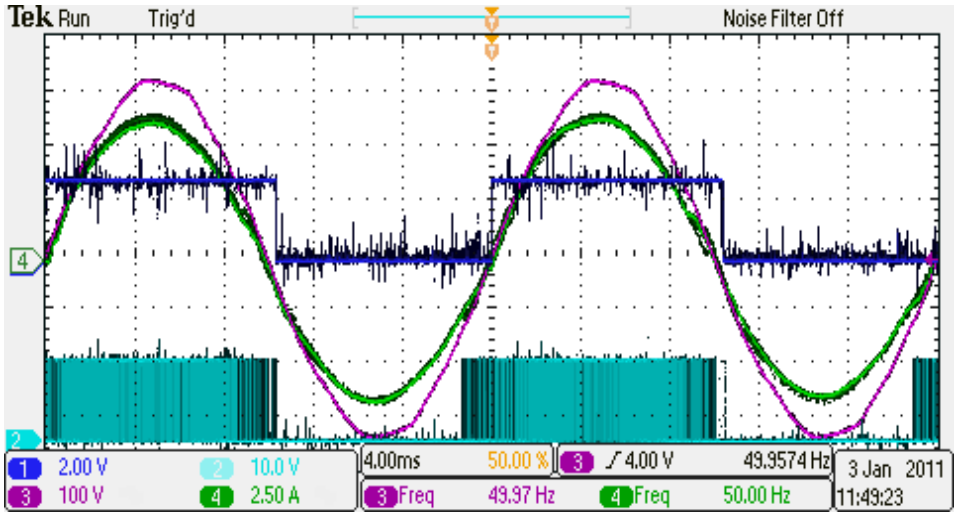


Fig. A.2.

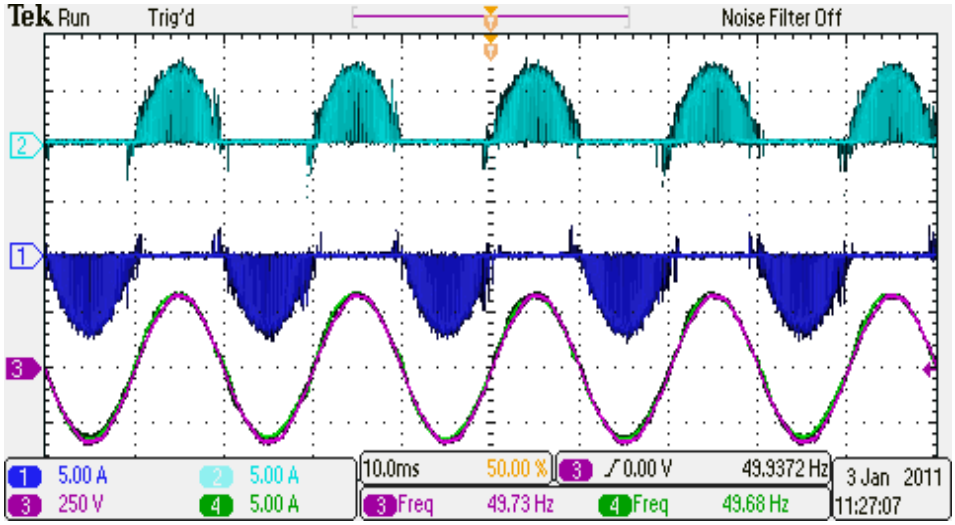


Fig. A.3: